Micro Processors and Interfacing (EEE F241)

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI
K.K. BIRLA GOA CAMPUS

Design assignment on Building an IC Tester

Submitted to Dr. K.R. Anupama

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BATCH NO::81

OBJECTIVE:

Design a Microprocessor based Tester to test the logical functioning of the following chips: (i) 7400 (ii) 7402 (iii) 7410 The IC to be tested will be inserted in a 14 pin ZIF socket. The IC number is to be entered via a keyboard. The keyboard has keys 0-9, backspace, enter and test. The user places the IC in the ZIF socket closes it - then enters the IC No, followed by enter key. The IC No. is displayed on the 7-segment display. The testing will start once the user presses test key. After Test the result PASS/FAIL must be displayed on the 7-segment display. Design the necessary hardware and write the necessary ALP for implementing.

DESIGN SPECIFICATIONS

P3-IC TESTER :Design a Microprocessor based Tester to test the logical functioning of the following chips: (i) 7400 (ii) 7402 (iii) 7410

- The IC to be tested will be inserted in a 14 pin ZIF socket.
- The IC number is to be entered via a keyboard. The keyboard has keys 0-9, backspace, enter and test. The user places the IC in the ZIF socket closes it - then enters the IC No, followed by enter key.
- The IC No. is displayed on the 7-segment display. The testing will start once the user presses test key.
- After Test the result PASS/FAIL must be displayed on the 7-segment display.
- Design the necessary hardware and write the necessary ALP to implement this task.

- 8253 Timer is used to create the delay of 20 ms
- PNP BJTs are being used to enable the display one by one to show the result of test and IC number
- The system generates to selector o/p at PC4 and PC5 of 8255(2) depending upon IC number entered

  7402-00

  7410-01

  7400-10

- Demuxes are connected to the possible input pins of ICs through ZIF. Demux uses selector inputs to decide which signal should go to which pin of ZIF based on IC number entered

- Mux is connected to the possible output pins of given ICs through ZIF. Output of the MUX goes to PB0 to PB3.
- These O/P generated at O/P pins of ZIF(decided by IC number entered) are taken as I/P through MUX and are compared against the stored truth table for corresponding set of I/Ps.
- The use of MUX and DEMUX is based on the idea that each gate of the IC can be checked simultaneously by giving same set of signals as input.
- For 7400 and 7402 I/P set is (I1,I2){which can be given to all four gates simultaneously} and output set is (O1,O2,03,04). For 7410, it's (I1,I2,I3) and (O1,O2,O3).
- Testing the ICs other than 7400, 7402, 7410 and damaged ICs gives O/P as FAIL on the 7 segment Display.
- If the IC is working, the Display shows PASS

ASSUMPTIONS IN DESIGN

1. The first key pressed is always a digit (backspace is never pressed in the beginning).
2. Only test key is pressed after the enter key

Components used:

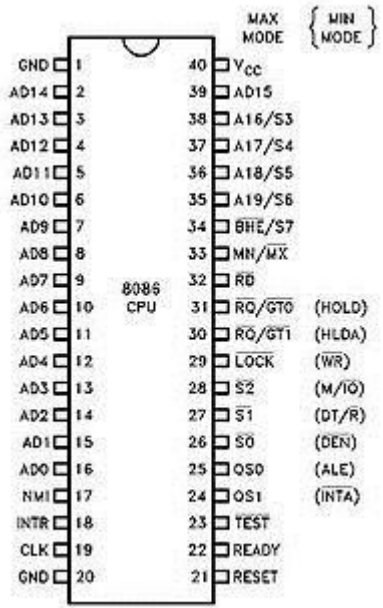
1. 8086 Microprocessor
2. 2N2905-Low power BJT
3. 8255A (Programmable Peripheral Interface with 24 I/O lines) -2 NOS
4. 74LS138 (3:8 Decoder) - 3 NOS
5. 74LS245 (Octal Bus transceivers with tristate output) -2 NOS
6. 74LS373 (Octal D-Type transparent latches with 3 state outputs) -3 NOS
7. 2732 (16K (4Kx4) EPROM) -4 NOS
8. 6116 (4K (2Kx2) Static RAM) -2 NOS

9. 7400 (Quadruple 2-input positive NAND gates)
10. 7402 (Quadruple 2-input positive NOR gates)
11. 7410 (Triple 3-input positive NAND gates)
12. 7-Segment Anode Display
13. SW-SPDT (Interactive SPDT switch (Momentary Action)
14. Resistances-10K, 150 ohms, 1.5K-Quantity 4 each
15. 74153-Dual 1 of 4 line Multiplexer
16. 74LS139-Dual 1 of 4 Demultiplexer
17. 8253 - Programmable Interval Timer
18. ZIF socket

PIN OUTS OF COMPONENTS USED

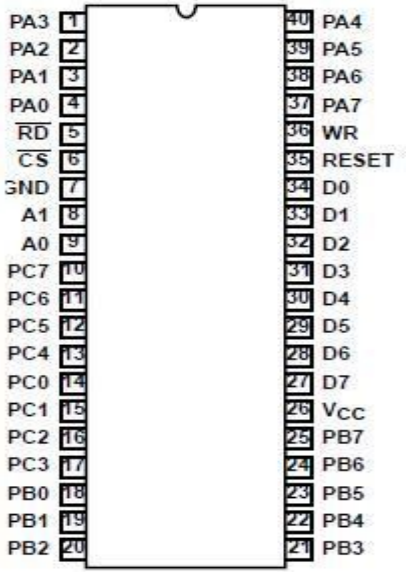
8086

Microprocessor Quantity-1



8255A

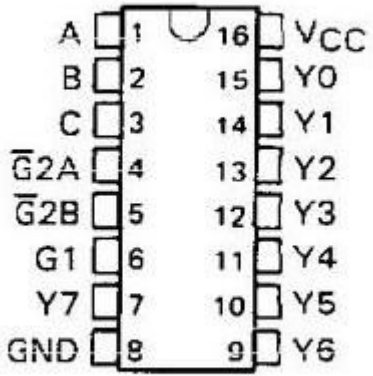
Microprocessor Programmable Peripheral Interface Quantity-2



Decoder Buffer

74LS138 74LS245

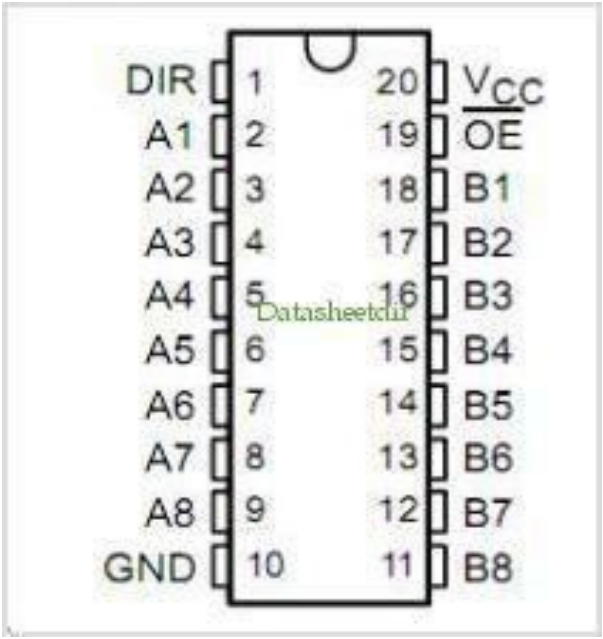
Quantity-3



Decoder Buffer

74LS245

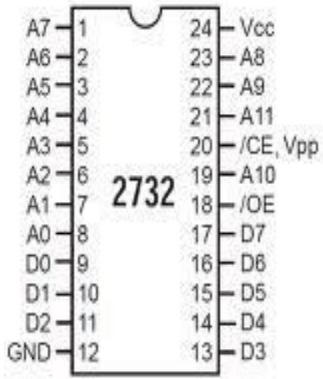
Quantity-1 Quantity-2



ROM

2732

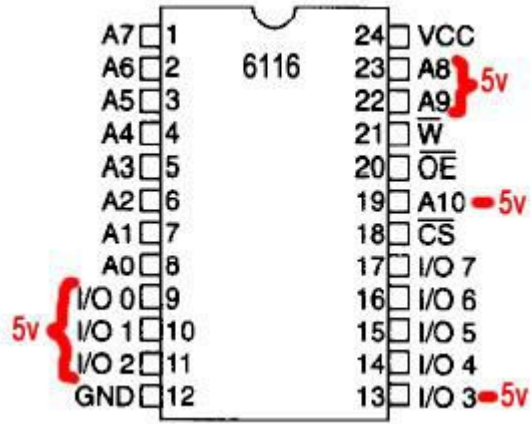
Quantity-4



RAM

6116

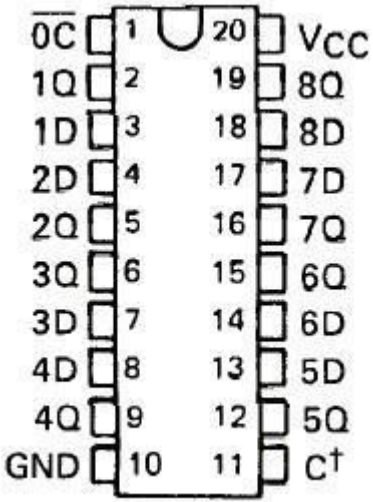
Quantity-2



Latch

74LS373

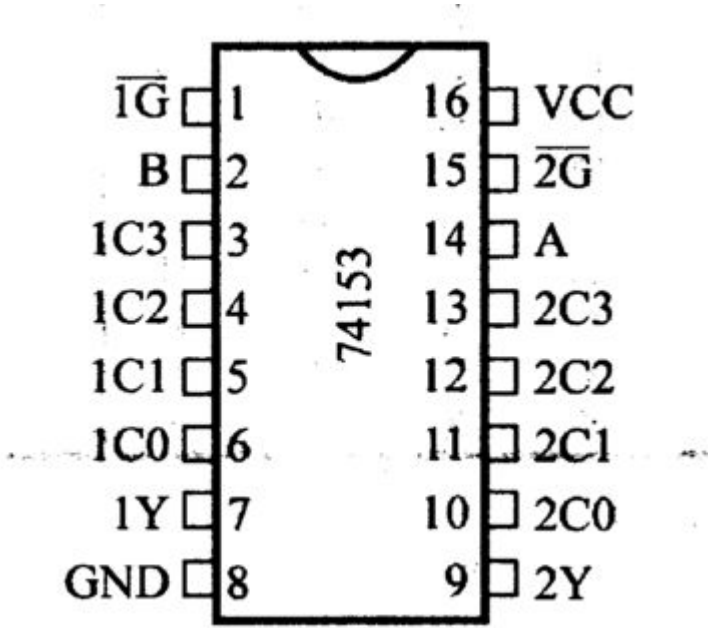
Quantity-3



Dual 4 line to 1 line Multiplexer

74153

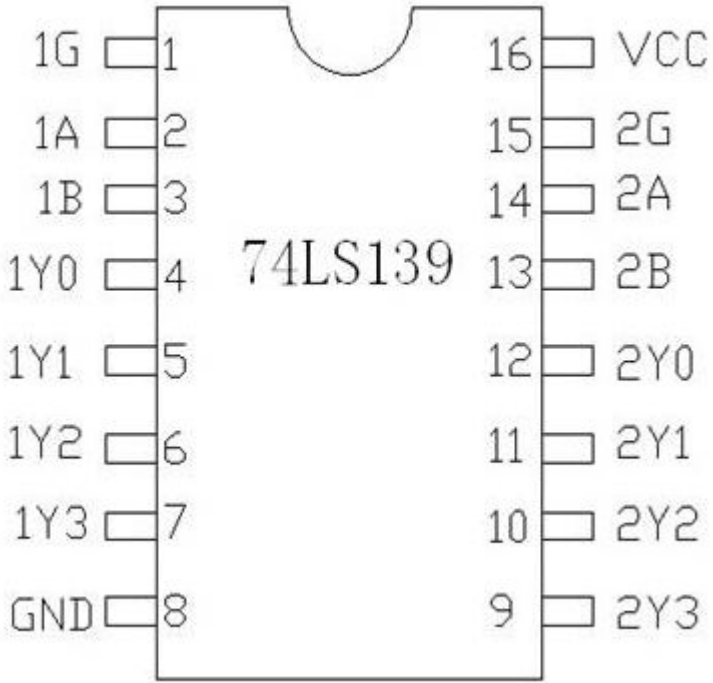
Quantity-2



Dual 1 of 4 Demultiplexer

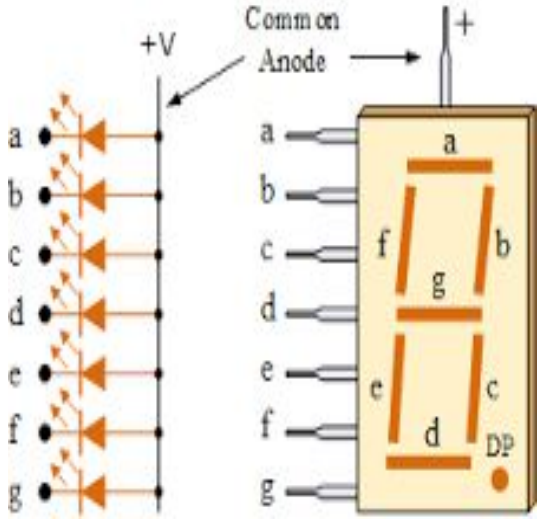
74LS139

Quantity-2



7 Segment Anode Display

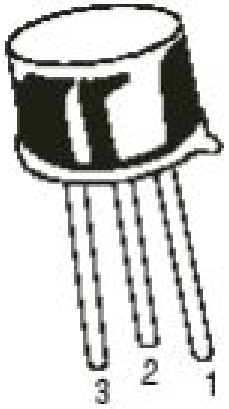
Quantity-4



Bipolar Junction Transistor

2N2905

Quantity-4

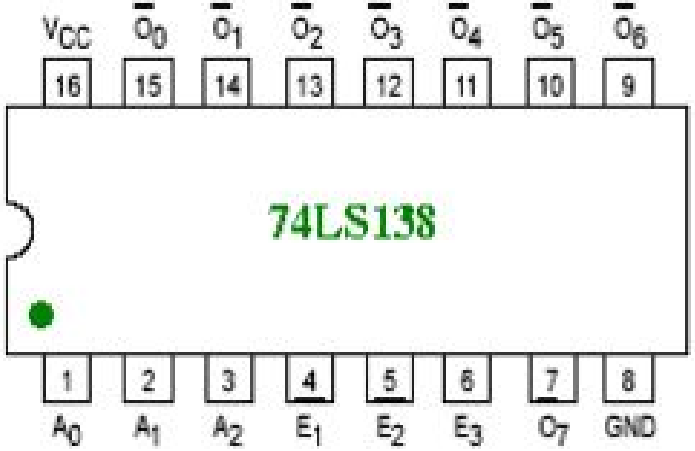


Pin Configuration
1. Emitter
2. Base
3. Collector

3 Line to 8 line Decoder

74LS138

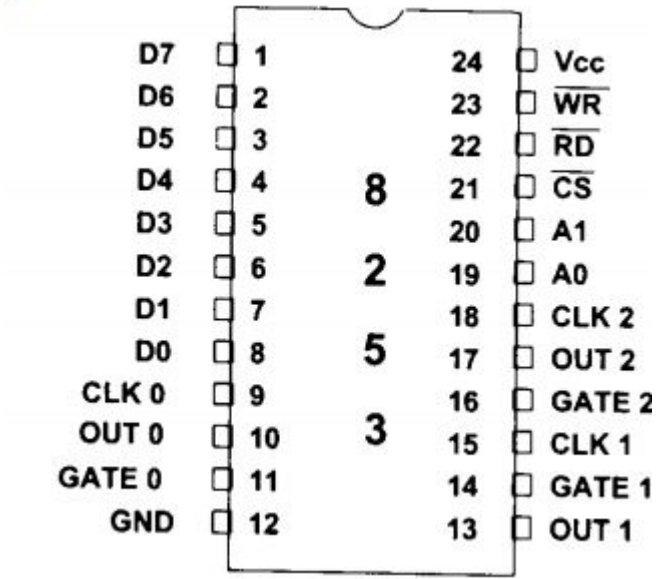
Quantity-1



Timer

8253

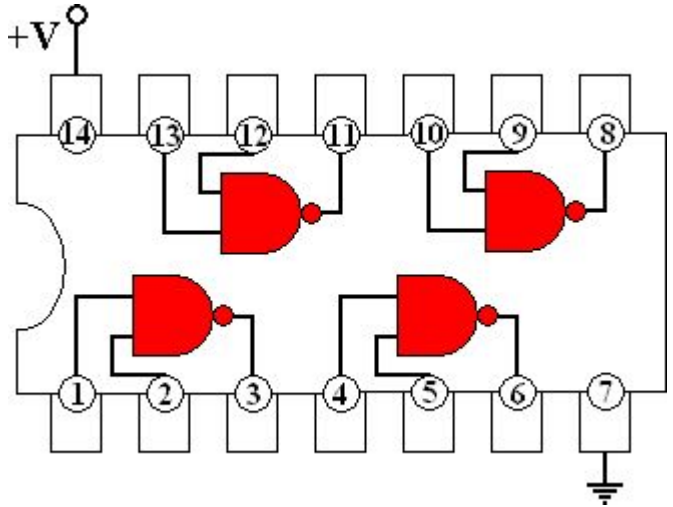
Quantity-1

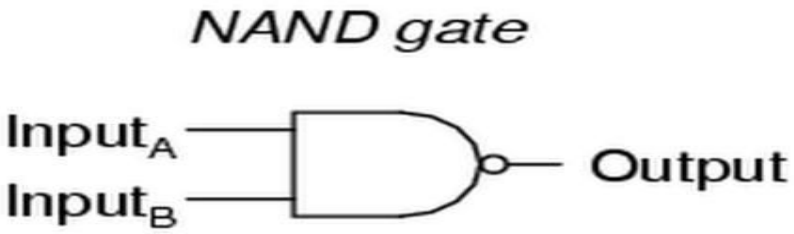


IC's TO BE TESTED

IC-7400

2 Input NAND Gate IC



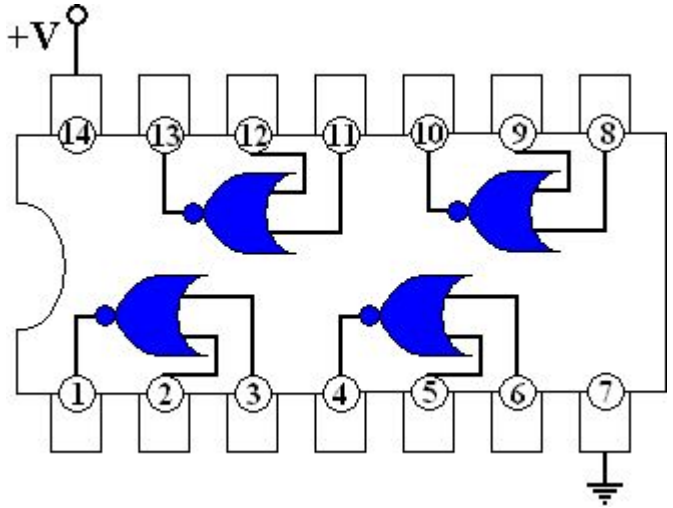


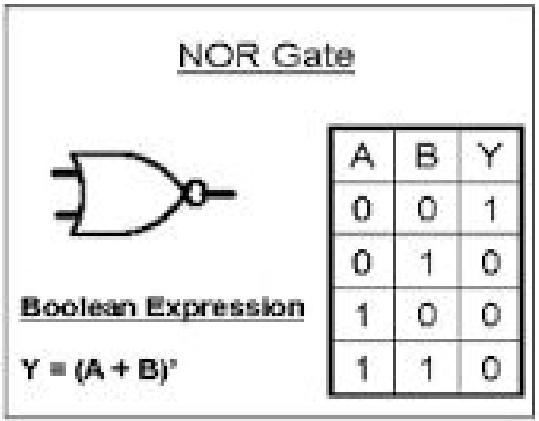
A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

IC's TO BE TESTED

IC-7402

2 Input NOR Gate IC

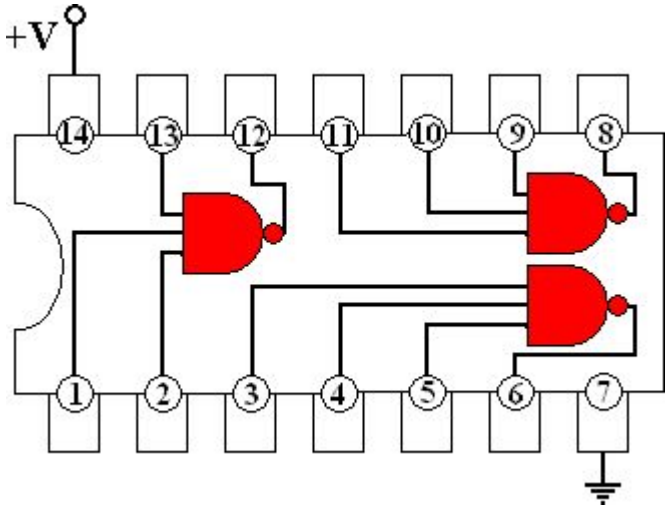


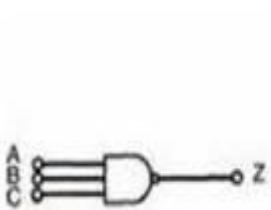


IC's TO BE TESTED

IC-7410

3 Input NAND Gate IC





A	B	C	Z
1	1	1	0
1	1	0	1
1	0	1	1
1	0	0	1
0	1	1	1
0	1	0	1
0	0	1	1
0	0	0	1

Memory interfacing

Memory Requirements:

In proteus 7 minimum ROM chip available is 4K and minimum RAM chip available is 2k. We need to interface :

8K ROM starting at 00000H

4K RAM starting at 02000H

8K ROM starting at FE000H

No of Chips:

2732 ROM (Size of ROM = 32/8 = 4K) x4

6116 RAM (Size of RAM = 16/8 = 2K) x2

MEMORY ALLOCATION

Memory Allocation:

ROM1E - 00000H, 00002H, 00004H……..01FFEH

ROM1O - 00001H, 00003H, 00005H……..01FFFH

RAM1E - 02000H, 02002H, 02004H……..02FFEH

RAM1O - 02001H, 02003H, 02005H……..02FFFH

ROM2E - FF000H, FF002H, FF004H……..FFFFEH

ROM2O - FF001H, FF003H, FF005H……..FFFFFH

ROM1: 00000H-01FFFH

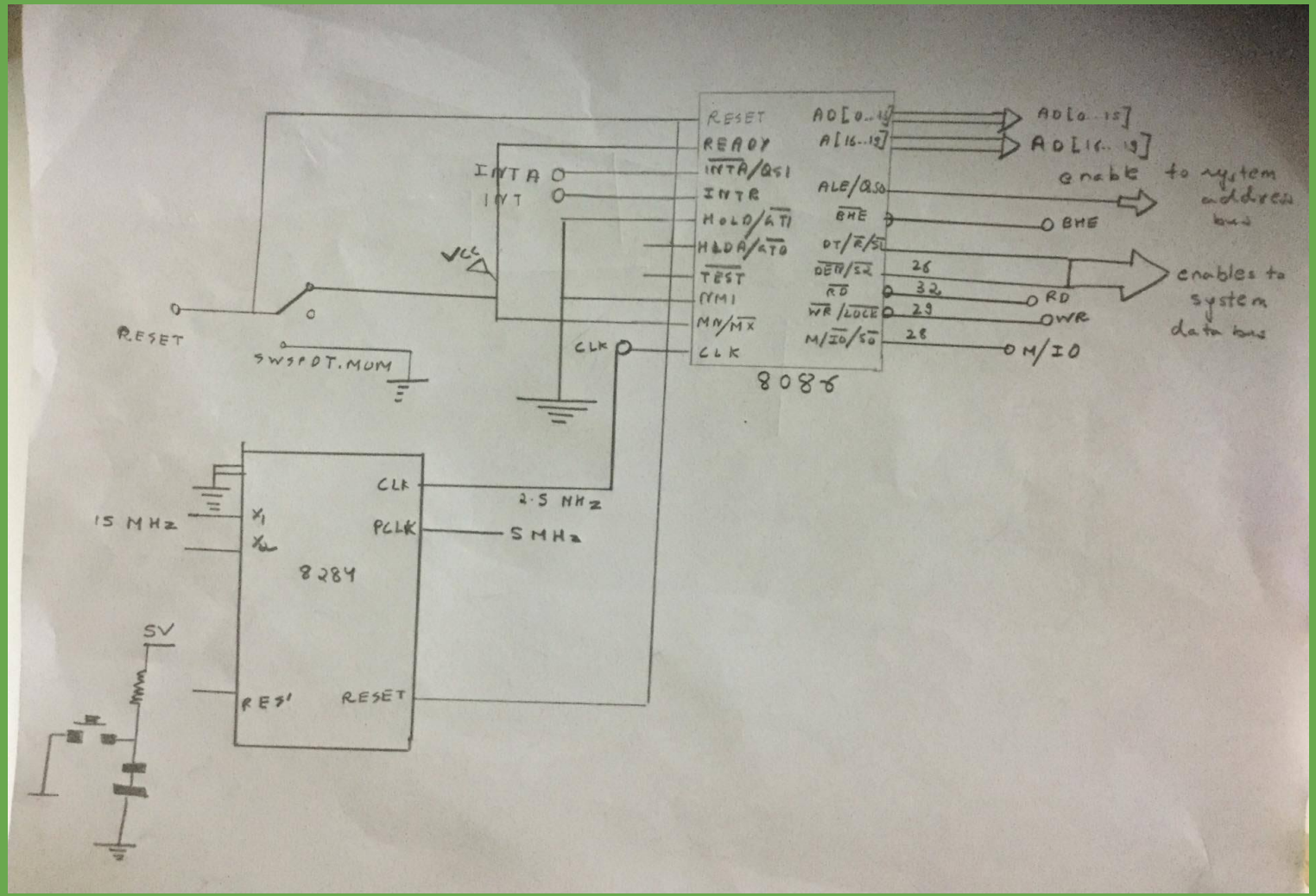
A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	...	A0
0	0	0	0	0	0	0	0	0	0	0	...	0
0	0	0	0	0	0	0	1	1	1	1	...	1

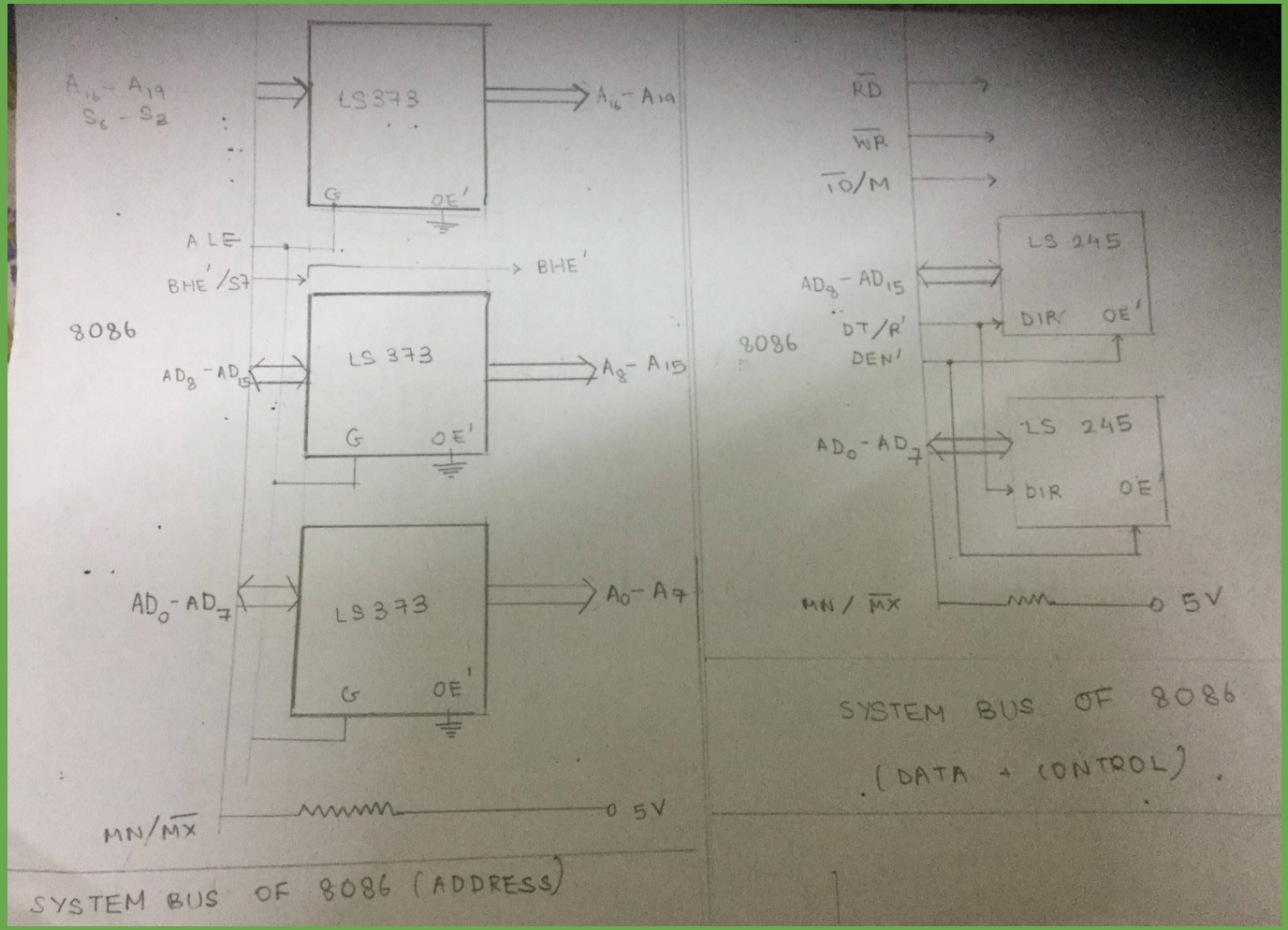
ROM1: FE000H-FFFFFH

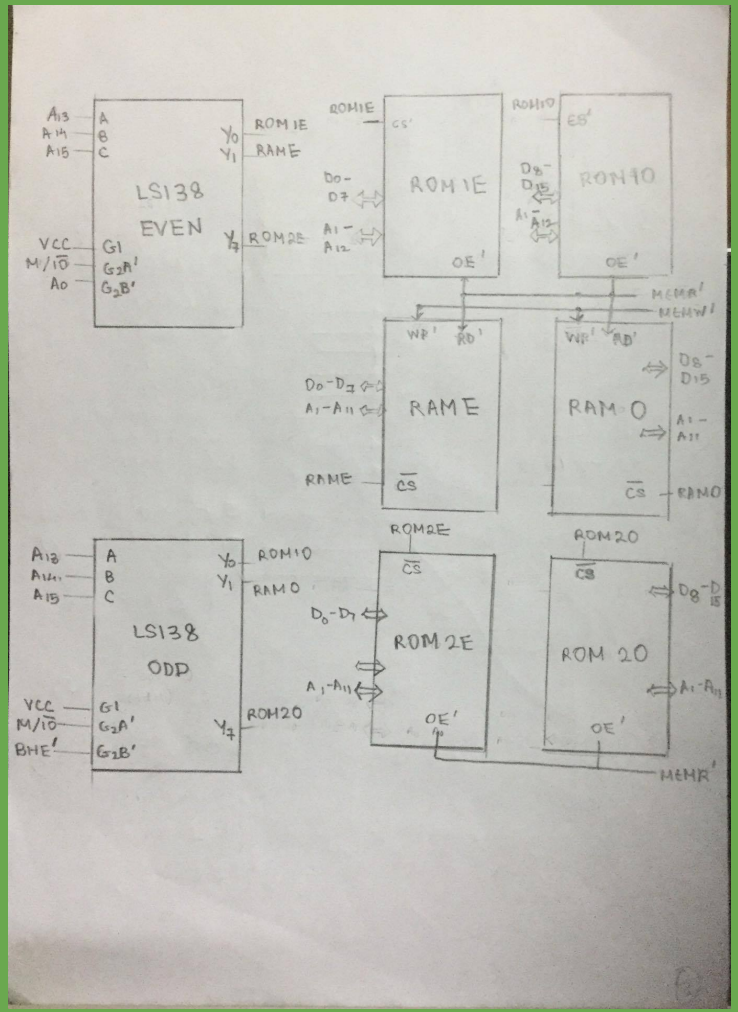
A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	...	A0
1	1	1	1	1	1	1	0	0	0	0	...	0
1	1	1	1	1	1	1	1	1	1	1	...	1

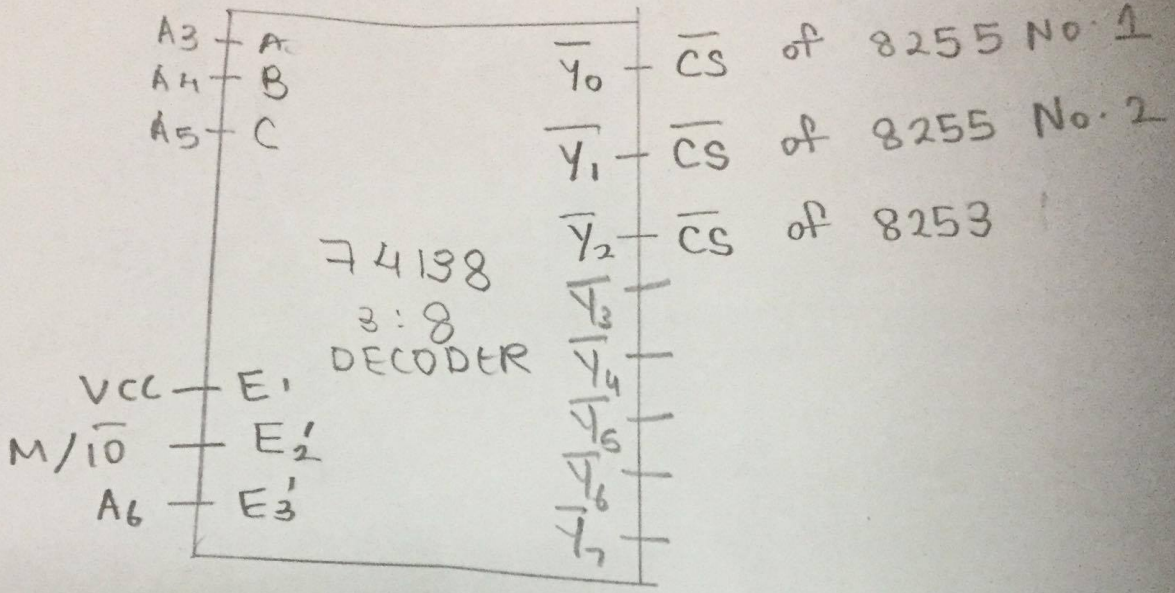
RAM : 02000-02FFFH

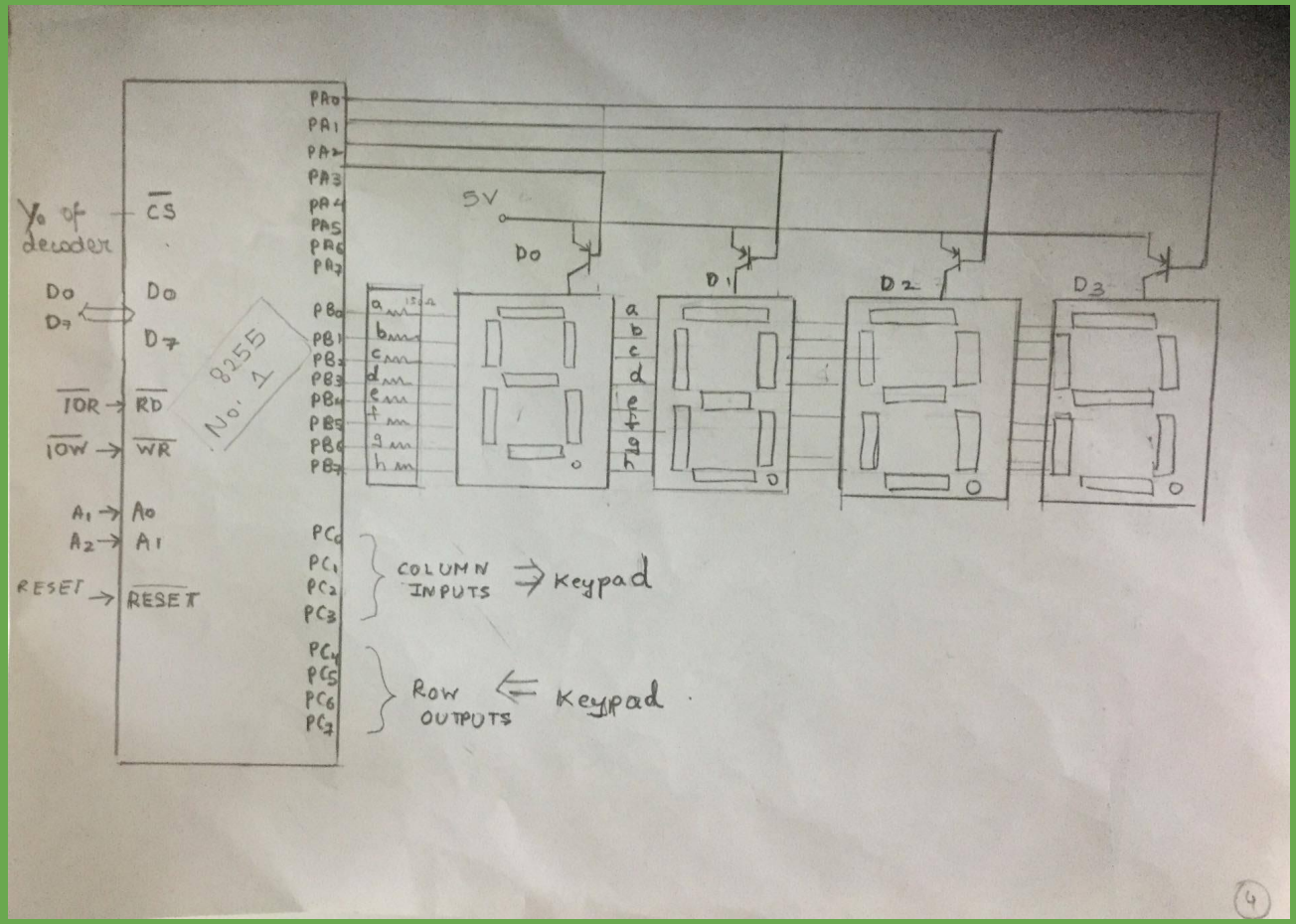
A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	...	10
0	0	0	0	0	0	1	0	0	0	0	...	0
0	0	0	0	0	0	1	0	1	1	1	...	1


RESET
READY
INTA/QS1
INTR
HOLD/RTI
HLDA/RTO
TEST
MN/MX
CLK
AD[0..15]
A[16..19]
ALE/QS0
BHE
DT/R/S1
DEN/S2
RD
WR/LOCK
M/IO/S0
8086
AD[0..15]
AD[16..19]
enable to system address bus
BHE
enables to system data bus
26
32
RD
29
WR
28
M/IO
INTA
INT
VCC
RESET
SWSPDT.MOM
CLK
2.5 MHz
15 MHz
X1
X2
CLK
PCLK
5 MHz
8284
5V
RES'
RESET

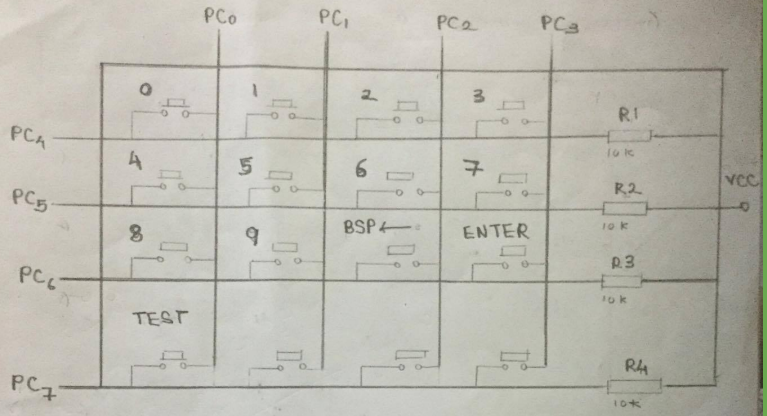

A_{16} - A_{19}
S_6 - S_3
LS373
A_{16} - A_{19}
G
OE'
ALE
BHE'/S7
BHE'
8086
AD_8 - AD_{15}
LS 373
A_8 - A_{15}
G
OE'
AD_0 - AD_7
LS373
A_0 - A_7
G
OE'
MN/$\overline{MX}$
5V
SYSTEM BUS OF 8086 (ADDRESS)
$\overline{RD}$
$\overline{WR}$
$\overline{IO}/M$
LS 245
AD_8 - AD_{15}
DT/R'
DEN'
DIR
OE'
8086
LS 245
AD_0 - AD_7
DIR
OE'
MN / $\overline{MX}$
5V
SYSTEM BUS OF 8086
(DATA + CONTROL)


LS138
EVEN
A13
A14
A15
A
B
C
Y0
Y1
Y7
ROM1E
RAME
ROM2E
VCC
G1
M/IO
G2A'
A0
G2B'
ROM1E
CS'
ROM1E
OE'
D0-D7
A1-A12
ROM1O
ES'
ROM1O
OE'
D8-D15
A1-A12
MEMR'
MEMW'
WR'
RD'
RAME
RAM O
D0-D7
A1-A11
D8-D15
A1-A11
RAME
CS
CS
RAMO
ROM2E
ROM2O
LS138
ODD
A12
A14
A15
Y0
Y1
Y7
ROM1O
RAMO
ROM2O
VCC
M/IO
BHE'
G1
G2A'
G2B'
ROM2E
CS
ROM 2O
CS
D0-D7
A1-A11
D8-D15
A1-A11
OE'
OE'
MEMR'

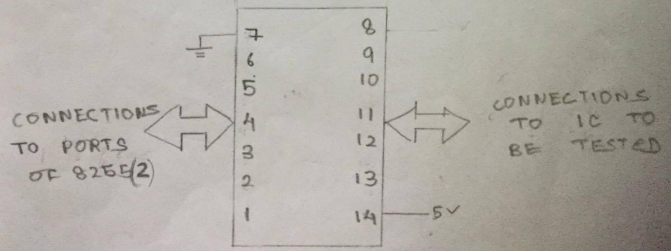

A3
A4
A5
A
B
C
74138
3:8
DECODER
VCC
M/IO
A6
E1
E2'
E3'
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
CS of 8255 No. 1
CS of 8255 No. 2
CS of 8253

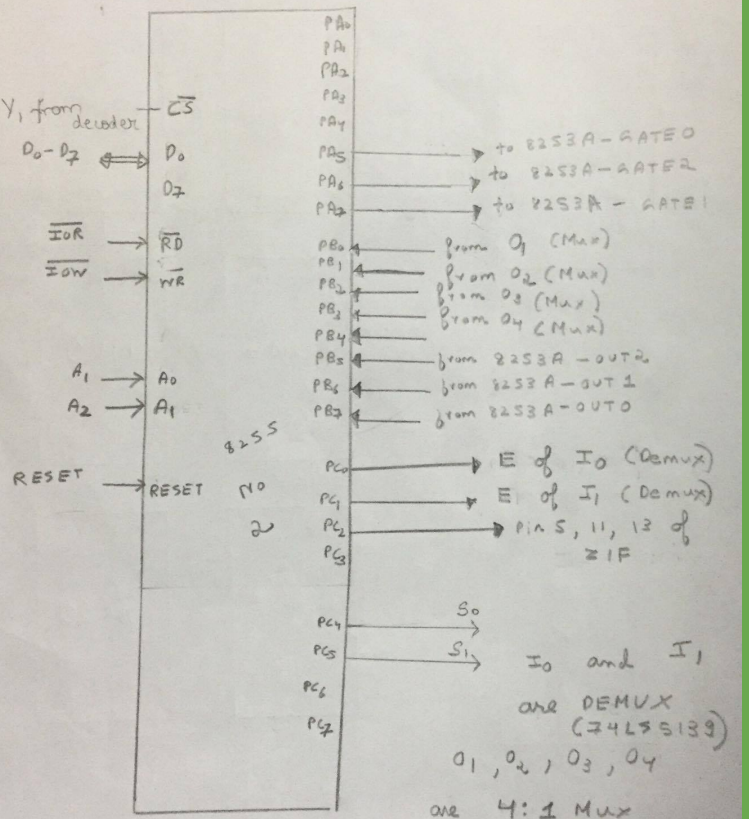

Y0 of decoder
CS
D0
D7
D0
D7
IOR
RD
IOW
WR
A1
A0
A2
A1
RESET
RESET
8255 No. 1
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
5V
D0
D1
D2
D3
a
b
c
d
e
f
g
COLUMN INPUTS ⇒ Keypad
ROW OUTPUTS ⇐ Keypad

(to 8255 (1))



ZIF SOCKET




Y1 from decoder
CS
D0 - D7
D0
D7
IOR
RD
IOW
WR
A1
A0
A2
A1
8255
RESET
RESET
NO
2
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
to 8253A-GATE0
to 8253A-GATE2
to 8253A-GATE1
from O1 (Mux)
from O2 (Mux)
from O3 (Mux)
from O4 (Mux)
from 8253A-OUT2
from 8253A-OUT1
from 8253A-OUT0
E of I0 (Demux)
E of I1 (Demux)
Pin 5, 11, 13 of 74F
S0
S1
I0 and I1 are DEMUX (74LS139)
O1, O2, O3, O4 are 4:1 Mux 74LS153
S0 and S1 are select lines for Muxes and Demuxes

4-23-2016 06:48

Inputs are classified as I_1, I_2 and I_3 (I_3 is only for 7410)

O/P are classified as O_1, O_2, and O_3 and O_4 (O_4 is for 7400 and 7402)

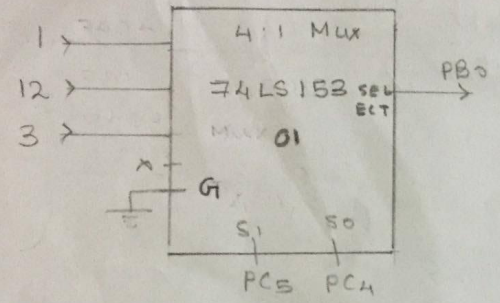
Pins of Ic →

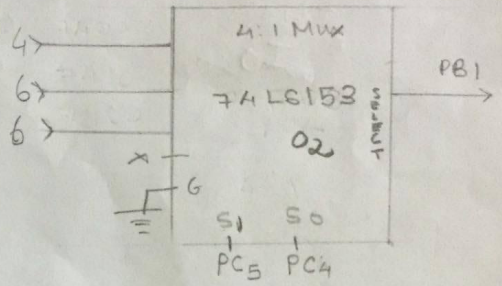
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
7402	O_1	I_1	I_2	O_2	I_1	I_2	G	I_1	I_2	O_3	I_1	I_2	O_4	V
7410	I_1	I_2	I_1	I_2	I_3	O_2	G	O_3	I_1	I_2	I_3	O_1	I_3	V
7400	I_1	I_2	O_1	I_1	I_2	O_2	G	O_3	I_2	I_1	O_4	I_2	I_1	V

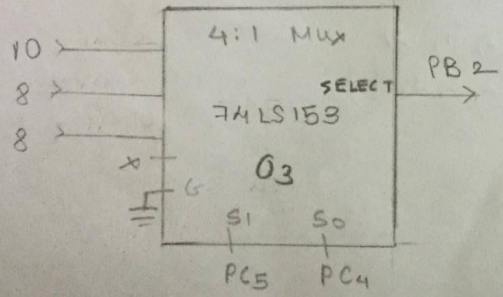
G: GND

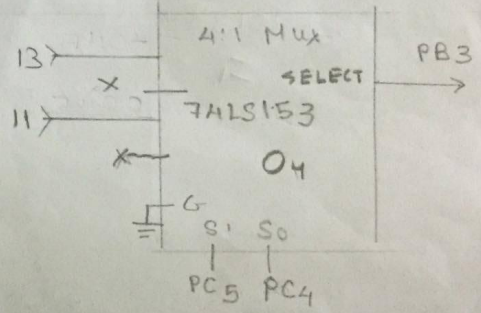
V: V_{cc}

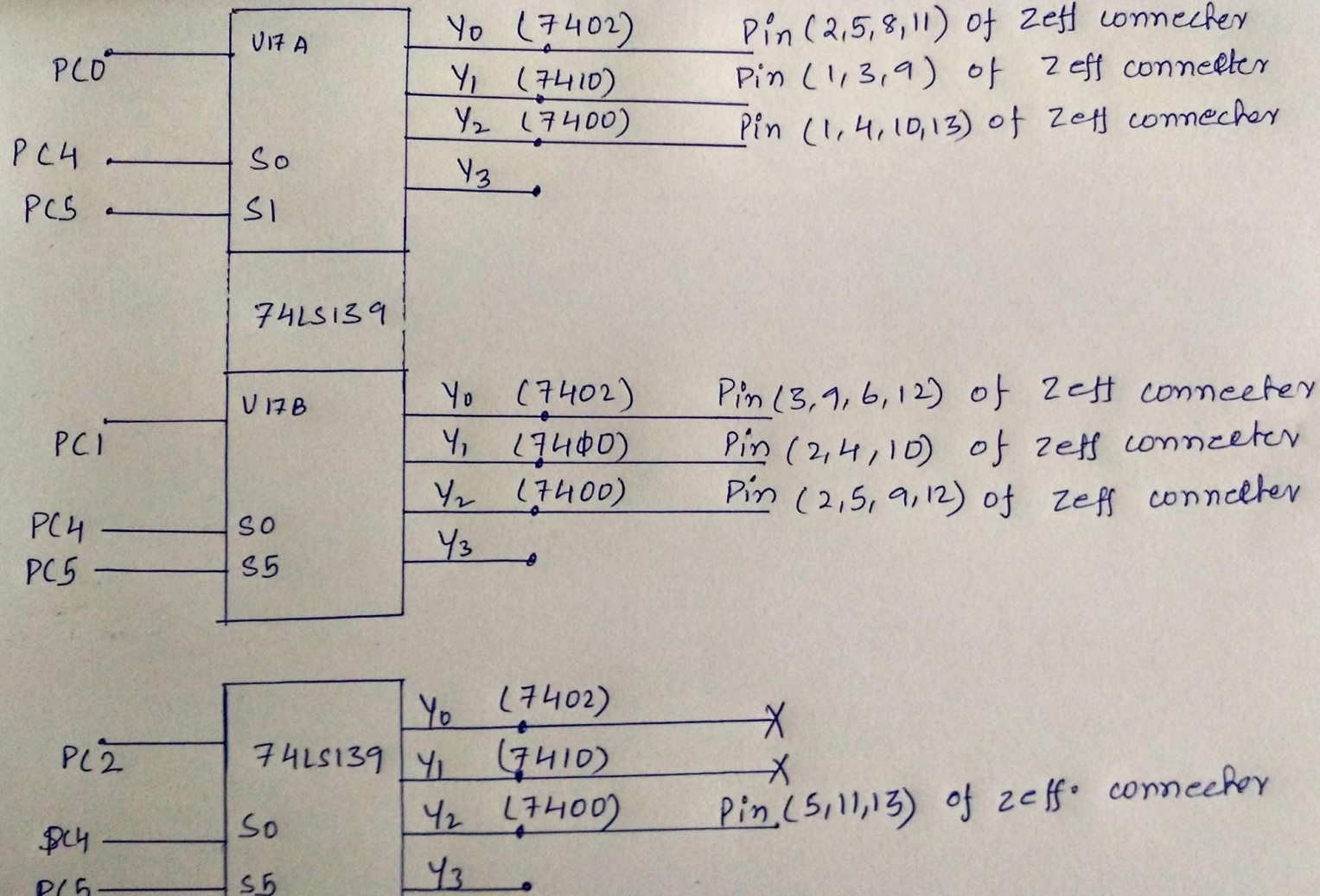
OUTPUT MULTIPLEXING :





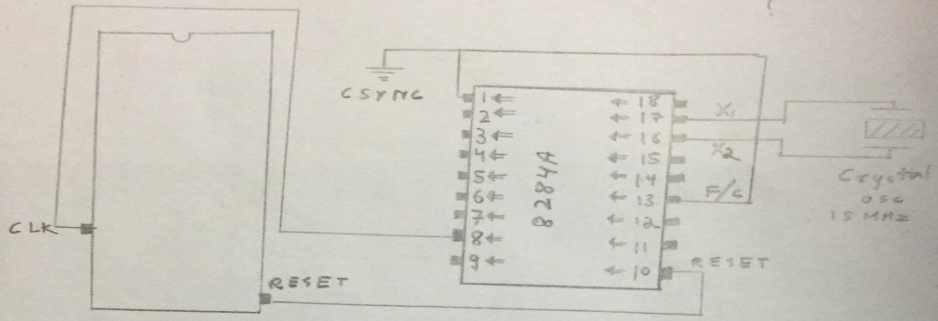




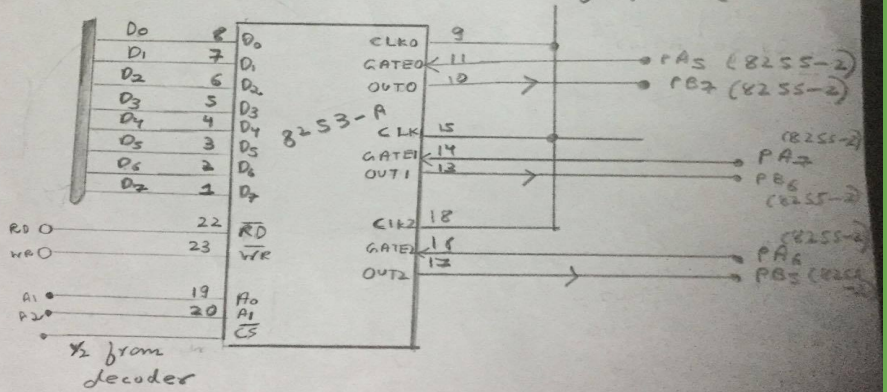


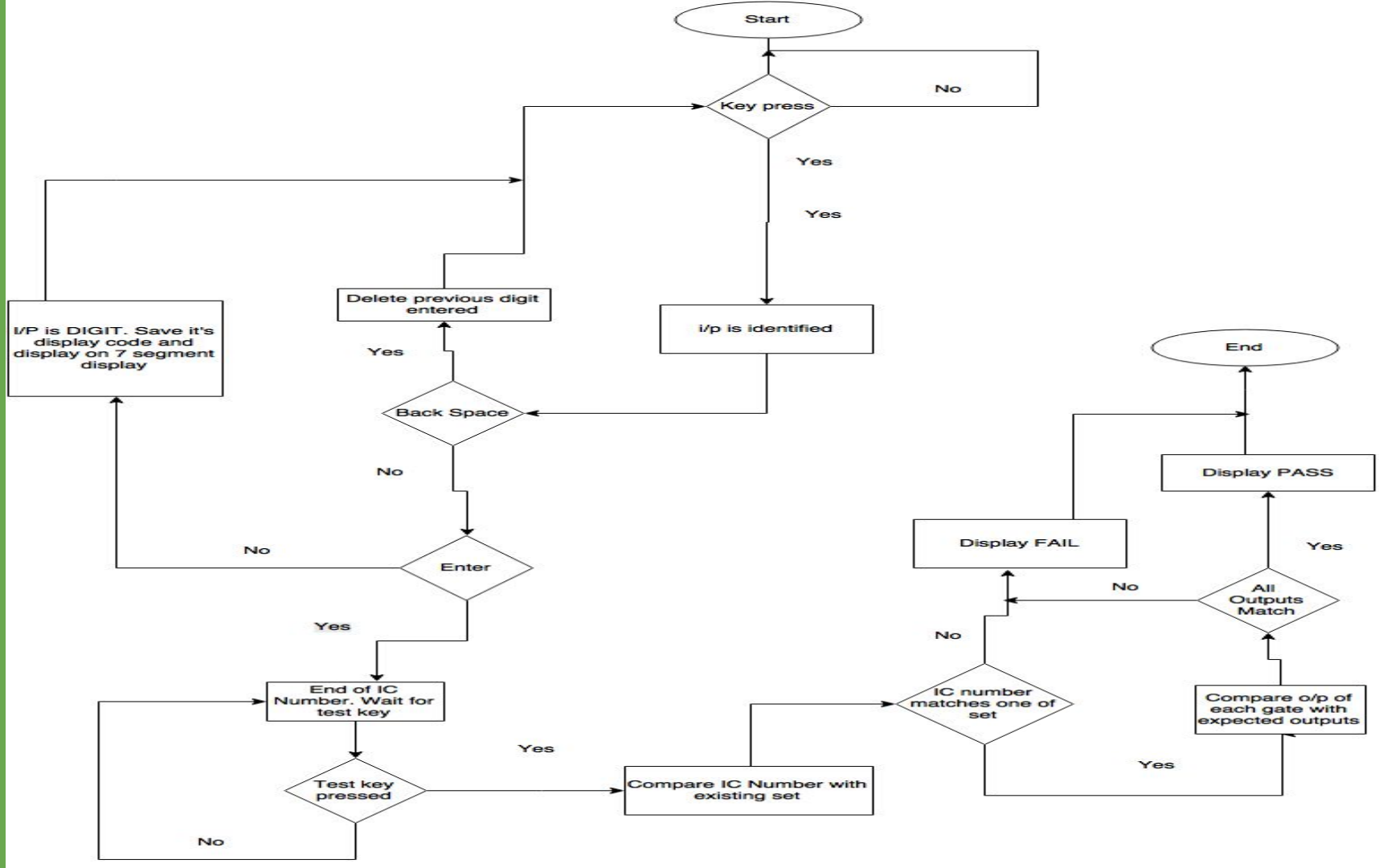
4-23-2016 06:31

8086 with 8284 clock generator



clk frequency 2.5MHz




Start
Key press
No
Yes
Yes
Delete previous digit entered
I/P is DIGIT. Save it's display code and display on 7 segment display
i/p is identified
Yes
Back Space
No
No
Enter
Yes
End of IC Number. Wait for test key
Test key pressed
Yes
No
Compare IC Number with existing set
IC number matches one of set
No
Yes
Compare o/p of each gate with expected outputs
All Outputs Match
No
Yes
Display FAIL
Display PASS
End