

CSC 343 Spring 2021

## Laboratory Exercise Tutorial:

Design Entry Specified:

Schematic Diagram of digital circuits

Hardware Description Language (VHDL)

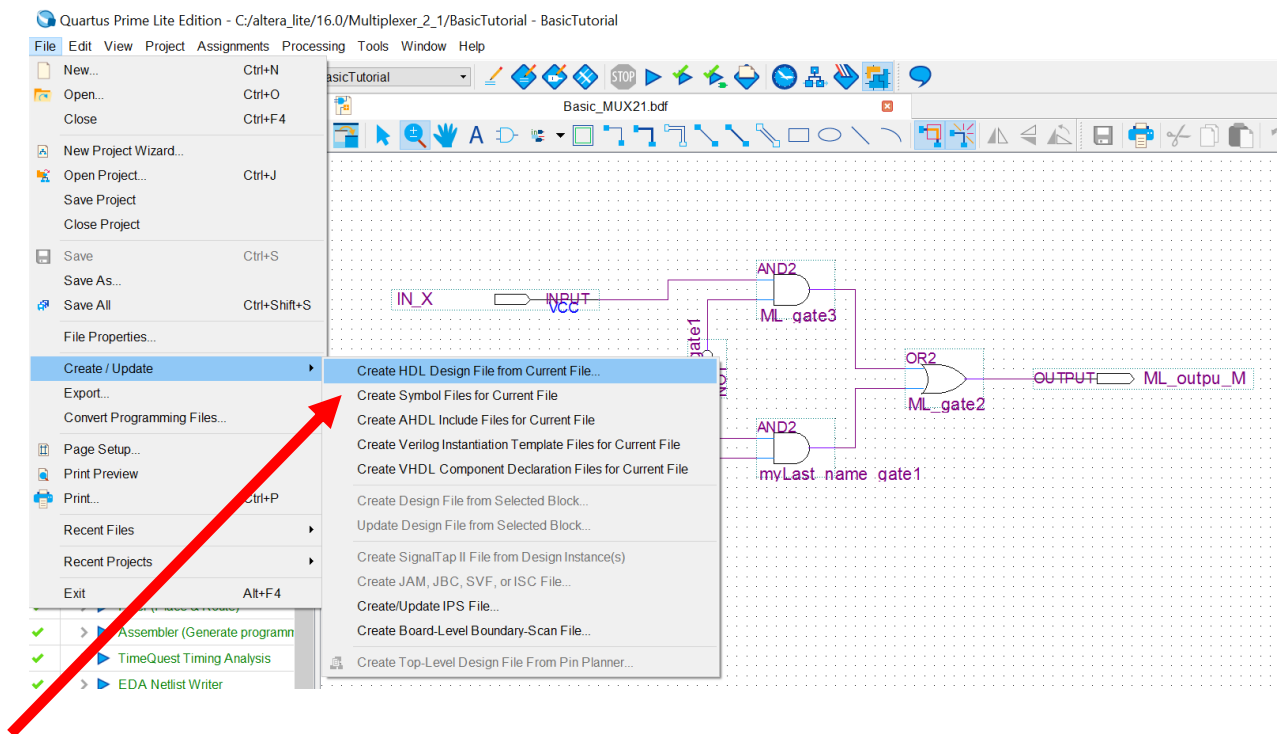
VHDL with LPM( Library Parameterized Modules)

*Instructor: Professor Izidor Gertner*

## Creating VHDL code from a Block Diagram

With your block diagram file open, navigate to **File > Create / Update > Create HDL Design File from Current File...**

Notice that you have to be using the full diagram made from primitive gates, not the one where the symbol file is used.



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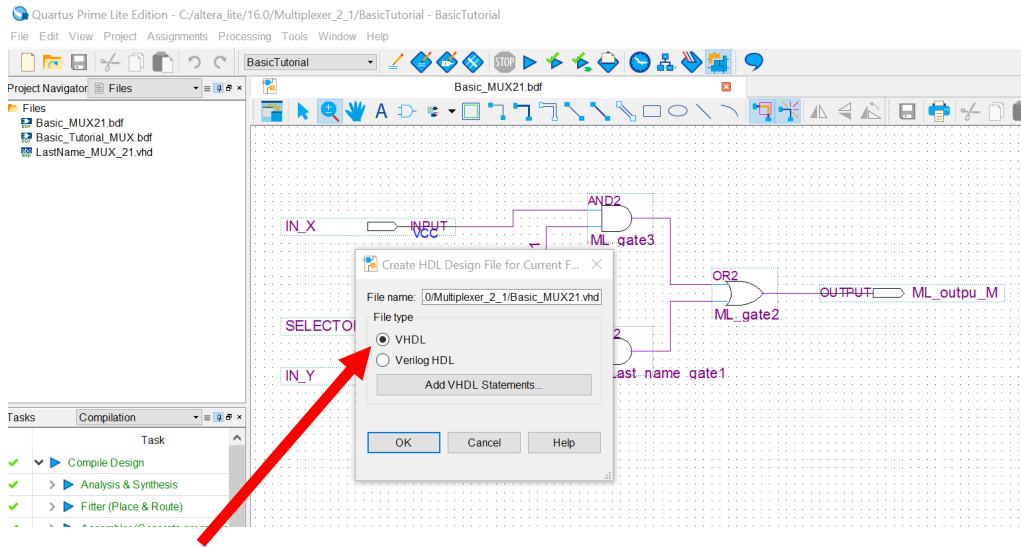
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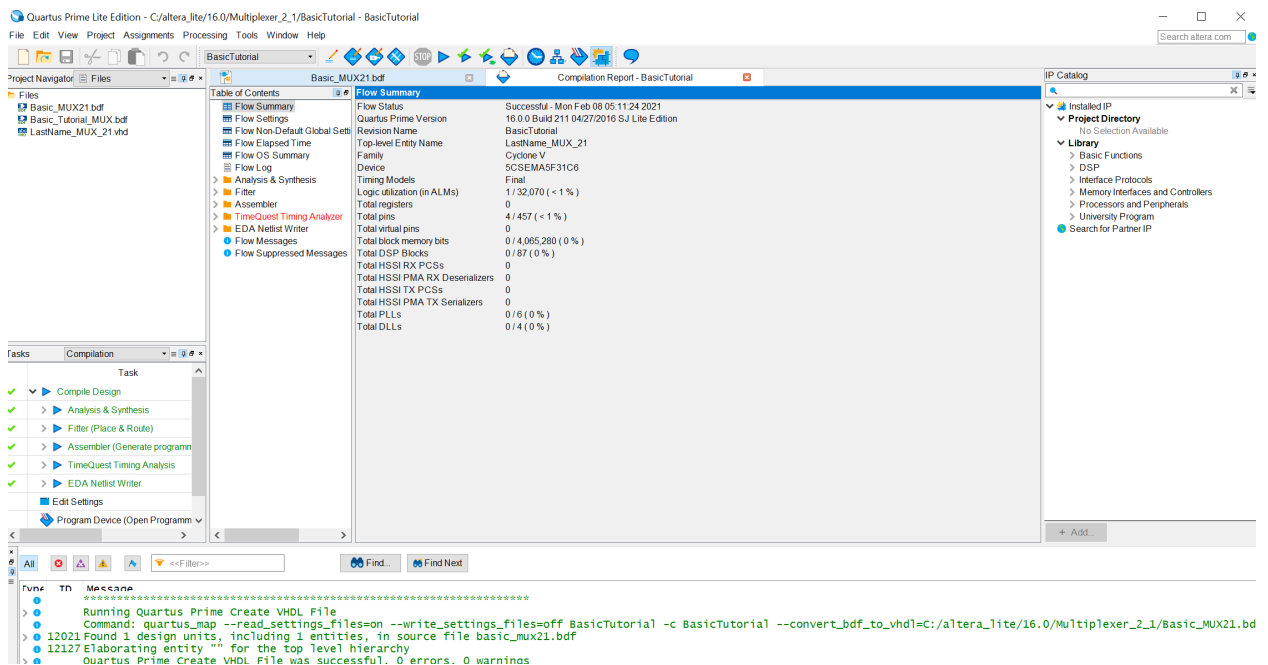
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When the pop up window opens, select the VHDL option.

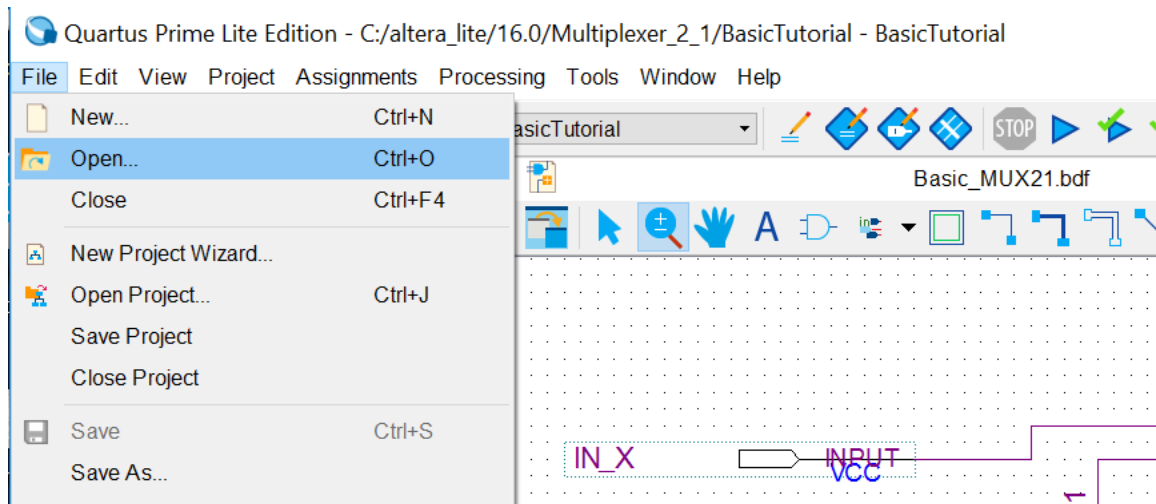


The compilation will automatically start, however this compilation is only concerning the file creation, unlike a normal compilation of a top-level entity.

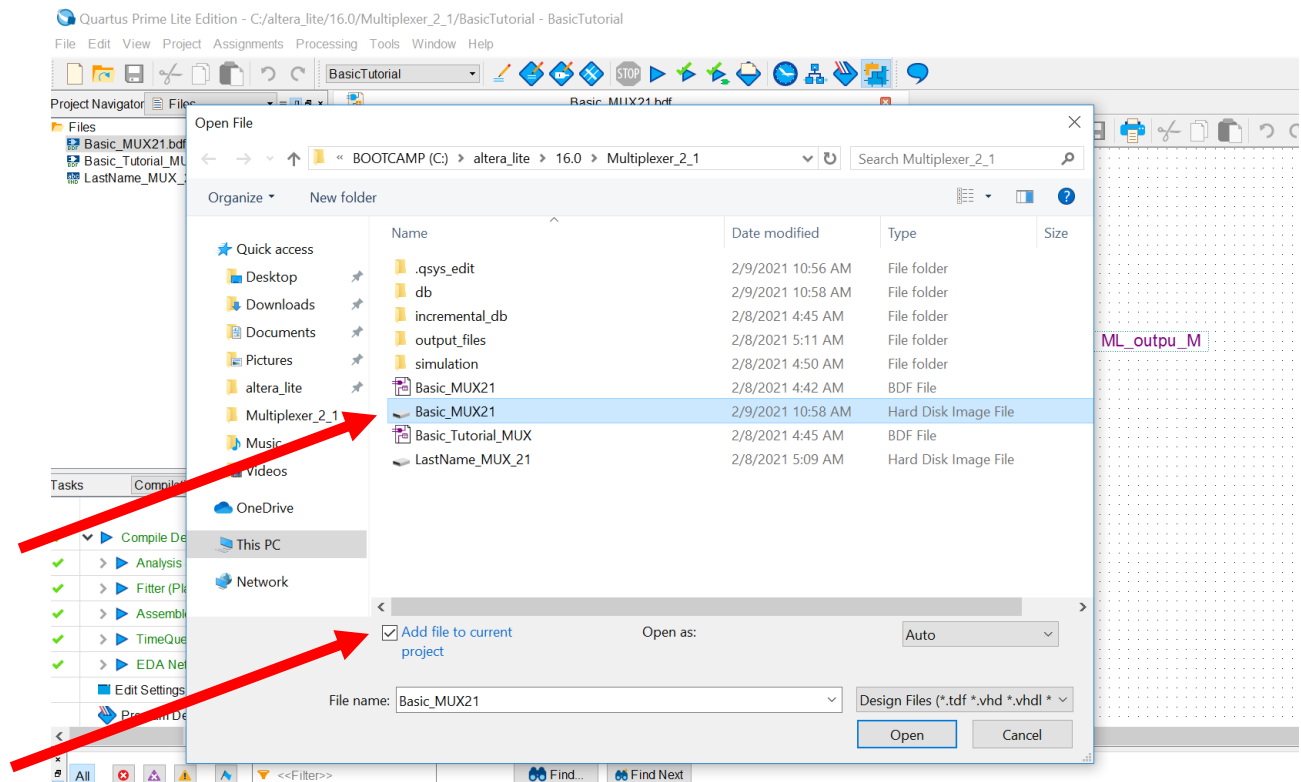


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Open the file, navigate to where your project is.



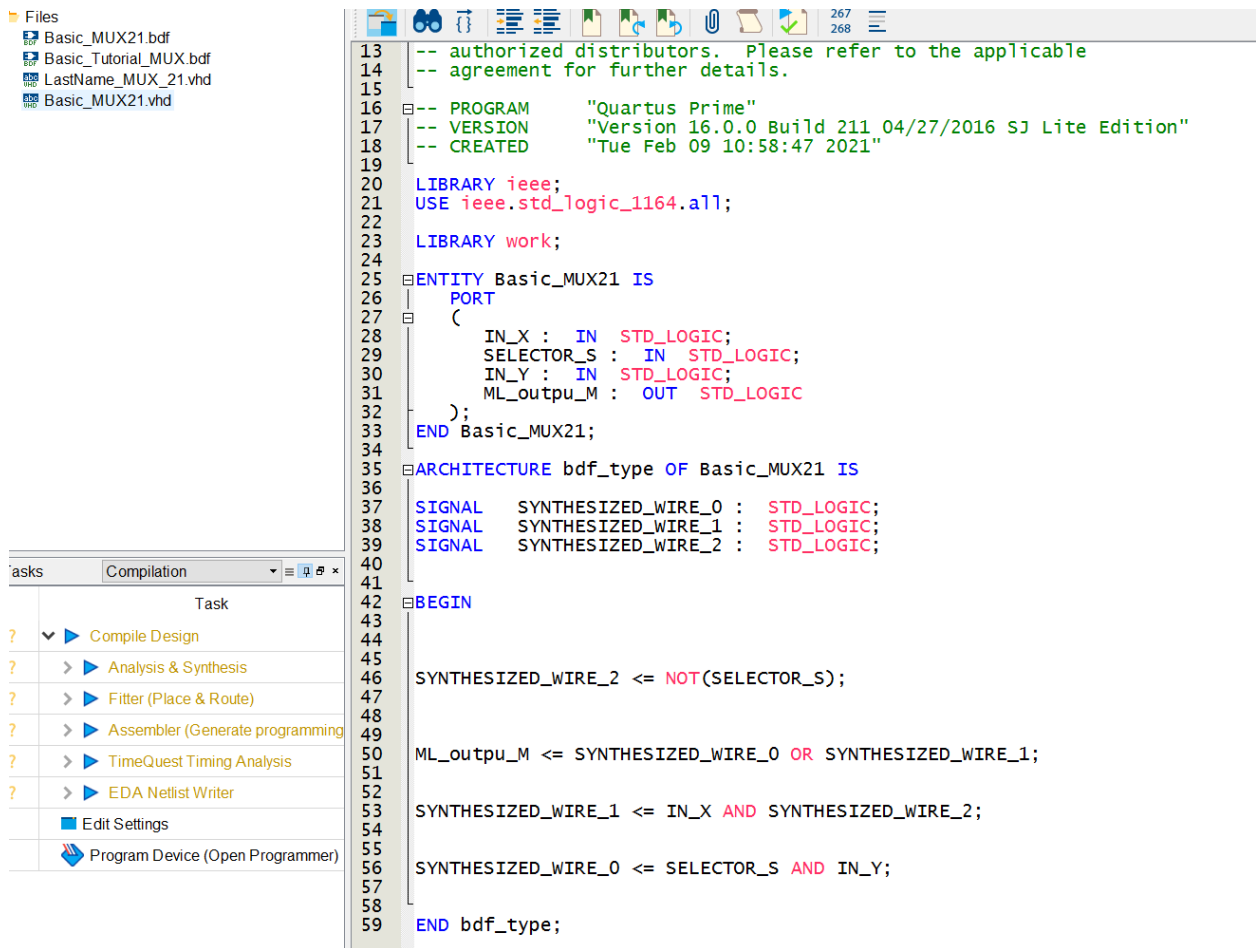
Make sure “Add file to current project” is ticked.



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This is what your file should look like within the project.



The screenshot displays the Quartus Prime IDE interface. On the left, the 'Files' pane shows a project structure with four files: 'Basic\_MUX21.bdf', 'Basic\_Tutorial\_MUX.bdf', 'LastName\_MUX\_21.vhd', and 'Basic\_MUX21.vhd'. A red arrow points to 'Basic\_MUX21.vhd'. Below the file list is a 'Tasks' pane with a 'Compilation' tab, showing a list of tasks: 'Compile Design', 'Analysis & Synthesis', 'Fitter (Place & Route)', 'Assembler (Generate programming)', 'TimeQuest Timing Analysis', 'EDA Netlist Writer', 'Edit Settings', and 'Program Device (Open Programmer)'. The main editor window on the right shows the VHDL code for 'Basic\_MUX21.vhd'. The code includes a library declaration for 'ieee' and 'std\_logic\_1164.all', a port declaration for 'Basic\_MUX21' with inputs 'IN\_X', 'SELECTOR\_S', 'IN\_Y' and output 'ML\_outpu\_M', and an architecture 'bdf\_type' that implements a 2-to-1 multiplexer using synthesized wires and logic gates.

```
13 -- authorized distributors. Please refer to the applicable
14 -- agreement for further details.
15
16 -- PROGRAM      "Quartus Prime"
17 -- VERSION      "Version 16.0.0 Build 211 04/27/2016 SJ Lite Edition"
18 -- CREATED      "Tue Feb 09 10:58:47 2021"
19
20 LIBRARY ieee;
21 USE ieee.std_logic_1164.all;
22
23 LIBRARY work;
24
25 ENTITY Basic_MUX21 IS
26     PORT
27     (
28         IN_X : IN  STD_LOGIC;
29         SELECTOR_S : IN  STD_LOGIC;
30         IN_Y : IN  STD_LOGIC;
31         ML_outpu_M : OUT STD_LOGIC
32     );
33 END Basic_MUX21;
34
35 ARCHITECTURE bdf_type OF Basic_MUX21 IS
36
37     SIGNAL SYNTHESIZED_WIRE_0 : STD_LOGIC;
38     SIGNAL SYNTHESIZED_WIRE_1 : STD_LOGIC;
39     SIGNAL SYNTHESIZED_WIRE_2 : STD_LOGIC;
40
41 BEGIN
42
43
44
45     SYNTHESIZED_WIRE_2 <= NOT(SELECTOR_S);
46
47
48     ML_outpu_M <= SYNTHESIZED_WIRE_0 OR SYNTHESIZED_WIRE_1;
49
50
51
52     SYNTHESIZED_WIRE_1 <= IN_X AND SYNTHESIZED_WIRE_2;
53
54
55     SYNTHESIZED_WIRE_0 <= SELECTOR_S AND IN_Y;
56
57
58
59 END bdf_type;
```

Set this new file as the top-level entity in the project, and then start compilation.

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Quartus Prime Lite Edition - C:/altera\_lite/16.0/Multiplexer\_2\_1/BasicTutorial - BasicTutorial

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Files

Files

- Basic\_MUX21.bdf
- Basic\_Tutorial\_MUX.bdf
- LastName\_MUX\_21.vhd
- Basic\_MUX21.vhd

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Sett
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Flow Messages
- Flow Suppressed Messages

Flow Summary

Flow Status: Flow Failed - Tue Feb 09 12:16:05 2021

Quartus Prime Version: 16.0.0 Build 211 04/27/2016 S.J. Lite Edition

Revision Name: BasicTutorial

Top-level Entity Name: Basic\_MUX21

Family: Cyclone V

Device: 5CSEMA5F31C6

Timing Models: Final

Logic utilization (in ALMs): N/A until Partition Merge

Total registers: N/A until Partition Merge

Total pins: N/A until Partition Merge

Total virtual pins: N/A until Partition Merge

Total block memory bits: N/A until Partition Merge

Total PLLs: N/A until Partition Merge

Total DLLs: N/A until Partition Merge

Tasks

Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- TimeQuest Timing Analysis
- EDA Netlist Writer

Find...

Find Next

Run: TN Message

\*\*\*\*\*

Running Quartus Prime Analysis & Synthesis

Command: quartus\_map --read\_settings\_files=on --write\_settings\_files=off BasicTutorial -c BasicTutorial

20028 Parallel compilation is not licensed and has been disabled

12021 Found 1 design units, including 1 entities, in source file basic\_mux21.bdf

12021 Found 1 design units, including 1 entities, in source file basic\_tutorial\_mux.bdf

12021 Found 2 design units, including 1 entities, in source file lastName\_mux\_21.vhd

12049 Can't compile duplicate declarations of entity "Basic\_MUX21" into library "work"

12021 Found 2 design units, including 1 entities, in source file basic\_mux21.vhd

Quartus Prime Analysis & Synthesis was unsuccessful. 3 errors, 1 warning

293001 Quartus Prime Full Compilation was unsuccessful. 5 errors, 1 warning

A library error occurs due to the generated file's name being the same as the block diagram one. In the earlier dialogue where we selected VHDL as the file type, the filename was locked. There is a quick way to fix this:

Go back to editing the file, and find the **Edit > Replace** feature

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Quartus Prime Lite Edition - C:/altera\_lite/16.0/Multiplexer\_2\_1/BasicTutorial - BasicTutorial

File Edit View Project Assignments Processing Tools Window Help

Basic\_MUX21.vhd\*

```
PROGRAM "Quartus Prime"
VERSION "Version 16.0.0 Build 211 04/27/2016 SJ
CREATED "Tue Feb 09 12:09:49 2021"

BRARY ieee;
E ieee.std_logic_1164.all;

BRARY work;

TITY Basic_MUX21 IS
PORT
(
  IN_X : IN STD_LOGIC;
  SELECTOR_S : IN STD_LOGIC;
  IN_Y : IN STD_LOGIC;
  ML_outpu_M : OUT STD_LOGIC
);
D Basic_MUX21;

CHITECTURE bdf_type OF Basic_MUX21 IS
```

Replace

Find what: Basic\_MUX21

Replace with: Basic\_MUX21\_VHDL

☐ Match case

☐ Find whole words only

☐ Use regular expressions

Search: Down

☐ Search selection only

Find Next

Replace

Replace All

Mark All (Current)

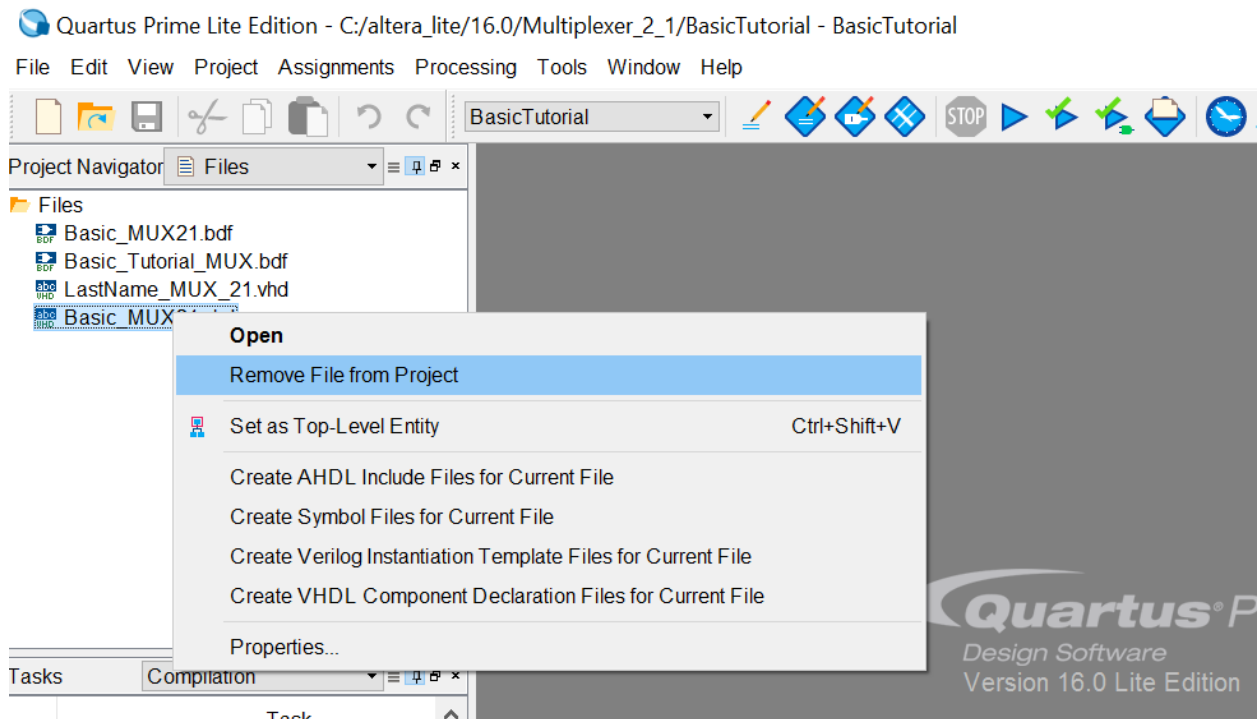
Mark All (All Files)

Cancel

Replace all instances of the problematic name.

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Remove the file from the project in the **Files** tab



Find the file in your project folder and manually re-name it to whatever you replaced the problematic file name with.

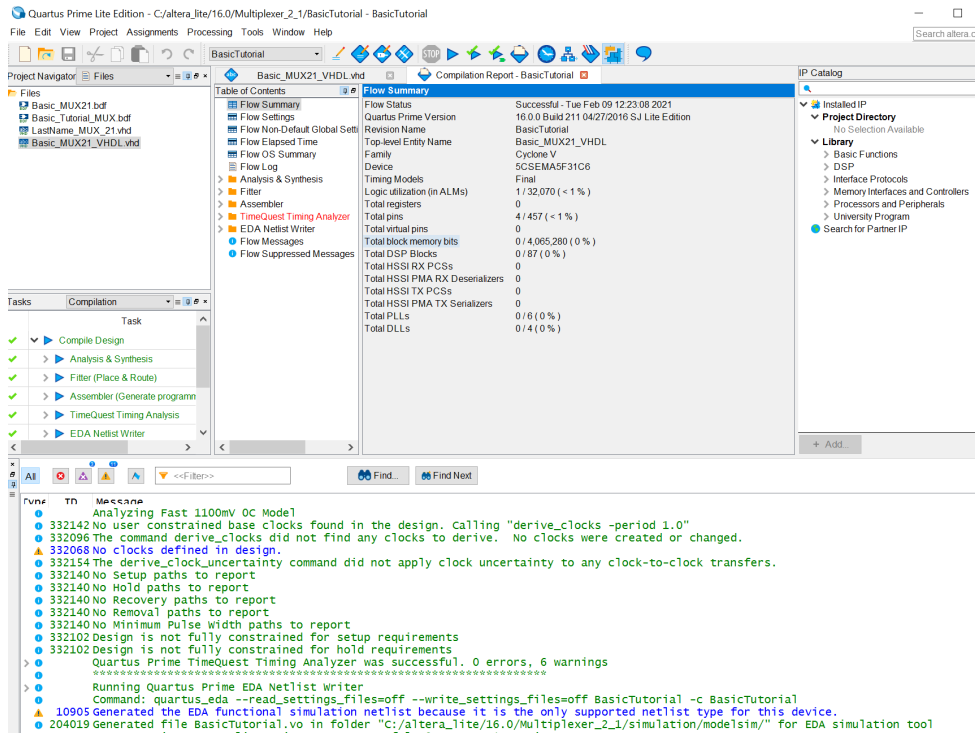
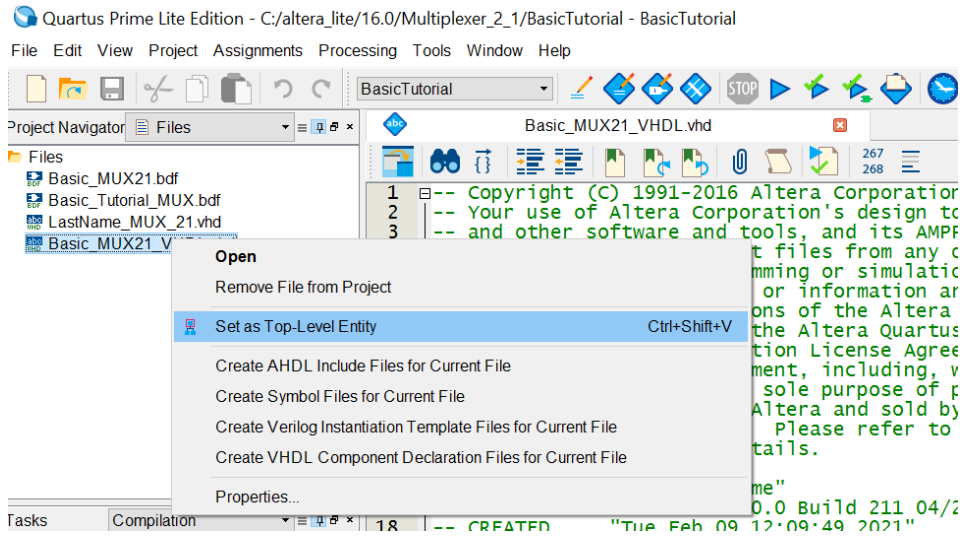
altera_lite > 16.0 > Multiplexer_2_1				Search Multiplex
Name	Date modified	Type	Size	
Basic_MUX21_VHDL	2/9/2021 12:19 PM	Hard Disk Image File	2 KB	

Now, repeat the step where you opened the file and again make sure the “Add file to project” box is ticked.

# Laboratory Exercise Tutorial: Design Entry Specified: Schematic Diagram of digital circuits Hardware Description Language (VHDL) VHDL with LPM( Library Parameterized Modules)

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Set it as the top-level entity once again, and compile. It will have no error this time.





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## VHDL with LPM( Library Parameterized Modules)

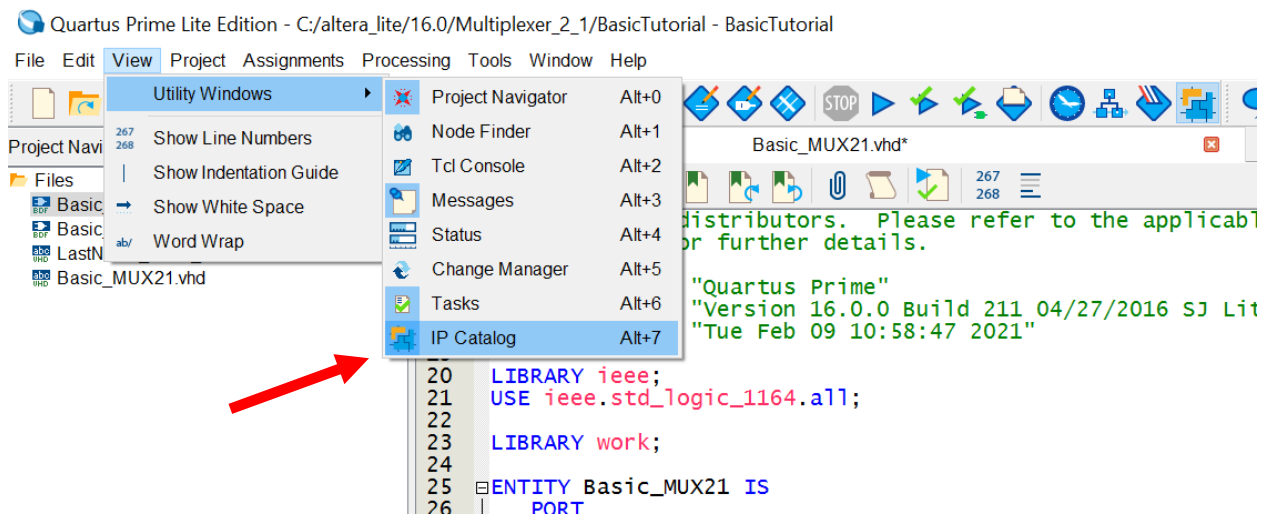
*Instructor: Professor Izidor Gertner*

## Using the Library of Parameterized Modules (LPM) to Create a VHDL File

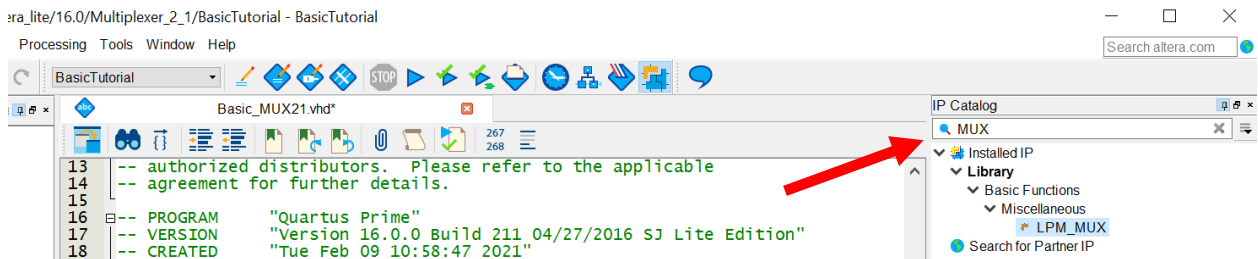
The Multiplexer is already included as a pre-built customizable module in Quartus.

There are a variety of other LPMs in the **IP Catalog** too. Let's first make sure that the

**IP Catalog** window is enabled; find this toggle in **View > Utility Windows > IP Catalog**



Within the **IP Catalog**, search for **MUX**. Double click on **LPM\_MUX**.



Laboratory Exercise Tutorial:

Design Entry Specified:

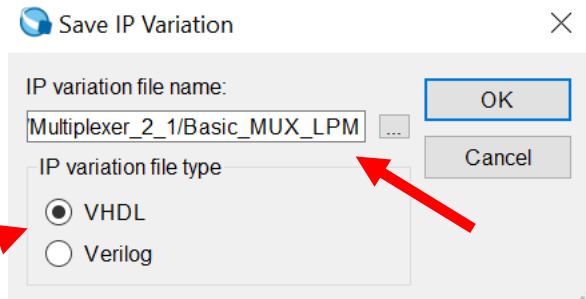
Schematic Diagram of digital circuits

Hardware Description Language (VHDL)

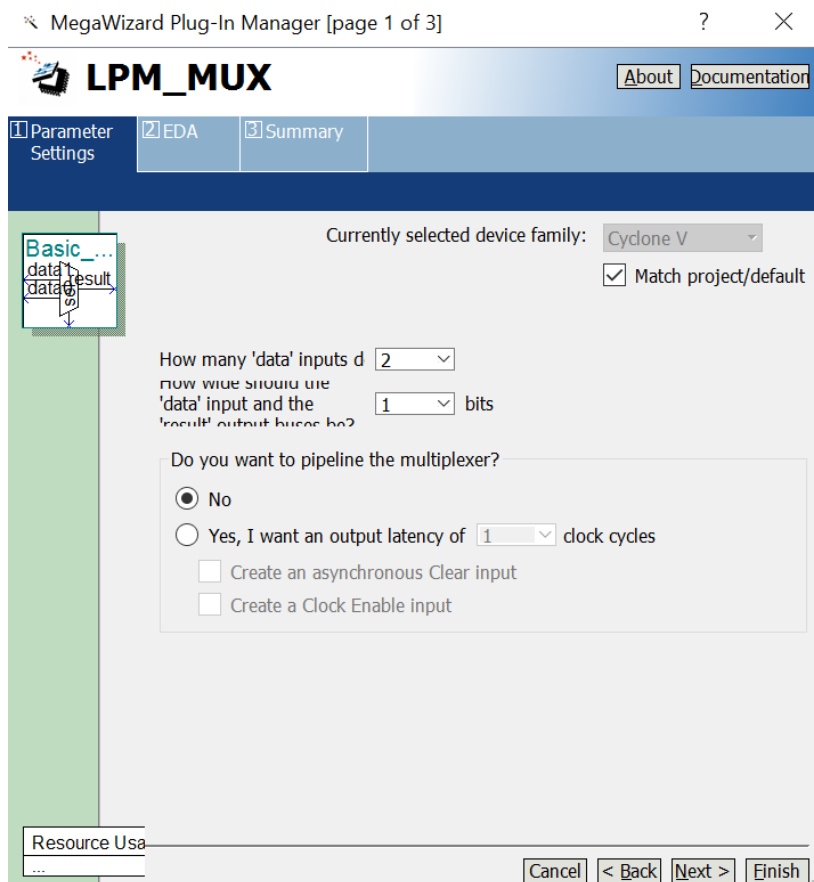
VHDL with LPM( Library Parameterized Modules)

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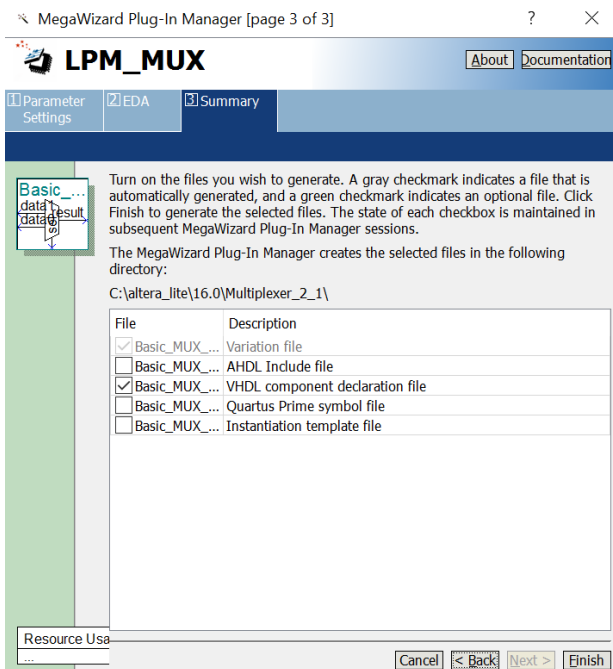
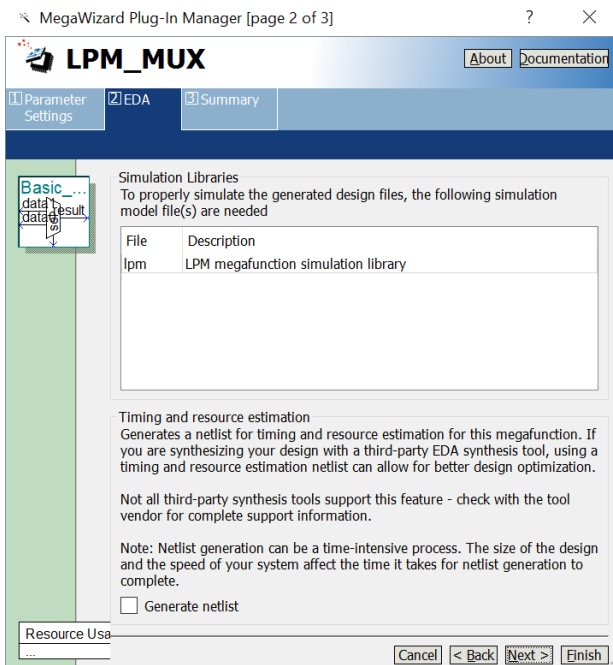
This time you will be able to change the filename. I chose **Basic\_MUX\_LPM.vhd**, make sure it is not the same as your other files, even if they are block diagrams. Again, choose **VHDL** as the file type.



The **MegaWizard** window will open, make sure your options are the same.

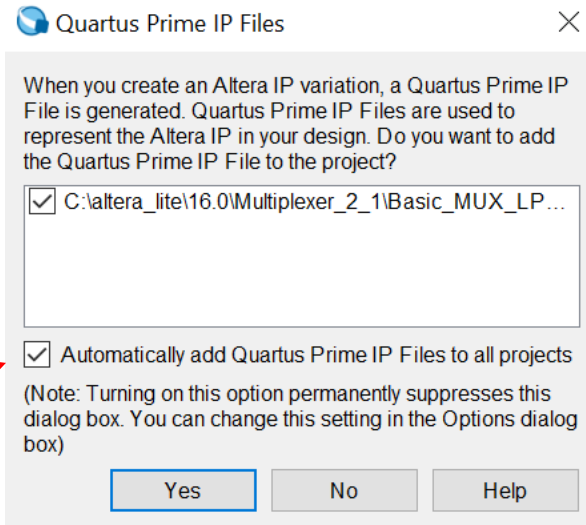


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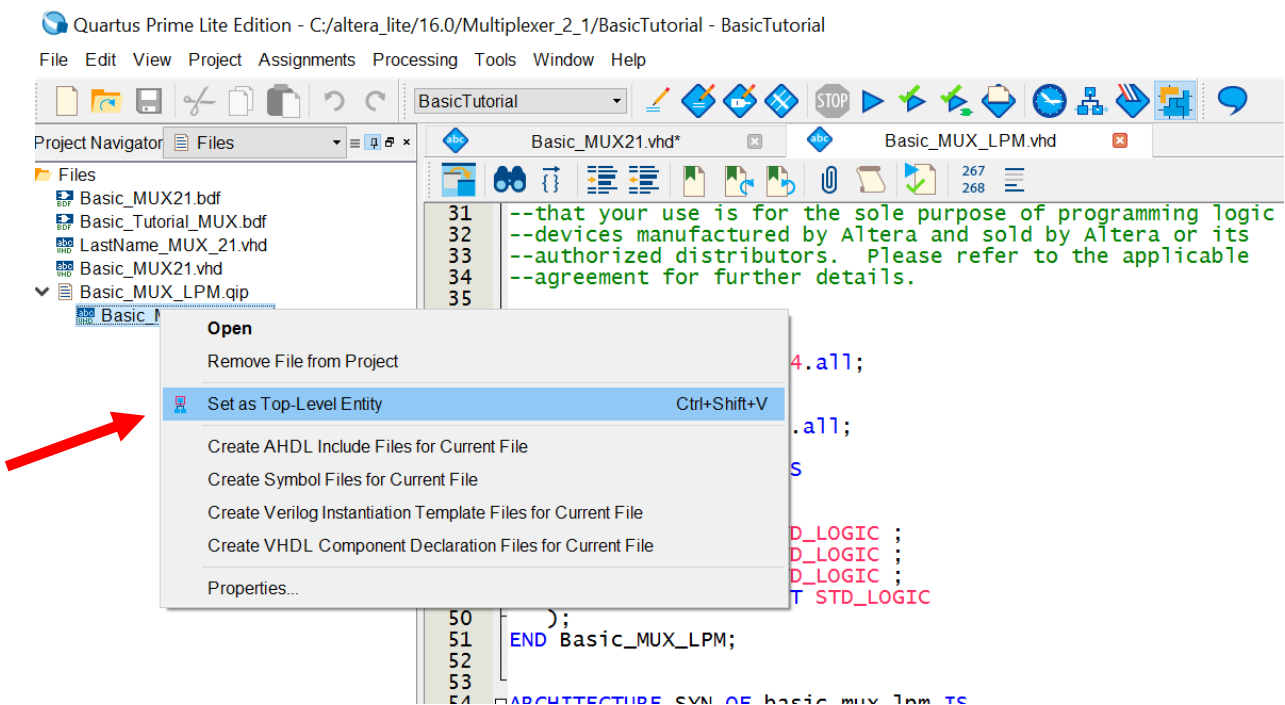


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Make sure the box is ticked.



Find the new file in the **Files** tab, set it as the top-level entity, and compile.



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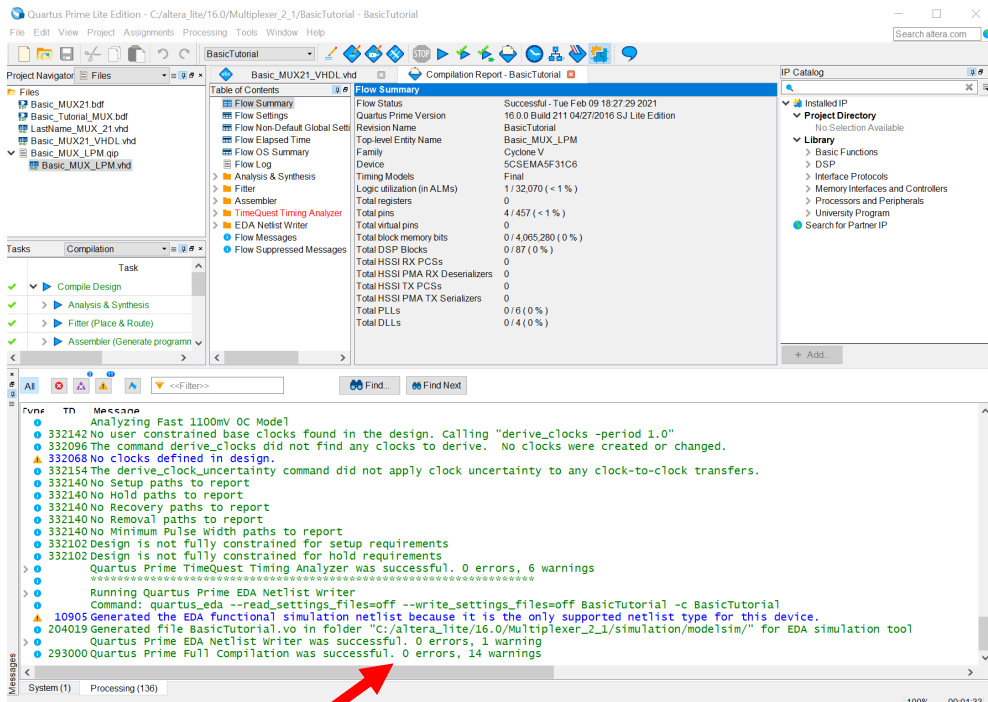
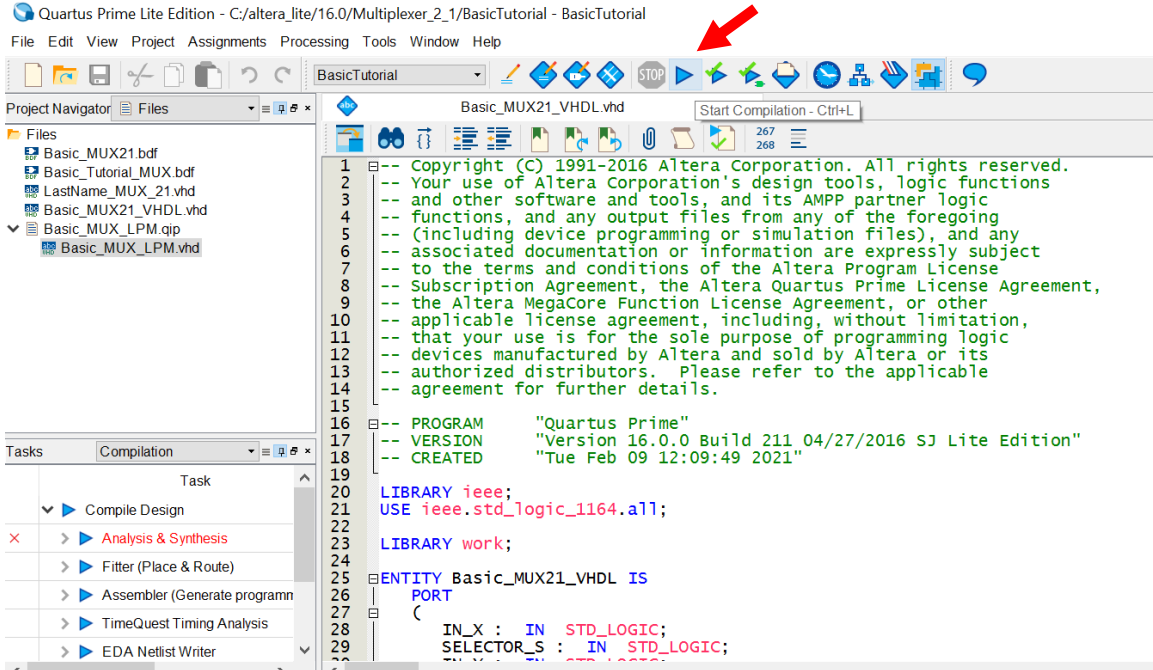
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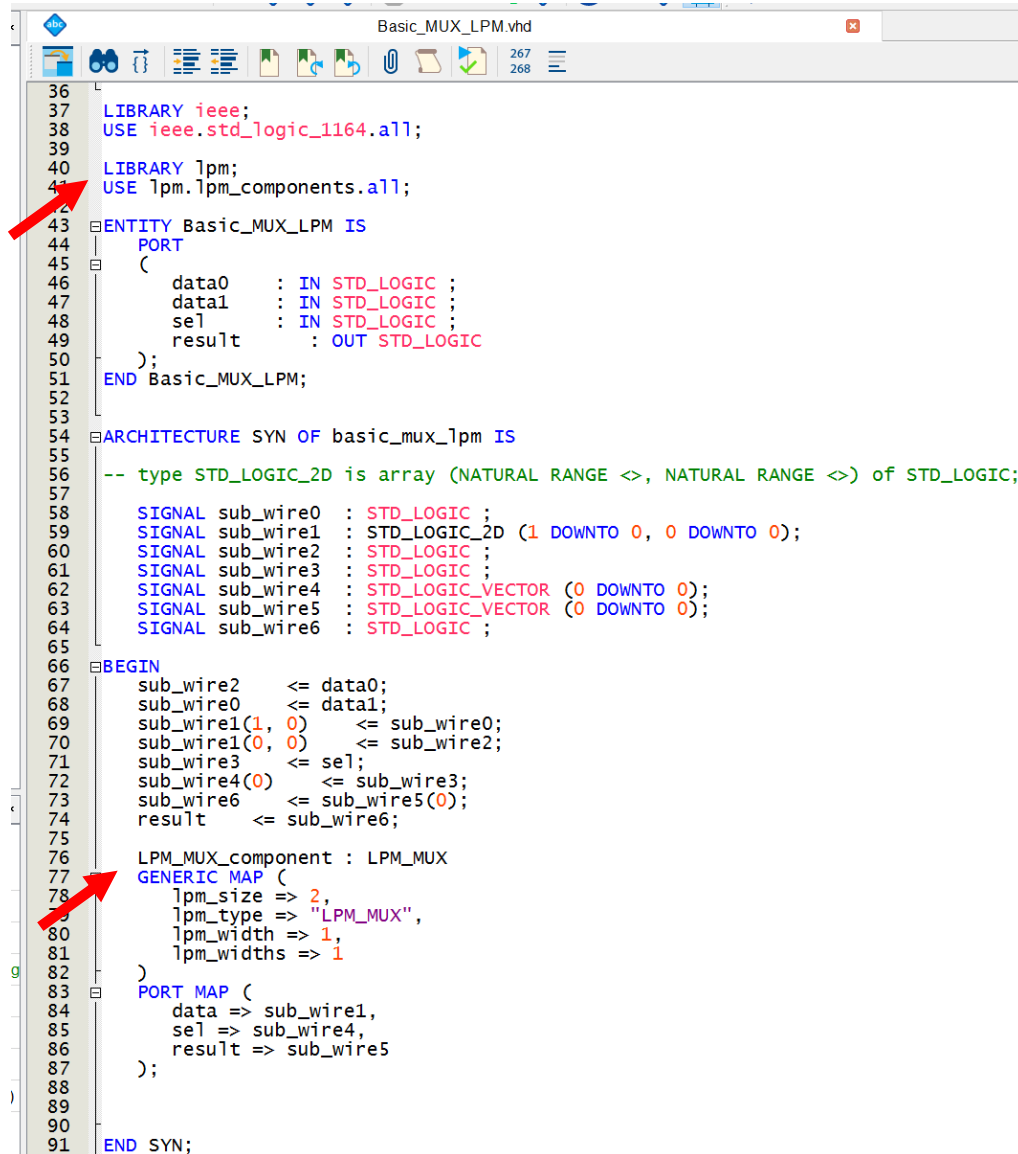
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The code generated by Quartus looks more complex than the VHDL implementation we wrote by hand for a 2:1 Multiplexer. This is because the Quartus version is adapted to handle larger input sizes (for example 4:1 or 8:1).



```

36
37 LIBRARY ieee;
38 USE ieee.std_logic_1164.all;
39
40 LIBRARY lpm;
41 USE lpm.lpm_components.all;
42
43 ENTITY Basic_MUX_LPM IS
44     PORT
45     (
46         data0      : IN STD_LOGIC ;
47         data1      : IN STD_LOGIC ;
48         sel        : IN STD_LOGIC ;
49         result     : OUT STD_LOGIC
50     );
51 END Basic_MUX_LPM;
52
53
54 ARCHITECTURE SYN OF basic_mux_lpm IS
55
56     -- type STD_LOGIC_2D is array (NATURAL RANGE <>, NATURAL RANGE <>) of STD_LOGIC;
57
58     SIGNAL sub_wire0 : STD_LOGIC ;
59     SIGNAL sub_wire1 : STD_LOGIC_2D (1 DOWNTO 0, 0 DOWNTO 0);
60     SIGNAL sub_wire2 : STD_LOGIC ;
61     SIGNAL sub_wire3 : STD_LOGIC ;
62     SIGNAL sub_wire4 : STD_LOGIC_VECTOR (0 DOWNTO 0);
63     SIGNAL sub_wire5 : STD_LOGIC_VECTOR (0 DOWNTO 0);
64     SIGNAL sub_wire6 : STD_LOGIC ;
65
66 BEGIN
67     sub_wire2 <= data0;
68     sub_wire0 <= data1;
69     sub_wire1(1, 0) <= sub_wire0;
70     sub_wire1(0, 0) <= sub_wire2;
71     sub_wire3 <= sel;
72     sub_wire4(0) <= sub_wire3;
73     sub_wire6 <= sub_wire5(0);
74     result <= sub_wire6;
75
76     LPM_MUX_component : LPM_MUX
77     GENERIC MAP (
78         lpm_size => 2,
79         lpm_type => "LPM_MUX",
80         lpm_width => 1,
81         lpm_widths => 1
82     )
83     PORT MAP (
84         data => sub_wire1,
85         sel => sub_wire4,
86         result => sub_wire5
87     );
88
89
90
91 END SYN;

```

Notice also that there are no logical statements above. The main action is happening behind the scenes within the **LPM Library**.