CS 343, Spring 2021

Self-Check 3B

TUTORIAL Introduction to Test_bench VHDL using ModelSim software tools using as an example digital N bit ADDER / Subtractor circuits

Instructor: Professor Izidor Gertner

Spring Semester , 2021

Objective

Testbech for N bit adder / subtractor

To write testbench file in VHDL to verify correctness of N bit adder/ subtractor unit. You must verify the correctness for signed integers.

In addition

1. Testbench file has to verify if an operation sets correctly the OVERFLOW bit.
2. Testbench file has to verify if an operation sets correctly the ZERO bit.
3. Testbench file has to verify if an operation sets correctly the NEGATIVE bit.

Do the above For N=4, 16, 32 bits.

e.g. for N=4 we 256 have 256 possible inputs.

To demonstrate that your test bench code is correct, you can introduce an error in your design file and show that your test bench code detects the error, prints out the input values, and the expected correct value, corresponding simulation time.

Enhanced Testbech for N bit comparator unit

1. Create a testbench file for compartos based on the template given here.
2. It is often required to locate a word stored in an array of size N. Each element in an array 32 bit word. In order to locate the word in an array, you compare query word with every element in an array until you find it.

   In VHDL, créate an array of size N. Each Word in the array is 32 bit. Create a digital ciurcuit in VHDL that locates the query Word.

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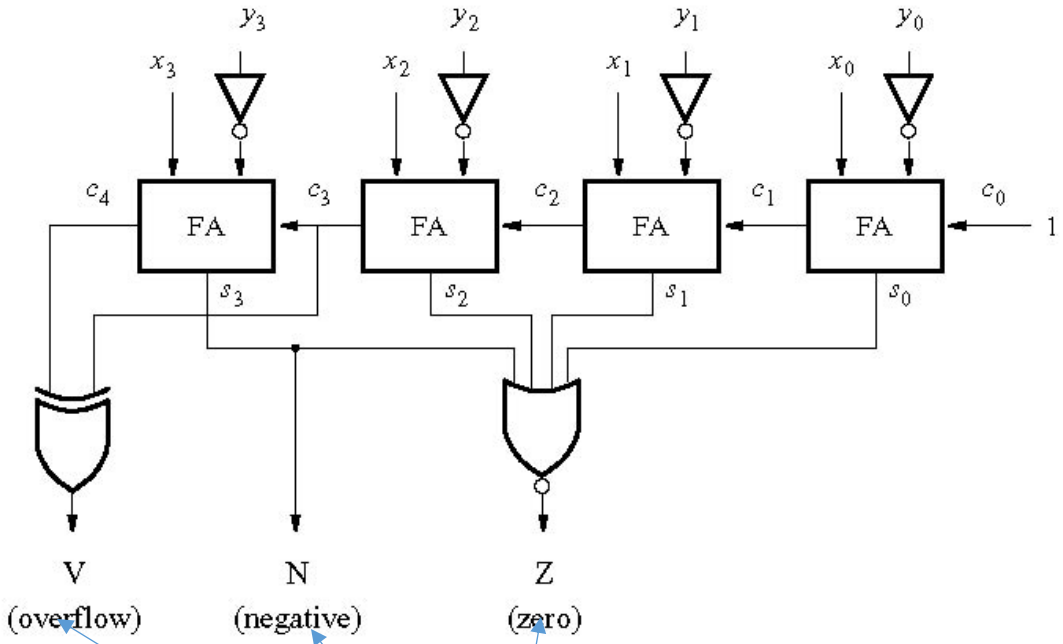

Figure 1. 4 Bit Comparator circuit. It outputs 4 FLAGS: V,N,Z.

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1. Template for test_bench file for My4Bit adder using MODELSIM Tool

1.1 ModelSim installation(REVIEW):

ModelSim is a multi-language HDL simulation environment by Mentor Graphics, for simulation of hardware description languages such as VHDL and Verilog. Simulation is performed using the graphical user interface (GUI), or automatically using scripts.

For this part you must have ModelSim installed in your computer. Altera gives you the choice to download ModelSim as bundle when you download Quartus from their website.

- If you followed our tutorial on installing Quartus and ModelSim, you are ready to go and you can ignore the bullet point bellow. (Alternatively, if you haven't installed any of these programs, please follow our tutorial on Quartus and ModelSim download and setup, then come back to this lab).

- If you have Quartus installed but not ModelSim, you can download it independently from their website, just make sure you choose the same version of Quartus you already have in your computer before starting download. Go to:

  http://dl.altera.com/?edition=subscription&product=modelsim_ae#tabs-2

  The following shows the download page from Altera. It is important that you know which version of Quartus you have installed in your computer. If you don't know, open up Quartus, then go to **Help > About Quartus II**

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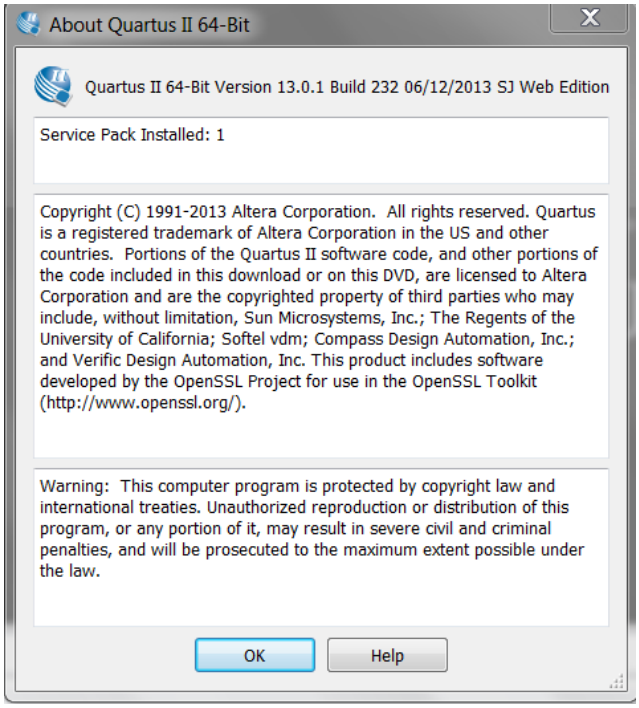

Figure 6. Screenshot of our Quartus version.
Our version is 13.0 service pack 1, yours may be different.

The next screenshot shows the download page for the Quartus software. Notice that at the top it says Subscription Edition although you may have downloaded the Free Web edition. This is irrelevant: it doesn't matter if it is part of the FREE or SUBSCRIPTION edition, ModelSim as a component is the same for both editions. Make sure you are logged into your Altera account (since you installed Quartus, we assume you have an account already with them).

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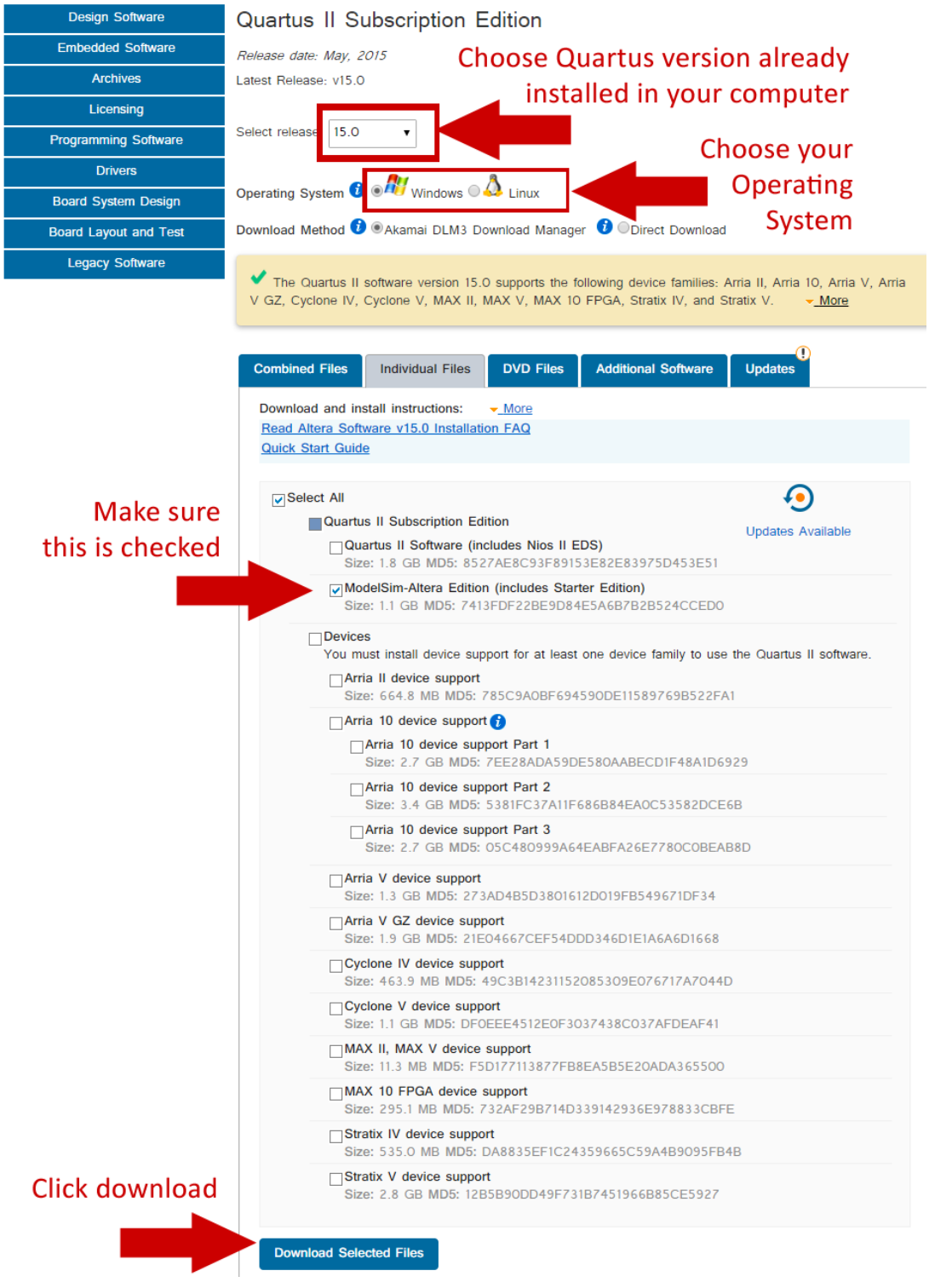

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Figure 7. ModelSim download page

1.2 ModelSim basics (REVIEW):

1. Open ModelSim. To run ModelSim, go to terminal and type vsim. This tutorial was done on a Windows environment, so we will show the corresponding Windows system screenshots but other operating systems should follow similar steps.

   If you are on Windows go to **Start > Run**. Type in "cmd" (without quotes) in the input field, then hit **Enter**. Alternatively, you could also search for Command Prompt in the search field in the Start Menu.
   If you are on Linux, right click your desktop and click Terminal.

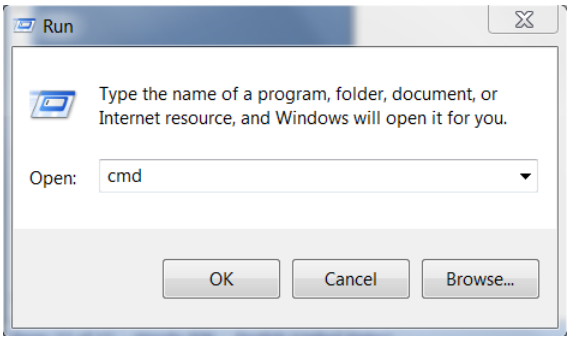

Figure 8. Run Command in Windows

2. In terminal type "vsim" (without the quotes).

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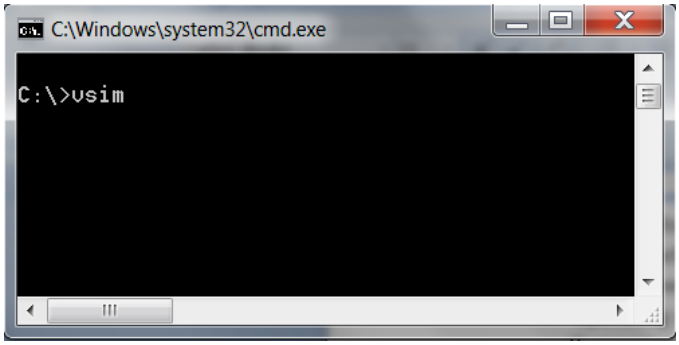

Figure 9. Terminal and ModelSim start command

You are now taken to the main screen of ModelSim, a Welcome splash screen will appear and you are now ready to start testing your circuit designs.
The initial screen of ModelSim is shown below:

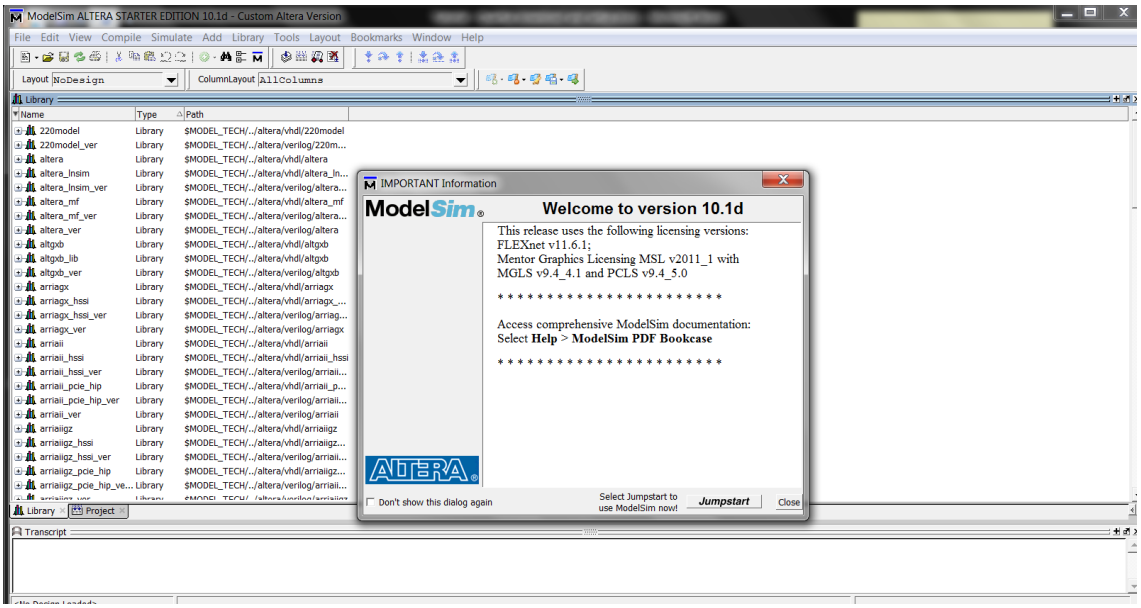

Figure 10. ModelSim Welcome screen

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3. When the Welcome screen appears, hit Close. Now go to Now go to ***File > New > Project.*** If a message appears asking if you want to close the current project just accept.
4. The Create New Project dialog appears, enter a name for your project, you can call it **Test_Bench_LastName_My4Bit adder**. See figure 11.
5. Browse a location for your new project.
6. In the Default Library Name, if empty, call it **work**.

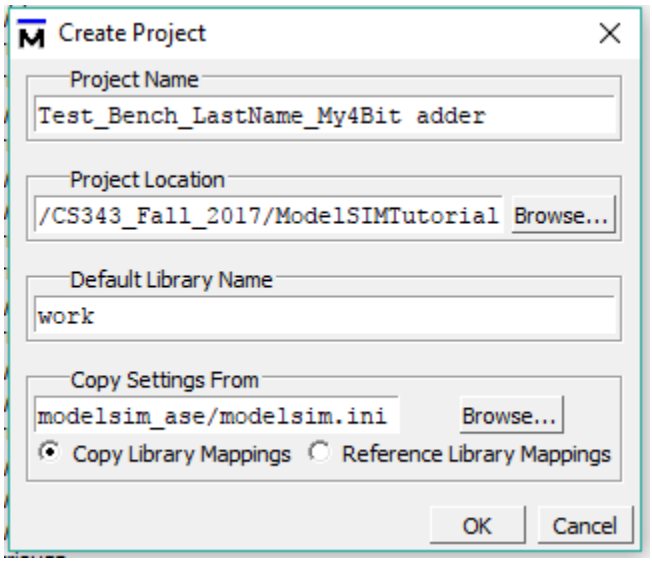

Figure 11. Create New Project dialog in ModelSim

7. The Add items to project dialog appears (See figure 12). In the previous lab we described the 4 bit adder and all components we are going to implement test_bench and we gave you the VHDL code for it. Right now we are going to create a new VHDL file and copy-paste the given code to it. Click **Create New File**.

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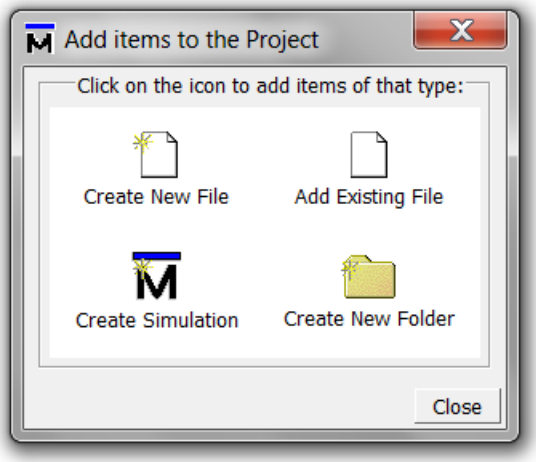

Figure 12. Add items dialog

In the same directory where you design files are stored, CREATE a TESTEBENCH file for 4 bit adder following example below.

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VHDL CODE for test_bench_4BIT adder

```
--test_adder4pckg.vhd

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use ieee.std_logic_unsigned.all;
USE work.fulladd_package.all ;

entity test_my4add is
end test_my4add;

architecture arch_test of test_my4add is
--componengt declaration for the Unit Under Test
component my4add
          PORT (Cin: IN STD_LOGIC;
             X,Y: IN STD_LOGIC_VECTOR(3 DOWNTO 0);
             Sout: OUT STD_LOGIC_VECTOR(3 DOWNTO 0);
             Cout: OUT STD_LOGIC );
end component;

signal A,B,S :STD_LOGIC_VECTOR(3 DOWNTO 0);
signal  Ci,Co :STD_LOGIC;
begin
-----Instantiate the Unit Under Test (UUT)
uut: my4add port map (
     Cin => Ci,
     X   => A,
```

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```
        Y    => B,
     Sout    => S,
     Cout =>Co
);
---- Test Bench ---User Defined Process
tb : process
begin
--Hold reset state for 100 ns
wait for 100 ns;
report "Hello Simulator";
A<="0000";
B<="0000";
Ci<='0';
--Loop over all values of A
for I in 0 to 2 loop
--Loop over all values of B
     for J in 0 to 2 loop
         --Wait for output to update
          wait for 10 ns;
```

---report " the A+B = " & integer'image(to_integer(unsigned((A+B))));
---The statement below checks for ALL possible input values if the ouput is correct.

```
assert (S = A+B) report "The sum from 4 bit adder is S= " &
integer'image(to_integer(unsigned((S)))) &
" while the expected  A+B = " &
integer'image(to_integer(unsigned((A+B)))) severity ERROR;
--Increment to the next value of B
B<=B+"0001";
end loop;
--Increment to the next value of A
A<=A+"0001";

--Echo to users test is finished
end loop;
```

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```
report "Test completed";
wait; -- will wait for ever
end process;
---END   User Defined Process
end arch_test;
```

8. Create all VHDL code for components and testBecnh file, compile all.
   Select Start Simlulation->Start Simulation

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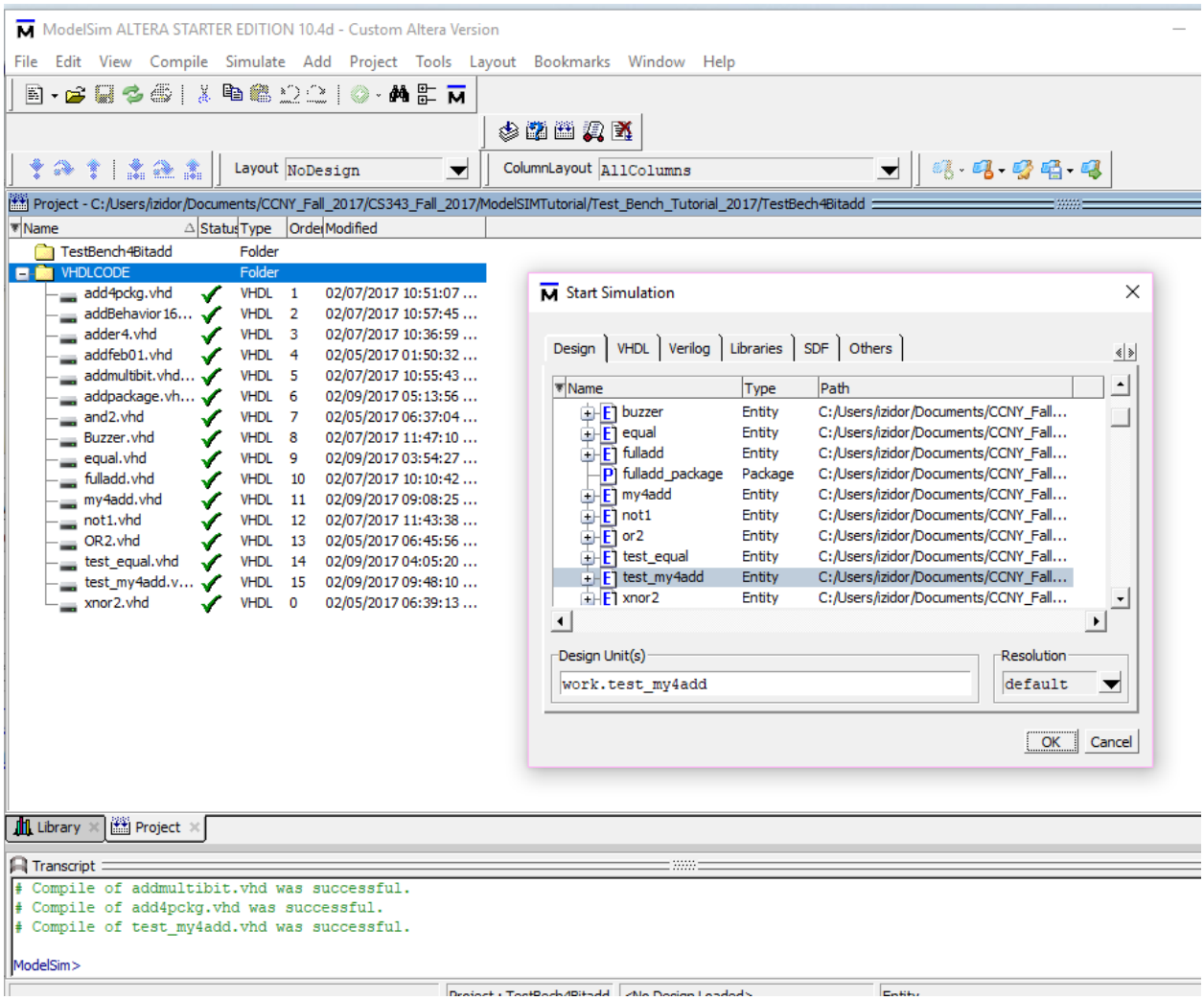

CLICK OK. You should get the following window

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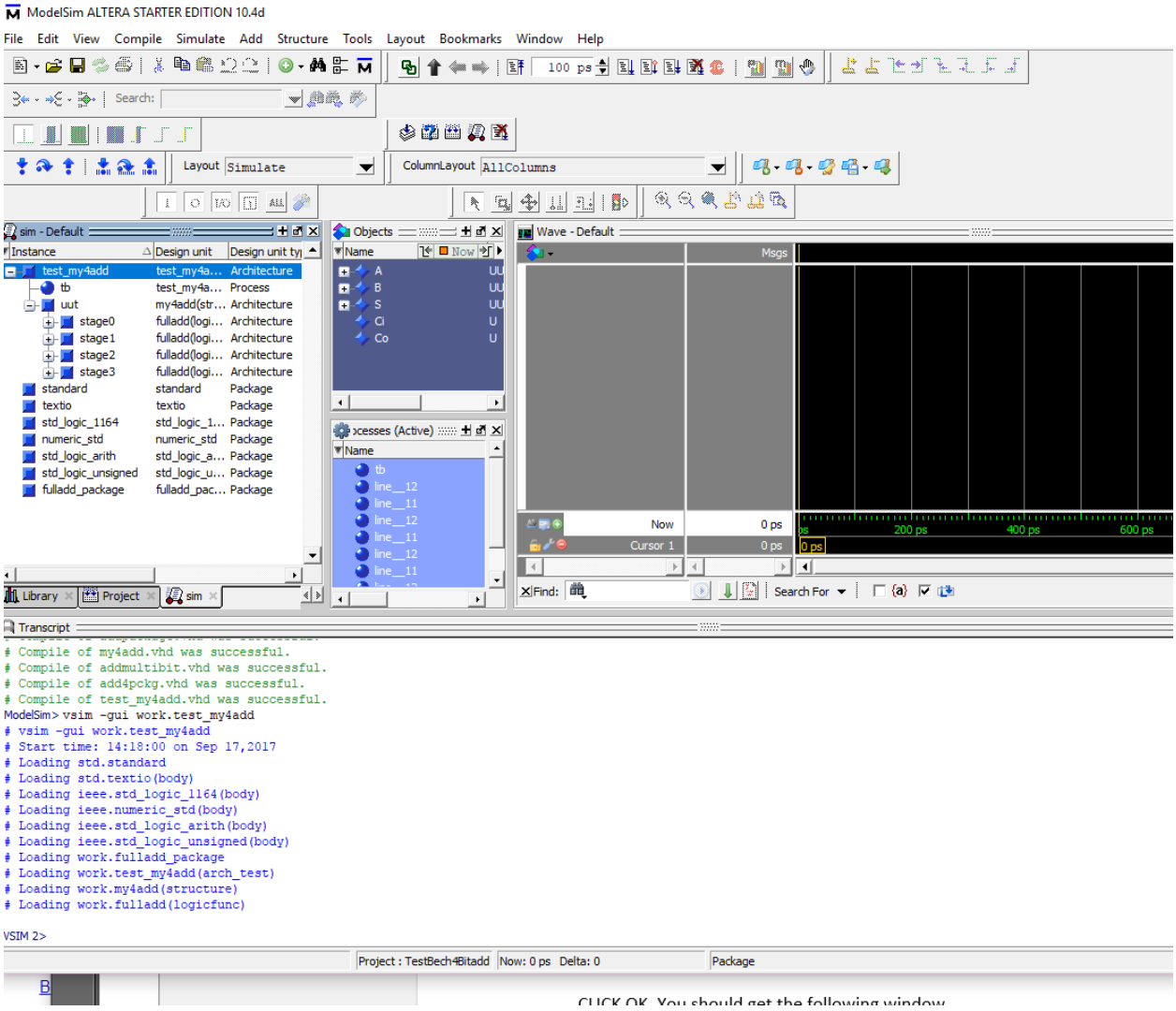

In the figure **UUT stands for Unit Under Test.**

Now you ready to run simulation.

9. **Simlutate->RUN and select one**
    a. **Run 100**
    b. **Run next**

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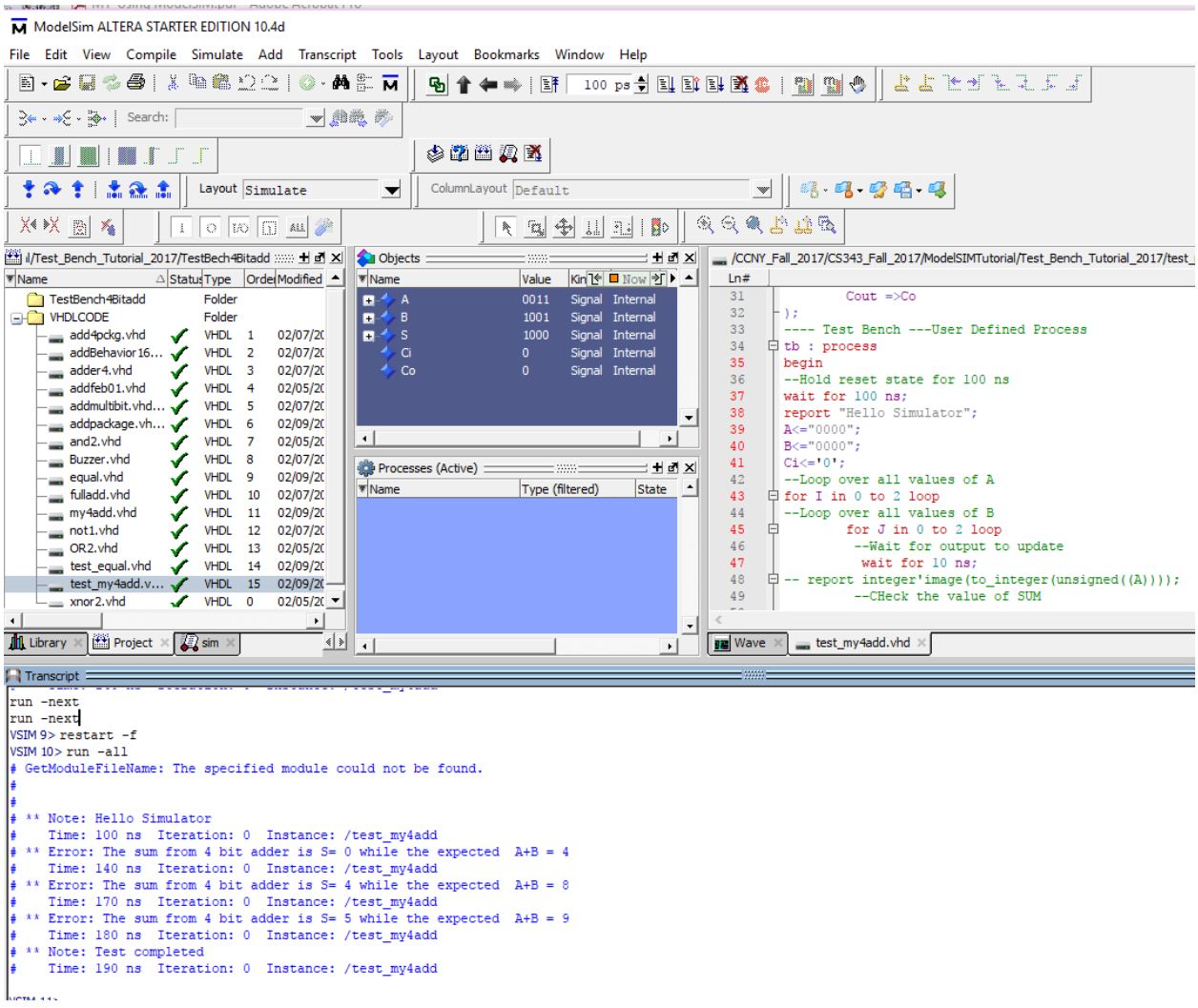
c. **Run all**

d. **Continue**

10. **In my example I run Run All.**

Errors are detected



To fnd an error I examine my design file my4bitadder.vhdl

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s/CCNY_Fall_2017/CS343_Fall_2017/ModelSIMTutorial/Test_Bench_Tutorial_2017/my4add.vhd (/test_my4add/uut) - Default

```
Ln#
 4  USE ieee.std_logic_1164.all ;
 5  USE work.fulladd_package.all ;
 6
 7  ENTITY my4add IS
 8          PORT(Cin : IN STD_LOGIC ;
 9               X, Y: IN   STD_LOGIC_VECTOR(3 DOWNTO 0) ;
10               Sout: OUT  STD_LOGIC_VECTOR(3 DOWNTO 0) ;
11               Cout: OUT  STD_LOGIC ) ;
12  END my4add ;
13
14  ARCHITECTURE Structure OF my4add IS
15          SIGNAL C : STD_LOGIC_VECTOR(1 TO 3) ;
16  BEGIN
17          stage0: fulladd PORT MAP ( Cin, X(0), Y(0), Sout(0), C(1) ) ;
18          stage1: fulladd PORT MAP ( C(1), X(1), Y(1), Sout(1), C(2) ) ;
19          stage2: fulladd PORT MAP ( X(2), X(2), Y(2), Sout(2), C(3) ) ;
20          stage3: fulladd PORT MAP ( C(3), X(3), Y(3), Sout(3), Cout ) ;
21  END Structure ;
22
```

I detect a typo in stage2. Carry in is signal X(2) and it should be C(2).

Easy fix. Recompile only myadd4bit.vhdl file.

You have to RESTART the simulation.

Then Run all

We get simulation completed, No errors!

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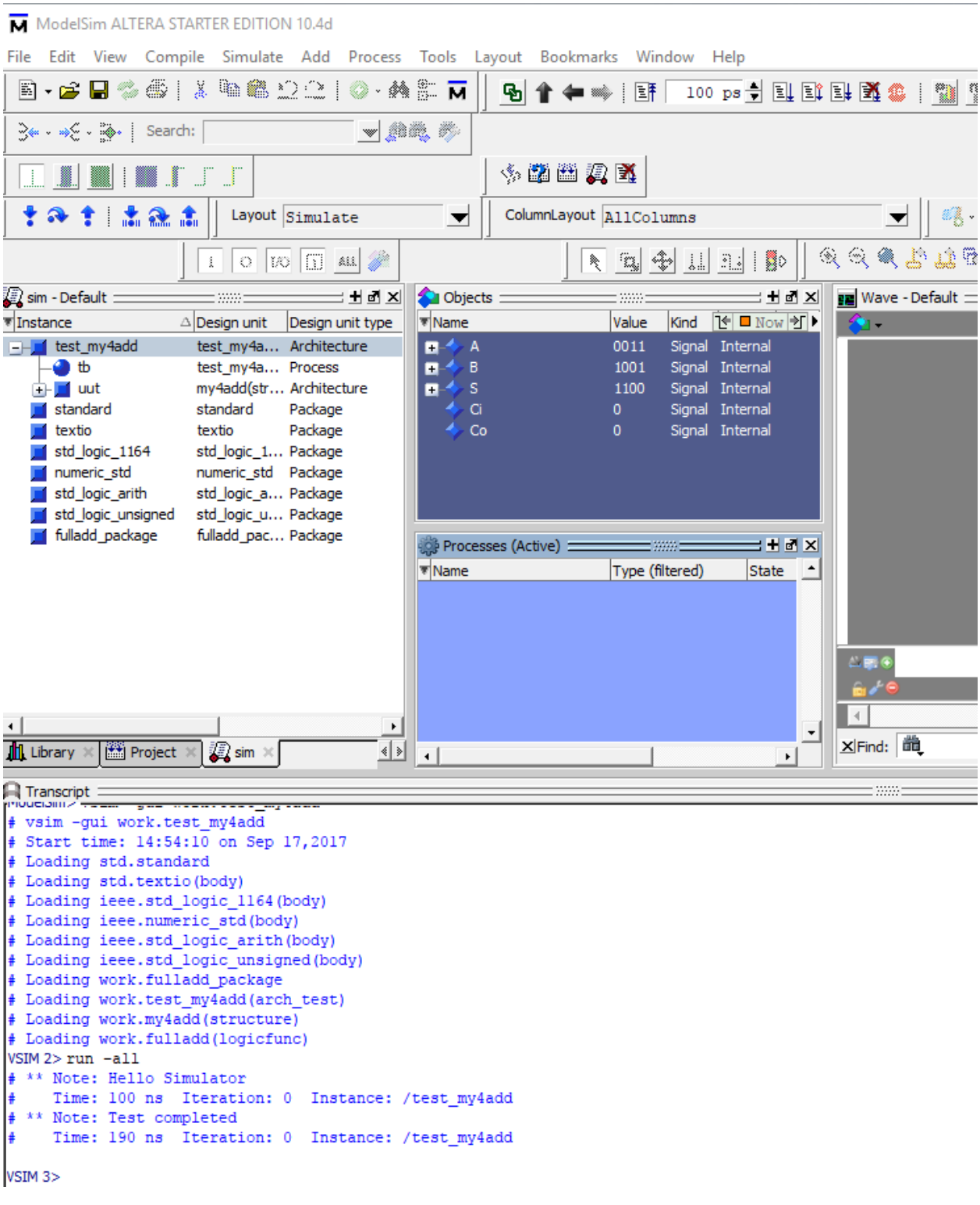

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As we can see no errors.
In the objects window we inspect A=0011 (+3). B= 1001 (-7).
Adder output S= 1100 (-4). The expected output A+B=0011 + 1001 = 1100.

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