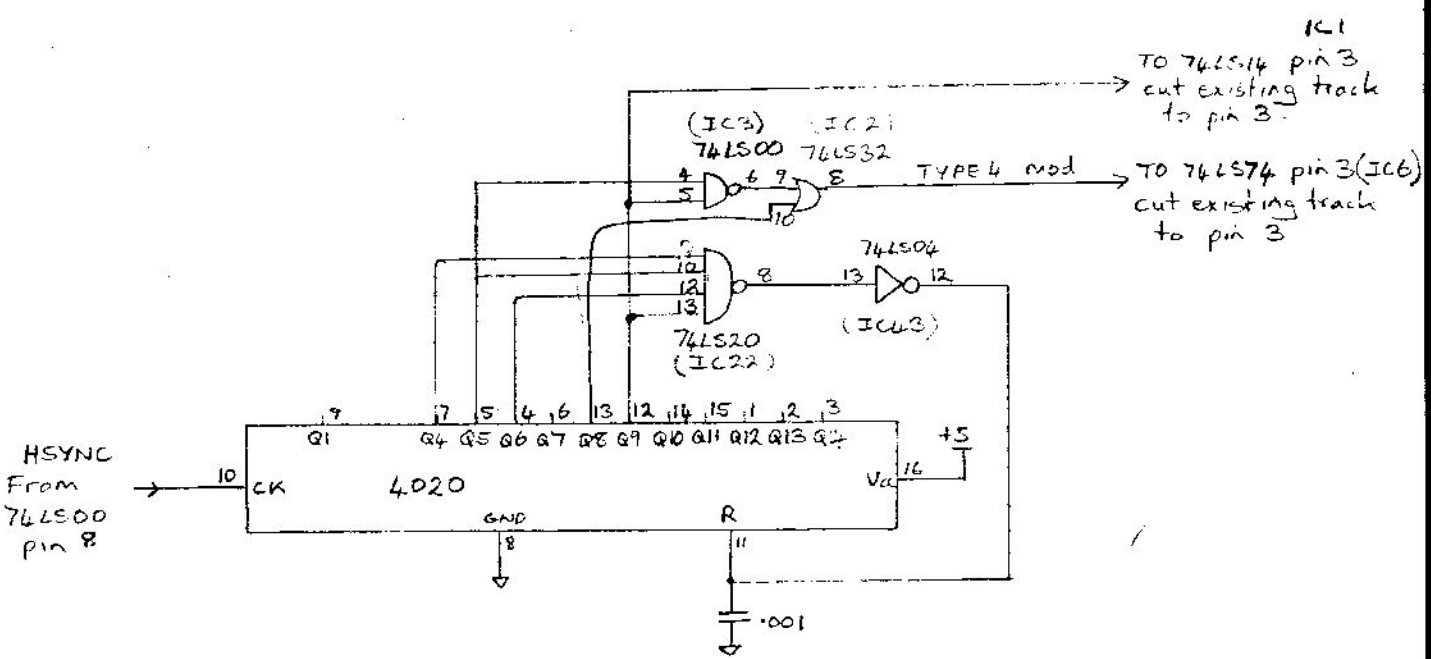
The Hows, Whys and Fixes for Pegasus "Jitter"

Recent investigations into the reasons and possible cures of Pegasus screen Jitter have revealed that there are at least 4 distinct causes. This report explains the theory behind these causes and suggests some modifications to erradicate the jitter.

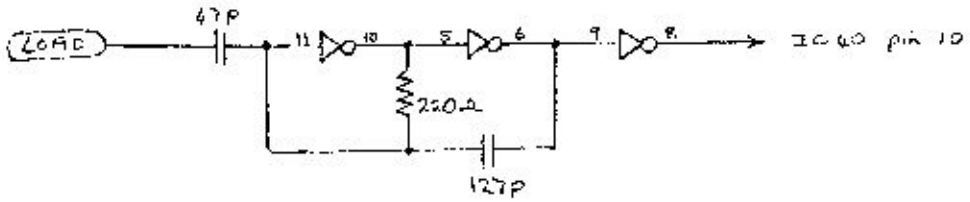
The 4 causes will be referred to as Types 1 to 4 respectively.

TYPE 1 JITTER

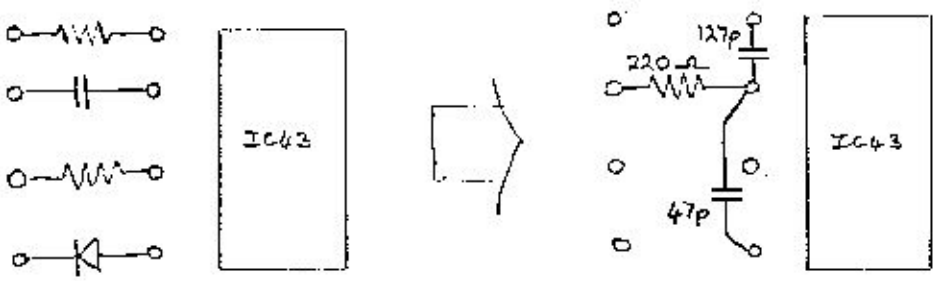
The frame rate for the video is initiated by a signal derived from the mains; Once the frame is started, everything is locked to the processor clock. So while the picture information doesn't jitter with respect to HSYNC and VSYNC, the frames themselves do jitter with respect to each other. In other words the VSYNC signals are not regular. Sometimes they are X x 64 us (HSYNCS occur every 64 us) apart and sometimes they are (X + 1) x 64 us apart. Normal TV sets have an oscillator which likes to look to regular VSYNC pulses. It will infact lock to a frequency with a period somewhere between X + 1 and X times 64 us. Then what you get is a picture sometimes slightly above and sometimes slightly below the true position. The cure is to use some kind of divider to derive your 50Hz from the processor clock, instead of the mains. The following mod uses one IC and some existing gates on the Pegasus board.



The 74LS20 gate has tracks running to it which must be cut. The 74LS04 becomes free from a modification to the dot clock oscillator which was given to us by G. Barbour of Christchurch. This modification stops shimmer on the displayed characters and stabilzes the oscillator frequency.



This modification only involves removing 4 components and replacing them with 3 components as shown.

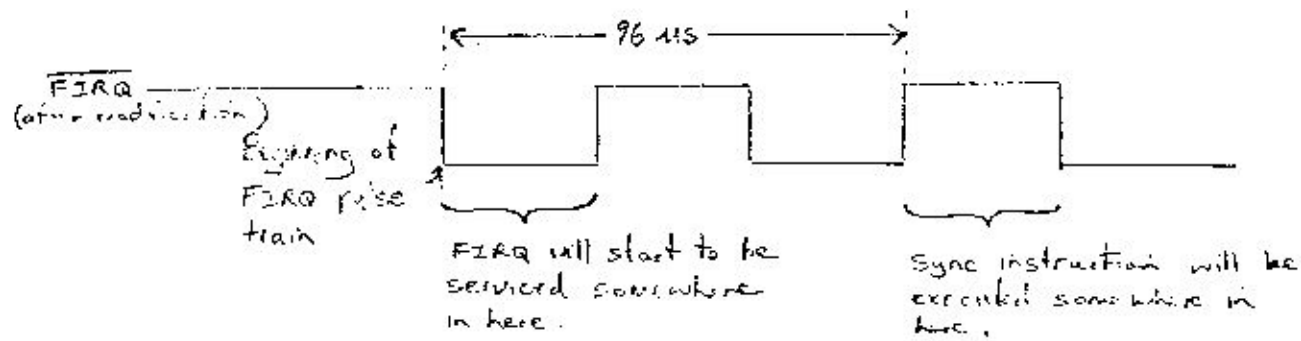


The IC43 gate at pins 13 and 12 is freed for use in the 4020 mod.

Type 2 Jitter

The FIRQ pulses generated by the existing Pegasus hardware are 8 us long. The 6809 chip however only checks the FIRQ pin after each instruction. Since 6809 instructions can take up to 20 us it is clear that it is possible for the chip to miss on FIRQ pulse. If it "sees" the following one then the whole picture will be 64 us too late i.e. one scan line too low on the screen. This causes jitter whenever programs with longish instructions are running.

The cure for Type 2 jitter is to take the FIRQs from the 74LS93 divider, IC7 pin 9. This is a square wave with 32 us each way. This modification also needs a new monitor version 2-3. The delays in this monitor are adjusted so that a) the picture is in the middle of the screen and b) the SYNC instruction is 96 us after FIRQ starts to be serviced. This ensures that the SYNC instruction is not executed while the FIRQ line is low, which would cause terrible sideways jitter.



From this drawing it can be seen that 32 us is the ideal length for the FIRQ pulse (which is active low) because it gives an equal mark space ratio square wave. If the FIRQ pulse were any longer, then the period in which the FIRQ line is high becomes correspondingly shorter and it is then possible for the SYNC instruction to occur while the FIRQ line is low, giving sideways jitter.

If the FIRQ pulse is shorter than 20 us it is possible for them to be missed by the processor. In fact the full 32 us is better because it allows the programmer to mask off FIRQs for two or three instructions if he wishes, without missing an FIRQ.

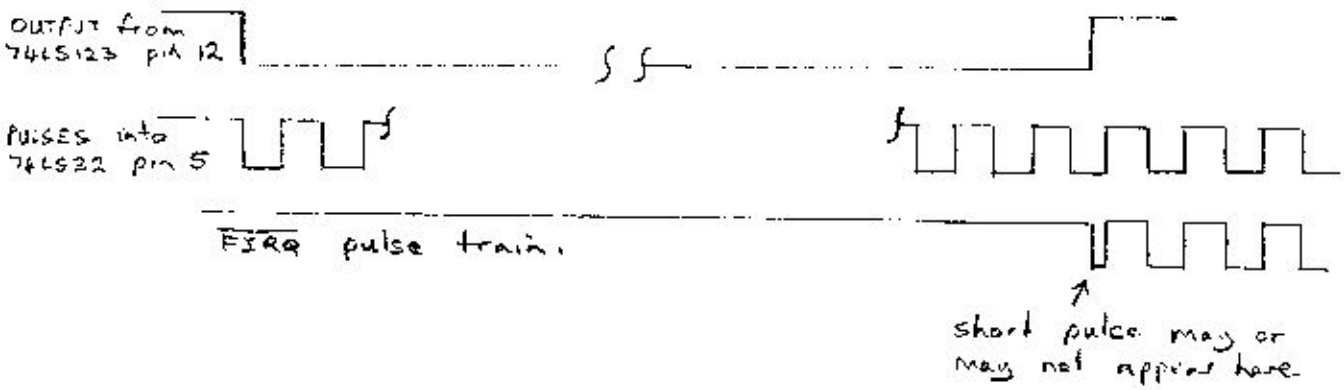
So 32 us FIRQs are used. The time from the start of servicing of the FIRQ to the SYNC instruction in the monitor is adjusted to be 96 us. Also since the new FIRQs are out of phase with the old ones, the monitor has its delay that positions the picture in the middle of the screen adjusted.

The actual modification is done by cutting the track to the IC2 74LS32 pin 5 and jumping this pin to the 74LS93 pin 9 (IC7) and getting a version 2-3 monitor.

NB: Fixing type 2 jitter actually increases the probability of type 3 jitter.

Type 3 jitter

The timing from the VSYNC pulse to the start of the FIRQ burst of pulses is done by a 74LS123 one - shot. The delay is approx 3 ms, and since this is timed from an R-C network it cannot be set accurately. If the end of the delay comes during the time that the FIRQ pulse is low, then a small FIRQ pulse will be given to the processor before the burst of full length ones.



Since the pulse can be very short the processor may or may not "see" it. The 123 delay drifts with time and so the jitter will come and go.

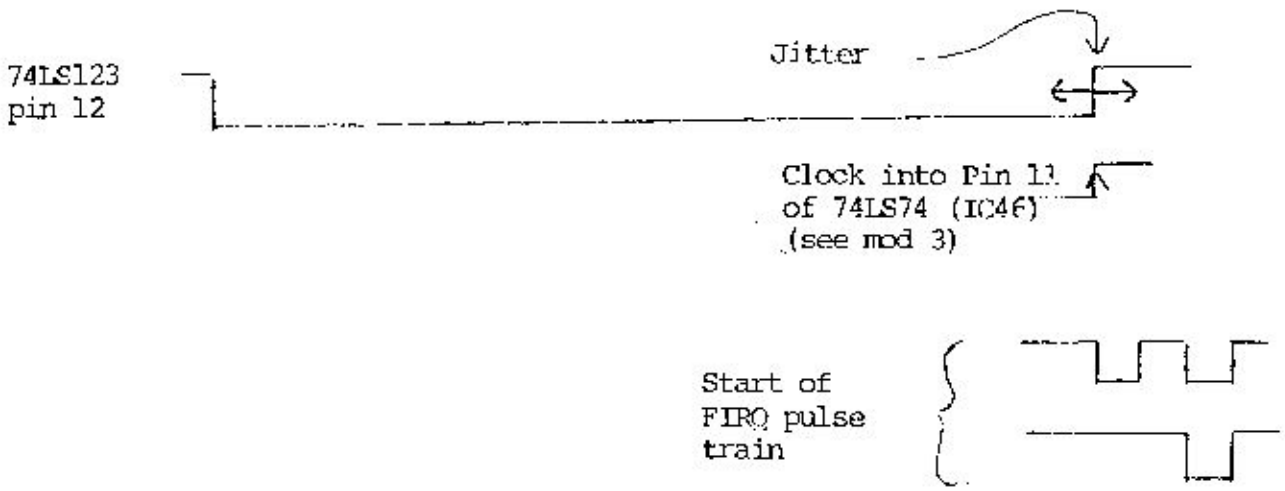
The cure is to clock IC46 b with FIRQ pulses instead of E. This F/F is redundant as it is anyway. The existing track to the 74LS74 pin 11 (IC46) cannot be cut as it is underneath the IC Instead it must be cut in two places and then 2 jumpers need to be put in.

Cut the track running from IC46 pin 11 to the system PIA pin 25 and also cut the track running from IC46 pin 11 just before the hole where it goes through the board and on to pin 3 of the 74LS04 oscillator. (IC43). Now join this hole back to the PIA pin 25. Now join IC46 pin 11 to the 74LS32 pin 5 (IC2). Note that this half of IC46 does not appear in the drawings but it is used in the circuit.

NB: Type 3 jitter is also cured by the type 4 mod if using the 4020 I.C.

Type 4 jitter

Type 4 jitter is again caused by the 74LS123. Using an oscilloscope it can be seen that a noticeable jitter occurs in the delay pulse whenever the Pegasus is running a program. When the trailing edge of the pulse falls on or near the clocking point explained for type 3 mod then the jitter in the 123 will cause the first FIRQ pulse to appear sometimes latter and sometimes earlier.



The only way to get round this is to bypass the 74LS123 altogether and use some pulses derived from the Type 1 jitter mod. (see the drawing for the 4020 mod). The existing track to 74LS74 IC6 pin 3 must be cut and taken to the spare nand gate as shown. This will give a picture nicely in the middle of the screen. (vertically)

SUMMARY OF JITTER MOD. COMBINATIONS

Requires 4020 mod new monitor	1,2, 4
Requires new Monitor only	2 & 3
Requires nothing	3
Requires 4020 only	1, & 4

All 3 modifications are needed to get a really rock solid picture all the time.

Modifications 2 & 3 are relatively simple to do and we recommend that they be done as they do contribute some improvement.

They will be done on all Pegasi going out from now on.