Method for reducing false positives using pattern binning based on unsupervised learning

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ABSTRACT

Semiconductor inspections face the challenge of maintaining high sensitivity for detecting defects while minimizing false positives. Distinguishing small defects from manufacturing variations such as line edge roughness becomes increasingly difficult as process shrinking continues. To effectively address this challenge, it is essential to adjust the detection sensitivity in accordance with the characteristics of the circuit pattern. We have developed a method for classifying circuit patterns using unsupervised segmentation techniques applied to SEM images. This approach enables automatic discrimination of areas such as memory cell regions and peripheral circuit pattern regions without requiring design data. By adjusting the sensitivity depending on the pattern region, the proposed method is able to reduce false positives by over 90% for memory devices.

Keywords: Visual Inspection, False Positive Reduction, Image Segmentation, Unsupervised Learning

1. INTRODUCTION

In-line wafer inspection systems are utilized to detect defects and identify the causes of abnormalities that occur early in the manufacturing process.[1] In these systems, an imaging device with a microscope captures and detects defects from images. The importance of using a scanning electron microscope (SEM) for visual inspection to detect small defects in semiconductor manufacturing is increasingly recognized. In general, when the sensitivity of defect detection is increased to identify small defects on the nanometer scale, it often results in a higher number of false positives due to manufacturing variations in the circuit pattern. The main challenge in defect inspection is how to suppress false positives caused by manufacturing variations while detecting defects with high sensitivity.

Distinguishing small defects from manufacturing variations, such as line edge roughness, becomes more challenging as processes continue to shrink. Therefore, this research aims to develop image processing technology capable of achieving both highly sensitive defect detection and effective false positive suppression.

2. REDUCING FALSE POSITIVES USING PATTERN BINNING

Defect inspection equipment identifies the locations of defects in captured images through image processing. A common approach is to calculate the gray-level difference between the input image and the reference image and then extract areas where this difference exceeds a defined criteria as candidate defects. For the extracted candidate defects, the system discriminates between real defects and false positives, outputting only those identified as real defects. A simple processing method involves quantifying the likelihood of a defect candidate being an actual defect as an anomaly score and then discriminating by applying a threshold to score. However, as critical defects become smaller and more similar in size to manufacturing variations, it is increasingly difficult to sufficiently reduce false positives using only threshold-based processing of anomaly scores.

A discriminator, particularly one utilizing supervised machine learning, is effective in reducing false positives. However, reducing annotation costs remains a significant challenge, as user annotation is often required for many

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defects to enhance classification accuracy. In addition, a method has been demonstrated that focuses on the characteristic that the required inspection sensitivity varies depending on the inspection area.[2] It adjusts the sensitivity according to inspection areas classified based on design information to improve detection accuracy.

In this study, we propose machine learning-based segmentation technology to classify inspection areas without requiring additional information such as design data or user annotations. By adjusting sensitivity for each segment, it becomes possible to achieve both enhanced detection sensitivity and reduced false positives. Fig. 1 illustrates the flow of the defect detection process with sensitivity adjustment applied using this method. The image is divided into multiple segments based on the appearance of the circuit pattern such as the cell area, peripheral circuit, and intermediate area. Since false positives frequently occur in areas with significant manufacturing variations, such as the intermediate area, lowering the detection sensitivity of the segments corresponding to the intermediate area can effectively reduce the occurrence of false positives.

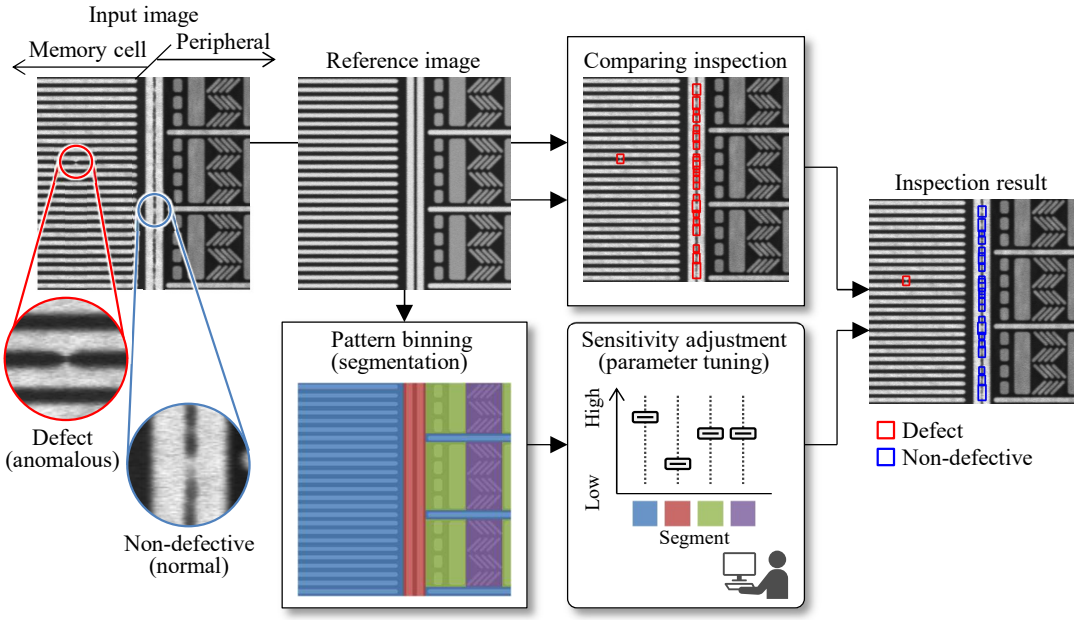

Figure 1. False positive reduction based on segmentation technique

3. PATTERN BINNING METHOD BASED ON UNSUPERVISED LEARNING

In recent years, deep neural networks have led to significant advancements in performance for many tasks, including image classification and segmentation. However, achieving a high performance requires a large amount of user-provided data with accurate labels. In particular, image segmentation requires precise pixel-level annotation, which is an extremely labor-intensive and costly process. In the context of this research, which focuses on circuit pattern segmentation, accurate pixel annotation based on the appearance of various elements like memory cells, peripheral areas, and intermediate areas is essential. Circuit patterns vary in appearance depending on the device and layer, and these appearances are likely to evolve with changes in the manufacturing process. Consequently, it is impractical to pre-learn all circuit patterns, making it necessary to adapt learning directly on the production line. Given the high cost associated with manual annotation for segmentation, it is impractical to adapt on supervised learning methods. Therefore, leveraging image segmentation technology that utilizes unsupervised learning becomes crucial to reduce false positives and manage costs effectively.

Invariant information clustering (IIC),[3] which utilizes mutual information, has been proposed as a technique for clustering and segmenting images without the need for user annotations. IIC employs a deep neural network as the discriminator to achieve high classification accuracy and can be trained to optimize mutual information without user-provided labels. In this study, we have developed an image segmentation process for semiconductor

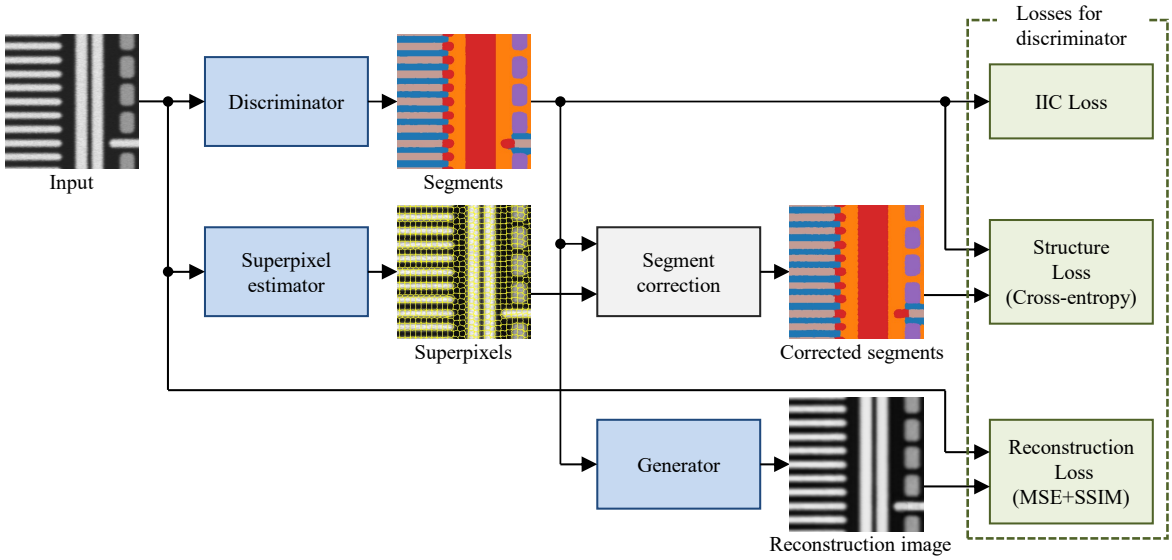

Figure 2. Training architecture of proposed segmentation process.

circuit patterns utilizing the IIC method. This approach allows us to effectively segment complex patterns without relying on extensive manual labeling, thereby streamlining the process in a cost-effective manner.

Fig. 2 shows the architecture of the proposed segmentation process, where the discriminator $\mathcal{D}$ plays a crucial role. To enhance segmentation accuracy, we devised three learning losses for the discriminator: (a) IIC loss, (b) segment correction error, and (c) reconstruction error. The specific formulations for these learning losses are detailed in Eq. (1). Each loss will be thoroughly explained in the subsequent sections.

$$\mathcal{L}_{\text{discriminator}} = \mathcal{L}_{\text{IIC}} + \mathcal{L}_{\text{structure}} + \mathcal{L}_{\text{recon}} \tag{1}$$

3.1 IIC Loss $\mathcal{L}_{\text{IIC}}$

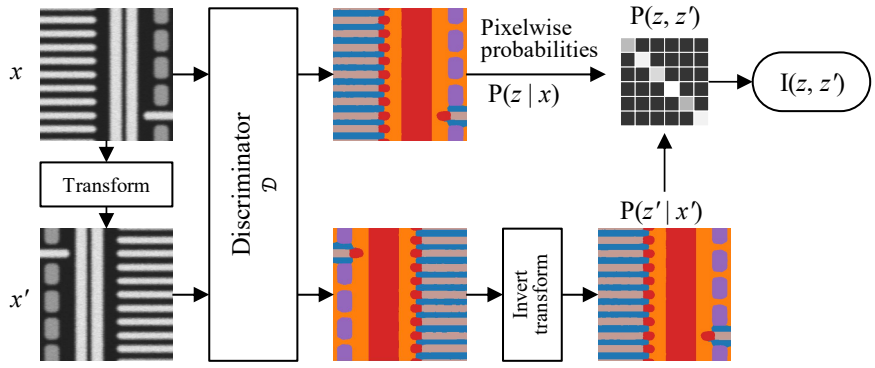

Figure 3. Calculation flow of mutual information for IIC based image segmentation.

The IIC method[3] assesses the mutual information between the classification results of two paired images. The process for calculating mutual information developed in this study is depicted in Fig. 3. To generate a pair of images, an image transformation is applied to the input image x to generate x'. In this example, the image is rotated by 180 degrees, but it can also be rotated by 90 degrees or flipped vertically or horizontally.

The output of the discriminator $\mathcal{D}_c(x) \in [0,1]^C$ can be interpreted as the probability distribution of a discrete variable z over C classes. Formally, it is expressed as $\mathbf{P}(z = c|x) = \mathcal{D}_c(x)$. At this stage, $\mathbf{P}(z' = c|x')$ is inverse-transformed to align with $\mathbf{P}(z = c|x)$. Now, consider a pair of segment assignment variables, z and

z', corresponding to two inputs, x and x'. Their conditional joint distribution is expressed as $\mathbf{P}(z = c; z' = c'|x, x') = \mathcal{D}_c(x)\mathcal{D}_{c'}(x')$: The mutual information $I(z, z')$ is calculated using Eq. (2) based on the conditional joint distribution $\mathbf{P}$. By maximizing the mutual information, the discriminator is trained to uniformly classify each pixel in the x and x' images into the same class. We define Eq. (3) as the loss function for the discriminator, enabling it to be optimized using SGD or Adam optimizers in combination with other loss terms.

$$I(z, z') = \sum_{c=1}^{C} \sum_{c'=1}^{C} \mathbf{P}_{cc'} \ln \frac{\mathbf{P}_{cc'}}{\mathbf{P}_c \mathbf{P}_{c'}} \tag{2}$$

$$\mathcal{L}_{\mathrm{IIC}} = -I(z, z') \tag{3}$$

3.2 Structural Loss $\mathcal{L}_{\mathbf{struct}}$

Refining the segmentation results using image processing techniques is an effective method for generating spatially continuous segments while minimizing the occurrence of small, noisy areas. One approach we explored involves the refinement of segments by using superpixels, which are calculated from the input image through the superpixel estimator $\mathcal{P}$. Superpixels can also be estimated using a fully convolutional network.[4] As a result of our investigation, we decided to refine the segments output by the discriminator using superpixels. We incorporated the error before and after refinement into the discriminator's loss function. Consequently, the discriminator is trained to directly output segments that have been refined using superpixels. This methodology not only ensures more accurate segmentation but also eliminates the need to calculate superpixels during the prediction step, effectively reducing processing time. The error before and after segment refinement is calculated using cross-entropy, as defined in Eq. (4).

$$\mathcal{L}_{\mathrm{struct}} = -\sum_{n=1}^{N} \mathcal{F}(\mathcal{D}(x_n), \mathcal{P}) \log(\mathcal{D}(x_n)) \tag{4}$$

3.3 Reconstruction Loss $\mathcal{L}_{\mathbf{recon}}$

If the segmentation result accurately reflects the structure of the circuit pattern, the input image can be reconstructed from the segmentation result. We developed an image generator that takes the segmentation result as input and produces a grayscale image as output. The grayscale difference between the input image and the reconstructed image serves as the reconstruction error, denoted as $\mathcal{L}_{\mathrm{recon}}$. Both the discriminator and the image generator are trained to minimize this error. The grayscale difference is quantified by Eq. (5), where $\mathcal{G}$ is the image generator, MSE is the mean squared error, and SSIM is the structural similarity.[5] Consequently, the training of the discriminator $\mathcal{D}$ is enhanced to produce segmentation results from which the image generator $\mathcal{G}$ can accurately reconstruct the input image.

$$\mathcal{L}_{\mathrm{recon}} = \sum_{n=1}^{N} (\mathrm{MSE}(x_n, \mathcal{G}(\mathcal{D}(x_n))) + (1.0 - \mathrm{SSIM}(x_n, \mathcal{G}(\mathcal{D}(x_n))))) \tag{5}$$

4. EVALUATION RESULTS

4.1 Example of Segmentation Results

The processing results for different segment counts C are shown in Fig. 4. Increasing the number of segments enables a more detailed classification of fine structures. The number of segments, which is a user-defined parameter, can initially be set to a high value to capture detailed structures. Later, to reduce false positives, these segments can be merged during the sensitivity adjustment process.

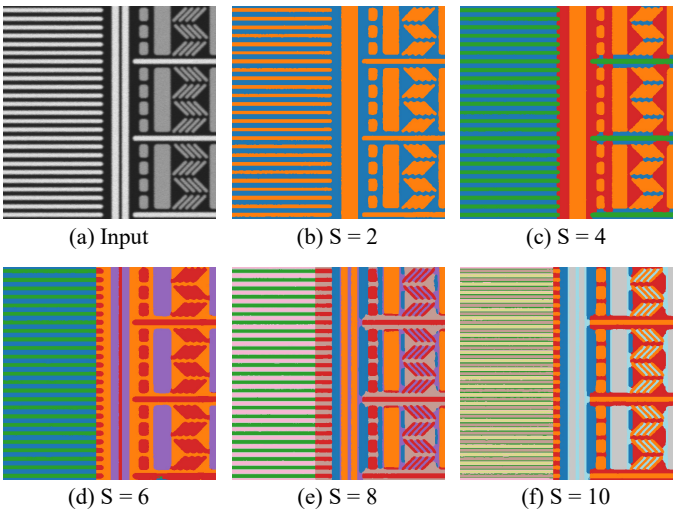

Figure 4. Processing results for different segment counts C.

4.2 False Positive Reduction

We evaluated the effectiveness of the proposed method using images of real devices. The conditions for training and evaluation are summarized in Tables 1 and 2.

Table 1. Training conditions.

Device type	No. of images	Image size [pixel]	No. of segs. C	Training epochs
Memory	214,720	600 × 600	20	20
Logic	30,030	600 × 600	20	20

Table 2. Evaluation conditions.

Device type	No. of images	No. of DOIs
Memory	53,680	5
Logic	3,604,370	40

Since all defect candidates appearing in segments without defects of interest (DOIs) are considered false positives, the detection sensitivity for such segments can be reduced. While various methods can be utilized for adjusting the detection sensitivity we chose to multiply the abnormality degree calculated for each defect candidate by a coefficient, α_s ($s \in \{1, ..., C\}$). Other methods of sensitivity adjustment include modifying the abnormality offset for each segment and tweaking the image processing parameters used in the defect candidate extraction process for each segment.

The segments of interest which may contain DOIs are identified from the segmentation results. For non-interest segments, the α_s value was set to 0.5, effectively halving the sensitivity.

The receiver operating characteristic (ROC) curve, which visualizes the performance evaluation of false positive identification, is shown in Fig. 5. The ROC curve plots the relationship between the false positive rate and the defect detection rate (recall) as the detection threshold is varied, with the false positive rate on the horizontal axis and the defect detection rate on the vertical axis. The closer the curve is to the top-left corner (false positive rate 0, detection rate 100%), the better the performance is considered to be.

By adjusting the sensitivity for each segment, the slope of the curve improved for both memory devices and logic devices. While ensuring no defects of interest were overlooked, false positives were reduced by 96.5% for memory devices and 56.6% for logic devices.

As stated above, the proposed method enables segmentation based on the type of circuit pattern without requiring user annotations or design data. We confirmed that false positives can be effectively reduced by adjusting the defect detection sensitivity for each segment.

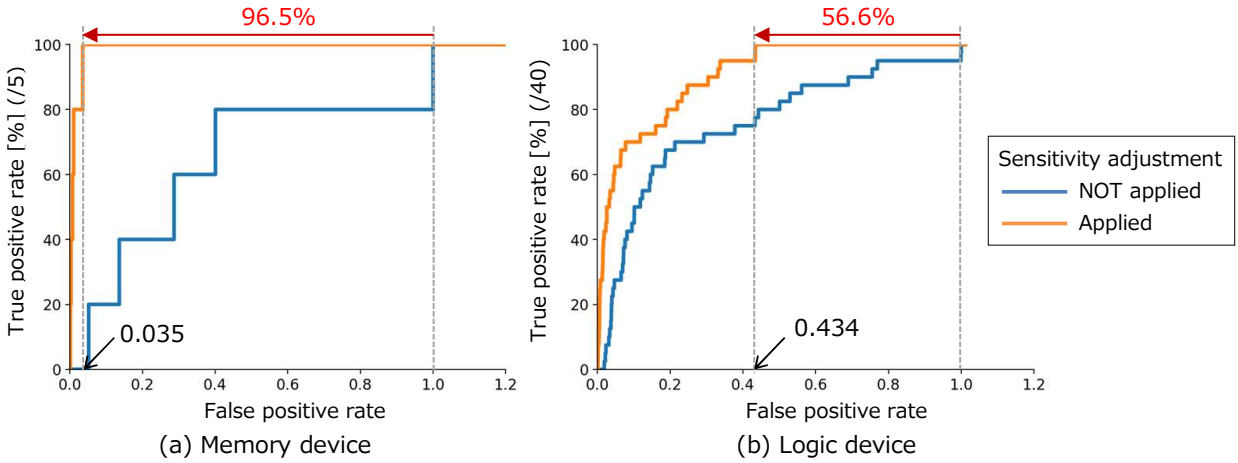

Figure 5. Results of performance evaluation for false positive identification using ROC curves.

5. CONCLUSION

We proposed a method to reduce false positives through pattern binning based on unsupervised learning. This method segments captured images into regions, such as memory cells, peripheral circuits, and intermediate areas, based on the appearance of circuit patterns. By tailoring the sensitivity for each region, false positives can be effectively reduced. In the evaluation, assuming no drop in DOI detection, false positives were reduced by 96.5% for a memory device and 56.6% for a logic device. These results demonstrate the effectiveness of the proposed method in segmenting circuit patterns and reducing false positives.

REFERENCES

[1] Guldi, R., "In-line defect reduction from a historical perspective and its implications for future integrated circuit manufacturing," *IEEE Transactions on Semiconductor Manufacturing* **17**(4), 629–640 (2004).

[2] Tolle, I. and Jain, A., "Innovative scalable design based care area methodology for defect monitoring in production," in [*2017 28th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)*], 144–148 (2017).

[3] Ji, X., Vedaldi, A., and Henriques, J., "Invariant information clustering for unsupervised image classification and segmentation," in [*2019 IEEE/CVF International Conference on Computer Vision (ICCV)*], 9864–9873 (2019).

[4] Yang, F., Sun, Q., Jin, H., and Zhou, Z., "Superpixel segmentation with fully convolutional networks," in [*2020 IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR)*], 13961–13970 (2020).

[5] Wang, Z., Bovik, A., Sheikh, H., and Simoncelli, E., "Image quality assessment: from error visibility to structural similarity," *IEEE Transactions on Image Processing* **13**(4), 600–612 (2004).