Nerissa A. Finnen

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EDUCATION

College Education

- Pasadena, CA
- California Institute of Technology (Caltech) 2022 -2026
- Bachelor of Science in Electrical Engineering: GPA 3.6/4.0
- Relevant Coursework: Analog Circuit Design, Analog Design Laboratory, High Frequency Systems Laboratory, Mixed-Mode Integrated Circuits, Advanced Digital Systems Design, Feedback and Control Circuits

TECHNICAL SKILLLS

Programming Languages: Python, Java, Assembly, C, MATLAB, Mathematica, VHDL

Design Software: Fusion 360, KiCad, Altium, LTSpice, CST, VHDL, MWO, AWR, Arduino, AVR Studio 4, Cadence Virtuoso

Electrical Equipment: Oscilloscope, power supplies, multimeters, spectrum analyzer, function generators, noise temperature measurement, vector network analyzer (VNA)

EXPERIENCE

Electrical Engineering Research Intern 2025-present

ETHZ (IDEAS Group): *Zurich, Switzerland*

- Conducting mathematical derivations of non-idealities for time-modulated array antennas
- Simulated lobe patterns using MATLAB and presented developments in research meetings

President of Caltech IEEE branch 2024-present

Caltech: *Pasadena, CA*

- Planned social, soldering, and informational events for Electrical Engineering community at Caltech
- Performed reimbursements for events and membership fees

Teaching Assistant 2023-present

Caltech: *Pasadena, CA*

- Taught students Diptrace for schematic, and PCB layout design and soldering skills
- Reviewed and troubleshooted 60 PCBs

Electrical Engineering Research Intern 2024-2024

Caltech High-Speed Integrated Circuits (CHIC): *Pasadena, CA*

- Designed PCBs with Altium and soldered to test components for a flexible RF board
- Developing a flexible, thin, lightweight thermal management system for flexible 2-D array PCBs with CST
- Presented oral presentation to a general audience of the research progress for the thermal management system

PROJECTS

8 GHz DLL 2025

- Designed in Cadence Maestro an 8 GHz delay locked loop in 45 nm CMOS with minimal RMS and peak to peak jitter, phase offset, duty cycle distortion and low power.
- Achieved locking with 150 MHz power supply and input noise at 720°, 810°, 900°, and degraded results at 990°

16-bit Serial Divider 2025

- Implemented a non-restoring division algorithm for 16-bit unsigned serial divider on a Xilinx chip with VHDL

4.35 GHz Speed Gun 2024

- Constructed 4.35 GHz speed measuring device with custom Wilkinson power dividers, low noise amplifiers, oscillator, and antennas and manufactured parts
- Microwave Office was used to simulate the designs of the custom parts, while hand calculations were performed to determine the necessary antenna dimensions
- The frequency data was converted to audio that was analyzed in python to calculate the speed of moving objects

Two-Waveform Function Generator 2024

- Designed a PCB for a two-waveform function generator that produced triangle, and square waves from 1 kilohertz to 100 kilohertz range, with amplitude, frequency, and DC offset control
- Utilized LTSpice for simulations to advise component selection and design decisions

Ball and Beam Control 2024

- Designed, and debugged PID controller to balance a ball on a beam with reference voltages and feedback control