Nerissa A. Finnen

nfinnenct@gmail.com (260)-446-1798

EDUCATION

College Education

- Pasadena, CA
- California Institute of Technology (Caltech) 2022 -2026
- Bachelor of Science in Electrical Engineering: GPA 3.6/4.0
- Relevant Coursework: Analog Circuit Design, Analog Design Laboratory, High Frequency Systems Laboratory, Mixed-Mode Integrated Circuits, Advanced Digital Systems Design, Feedback and Control Circuits

TECHNICAL SKILLLS

Programming Languages: Python, Java, Assembly, C, MATLAB, Mathematica, VHDL

Design Software: Fusion 360, KiCad, Altium, LTSpice, CST, VHDL, MWO, AWR, Arduino, AVR Studio 4, Cadence Virtuoso

Electrical Equipment: Oscilloscope, power supplies, multimeters, spectrum analyzer, function generators, noise temperature measurement, vector network analyzer (VNA)

EXPERIENCE

Electrical Engineering Research Intern 2025-present

ETHZ (IDEAS Group): *Zurich, Switzerland*

- Conducting mathematical derivations of non-idealities for time-modulated array antennas
- Simulated lobe patterns using MATLAB and presented developments in research meetings

President of Caltech IEEE branch 2024-present

Caltech: *Pasadena, CA*

- Planned social, soldering, and informational events for Electrical Engineering community at Caltech
- Performed reimbursements for events and membership fees

Teaching Assistant 2023-present

Caltech: *Pasadena, CA*

- Taught students Diptrace for schematic, and PCB layout design and soldering skills
- Reviewed and troubleshooted 60 PCBs

Electrical Engineering Research Intern 2024-2025

Caltech High-Speed Integrated Circuits (CHIC): *Pasadena, CA*

- Designed PCBs with Altium and soldered to test components for a flexible RF board
- Developing a flexible, thin, lightweight thermal management system for flexible 2-D array PCBs with CST
- Presented oral presentation to a general audience of the research progress for the thermal management system

PROJECTS

SH-2 CPU 2025

- Designed a RISC instruction set CPU with partner in VHDL including 4 blocks of 256 longwords RAM
- Implemented nearly all instructions and read/write RAM functionality
- Used two stage pipelining to execute multi-clock instructions

16-bit Serial Divider 2025

- Implemented a non-restoring division algorithm for 16-bit unsigned serial divider on a Xilinx chip with VHDL

AVR Instruction Assembler 2024

- Designed an assembler in Java to implement the AVR instruction set and select pseudo-op instructions
- Implemented labels, forward references, symbolic constants, and file inclusions

Ball and Beam Control 2024

- Designed, breadboarded, and debugged a PID controller to balance a metal ball on a metal beam using reference voltages and feedback control
- Characterized the behavior of the controller by measuring the time it took to balance the ball

HEXER Game 2023

- Designed an 8-bit Harvard Architecture accumulator-based CPU in ABEL
- Implemented the game HEXER with the designed CPU in AVR assembly

HOBBY PROJECTS

PCB Dorm Keychain 2025

- Currently designing a low-cost PCB LED keychain in KiCad for new student welcoming event