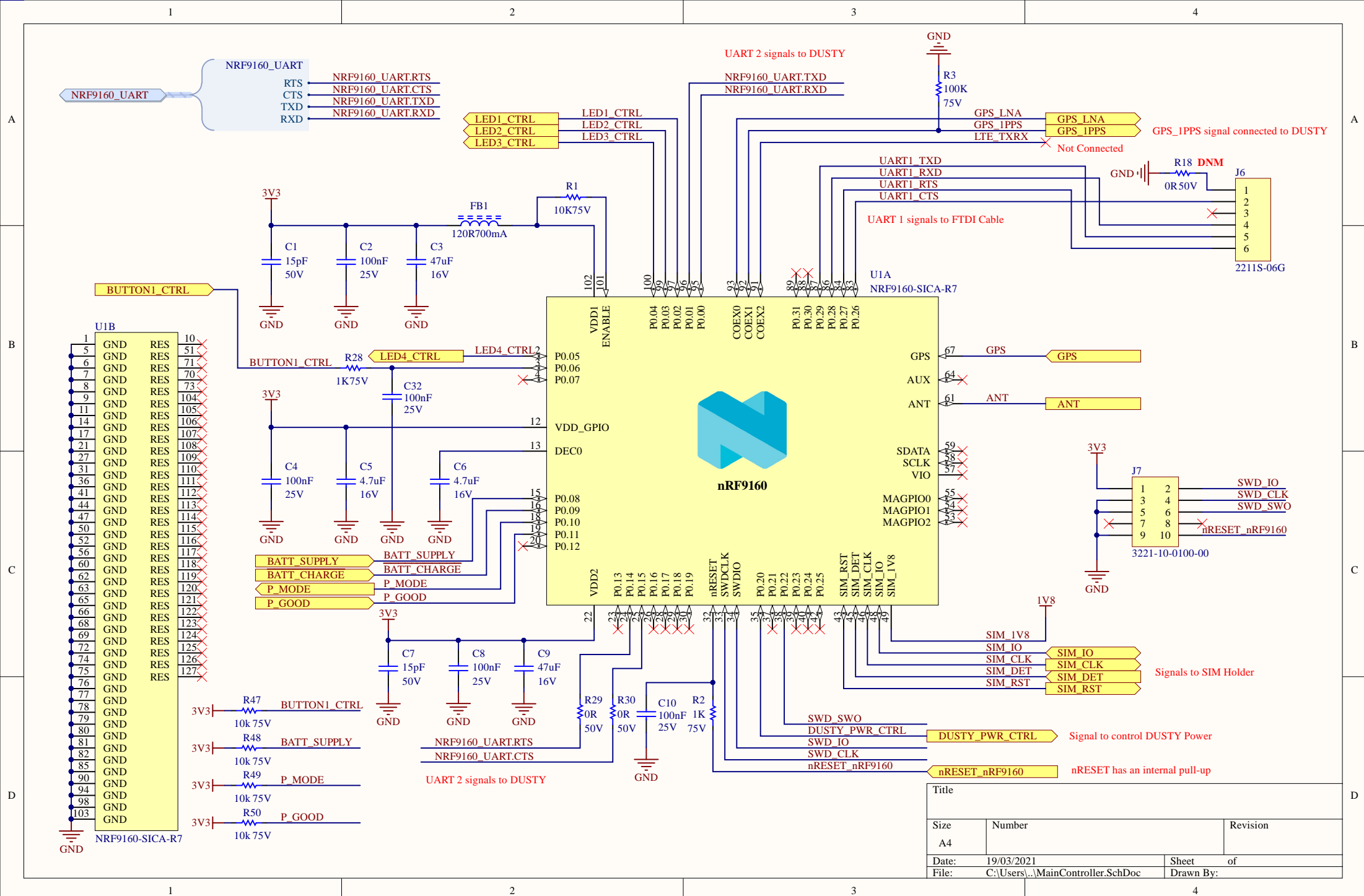
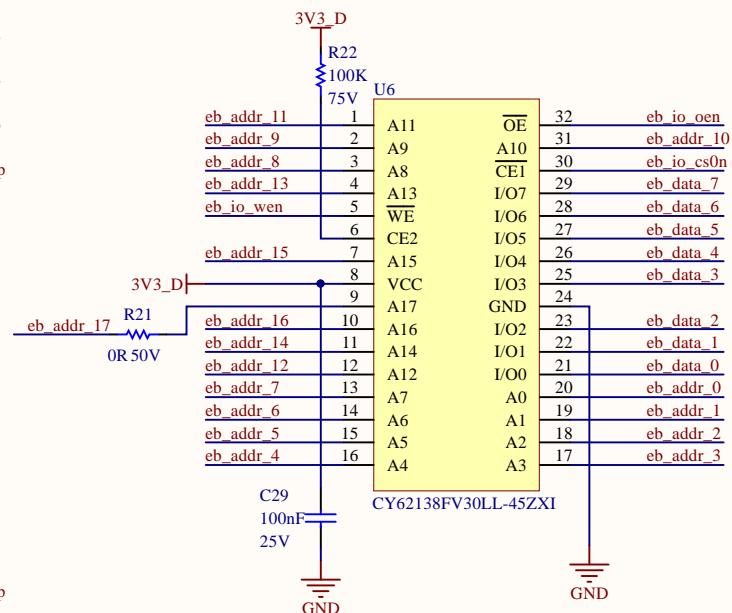
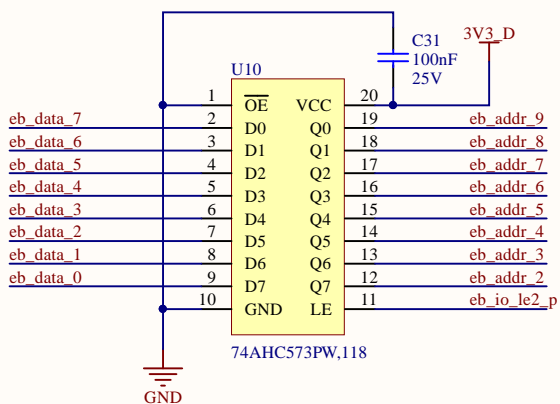
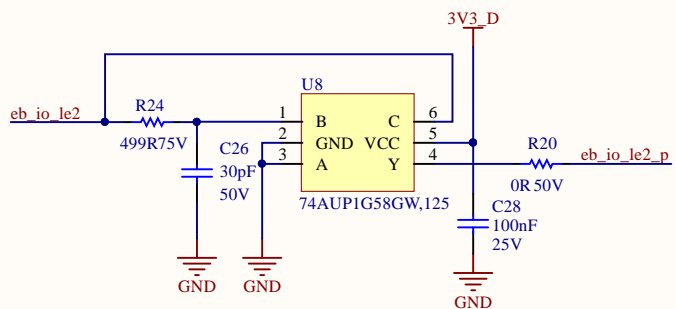
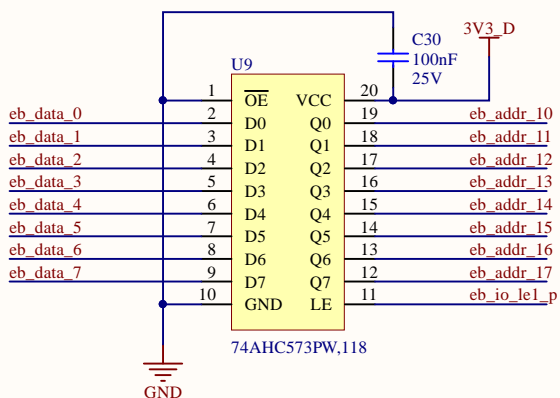
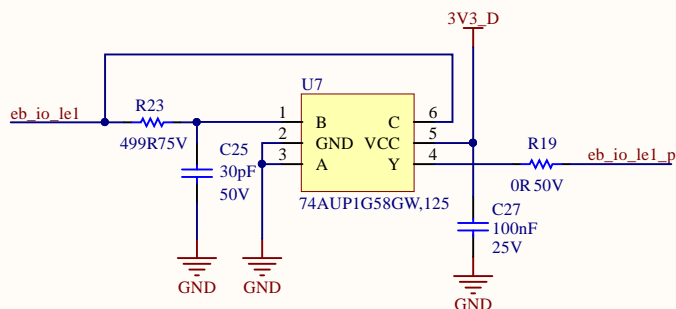
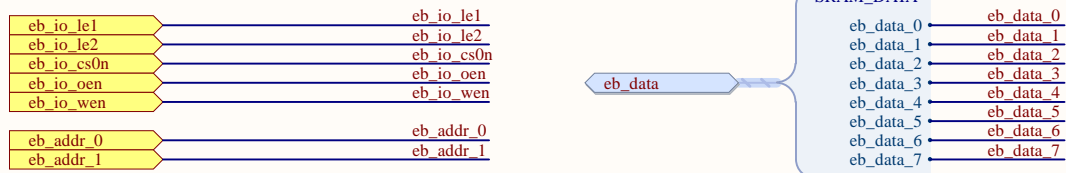


Title		
Size	Number	Revision
A4		
Date:	19/03/2021	Sheet of
File:	C:\Users\...Main.SchDoc	Drawn By:



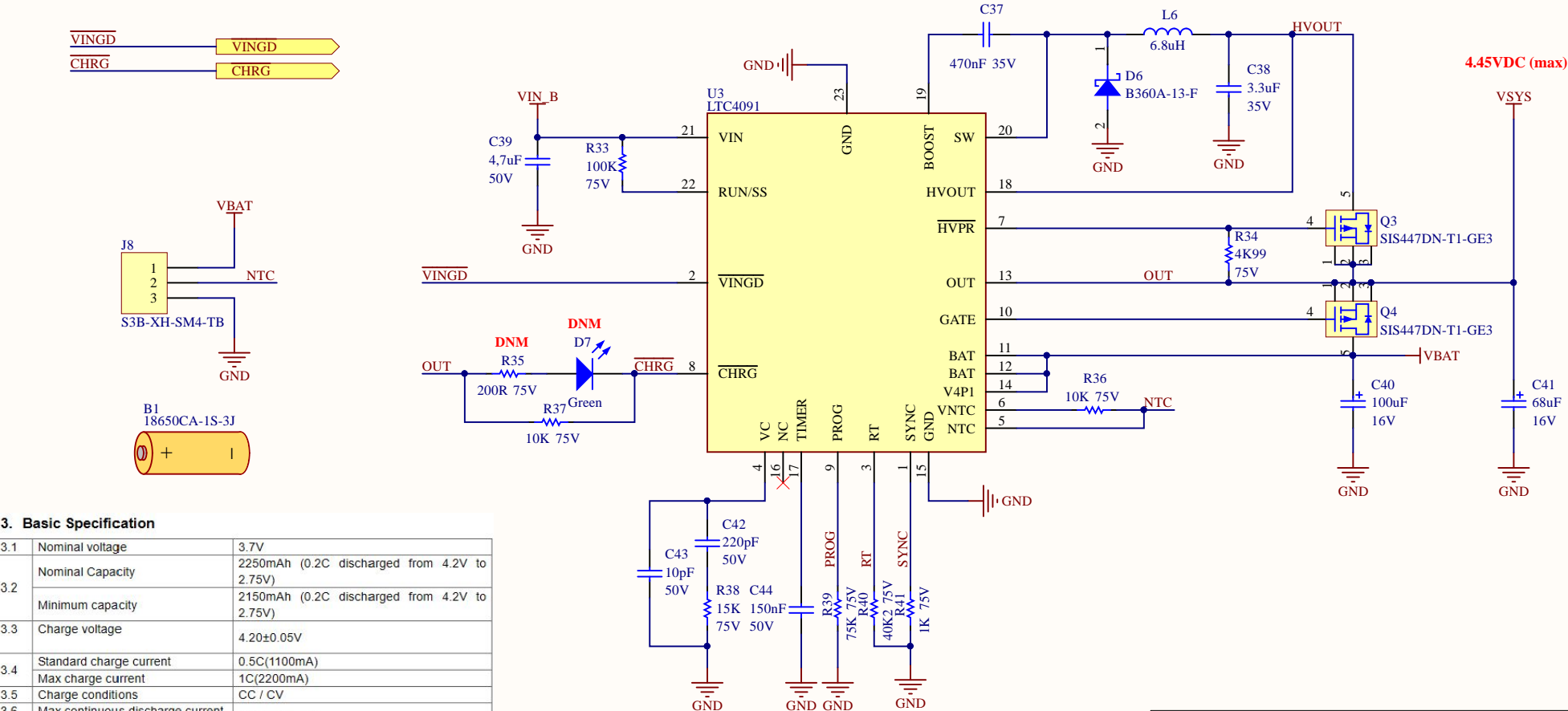
## INPUTS / OUTPUTS



Title			
Size A4	Number		Revision
Date:	19/03/2021	Sheet	of
File:	C:\Users\...\Memory.SchDoc	Drawn By:	

**VINGD (Pin 2):** The VINGD pin is the open collector output of an internal comparator. VINGD remains high impedance until sufficient voltage is present on VIN to enable the switching regulator and RUN/SS is high.

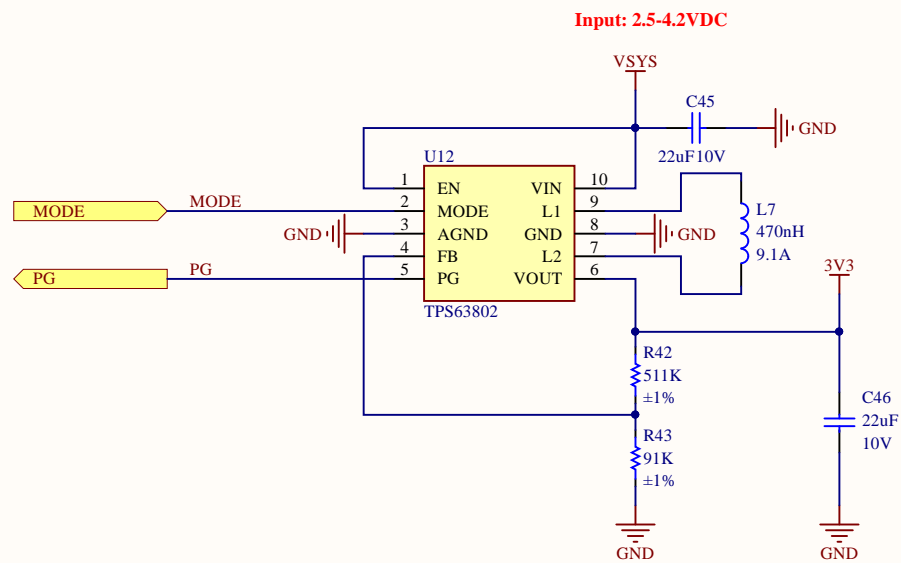
**CHRG (Pin 8):** Open-Drain Charge Status Output. When the battery is being charged, the CHRG pin is pulled low by an internal N-channel MOSFET. When the timer runs out or the charge current drops below 10% of the programmed charge current or the input supply is removed, the CHRG pin is forced to a high impedance state.



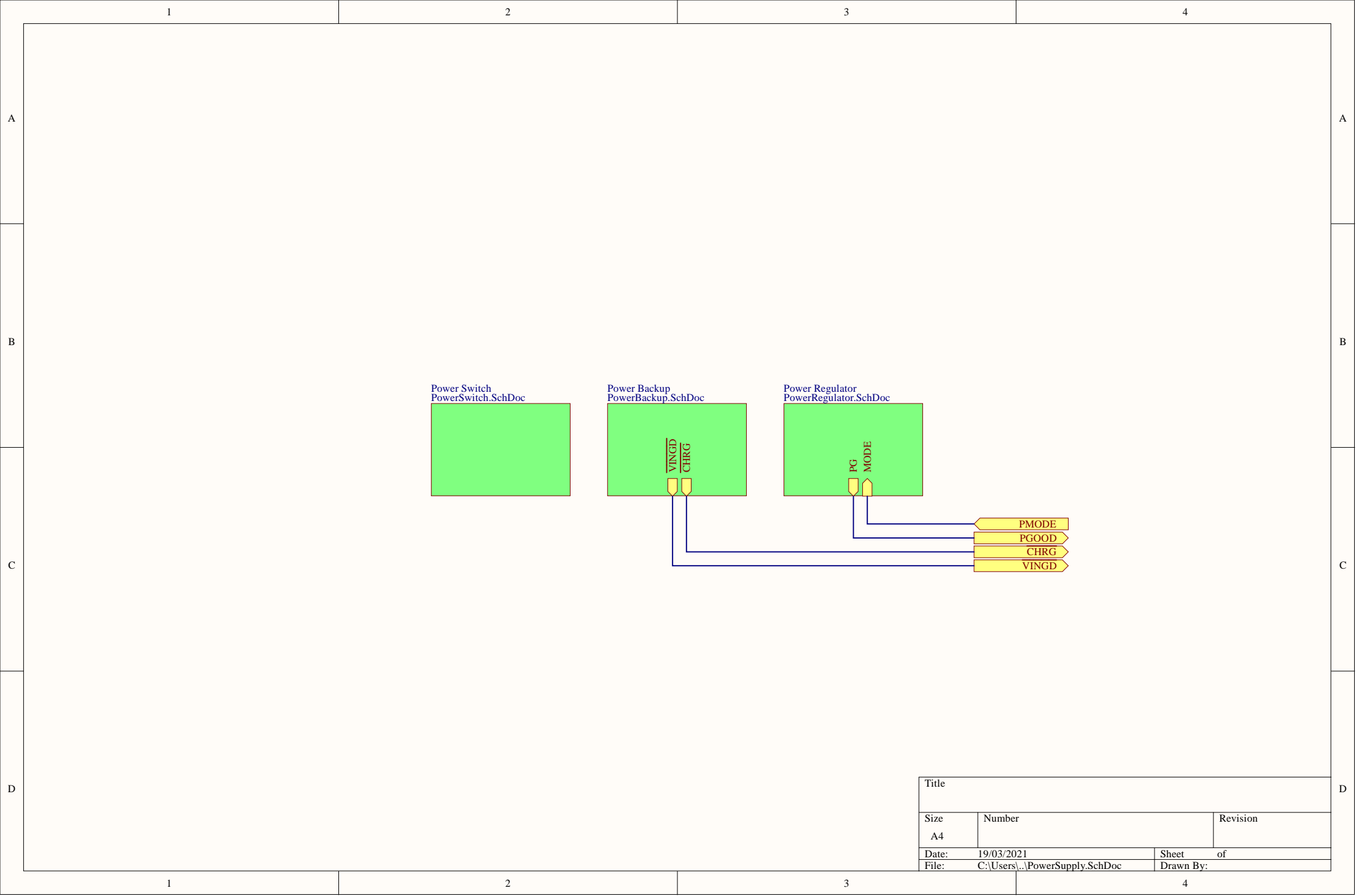
3. Basic Specification

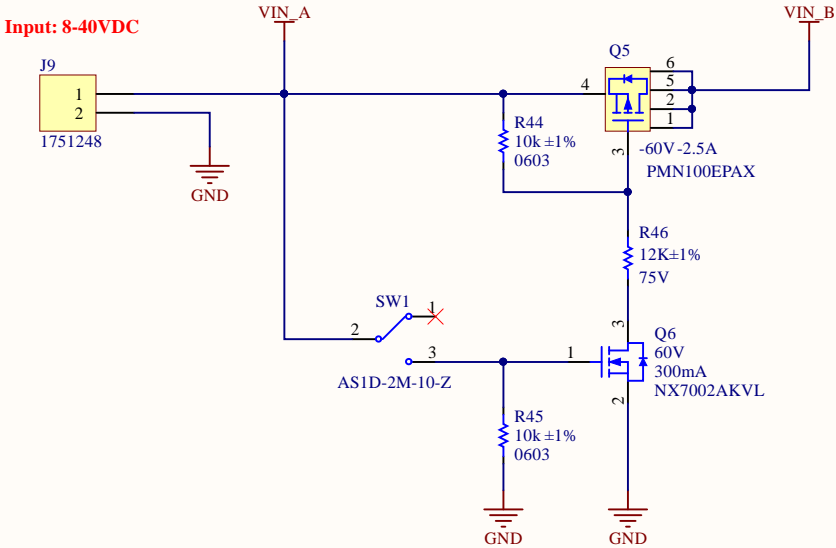
3.1	Nominal voltage	3.7V
3.2	Nominal Capacity	2250mAh (0.2C discharged from 4.2V to 2.75V)
	Minimum capacity	2150mAh (0.2C discharged from 4.2V to 2.75V)
3.3	Charge voltage	4.20±0.05V
3.4	Standard charge current	0.5C(1100mA)
	Max charge current	1C(2200mA)
3.5	Charge conditions	CC / CV
3.6	Max continuous discharge current	1C ( 2200mA )
3.7	Max peak discharge current	1C ( 2200mA)
3.8	Discharge cut-off voltage	2.3V±0.075V
3.9	Internal Impedance	≤180mohm (after charged)
3.10	Thermistor	10K NTC

Title		
Size	Number	Revision
A4		
Date:	19/03/2021	Sheet of
File:	C:\Users\PowerBackup.SchDoc	Drawn By:

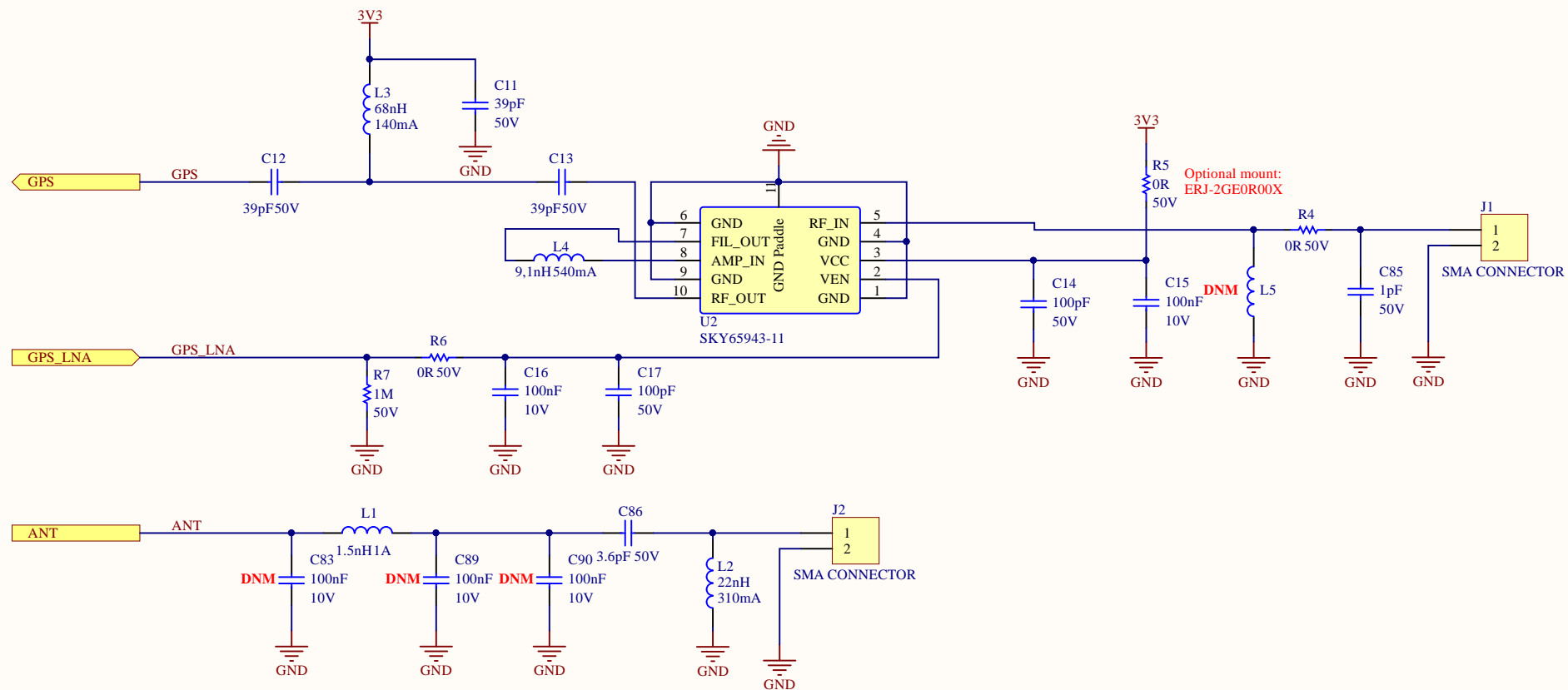


Title		
Size	Number	Revision
A4		
Date:	19/03/2021	Sheet of
File:	C:\Users\...PowerRegulator.SchDoc	Drawn By:





Title			
Size	Number		Revision
A4			
Date:	19/03/2021		Sheet of
File:	C:\Users\...\PowerSwitch.SchDoc		Drawn By:



Title		
Size	Number	Revision
A4		
Date:	19/03/2021	Sheet of
File:	C:\Users\...Radiofrequency.SchDoc	Drawn By:



A

A

B

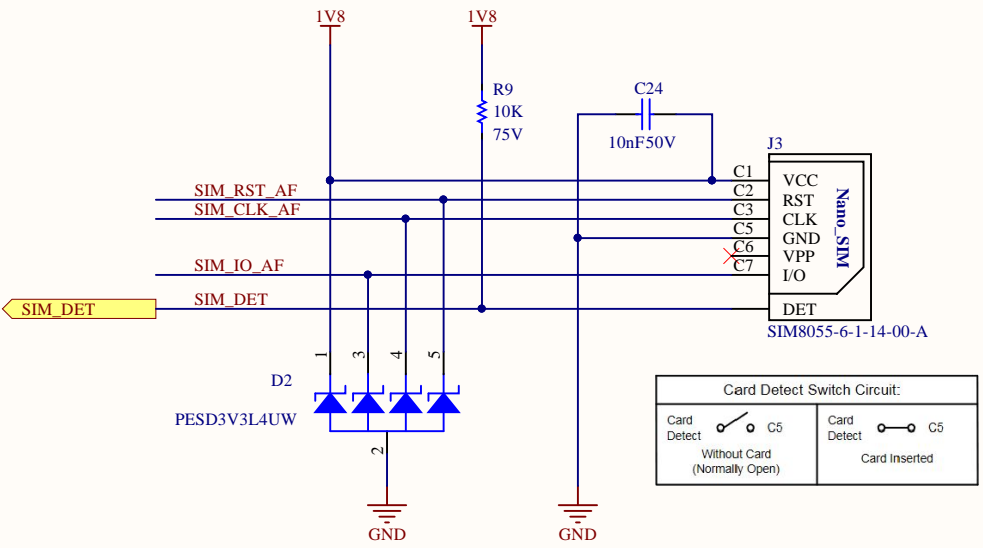
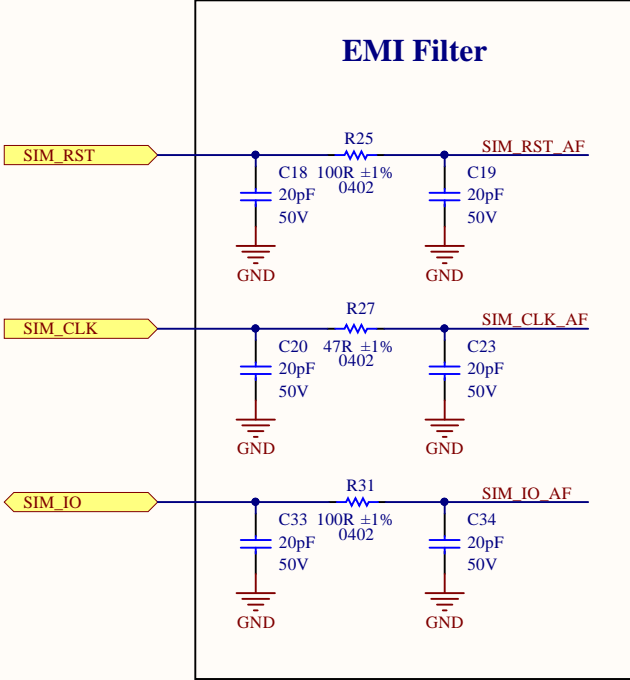
B

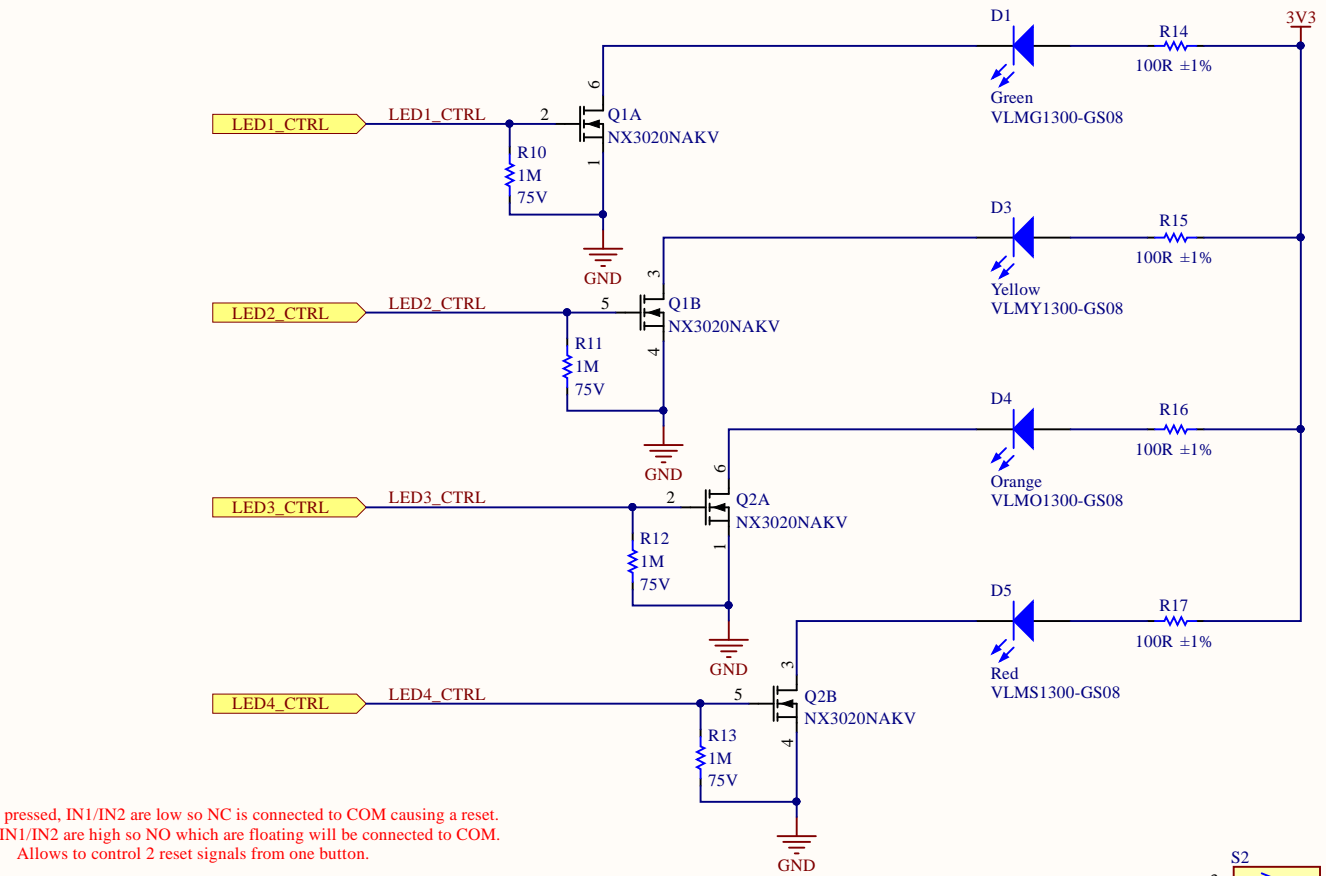
C

C

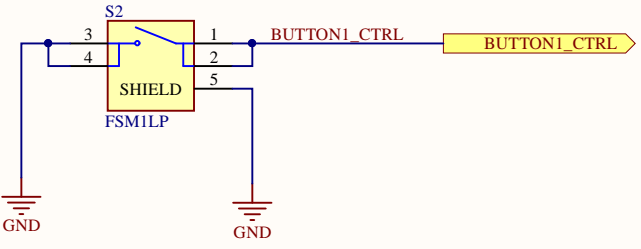
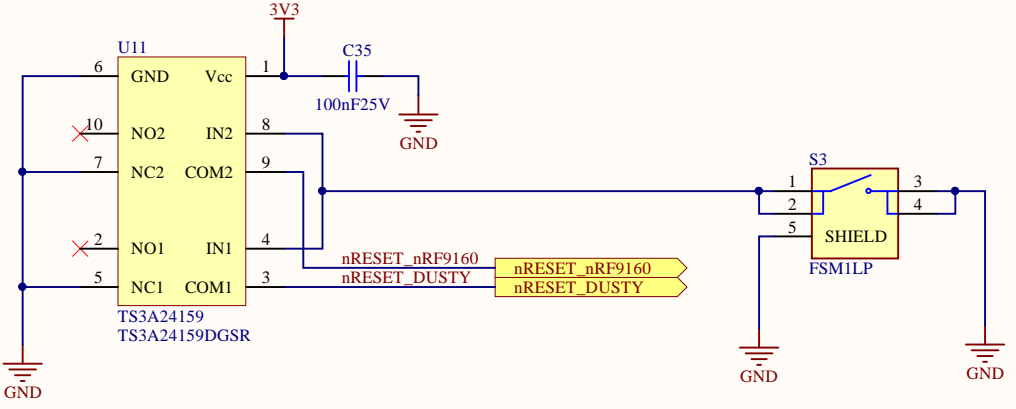
D

D

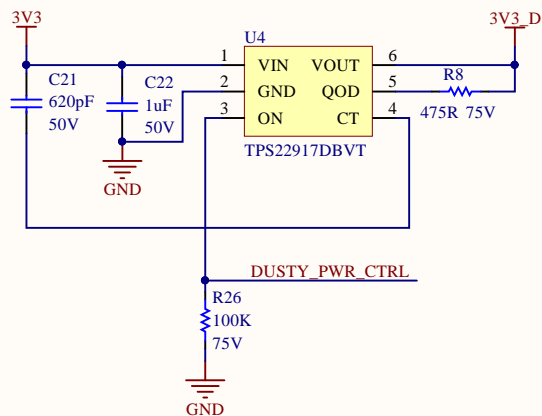




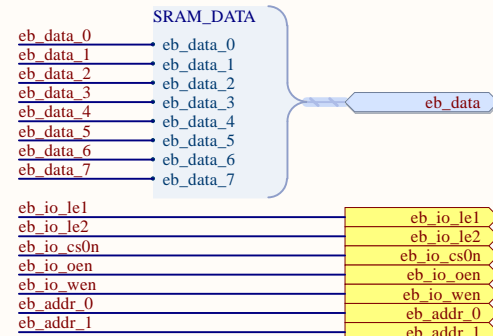
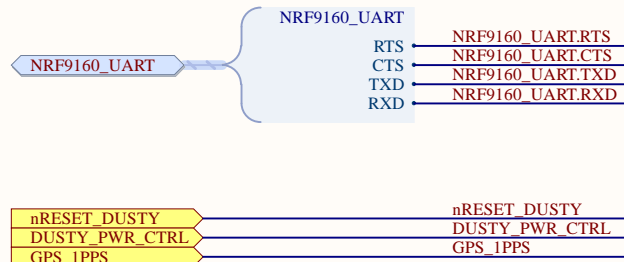
When SW3 is pressed, IN1/IN2 are low so NC is connected to COM causing a reset.  
By default IN1/IN2 are high so NO which are floating will be connected to COM.  
Allows to control 2 reset signals from one button.



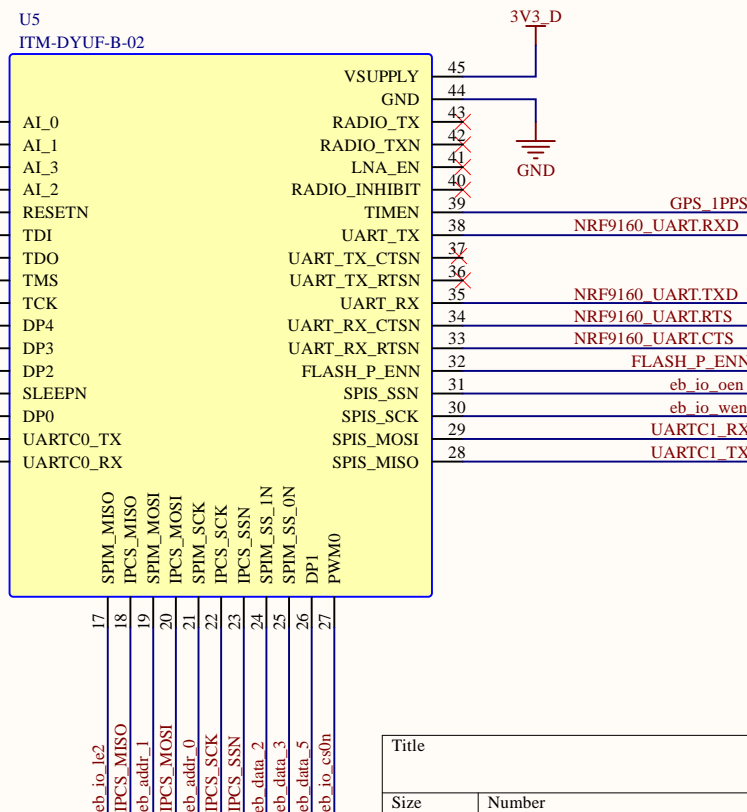
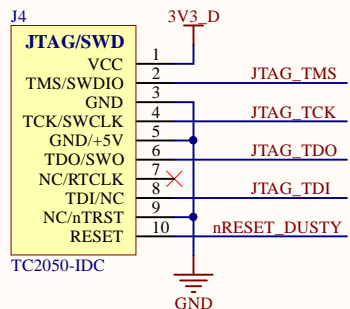
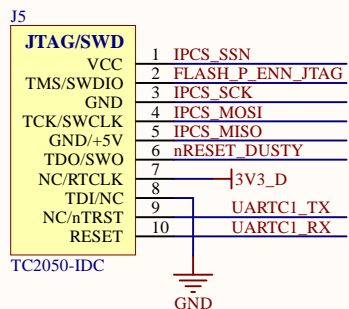
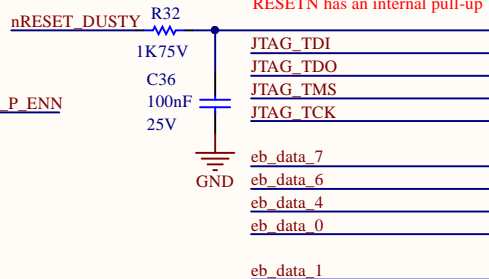
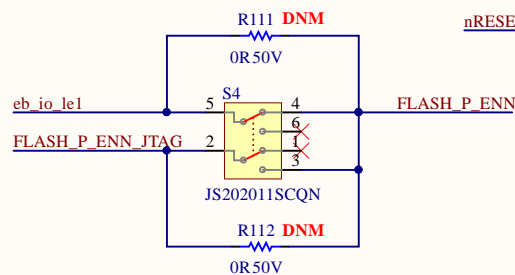
Title		
Size	Number	Revision
A4		
Date:	19/03/2021	Sheet of
File:	C:\Users\...\UserInterface.SchDoc	Drawn By:



## INPUTS / OUTPUTS



Mount SW4 for debugging, mount R111/R112 for deployment



Previously eb\_io\_le1

Review UARTC1 pinout for LTC5800

Title		
Size	Number	Revision
A4		
Date:	19/03/2021	Sheet of
File:	C:\Users\...\\WiFi.SchDoc	Drawn By: