iSWAP - Interposer SWAP

By

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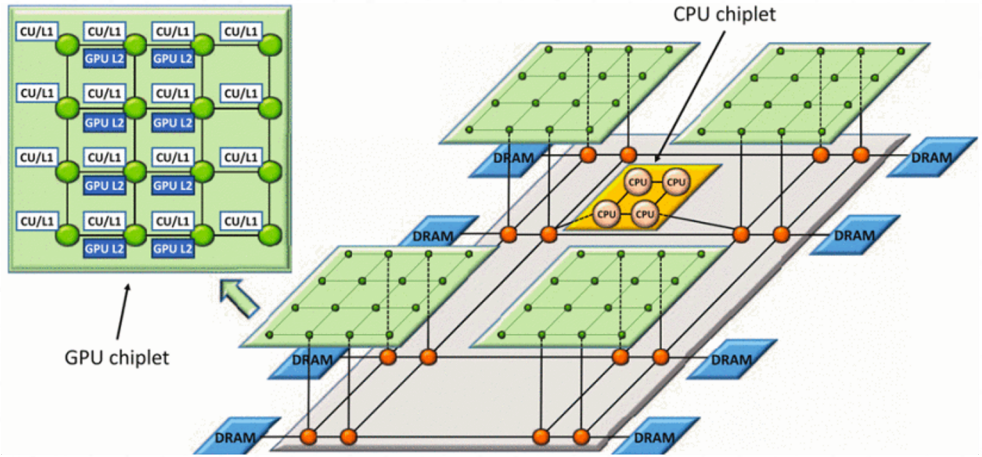

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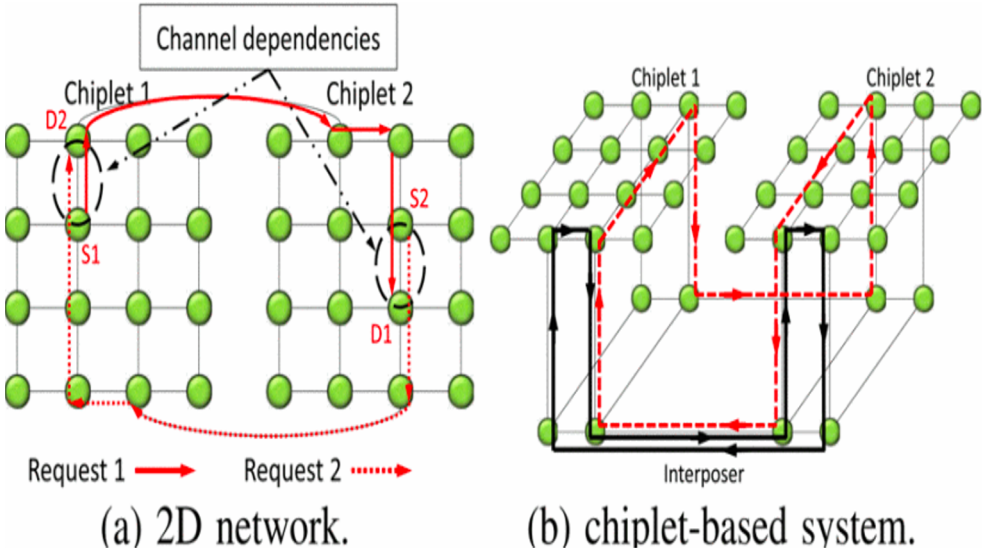
Problem Statement

- To avoid deadlocks in systems where-in deadlock free chiplets and deadlock free interposer are integrated.

- Prior approaches involves
  - Using global system-level knowledge of the SoC
  - High costs of required virtual channels.
  - Turn restrictions on local routing algorithms.



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Qualitative Comparison of Deadlock Freedom Mechanism - Modularity Centric

Design	Topology	VC	Flow Control
Dally/Turn Restriction [1]	✗	✓	✓
Duato/Escape VC[2]	✗	✗	✓
BFC Based[3]	✓	✓	✗
Deflection Based[4]	✓	✓	✗
Coordination-based[5]	✓	✓	✗
iSWAP	✓	✓	✓

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Qualitative Comparison of Modular Deadlock Freedom Mechanisms

Design	Full Path diversity	W/O Injection Control	Topology Agnostic	Router Micro Architecture Modularity
Composable Routing[5]	✗	✓	✗	✓
Remote Control[6]	✓	✗	✗	✓
UPP [7]	✓	✓	✓	✗
iSWAP	✓	✓	✓	✓

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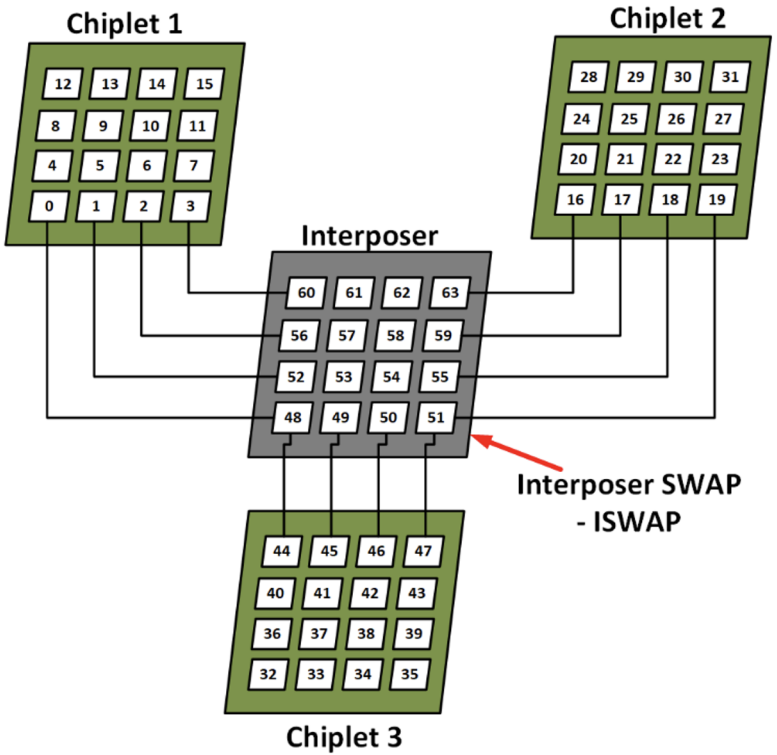
Proposed Solution - iSWAP

iSWAP

- Interposer will always have a portion of integration induced deadlock cycle.
- Using SWAP[8] only in interposer -> reducing area overhead and complexity overhead, gaining chiplet design modularity

Advantages:

- Deadlock freedom.
- Modularity support.
- Performance boost with better path diversity.



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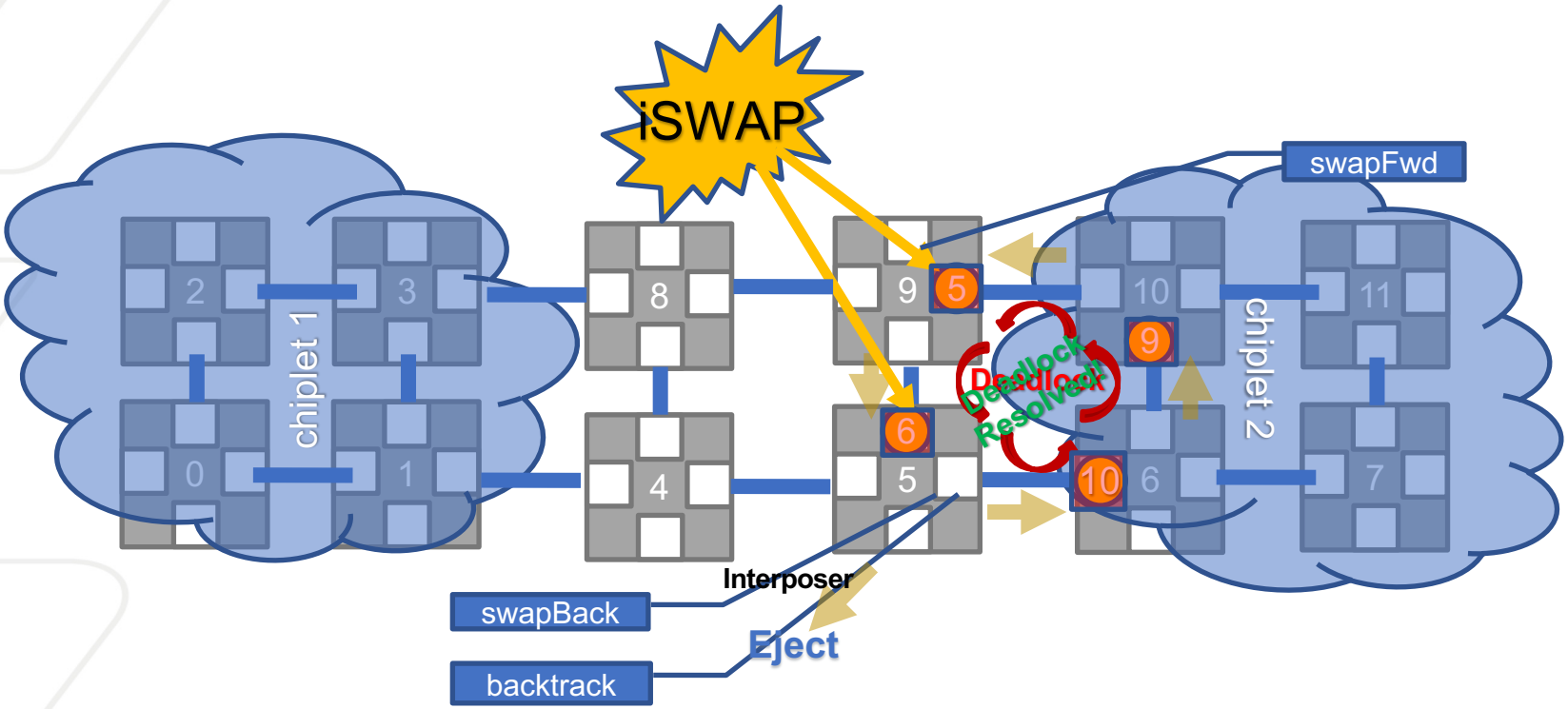
iSWAP in action



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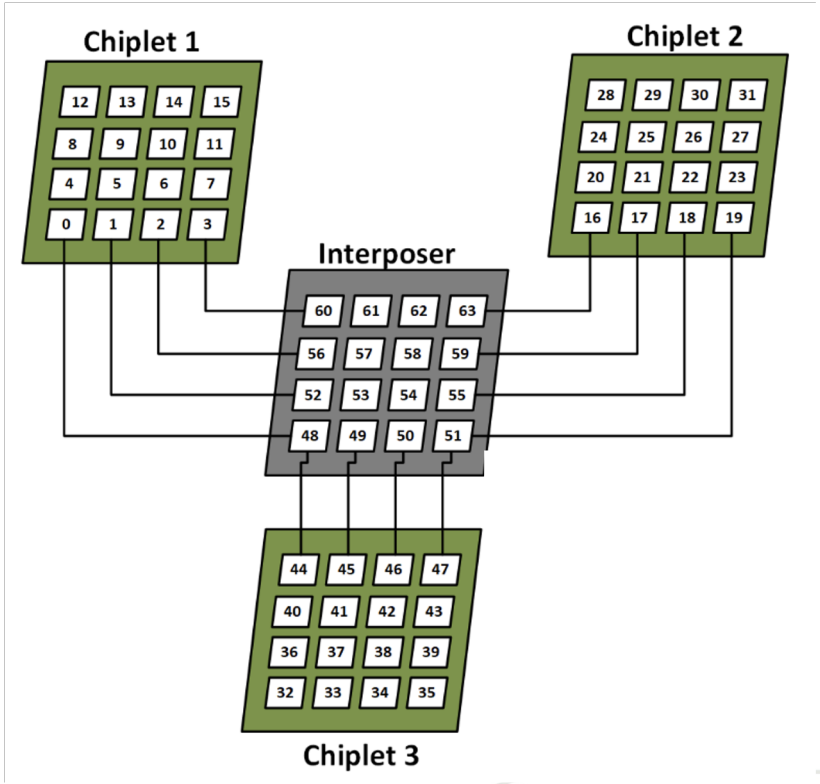
Implementation

Topology

- 2^n routers as per garnet2.0 requirement.
- Inherited mesh 8x8 topology.
- Modified the links to model the heterogeneity.
- By choosing the edge routers as boundary routers, we are avoiding the usage of higher radix routers



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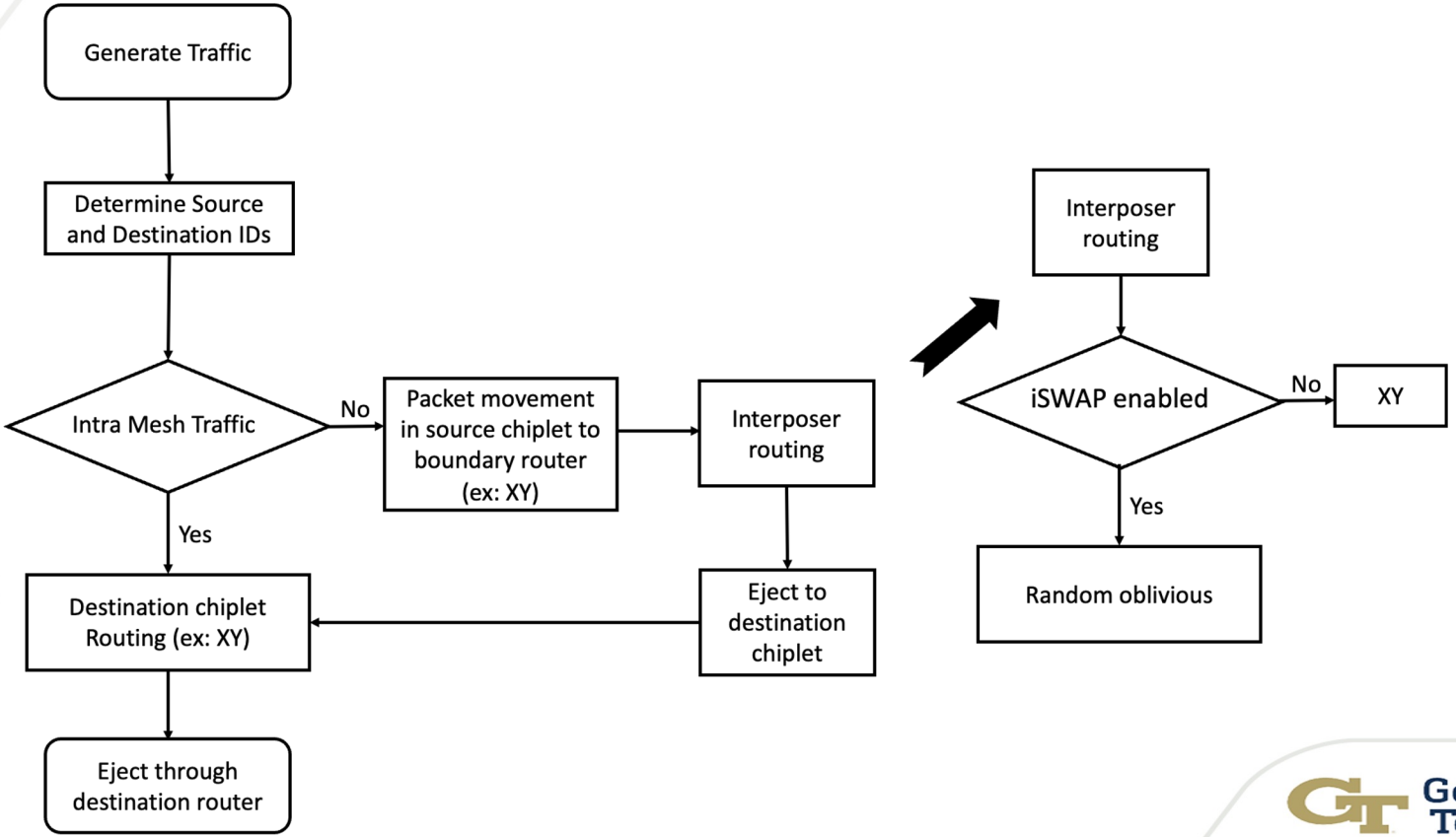
Routing



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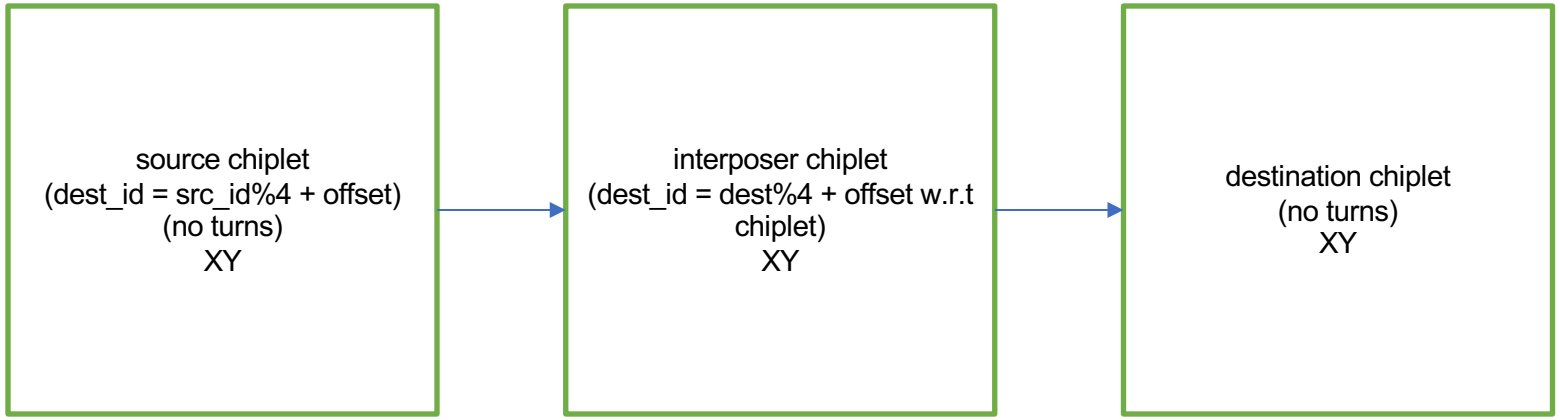
Composable - with Turn restrictions



For inter-mesh traffic

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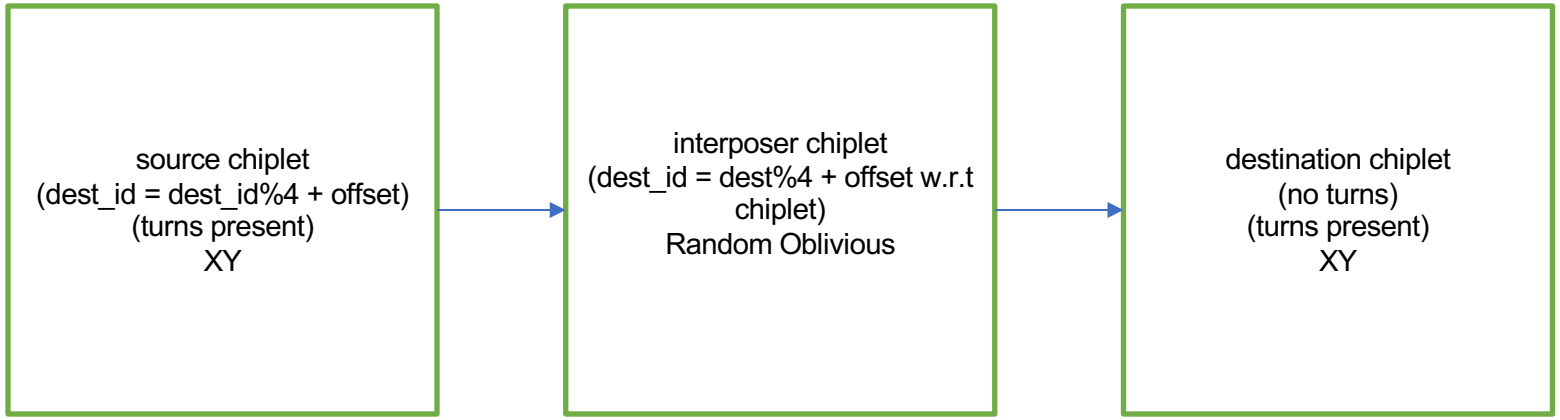
iSWAP routing

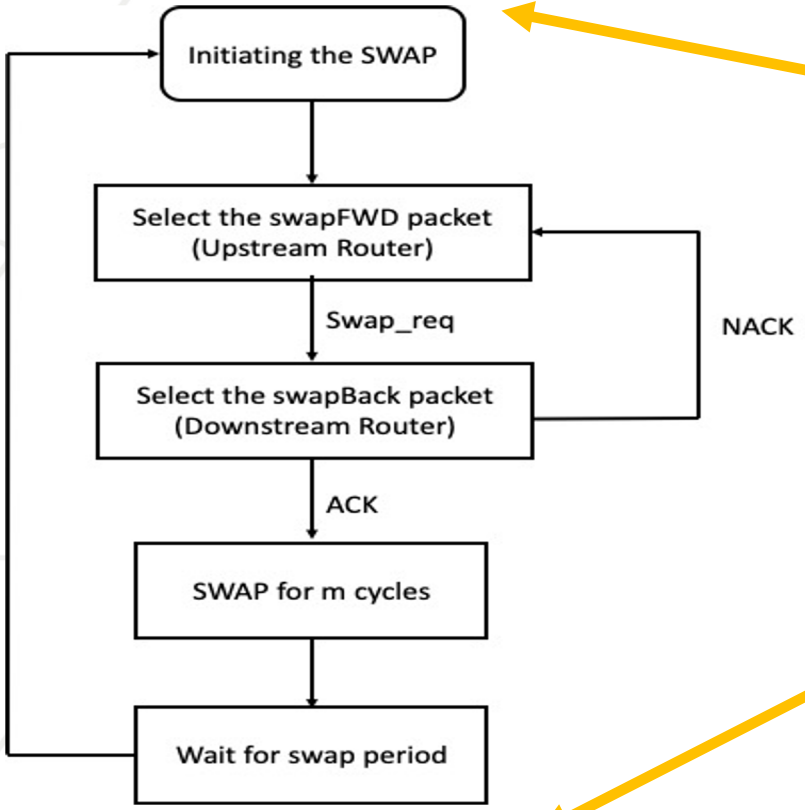


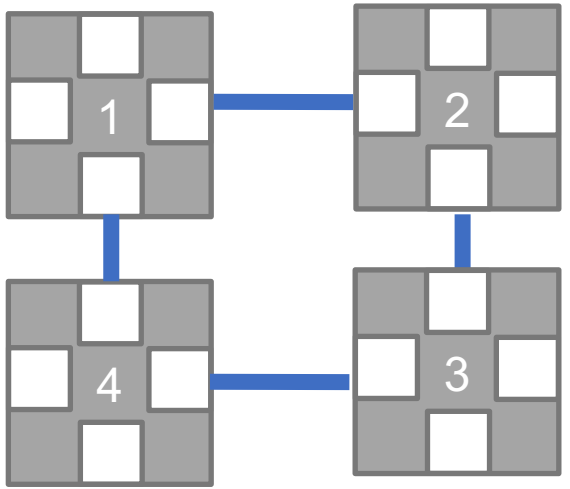
For inter-mesh traffic

SWAP: Main Ideas

- SWAP implies interchanging two packets from two adjacent routers
- Requires no additional buffers
- Leverages the *bidirectional* links to simultaneously send two packets
- Topology and Routing Algorithm agnostic
- If any VC at the downstream is empty, SWAP is not performed

iSWAP : Extension of SWAP





Interposer Routers

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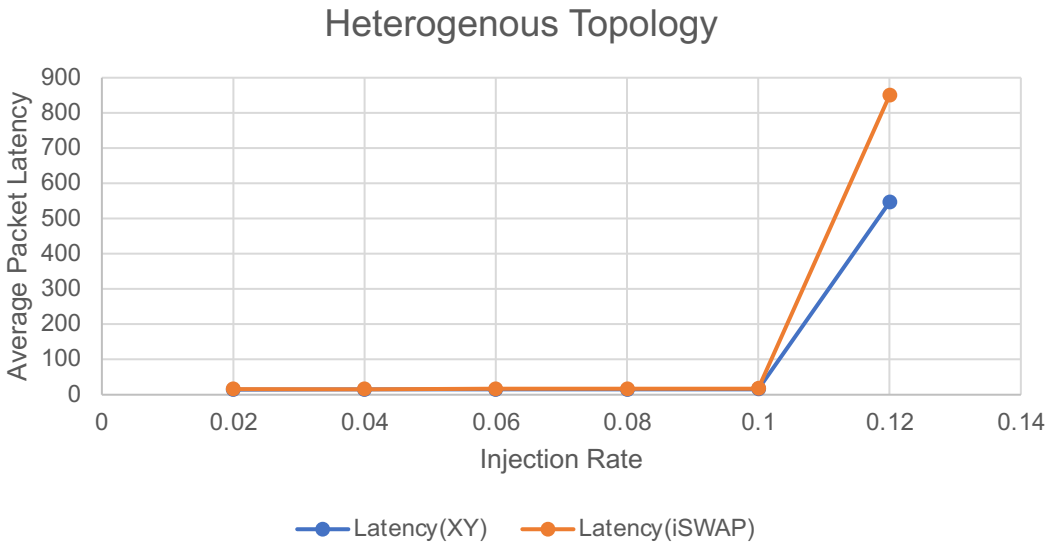
Evaluation

Network Configuration	
Topology	Heterogenous Mesh
VCs	4 VCs per Vnet
Link	128 bit
Flow Control	VCT
Packet Size	1 flit per packet
Synthetic Traffic	Uniform Random



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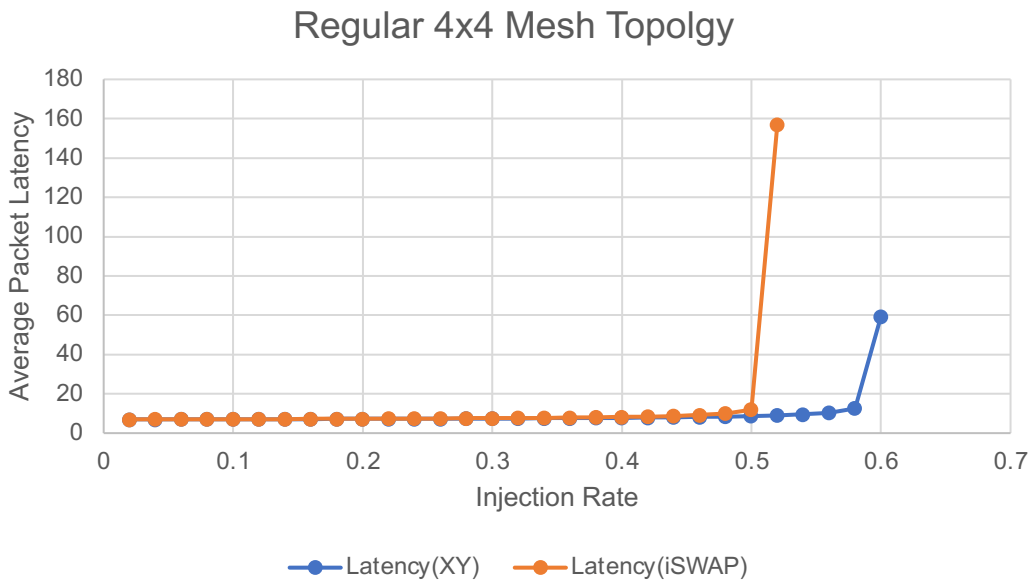
Continued …

Network Configuration	
Topology	4x4 Mesh
VCs	4 VCs per Vnet
Link	128 bit
Flow Control	VCT
Packet Size	1 flit per packet
Synthetic Traffic	Uniform Random



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Future work

- Improving performance with iSWAP
- Implementing the same in Garnet 3.0
- Using different routing and number of VCs in each of the chiplets
- Power estimation and comparison

Q & A

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References

[1]: Deadlock-free message routing in multiprocessor interconnection networks [IEEE Trans. Computer, 1987]

[2]: A new theory of deadlock-free adaptive routing in wormhole networks. [IEEE Trans. On Parallel and Dist. Sys, 1993]

[3]: Bubble Flow Control [IPDPS 2011]

[4]: BLESS [ISCA'09] CHIPPER [HPCA'11]

[5]: DISHA [IPDPS'95] Static Bubble [HPCA'17] SPIN [ISCA'18]

[6]: Modular routing design for chiplet-based systems," in *2018 ACM/IEEE 45th Annual International Symposium on Computer Architecture (ISCA)*, 2018

[7]: Remote control: A simple deadlock avoidance scheme for modular systems-on-chip," *IEEE Transactions on Computers*

[8]: SWAP: Synchronized Weaving of Adjacent Packets for Network Deadlock Resolution

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