

# UniversalPps Analyzer

## Reference Manual

Product Info	
Product Manager	Sven Meier
Author(s)	Sven Meier
Reviewer(s)	-
Version	1.1
Date	15.02.2019

## Copyright Notice

Copyright © 2018 NetTimeLogic GmbH, Switzerland. All rights reserved.

Unauthorized duplication of this document, in whole or in part, by any means, is prohibited without the prior written permission of NetTimeLogic GmbH, Switzerland.

All referenced registered marks and trademarks are the property of their respective owners

## Disclaimer

The information available to you in this document/code may contain errors and is subject to periods of interruption. While NetTimeLogic GmbH does its best to maintain the information it offers in the document/code, it cannot be held responsible for any errors, defects, lost profits, or other consequential damages arising from the use of this document/code.

NETTIMELOGIC GMBH PROVIDES THE INFORMATION, SERVICES AND PRODUCTS AVAILABLE IN THIS DOCUMENT/CODE "AS IS," WITH NO WARRANTIES WHATSOEVER. ALL EXPRESS WARRANTIES AND ALL IMPLIED WARRANTIES, INCLUDING WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF PROPRIETARY RIGHTS ARE HEREBY DISCLAIMED TO THE FULLEST EXTENT PERMITTED BY LAW. IN NO EVENT SHALL NETTIMELOGIC GMBH BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, CONSEQUENTIAL, SPECIAL AND EXEMPLARY DAMAGES, OR ANY DAMAGES WHATSOEVER, ARISING FROM THE USE OR PERFORMANCE OF THIS DOCUMENT/CODE OR FROM ANY INFORMATION, SERVICES OR PRODUCTS PROVIDED THROUGH THIS DOCUMENT/CODE, EVEN IF NETTIMELOGIC GMBH HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

IF YOU ARE DISSATISFIED WITH THIS DOCUMENT/CODE, OR ANY PORTION THEREOF, YOUR EXCLUSIVE REMEDY SHALL BE TO CEASE USING THE DOCUMENT/CODE.

## Overview

NetTimeLogic's PPS Analyzer is specifically designed for (PTP) Plugfests where multiple devices are synchronizing each other, and the accuracy of the individual devices shall be measured via PPS (offset from reference PPS). The device has 8 PPS inputs that are measured simultaneously, and it synchronizes itself to an additional reference PPS input. Additionally, it has a PPS output of the synchronized clock which is used for PPS measurement. Multiple PPS Analyzers can be connected to the same host and are all discovered automatically. It uses a serial interface (mostly over USB) to access the registers in the FPGA. In the FPGA it uses NetTimeLogic's configuration IP which represents an AXI Master to the other IP cores. It uses a proprietary protocol to convert the serial data stream from/to AXI register access. The core part consists of the following NetTimeLogic IP cores: PPS Slave IP core, PPS Master IP core, Adjustable Counter Clock IP core and multiple instances of the Signal Timestamp IP core. The tool needs no configuration and self-discovers all cores available in the design. It allows to access all registers in the design (also third party) which are connected to the AXI bus.

The PPS analyzer is implemented on an Arty Development Board from Digilent © with a specific shield which contains a serial termination of 20 Ohm and 3.3V buffers which allow PPS inputs of up to 15V.

## Key Features:

- 8 PPS Inputs
- 1 Reference PPS Input
- 1 PPS Output
- Synchronized Clock via PPS
- Timestamp resolution 10ns
- PPS compensated for synchronization error introduced by the reference PPS
- Delay compensation of input buffers and cable lengths (global)
- Cable Compensation individually on each PPS input
- Save Screen as PNG, JPG or TIFF
- Log values as CSV

## Revision History

This table shows the revision history of this document.

Version	Date	Revision
0.1	16.04.2018	First draft
1.0	21.06.2018	Added logging
1.1	15.02.2019	Added delay screen

Table 1: Revision History

---

# Content

<b>1</b>	<b>INTRODUCTION</b>	<b>7</b>
1.1	Context Overview	7
1.2	Function	7
<b>2</b>	<b>PPS ANALYZER</b>	<b>9</b>
2.1	Hardware	9
2.1.1	Pinout	10
2.2	Software	11
2.3	Run	13
2.4	Download	13

## Definitions

Definitions	
PPS Slave Clock	A clock that can synchronize itself to a PPS input
PPS Master Clock	A clock that generates a PPS to synchronize other nodes via a PPS output
Signal Timestamp	A core which takes timestamps on a edge of a signal and can compensate delays
Offset	Phase difference between clocks
Drift	Frequency difference between clocks

Table 2: Definitions

## Abbreviations

Abbreviations	
AXI	AMBA4 Specification (Stream and Memory Mapped)
CSV	Character separated value
PPS	Pulse Per Second
PS	PPS Slave
PM	PPS Master
TS	Timestamp
FPGA	Field Programmable Gate Array
VHDL	Hardware description Language for FPGA's

Table 3: Abbreviations

# 1 Introduction

## 1.1 Context Overview

The PPS Analyzer is designed to compare PPS references from multiple sources simultaneously and check their accuracy against a reference PPS. It synchronizes itself to the reference PPS input and generates a reference PPS from this synchronized clock. The PPS is compensated for the input and output delays introduced by the 3.3V buffers. The 3.3V buffers are optional but it has to be taken care of, that the PPS input and output pins are directly connected to the FPGA input via a 200 Ohm serial resistor. Also the design compensates the delay of the 3.3V buffer which means that if the buffers are not inserted the reference clock has an offset of the 3.3V buffers (25ns). This however has no influence on the accuracy measurement since the delay applies to all Inputs including the reference PPS. Only the output PPS is then shifted by the sum of output and input delay (50ns). All PPS cables shall be of the same length, and can be compensated for in 5ns steps.

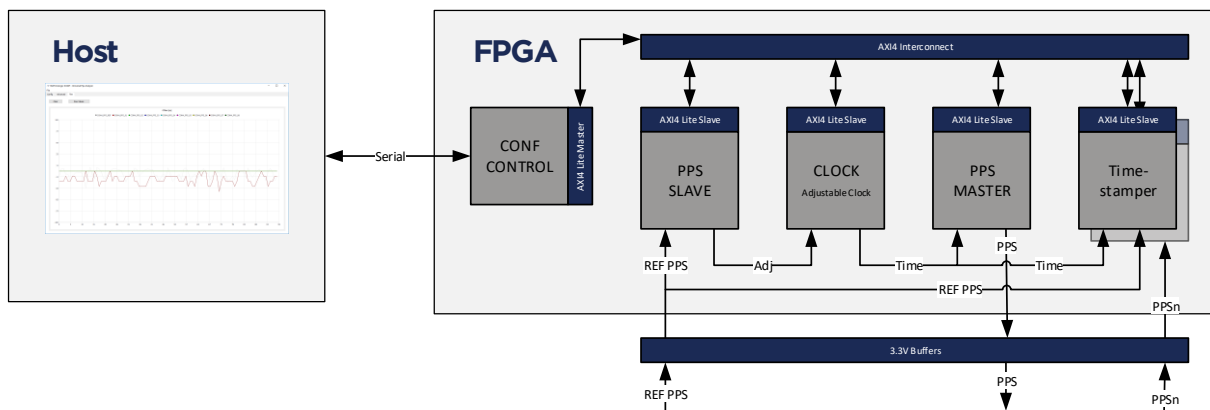


Figure 1: Context Block Diagram

## 1.2 Function

The PPS Analyzer synchronizes itself to the reference PPS via the NetTimeLogic PPS Slave IP core and generates a reference PPS based on the synchronized clock via the NetTimeLogic PPS Master IP Core. The 8 PPS inputs are timestamped via the NetTimeLogic Signal Timestamper IP core on the rising edge of the PPS input. The timestamps are then passed to the application where the difference to the next or last second overflow of the reference clock which is synchronized to the

reference PPS is calculated. The current error of the reference PPS is also measured via an additional Timestamper and can be used to compensate the error introduced by the synchronization in the application.



## 2 PPS Analyzer

### 2.1 Hardware

The PPS Analyzer hardware is built out of two components:

- The FPGA Module
- A custom Arduino Shied which contains the 3.3V buffers (M74HC4050B1R) and the 20 Ohm serial resistors as well as some Schottky diodes (5V) to protect the FPGA and buffers from to high input voltages and the BNC connectors. (optional)

The Arty board is an FPGA board from Digilent Inc. with an Artix7 FPGA from Xilinx. (<http://store.digilentinc.com/artix-7-fpga-development-board-for-makers-and-hobbyists/>)

The PPS Analyzer is designed for 3.3V PPS inputs but allows also higher PPS inputs up to 15V if the 3.3V buffers (M74HC4050B1R) are used. If no buffers are used make sure that your inputs are providing 3.3V voltage levels.

Since the shield contains no logic except of ensuring correct voltage levels and protecting the FPGA IO pins it can be easily built yourself, the only requirement is that the pins are connected to the correct IOs (See 2.1.1 for details)

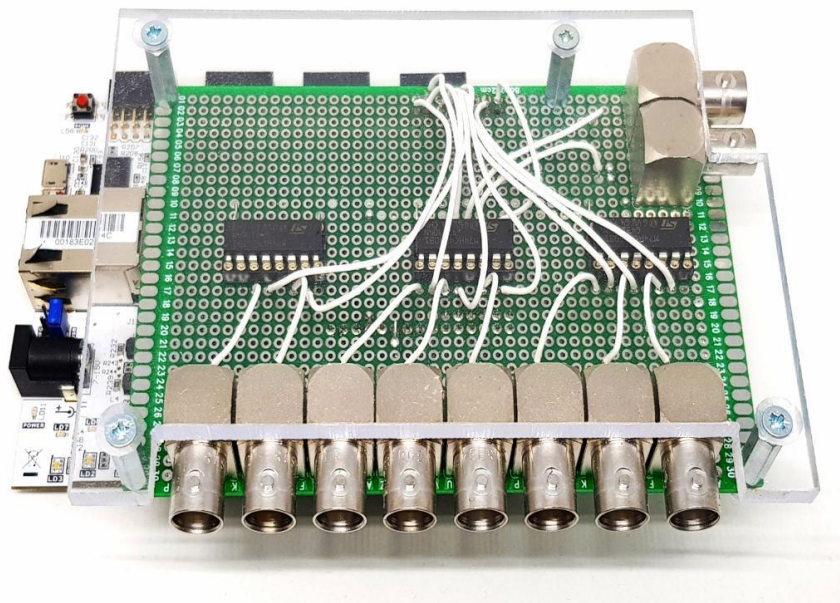


Figure 2: PPS Analyzer Hardware

## 2.1.1 Pinout

The signals are connected to the following pins on the Arty board, naming is according to printing on the board.

Signal Name	Arty Pin	FPGA Pin	Description
REF_PSS_IN	IO26	U11	Reference PPS input
PPS1	IO27	V16	Measure PPS input 1
PPS2	IO28	M13	Measure PPS input 2
PPS3	IO29	R10	Measure PPS input 3
PPS4	IO30	R11	Measure PPS input 4
PPS5	IO31	R13	Measure PPS input 5
PPS6	IO32	R15	Measure PPS input 6
PPS7	IO33	P15	Measure PPS input 7
PPS8	IO3	T11	Measure PPS input 8
REF_PPS_OUT	IO6	T15	(Reference) PPS output

Table 4: Pinout

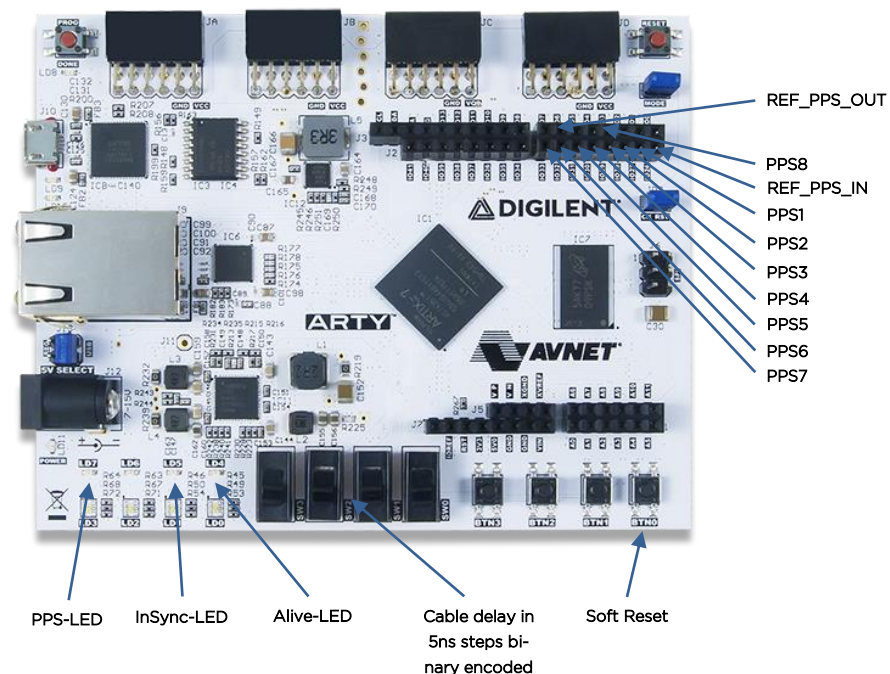


Figure 3: Arty (source Digilent Inc)

## 2.2 Software

The PPS Analyzer software is a simple Qt application, discovering and connecting to all available PPS Analyzer hardware (via USB/UART) connected and starting to show the PPS measurements.

The measurement screen (only current) can be saved, cleared and it can be chosen to use compensated or raw values. In general, the compensated values should be used since this removes much of the synchronization error introduced by the reference PPS.

In addition to saving the screen the measurement values can be logged as CSV file (separator “;”). Once the logging is started all new values are logged to a file until logging is stopped or the application closed. Every time a log is started a new file with the date is created (can be changed).

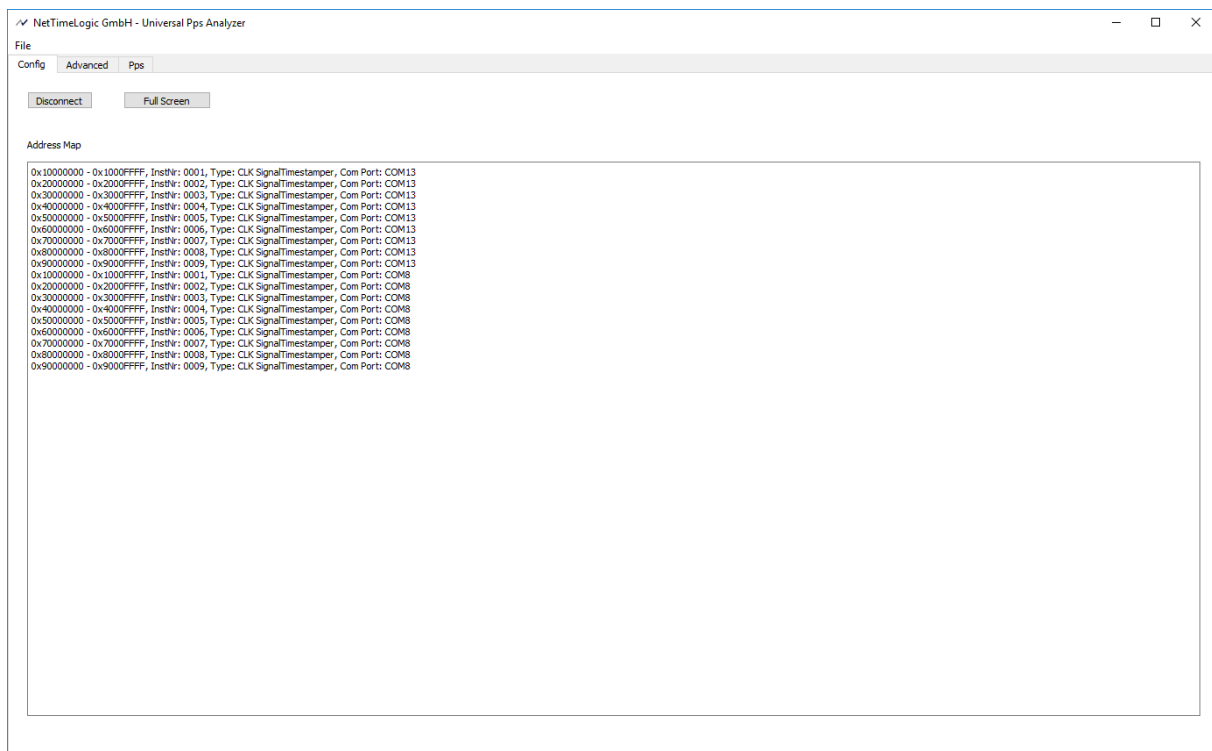


Figure 4: PPS Analyzer Software Connected



Figure 5: PPS Analyzer Software PPS

Also, the delays of the individual PPS can be configured to compensate. The delay can be to compensate different delays on input buffers or different delays due to different cable lengths from the source to the PPS inputs. The configured delay is subtracted from the measured offset for each PPS individually, positive and negative values are possible.

First choose the PPS Analyzer on which you want to configure the delays then choose the PPS input to correct. If you are done with an Analyzer press “Change Delays”, only then the values will have an effect.

Note: Be aware, that changing the delay on the reference PPS has an influence on all PPS belonging to the same analyzer.

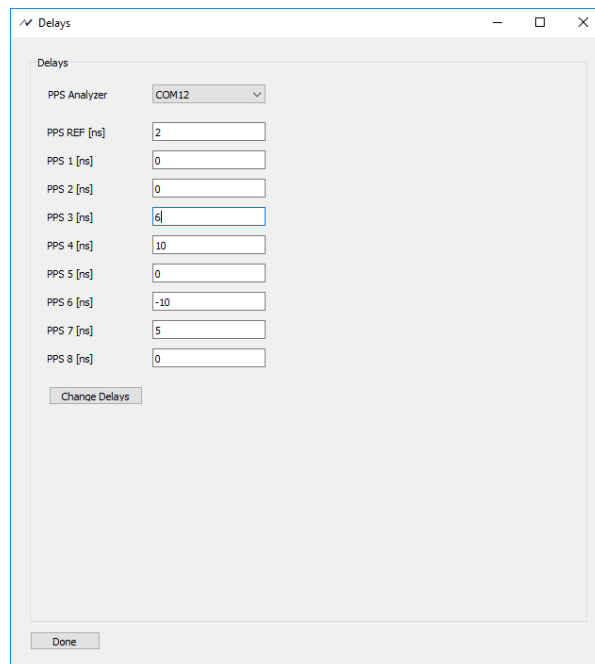


Figure 6: PPS Analyzer Software Delay Screen

## 2.3 Run

1. Connect the Arty board via USB (which is combined JTAG and UART)
2. Download the bitstream to your Arty (via JTAG or flashed)
3. Connect a PPS to the REF\_PPS\_IN input
4. Connect the other PPS inputs (if not all are used make sure they are on a stable 0 logic level, there are weak pull downs on the pins).
5. Open the Universal PPS Analyzer application
6. Press Connect
7. Wait until the grey signal which is the reference PPS error is close to zero and the InSync LED is lit on the Arty, then clear the screen.
8. Check your PPS signals

## 2.4 Download

The bitstream and application can be downloaded from <http://www.nettime-logic.com/downloads.php>

The source code of the GUI can be found here:

<https://github.com/NetTimeLogic/UniversalPpsAnalyzer>

The download page is password protected, contact us via [contact@nettime-logic.com](mailto:contact@nettime-logic.com) to get access.

The PPS Analyzer software is free of charge and available under the LGPL 3.0 license. The FPGA part is available as freeware, binary only.

---

## A List of tables

Table 1:	Revision History.....	4
Table 2:	Definitions.....	6
Table 3:	Abbreviations .....	6
Table 4:	Pinout.....	10

## B List of figures

Figure 1:	Context Block Diagram .....	7
Figure 2:	PPS Analyzer Hardware .....	9
Figure 3:	Arty (source Digilent Inc) .....	10
Figure 4:	PPS Analyzer Software Connected.....	11
Figure 5:	PPS Analyzer Software PPS.....	12
Figure 6:	PPS Analyzer Software Delay Screen .....	13