Functional simulation of the RISC-V core Verilog netlist and testbench

1.Introduction of iverilog and gtkwave:

Icarus Verilog (iVerilog) is a free, open-source Verilog simulator and synthesis tool, while GTKWave is a waveform viewer that displays simulation results, making them a powerful combination for Verilog development.

- What is Verilog netlist?

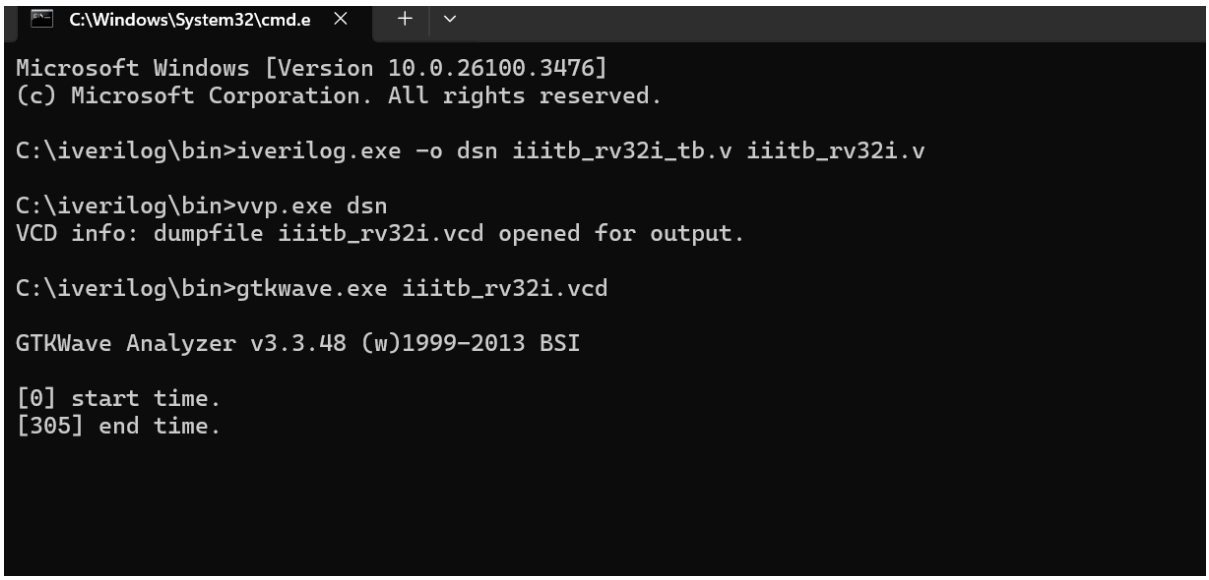
In the context of Verilog and digital design, a netlist is a textual description of the connectivity of a circuit, detailing the components, their interconnections, and optionally, their placement and routing, serving as a blueprint for simulation and physical implementation.

- Why test bench is necessary for RISC-V core?

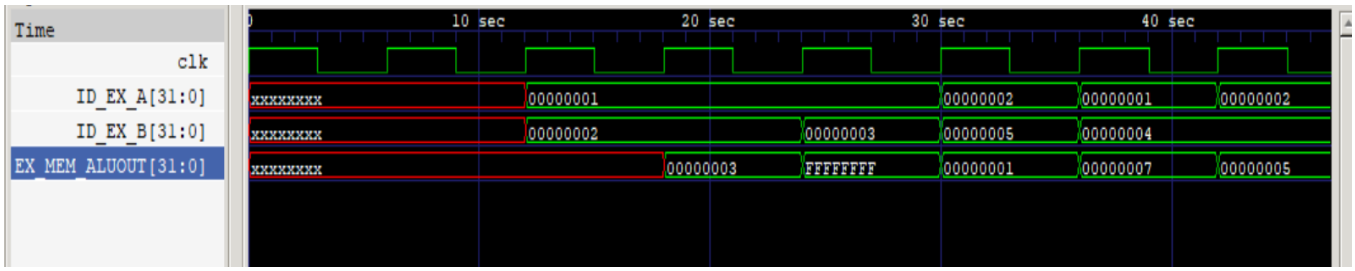
A testbench is crucial for verifying RISC-V cores because it provides a controlled environment to simulate and test the core's functionality, ensuring it adheres to the RISC-V instruction set architecture (ISA) and performs as expected

2. Installed iverilog and gtkwave for windows

Command for simulation:



3.Output



Values:

r1=00000001

r2=00000002

r3=00000003

r4=00000004

r5=00000005

Instructions and their outputs are shown below which can be verified through the output waveform:

- add r6,r1,r2

  r6=00000003

- sub r7,r1,r2

  r7=FFFFFFFF

- and r8,r1,r3

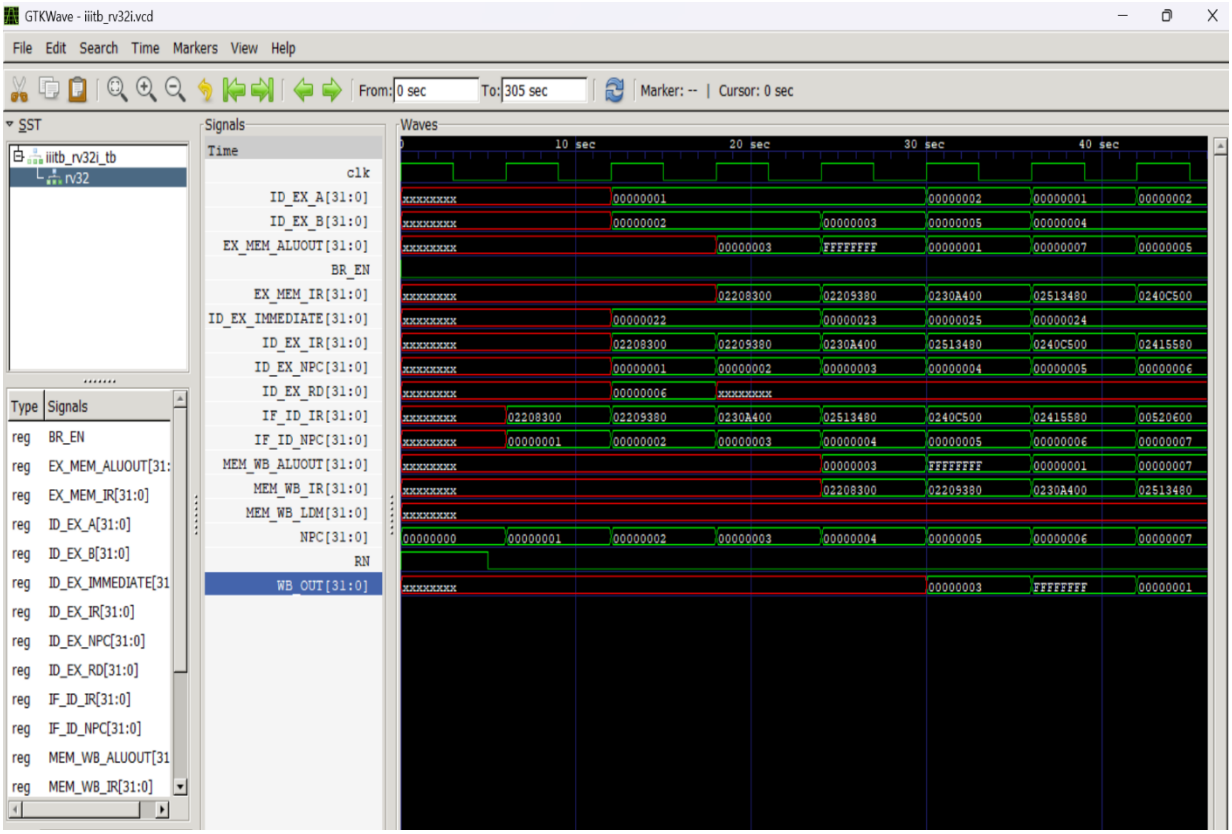
  r8=00000001

- or r9,r2,r5

  r9=00000007

- xor r10,r1,r4

r10=00000005



The above figure shows all the signals of Verilog netlist.