$[rwe == 0]$ & $[\texttt{dataOnOff} == 0]/$
$[\texttt{ready} = 1]$
stop frame blocking

$[C_r \neq N_f]/[\texttt{frameValid} = 1]$
remain for $N_f \cdot t_c$ ns to consecutively
read the realized frame samples from
SP-RAM and output them via the
$\texttt{frameSample}$ output

$[\texttt{dataOnOff} == 1]$ & $[\texttt{dataValid} == 0]/$
wait for around t_s ms to receive a sample
at the $\texttt{dataSample}$ input

$[\texttt{dataOnOff} == 0]/$
$[\texttt{ready} = 1]$
remain in the idle state

$[\texttt{dataOnOff} == 1]/$
$[\texttt{ready} = 0]$
start frame blocking;
switch to memory write phase
to realize a frame in SP-RAM

$[\texttt{dataOnOff} == 1]$ & $[\texttt{dataValid} == 1]$
or
$[\texttt{dataOnOff} == 0]$ & $[C_w \neq 0]/$
$[rwe = 1]$
write the received sample or
a zero magnitude sample
in SP-RAM

$[rwe == 1]$ & $[fb == 1]$ & $[C_w == N_f]$
or
$[rwe == 1]$ & $[fb == 0]$ & $[C_w == N_f - N_o]/$
$[rwe = 0]$
switch to memory read phase to output
the realized frame from SP-RAM

power-up

$[\texttt{dataOnOff} == 0]$ & $[C_w == 0]/$
$[\texttt{ready} = 1]$
stop frame blocking

$[rwe == 1]$ & $[fb == 1]$ & $[C_w \neq N_f]$
or
$[rwe == 1]$ & $[fb == 0]$ & $[C_w \neq N_f - N_o]/$
$[rwe = 0]$
continue to realize a frame in SP-RAM

$[C_r == N_f]/[\texttt{frameValid} = 0]$
continue frame blocking to realize
the subsequent frame in SP-RAM

$[rwe == 0]$ & $[\texttt{dataOnOff} == 1]/$
continue frame blocking