Big background

Related work in this area

 How to tackling with the memory bandwidth bottleneck and improve the performance? (Especially for <u>embedded system</u>)

better cache hit rate

Through program code transformation (eg. Loop blocking)

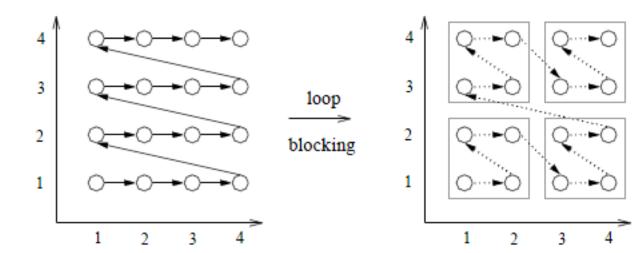
Increasing memory port utilization

Coding Address

reduce transition
activity on address bus,
thus reduce power

Reconfigurable cache architecture

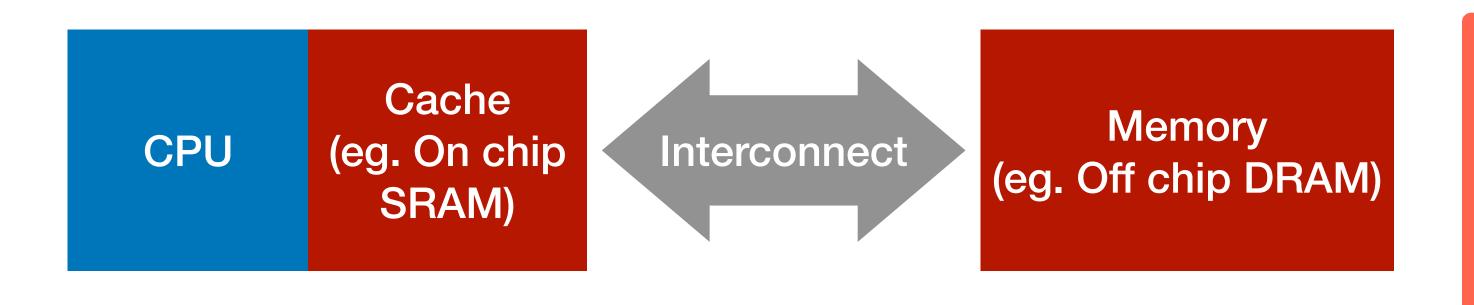
But introduced <u>more</u> architectural overhead



This paper's focus

A more specific problem this paper works on

A macro view

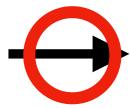


Weaker binding

Can we achieve <u>same</u> performance with smaller bandwidth?

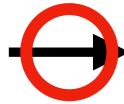
Two
Dependencies
Exist here

The higher performance needs



The higher bandwidth needs

The higher bandwidth it utilized -



The higher energy it consumed

Strong binding
Need Device level innovation
(Eg. New type memory)