# Big background

## The theme

- Memory wall - mismatch between cpu development and memory BW
- Memory bandwidth is the bottleneck of improving processor performance

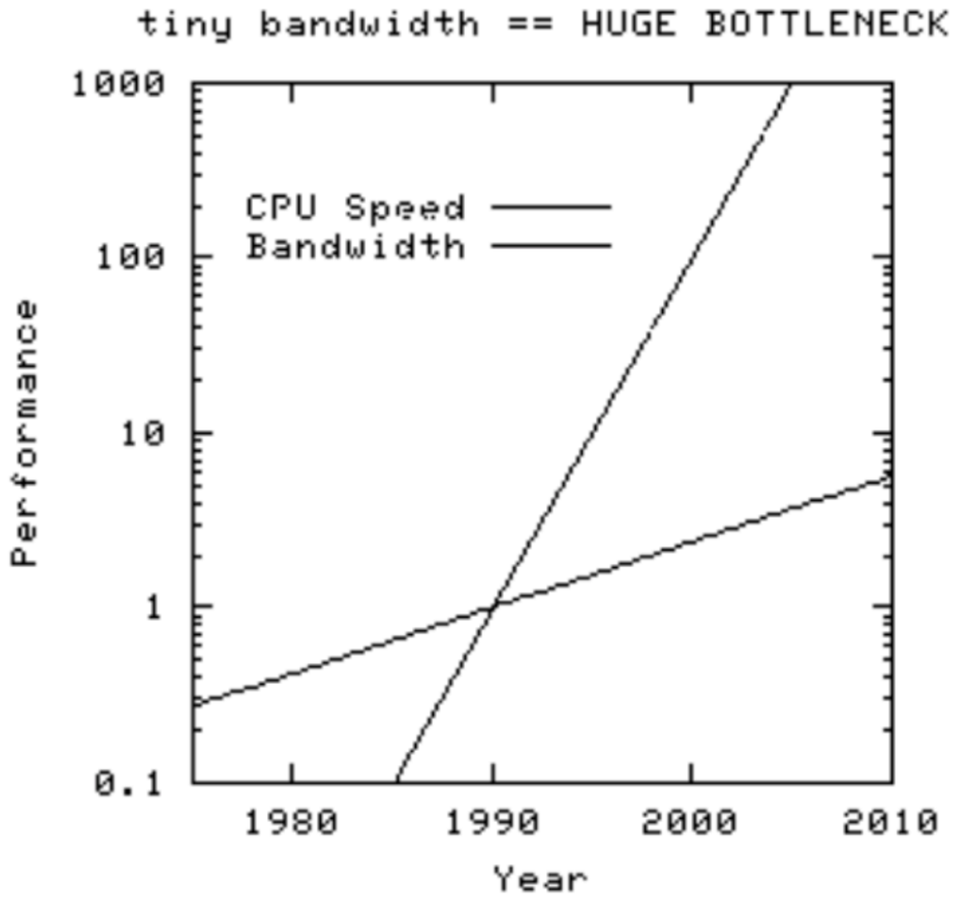


**Figure 5: McCalpin's CPU Speed vs. Bandwidth**

McKee, Sally A. "Reflections on the memory wall." *Proceedings of the 1st conference on Computing frontiers*. 2004.

# Big background

## Related work in this area

- How to tackling with the memory bandwidth bottleneck and improve the performance? (Especially for embedded system)

better **cache hit rate**

Through program code transformation (eg. Loop blocking)

Increasing memory port utilization

Coding Address

reduce transition activity on address bus, thus reduce power

Reconfigurable cache architecture

But introduced more architectural overhead