Big background

Related work in this area

- How to tackling with the memory bandwidth bottleneck and improve the performance? (Especially for embedded system)

better **cache hit rate**

Through program code transformation (eg. Loop blocking)

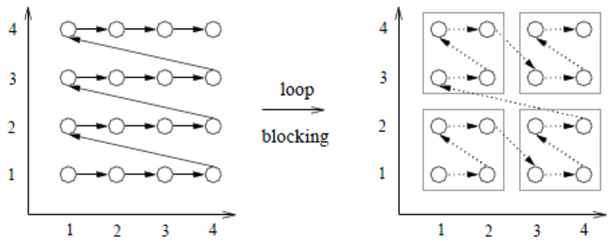
Increasing memory port utilization

Coding Address

reduce transition activity on address bus, thus reduce power

Reconfigurable cache architecture

But introduced more architectural overhead



This paper's focus

A more specific problem this paper works on

- A macro view