A single case

Power comparison - p1

- For off chip **memory access**
- dram_power = 2W 8bit(1Byte/cycle), keeping access dram @100MHz
- bus_power = 0.6W 8bit(1Byte) bus, being active every cycle @100MHz
- mem_power = bandwidth * (dram_power + bus_power)

Cpu is not visiting memory all the time

Hence its unit is Byte/cycle, it can be understood as **the percentage utilization** of the memory port

Less use means less power consumption

- bandwidth_tradition(0.32) > bandwidth_spilt(0.26)
- Hence: **mem_power_tradtion > mem_power_split**

A single case

Power comparison - p2

- For **cache access**
- cache energy consumption per cache access depends on total cache size, 6KB(spatial cache)<8KB(traditional), 2KB(temporal cache)<8KB(traditional)
- the proposed split cache is energy saving in each cache access:
- energy_per_cache_access_tradition > energy_per_cache_access_split
- similar hit rate means similar access numbers.
- cache_energy = access_numbers * energy_per_cache_access
- Obvious: **cache_power_tradition > cache_power_split**