LAB - 01

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SECTION: CSE-2

COURSE: EEE-4384

Task -1

Name of the experiment: Simulation of the Voltage-Current Characteristics of PN Junction Diode using PSIM

Objective:

To observe the voltage-current characteristics of PN junction diode under forward and reverse bias condition and to determine cut in voltage, reverse saturation current and forward dynamic resistance.

Theory:

A PN junction diode conducts only in one direction. It is an example of unilateral element. The V-I characteristics of the diode are curve between voltage across the diode (Vd) and current through the diode (Id). When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode) is connected to +ve terminal and N type (cathode) is connected to -ve terminal of the supply voltage is known as forward bias. The potential barrier is reduced, when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward

voltage. When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected to the –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current is due to minority charge carriers. An ideal PN junction Diode is a two terminal polarity sensitive device that has zero resistance (diode conducts) when it is forward biased and infinite resistance (diode doesn't conduct) when it is reverse biased.

Due to this characteristic, the diode finds number of applications as 1. Rectifiers in DC power supply,2. Switch in digital circuits, 3. Clamping, clipping circuits network used in TV Receiver,4. Demodulator (detector) circuits.

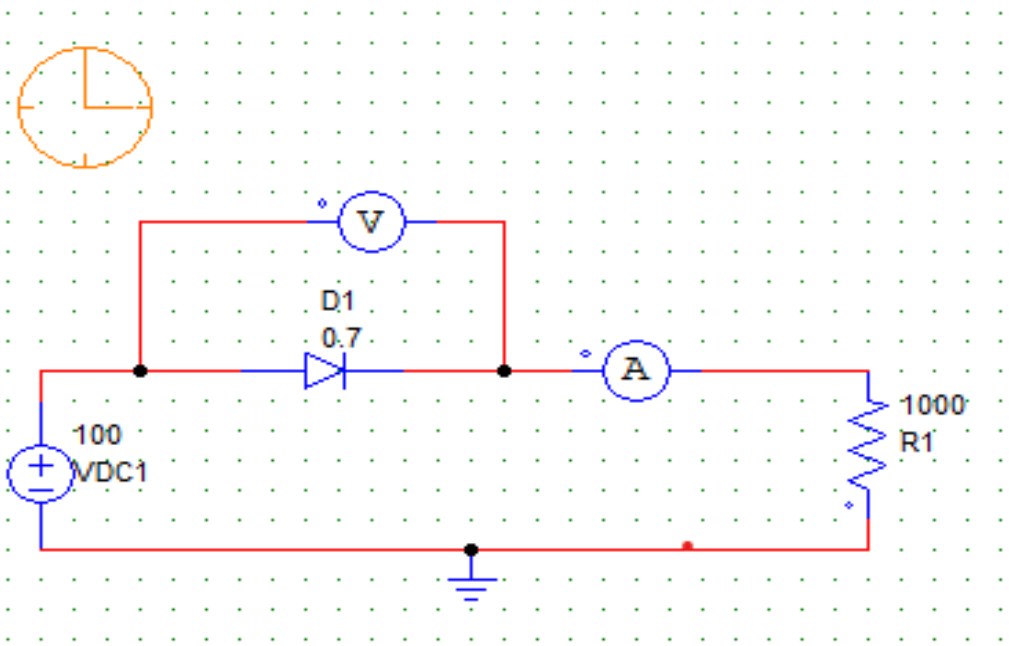


Fig: The circuit that has been drawn

Input Table :

Sl.No	DC Voltage Source(V)	Diode Voltage (V)	Diode Current (mA)	Current (mA)
1	0	0	0	0
2	0.1	0.1	2.00E-08	2.00E-05
3	0.2	0.2	3.00E-08	3.00E-05
4	0.3	0.3	4.00E-08	4.00E-05
5	0.4	0.4	4.50E-08	4.50E-05
6	0.5	0.5	5.00E-08	5.00E-05
7	0.6	0.6	6.00E-08	6.00E-05
8	0.7	0.62	6.10E-08	6.10E-05
9	1	0.7	3.00E-04	3.00E-01
10	50	0.70000002	5.00E-02	5.00E+01
11	70	0.70000003	7.00E-02	7.00E+01
12	100	0.70000009	9.00E-02	9.00E+01

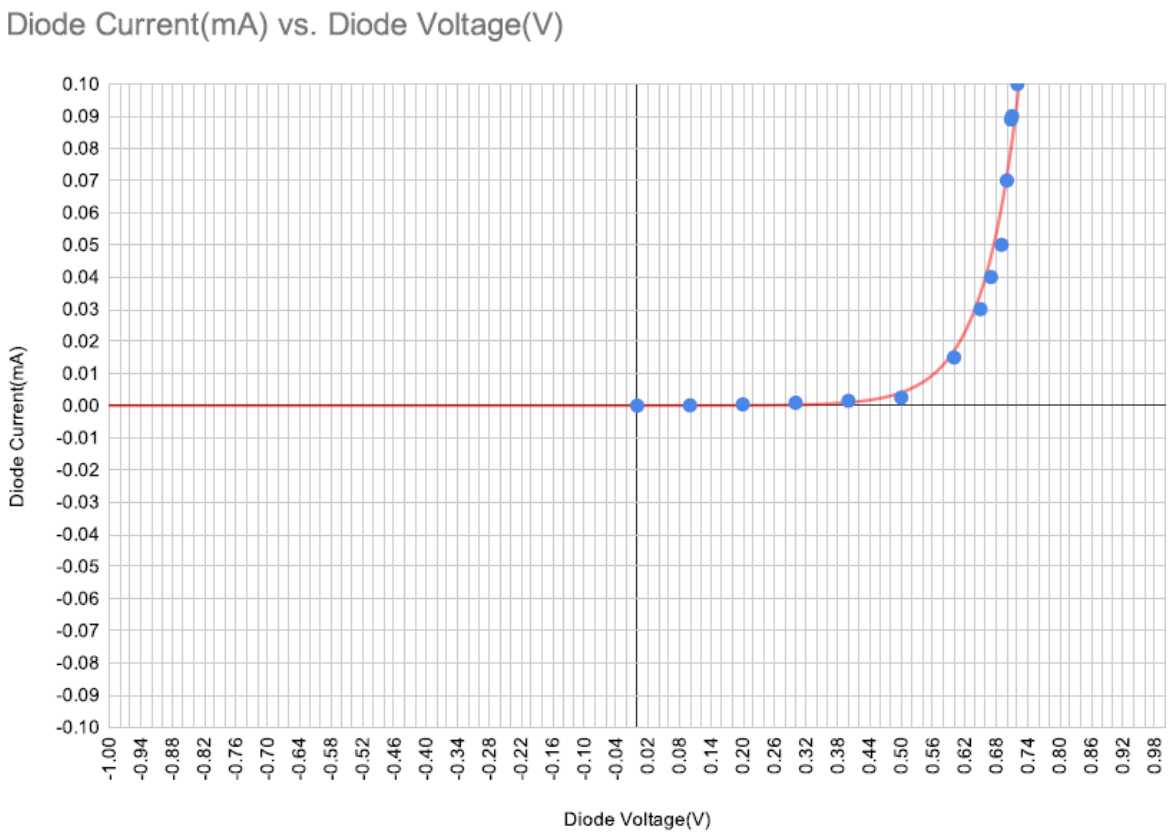


Fig: I vs V graph

Task -2

Name of the Experiment: Simulation of the Voltage-Current Characteristics of Zener Diode using PSIM.

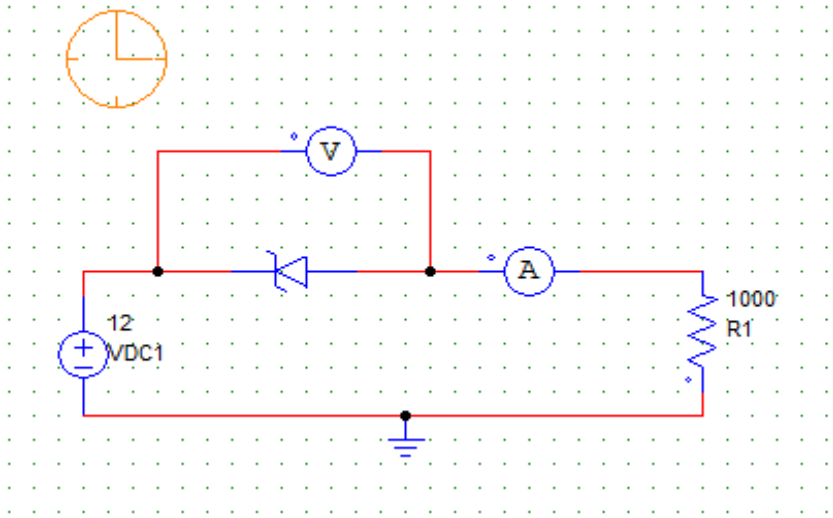


Fig: The Circuit for forward bias

Data Table for forward bias:

Sl.No	DC Voltage Source(V)	Diode Voltage (V)	iode Current (mA)	Current (mA)
1	0	0	0	0
2	0.1	0.1	1.00E-04	1.00E-01
3	0.2	0.2	4.00E-04	4.00E-01
4	0.3	0.3	9.00E-04	9.00E-01
5	0.4	0.4	1.50E-03	1.50E+00
6	0.5	0.5	2.50E-03	2.50E+00
7	0.6	0.6	1.50E-02	1.50E+01
8	0.7	0.62	3.00E-02	3.00E+01
9	1	0.7	3.00E-04	3.00E-01
10	50	0.70000002	5.00E-02	5.00E+01
11	70	0.70000003	7.00E-02	7.00E+01
12	100	0.70000009	9.00E-02	9.00E+01

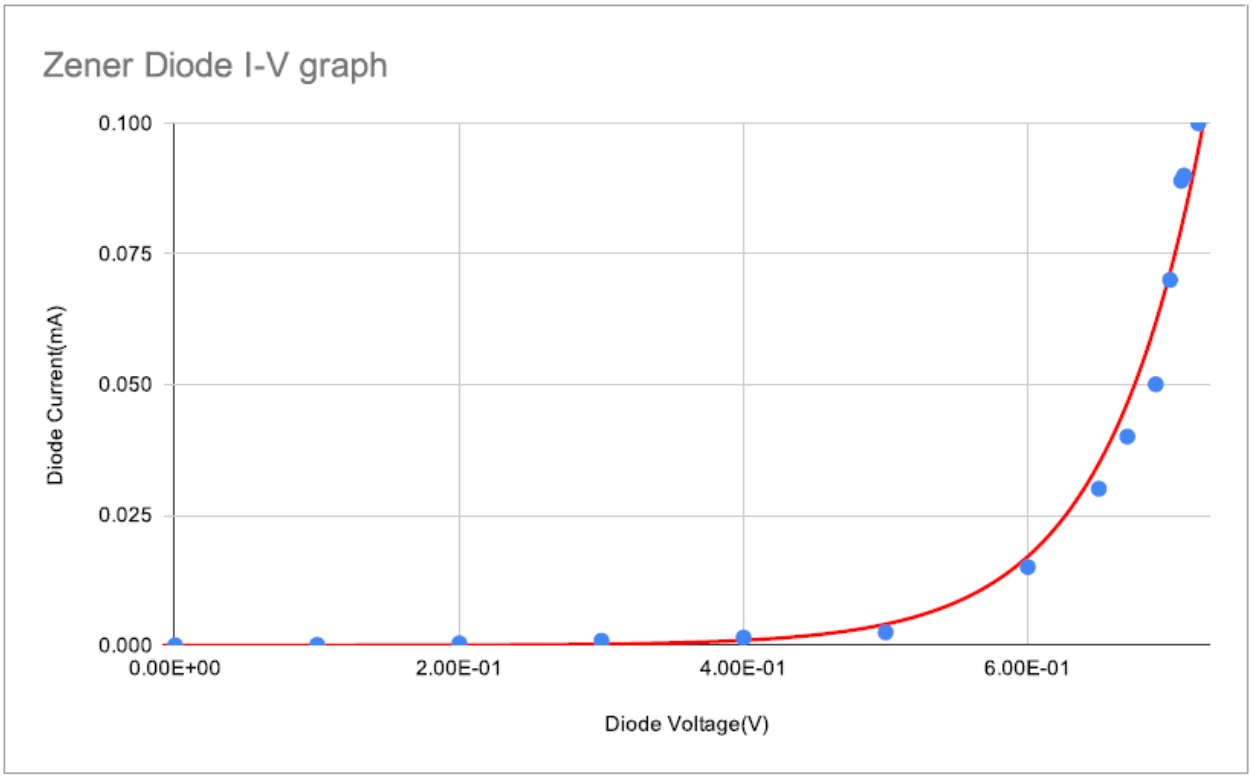


Fig: Graph for forward bias in Zener diode

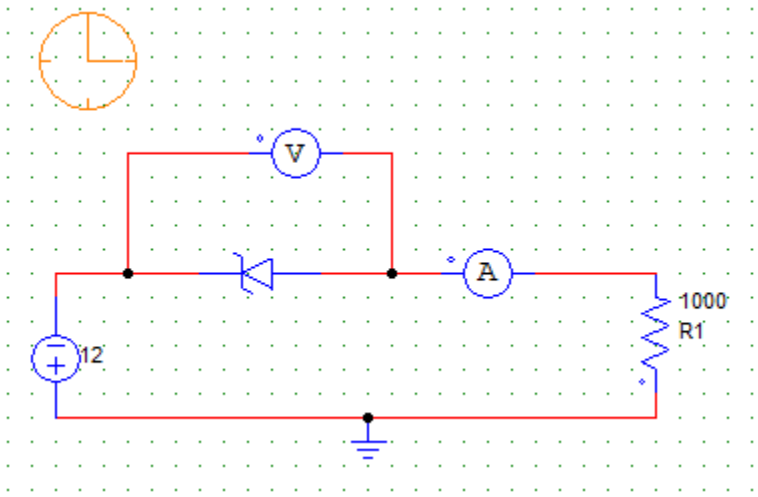


Fig: The circuit for reverse bias

Data Table for reverse bias:

Sl.No	Reverse Bias(V)	Diode(V)	Diode I(A)	Current (mA)
1	0	0	0.00E+00	0.00E+00
2	1	-1	0.00E+00	0.00E+00
3	5	-5	0.00E+00	0.00E+00
4	8	-5.001	0.00E+00	0.00E+00
5	10	-10	-8.00E-06	-8.00E-03
6	11	-10.001	-1.00E-06	-1.00E-03
7	12	-12	-1.00E-05	-1.00E-02
8	12.3	-12	-3.00E-04	-3.00E-01
9	12.5	-12	-5.00E-04	-5.00E-01
10	13	-12	-1.00E-03	-1.00E+00
11	14	-12	-2.00E-03	-2.00E+00

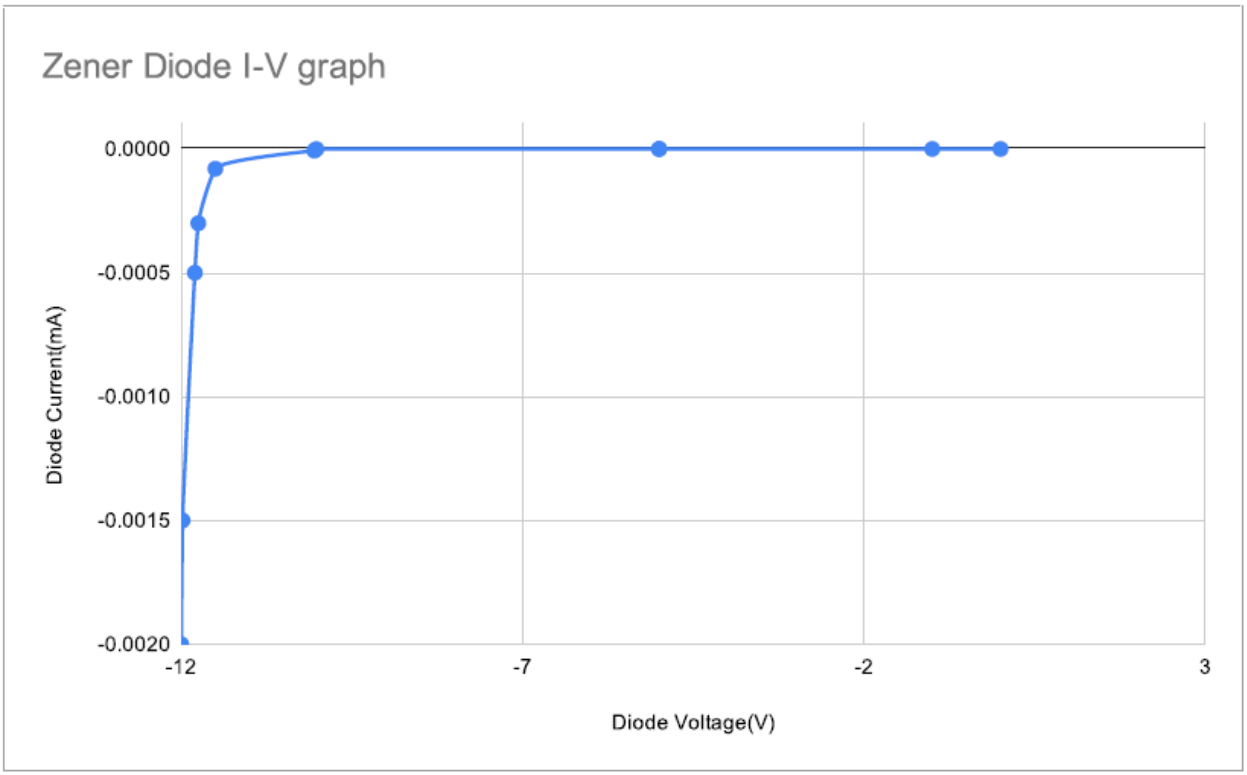


Fig: Graph for reverse bias in Zener diode

Task 3:

Name of the experiment : To simulate the Circuit and observe the wave shapes of Half wave Diode Rectifier using PSIM.

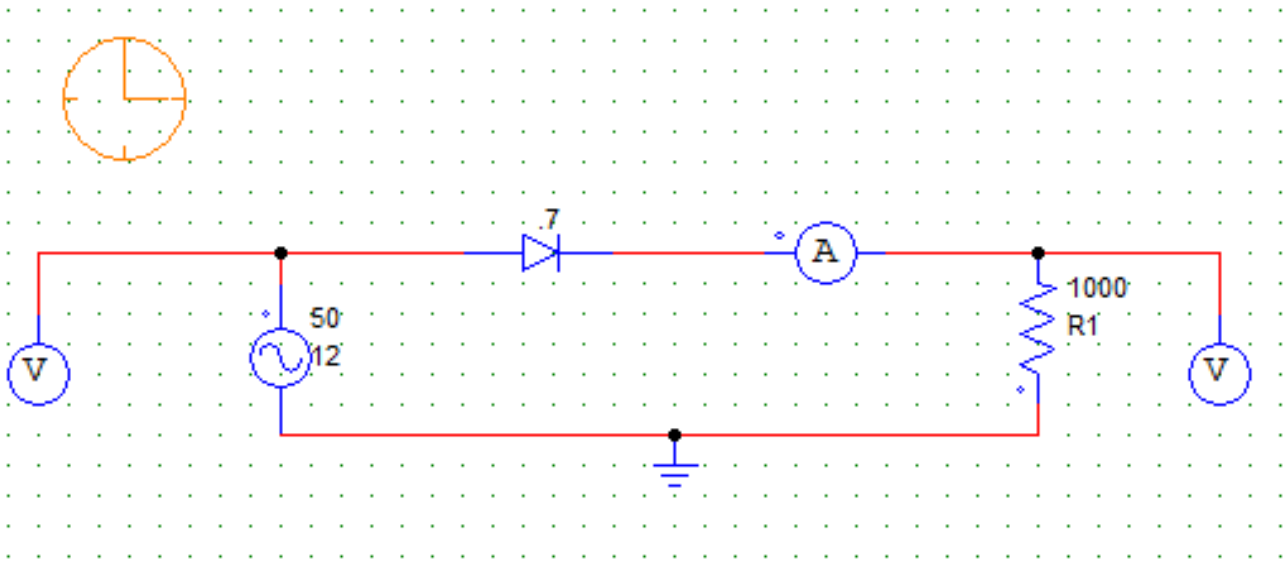


Fig: Half wave rectifier circuit

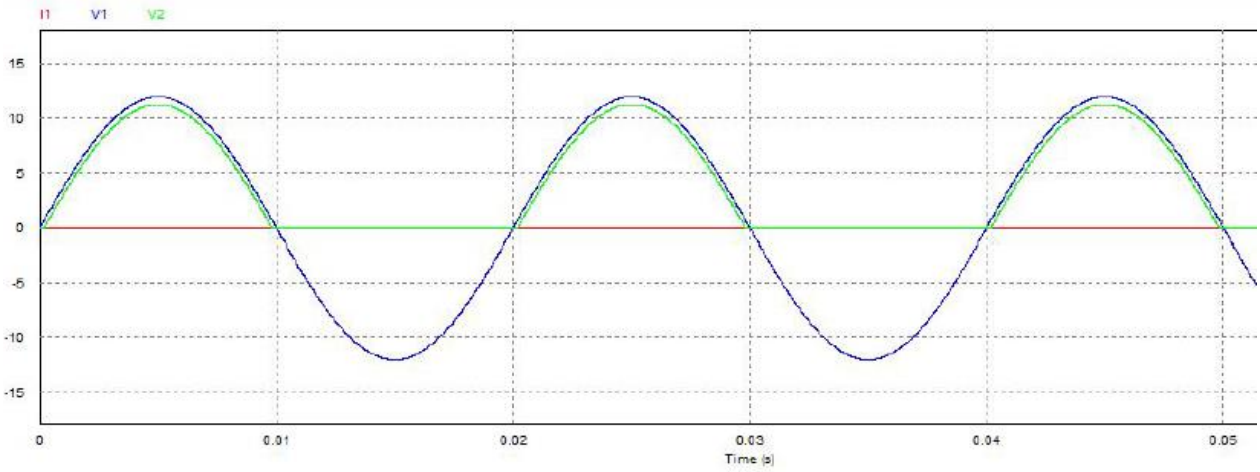


Fig: Graph representing half wave rectification

Data Table:

Sl.No	T	V1	V2
1	2.77E-04	1.04E+00	3.45E-01
2	7.77E-04	2.90E+00	2.20E+00
3	1.44E-03	5.26E+00	4.56E+00
4	2.10E-03	7.38E+00	6.68E+00
5	2.78E-03	9.19E+00	8.49E+00
6	3.49E-03	1.07E+01	9.99E+00
7	4.16E-03	1.16E+01	1.09E+01
8	4.77E-03	1.20E+01	1.13E+01
9	5.27E-03	1.20E+01	1.13E+01
10	5.72E-03	1.17E+01	1.10E+01
11	6.22E-03	1.11E+01	1.04E+01
12	6.66E-03	1.04E+01	9.70E+00
13	7.22E-03	9.21E+00	8.51E+00
14	7.55E-03	8.35E+00	7.65E+00
15	8.33E-03	6.03E+00	5.33E+00
16	8.99E-03	3.74E+00	3.04E+00
17	9.44E-03	2.12E+00	1.42E+00
18	9.77E-03	8.71E-01	1.71E-01
19	9.94E-03	2.44E-01	2.45E-05
20	1.03E-02	-1.22E+00	-1.22E-04
21	1.13E-02	-4.65E+00	-4.65E-04
22	1.24E-02	-8.15E+00	-8.15E-04

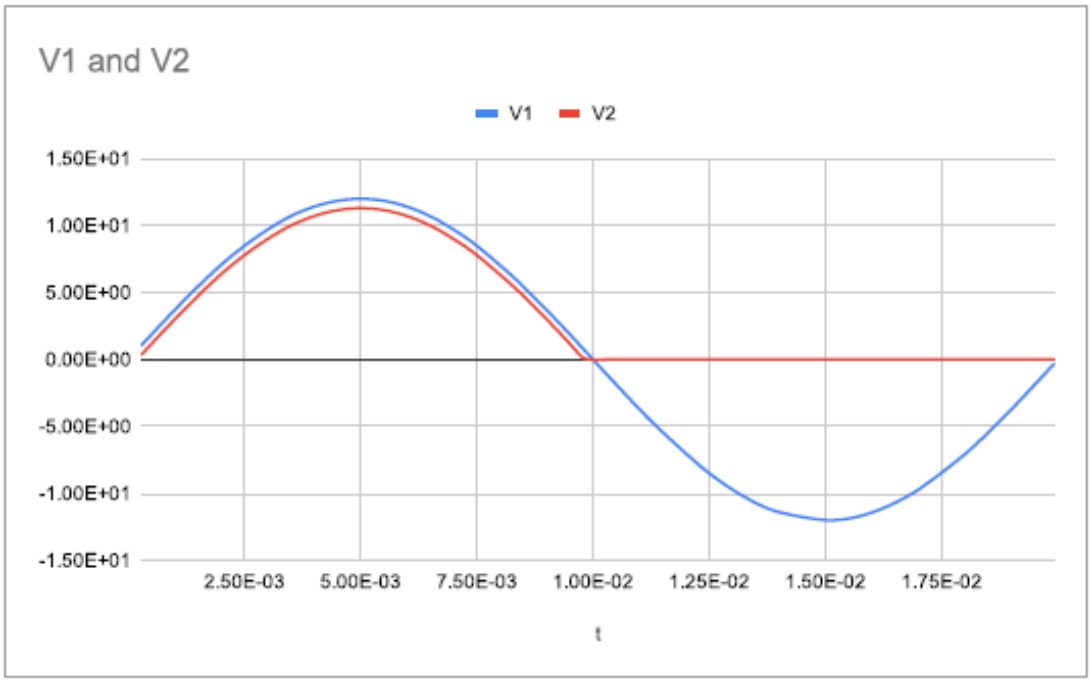


Fig: The graph of V1 and V2

Task – 4 :

Name of the experiment : Simulate the Circuit and observe the wave shapes of Full wave Diode Rectifiers using PSIM.

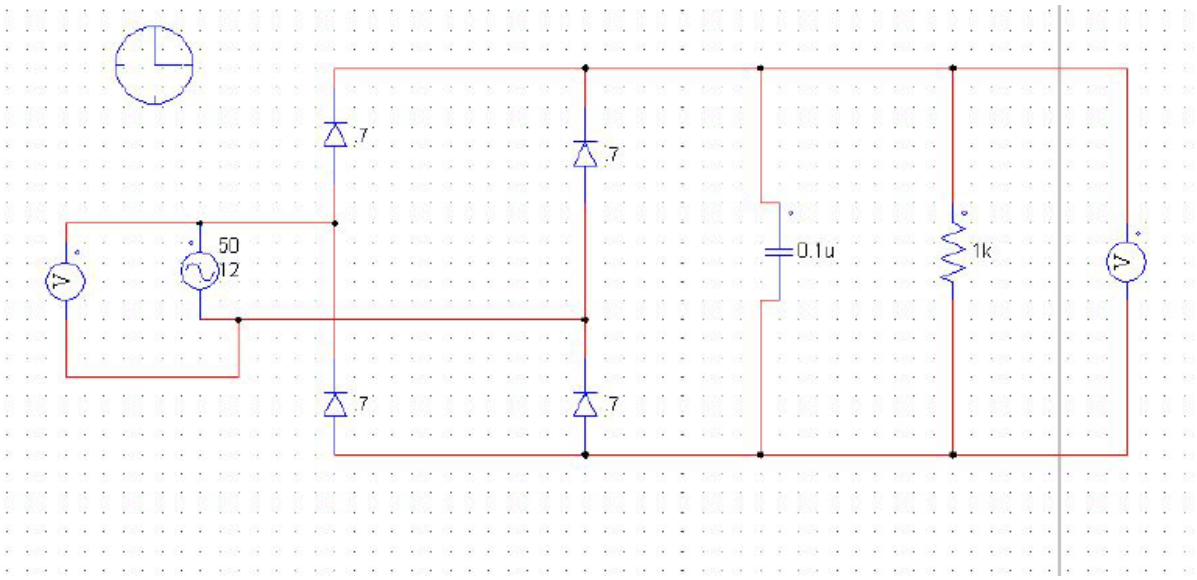


Fig : simulating the following circuit

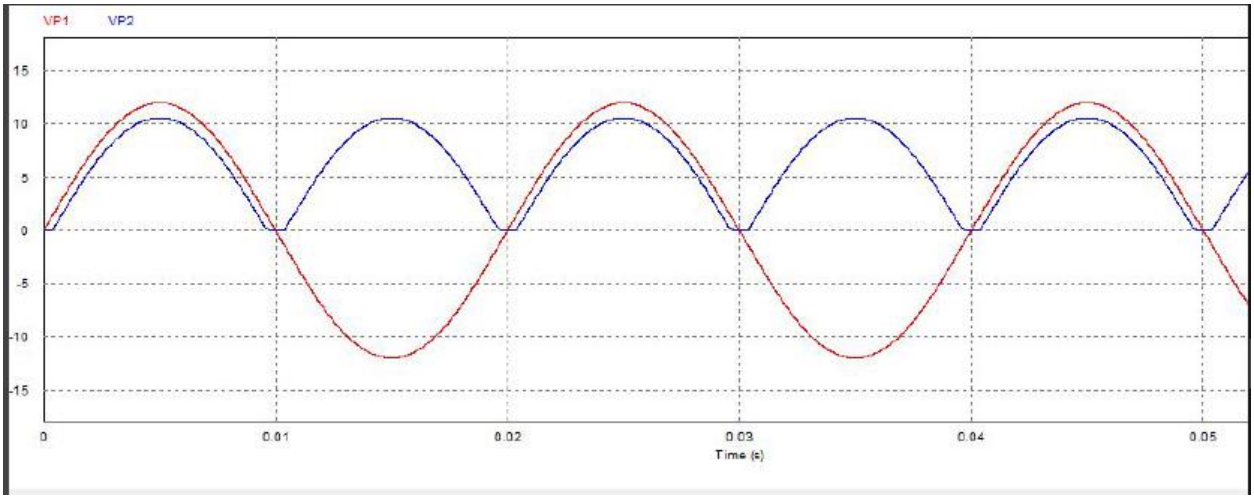


Fig : Full wave diode rectification graph

Data table:

Sl.No	T	Vp1	Vp2
1	5.55E-05	-4.16E-10	2.09E-01
2	8.94E-05	-5.91E-10	3.37E-01
3	1.00E-05	3.77E-02	-9.33E-11
4	3.88E-04	1.46E+00	6.11E-02
5	1.02E-03	3.78E+00	2.38E+00
6	2.03E-03	7.14E+00	5.74E+00
7	3.04E-03	9.80E+00	8.40E+00
8	4.05E-03	1.15E+01	1.01E+01
9	5.06E-03	1.20E+01	1.06E+01
10	6.07E-03	1.13E+01	9.93E+00
11	7.08E-03	9.53E+00	8.13E+00
12	8.09E-03	6.78E+00	5.38E+00
13	9.10E-03	3.35E+00	1.95E+00
14	9.43E-03	2.11E+00	3.16E-01
15	1.01E-02	-4.15E-01	1.10E-03

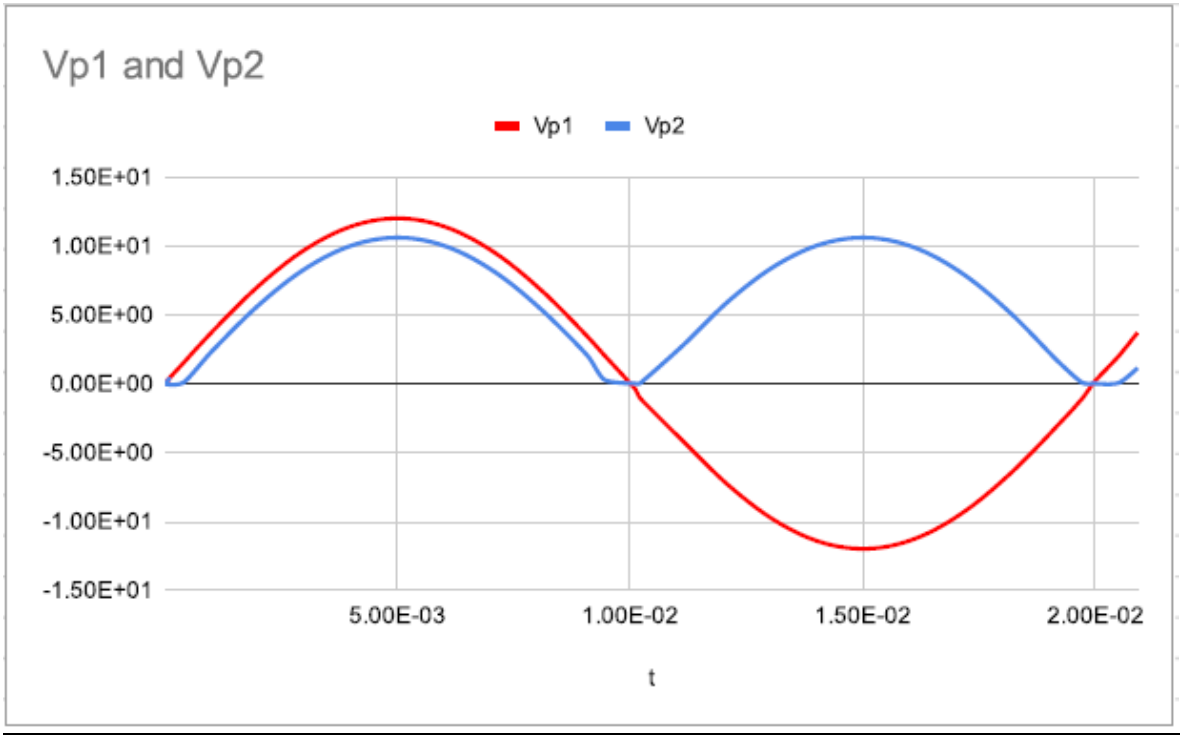
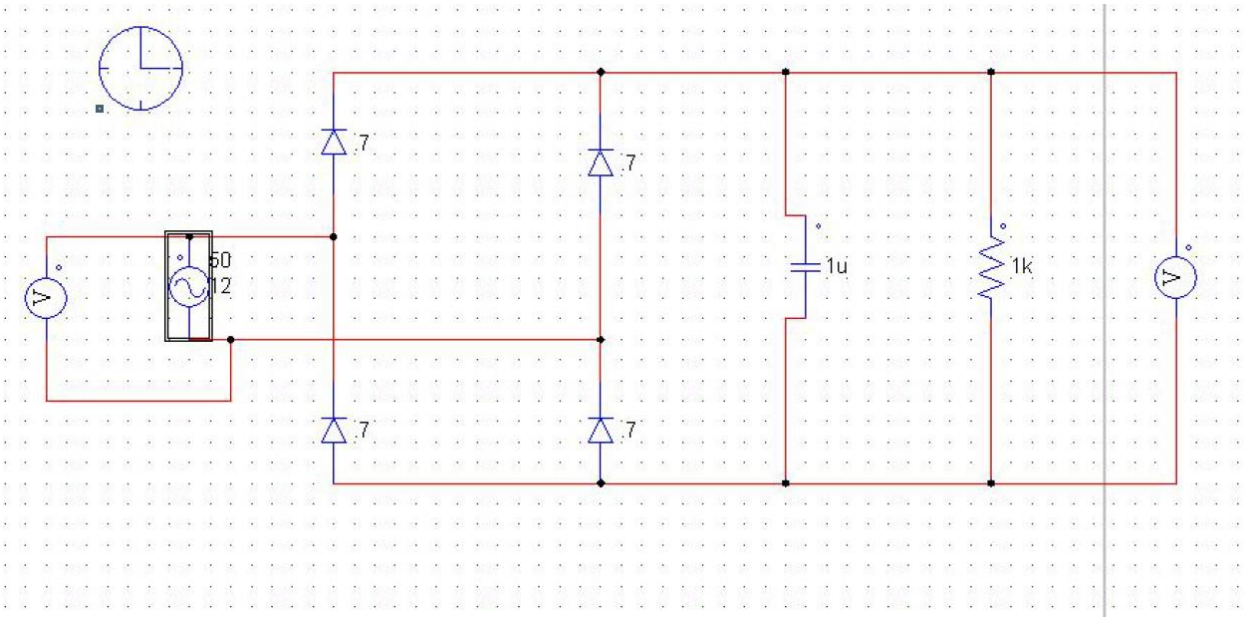
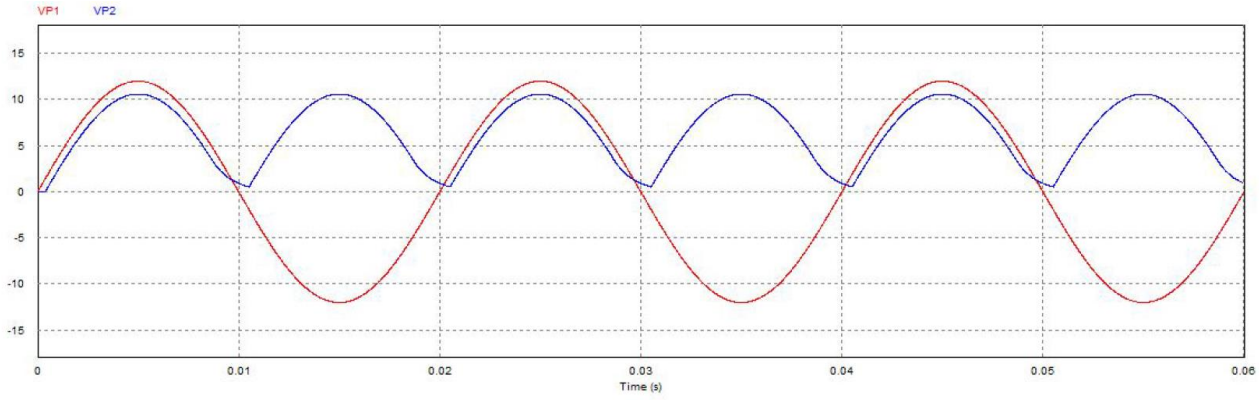


Fig: Vp1 and Vp2 graph


.7
.7
.7
.7
1u
1k
60
12


VP1
VP2
15
10
5
0
-5
-10
-15
0
0.01
0.02
0.03
0.04
0.05
0.06
Time (s)

Data table :

Sl.No	T	V1	V2
1	5.54E-05	2.09E-01	2.57E-09
2	1.95E-04	7.35E-01	6.77E-09
3	2.96E-04	1.12E+00	7.96E-09
4	3.19E-04	1.20E+00	8.03E-09
5	3.58E-04	1.35E+00	7.99E-09
6	6.84E-04	2.56E+00	9.80E-01
7	1.07E-03	3.97E+00	2.30E+00
8	1.67E-03	6.02E+00	4.60E+00
9	2.51E-03	8.52E+00	7.10E+00
10	3.44E-03	1.06E+01	9.18E+00
11	4.36E-03	1.18E+01	1.04E+01
12	4.91E-03	1.20E+01	1.06E+01

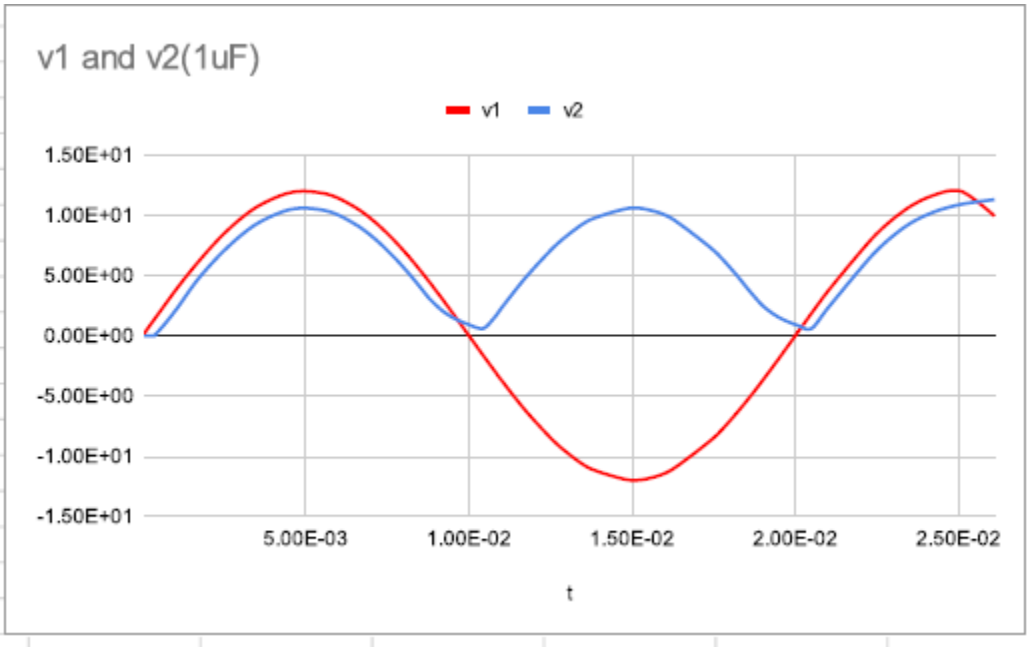
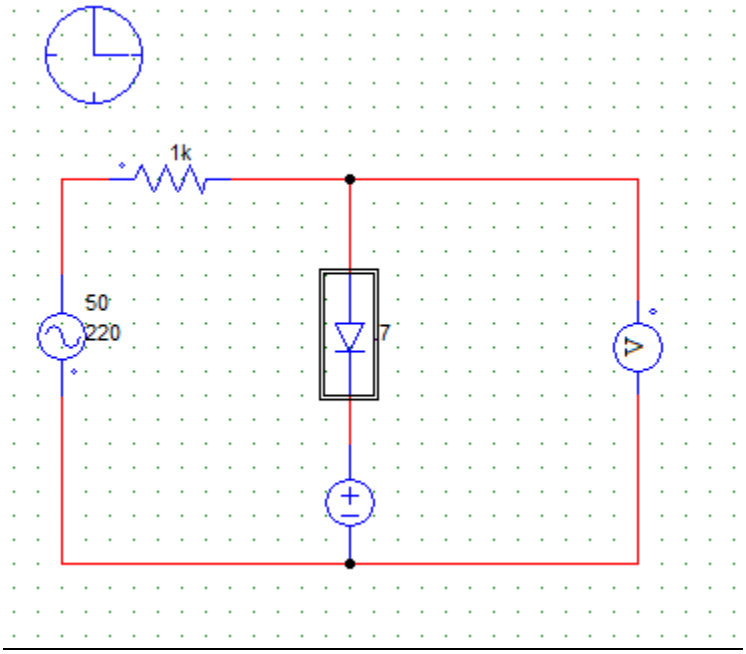
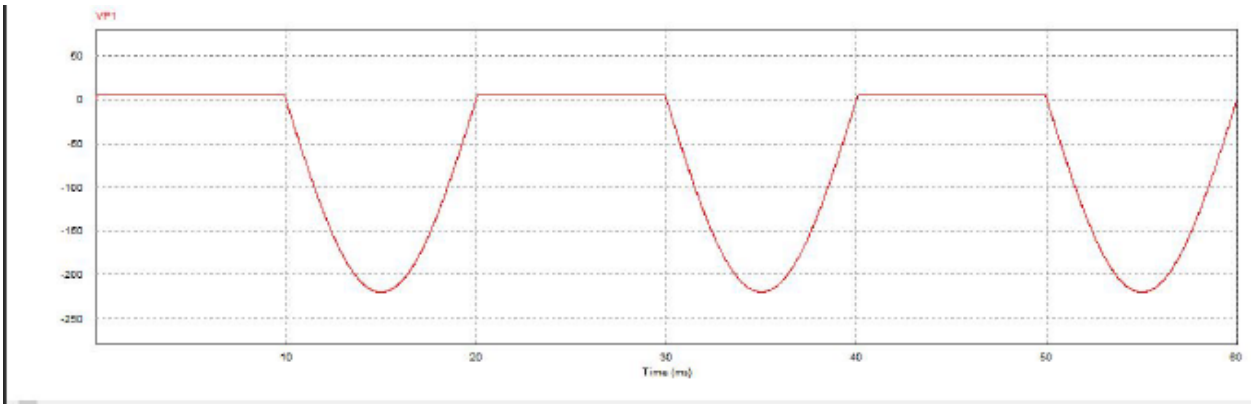


Fig: v1 and v2 graph

Assignment 1:





Data Table:

Sl.no	Time	Vp1
1	0.01008	-5.52757
2	0.01015	-10.3619
3	0.01038	-26.1983
4	0.01065	-44.6082
5	0.01081	-55.3749
6	0.01241	-151.088
7	0.01307	-180.766
8	0.01364	-200.203
9	0.01471	-219.065
10	0.01533	-218.796
11	0.01606	-207.893

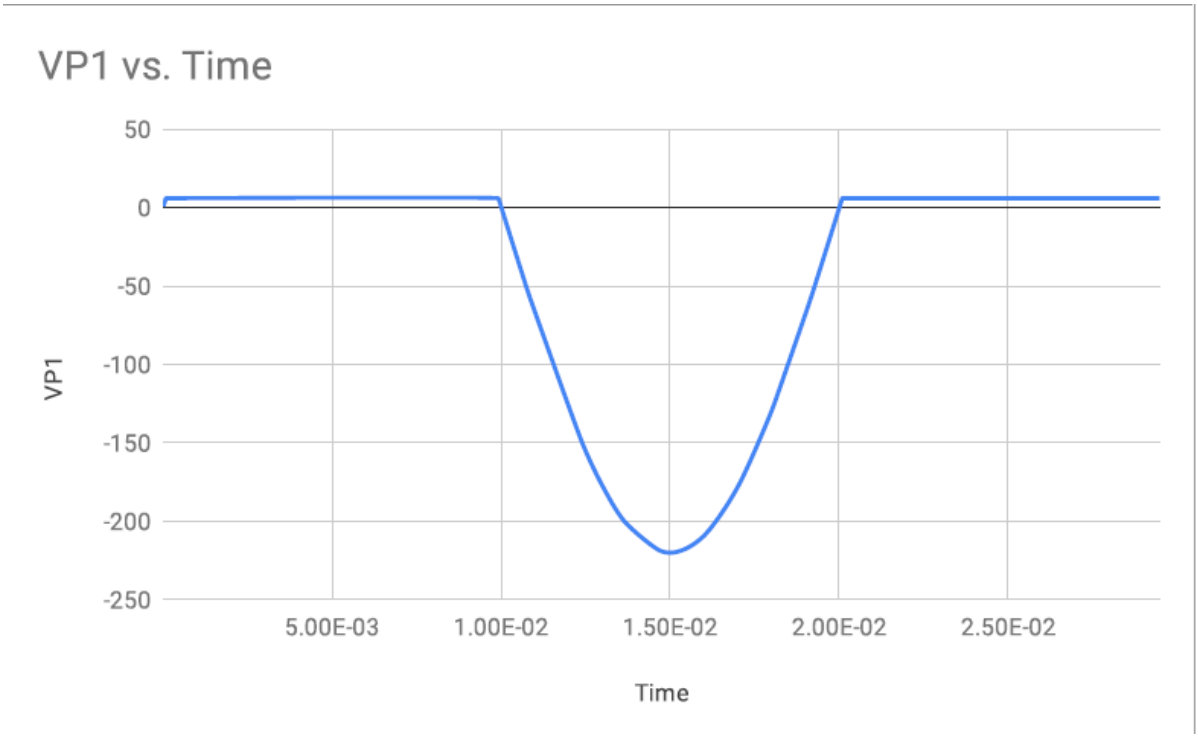


Fig: V_{P1} vs Time graph