Week 9 - T1 2020

Digital Integrated Circuits

ELEC2141: Digital Circuit Design

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Overview

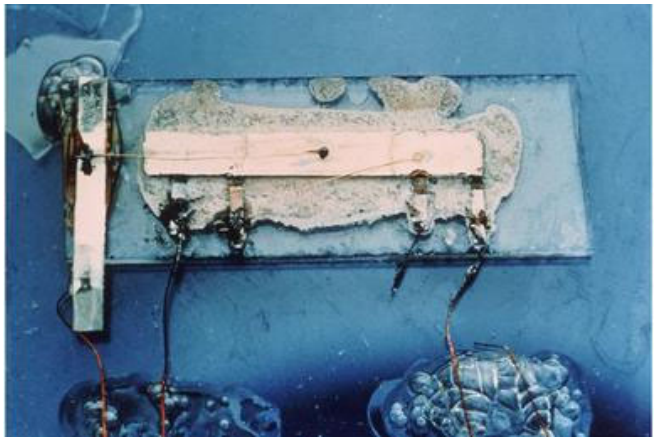
- Integrated circuits
- Digital logic families
- RTL, DTL, TTL logic
- MOSFET logic
- CMOS logic

Reading: Mano - Chapter 5: 5.1

Integrated circuits

An *integrated circuit* (informally, a "chip") is a semiconductor crystal (most often silicon) containing the electronic components for the digital gates and storage elements which are interconnected on the chip

The first integrated circuit was made from germanium by *Jack Kilby* in 1958. *Kilby* won the 2000 Nobel Prize in physics for his part in the invention of the integrated circuit.



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Integrated circuits

Terminology - Levels of chip integration

- ***SSI*** (*small-scale integration*) - fewer than 10 gates
- ***MSI*** (*medium-scale integration*) - 10 to 100 gates
- ***LSI*** (*large-scale integration*) - 100 to thousands of gates
- ***VLSI*** (*very large-scale integration*) - thousands to 100s of millions of gates
- ***ULSI*** *(ultra large-scale integration)* – more than 1 million gates
- ***GSI*** *(giga-scale integration)* – more than 1 billion transistors

Digital logic families

The IC digital logic families are

BJT
- RTL – Resistor-transistor logic
- DTL – Diode-transistor logic
- TTL – Transistor-transistor logic
- ECL – Emitter-coupled logic

FET
- MOS - Metal oxide semiconductor
- CMOS – Complementary metal-oxide semiconductor

The basic circuit in each is a NAND or NOR gate

Each IC logic family has a data book that lists all the integrated circuits in that family

The differences in the logic functions are in the specific electrical characteristics of the basic gate from which the circuit is constructed

Digital logic families

n-type e^- phosphorus doped
p-type e^+ boron doped

The first four digital logic families listed above – RTL,DTL,TTL,ECL- use bipolar junction transistors.

A bipolar junction transistor (BJT) can be a npn or pnp junction transistor.

The operation of a bipolar transistor depends on the flow of two types of carriers: electrons and holes.

The last two families- MOS and CMOS- employ a type of unipolar transistor called a metal-oxide-semiconductor field effect transistor (MOSFET or MOS in short).

The operation of a unipolar transistor depends of the flow of one type of majority carrier (electrons or holes).

Characteristics of logic families

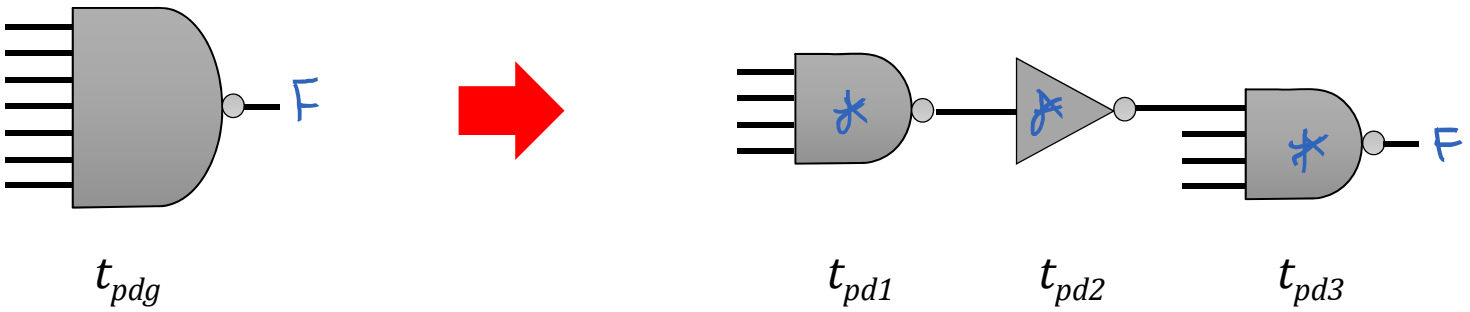
The most important parameters that are evaluated and compared in IC digital logic families are

- Fan-in
- Fan-out
- Power dissipation
- Propagation delay
- Noise margin
- Cost

Fan-in

Fan-in is the number of inputs to a gate, it is generally restricted to no more than **four** or **five** inputs. This is primarily due to gate speed.
Larger fan-in can be built from gates with lower fan-in during technology mapping.

Example: A 7-input NAND gate can be implemented with two 4-input NAND gates and an inverter.



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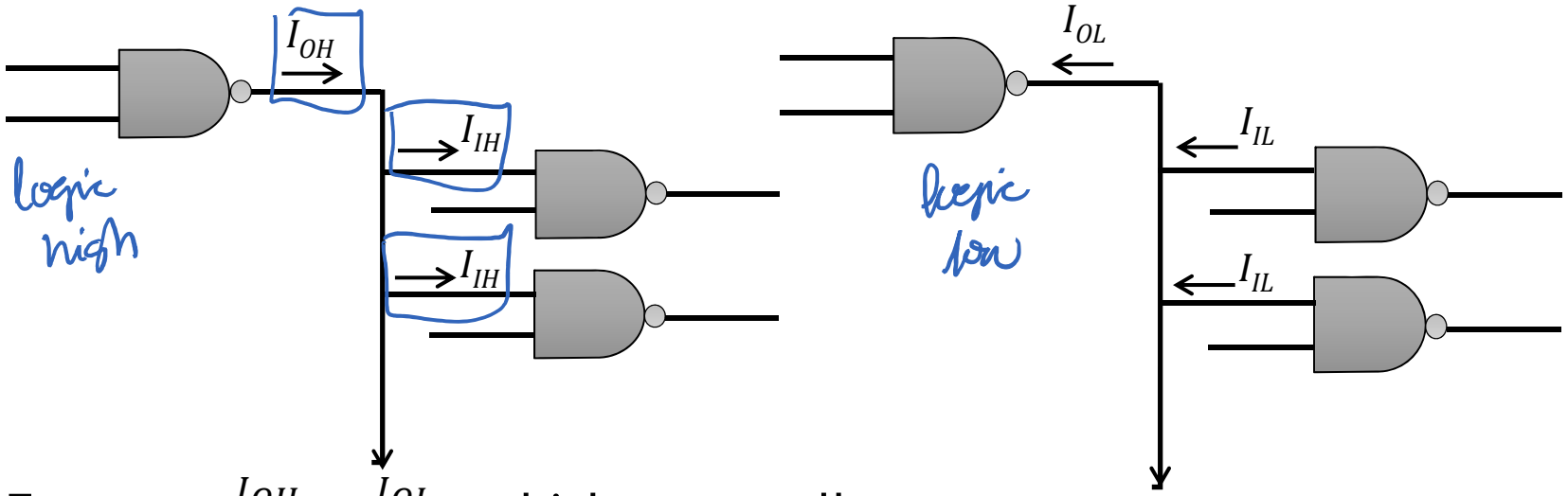
Fan-out

Fan-out is the maximum number of inputs that can be connected to the output of a gate without degrading its normal operation

Essentially, it is the number of standard loads that can be connected to the output of the gate

It is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of a gate



Fan-out = $\frac{I_{OH}}{I_{IH}}$ or $\frac{I_{OL}}{I_{IL}}$, whichever smaller

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Fan-out

A **standard load** refers to the amount of current needed by the input of gate in a logic family for current operation

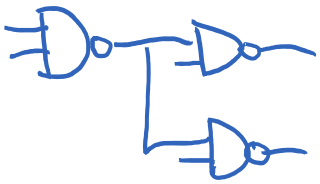
For example, the standard TTL gate have the following values for the currents:

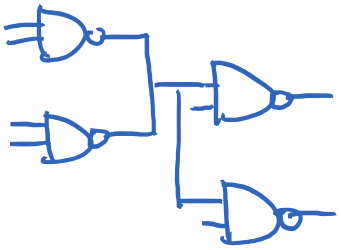
$I_{OH} = 400\mu A$ $I_{IH} = 40\mu A$ Fan-out $= \frac{400}{40} = 10$

$I_{OL} = 16mA$ $I_{IL} = 1.6mA$ Fan-out $= \frac{16}{1.6} = 10$

The fan-out of standard TTL is 10

This means the output of a TTL gate can drive up to 10 inputs of other gates in the same logic family





Power Dissipation

P_T/A

$2-3\,W/mm^2$

Specifies the amount power needed by the gate and represents the power delivered to the gate from the power supply

It is calculated from the supply voltage, V_{cc} and the current I_{cc} that is drawn by the circuit as $V_{cc} \times I_{cc}$

$$P_D(avg) = I_{CC}(avg) \times V_{cc}$$

where $$I_{CC(avg)} = \frac{I_{CCH} + I_{CCL}}{2}$$

DC

I_{CCH} is the current drawn from the power supply when the output of the gate is in the high level

I_{CCL} is the current drawn from the power supply when the output of the gate is in the low level

$P_{dyn} = CV^2 f$

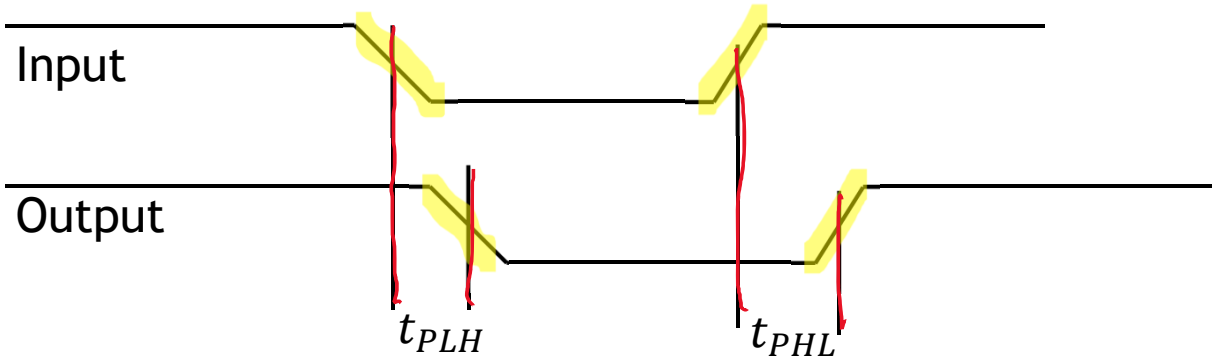
Propagation delay

Specifies the transition delay time for the signal to propagate from input to output when the binary input signal changes in value

The propagation delay is measured in nanoseconds (ns)

The signals that travel from the inputs of a digital circuit to its output pass through a series of gates. The sum of the propagation delays through the gates is the total delay of the circuit

Propagation delay is calculated from the input and output waveforms



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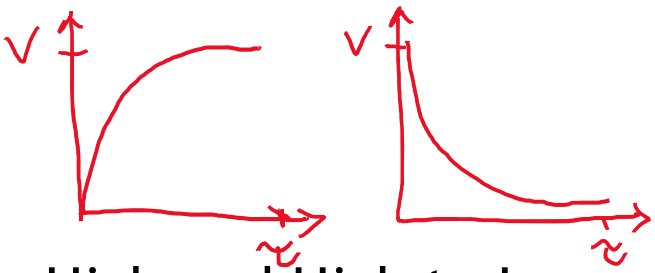
Propagation delay



Two delays are often considered: Low to High and High to Low

The two delays are not always the same and vary depending on the loading conditions

The longer delay of the two is taken as the propagation delay

Example: The delays for a standard TTL are $t_{PLH} = 7ns$ 11ns and $t_{PHL} = 11ns$ and are measured with a load resistance of 400 ohms and a load capacitance of 15pF

Propagation delay of a transistor circuit depends on two factors: storage time and RC time constants $\tau = RC$

Usually, manufacturers supply a formula or table that considers a fixed delay plus a delay per unit standard load times the standard loads driven

$t_{fd} + SL_{ud} \times SL$

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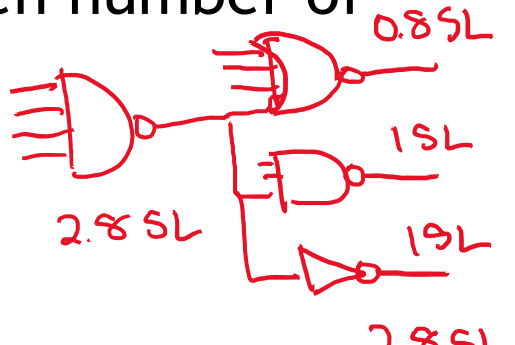
Propagation delay

Example: A 4 input NAND gate output is attached to the inputs of the following gates with the given number of standard loads representing their inputs:



4-input NOR gate - 0.8 standard load
3-input NAND gate – 1.00 standard load, and
inverter – 1.00 standard load

The formula for the delay of the 4-input NAND gate is

internal prop. NAND

$$t_{Pd} = 0.07 + 0.021\text{xSL ns}$$

$$t_{Pd} = 0.07 + 0.021\,(0.8 + 1 + 1)\text{ ns} = 0.129\text{ns}$$

In modern high-speed circuits, the portion of the gate delay due to wiring capacitance is often significant. Often it is difficult to evaluate since it depends of the layout of the wires in the integrated circuit

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Noise margin

Noise margin refers to the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit's output

Noises are unwanted signals that are superimposed on the normal operating signal

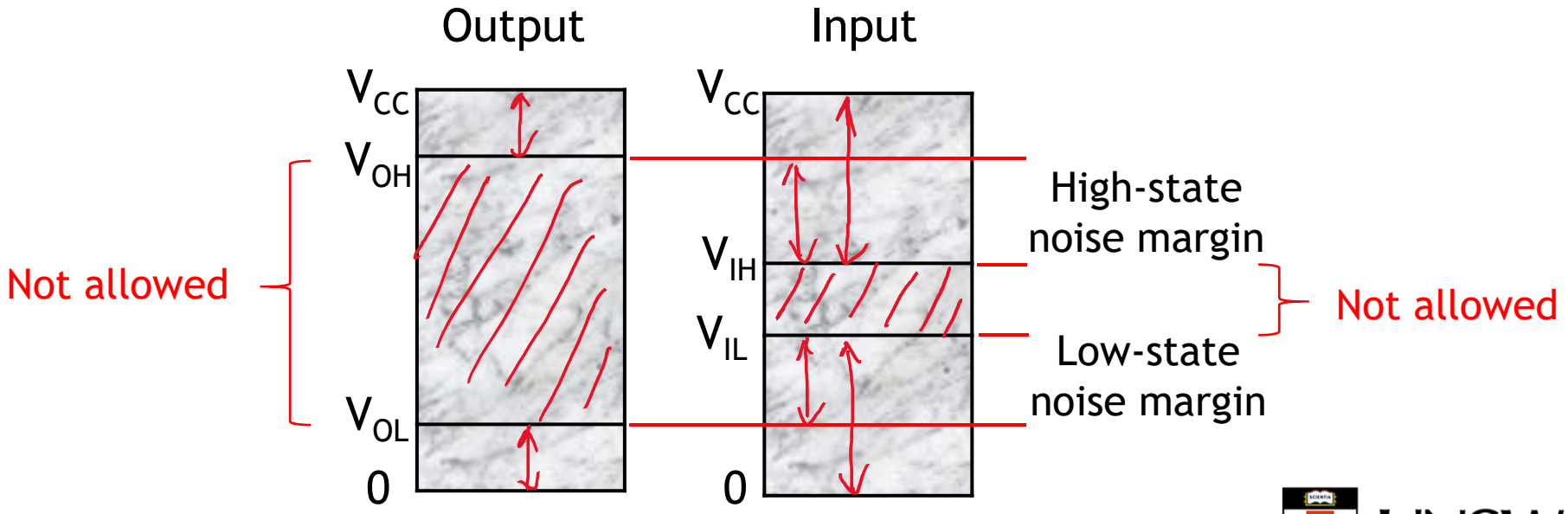
It is expressed in volts and represents the maximum noise that can be tolerated by the gate

It is calculated for the knowledge of the voltage signal available in the output of the gate and the voltage signal required in the input of the gate

Noise Margin

It is expressed in volts and represents the maximum noise that can be tolerated by the gate.

Calculated for the knowledge of the voltage signal available in the output of the gate and the voltage signal required in the input of the gate.



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Cost

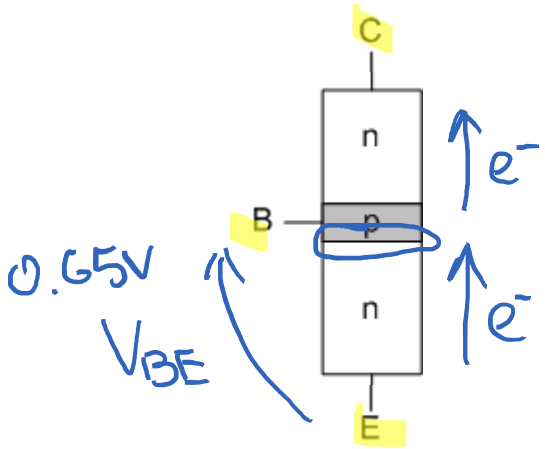
In an integrated circuit

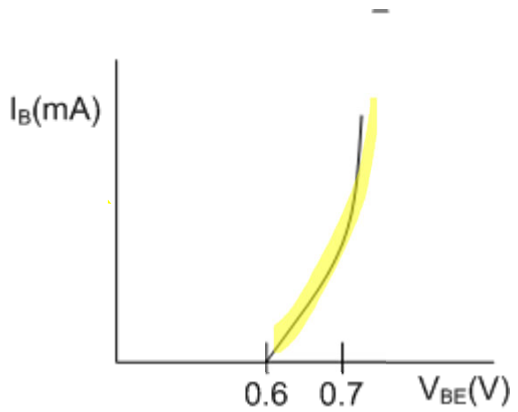
- The cost of a gate is proportional to the *chip area* occupied by the gate
- The gate area is roughly proportional to the *number and size of the transistors* and the *amount of wiring* connecting them
- Ignoring the wiring area, the gate area is roughly proportional to the *gate input count*
- So gate input count is a rough measure of gate cost

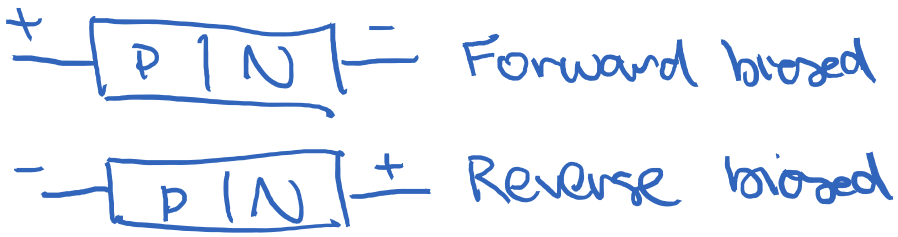
If the actual chip layout area occupied by the gate is known, it is a far more accurate measure

Bipolar transistor characteristics

Bipolar transistors may be npn or pnp type.
Typical bipolar IC transistors are the npn type.







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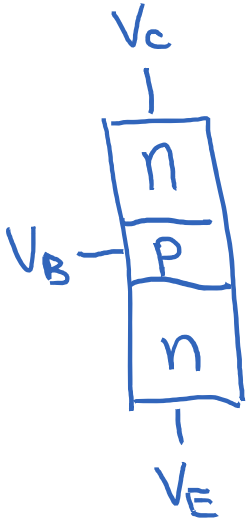
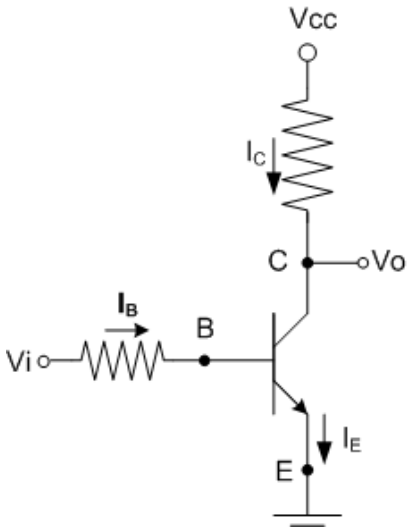
Bipolar transistor characteristics





$\beta = h_{fe} \sim 100$

	Region	V_{BE} (V)	V_{CE}(V)	Current	B-E	B-C	
OFF	Cutoff	<0.6	Open Circuit	$I_B=I_C=0$	RB	RB	$V_E > V_B < V_C$
Amp.	Active	0.6-0.7	>0.8	$I_C=h_{fe}I_b$	FB	RB	$V_E < V_B < V_C$
ON	Saturation	0.7-0.8	0.2	$I_B >= I_{CS}/h_{fe}$	FB	FB	$V_E < V_B > V_C$

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BJTs in digital logic

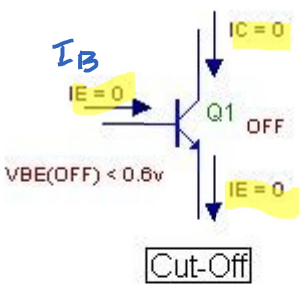
In digital circuits, BJTs are used as on/off switches

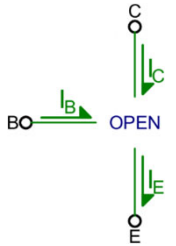
$I_E = I_C + I_B$

A BJT is off when in cutoff mode

$V_B < V_E$ and $V_B < V_c$

Both junctions are reverse biased and it behaves as an open circuit

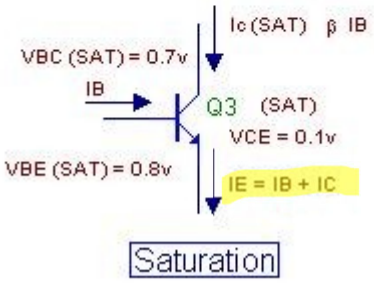


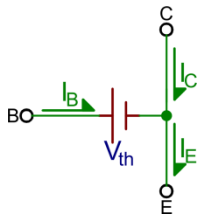


A BJT is on when in saturation

$V_B > V_E$ and $V_B > V_c$

Both junctions are forward biased and it behaves as a short circuit between the collector and emitter





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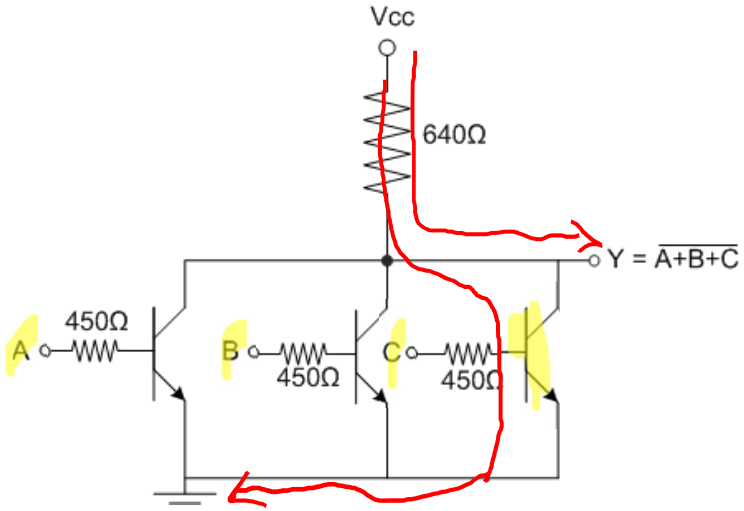
RTL circuits

The basic block in the RTL digital logic family is the NOR gate



A	B	C	Y
0	0	0	1
0	0	1	0
⋮	⋮	⋮	⋮
1	1	1	0

The noise margin for low signal input is 0.6-0.2 = 0.4 V

The fan-out of the RTL is limited by a high output voltage. Any voltage below 1V in the output may not drive the next transistor into saturation

Fan out, power dissipation, and propagation delay are 5, 12mW and 25ns respectively

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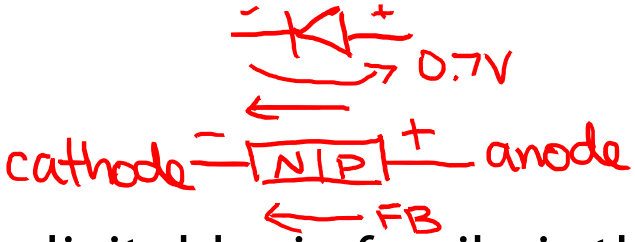
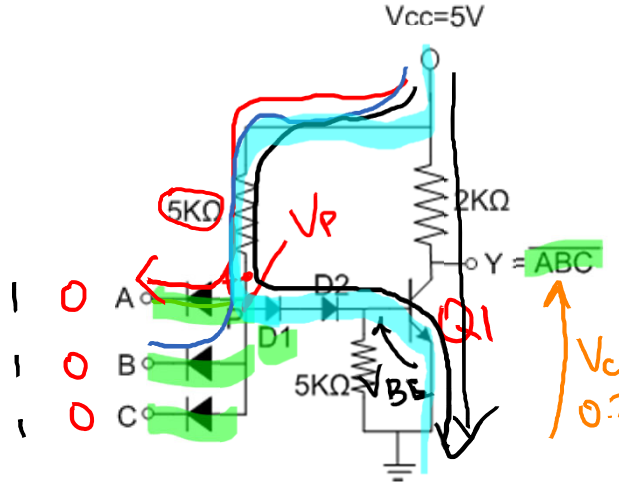
DTL circuits



The basic block in the DTL digital logic family is the NAND gate



A	B	C	Y	Vp	Q1
0	0	0	1	0.7V	OFF/OPEN
0	0	1	1	0.7V	OFF/OPEN
1	1	1	0	2.1V	ON/CLOSE

The two voltage levels are 0.2 V for low and 4-5V for high level

If any input of the gate is low at 0.2V, the corresponding input diode conducts current through Vcc and the 5-KΩ resistor into the input node

The potential at P will not be sufficient enough to forward drive the two diodes and Q1. Hence, Q1 will be switched off, sending Y to high

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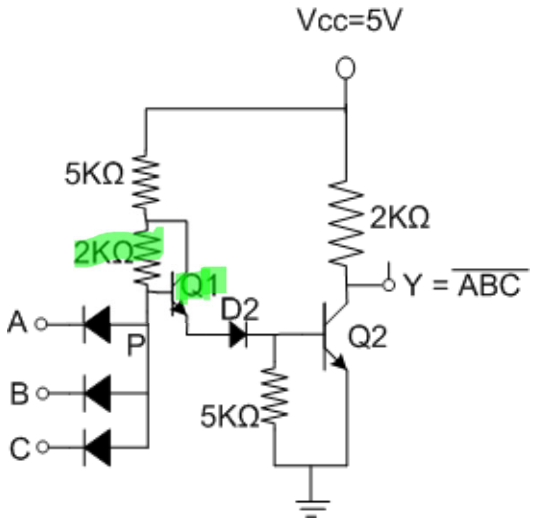
DTL circuits

When all inputs are high, D1, D2 and Q1 will be driven by V_{cc} through 5KΩ. With Q1 in saturation region, the output voltage Y will sit at 0.2V (low)

The power dissipation is about 12mW and the propagation delay averages 30ns

The noise margin is about 1V and the fan-out can go as high as 8

The fan-out is limited by the maximum current that flow in the collector of the saturated transistor but can be increased by replacing D1 with a transistor



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TTL circuits

The original basic transistor-transistor logic (TTL) gate was a slight improvement over DTL gate

TTL is now the most commonly used BJT based logic family in the design of digital systems

Currently, MOS and CMOS are the dominant technologies in VLSI circuits

The basic logic circuit of TTL digital logic family is NAND gate

There are several subfamilies or series of TTL technology

TTL circuits

TTL series name	Prefix	Fan-out	Power dissipation (mW)	Propagation delay	Speed-power product
Standard	74	10	10	9	90
Low Power	74L	20	1	33	33
High speed	74H	10	22	6	132
Schottky	74S	10	19	3	57
Low-power Schottky	74LS	20	2	9.5	19
Advanced Schottky	74AS	40	10	1.5	15
Advanced low-power schottky	74ALS	20	1	4	4
Fast	74F	20	4	3	12

TTL circuits

The standard TTL gate has been designed with different resistor values to produces gates with lower power dissipation or with higher speed

- In high speed TTL: reduce resistor to reduce propagation delay, but causes more power dissipation
- In low power TTL: increase resistor to reduce power dissipation, but causes longer propagation delay.

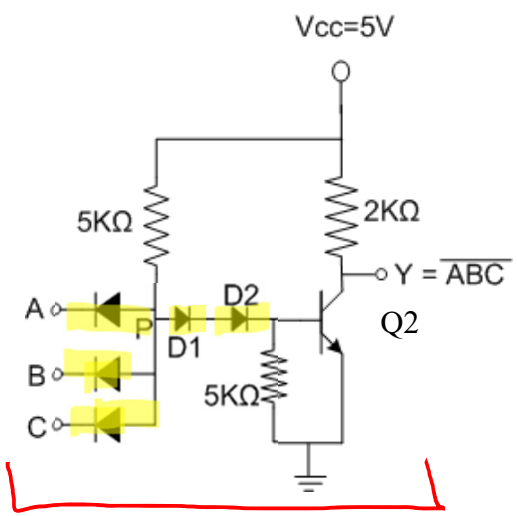
The schottky TTL increase speed of operation without an excessive increase in power dissipation

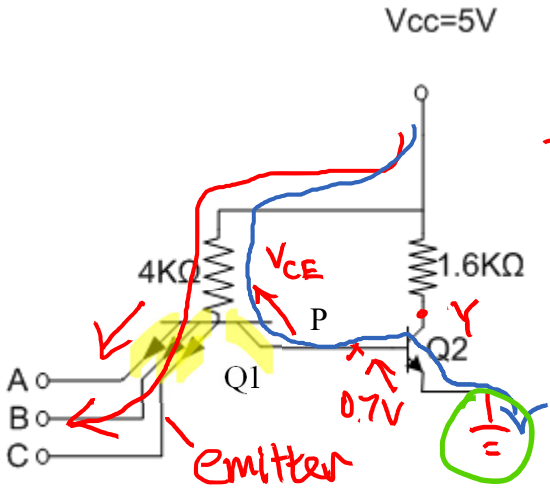
It removes the storage time delay by preventing the transistor from going into saturation.

TTL gates come in three different types of output configuration: Open- collector output, Totem-pole output and Three-state output

TTL circuits

In TTL, the diodes are replaced by a transistor





A B C	Y	BE Q1	Q2
0 0 0	1	FB	OFF
1 1 1	0	RB	ON
⋮			
0 0 1	0		
0 1 0	0	"	"
1 0 0	0		

When one or more low inputs are applied, current will flow out the emitter of Q1, the voltage at P will be V_{CE} = 0.2 V and Q2 will be off

When all inputs are high, current will flow out the collector and Q2 will turn on

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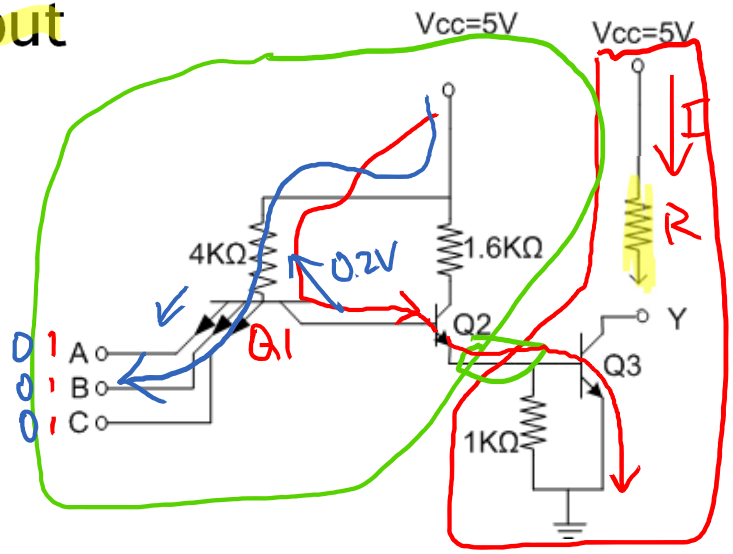
TTL circuits

Open-collector output

A B C	Q1	Q2	Q3	Y
1 1 1	OFF	ON	ON	L
0 0 0	ON	OFF	OFF	H
0 0 1	⋮	⋮	⋮	H
0 1 0	⋮	⋮	⋮	
1 0 0	⋮	⋮	⋮	



Three applications of open-collector gates: driving a lamp or relay, perform wired logic and constructing a common-bus system

The propagation delay is limited by the load resistance and capacitance

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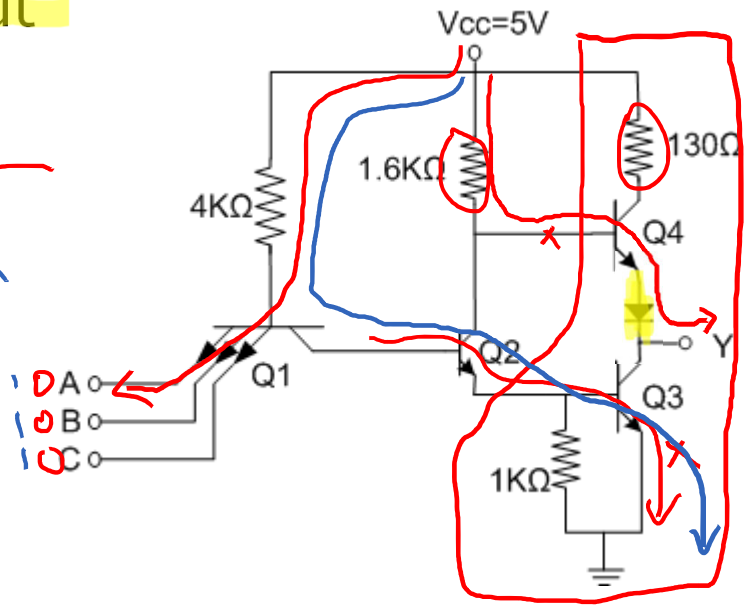
TTL circuits

Totem-Pole output

ABC	Q1	Q2	Q3	Q4	Y
000	ON	OFF	OFF	ON	H
111	OFF	ON	ON	ON	L



$V_E < V_B < V_C$ BE FB BC RB

5V - 0.7V

By replacing the passive pull-up resistor RL with active pull-up circuit, it is possible to reduce propagation by almost 4 fold

This comes at a price of higher power dissipation

The Schottky TTL gate can achieve higher speed at lower power dissipation

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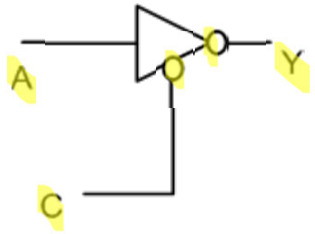
TTL circuits

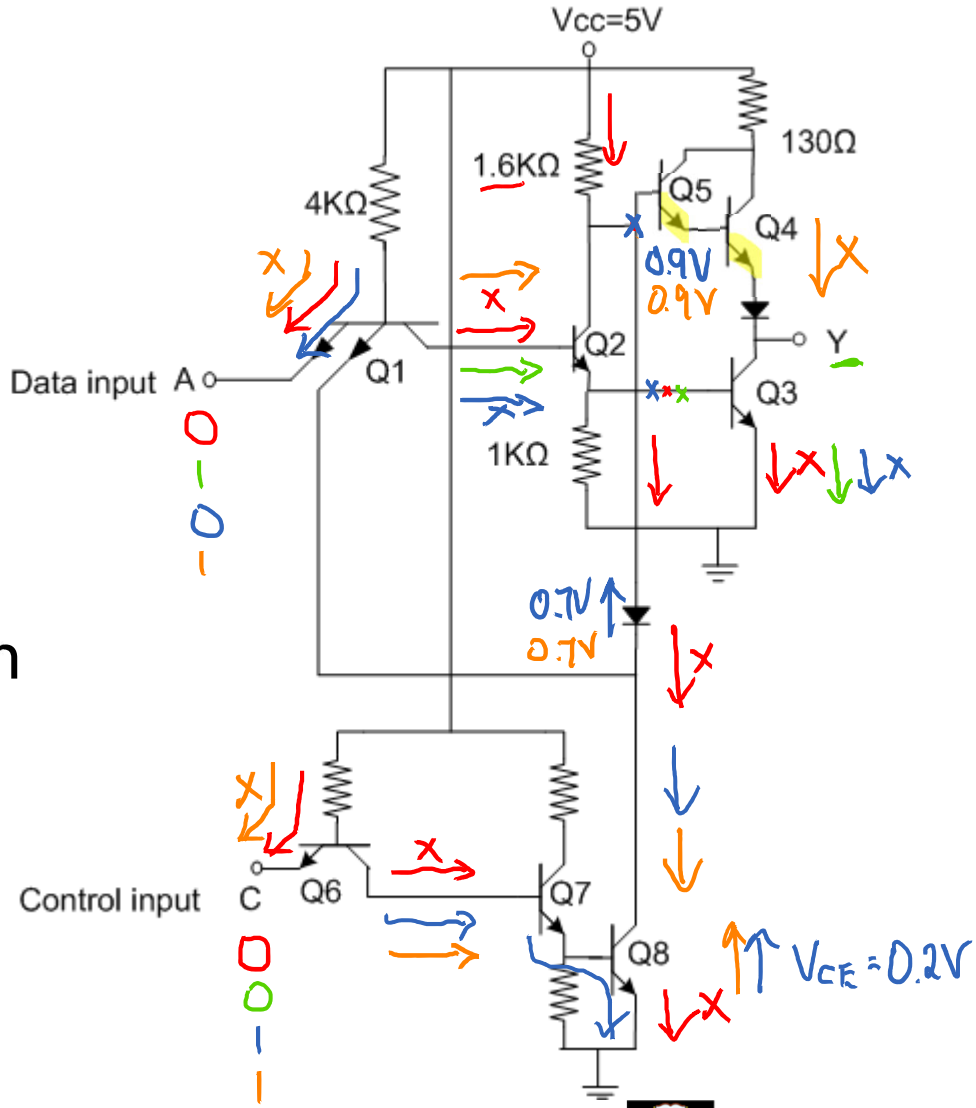
Three-state Gate



Y= $\bar{A}$ if C= low

Y high impedance if C = high

C	A	Y	Q7	Q8	Q2	Q3	Q4	Q5
0	0	1	OFF	OFF	OFF	OFF	ON	ON
0	1	0	OFF	OFF	ON	ON	ON	ON
1	0	Hi Z	ON	ON	OFF	OFF	OFF	OFF
1	1	Hi Z	ON	ON	ON	OFF	OFF	OFF



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ECL circuits

ECL (Emitter-coupled logic) is a non-saturated digital logic family

Since transistors do not saturate, it is possible to achieve propagation delays as low as 1-2ns

Its noise immunity and power dissipation are the worst of all in the logic families available

MOS transistors and CMOS logics

MOS: **M**etal **O**xide **S**emiconductor

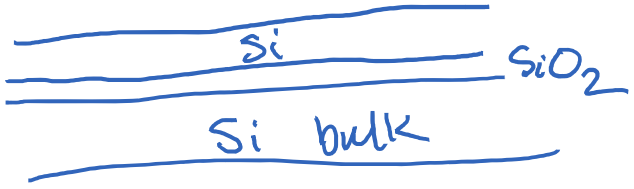
Unipolar transistor – field effect transistor (FET) uses electric field to control the flow of current. Three terminals: source, gate, and drain.

Two types of MOS - nMOS and pMOS.

CMOS: **C**omplementary **M**etal **O**xide **S**emiconductor.

CMOS technology dominates the market due to its high circuit density, high performance, and low power consumption. Often find in digital, analog, and mixed-signal ICs.

Fabricated on silicon or silicon-on-insulator (SOI) wafers.



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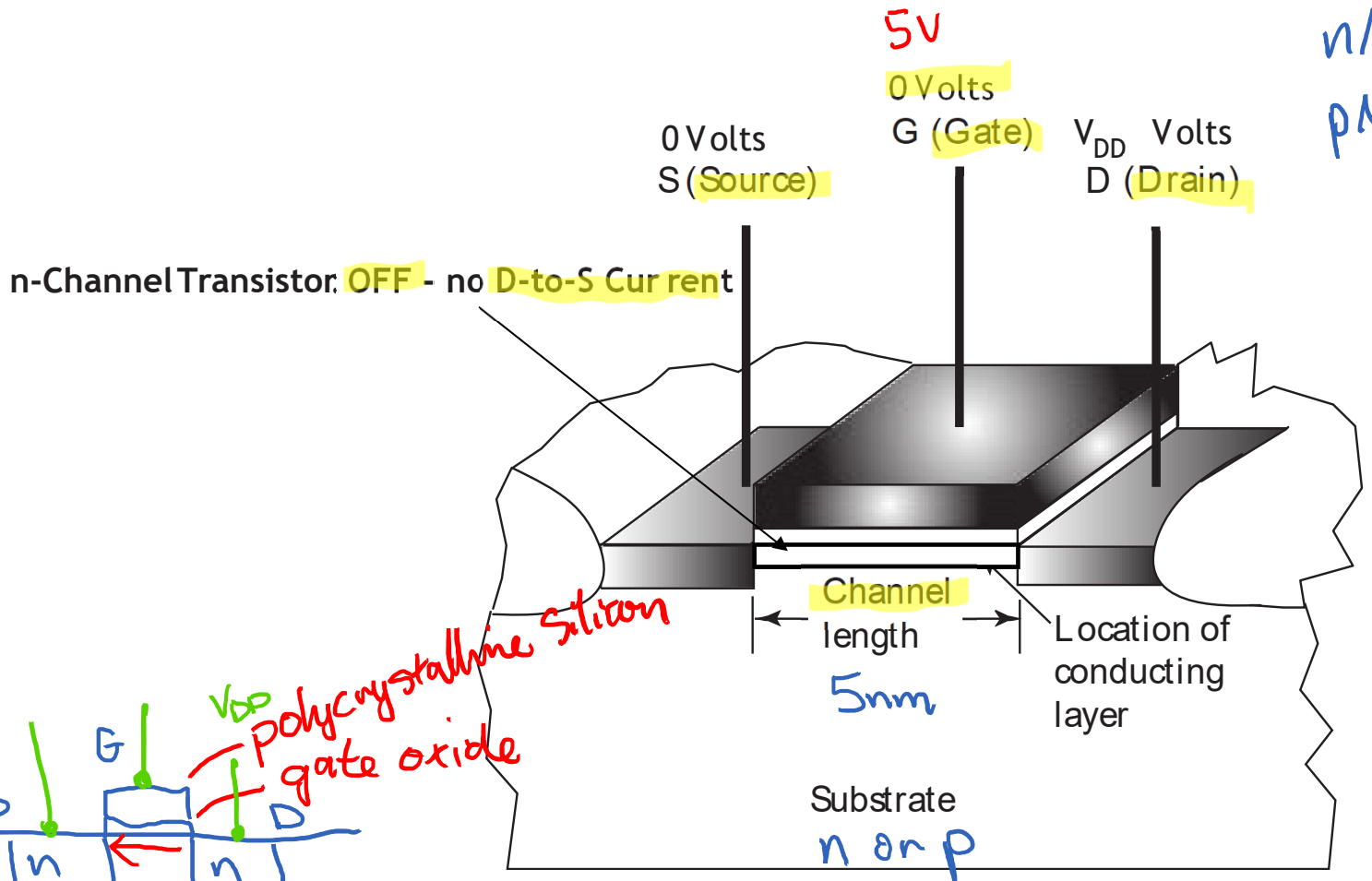
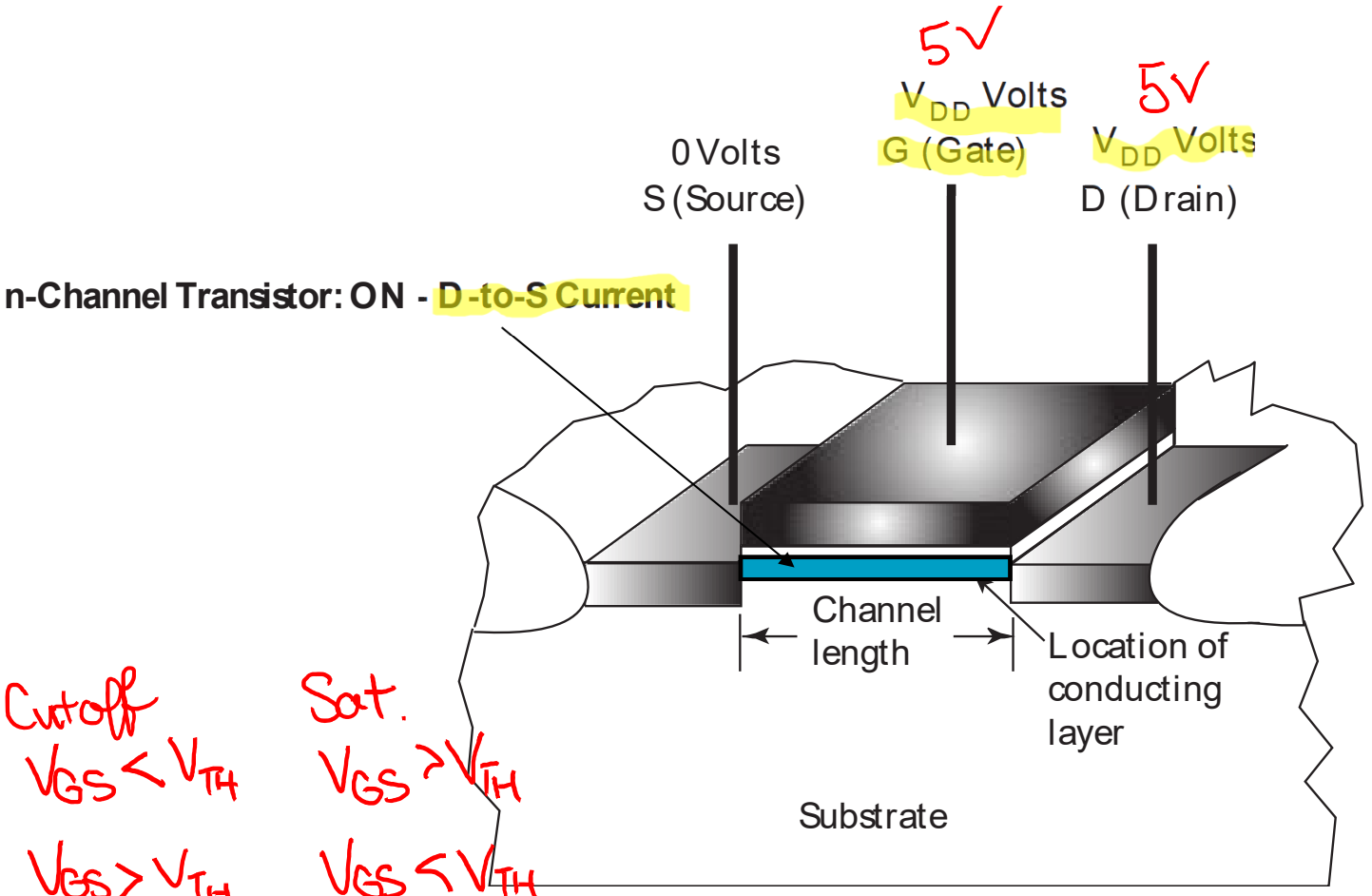
MOS transistor



UNSW SYDNEY

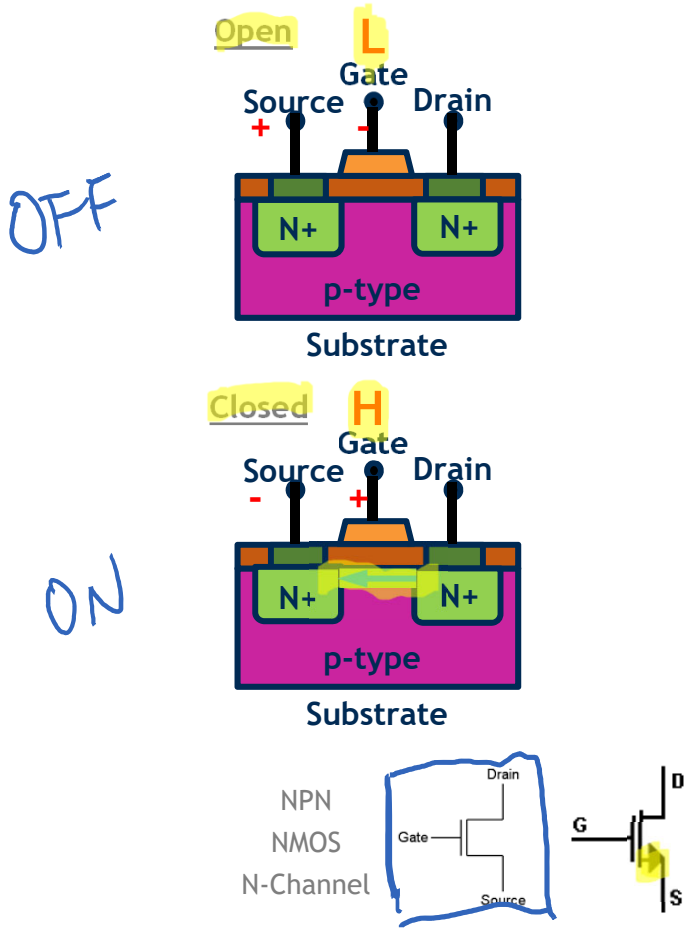
MOS transistor

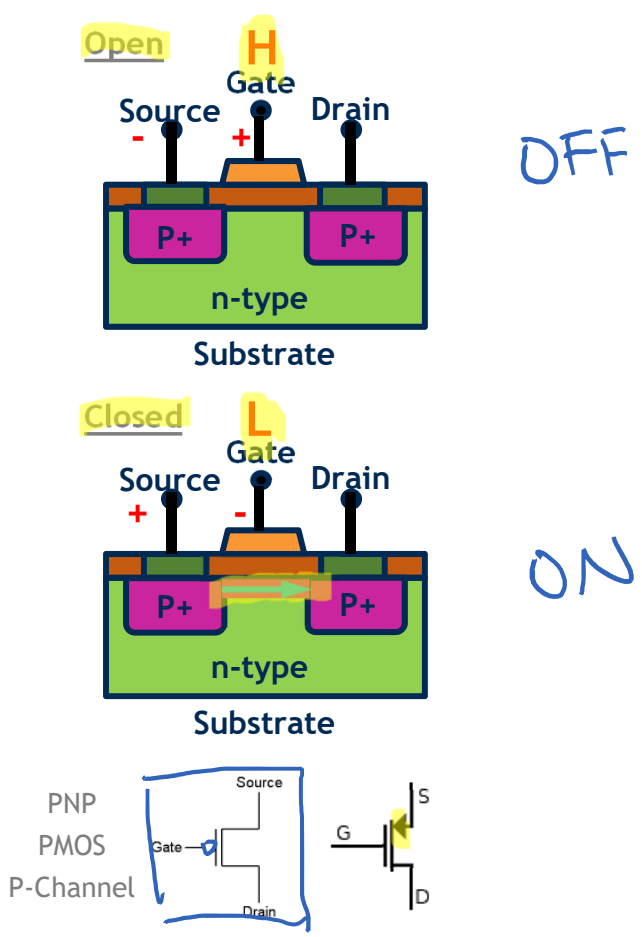


	Cutoff	Sat.
nMOS	$V_{GS} < V_{TH}$	$V_{GS} > V_{TH}$
pMOS	$V_{GS} > V_{TH}$	$V_{GS} < V_{TH}$

UNSW SYDNEY

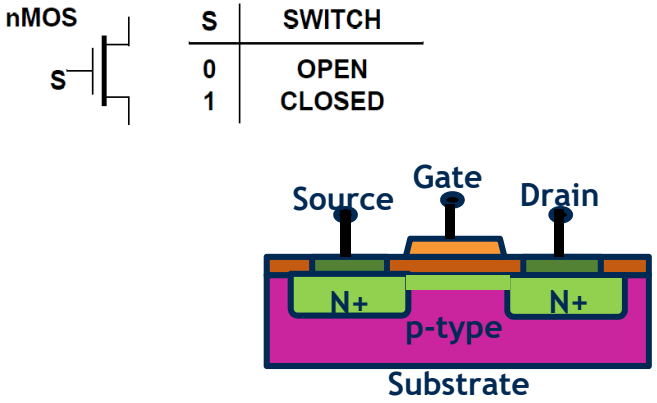
MOS symbol





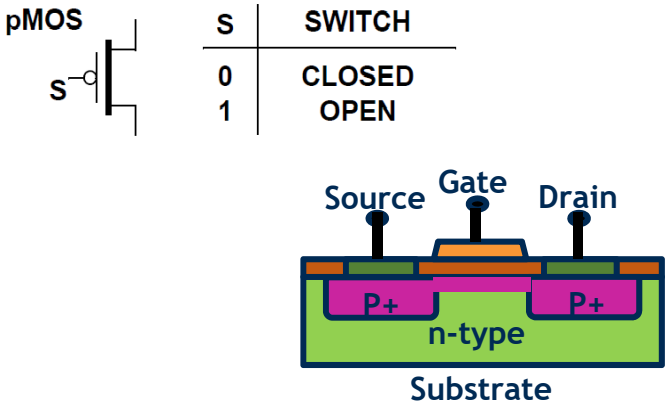
UNSW SYDNEY

MOS logic



nMOS when CLOSED

Transmits logic level 0 well
Transmits logic level 1 poorly



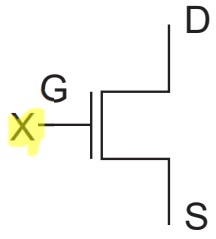
pMOS when CLOSED

Transmits logic level 1 well
Transmits logic level 0 poorly

UNSW SYDNEY

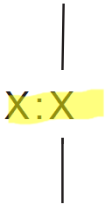
Switching model of MOS

n-Channel – Normally Open (NO) Switch Contact



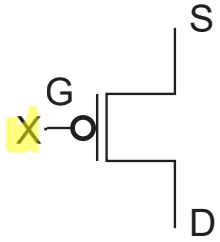
Symbol

Switch Model:



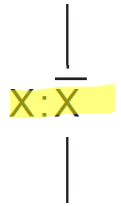
Simplifed
Switch Model

p-Channel – Normally Closed (NC) Switch Contact



Symbol

Switch Model

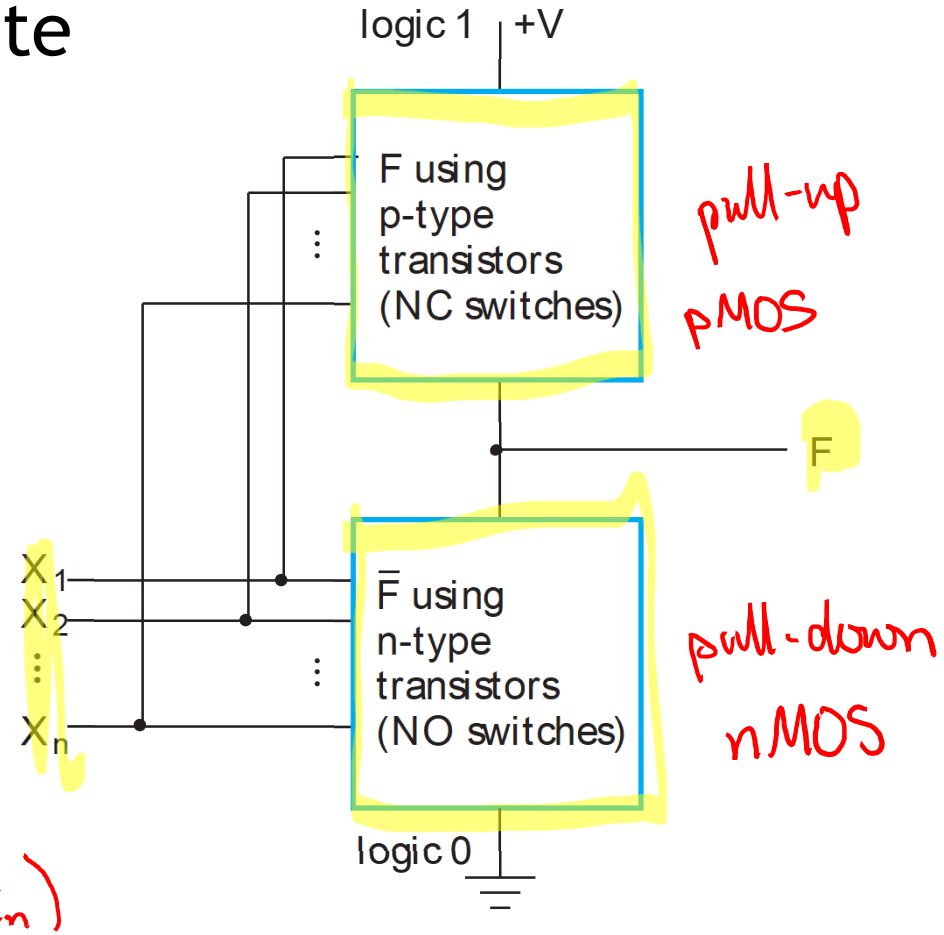


Simplified
Switch Model

UNSW SYDNEY

Fully complementary MOS (CMOS)

Circuit structure for fully-complementary (CMOS) gate

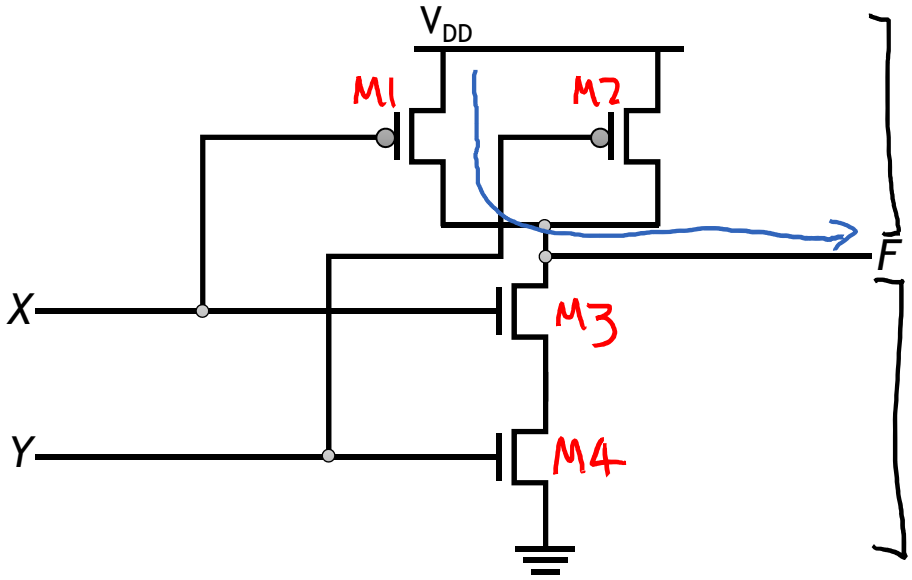


General Structure

$F = f(x_1 \cdots x_n)$

UNSW SYDNEY

CMOS NAND implementation



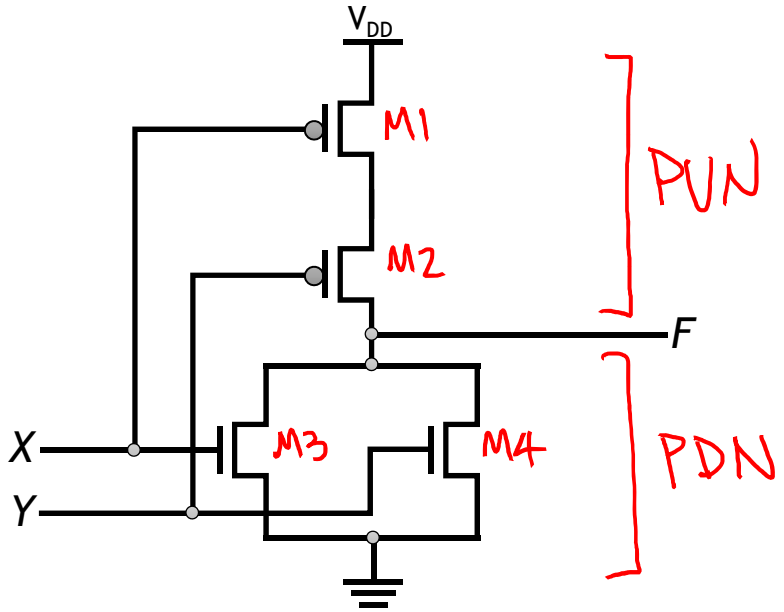
$F = \overline{XY} = \bar{X} + \bar{Y}$

$\bar{F} = XY$

X	Y	F	M1	M2	M3	M4
L	L	H	✓	✓	x	x
L	H	H	✓	x	x	✓
H	L	H	x	✓	✓	x
H	H	L	x	x	✓	✓

UNSW SYDNEY

CMOS NOR implementation

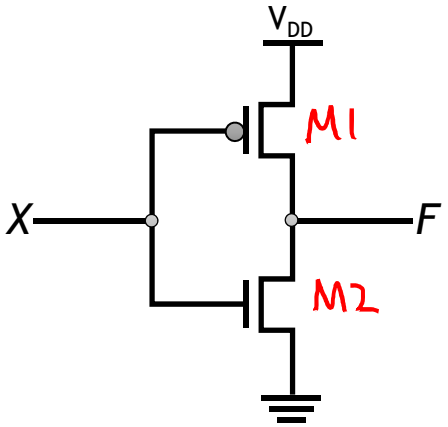


$F = \overline{X+Y} = \bar{X} \cdot \bar{Y}$

$\bar{F} = X+Y$

X	Y	F	M1	M2	M3	M4
L	L	H	✓	✓	x	x
L	H	L	✓	x	x	✓
H	L	L	x	✓	✓	x
H	H	L	x	x	✓	✓

CMOS NOT implementation



X	F	M1	M2
L	H	✓	✗
H	L	✗	✓

$F = \overline{X}$

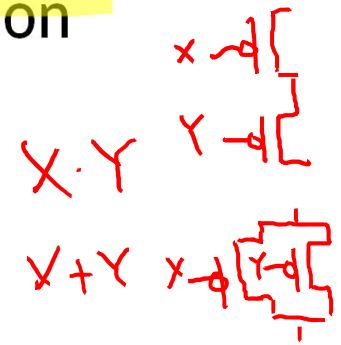
$\overline{F} = X$

UNSW SYDNEY

CMOS for any Boolean function

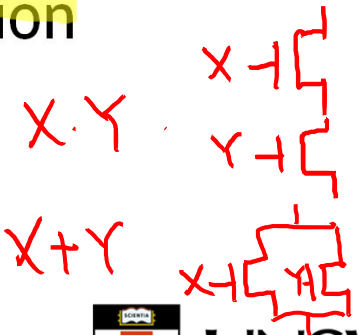
Pull-up section of switch network – using F

- Use complements for all literals in expression
- Use only pMOS devices
- Form series network for an AND operation
- Form parallel network for an OR operation



Pull-down section of switch network – using $\overline{F}$

- Use complements for all literals in expression
- Use only nMOS devices
- Form series network for an AND operation
- Form parallel network for an OR operation



UNSW SYDNEY

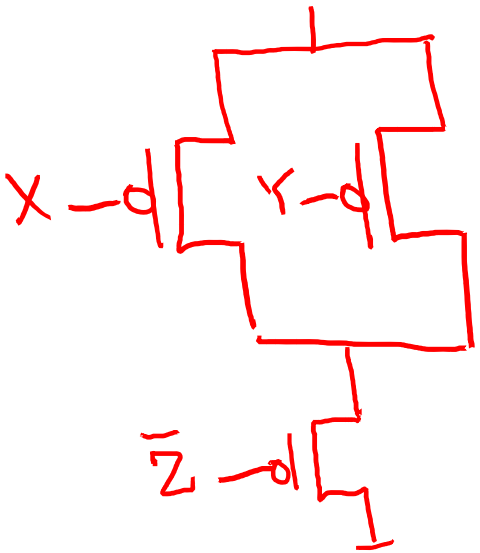
CMOS for any Boolean function

series AND parallel OR

Example: Find a CMOS gate with the following function

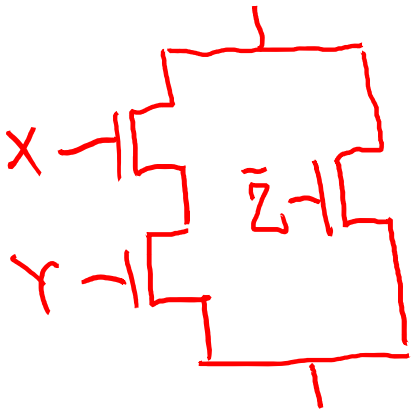
$$F = \bar{X}Z + \bar{Y}Z = (\bar{X} + \bar{Y})Z$$

PUN



PDN

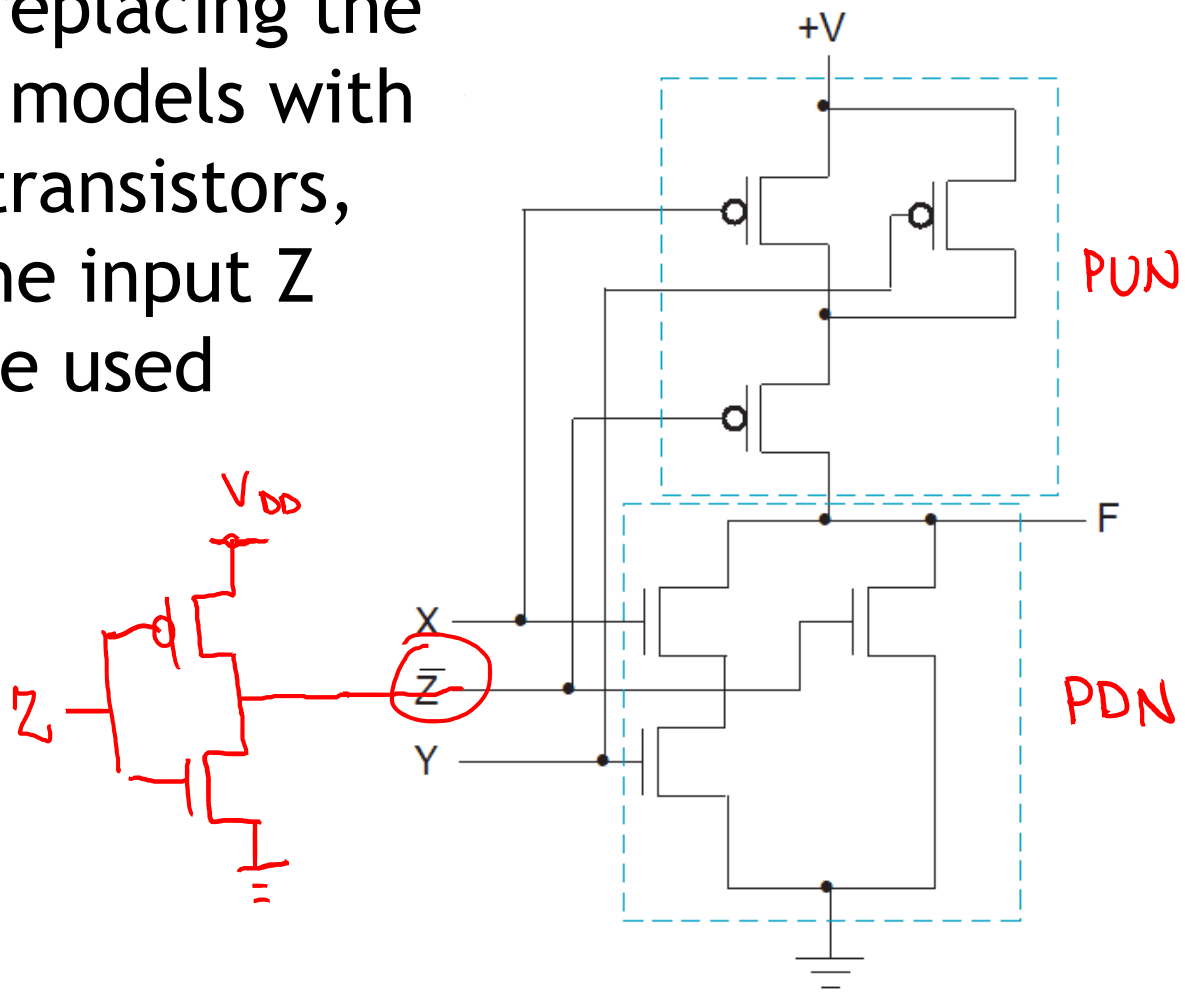
$\bar{F} = (X \cdot Y) + \bar{Z}$



UNSW SYDNEY

CMOS for any Boolean function

When replacing the switch models with CMOS transistors, note the input Z must be used



UNSW SYDNEY

CMOS for any Boolean function

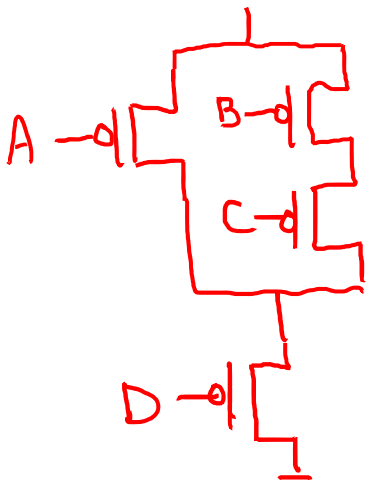
series - AND parallel - OR

Problem: implement the function in CMOS

$$F = \overline{D + A(B + C)}$$

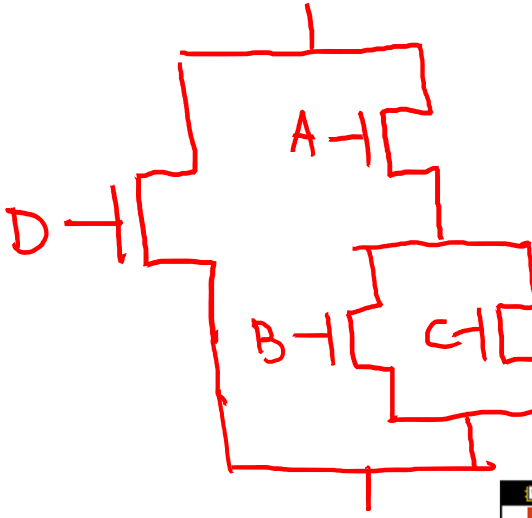
PUN

$F = \bar{D} \cdot (\bar{A} + \bar{B}\bar{C})$



PDN

$\bar{F} = D + A(B+C)$

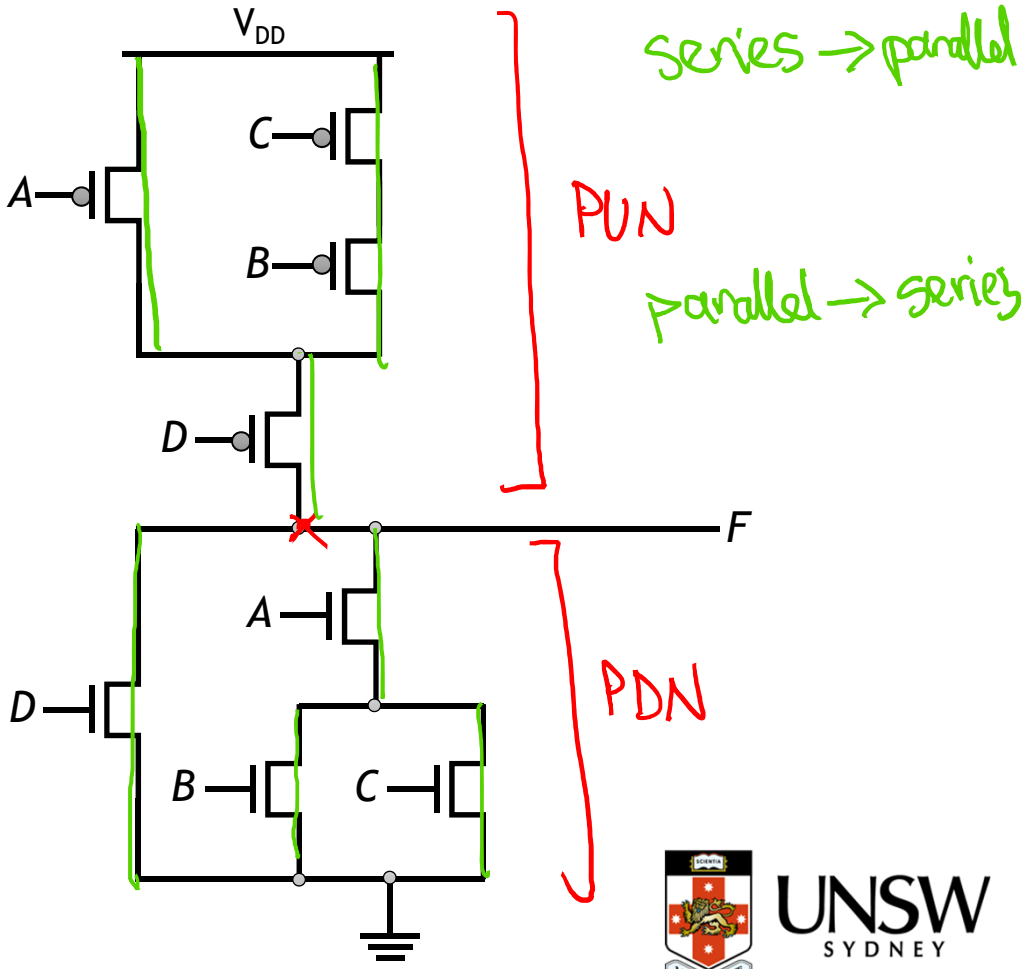


UNSW SYDNEY

CMOS for any Boolean function

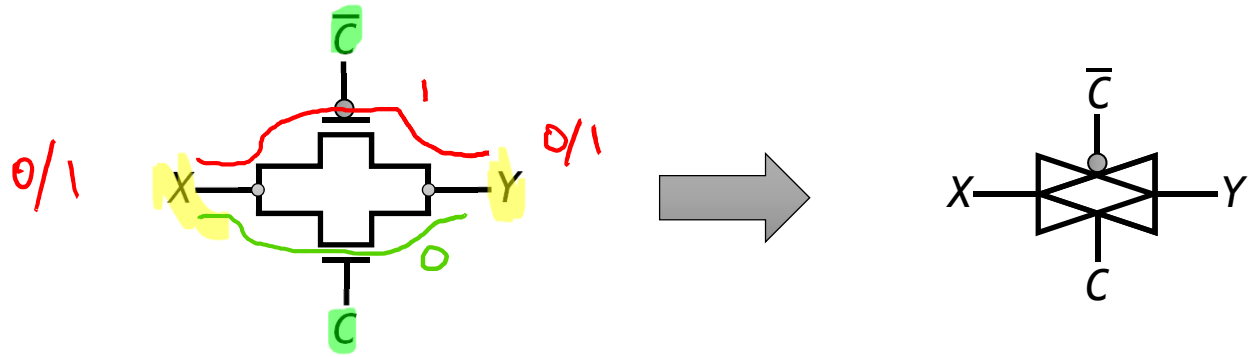
Example: implement the function in CMOS

$$F = \overline{D + A(B + C)}$$



Transmission gates

A *Transmission Gate* is constructed using one NMOS and one PMOS transistors:



nMOS pMOS

C = 1 ON ON

C = 0 OFF OFF

pMOS → 1 0 X

nMOS → 0 1 X

UNSW SYDNEY

Transmission gates

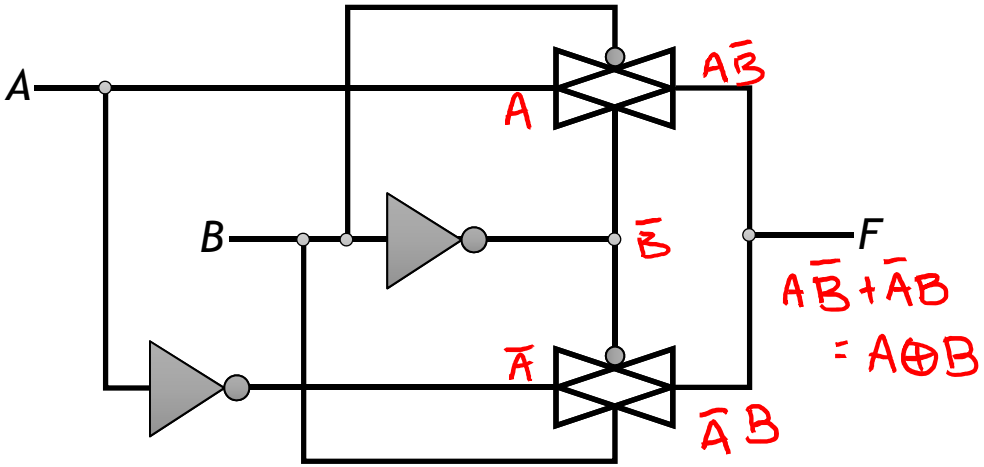
A transmission gate acts as an electronic switch

It is used to pass or block a signal between two points in the circuit

When $C = 1$ ($\overline{C} = 0$), one of the transistors will be on (depending on the value of X) and a path exists between X and Y

When $C = 0$ ($\overline{C} = 1$), both transistors will be off (regardless of the value of X) and no path exists between X and Y

CMOS XOR implementation



A	B	F
L	L	L
L	H	H
H	L	H
H	H	L

UNSW SYDNEY

CMOS logics transistor count

Logic gate	Transistor count
Buffer	4
NOT	2
NAND 2-input	4
NOR 2-input	4
AND 2-input	6
OR 2 input	6
XOR	6