Cycle	Instr. Retired	Reason
7	st r5, r1, 0	When the st instruction is at the Decode stage, it realizes that it is going to read r1 from a register that has not been loaded from memory yet, hence a nop is bubbled twice throughout the rest of the pipeline stages and the decode stage of st is done again.
7	NOP	Second stall cycle
11	st r6, r1, 1	When the st instruction is at the Decode stage, it realizes that it is going to read r1 from a register that has not been loaded from memory yet, hence a nop is bubbled twice throughout the rest of the pipeline stages and the decode stage of st is done again.
11	NOP	Second stall cycle
13	st r7, r1, 1	When the st instruction is at the Decode stage, it realizes that it is going to read r1 from a register that has not been loaded from memory yet, hence a nop is bubbled twice throughout the rest of the pipeline stages and the decode stage of st is done again.
13	NOP	Second stall cycle

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
lbi r0, 0	F	D	X	M	W															
lbi r5, 43		F	X	D	M	W														
lbi r6, 43			F	X	D	M	W													
lbi r7, 43				F	X	D	M	W												
ld r1, r0, 0					F	D	X	M	W											
st r5, r1, 0						F	D	NOP	NOP	NOP										
							NOP	NOP	NOP	NOP	NOP									
								F	D	X	M	W								
ld r1, r0, 2									F	D	X	M	W							
st r6, r1, 1										F	D	NOP	NOP	NOP						
											NOP	NOP	NOP	NOP	NOP					
ld r1, r0, 4												F	D	X	M	W				
st r7, r1, 1													F	D	NOP	NOP	NOP			
														NOP	NOP	NOP	NOP	NOP		
															F	D	X	M	W	
hal																F	D	X	M	W