Nevindu Medan Batagoda

CS/ECE552 Karu Sankaralingam

Project Plan

23rd February 2021

1. **Design Review (Due on 4th March 2021)**

Have a complete schematic of an unpipelined implementation of the WISC-SP13 implementation processor.

Schedule:

* 1. 28th February – Go through the related material in the book and get an idea of how to adapt the book design to the ISA of the WISC-SP13 processor.
  2. 30th February – Have an idea of which components come together and why. Start drawing the first drafts of the design.
  3. 2nd March – Have a final draft of the design ready well ahead of the hard deadline.
  4. 4th March – Hard deadline. Have the design submitted, and sign up for the 10-min design review meeting.

1. **Demo #1 – Unpipelined Design (Due on 23rd March 2021)**

Design a single-cycled non-pipelined WISC-SP13 processor.

Schedule:

1. 2nd March – Start working on HW 3; Use the register designed on the Homework in the Demo.
2. 9th March – Hand in HW3.
3. 20th March – Have a completed design which passes all the Simple test. Design own testbenches to further debug.
4. 21st March – Have final design ready.
5. 23rd March – Submit design.
6. **Demo #2 – Pipelined Design (Due on 13th April)**

Make a working pipelined version of our design. No optimizations necessary. This design will use the single-cycle perfect memory model as well.

Schedule:

* 1. 23rd March – Start working on HW4.
  2. 28th March –Have the instruction timeline document complete.
  3. 6th April – Submit HW4. Start work on HW5.
  4. 9th April -– Write additional test cases to debug the code.
  5. 11th April – Have a working design; continue testing.
  6. 13th April – Submit the design.

1. **Cache FSM (Due on 15th April)**

Schedule:

* 1. 13th April – Start designing the Cache FSM.
  2. 15th April – Submit the Cache FSM

1. **Cache Demo - Two-way Set-associative Cache (Due on 4th May)**

Design and test a cache to be used in the final design.

Schedule:

* 1. 15th April – Start working on HW6.
  2. 20th April – Have a comprehensive understanding of the inner workings of the Cache that needs to be designed for the project.
  3. 22nd April – Finish work on the direct-mapped cache.
  4. 28th April – Have a working design of the two-way set associative cache and start testing.
  5. 30th April – Synthesize the set associative cache.
  6. 1st May – Continue debugging your design.
  7. 4th May – Submit the design.