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CS 552: Design Review Document

**Schematic**

Diagram, schematic

Description automatically generated

**Control Signal Table**

Instructions completed: <list all of the instructions that are filled out>

Create a table for the control signals of all instructions. Each value should be either 0 or 1, but add an asterisk (\*) if either could work (i.e. the control signal doesn’t have an impact on the outcome of the instruction’s execution).

All instructions are listed here: <http://pages.cs.wisc.edu/~karu/courses/cs552/spring2021/wiki/index.php/Main/ISASpecification>

An example would be:

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction Name | Instruction Format | ALUOp | RegDst | Branch | Zero | ALUSrc | PCSrc | MemWrite | MemRead | MemToReg |
| BEQZ | BEQZ Rs, Signed Im | 0\* | 0\* | 1 | 1 | 0\* | 1 | 0\* | 0\* | 0\* |
| BNEQZ | BNEQZ Rs, Signed Im | 0\* | 0\* | 1 | 0 | 0\* | 0 | 0\* | 0\* | 0\* |
| LD | LD Rd, Rs, immediate |  |  |  |  |  |  |  |  |  |