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| --- | --- | --- |
| Cycle | Instr. Retired | Reason |
| 7 | st r5, r1, 0 | When the st instruction is at the  Decode stage, it realizes that it is going to read r1 from a register that has not been loaded from memory yet, hence a nop is bubbled twice throughout the rest of the pipeline stages and the decode stage of st is done again. |
| 7 | NOP | Second stall cycle |
| 11 | st r6, r1, 1 | When the st instruction is at the  Decode stage, it realizes that it is going to read r1 from a register that has not been loaded from memory yet, hence a nop is bubbled twice throughout the rest of the pipeline stages and the decode stage of st is done again. |
| 11 | NOP | Second stall cycle |
| 13 | st r7, r1, 1 | When the st instruction is at the  Decode stage, it realizes that it is going to read r1 from a register that has not been loaded from memory yet, hence a nop is bubbled twice throughout the rest of the pipeline stages and the decode stage of st is done again. |
| 13 | NOP | Second stall cycle |

Chart, scatter chart

Description automatically generated