

SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

- Choice of Eight Latches or Eight D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Clock-Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce DC Loading on Data Lines ('S373 and 'S374)

description

These 8-bit registers feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The high-impedance 3-state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pullup components. These devices are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches, meaning that while the enable (C or CLK) input is high, the Q outputs follow the data (D) inputs. When C or CLK is taken low, the output is latched at the level of the data that was set up.

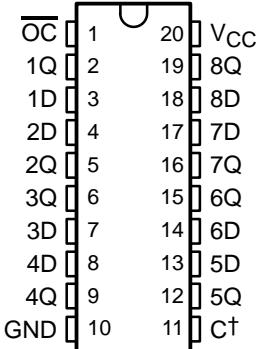
The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output-control (\overline{OC}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

\overline{OC} does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered, even while the outputs are off.

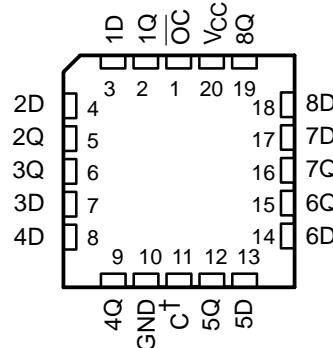
SN54LS373, SN54LS374, SN54S373,
SN54S374 . . . J OR W PACKAGE
SN74LS373, SN74S374 . . . DW, N, OR NS PACKAGE
SN74LS374 . . . DB, DW, N, OR NS PACKAGE
SN74S373 . . . DW OR N PACKAGE

(TOP VIEW)



[†]C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

SN54LS373, SN54LS374, SN54S373,
SN54S374 . . . FK PACKAGE
(TOP VIEW)



[†]C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LS373, SN54LS374, SN54S373, SN54S374,

SN74LS373, SN74LS374, SN74S373, SN74S374

OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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ORDERING INFORMATION

| T _A | PACKAGE [†] | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|-----------------------|------------------|
| 0°C to 70°C | PDIP – N | Tube | SN74LS373N |
| | | Tube | SN74LS374N |
| | | Tube | SN74S373N |
| | | Tube | SN74S374N |
| | SOIC – DW | Tube | SN74LS373DW |
| | | Tape and reel | SN74LS373DWR |
| | | Tube | SN74LS374DW |
| | | Tape and reel | SN74LS374DWR |
| | SOP – NS | Tube | SN74S373DW |
| | | Tape and reel | SN74S373DWR |
| | | Tube | SN74S374DW |
| | | Tape and reel | SN74S374DWR |
| | SSOP – DB | Tape and reel | SN74LS373NSR |
| | | Tape and reel | 74LS373 |
| | | Tape and reel | 74LS374 |
| -55°C to 125°C | CDIP – J | Tube | SN54LS373J |
| | | Tube | SNJ54LS373J |
| | | Tube | SN54LS374J |
| | | Tube | SNJ54LS374J |
| | | Tube | SN54S373J |
| | | Tube | SNJ54S373J |
| | | Tube | SN54S374J |
| | | Tube | SNJ54S374J |
| | CFP – W | Tube | SNJ54LS373W |
| | | Tube | SNJ54LS374W |
| | | Tube | SNJ54S374W |
| | LCCC – FK | Tube | SNJ54LS373FK |
| | | Tube | SNJ54LS374FK |
| | | Tube | SNJ54S373FK |
| | | Tube | SNJ54S374FK |

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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Function Tables

**'LS373, 'S373
(each latch)**

| INPUTS | | | OUTPUT |
|-----------------|---|---|--------|
| \overline{OC} | C | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

**'LS374, 'S374
(each latch)**

| INPUTS | | | OUTPUT |
|-----------------|------------|---|--------|
| \overline{OC} | CLK | D | Q |
| L | \uparrow | H | H |
| L | \uparrow | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

SN54LS373, SN54LS374, SN54S373, SN54S374,

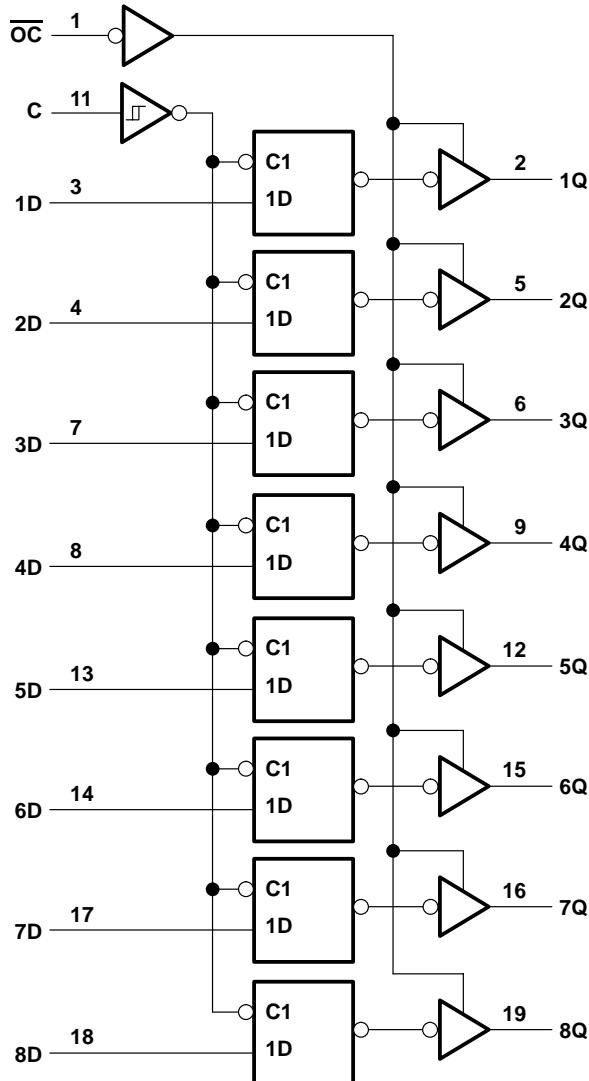
SN74LS373, SN74LS374, SN74S373, SN74S374

OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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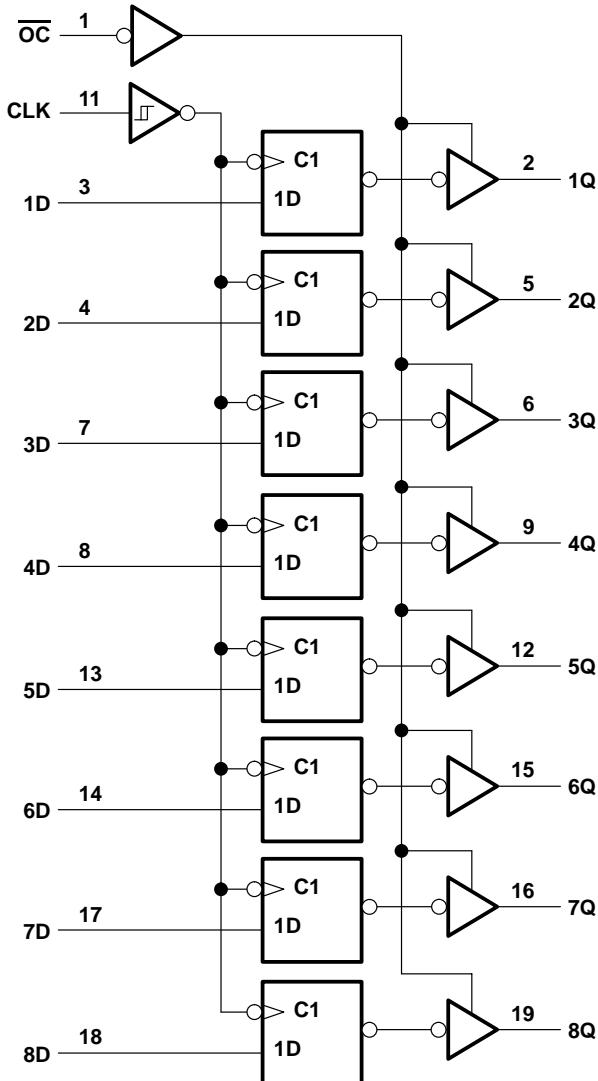
logic diagrams (positive logic)

'LS373, 'S373
Transparent Latches



□ for 'S373 Only

'LS374, 'S374
Positive-Edge-Triggered Flip-Flops



□ for 'S374 Only

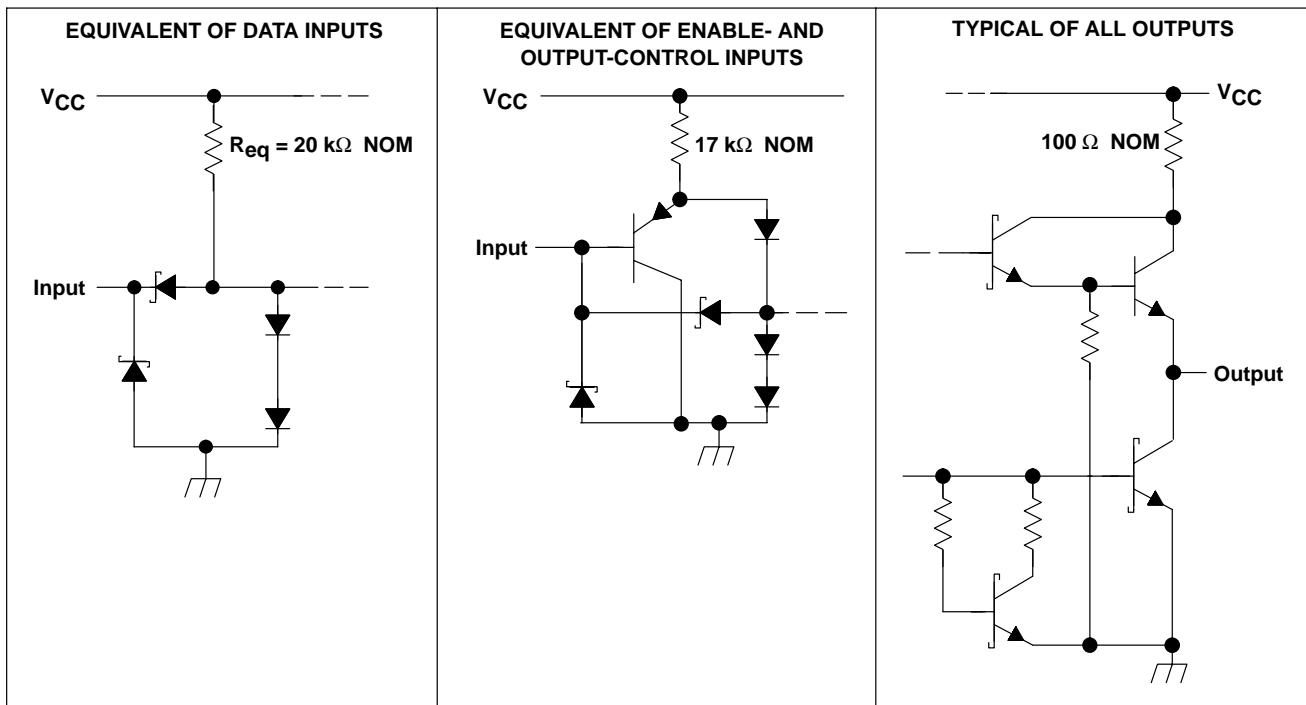
Pin numbers shown are for DB, DW, J, N, NS, and W packages.

**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

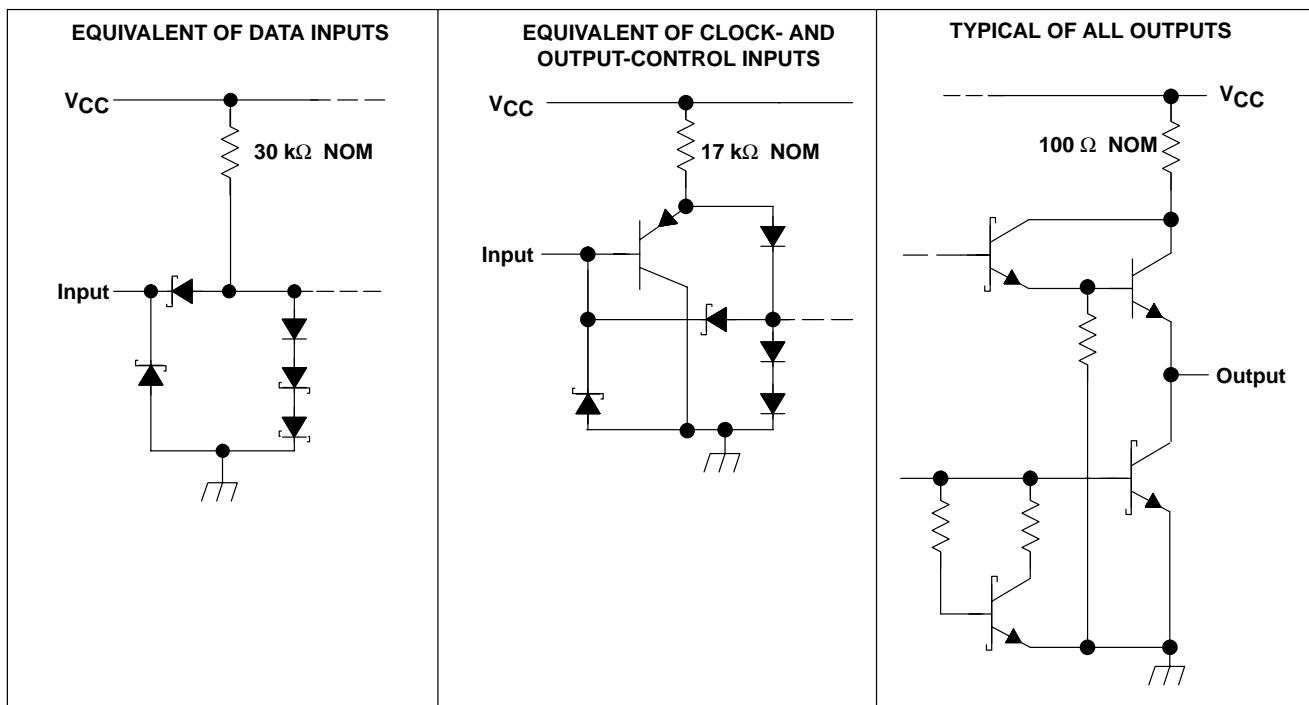
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schematic of inputs and outputs

'LS373



'LS374



SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374

**SN74LS373, SN74LS374, SN74S373, SN74S374
SEVEN-SEGMENT TRANSPARENT LATCHES AND**

OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†
(‘LS devices)

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

| | | | SN54LS' | | | SN74LS' | | | UNIT |
|-----------------|--------------------------------|----------|---------|-----|-----|---------|-----|------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | | 4.5 | 5 | 5 | 4.75 | 5 | 5.25 | V |
| V _{OH} | High-level output voltage | | | | 5.5 | | | 5.5 | V |
| I _{OH} | High-level output current | | | | -1 | | | -2.6 | mA |
| I _{OL} | Low-level output current | | | | 12 | | | 24 | mA |
| t _w | Pulse duration | CLK high | | | 15 | | | 15 | ns |
| | | CLK low | | | 15 | | | 15 | |
| t _{su} | Data setup time | 'LS373 | | | 5↓ | | | 5↓ | ns |
| | | 'LS374 | | | 20↑ | | | 20↑ | |
| t _h | Data hold time | 'LS373 | | | 20↓ | | | 20↓ | ns |
| | | 'LS374‡ | | | 5↑ | | | 0↑ | |
| T _A | Operating free-air temperature | | -55 | | 125 | 0 | | 70 | °C |

[‡]The t_h specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns (commercial only).

**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS [†] | SN54LS' | | | SN74LS' | | | UNIT |
|------------------|--|--|-------------------------|----------|----------|------------------|------|------|
| | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | |
| V _{IH} | High-level input voltage | | | 2 | | | 2 | V |
| V _{IL} | Low-level input voltage | | | | 0.7 | | 0.8 | V |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = -18 mA | | | -1.5 | | -1.5 | V |
| V _{OH} | High-level output voltage | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX | | 2.4 3.4 | | 2.4 3.1 | | V |
| V _{OL} | Low-level output voltage | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max | I _{OL} = 12 mA | 0.25 0.4 | | 0.25 0.4 | | V |
| | | | I _{OL} = 24 mA | | | 0.35 0.5 | | |
| I _{OZH} | Off-state output current, high-level voltage applied | V _{CC} = MAX, V _O = 2.7 V | | | 20 | | 20 | μA |
| I _{OZL} | Off-state output current, low-level voltage applied | V _{CC} = MAX, V _O = 0.4 V | | | -20 | | -20 | μA |
| I _I | Input current at maximum input voltage | V _{CC} = MAX, V _I = 7 V | | | 0.1 | | 0.1 | mA |
| I _{IH} | High-level input current | V _{CC} = MAX, V _I = 2.7 V | | | 20 | | 20 | μA |
| I _{IL} | Low-level input current | V _{CC} = MAX, V _I = 0.4 V | | | -0.4 | | -0.4 | mA |
| I _{OS} | Short-circuit output current [§] | V _{CC} = MAX | | -30 -130 | -30 -130 | | | mA |
| I _{CC} | Supply current | V _{CC} = MAX, Output control at 4.5 V | 'LS373 | 24 40 | | 24 40 | | mA |
| | | | 'LS374 | 27 40 | | 27 40 | | |

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'LS373 | | | 'LS374 | | | UNIT |
|------------------|-----------------|-------------|--|--------|-----|-----|--------|-----|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| f _{max} | | | R _L = 667 Ω, C _L = 45 pF, See Note 3 | | | | 35 | 50 | | MHz |
| t _{PLH} | Data | Any Q | R _L = 667 Ω, C _L = 45 pF, See Note 3 | 12 | 18 | | | | | ns |
| t _{PHL} | | | | 12 | 18 | | | | | |
| t _{PLH} | C or CLK | Any Q | R _L = 667 Ω, C _L = 45 pF, See Note 3 | 20 | 30 | | 15 | 28 | | ns |
| t _{PHL} | | | | 18 | 30 | | 19 | 28 | | |
| t _{PZH} | \overline{OC} | Any Q | R _L = 667 Ω, C _L = 45 pF, See Note 3 | 15 | 28 | | 20 | 26 | | ns |
| t _{PZL} | | | | 25 | 36 | | 21 | 28 | | |
| t _{PHZ} | \overline{OC} | Any Q | R _L = 667 Ω, C _L = 5 pF | 15 | 25 | | 15 | 28 | | ns |
| t _{PLZ} | | | | 12 | 20 | | 12 | 20 | | |

NOTE 3: Maximum clock frequency is tested with all outputs loaded.

f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level



SN54LS373, SN54LS374, SN54S373, SN54S374,

SN74LS373, SN74LS374, SN74S373, SN74S374

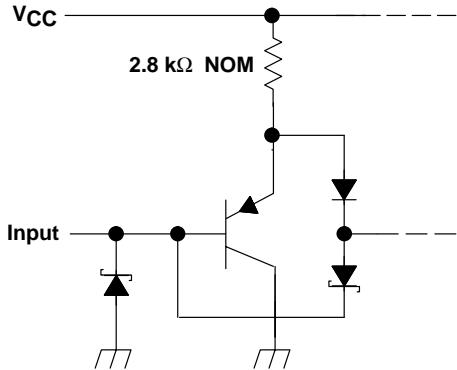
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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schematic of inputs and outputs

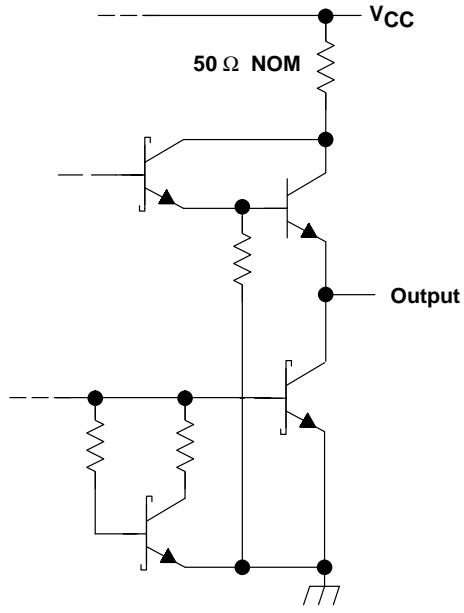
'S373 and 'S374

EQUIVALENT OF EACH INPUT



'S373 and 'S374

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†
(‘S devices)

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions

| | | | SN54S' | | | SN74S' | | | UNIT |
|-----------------|--------------------------------|-------|--------|-----|-----|--------|-----|------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{OH} | High-level output voltage | | | | 5.5 | | | 5.5 | V |
| I _{OH} | High-level output current | | | | -2 | | | -6.5 | mA |
| t _w | Pulse duration, clock/enable | High | | 6 | | 6 | | | ns |
| | | Low | | 7.3 | | 7.3 | | | |
| t _{su} | Data setup time | 'S373 | | 0↓ | | 0↓ | | | ns |
| | | 'S374 | | 5↑ | | 5↑ | | | |
| t _h | Data hold time | 'S373 | | 10↓ | | 10↓ | | | ns |
| | | 'S374 | | 2↑ | | 2↑ | | | |
| T _A | Operating free-air temperature | | -55 | | 125 | 0 | | 70 | °C |

SN54LS373, SN54LS374, SN54S373, SN54S374,

SN74LS373, SN74LS374, SN74S373, SN74S374

OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (SN54S373, SN54S374, SN74S373, SN74S374)

| PARAMETER | | TEST CONDITIONS† | | | | MIN | TYP‡ | MAX | UNIT | |
|------------|-----------------------|--|---|--|--|------|------|-----|---------------|--|
| V_{IH} | | | | | | 2 | | | V | |
| V_{IL} | | | | | | 0.8 | | | V | |
| V_{IK} | | $V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$ | | | | -1.2 | | | V | |
| V_{OH} | SN54S' SN74S' | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = \text{MAX}$ | | | | 2.4 | 3.4 | | V | |
| | | | | | | 2.4 | 3.1 | | | |
| V_{OL} | | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 20 \text{ mA}$ | | | | 0.5 | | | V | |
| I_{OZH} | | $V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_O = 2.4 \text{ V}$ | | | | 50 | | | μA | |
| I_{OZL} | | $V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_O = 0.5 \text{ V}$ | | | | -50 | | | μA | |
| I_I | | $V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$ | | | | 1 | | | mA | |
| I_{IH} | | $V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$ | | | | 50 | | | μA | |
| I_{IL} | | $V_{CC} = \text{MAX}$, $V_I = 0.5 \text{ V}$ | | | | -250 | | | μA | |
| $I_{OS}^§$ | | $V_{CC} = \text{MAX}$ | | | | -40 | -100 | | mA | |
| I_{CC} | $V_{CC} = \text{MAX}$ | 'S373 | Outputs high | | | 160 | | | mA | |
| | | | Outputs low | | | 160 | | | | |
| | | | Outputs disabled | | | 190 | | | | |
| | | 'S374 | Outputs high | | | 110 | | | | |
| | | | Outputs low | | | 140 | | | | |
| | | | Outputs disabled | | | 160 | | | | |
| | | | CLK and \overline{OC} at 4 V, D inputs at 0 V | | | 180 | | | | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'S373 | | | 'S374 | | | UNIT |
|-----------|-----------------|----------------|--|-------|-----|-----|-------|-----|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| f_{max} | | | $R_L = 280 \Omega$, $C_L = 15 \text{ pF}$, See Note 3 | | | | 75 | 100 | | MHz |
| t_{PLH} | Data | Any Q | $R_L = 280 \Omega$, $C_L = 15 \text{ pF}$, See Note 3 | 7 | 12 | | | | | ns |
| t_{PHL} | | | | 7 | 12 | | | | | |
| t_{PLH} | C or CLK | Any Q | $R_L = 280 \Omega$, $C_L = 15 \text{ pF}$, See Note 3 | 7 | 14 | | 8 | 15 | | ns |
| t_{PHL} | | | | 12 | 18 | | 11 | 17 | | |
| t_{PZH} | \overline{OC} | Any Q | $R_L = 280 \Omega$, $C_L = 15 \text{ pF}$, See Note 3 | 8 | 15 | | 8 | 15 | | ns |
| t_{PZL} | | | | 11 | 18 | | 11 | 18 | | |
| t_{PHZ} | \overline{OC} | Any Q | $R_L = 280 \Omega$, $C_L = 5 \text{ pF}$ | 6 | 9 | | 5 | 9 | | ns |
| t_{PLZ} | | | | 8 | 12 | | 7 | 12 | | |

NOTE 3. Maximum clock frequency is tested with all outputs loaded.

f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

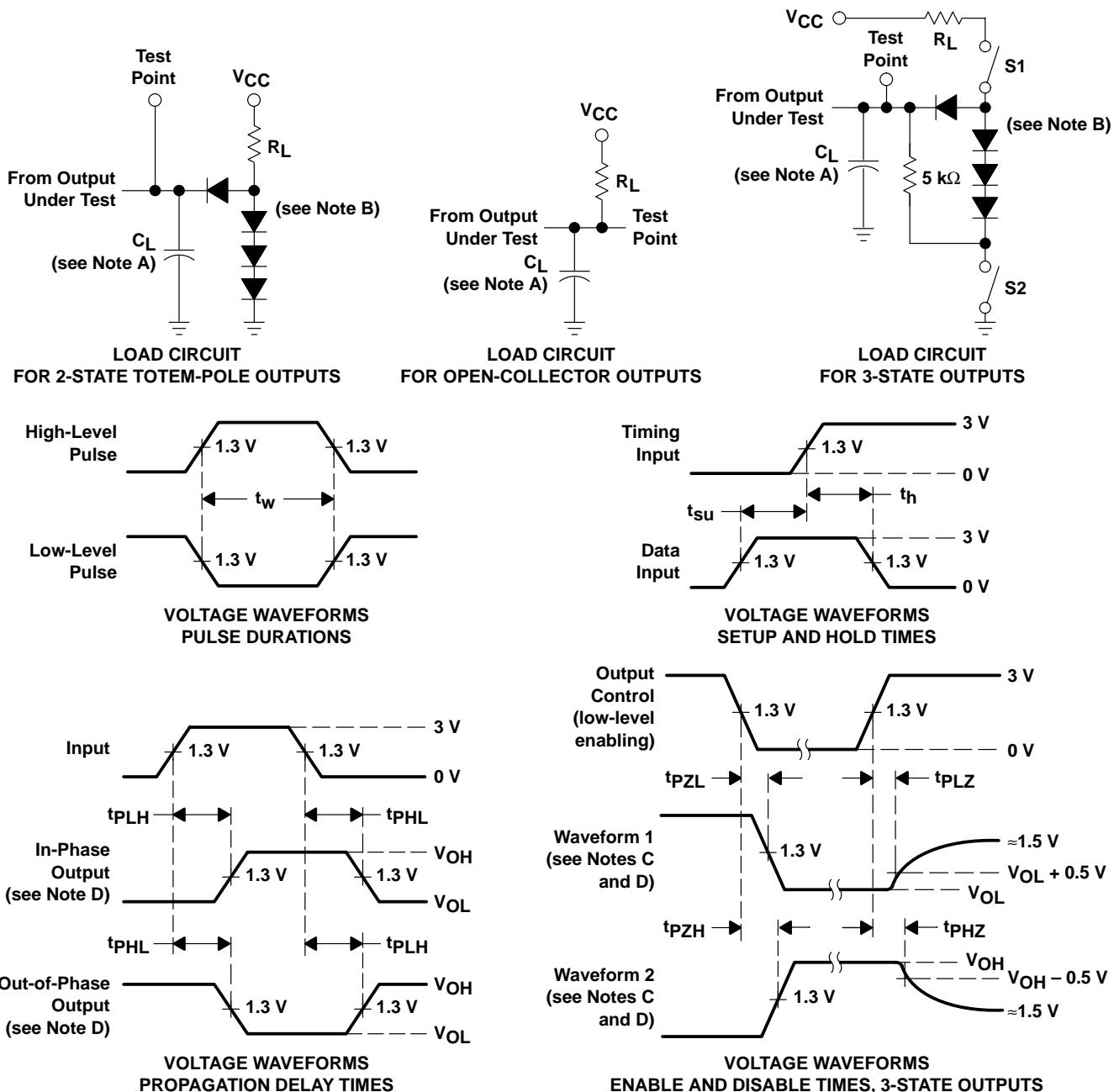
t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level



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PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



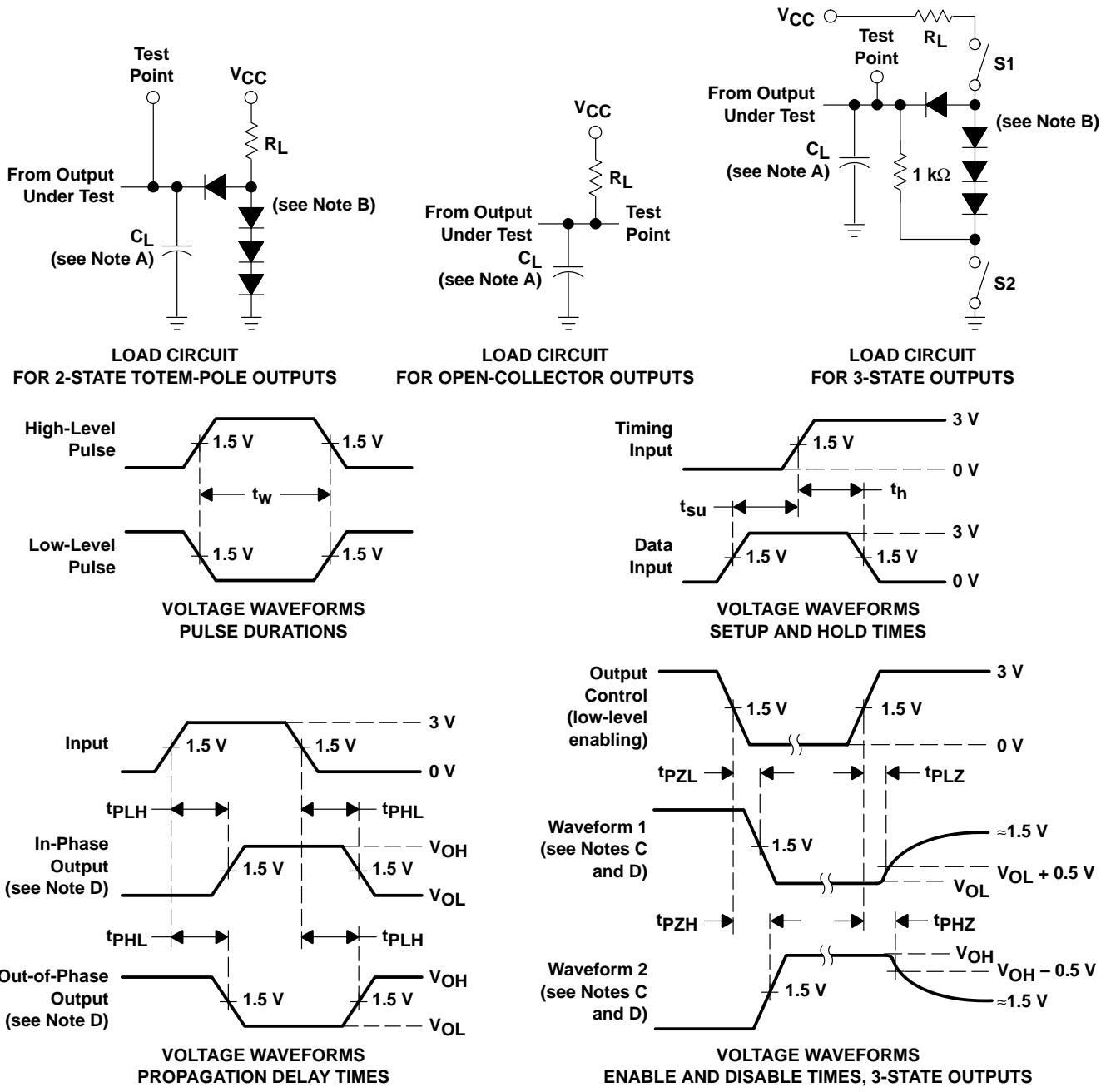
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N3064 or equivalent.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 - E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 - F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O \approx 50 \Omega$, $t_r \leq 1.5 \text{ ns}$, $t_f \leq 2.6 \text{ ns}$.
 - G. The outputs are measured one at a time with one input transition per measurement.
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54S/74S DEVICES**



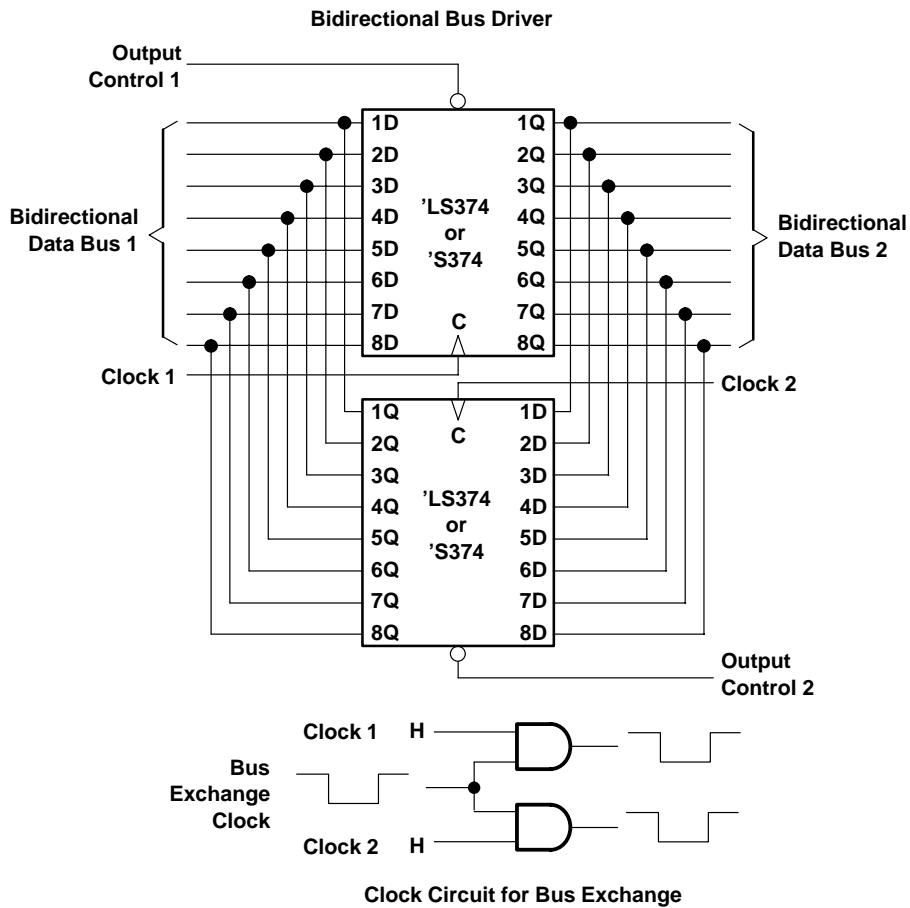
- NOTES:
- C_L includes probe and jig capacitance.
 - All diodes are 1N3064 or equivalent.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 - All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50 \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
 - The outputs are measured one at a time with one input transition per measurement.
 - All parameters and waveforms are not applicable to all devices .

Figure 2. Load Circuits and Voltage Waveforms

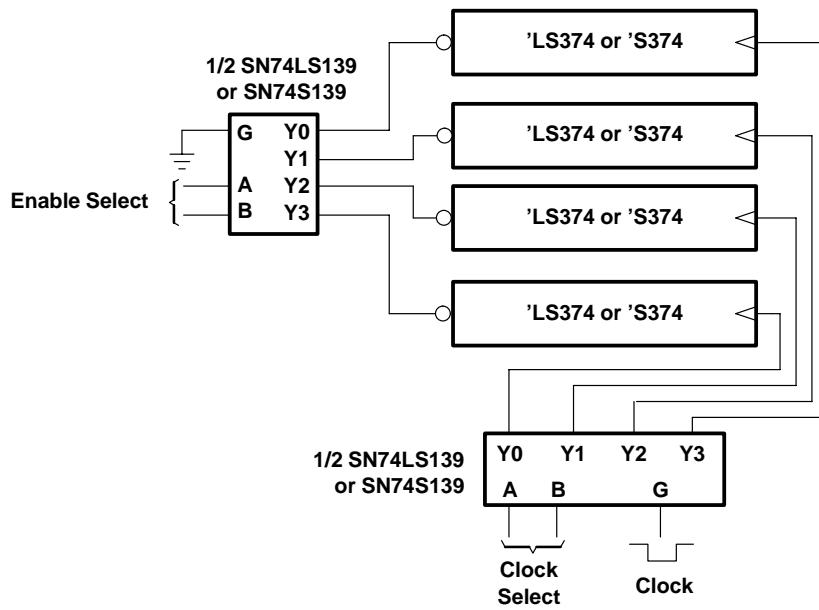
**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

TYPICAL APPLICATION DATA



Expandable 4-Word by 8-Bit General Register File



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|------------------|----------------------|--------------|------------------------------------|----------------|
| 5962-7801102VRA | ACTIVE | CDIP | J | 20 | 20 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-7801102VR A SNV54LS374J | Samples |
| 5962-7801102VSA | ACTIVE | CFP | W | 20 | 25 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-7801102VS A SNV54LS374W | Samples |
| 78011022A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 78011022A SNJ54LS 374FK | Samples |
| 7801102RA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 7801102RA SNJ54LS374J | Samples |
| 7801102SA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 7801102SA SNJ54LS374W | Samples |
| JM38510/32502B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32502B2A | Samples |
| JM38510/32502BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 32502BRA | Samples |
| JM38510/32502BSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32502BSA | Samples |
| JM38510/32502SRA | ACTIVE | CDIP | J | 20 | 20 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 32502SRA | Samples |
| JM38510/32502SSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32502SSA | Samples |
| JM38510/32503B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32503B2A | Samples |
| JM38510/32503BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 32503BRA | Samples |
| JM38510/32503BSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32503BSA | Samples |
| M38510/32502B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32502B2A | Samples |
| M38510/32502BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 32502BRA | Samples |
| M38510/32502BSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32502BSA | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|-------------------------|----------------|
| M38510/32502SRA | ACTIVE | CDIP | J | 20 | 20 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 32502SRA | Samples |
| M38510/32502SSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32502SSA | Samples |
| M38510/32503B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32503B2A | Samples |
| M38510/32503BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 32503BRA | Samples |
| M38510/32503BSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32503BSA | Samples |
| SN54LS373J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS373J | Samples |
| SN54LS374J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS374J | Samples |
| SN54S373J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54S373J | Samples |
| SN54S374J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54S374J | Samples |
| SN74LS373DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS373 | Samples |
| SN74LS373DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS373 | Samples |
| SN74LS373DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS373 | Samples |
| SN74LS373DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS373 | Samples |
| SN74LS373DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS373 | Samples |
| SN74LS373DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS373 | Samples |
| SN74LS373N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS373N | Samples |
| SN74LS373N3 | OBsolete | PDIP | N | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74LS373NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS373N | Samples |
| SN74LS373NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS373 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|-------------------------|----------------|
| SN74LS373NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS373 | Samples |
| SN74LS373NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS373 | Samples |
| SN74LS374DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS374A | Samples |
| SN74LS374DBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS374A | Samples |
| SN74LS374DBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS374A | Samples |
| SN74LS374DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS374 | Samples |
| SN74LS374DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS374 | Samples |
| SN74LS374DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS374 | Samples |
| SN74LS374DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS374 | Samples |
| SN74LS374J | OBSOLETE | CDIP | J | 20 | TBD | Call TI | Call TI | 0 to 70 | | | |
| SN74LS374N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS374N | Samples |
| SN74LS374N3 | OBSOLETE | PDIP | N | 20 | TBD | Call TI | Call TI | 0 to 70 | | | |
| SN74LS374NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS374N | Samples |
| SN74LS374NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS374 | Samples |
| SN74LS374NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS374 | Samples |
| SN74LS374NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS374 | Samples |
| SN74S373DW | NRND | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S373 | |
| SN74S373DWE4 | NRND | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S373 | |
| SN74S373DWG4 | NRND | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S373 | |



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PACKAGE OPTION ADDENDUM

25-Sep-2013

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------|------------------|----------------------|--------------|-------------------------------|---------|
| SN74S373J | OBsolete | CDIP | J | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74S373N | NRND | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S373N | |
| SN74S373N3 | OBsolete | PDIP | N | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74S373NE4 | NRND | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S373N | |
| SN74S374J | OBsolete | CDIP | J | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74S374N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S374N | Samples |
| SN74S374N3 | OBsolete | PDIP | N | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74S374NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S374N | Samples |
| SNJ54LS373FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54LS 373FK | Samples |
| SNJ54LS373J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS373J | Samples |
| SNJ54LS373W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SNJ54LS373W | Samples |
| SNJ54LS374FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 78011022A SNJ54LS 374FK | Samples |
| SNJ54LS374J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 7801102RA SNJ54LS374J | Samples |
| SNJ54LS374W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 7801102SA SNJ54LS374W | Samples |
| SNJ54S373FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54S 373FK | Samples |
| SNJ54S373J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54S373J | Samples |
| SNJ54S374FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54S 374FK | Samples |
| SNJ54S374J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54S374J | Samples |
| SNJ54S374W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SNJ54S374W | Samples |

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54LS373, SN54LS373-SP, SN54LS374, SN54LS374-SP, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 :

- Catalog: [SN74LS373](#), [SN54LS373](#), [SN74LS374](#), [SN54LS374](#), [SN74S373](#), [SN74S374](#)
- Military: [SN54LS373](#), [SN54LS374](#), [SN54S373](#), [SN54S374](#)
- Space: [SN54LS373-SP](#), [SN54LS374-SP](#)

NOTE: Qualified Version Definitions:



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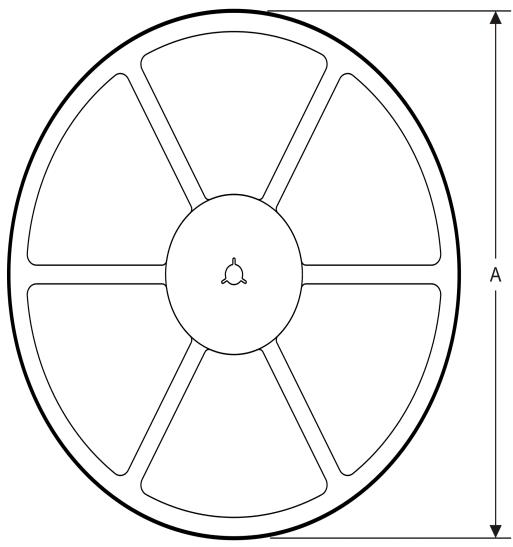
PACKAGE OPTION ADDENDUM

25-Sep-2013

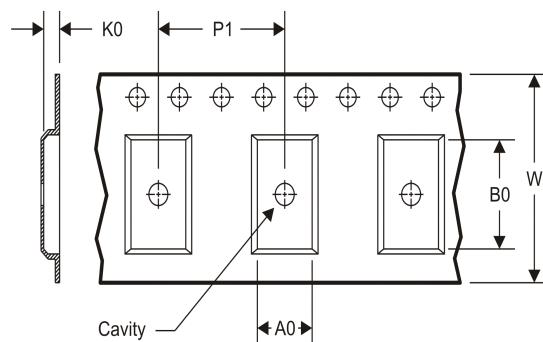
-
- Catalog - TI's standard catalog product
 - Military - QML certified for Military and Defense Applications
 - Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

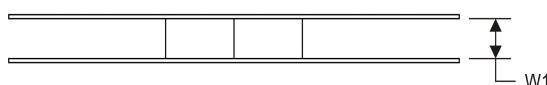
REEL DIMENSIONS



TAPE DIMENSIONS



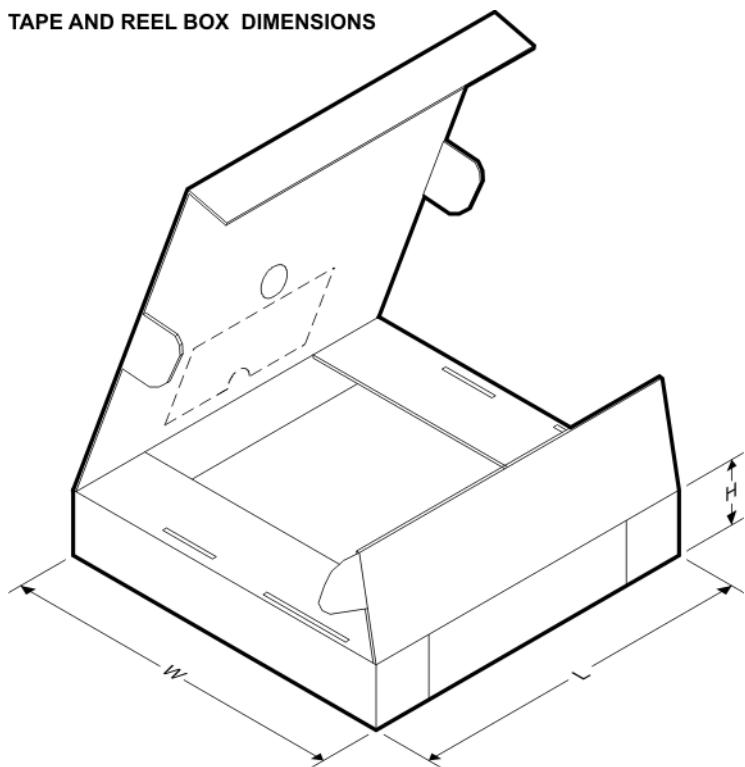
| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |



TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS373DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS373NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LS374DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS374DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS374NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


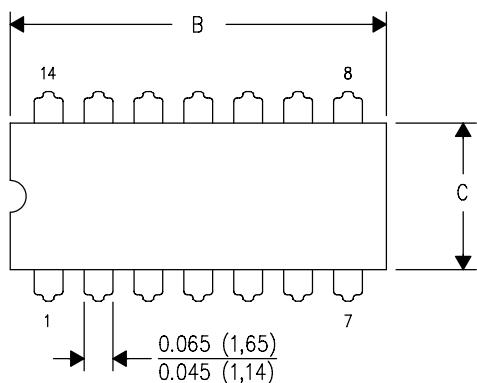
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS373DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS373NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS374DBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LS374DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS374NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

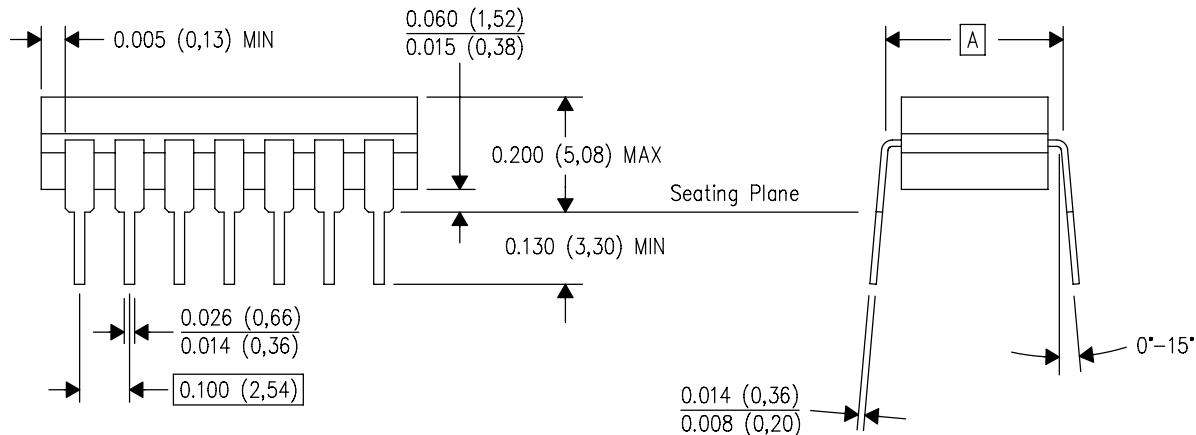
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS **\nDIM | 14 | 16 | 18 | 20 |
|--------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

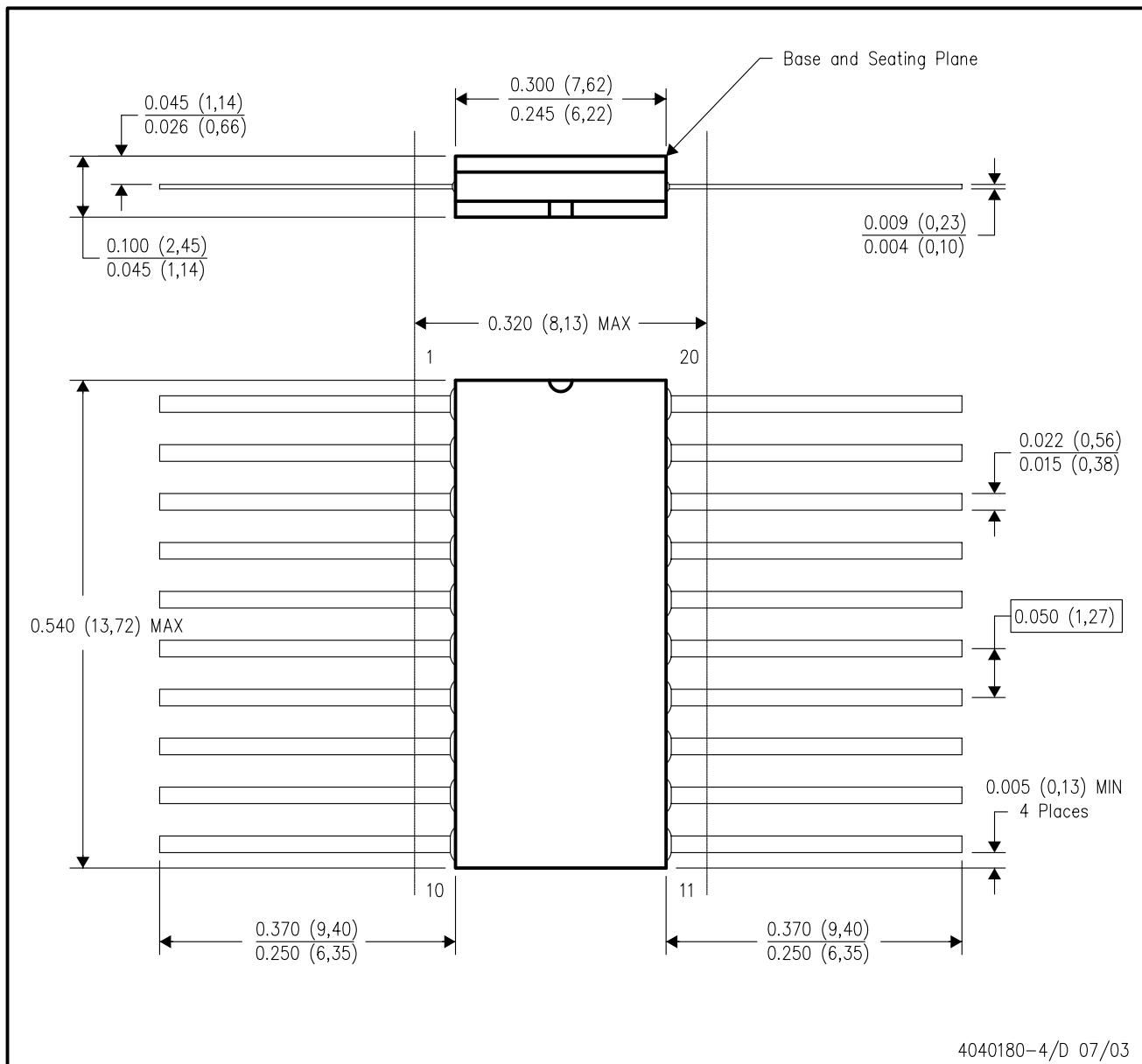


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

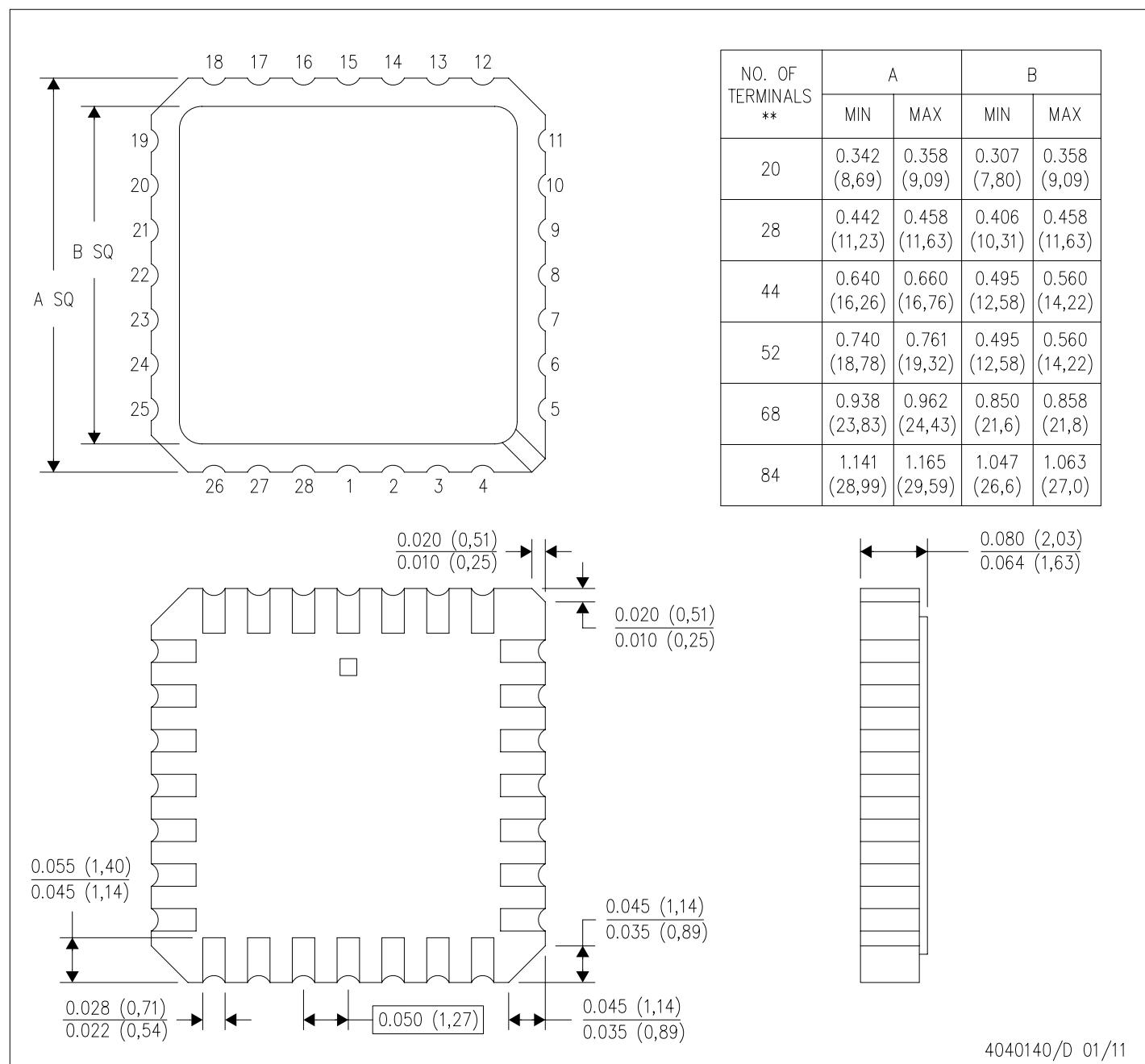


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



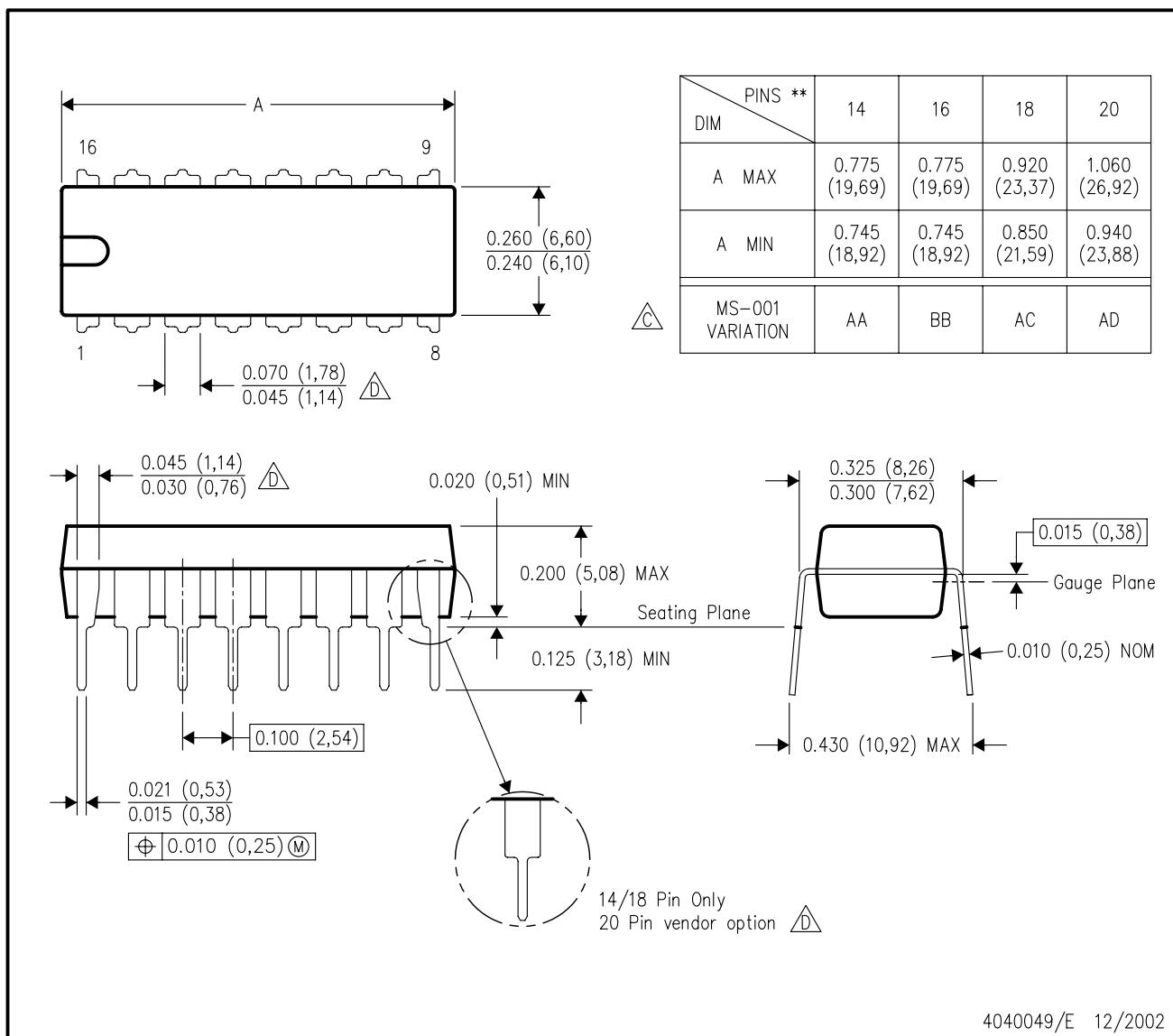
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

4040140/D 01/11

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

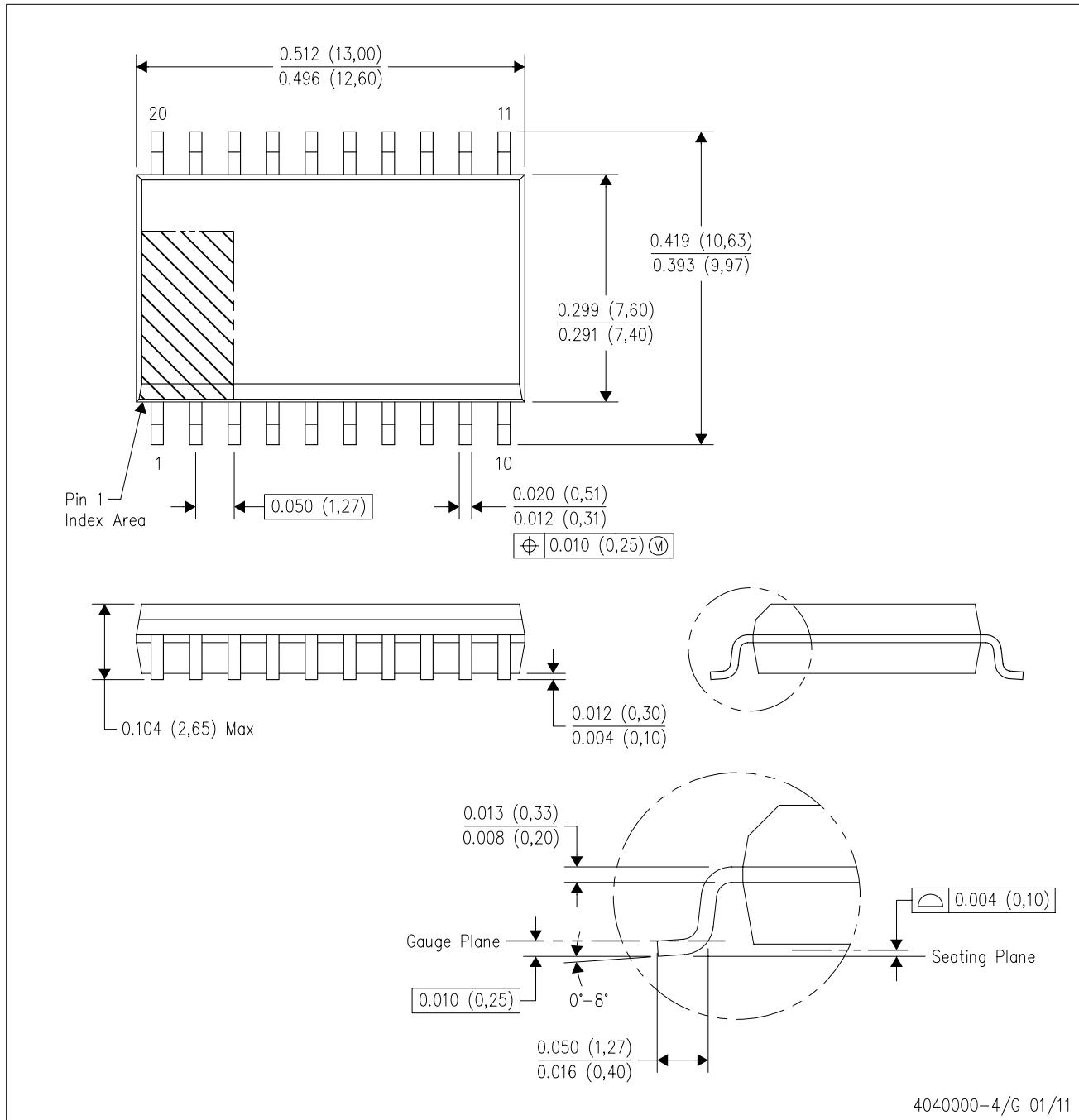
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



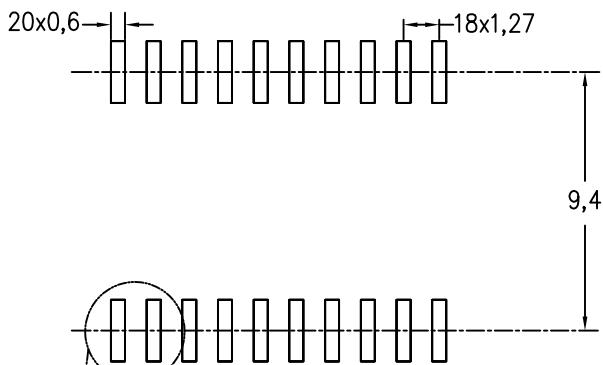
- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
 - D. Falls within JEDEC MS-013 variation AC.

LAND PATTERN DATA

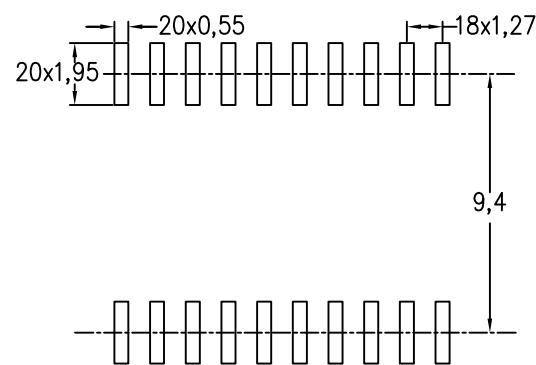
DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

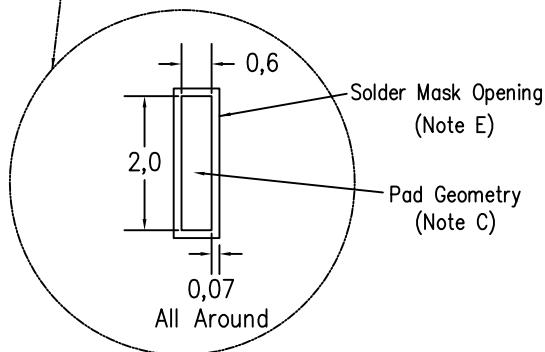
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Non Solder Mask Define Pad



4209202-4/F 08/13

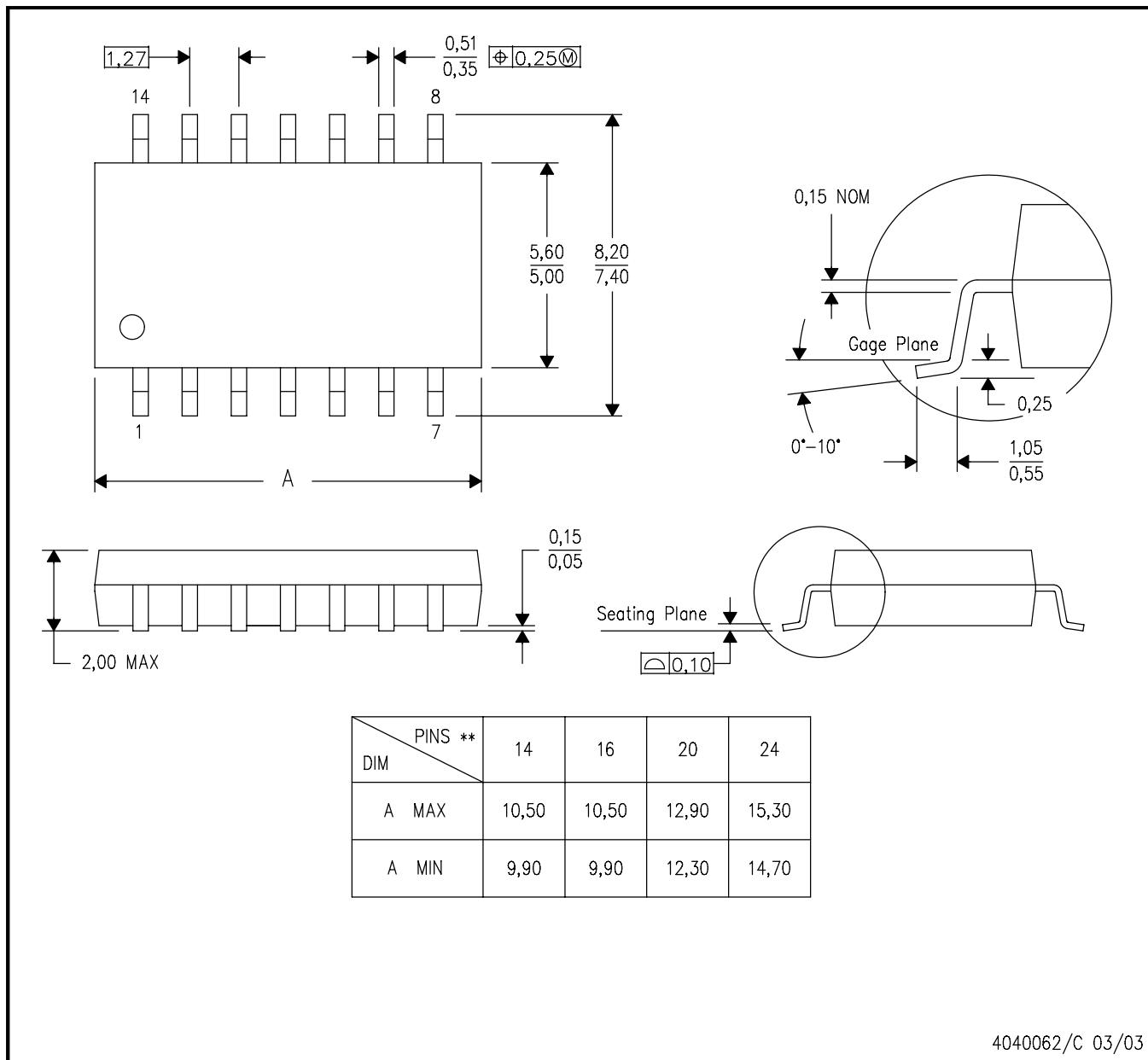
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

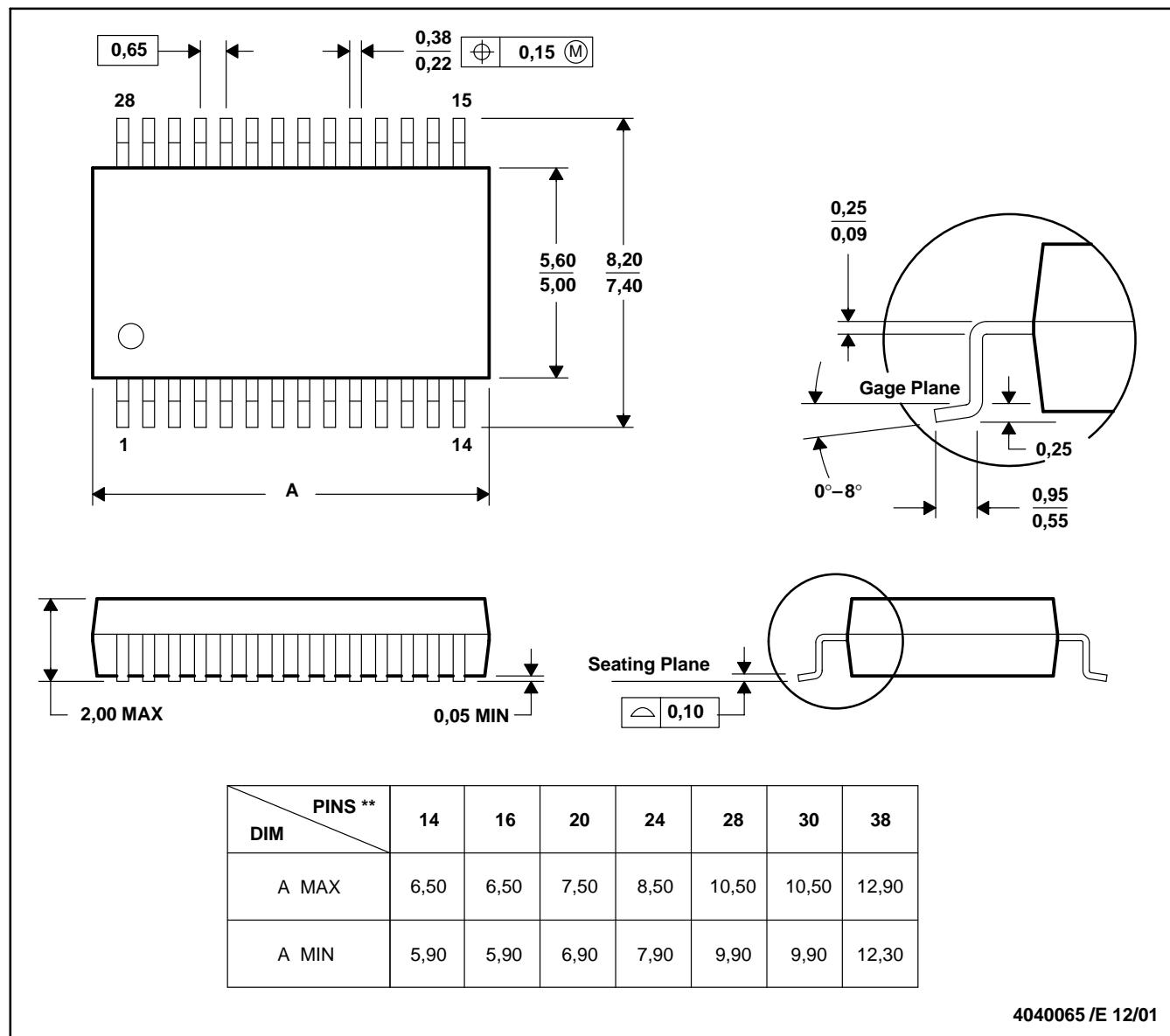


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. Falls within JEDEC MO-150

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