Assignment II – Cache Design   tag   index   offset

Please design an experiment (using the cache simulator) for studying the factors that affect the performance of cache accesses. We will address traces from gcc_ld_trace.txt [2000001] or go_ld_trace.txt as benchmarks. Please fill your results and plot graph of each table. In particular, what does the results suggest about the design of cache.

a. Block Size Tradeoff on direct mapped cache (Miss Rate)

Block Size (Bytes)	Direct mapped			
	Cache Size (KB)			
	4	8	16	32
4	16.52 %	11.24 %	7.50 %	5.25 %
8	17.39 %	11.69 %	7.67 %	5.21 %
16	16.13 %	10.79 %	6.99 %	4.66 %
32	15.62 %	10.33 %	6.63 %	4.41 %

b. N-way associative cache with replacement algorithms: Least recently used (LRU), and Round Robin (RR). 32 Block size (Bytes) [Fix Block Size : 32]
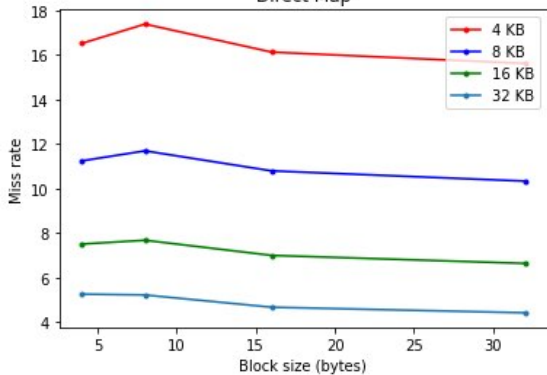
Cache Size (KB)	Associativity			
	Two-way		Four-way	
	LRU	RR	LRU	RR
1	24.62 %	25.74 %	22.77 %	37.09 %
4	11.30 %	12.16 %	9.68 %	18.86 %
8	7.38 %	8.00 %	6.16 %	12.59 %
32	2.26 %	2.47 %	1.77 %	4.85 %
512	0.38 %	0.39 %	0.37 %	0.52 %
1024	0.37 %	0.37 %	0.37 %	0.38 %

Note that simulation code and traces can be downloaded from
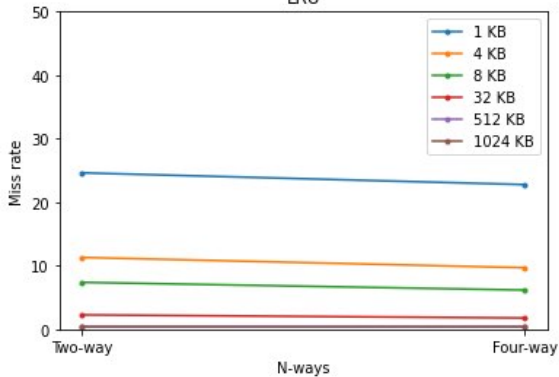https://www.cp.eng.chula.ac.th/~krerk/books/Computer%20Architecture/CacheSim

• The result suggests that we should use LRU four-way associative cache Since it has the least miss rate.

Direct Map

LRU

RR