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Computer System Architecture – 1st semester/2021
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https://github.com/NewGamezzz/CacheSim

Assignment II – Cache Design

tag index offset

Please design an experiment (using the cache simulator) for studying the factors that affect the performance of cache accesses. We will address traces from gcc_ld_trace.txt (2000001) or go_ld_trace.txt as benchmarks. Please fill your results and plot graph of each table. In particular, what does the results suggest about the design of cache.

a. Block Size Tradeoff on direct mapped cache (Miss Rate)

	Direct mapped			
Block Size (Bytes)	Cache Size (KB)			
	4	8	16	32
4	16.52 %	11.24 %	7.50 %	5.25 %
8	17.39 %	11.69 %	7.67 %	5.21 %
16	16.13 %	10.79 %	6.99 %	4.66 %
32	15.62 %	10.33 %	6.63 %	4.41 %

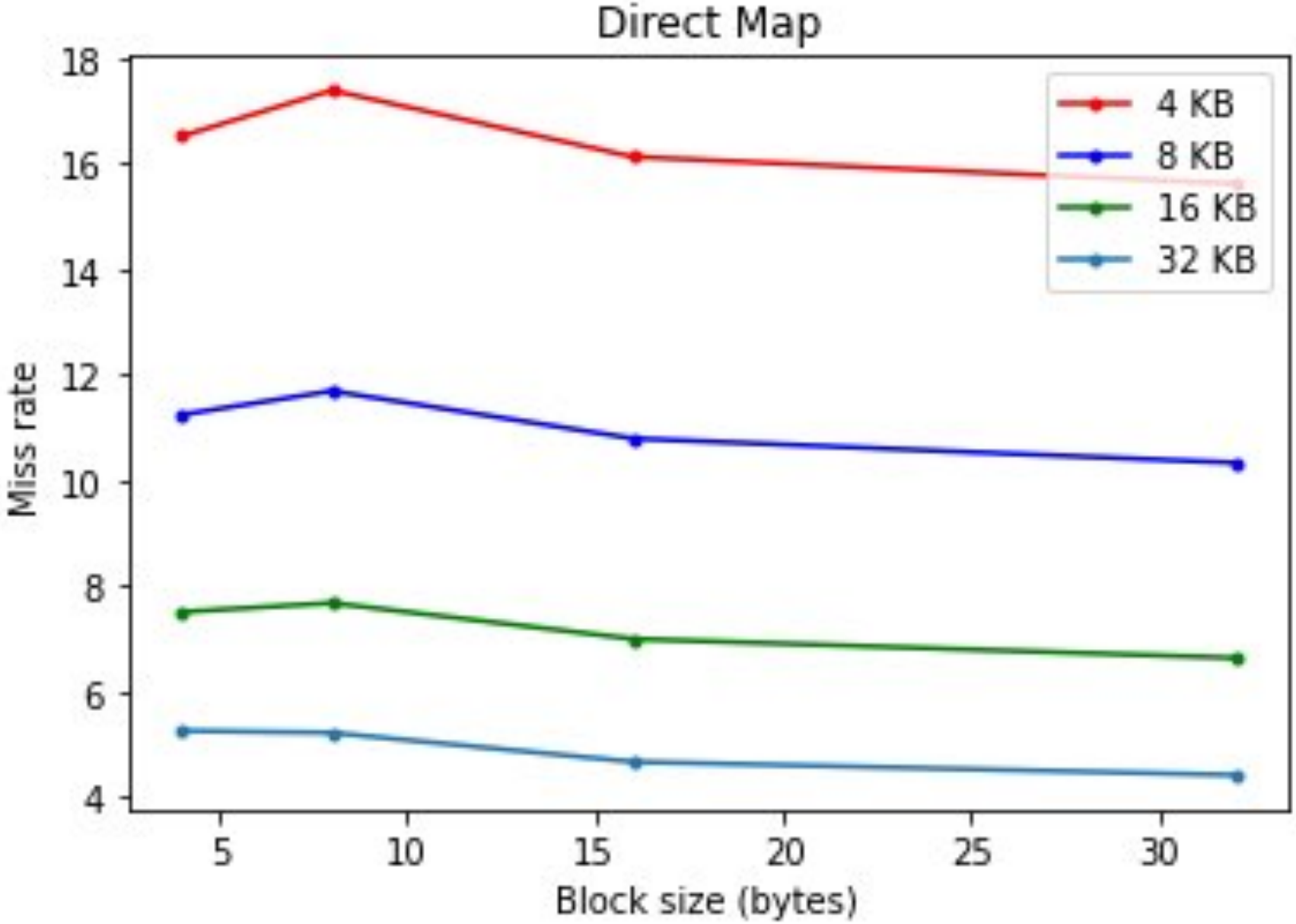
1.) Miss rate from block size 4 to 8 of every cache size is increased. However, after block size 8, if block size or cache size is increased, miss rate will be decreased.

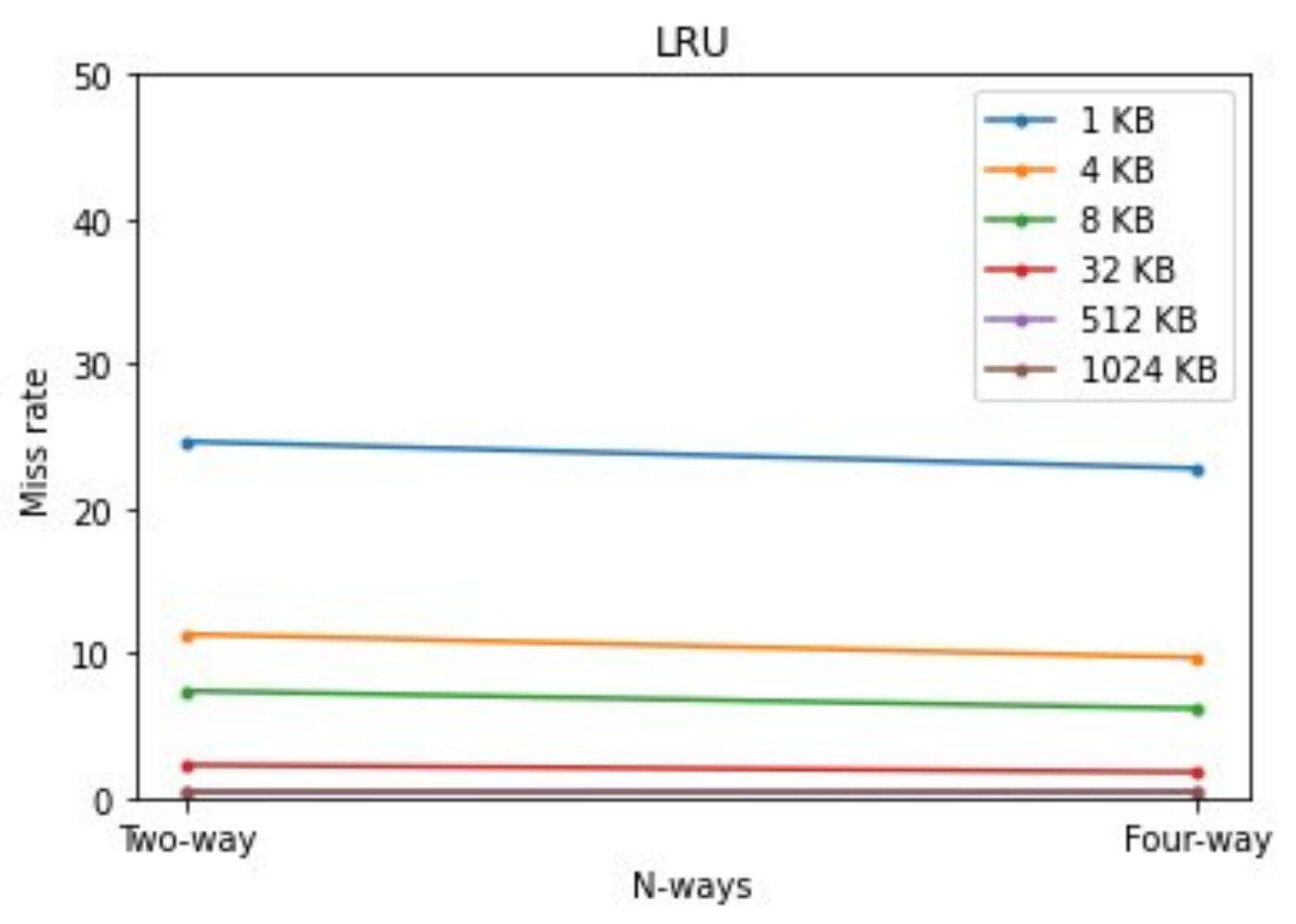
b. N-way associative cache with replacement algorithms: Least recently used (LRU), and Round Robin (RR). 32 Block size (Bytes) [Fix Block Size : 32]

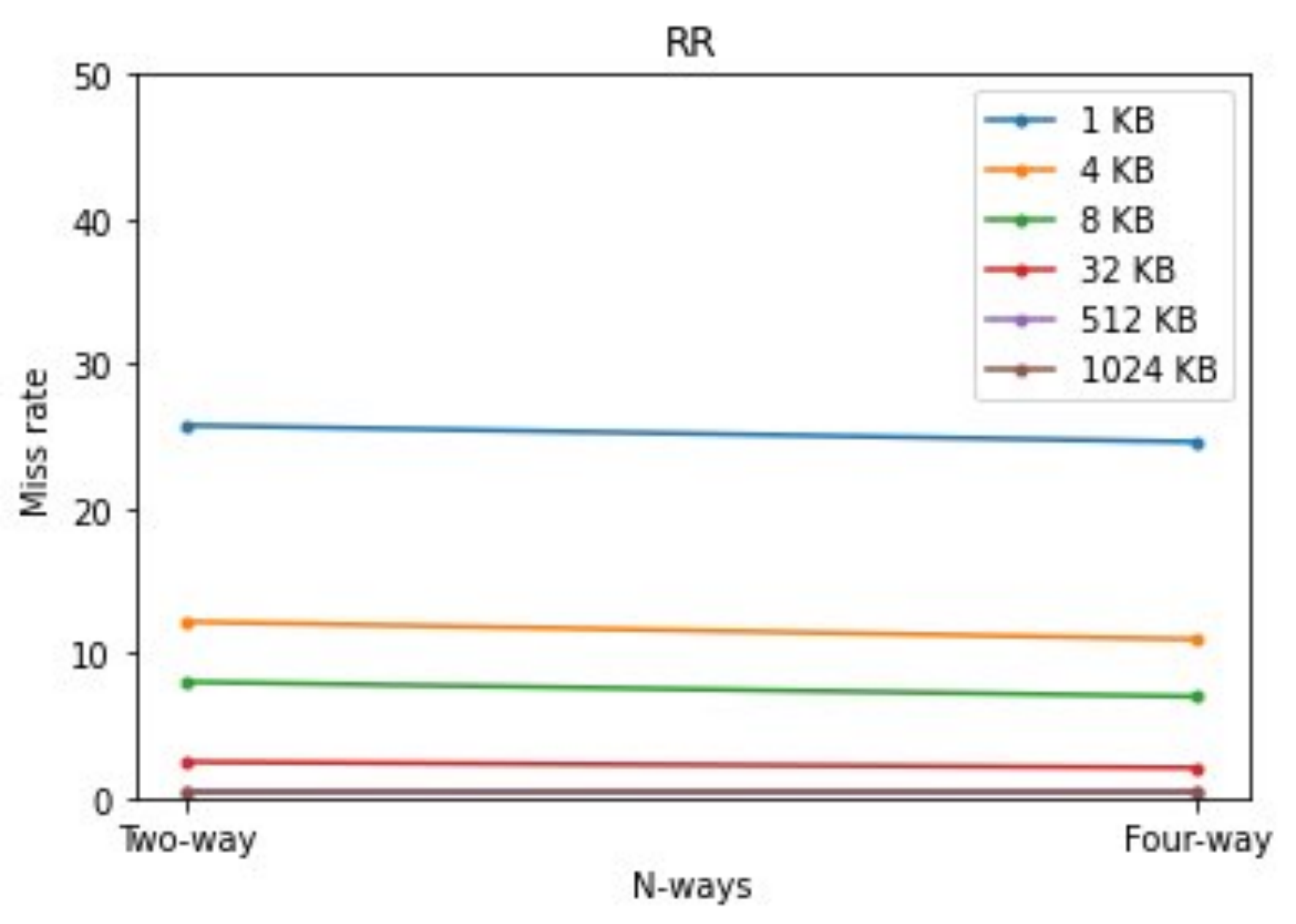
	Associativity			
Cache Size (KB)	Two-way		Four-way	
	LRU	RR	LRU	RR
1	24.62 %	25.74 %	22.77 %	24.59 %
4	11.30 %	12.16 %	9.68 %	10.95 %
8	7.38 %	8.00 %	6.16 %	6.99 %
32	2.26 %	2.47 %	1.77 %	2.07 %
512	0.38 %	0.39 %	0.37 %	0.37 %
1024	0.37 %	0.37 %	0.37 %	0.37 %

Note that simulation code and traces can be downloaded from
https://www.cp.eng.chula.ac.th/~krerk/books/Computer%20Architecture/CacheSim

2) The result suggests that we should use LRU four-way associative cache since it has the least miss rate.


Direct Map
18
16
14
12
10
8
6
4
Miss rate
5
10
15
20
25
30
Block size (bytes)
4 KB
8 KB
16 KB
32 KB


LRU
50
40
30
20
10
0
Miss rate
1 KB
4 KB
8 KB
32 KB
512 KB
1024 KB
Two-way
Four-way
N-ways


RR
50
40
30
20
10
0
Miss rate
1 KB
4 KB
8 KB
32 KB
512 KB
1024 KB
Two-way
Four-way
N-ways