Question 1

Part A

16KB cache = 16,384 Bytes = 2^{14} Bytes $\Rightarrow$ 32 - 14 = 18 tag bits
64B blocks = 2^6 Byte blocks $\Rightarrow$ 6 offset bits
14 - 6 = 8 index bits
0x00ffb048 = 0000 0000 1111 1111 1011 0000 0010 1000

tag	index	offset
0000 0000 1111 1111 01	11 0000 00	10 1000

Part B

512KB cache = 524,288 Bytes = 2^{19} Bytes
16B blocks = 2^4 byte blocks
8 way associative $\Rightarrow 2^3$
Index: $19 - 3 = 16$ index bits
Offset: $4 = 4$ offset bits
Tag: $32 - 15 - 3 = 12$ tag bits
0x1a2b3c4d = 0001 1010 0010 1011 0011 1100 0100 1101

tag	index	offset
0001 1010 0010	1011 0011 1100 0100	1101

Part C

hit time = 4 cycles
miss time = 28 cycles
miss rate = 1 - hit rate = 1 - 0.75 = 0.25
miss penalty = miss time - hit time = 28 - 4 = 24 cycles

$$AMAT = 4 + 0.25 \cdot 24 = 10$$

AMAT = 10 cycles

Part D

L1 hit time = 2 cycles
L1 hit rate = 0.75 ⇒ 0.25 miss rate
L2 hit time = 2 + 8 = 10 cycles
L2 hit rate = 0.5 ⇒ 0.5 miss rate
L2 miss penalty = 80 cycles

$$\begin{aligned} AMAT &= 2 + 0.25 \cdot ((10 + 0.5 \cdot 80) - 2) \\ &= 2 + 0.25 \cdot ((50) - 2) \\ &= 2 + 0.25 \cdot (48) \\ &= 2 + 12 = 14 \end{aligned}$$

AMAT = 14

Question 2

16KB capacity
16B block size/cache line
2 way associativity
no. of blocks = $2^{14}/2^4 = 2^{10} = 1024$ blocks, with two longs each and there are 512 sets.

a)Since each block can hold up to two longs, then the cache should miss every other long. Since if we look for a[0][0] in the cache, it will miss, and then both a[0][0] and a[0][1] will be stored in the cache.

Cache hit rate: 50%

b)Due to the way that the loops access the array, the hit rate will be 0%. Since the code accesses the array column wise, there will not be enough space in the cache for a hit

c)Compulsory miss, due to a lack in block size

d)Conflict miss, due to a lack of associativity.

e)Block size, this way more longs can be stored in the cache at a miss.

f)Increase associativity