Benchmark 1: spec00-bzip2

These are the cache values from the **bzip2** benchmark without any changes.

Instruction Count: 362,993,028

Cycle Count: 417,769,347

Sampler: TASS

Cache	Average Memory Latency	MemAccesses	MissRate1	MissRate2	RD	WR	BUS
IL1	2.0	238,638,066	0%	0%	100%	0%	0%
DL1	9.1	114,584,807	2.7%	4.5%	96.9%	95.7%	0%
L2	63.6	3,124,247	66.8%	66.8%	33.2%	0%	0%
Memory	60	1,936,828	0%	0%	100%	100%	0%

For the first parameter change, I wanted to see what would happen if I increase the associativity of the IL1 cache from 4 to 8. I was expecting an increase in the miss rate, hoping that there would be a slight increase in the number of capacity misses. Here are the results.

Cache	Average Memory Latency	MemAccesses	MissRate1	MissRate2	RD	WR	BUS
IL1	2.0	238,638,068	0%	0%	100%	0%	0%
DL1	9.0	114,584,600	2.7%	4.5%	96.9%	95.7%	0%
L2	63.6	3,093,261	66.6%	66.6%	33.4%	0%	0%
Memory	60	1,916,468	0%	0%	100%	100%	0%

Most of the benchmark results did not change except for a slight decrease in the hit rate of the **L2** cache. I'm not quite sure why this happened, my assumption is that some of the data had been pushed down to a lower level which resulted in more hits. Specifically, an increase in 0.2% for the hit rate of read instructions.

The next change was a decrease in the block size of the **DL1 cache from 32 to 8**. I expected an increase in the miss rate if I were to decrease the spacial locality of that level. With an increased miss rate with the L1 cache, I was also expecting an increase in the number of memory accesses for L2. Here are the results. As expected, there was an increase

Cache	Average Memory Latency	MemAccesses	MissRate1	MissRate2	RD	WR	BUS
IL1	2.0	238,638,068	0%	0%	100%	0%	0%
DL1	9.2	114,584,600	4.9%	7.4%	94.7%	93.1%	0%
L2	63.6	5,620,958	35.2%	38.9%	63.4%	0%	0%
Memory	60	1,762,288	0%	0%	100%	100%	0%

in miss rate for DL1 and in the number of memory accesses for L2. Although for a decrease in bloack size from 32 to 8, I was expecting a much larger increase in miss rate. I also did not expect the miss rate of the L2 cache to decrease as much as it did. I assume this is due to a lot of data having to be pushed down to L2 instead of being stored in L1, which would then lead to an increase in its hit rate.

Benchmark 2: spec00-crafty

 $\textbf{Instruction Count: } 362,\!993,\!023$

Cycle Count: 406,031,896

Sampler: TASS

Cache	Average Memory Latency	MemAccesses	MissRate1	MissRate2	RD	WR	BUS
IL1	2.3	235,407,812	0.2%	0.4%	99.8%	0%	0%
DL1	7.1	116,117,768	0.6%	0.7%	99.1%	99.9%	0%
L2	77.1	1,075,601	97.0%	97.0%	3.0%	0%	0%
Memory	60	1,023,978	0%	0%	100%	100%	0%

First change was to increase block size of DL1 from 32 to 64. Based on the previous benchmark, I was expecting a small increase or decrease of miss rate, since I would be increasing spatial locality, but decreasing temporal locality. Without knowing exactly what the benchmarks are performing, it would be difficult to make an educated guess of the effects. There would be an minuscule increase in the miss rate of DL1, but a quite significant de-

Cache	Average Memory Latency	MemAccesses	MissRate1	MissRate2	RD	WR	BUS
IL1	2.3	235,407,809	0.2%	0.4%	99.8%	0%	0%
DL1	7.1	116,117,175	0.7%	0.9%	98.9%	99.8%	0%
L2	55.3	1,235,659	59.0%	59.9%	40.1%	0%	0%
Memory	60	727,730	0%	0%	100%	100%	0%

crease in the miss rate of the L2 cache. Similar to the previous benchmark, this was probably due to the L1 cache not being able to hold as much data as before. There was also a decrease in the number of memory accesses from main memory.

The next change was to **decrease associativity of DL1 from 4 to direct-mapped**. I was attempting to make a more significant change to the hit rate of DL1 since all the previous changes have been small. The results are as follows

Cache	Average Memory Latency	MemAccesses	MissRate1	MissRate2	RD	WR	BUS
IL1	2.3	235,407,809	0.2%	0.4%	99.8%	0%	0%
DL1	9.8	116,117,045	3.7%	4.6%	95.1%	97.6%	0%
L2	71.9	4,704,187	92.6%	92.6%	7.4%	0%	0%
Memory	60	3,957,805	0%	0%	100%	100%	0%

As hoped, the change created a much more significant change. By changing the associativity of the L1 cache from 4 to being direct-mapped, there was a significant increase of misses overall. A 3% increase in primary misses for L1 is the largest change I have observed so far. Furthermore, although there was technically a slight decrease in miss rate for L2, the number of memory accesses increased significantly, which results in more misses in general.

Benchmark 3: spec00-gcc

Instruction Count: 362,993,023

Cycle Count: 822,813,193

Sampler: TASS

For these tests I wanted to try and affect the sim time instead of playing with the cache

parameters. Here are the base values

	Rabbit	Warmup	Detail	Timing
KIPS	97816	N/A	517248	1308
Time	11.6%	0%	1.8%	86.6%
Inst	51.8%	0%	43%	5.2%

Simulation Time: 347.499 seconds

For the first change, I reduced the L3(I assume this is main memory) size from 2GB to 1GB. I was expecting a large increase in the simulation time, and perhaps an increase in miss rate for memory. Here are the results

	Rabbit	Warmup	Detail	Timing
KIPS	102904	N/A	248056	11288
Time	5.7%	0%	2%	92.4%
Inst	51.8%	0%	43%	5.2%

Simulation Time: 648.099 seconds

As expected, the total simulation time doubled entirely from reducing the size of memory. Sadly, there were no changes to the miss rates of any of the caches, which is why none of the values are currently displayed. However, I was confused as to why the IPC did not change, as I had initially thought that the reducing in memory capacity would have at least a minor effect.

The next change was to the **instruction queue size from 24 to 12**. I am expecting changes similar to that of the previous benchmark test, here are the results.

	Rabbit	Warmup	Detail	Timing
KIPS	101110	N/A	244754	11199
Time	5.7%	0%	2%	92.4%
Inst	51.8%	0%	43%	5.2%

Simulation Time: 653.169 seconds

Similar to the previous test, I was expecting more changes to the CPU's general performance, but the only thing that changed was the massive increase in simulation time as well. This effect makes sense as the CPU can only look at half the instructions at a time.

Benchmark 4: spec00-gzip

Instruction Count: 362,993,053 Cycle Count: 352,727,393

Sampler: TASS

Cache	Average Memory Latency	MemAccesses	MissRate1	MissRate2	RD	WR	BUS
IL1	2	237,010,544	0%	0\$	100%	0%	0%
DL1	11.4	101,478,498	2.5%	6.6%	97.8%	90.0%	0%
L2	67.6	2,504,678	33.9%	33.9%	66.1%	0%	0%
Memory	60	1,371,981	0%	0%	100%	100%	0%

The first parameter change was to **completely remove the IL1** cache. I wanted to see the effect it would have by removing a whole level of the cache. I expect to have an increase in memory accesses for DL1 and perhaps a change in the miss rate for all the lower level caches. Here were the results

Cache	Average Memory Latency	MemAccesses	MissRate1	MissRate2	RD	WR	BUS
IL1	-	-	-	-	-	-	-
DL1	11.4	101,478,498	2.5%	6.6%	97.8%	90.0%	0%
L2	67.6	2,504,025	33.9%	33.9%	66.1%	0%	0%
Memory	60	1,371,085	0%	0%	100%	100%	0%

For some reason nothing had changed except for the fact the IL1 cache was missing from the report, I was sure that I did it correctly, so I am unsure as to why none of the values had changed. I expected the number of memory accesses to change for DL1 but it had stayed the exact same.

This time I wanted to **remove DL1** instead and see if there would be any change. Because of the previous benchmark test not having any affect, I expect the same from this one. Here are the results

Cache	Average Memory Latency	MemAccesses	MissRate1	MissRate2	RD	WR	BUS
IL1	2.0	237,010,637	0%	0%	100%	0%	0%
DL1	-	-	-	-	-	-	-
L2	67.6	425	99.8%	99.8%	0%	0%	0%
Memory	60	425	0%	0%	99.9%	100%	0%

Due to the removal of the DL1 cache, there was a significant decrease in memory accesses from L2 and main memory, which basically no hits. I am still unsure as to why this is the case, as I would have though there would be an increase in memory accesses with the lower levels. I might have changed the parameters incorrectly in my bash script.

Appendix

bzip2: base

```
# File : esesc_ispec00_bzip2.iliZKn : Sun Oct 16 14:35:50 2022

Sampler O (Procs O)
Rabbit Narnup Detail Timing Total KIPS

KIPS 98587 N/A 608975 1084 27196

Time 14.3% 0.0% 1.9% 83.6% : Sin Time (s) 284.599 Exe 245.747 ms Sin (1700MHz)
Inst 51.8% 0.0% 43.0% 5.2% : Approx Total Time 4743.372 ms Sin (1700MHz)

Proc : Delay : Avg_Time : BPType : Total : RAS : BPred : BTB : iBTB : BTAC : NasteRatio : MPKI 0 : 3 : 25.704 : 2bit : 92.60% : 100.00% of 6.87% : 91.32% of 85.25% : 95.24% of 52.37% : 0.00% : 0.00% : 0.14% : 10.60 0 : 4 : 25.704 : 2bit : 92.60% : 0.00% of 0.00% : 91.44% of 86.49% : 0.00% of 0.00% : 52.37% : (1.24% fixed) : 10.60 Proc : nCommit : nInst : AALU : BALU : CALU : LALU : SALU : LD Fwd : Replay : Norst Unit (clk) 0 : 362993010 : 362993028 : 53.13% : 15.31% : 0.00% : 22.37% : 9.19% : 6.16% : N/A : 0.00

Proc : IPC uIPC Active Cycles Busy LDQ STQ INIn ROB Regs IO maxR MtSbr Br4clk broblay 0 0.87 0.87 1.00 41769347 43.4 0.0 0.7 3.6 0.1 3.6 0.0 0.0 0.0 0.0 0.0 0.0 12.5

Cache Occ AvgMemLat MemAccesses MissRate (RD, MR, BUS) 11(0) 0.0 2.0 238638066 0.0% 0.0% (100.0%, 0.0%, 0.0%) 0.80 0.0 0.0 0.0 0.0 0.0 0.0 CB/s

DL1(0) 0.0 63.6 3124247 66.8% 66.8% (33.2%, 0.0%, 0.0%) 0.8 0.0 GB/s

Memory(0) 0.0 60.0 1936828 0.0% 0.0% (100.0%, 100.0%, 0.0%) 0.5 0.0 GB/s
```

bzip2: IL1 associativity from 4 to 8

bzip2: DL1 block size from 32 to 8

crafty: base

crafty: DL1 block size from 32 to 64

crafty: DL1 associativity from 4 to 1

```
# File : esesc_3spec00_crafty.CtMmQv : Sun Oct 16 15:30:47 2022

Sampler (Procs 0)

Rabbit Narrupp Detail Turing Total KIPS

KIPS

FIRE 97:31 NV No S97:97 1332 22177

KIPS 97:31 NV No S97:97 1332 22177

Froc: Delay : Avg.Time : BPType : Total : PAS : BPred : BTB : BTB : BTAC : MasteRatio : MPKI 0 : 3 : 34.232 : Zbit : 90.45% : 99.92% of 4.80% : 83.05% of 56.2% : 11.75% of 48.33% : 0.00% : 0.00% : 0.00% : 11.16

0 : 4 : 34.232 : Zbit : 90.45% : 99.92% of 4.80% : 83.05% of 56.2% : 11.75% of 48.33% : 0.00% : 0.00% : 0.00% : 11.16

0 : 4 : 34.232 : Zbit : 90.45% : 99.92% of 0.00% : 88.37% of 62.212 : M1.31% of 1.90% : 46.43% : (26.60% fixed) : 11.16

Proc: nConveit : nInst : AALU : BALU : CALU : LALU : SALU : LD Fwd : Replay : Morst Unit (clk)

0 : 36.2993018 : 36.2993024 : 55.41% : 12.25% : 0.35% : 21.76% : 10.22% : 3.32% : N/A : 0.00

Proc IPC UIPC Active Cycles Busy LDQ STQ INIn ROB Reps 10 maxBr Missr Br4CLk brDelay 0 0.67 0.67 0.67 1.00 53047431 33.7 0.1 0.0 3.6 0.0 13.7 0.0 0.0 0.0 0.0 0.0 8.5

Cache Occ AvgMenLat MenAccesses MissRate ( RD , NR, BUS)

L1(0) 0.0 2.3 253497991 0.2% 0.4% ( 99.8% 0.0% 0.0% 0.0%) 46.4 0.0 GB/s

ELCON D. 117045 3.7% 4.6% ( 95.1% 97.6% 0.0%) 0.9% 0.0 GB/s

L2(0) 0.0 71.9 4704187 92.6% 92.6% ( 77.8%, 0.0%) 0.0% 0.0 0.0 GB/s

Memory(0) 0.0 0.0 3057805 0.0% 0.0% (100.0%, 100.0%) 0.0% 0.0 0.0 0.0 0.0 GB/s
```

gcc: base

```
# File : esesc_ispec00_gcc.bskTkf : Sun Oct 16 18:23:56 2022

Sampler 0 (Procs 0)
RIPS 97816 N/A 517248 1308 21848
RIPS 97816 N/A 518248
RIPS 97816 N/A 518248
RIPS 18TB 18TAC : MasteRatio : MPKI
0 : 3 : 55.618 : Zitevel : 97.69% : 99.99% of 1.75% : 97.23% of 86.46% : 91.89% of 69.24% : 0.00% : 0.09% : 0.19% 3.32
RIPS 18TB 18TAC : MasteRatio : MPKI
0 : 3 : 55.618 : Zitevel : 97.69% : 9.99% of 1.75% : 97.23% of 86.46% : 91.89% of 69.24% : 0.00% : 0.19% 3.32
RIPS 18TB 18TAC : MasteRatio : MPKI
0 : 3 : 55.618 : Zitevel : 97.69% : 0.09% of 0.09% : 97.31% of 88.93% : 36.80% of 0.52% : 68.72% : (2.61% fixed) : 3.32
RIPS 18TB 18TAC : MasteRatio : MPKI
0 : 3 : 55.618 : Zitevel : 97.69% : 0.09% of 0.09% : 97.31% of 88.93% : 36.80% of 0.52% : 68.72% : (2.61% fixed) : 3.32
RIPS 18TB 18TAC : MasteRatio : MPKI
0 : 3 : 55.618 : Zitevel : 97.69% : 0.09% of 0.09% : 97.31% of 88.93% : 36.80% of 0.52% : 68.72% : (2.61% fixed) : 3.32
RIPS 18TB 18TAC : MasteRatio : MPKI
0 : 3 : 55.618 : Zitevel : 97.69% : 0.09% of 0.09% : 97.31% of 88.93% : 36.80% of 0.52% : 68.72% : (2.61% fixed) : 3.32
RIPS 18TB 18TAC : MasteRatio : MPKI
0 : 3 : 55.618 : Zitevel : 97.69% : 0.09% of 0.09% : 97.31% of 88.93% : 37.89% if 0.09% if 0.09% if 0.09% of 0.09% if 0.09
```

gcc: L3 size from 2GB to 1GB

```
# File : esess_Zepec00_gcc.8EMJS: Non Oct 17 19:23:18 2022

Sampler 0 (Procs 0)
Rabbit Narrup Detail Timing Total KIPS

KIPS 10:2904 N/A 248056 634 11:88

Time 5.7% 0.0% 2.0% 92.4% : Sim Time (s) 648.099 Exe 484.033 ms Sim (1700MHz)

Tims 5.1% 0.0% 43.0% 5.2% : Approx Total Time 9339.721 ms Sim (1700MHz)

Proc: Delay: Avg.Time : BPType : Total : RAS : BPred : BTB : 1BTB : BTAC : MasteRatio : MPKI 0 : 3 : 55.832 : Zbit : 97.60% : 99.98% of 1.75% : 97.23% of 86.46% : 91.69% of 69.24% : 0.00% : 0.00% : 0.19% 3.32 0 : 4 : 55.832 : Zbit : 97.60% : 0.00% of 0.00% of 0.00% : 97.31% of 88.03% : 36.80% of 0.52% : 68.72% ( 2.61% fixed) : 3.32

Proc: nCoewnit : nInst : AALU : BALU : CALU : LALU : SALU : LD Fwd : Replay : Morst Unit (clk) 0 : 362993010 : 362993022 : 37.55% : 14.11% : 0.01% : 22.20% : 25.73% : 1.53% : N/A : 0.00

Proc IPC UPC Active Cycles Busy LDQ STQ IMIn ROB Regs ID masker MtSBr Br4CIk br0elay 0 0.44 0.44 1.00 622855594 22.1 0.0 14.1 42.1 0.0 3.3 0.0 0.0 0.0 0.0 0.0 6.1

Cache Occ AvgMemLat MemAccesses MissRate (RD, MR, BUS) 11.00 0.00 0.00 6.7 173908055 17.4% 50.11% (7.0%, 0.0%) 0.0% 0.0%) 31.0 0.0 GB/s

L2(0) 0.0 5.5 30603818 99.0% 99.0% (1.0%, 0.0%) 31.0 0.0 GB/s

Memory(0) 0.0 60.8 13049868 0.0% 0.0% (100.0%, 100.0%, 0.0%) 1.7 0.0 GB/s
```

gcc: Instruction queue from 24 to 12

```
# File : eses_3spec00_gcc.wM7XjD : Non Oct 17 19:43:08 2022

Sampler 0 (Procs 0)

Robbit Marmup Detail Tining Total KIFS

KIPS 101110 N/A 24744 629 11199

Time 5.7% 0.0% 2.0% 92.3% : Sin Tine (s) 653.169 Exe 484.158 ms Sin (1700MHz)

Time 5.7% 0.0% 2.0% 92.3% : Approx fold Tine 9842.609 ms Sin (1700MHz)

Proc: Delay: Avg.Time : BPType : Total : RAS : BPred : BTB : BTAC : MasteRatio : NPKI 0 : 3 : 55.871 : 2bit : 97.60% : 99.98% of 1.75% : 97.23% of 86.46% : 91.89% of 69.24% : 0.00% : 0.00% of 9.33 : 0.00% : 0.00% of 0.0
```

gzip: base

gzip: IL1 removed

gzip: DL1 removed