CS6135_HW1 Report

109062648 柳孟芸

1. **A comparison table like the following one, and an explanation of the result (The table should be built under a fixed core utilization and clock period and you should specify them in the report.)**

core utilization : 0.7 , clock period : 180

	(congestion-driven, timing-driven)			
	(off, off)	(on, off)	(off, on)	(on, on)
slack	54.15	53.59	55.10	54.88
total cell area	368059.127445	367836.768029	367451.458276	367775.661626
total wirelength	1171455 micron	1163917 micron	1139781 micron	1159522 micron

① (off, off)：congestion & timing均未開啟，均沒有做優化，因此total cell area跟wirelength為四者之中最高。

② (on, off)：congestion為on，因在placement對於congestion做了優化，因此比起①的total cell area跟wirelength都有些許下降。

③ (off, on)：timing為on，total cell area跟wirelength為四者之中最低，performance最好。

④ (on, on) ：congestion & timing均開啟，雖然slack並未下降，但total cell area跟wirelength比起①已下降許多，由此可知需在兩者之間做取捨才可得到好的slack。

2. **The difference(s) between the congestion-driven placement and timing- driven placement**

Timing Driven顧名思義是指基於時序驅動進行的placement，is done when we are dealing with timing critical designs. Here the placement of standard cells will be done in such a way that the cells belonging to a critical path(paths which have max negative slack) will be placed close together, 但是可能會增加congestion (especially after routing).

Congestion Driven是指基於congestion做優化的placement，在place過程中tool會通過global route估算design中的繞線情況，從根據估算的congestion狀況進行placement的優化。通常在small size die中會選擇做Congestion Driven placement，因此the seperation between standard cells will be increased to take in to account the routing that will be done in the later stage,但是由於單元之間的間隔增加了，所以timing會延長。

- Sometimes we want the performance as good as possible <= timing driven
- Sometime we just want that routing is successful <= congestion driven

Generally, the performance of circuit with timing driven is better.In this case, it's better that the standard cells are placed together which may causes routing fail.但是一但繞線失敗，電路就無法運作進而毫無performance可言，所以我們必須在congestion-driven placement與timing- driven placement之間做取捨。

3. An explanation of why we insert filler cells

In short, Filler cells primarily are non-functional cells used to continue the VDD and VSS rails and establish the continuity of the N- well and the implant layers on the standard cell rows.

• Insert filler cells有兩個主要目的:

①They reduce the DRC Violations created by the base(NWell, PPlus & NPlus) layers.

②They help maintain the Power Rail connection continuity.

Basically filler cells will make power/ground and nwell continuity.
If we don't insert filler cells, there will be power/ground open between the standard cells(empty space) and also may be nwell spacing DRC error.

4. Your best clock period to maintain a minimum non-negative slack, the corresponding core utilization, the corresponding slack, the corresponding core area, and the corresponding total wirelength

best clock period : 128
the corresponding core utilization : 0.7
the corresponding slack : 1.44
the corresponding core area : 540789
the corresponding total wirelength : 1167943 micron