
STM32
CubeMX

1. Description

1.1. Project

Project Name	PM4_Firmware
Board Name	custom
Generated with:	STM32CubeMX 6.13.0
Date	04/06/2025

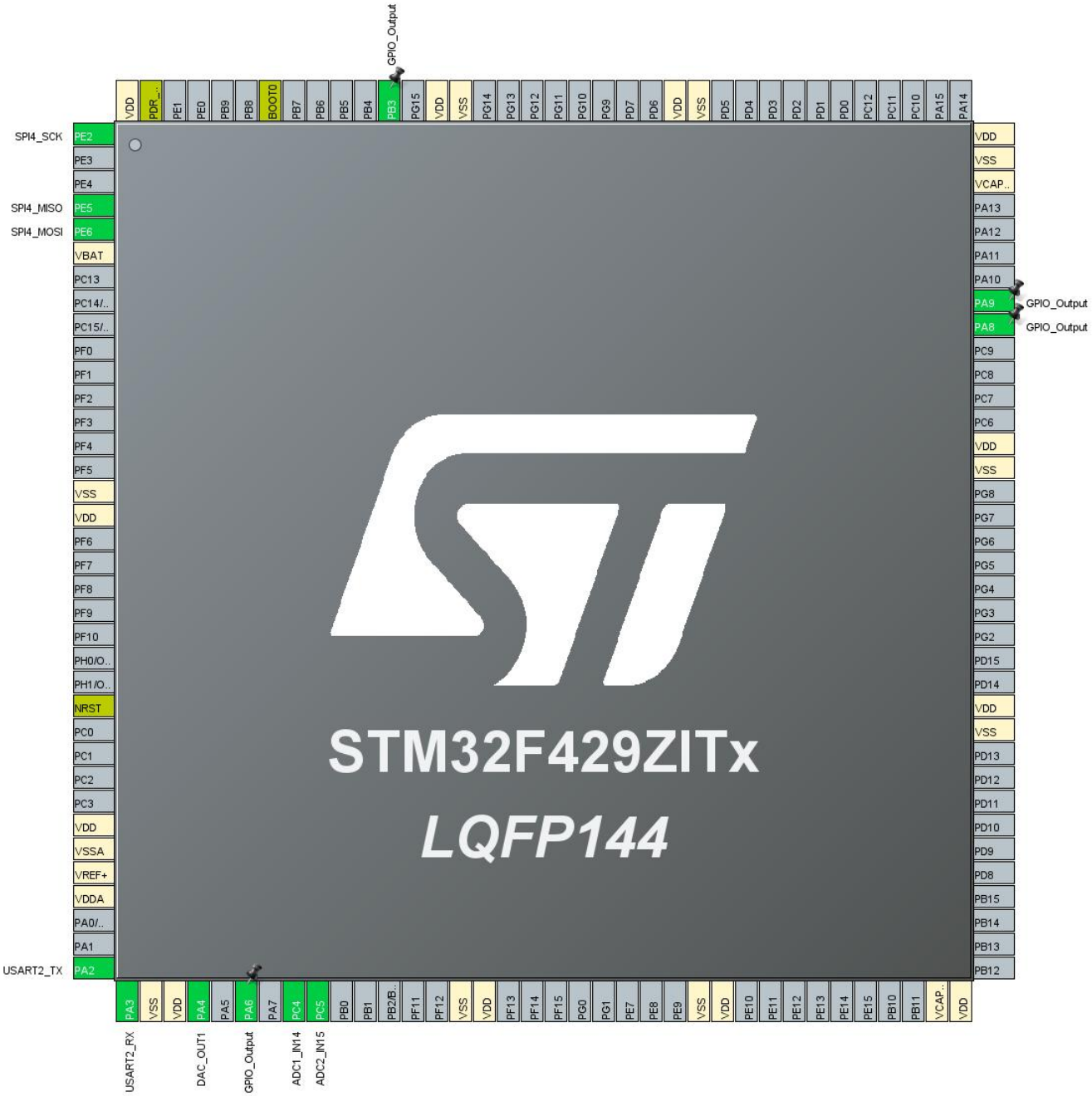
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



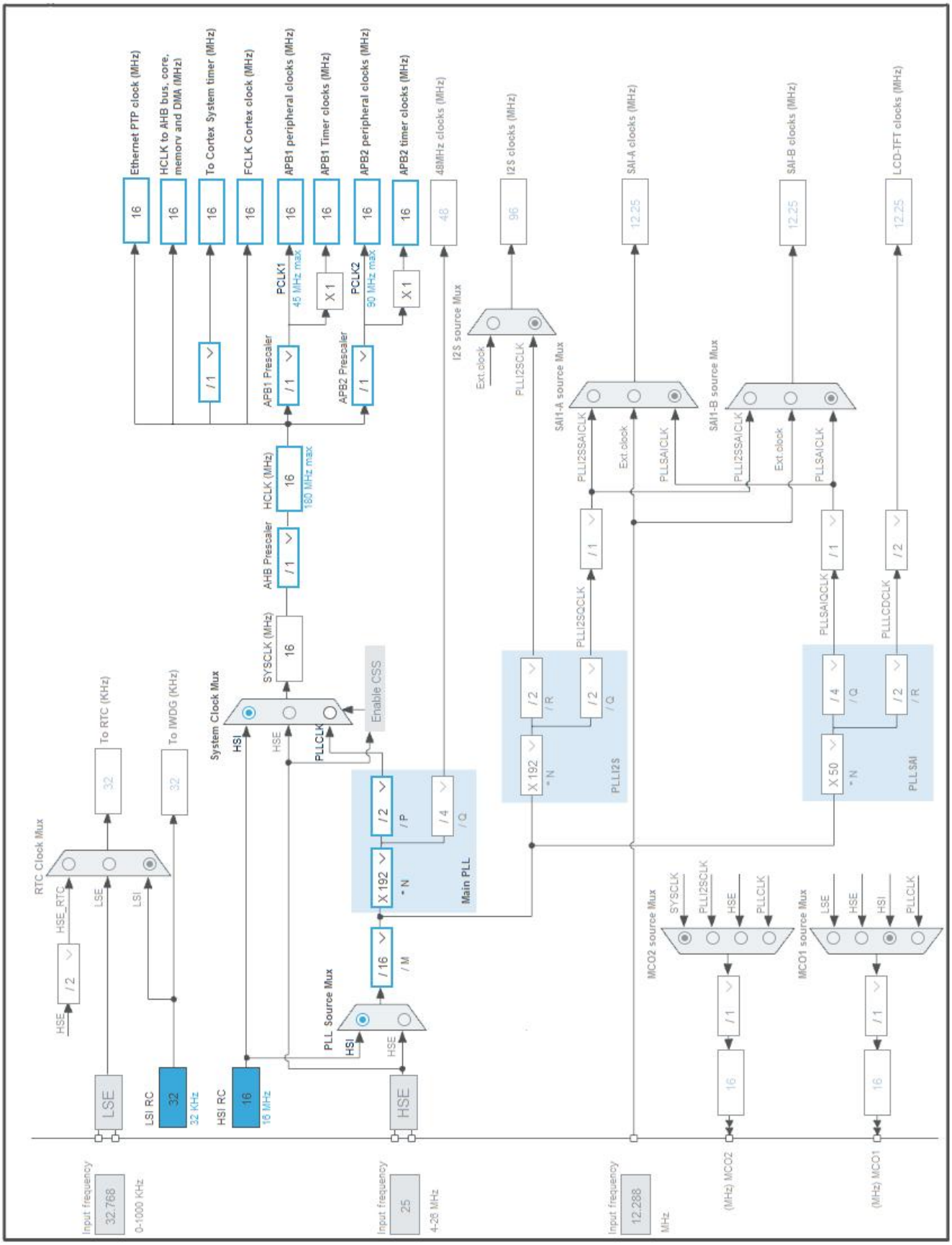
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SPI4_SCK	
4	PE5	I/O	SPI4_MISO	
5	PE6	I/O	SPI4_MOSI	
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
36	PA2	I/O	USART2_TX	
37	PA3	I/O	USART2_RX	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC_OUT1	
42	PA6 *	I/O	GPIO_Output	
44	PC4	I/O	ADC1_IN14	
45	PC5	I/O	ADC2_IN15	
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDD	Power		
100	PA8 *	I/O	GPIO_Output	
101	PA9 *	I/O	GPIO_Output	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
120	VSS	Power		
121	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
130	VSS	Power		
131	VDD	Power		
133	PB3 *	I/O	GPIO_Output	
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429ZITx
Datasheet	DS9405_Rev9

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

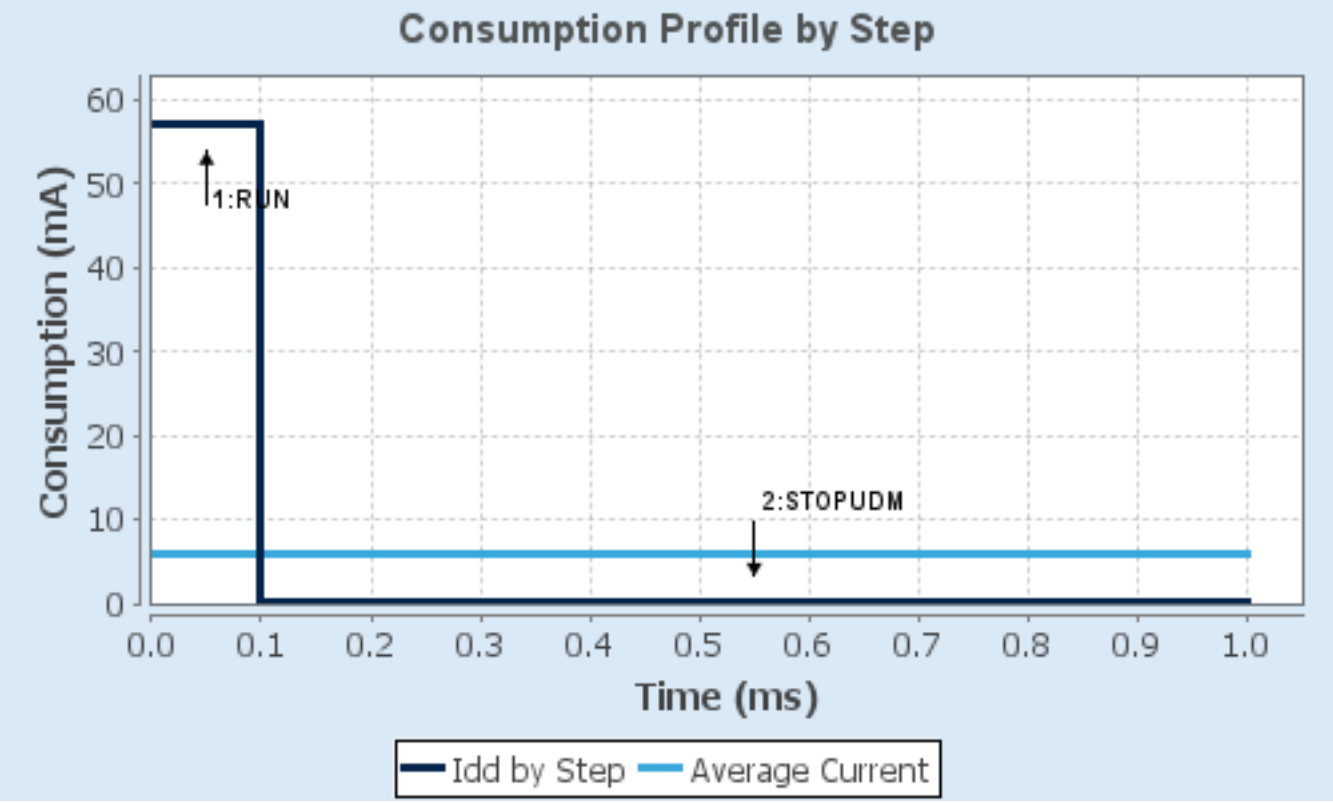
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	57 mA	100 µA
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	97.48	104.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	5.79 mA
Battery Life	24 days, 10 hours	Average DMIPS	225.0 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
60
50
40
30
20
10
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Software Project

2.1. Project Settings

Name	Value
Project Name	PM4_Firmware
Project Folder	C:\Users\roche\OneDrive\Dokumente\ZHAW\Sem_6\PM4\PM4_Radar\Code\PM
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_ADC2_Init	ADC2
6	MX_TIM2_Init	TIM2
7	MX_USART2_UART_Init	USART2
8	MX_DAC_Init	DAC
9	MX_SPI4_Init	SPI4
10	MX_TIM6_Init	TIM6

3. Peripherals and Middlewares Configuration

3.1. ADC1

mode: IN14

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Dual regular simultaneous mode only ***
DMA Access Mode	DMA access mode 2
Delay between 2 sampling phases	5 Cycles

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**2 ***
External Trigger Conversion Source	**Timer 2 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 14
Sampling Time	**15 Cycles ***
Rank	**2 ***
Channel	Channel 14
Sampling Time	**15 Cycles ***

WatchDog:

Enable Analog WatchDog Mode	false

3.2. ADC2

mode: IN15

3.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Dual regular simultaneous mode only ***

DMA Access Mode	**DMA access mode 2 ***
Delay between 2 sampling phases	5 Cycles

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Enabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
Rank	1
Channel	Channel 15
Sampling Time	**15 Cycles ***

WatchDog:

Enable Analog WatchDog Mode	false

3.3. DAC

mode: OUT1 Configuration

3.3.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	**Timer 6 Trigger Out event ***
Wave generation mode	Disabled

3.4. RCC

3.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 3
Power Over Drive	Disabled

3.5. SPI4

Mode: Full-Duplex Master

3.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**8.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

3.6. SYS

Timebase Source: SysTick

3.7. TIM2

Clock Source : Internal Clock

3.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**83 ***
Counter Mode	Up

Counter Period (AutoReload Register - 32 bits value)	**99 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	**Update Event ***

3.8. TIM6

mode: Activated

3.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**83 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**7 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

3.9. USART2

Mode: Asynchronous

3.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PC5	ADC2_IN15	Analog mode	No pull-up and no pull-down	n/a	
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
SPI4	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PA6	GPIO_Output	Output Push Pull	**Pull-up ***	Low	
	PA8	GPIO_Output	Output Push Pull	**Pull-down ***	Low	
	PA9	GPIO_Output	Output Push Pull	**Pull-down ***	Low	
	PB3	GPIO_Output	Output Push Pull	**Pull-down ***	Low	

4.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	**Very High ***
USART2_TX	DMA1_Stream6	Memory To Peripheral	Low
DAC1	DMA1_Stream5	Memory To Peripheral	**Medium ***

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

USART2_TX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

DAC1: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 stream5 global interrupt	true	0	0
DMA1 stream6 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM2 global interrupt	unused		
USART2 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream5 global interrupt	false	true	true
DMA1 stream6 global interrupt	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
DMA2 stream0 global interrupt	false	true	true

*** User modified value**

5. System Views

5.1. Category view

5.1.1. Current

6. Docs & Resources

Type	Link