

TP5

Exercise 1: Simulation of the AND gate with 03 inputs: $F = A \text{ and } B \text{ and } C$

Follow these steps to simulate this function:

1. On Quartus, create a new project (Project Name: TP5) in your work directory, and select the Device Family as in the previous labs. In the **EDA Tools setting** page, select **ModelSim Altera** on **simulation line**

(a) Quartus Prime Lite Edition

(b) New Project Wizard

Directory, Name, Top-Level Entity

What is the working directory for this project?
C:/MyProject/Lab0_vhdl

What is the name of this project?
MyFirstProject

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
MyFirstProject

Use Existing Project Settings...

(c) New Project Wizard

Family, Device & Board Settings

Device family: MAX10 (DA/DF/DC/SA/SC)

Device: MAX10 DA

Package: FBGA

Pin count: 484

Core speed grade: /

Name filter:

Show advanced devices: ☒

Available devices:

Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Emb
10M25DAF484C7G	1.2V	24960	360	360	691200	110
10M25DAF484I7G	1.2V	24960	360	360	691200	110
10M40DAF484C7G	1.2V	40368	360	360	1290240	250
10M40DAF484I7G	1.2V	40368	360	360	1290240	250
10M50DAF484C7G	1.2V	49760	360	360	1677312	288
10M50DAF484I7G	1.2V	49760	360	360	1677312	288

(d) New Project Wizard

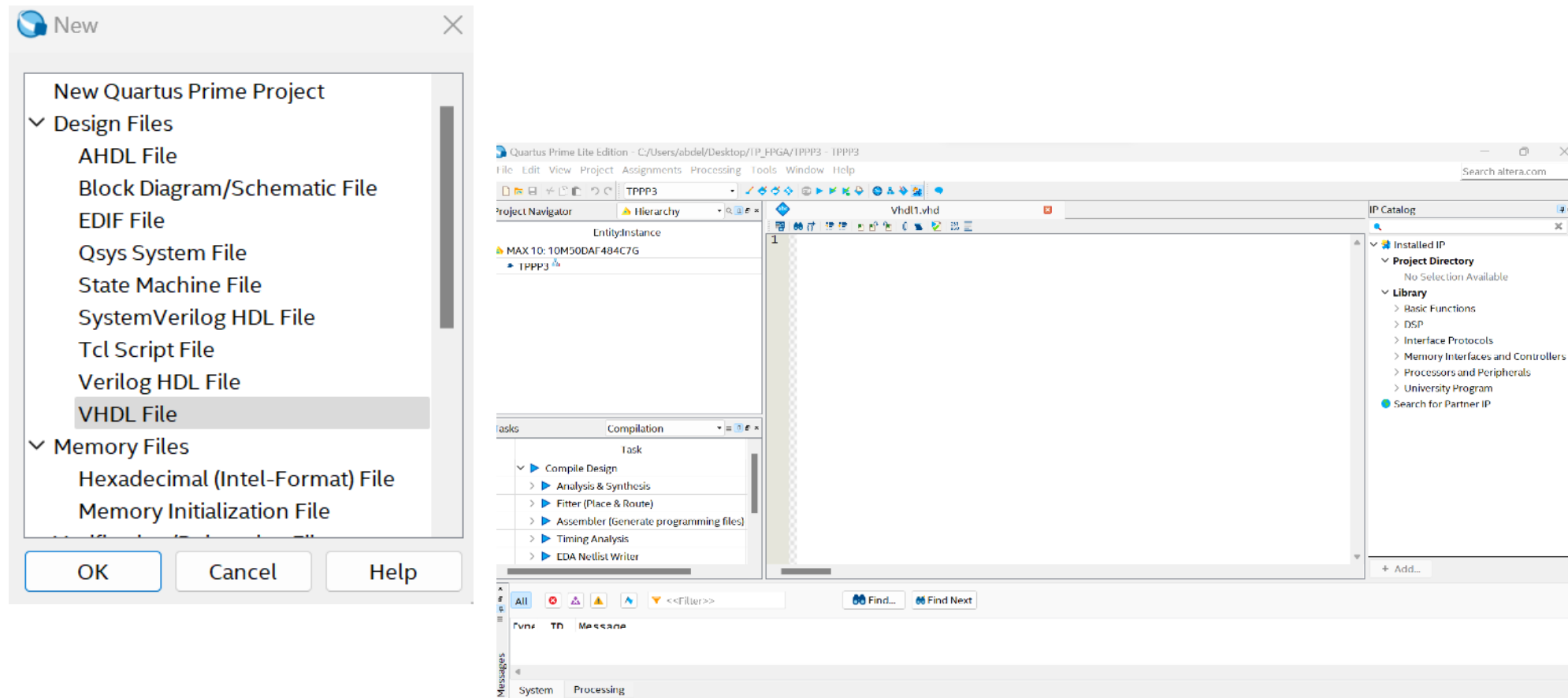
EDA Tool Settings

Specify the other EDA tools used with the Quartus Prime software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entr...	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Alti	Verilog HDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

2. Now, create a description of the function F (And gate with 03 inputs):
File -> New ->VHDL File (TP5 name of the VHDL file)



3. Complete the VHDL file as the given code:

```
1  library IEEE;
2  use ieee.std_logic_1164.all;
3
4  Entity TP5 is
5  |
6  Port ( A,B,C      : in STD_LOGIC;
7        F: out STD_LOGIC);
8  |
9  end TP5;
10
11 architecture Behavioral of TP5 is
12 |
13 |
14 |   F <= A and B and C;
15 |
16 | end Behavioral;
17
```

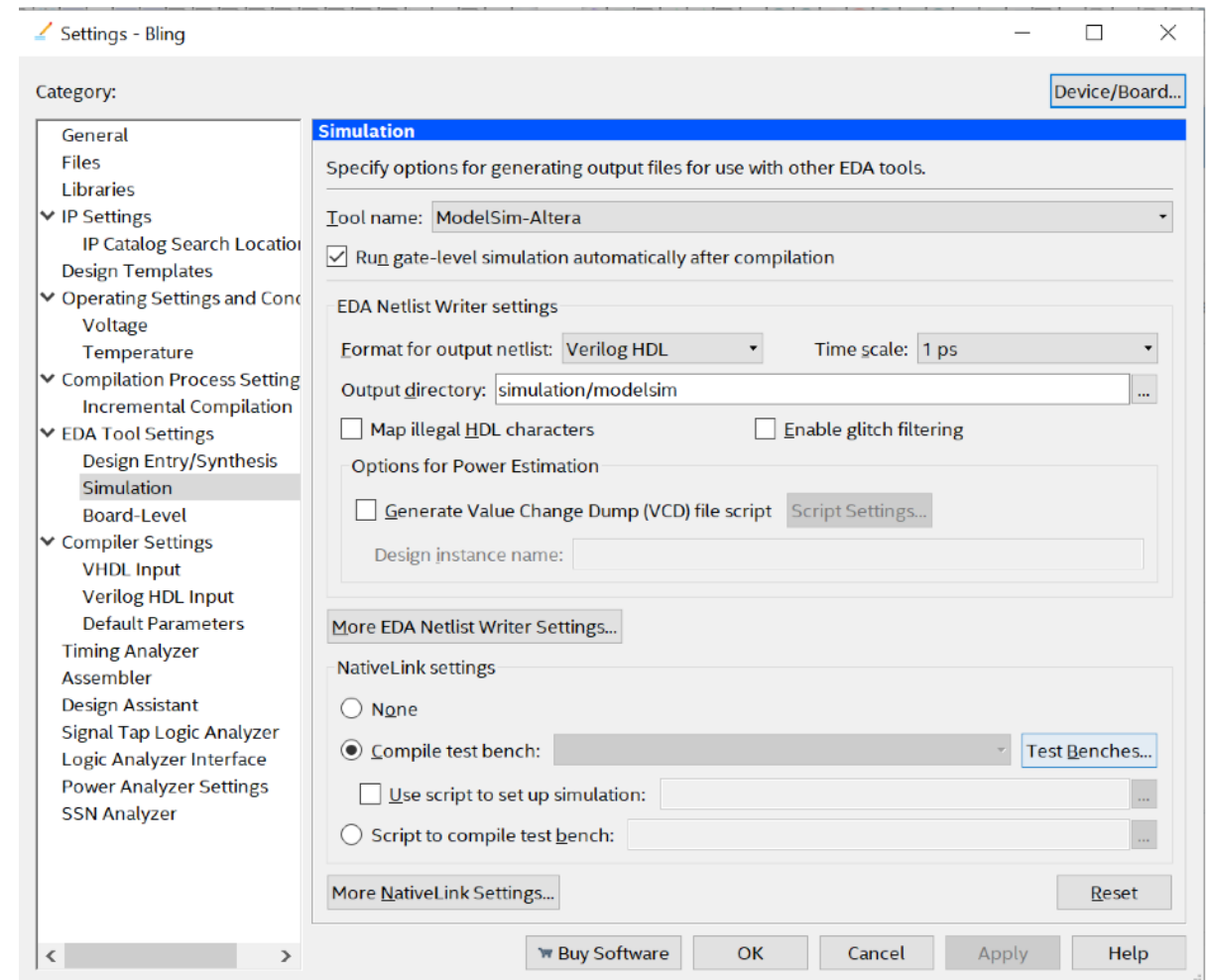
4. Compile your code to check that there aren't errors
5. To simulate you code, create a testbench file. It's another VHDL file:
File -> New -> VHDL file -> complete as a code given below.
save as TPAnd3TP, don't forget to check the box "Add the file to the current project"

```
1  library IEEE;
2  use ieee.std_logic_1164.all;
3
4  entity TBAnd3TP is
5  end TBAnd3TP;
6
7  architecture DESCRIPTION of TBAnd3TP is
8  |
9  | component TP5
10 | Port ( A, B, C      : in STD_LOGIC;
11 |       F : OUT std_logic);
12 | end component;
13 |
14 | -- Inputs
15 | signal A : std_logic := '0';
16 | signal B : std_logic := '0';
17 | signal C : std_logic := '0';
18 | -- Outputs
19 | signal F : std_logic;
20 |
21 | Begin
22 |
23 | Uut : TP5 port map
24 | (
25 |   A => A,
26 |   B => B,
27 |   C => C,
28 |   F => F);
29 |
30 | stim_proc: process
31 | begin
32 |
33 |   wait for 100 ns;
34 |
35 |   A<='1'; B<='0'; C<='1'; wait for 20 ns;
36 |   A<='0'; B<='1'; C<='0'; wait for 30 ns;
37 |   A<='1'; B<='1'; C<='1'; wait for 40 ns;
38 |
39 |   wait;
40 | end process;
41 |
42 | end;
43
```

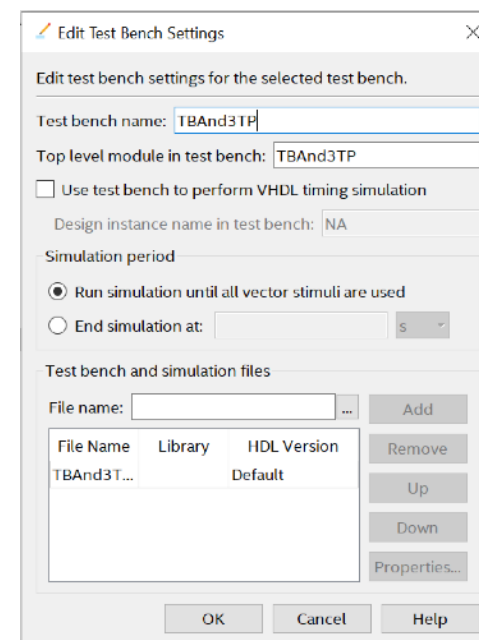
6. Compile this code to check that there aren't errors

7. To run simulation, follow these steps:

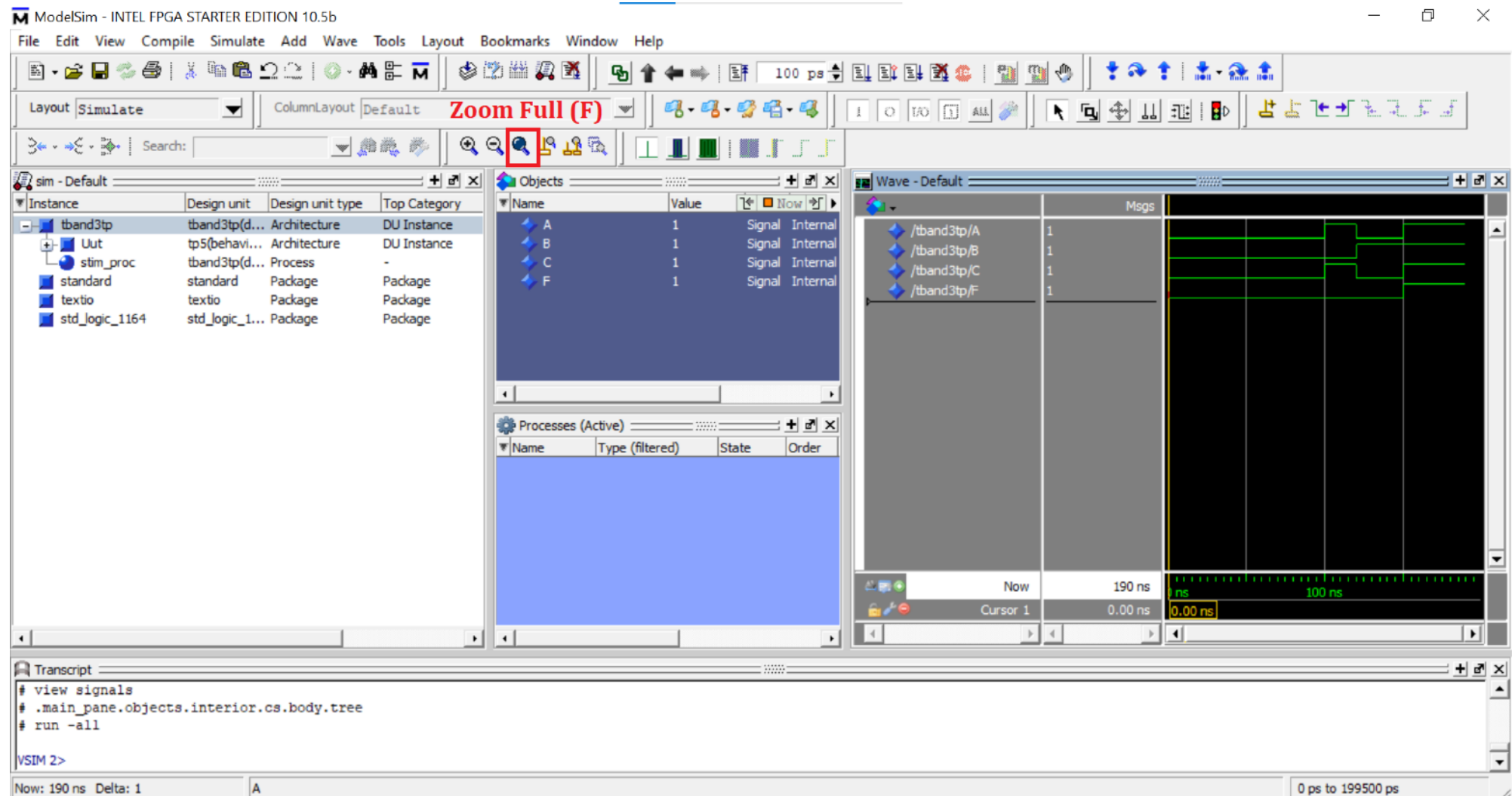
- Assignment -> Settings ..
- In the page Setting-Bling -> Simulation
- In Tool name -> ModelSim-Altera
- In Format for netlist -> Verilog HDL



- Click on Test Benches and a window of New Test Bench Setting appear. Write the name of the test bench file
- In Test Benches and simulation files click on TPAnd3TP.vhd -> ADD -> ok -> ok -> Apply ->ok



- Select Tools ->Tools → Run Simulation (to launch ModelSim)
- A ModelSim window appears. Click on “Zoom full” to visualize better the simulation



- Check the output F according the inputs A,B and C
- In your testbench file add this line in Stimulus process: A=0, B=1, C=1 for 50ns

Exercise 2: Simulation of the binary counter from 0 to 9 with clock period = 20ns

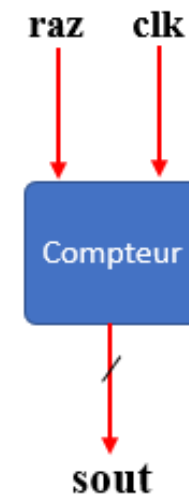
1- Create a New VHDL code and complete the code given below

```
entity compteurRAZ is
Port ( clk:      in STD_LOGIC ;
      raz :      in STD_LOGIC ;
      sout :      out STD_LOGIC_VECTOR (3 downto 0));
end compteurRAZ;

architecture Behavioral of compteurRAZ is

SIGNAL s_sout : STD_LOGIC_VECTOR (3 downto 0) :=“0000”;

-----
```



Complete this VHDL code

2- To simulate the counter, create a testbench file in which, we should:

- Set the clk-period to 20ns
- Create a process to generate a clk signal
- In stimulus process, add these instructions:
raz=1 and wait for 100ns
raz=0 and wait for 50ns
raz=1 and wait for 20ns
raz=0 and wait forever

Exercise 3: Simulation and implementation of the counter from 0 to 9 with clock period =1s and display the result on 7-segment displayer

Exercise 4: Simulation and implementation of the counter from 0000 to 9999 with clock period 1s and display the result on 7 segment displayer

```
1  library IEEE;
2  use ieee.std_logic_1164.all;
3  use ieee.std_logic_unsigned.all;
4  use ieee.numeric_std.all;
5
6  Entity CompteurRAZSig is
7  |
8  | Port ( clk, raz      : in STD_LOGIC;
9  |       SEG1: out STD_LOGIC_VECTOR(6 downto 0)
10 |       SEG2: out STD_LOGIC_VECTOR(6 downto 0)
11 |       SEG3: out STD_LOGIC_VECTOR(6 downto 0)
12 |       SEG4: out STD_LOGIC_VECTOR(6 downto 0));
13 | end CompteurRAZSig;
14 |
15 |
16 | Architecture Behavioral of CompteurRAZSig is
17 | |
18 | | signal INPUT1 : STD_LOGIC_VECTOR(3 downto 0) := "0000";
19 | | signal INPUT2 : STD_LOGIC_VECTOR(3 downto 0) := "0000";
20 | | signal INPUT3 : STD_LOGIC_VECTOR(3 downto 0) := "0000";
21 | | signal INPUT4 : STD_LOGIC_VECTOR(3 downto 0) := "0000";
22 | | signal cnt : integer := 0;
23 | |
```

