CSCI 113 (Intro. Computer Organization) **Exam 1** (100 pts) **Fall 2022**

//submit one email with attached file(s) to jpark@csufresno.edu. //Email title as CS113-Exam1-yourName

(25pts) **1.** (a) What is the input width of the decoder used in a 32x1 multiplexer?
(b) Draw a schematic diagram of 3-input XOR component (using only 2-input basic gates) based on the structural design.
(c) Consider the 1-bit ALU and show control signal names and values (total 4 bits) for Add, Sub, and Nor operations.
(d) Prove that the following two logic equations are equivalent: XOR = (A+B) · (A·B); XOR = (A·B) + (A·B)
(e) Write the overflow checking logic.

(20pts) **2.** Consider the following instruction mix and CPI values for computers M1 (rate=500 MHz) and M2 (rate=600 MHz):
Type1(50%): CPI_M1=1, CPI_M2=2; Type2(30%): CPI_M1=2, CPI_M2=1; Type3(20%): CPI_M1=3, CPI_M2 =4;
(a) Compute CPU execution times of M1 and M2, and answer which computer is how much times faster than the other.
(b) Compute MIPS rates of M1 and M2.

(10pts) **3.** Consider a computer C1(rate=800 MHz) on which a benchmark program execution takes 10 sec.
A design team is developing a new computer C2 aiming the double performance by increasing the clock rate with the cost of increased clock cycles with the factor of 2. What would be the clock rate of computer C2?

(15pts) **4.** MIPS ISA: Assume data (1A2B3C4D)hex and (D1C2B3A4)hex are stored in memory at address 0 and 4, respectively.
Consider the following 3 consecutive instruction executions: lw $t1, 2($zero); sw $t1, 4($zero); lw $t2, 3($zero);
(a) Show the final contents of $t1 and $t2 in hex number.
(b) How many memory accesses are made?
(c) Write a MIPS assembly code for negating $t2.

(15pts) **5.** Consider the following MIPS assembly code segment for implementing a loop:

```
Loop: lw   $t1, 12($s1);
      bne  $s2, $t1, Done;
      addi $s1, $s1, 4;
      j Loop;
      sll $t1, $s1, 3;
Done:
```

(a) Write the MIPS machine code in hex number for the 1st instruction (lw…).
//use: opcode=35, $s1(17), $t1(9)
(b) Write the MIPS machine code in hex number for the 2nd instruction (bne…).
//use: opcode=5, $t1(9), $s2(18)
(c) Write the MIPS machine code in hex number for the 5th instruction (sll…).
//use: opcode=0, function_code=0

(15pts) **6.** Consider the global pointer ($gp) value 10008000(hex).
(a) Write a MIPS assembly code for loading a word size data stored at memory address 10000380(hex) to register $t1.
(b) Compute and show the data address (in hex number) from the following sw instruction: sw $t1, 8034h ($gp);