CSCI 113 (Intro. Computer Organization) Exam 2 Spring 2022

//submit photo files to jpark@csufresno.edu. //Write email subject as CS113-Exam2-yourName.

(40 pts.) 1. Computer arithmetic

(a) Draw a schematic diagram of 4-bit ALU for {and, or, add, sub, nor, slt}.
In your diagram, please use a blank box for 1-bit ALU and show all inputs/outputs with names.

(b) Consider the 4-bit ALU in (a) and write control signal names/values for ***slt*** operation and explain the mechanism.

(c) Perform 4-bit Booth's multiplication for (-5)*(-7) and show registers' contents step by step for only the first 2 iterations.

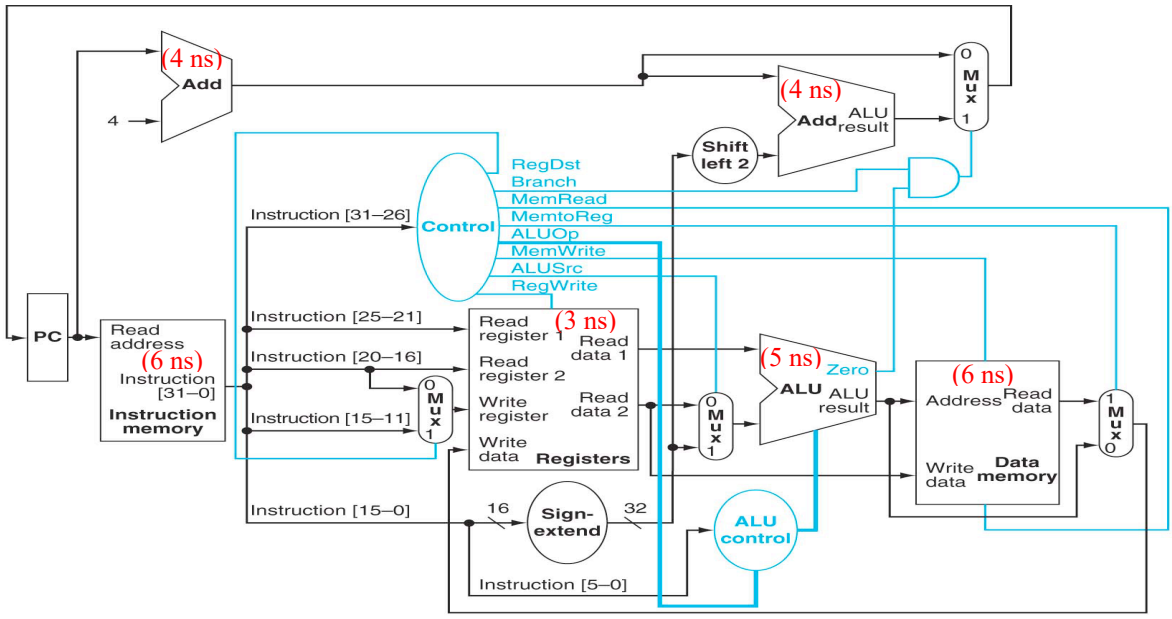
(d) Draw the hardware components for unsigned number division with 4-bit operands. Show register names.

(e) Perform 4-bit non-restoring division for (11/5) and show registers' contents step by step for only the first 2 iterations.

(20 pts.) 2. CPU – single-cycled implementation

(a) Compute the critical path time (in ns) for each of the following three instructions: ***sub, lw***, ***beq***

(b) For ***sub*** instruction, show control signal values for: RegDst, ALUSrc, MemtoReg, RegWrite



(40 pts.) 3. CPU – multi-cycled implementation

(a) Consider the following instruction sequence to be executed and compute the speedup of the multi-cycled CPU (shown in the following diagram) over the single-cycled CPU (shown in the diagram in #2).
sub $s5, $s2, $s4; **lw** $s3, 10($s1); **or** $s7, $s2, $s4; **beq** $s2, $s4, 100;

(b) Write the micro operations for the 2nd cycle of a ***beq*** instruction.

(c) Show all control signal names and values used in the 2nd cycle of a ***beq*** instruction execution.

(d) Show all control signal names and values used in the 4th cycle of a ***sub*** instruction.

(e) Draw the diagram of the hard-wired control unit (hardware component).