

1. M_1 rate = 500 MHz time = 30 sec $M_2 = 3$ times faster

$$\text{rate } M_2 = \frac{(30 \times 500 \text{ MHz})}{2} = \frac{15,000 \text{ n}}{2} = 7,500 \text{ MHz} = \frac{500}{\cancel{10}} \times 30 = \frac{500 \times 30}{1000} = 15000$$

$$\frac{5 \text{ clockcycles}}{10} M_1 = \text{rate } M_2 = \Rightarrow \boxed{7.5 \text{ GHz}}$$

2. bne op code = 5 sll opcode = 0 sll_funcode = 0, \$s1(7)

bne \$s1 \$s2

5	17	18					
01.01	10001	1001000	00000	00000	00000	00000	
5	8	12	4	\emptyset	\emptyset	\emptyset	\emptyset

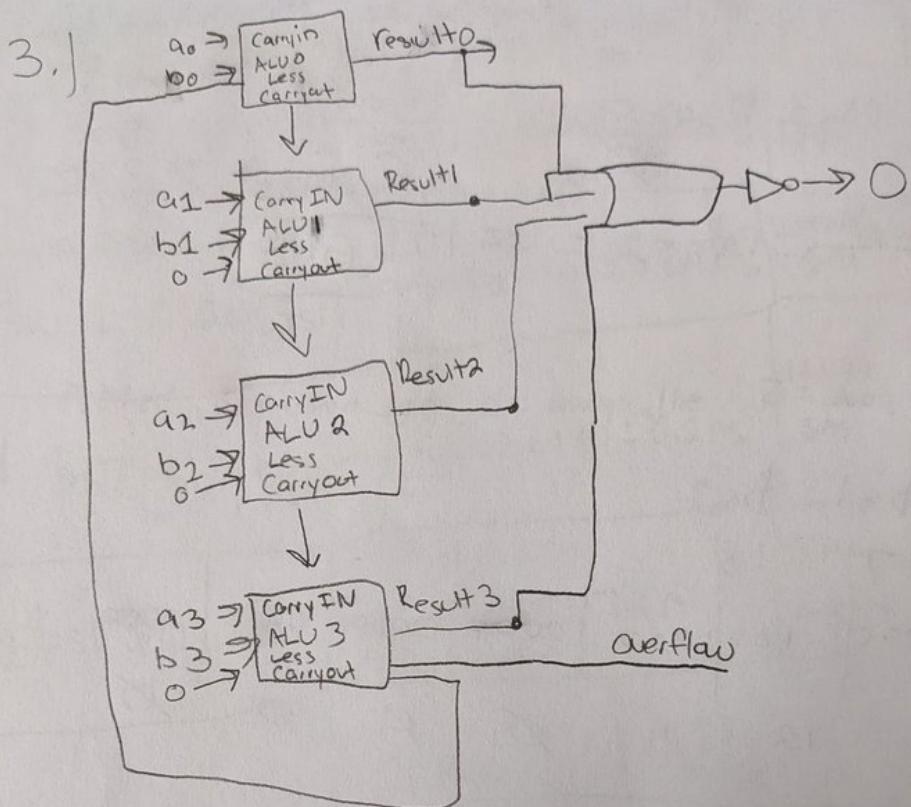
$\boxed{581C410000}$

10001

b.) sll \$s2 \$s1 4

0	0	18	17	4			
0000	0000	10010	10001	0100	0000	0000	0000
0	0	9	4	5	0	0	0

$\boxed{00945000}$



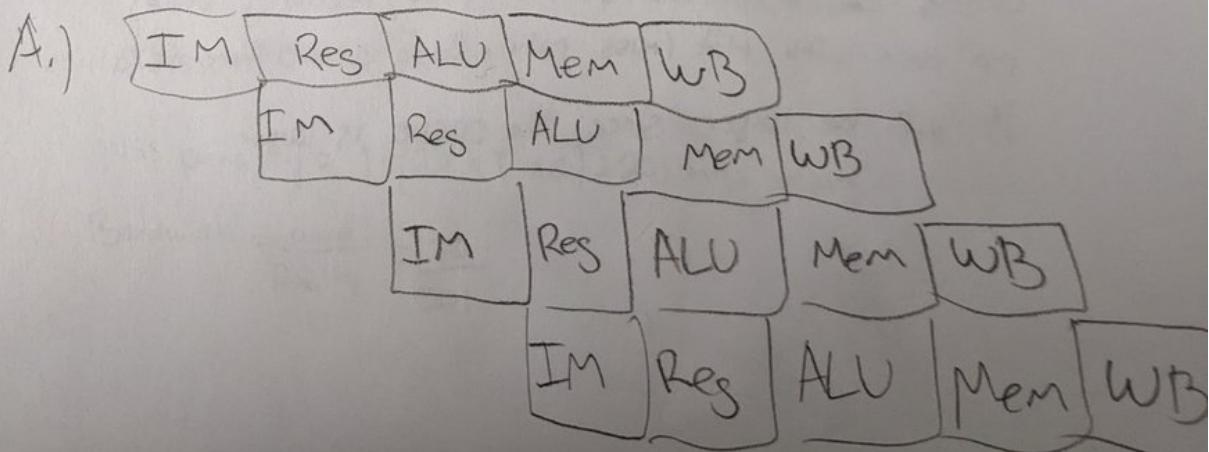
b. $-3 + -5$
MD \swarrow MQ

0611
1000
+ 1
1101 = 2s comp

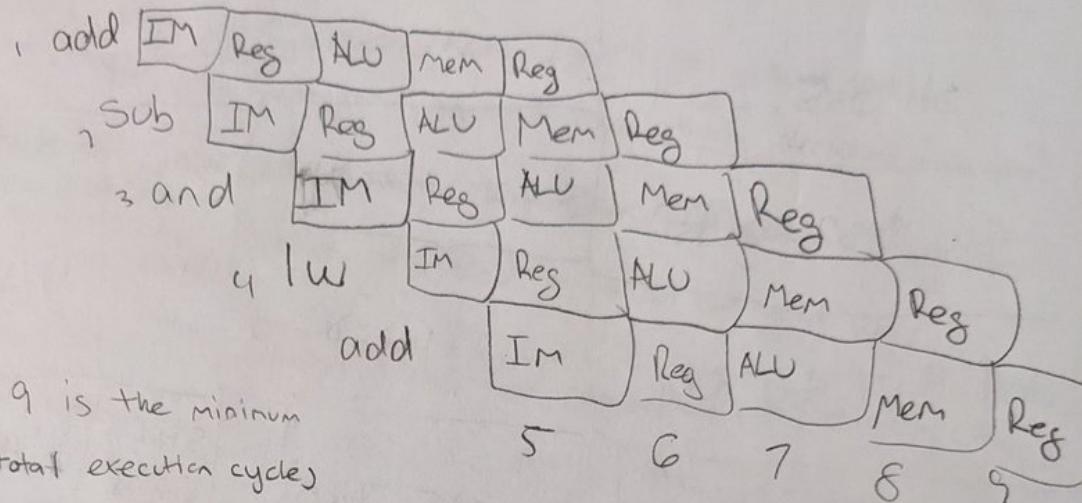
$$\begin{array}{r}
 \text{MD} \quad \text{AC} \quad \text{MQ} \quad \text{MQ-1} \\
 \begin{array}{r}
 0011 \quad 0000 \quad 1001 \\
 + 1101 \\
 \hline
 1101 \quad \text{overflow} \rightarrow 0
 \end{array} \\
 \begin{array}{r}
 \text{||} \\
 \text{|||} \quad 0 \quad | \quad 1100 \quad 1 \quad 771 \\
 + 0011 \\
 \hline
 1000 \quad 1100 \quad | \\
 \text{00011100} \rightarrow 0 \quad 771 \\
 000\ 01110 = 16
 \end{array}
 \end{array}$$

L1. lw \$33, \$10 \$s1	Single Cycle $S+1+1.2+5=12.2\text{ns}$	Multicycle $S+1.2+1=7.2\text{ns}$	Pipeline $5(3 \times 1) = 15\text{ns}$
S11 \$s5, \$s2 4	$S+1+1.2+5+1.2=18.4\text{ns}$	N/A	N/A
SW \$s2,20(\$s1)	$S+1.2+1+1.2=8.4\text{ns}$	$S+5+5$ 15ns.	$S+1.2$ 6.2 ns.
and \$s7, \$s1, \$s4	$S+1.2+1+1=8.2\text{ns}$	1+1+1 3ns	N/A
beq \$s1 \$s2 label:	$1+1.2+5=7.2\text{ns}$	$S+1.2$ 6.2 ns.	N/A
J100	N/A	N/A	N/A

5.1 MIPS Pipeline



5.B.) IM - Reg → ALU - Mem - Reg



6.) Increased block size

- a) Pros; By increasing block size we will have more space which should result in less misses

Cons; Increasing block size could be problematic because cache can only hold so much so recurring values can mess with hit/miss ratio. Also when there is a miss it will be larger since the cache is larger

6.A. Increased Associativity

Pros: We will have less Issues per cache portion

other other methods: Increased associativity decreases miss rates

Cons: It will have diminishing Returns the more it searches
and it handles the CPU in a not so good way.

6.) B. Two Alternatives: The first alternative is increasing the cache. The other way is involving the L2-cache.

7. a.) 2

b.) 4

c.) 18

d.) 64

8, a.) block 20 w DRam 20 clock data transfer = 2
address 1 clock

$$\text{Miss penalty} = 1 + [20 \times 2] = 20 \text{ Miss penalty}$$

$$\text{Bandwidth} = \frac{\text{word}}{\text{Penalty}} = \frac{20}{201}$$

8.b.) effective CPI = Ideal CPI + $\frac{\text{miss cycle}}{\text{width}}$
+ cache hits

$$1/S = 40\%$$

$$I \text{ cache} = 5\% \quad \text{Effective CPI} = 3 + (.05 * 100) + (.40 + .10 * 100)$$

$$D \text{ cache} = 10\%$$

$$\text{miss penalty} = 100 \text{ cycles}$$

$$\text{Ideal CPI} = 3$$

$$\boxed{\text{Effective CPI} = 58}$$

$$3 + 5 + 50$$