Project 1

Problem 1: (This problem is not related to SystemVerilog)
Design a sequential circuit S1 with the following requirements
a) The combinational logic part for the next state function should contain at least 3 NAND gates, 2 XOR gates and 2 OR gates.
b) The number of the flip-flops should be at least 4.
c) The sequential circuit should have at least an output.
d) Make sure that your design be different from those used by other students. If your design is identical to a design used by other students, you will be asked to revise your design and redo the work.

Instructions for Problem 1:
1) Draw your sequential circuit S1.
2) Create the next state function table for S1.
3) Draw the state transition graph of S1 including all the POSSIBLE states.
4) Figures should be plotted by using a professional software tool. Scanned or cut/paste hand drawn figures and writing are not acceptable.

Problem 2:
1) Write the SV code for a 2^n to n priority encoder in the dataflow model (continuous assignments)
2) Write the SV code for a 2^n to n priority encoder in the algorithmic model (always_comb).

Problem 3:
3) Write the SV code for a 16-bit carry look ahead adder in the dataflow model (continuous assignments)
4) Write the SV code for a 16-bit carry look ahead adder in the algorithmic model (always_comb).

Problem 4:
1) Write the SV code for a circuit whose 32-bit output is formed by shifting its 32-bit input three positions to the right and filling the vacant positions with the bit that was in the MSB before the shift occurred (shift arithmetic right).
2) Write the SV code for a circuit whose 32-bit output is formed by shifting its 32-bit input three positions to the left and filling the vacant positions with 0 (shift logical left).

Problem 5:
1) Write the SV code for a 6-bit Binary-to-Gray code converter in the dataflow model (continuous assign)
2) Write the SV code for a 6-bit Gary-to-Binary code converter in the algorithmic model (always_comb).

Problem 6: A comparator is a logic macro circuit that compares the magnitude of two n-bit binary operands. A 16-bit comparator determines if a 16-bit vector a[15:0] is equal to a 16-bit vector b[15:0].
5) Write the SV code for a 16-bit comparator in the dataflow model (continuous assignments)
6) Write the SV code for a 16-bit comparator in the algorithmic model (always_comb).

Project Instructions for Problems 2-6:

1. For each design, verify its correctness using your testbench with a simulator.
2. You should use the new SV statements instead of the old Verilog statements.
3. Turn in your report and code to the D2L by the deadline.
4. Your report must contain at least:
   - The SV code with the legible results from the testbench
   - Your code should be packaged and organized with the related task names.
5. Only one report is needed for each group. Indicate your email on the first page of your report.