Attendance number

18

A Student Camp

https://sites.google.com/view/quantumsite/home/student-camp-2025

A chance to study the quantum in ML

Selected participants will receive $300 to compensate for their time and effort.

When you file out the form:

Which professor recommended you participate in this student camp: Dr. Yong Shi

Deadline of Application: *Feb 21, 2025*

Dr. Yong Shi yshi5@kennesaw.edu with questions.

Midterm Review:

Chapter covered: 1~ 2 (slides and quiz and assignment)

Chapter1(Lecture 1-4):

Basic knowledge about the computer: computer performance, execute time, CPI and so on (for write response, if it is a calculation problem, you need to write down all the steps to get the full points instead of just final result)

$$\text{CPU Time} = \text{CPU Clock Cycles} \times \text{Clock Cycle Time}$$

$$= \frac{\text{CPU } clock\ cycles}{Clock\ Rate}$$

Midterm Review:

Chapter 2:

Lecture 5-10: basic knowledge about RISC-V set, arithmetic operation , data transfer operation, logical operation, Instructions for Making Decisions, Signed and Unsigned Numbers and so on.....

arithmetic operations: add, sub, addi (register or immediate number)

data transfer: lw, sw (register, memory address)

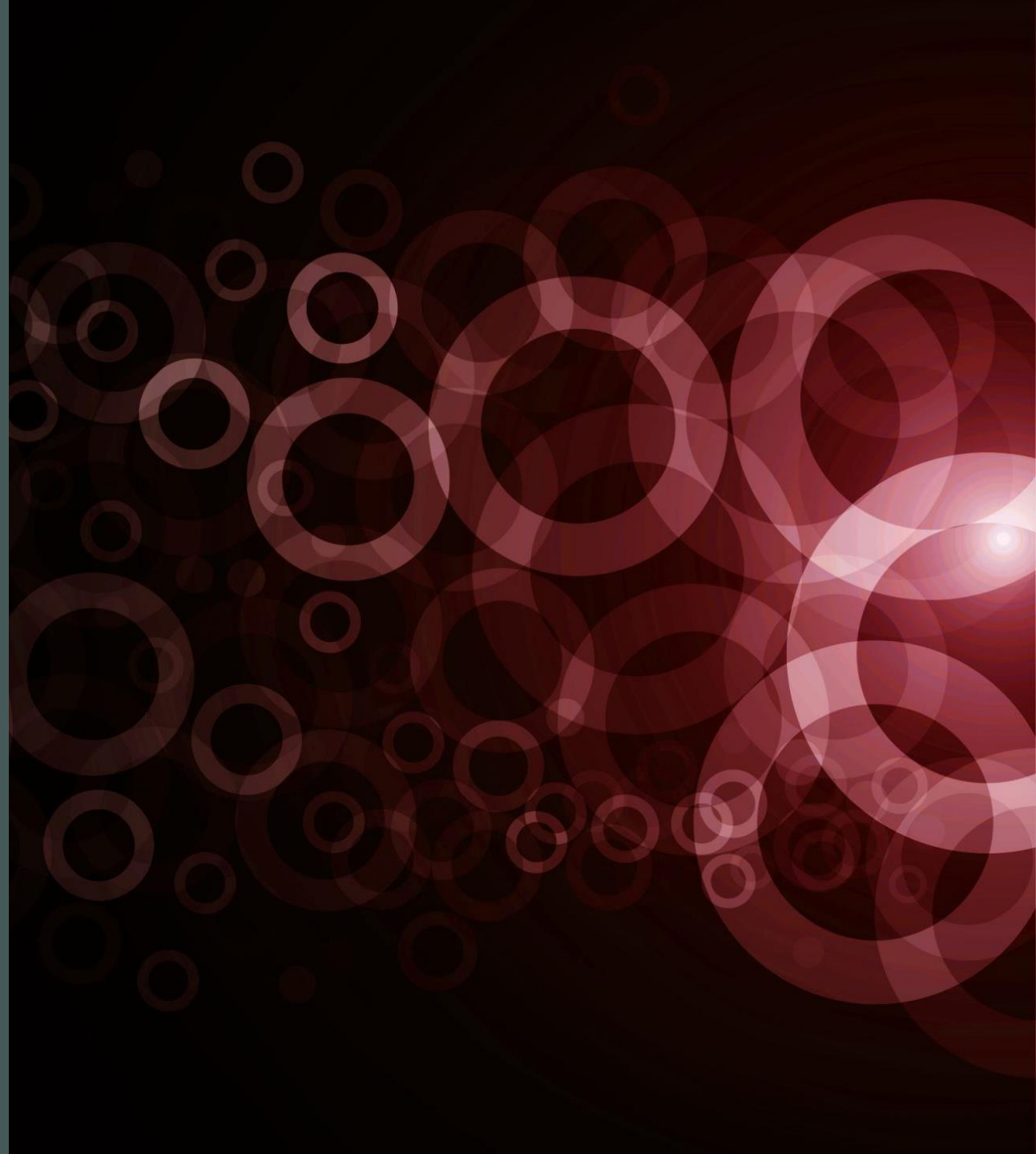
logical operations : slli (shift bit), AND (use as mask), OR(keep original), XOR (find the negative or use for the encryption)

Instructions for Making Decisions: conditional: bne, beq, bge, blt ; unconditional: jal, jalr

lui: load upper immediate

Mock_ Midterm

Chunlan Gao



Question 1

For the following C statement, write the corresponding RISC-V assembly code. Assume that the C variables f, g, and h, have already been placed in registers x5, x6, and x7 respectively. Use a minimal number of RISC-V assembly instructions. (**There is no subi in RISC-V**)

f = g + (h − 5);

Instruction	Points
addi x5, x7,-5	2
add x5, x5, x6	2

Question 3

For the following C statement, write the corresponding RISC-V assembly code. Assume that the variables f, g, h, i, and j are assigned to registers x5, x6, x7, x28, and x29, respectively. Assume that the base address of the arrays A and B are in registers x10 and x11, respectively.

B[8] = A[i-j]

Instruction	Points
sub t0, x28, x29	1
slli t0, t0, 2	1
add t0, x10, t0	1
lw t1, 0(t0)	2
Addi t2, 8	1
slli t2, t2, 2	1
add t2, x11, t2	1
sw t1, 0(t2)	2

Question 4

Assume the following register contents:

x5 = 0x1234, x6 = 0xABCD

For the register values shown above, what is the value of x7 in hex for the following sequence of instructions?(show your steps)

slli x7, x5, 4

AND x7, x7, x6

CRITERIA	POINTS
slli x7, x5, 4	1
And x7, x7, x6	3
Conversion to hexadecimal	1

slli x7, x5, 4

x5 = 0x00001234----> X7: 0x00012340

AND X7, X7 X6

X7: Binary: 0000 0000 0000 0001 0010 0011 0100 0000

AND X6: Binary: 0000 0000 0000 0000 1010 1011 1100 1101

Binary: 0000 0000 0000 0000 0010 0011 0100 000

X7=0x00002340 hex

Question 10

Find the shortest sequence of RISC-V instructions that extracts bits 16 down to 11 from register x5 and uses the value of this field to replace bits 31 down to 26 in register x6 without changing the other bits of registers x5 or x6. (Be sure to test your code using x5 = 0 and x6 = 0xffffffff. Doing so may reveal a common oversight.)

X5	0000	0000	0000	0000	0000	0000	0000	0000
X6	1111	1111	1111	1111	1111	1111	1111	1111
X6	0000	0011	1111	1111	1111	1111	1111	1111

```
# Step 1: Extract bits 16-11 from x5
addi x7, x0, 0x3F   # Load mask for bits 16 to 11 (0b111111)
slli x7, x7, 11     # Move mask to cover bits 16-11
and x28, x5, x7     # Extract bits 16-11 from x5
```

```
# Step 2: Move extracted bits to
position 31-26
slli x28, x28, 15   # Move bits from
16-11 directly to 31-26
```

```
# Step 3: Clear bits 31-26 in x6
lui x7, 0x03FFF     # Load upper part of
0x03FFFFFF
ori x7, x7, 0xFFF # Complete mask to clear bits
31-26
and x6, x6, x7      # Clear bits 31-26 in x6
```

```
# Step 4: Insert new bits into x6
or x6, x6, x28      # Merge extracted
bits into x6
```