NAND-AND NOR-OR

09:37

✱ Assignments :- B.1.b (using 90nm Foundry)

(I) B.1.b :-

a) 2 i/p NAND

b) 2 i/p NOR

c) 2 i/p AND

d) 2 i/p OR

✱ 2 i/p NAND, 2 i/p NOR Gates :-

2 i/p NAND | **2 i/p NOR**

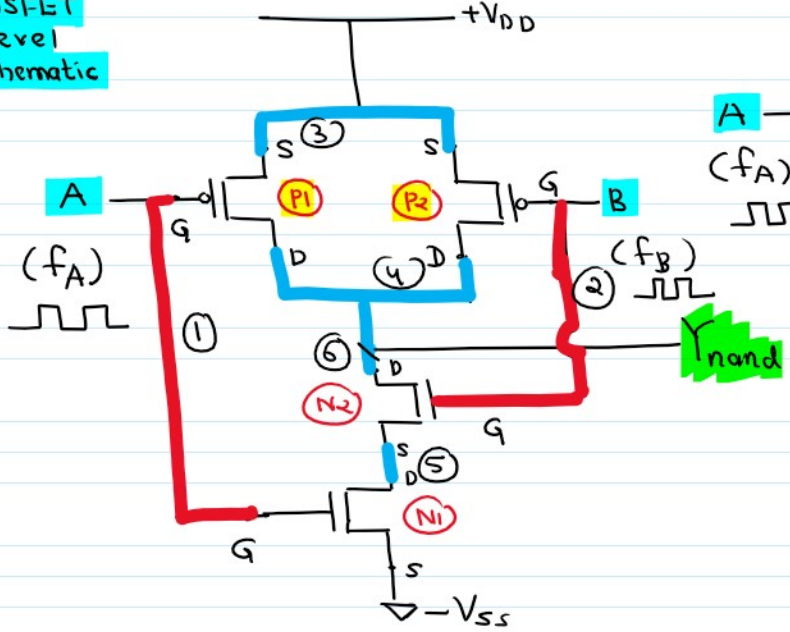
Symbols:

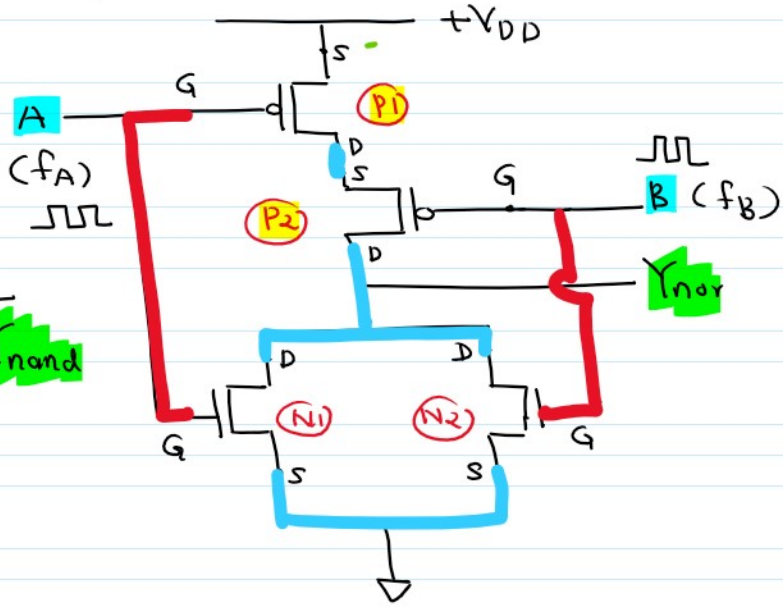
Expression:

$Y_{nand} = \overline{A \cdot B}$ — (P1//P2), (N1–N2)

$Y_{nor} = \overline{A + B}$ — (P1–P2), (N1//N2)

MOSFET Level Schematic





$f_A = \frac{1}{2} \cdot f_B$

$T_A \quad T_B$

$f_A = \frac{1}{2} f_B$

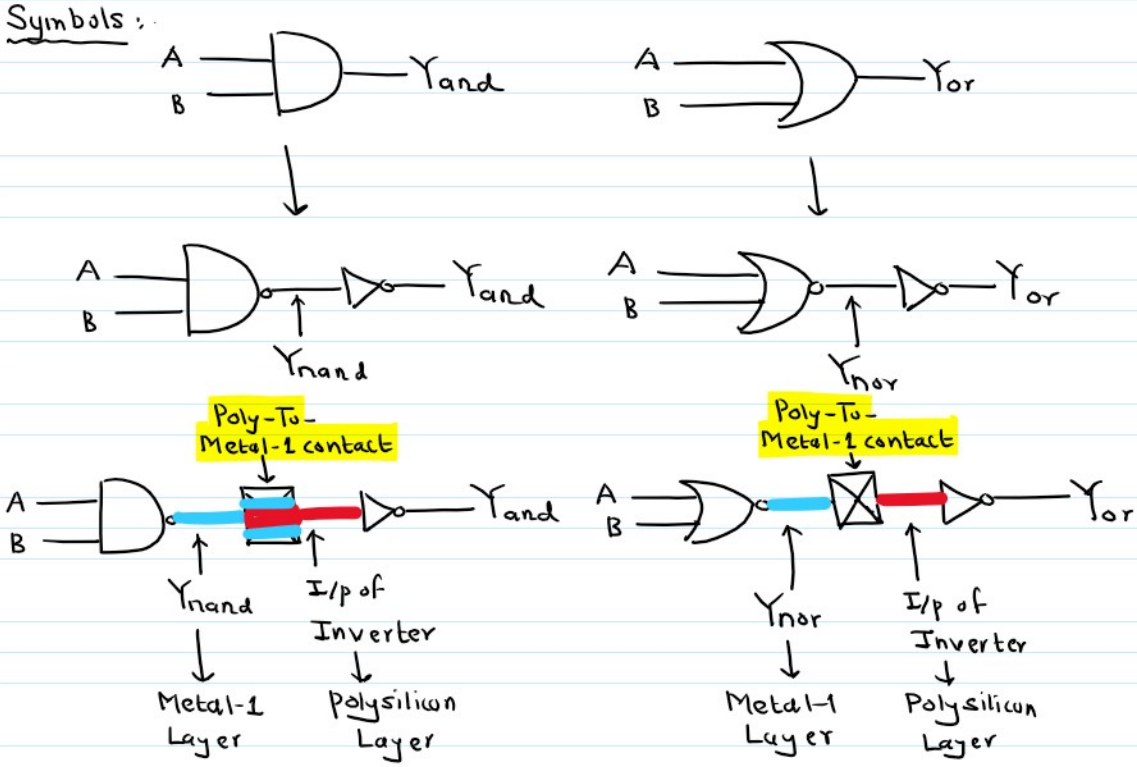
T_A T_B

A	B	Y_{nand}
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y_{nor}
0	0	1
0	1	0
1	0	0
1	1	0

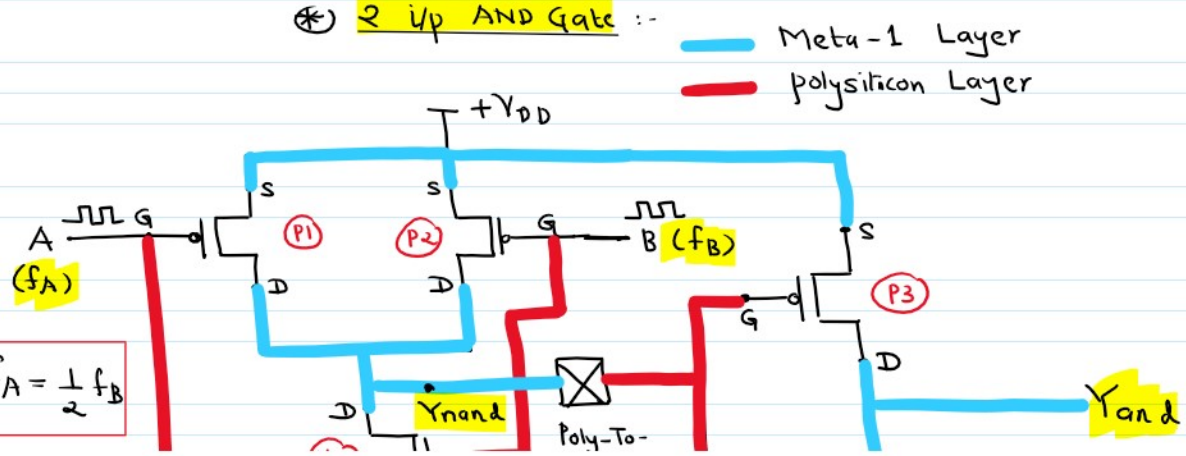
✱ 2 i/p AND, 2 i/p OR Gate:

Symbols:

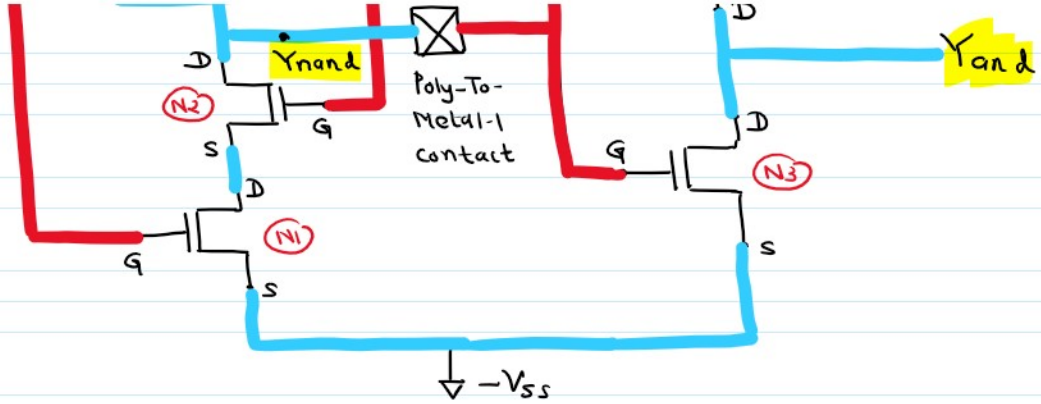


✱ MOSFET-Level Schematics for 2 i/p AND, 2 i/p OR Gate:-

✱ 2 i/p AND Gate:-



$f_A = \frac{1}{2} f_B$



✱ 2 ip OR Gate :-