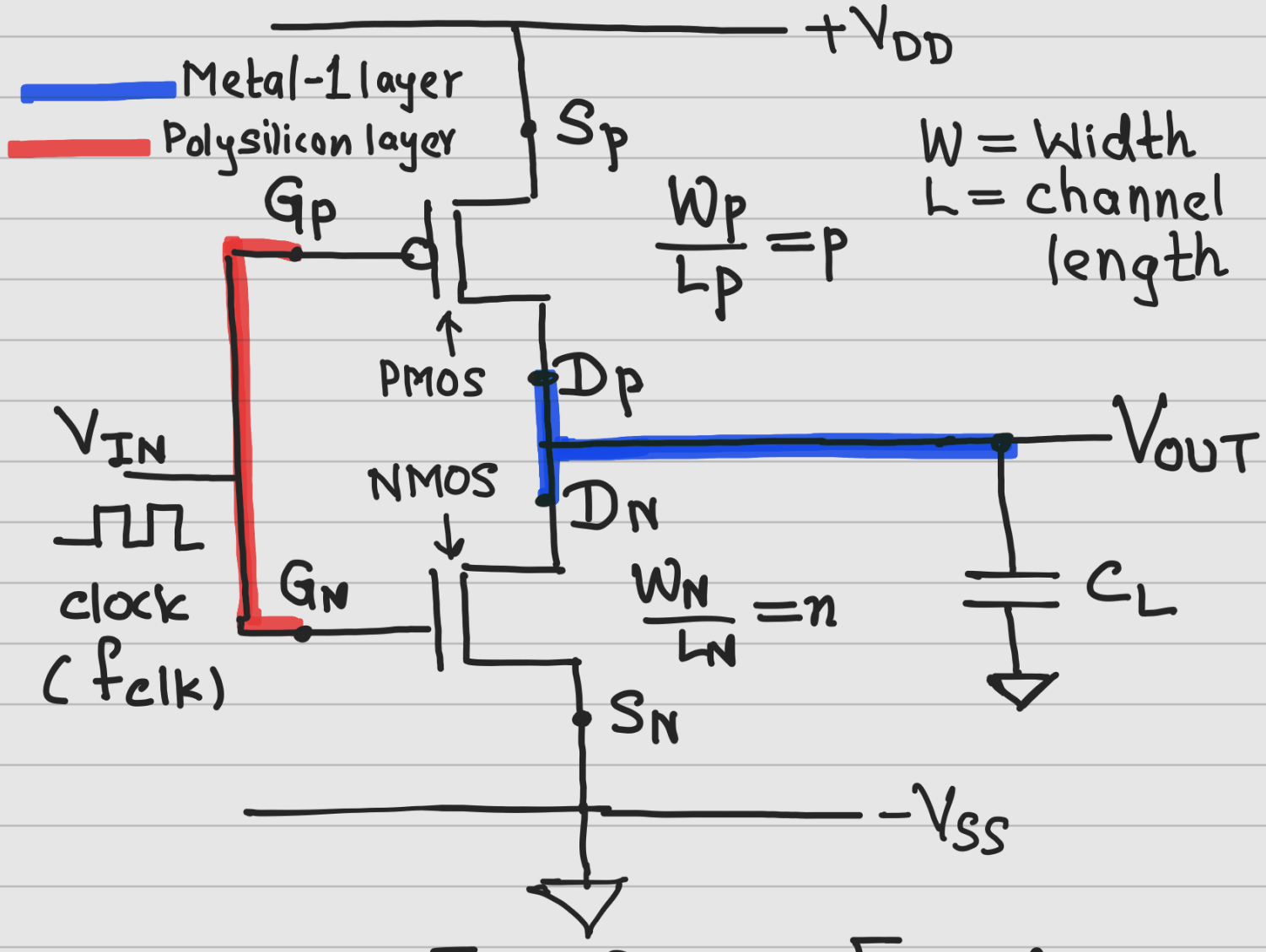
MOSFET-Level Schematic of CMOS Inverter (NOT Gate)
(Technology Independant)



W = Width
L = channel length

$\frac{W_P}{L_P} = P$

$\frac{W_N}{L_N} = n$

For 90 nm Foundry

PMOS { $W_P = 500\,nm$, $L_P = 100\,nm$ } $P = 5$

NMOS { $W_N = 500\,nm$, $L_N = 100\,nm$ } $n = 5$

$\frac{P}{n} = 1$

$V_{DD} = 1.2\,V$

$$P_{dynamic} = f_{clk} \cdot C_L \cdot (V_{DD})^2$$

✱ Nominal values :-

① $f_{clk} = 5\,GHz$

$\downarrow$

$T_{ON} = T_{OFF} = 0.09\,ns\ (90\,ps)$

$T_{rise} = T_{fall} = 0.01\,ns\ (10\,ps)$

$T_{clk} = T_{ON} + T_{OFF} + T_{rise} + T_{fall}$

$= 200\,ps$

② $C_L = 1\,fF\ (10^{-15}\,F)$

③ $V_{DD} = 1.2\,V$ (for 90nm Foundry)

$= 2\,V$ (for 180nm Foundry)

✱ $P_{dynamic}$ Analyses :-

$f_{clk}' = 2.5\,GHz$, $f_{clk}'' = 10\,GHz$ | $C_L = 1\,fF$] 90nm

$C_L' = 0.5\,fF$, $C_L'' = 2\,fF$ | $f_{clk} = 5\,GHz$] V_{DD} = 1.2V

$V_{DD}' = 2\,V$ | $f_{clk} = 5\,GHz$, $C_L = 1\,fF \rightarrow$ 180nm