Class	:	
Batch	:	
Roll. No	:	
ABC ID	:	
Assignment No.	:	B.3.a
Assignment Name	:	CMOS HALF-ADDER (Using MUX & MUX – Using TG)
Date Of Performance	:	

BLOCK DIAGRAM , TRUTH – TABLE OF HALF – ADDER

GATE – LEVEL SCHEMATIC OF HALF – ADDER

2:1 MULTIPLEXER SYMBOL & TRUTH-TABLE

CONVERTING 2:1 MULTIPLEXER INTO EX-OR GATE

CONVERTING 2:1 MULTIPLEXER INTO AND GATE

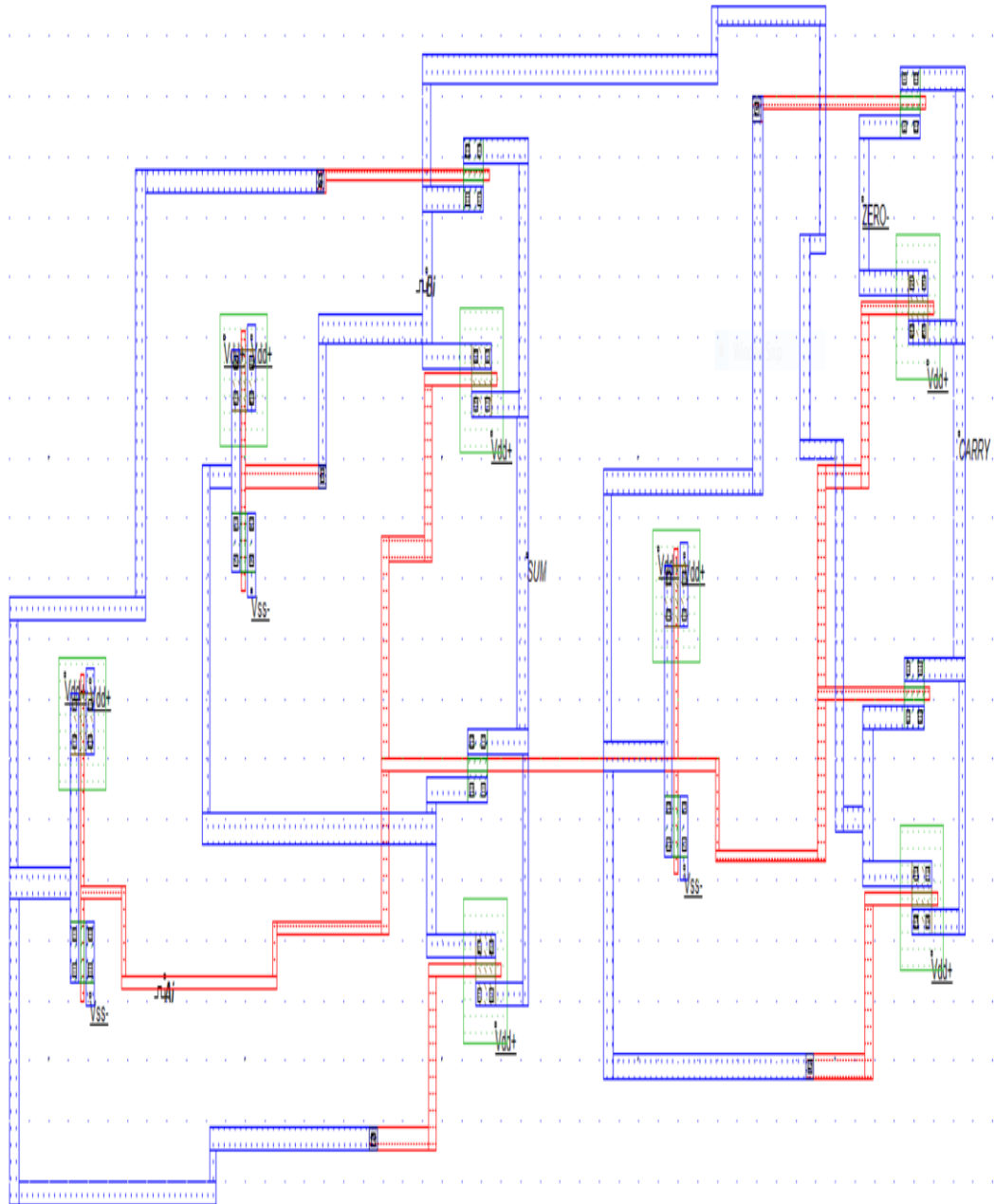# MULTIPLEXER – LEVEL SCHEMATIC OF HALF - ADDER

Truth Table:-

I/P's are ALWAYS STRONG

O/P :: S-1 = STRONG -1 , S-0 = STRONG - 0

INPUTS		OUTPUTS	
Ai	Bi	SUM	CARRY
0	0	S-0	S-0
0	1	S-1	S-0
1	0	S-1	S-0
1	1	S-0	S-1

Layout (90 nm Foundry) : (V_{dd} = 1.2 V)

Waveform:
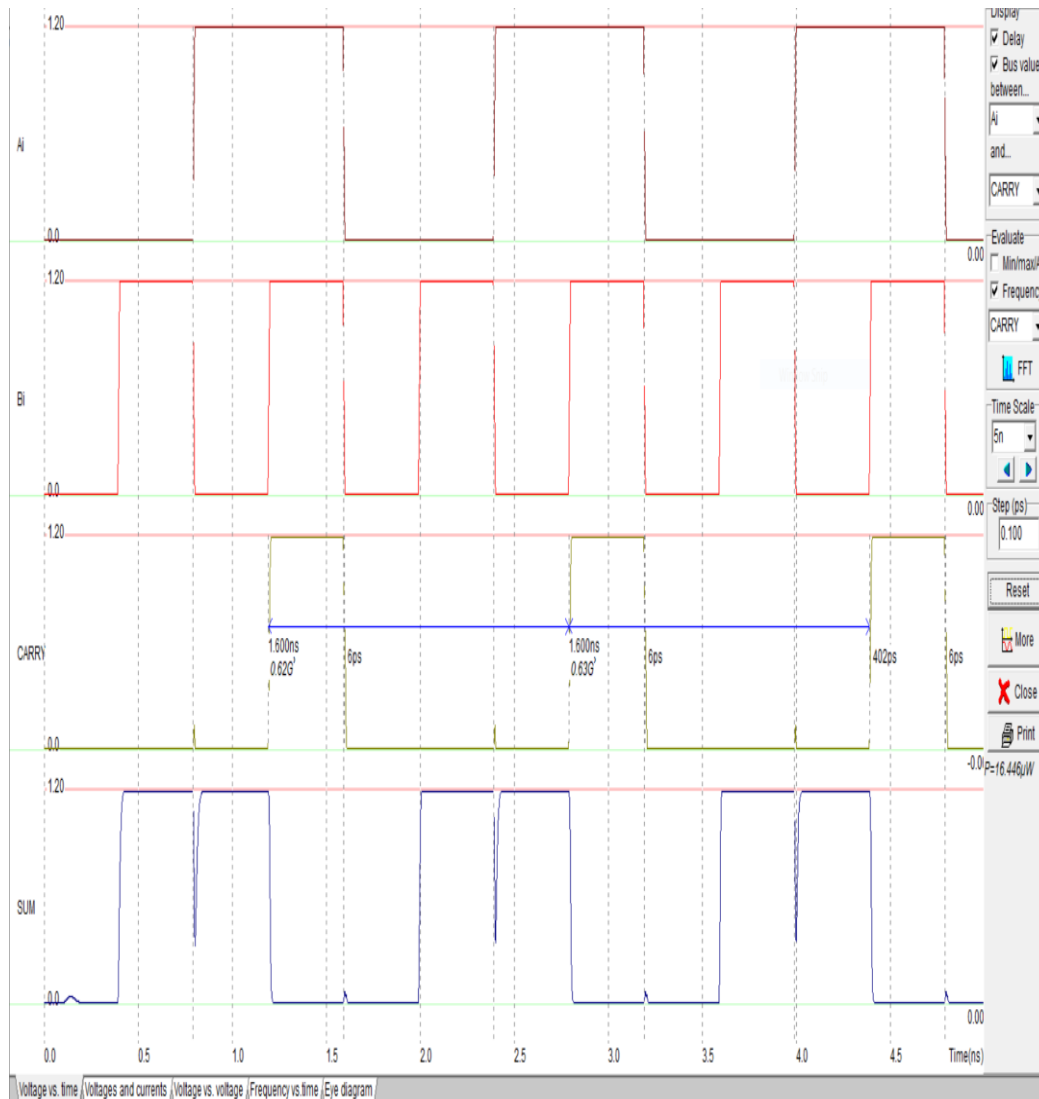
Conclusion:-

1) Drawn the LAYOUT for CMOS HALF-ADDER using 90 nm Foundry.
2) MOSFET Count for HALF-ADDER using Conventional CMOS Logic would be 28 MOSFETs (22 for EX-OR Gate + 6 for OR Gate)
3) Using the TG → MUX , MUX → LOGIC-GATE Approach , we reduced the MOSFET count to just 14 MOSFETs as seen in the LAYOUT.
4) Kept Frequency of 1st i/p (Ai) half that of frequency of 2nd i/p (Bi).
5) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.
6) Being a **Pure-CMOS System** (PMOS // NMOS & CMOS INVERTER) , it gives both **S-1** & **S-0** as O/P.