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Class	:	
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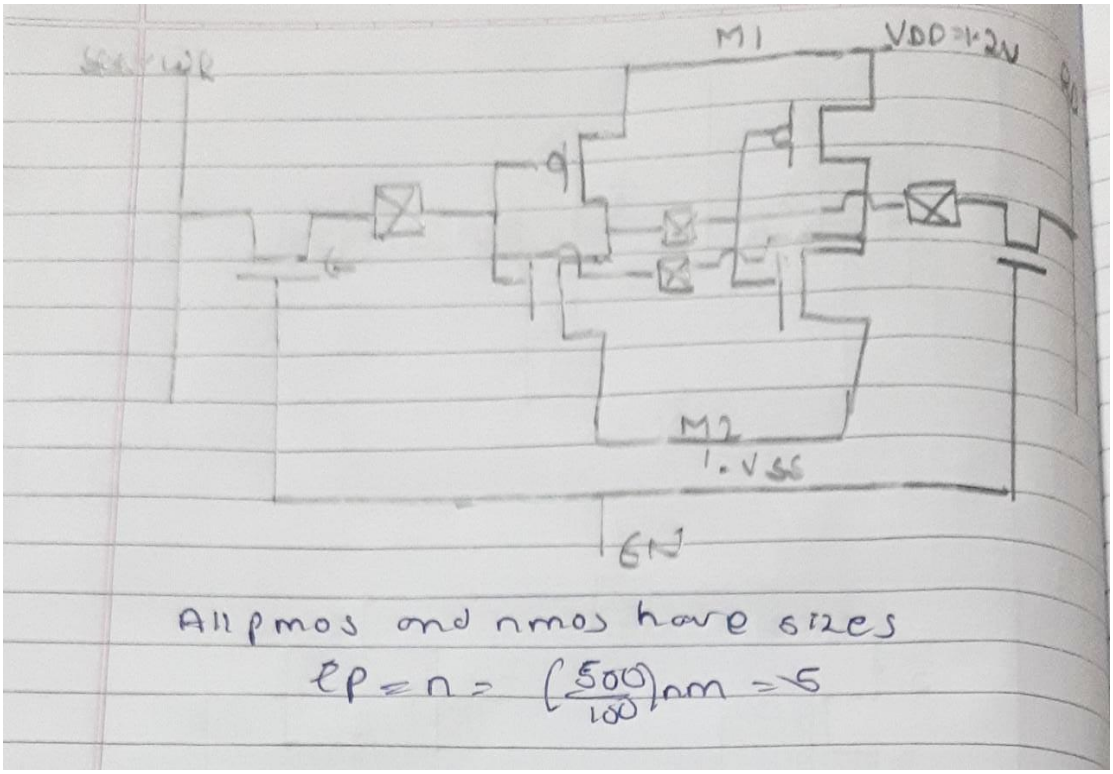
ABC ID	:	
Assignment No.	:	B.4.a
Assignment Name	:	1-bit SRAM (Using NMOS S/W)
Date Of Performance	:	

MOSFET-LEVEL SCHEMATIC of 1-bit SRAM Cell Using NMOS S/W :-



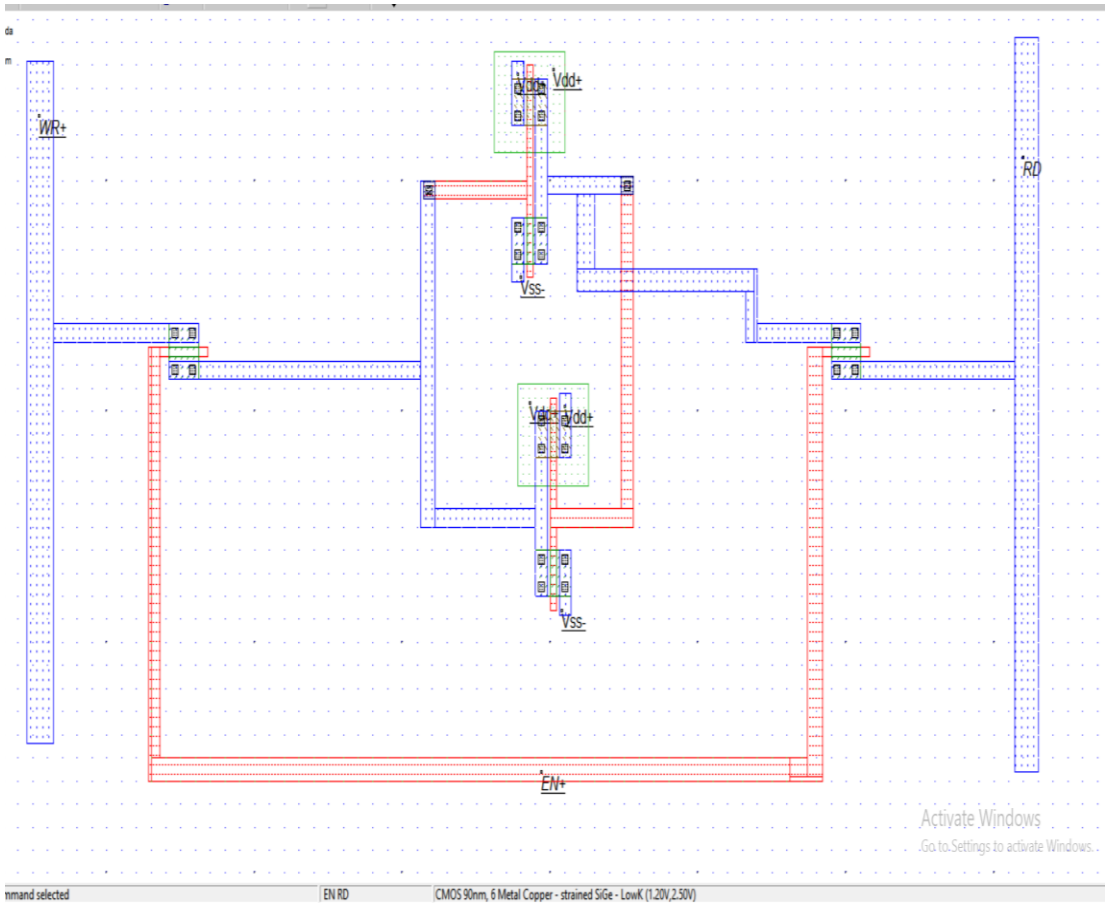
In the above Schematic :

- **N1 , N2 : NMOS S/W's**
- **I1 , I2 : CROSS – COUPLED CMOS INVERTERS**
- **System is NOT a PURE CMOS SYSTEM**
- **WR-line gets connected to RD line through N1 , N2 & I1-I2 pair**
- **N1 = N2 = ON / OFF , for EN = 1 / 0**
- **N1 , N2 Transmit "1" as WEAK-1 & "0" as STRONG-0**
- **I1 , I2 Transmit "1" as STRONG-0 , "0" as STRONG-1**

Truth Table:-

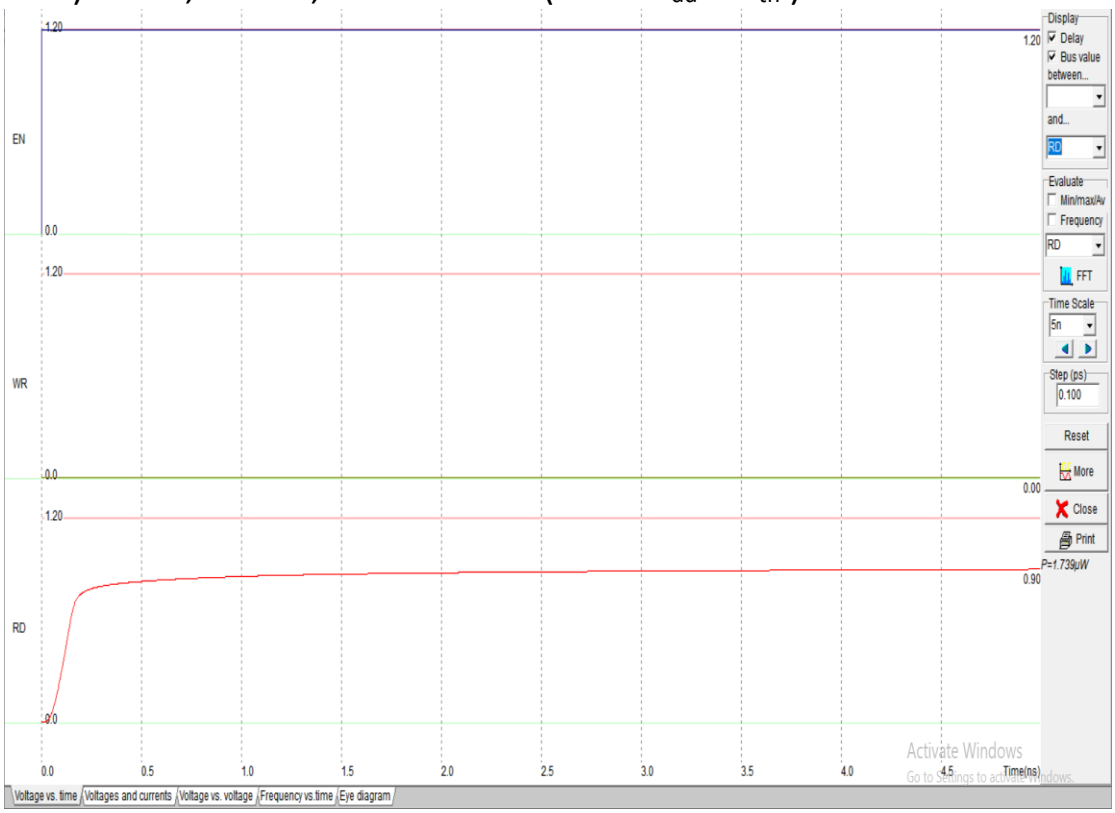
EN	WR	RD
1	0	WEAK-1 (Unacceptable)
1	1	STRONG-0 (Acceptable)
0	X	HOLD

Layout (90 nm Foundry) : (V_{dd} = 1.2 V)

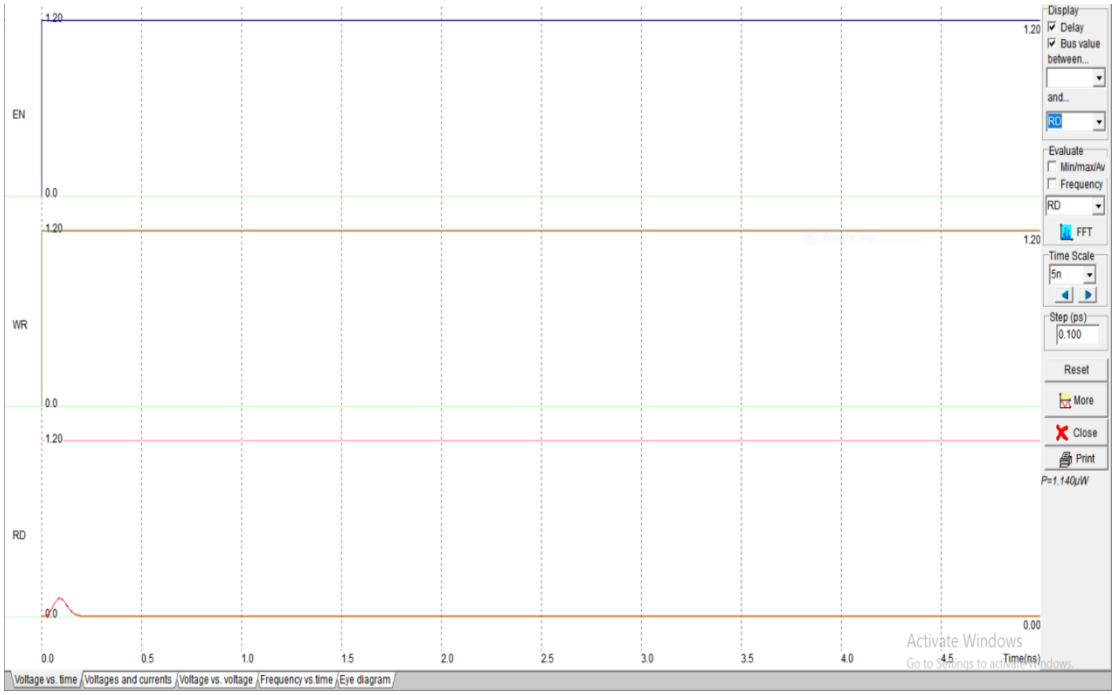


Waveforms:

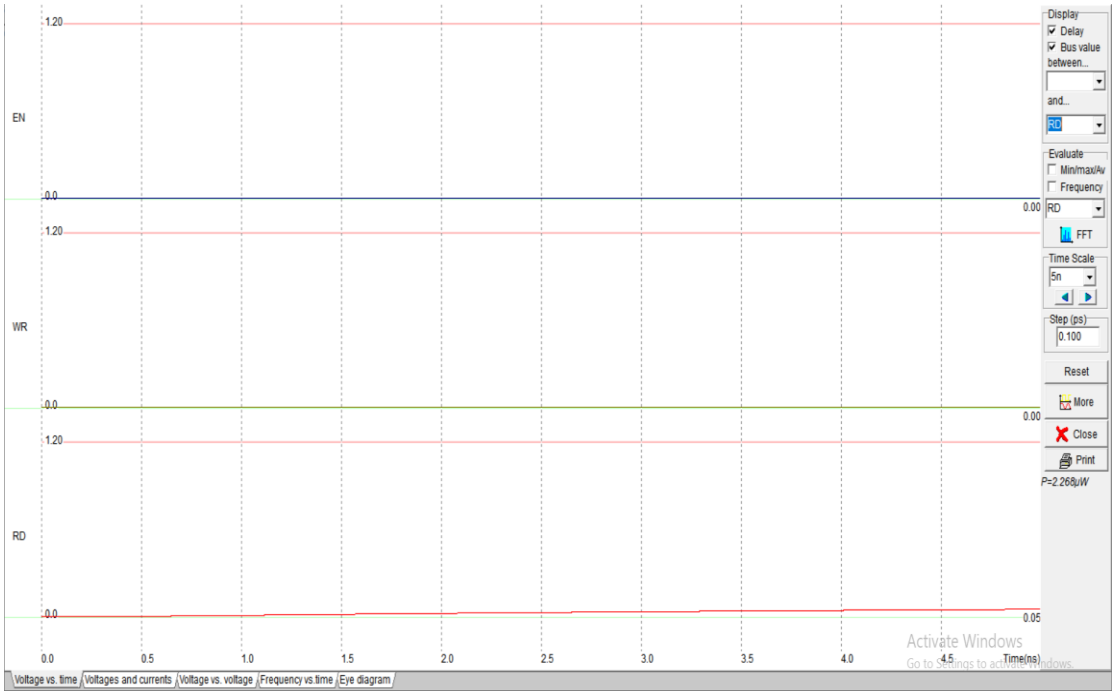
1) EN=1,WR = 0, RD =**Weak-1** (RD = $V_{dd} - V_{tn}$) = 0.9 V



2) EN=1,WR = 1, RD = **STRONG-0** (RD = – V_{ss}) = 0 V



3) EN=0,WR = 0 / 1 , RD = **HOLD (NO CHANGE)**



Conclusion :-

1) Drawn the LAYOUT of 1-bit SRAM Cell Using NMOS S/W's for 90 nm Foundry.
2) Not being a **Pure-CMOS System** (NMOS S/W's & CMOS INVERTERS) , it gives **RD = W-1 / S-0** for **WR = 0 / 1** respectively.
3) So , **"0" is READ as W-1** (*Unacceptable*) & **"1" is READ as S-0** (*Acceptable*)
4) ***The reason for above is the Presence of NMOS S/W's on both sides of CMOS INVERTERS (A Pure CMOS System)***
5) Replacing N1 , N2 with P-Channel Devices P1 , P2 will give W-0 & S-1 on RD-Line.
6) Having (N1 , P2) / (P1 , N2) will give S-1 & S-0 on RD-Line , but will need an ADDITIONAL CMOS INVERTER to simultaneously TURN-ON both S/W's ,so not Acceptable.