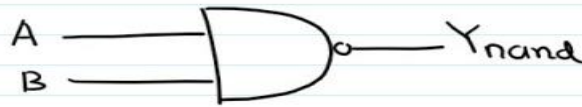


Class	:	
Batch	:	
Roll. No	:	
ABC ID	:	
Assignment No.	:	B.1.b , B.1.c
Assignment Name	:	CMOS 2 i/p NAND-AND , CMOS NOR-OR Logic Gates ( 90nm Foundry )
Date Of Performance	:	

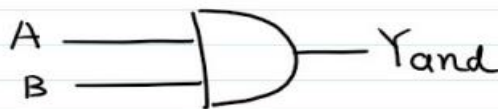
## BLOCK DIAGRAM / SYMBOLS :-

2 i/p NAND Gate



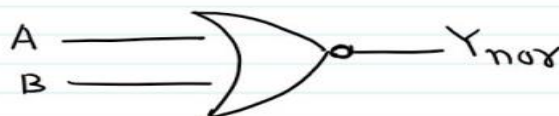
$$Y_{\text{nand}} = \overline{A \cdot B}$$

2 i/p AND Gate



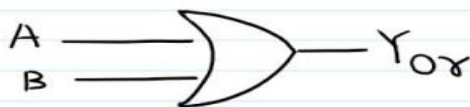
$$Y_{\text{and}} = A \cdot B$$

2 i/p NOR Gate



$$Y_{\text{nand}} = \overline{A + B}$$

2 i/p OR Gate



$$Y_{\text{or}} = A + B$$

## **MOSFET LEVEL SCHEMATIC & THEORY**

**Truth Tables :-**

**I/P's are ALWAYS STRONG**

**O/P :: S-1 = STRONG -1 , S-0 = STRONG - 0**

**1) 2 i/p NAND Gate :**

<b>A</b>	<b>B</b>	<b>Ynand</b>
<b>0</b>	<b>0</b>	<b>S-1</b>
<b>0</b>	<b>1</b>	<b>S-1</b>
<b>1</b>	<b>0</b>	<b>S-1</b>
<b>1</b>	<b>1</b>	<b>S-0</b>

**2) 2 i/p AND Gate :**

<b>A</b>	<b>B</b>	<b>Yand</b>
<b>0</b>	<b>0</b>	<b>S-0</b>
<b>0</b>	<b>1</b>	<b>S-0</b>
<b>1</b>	<b>0</b>	<b>S-0</b>
<b>1</b>	<b>1</b>	<b>S-1</b>

**3) 2 i/p NOR Gate**

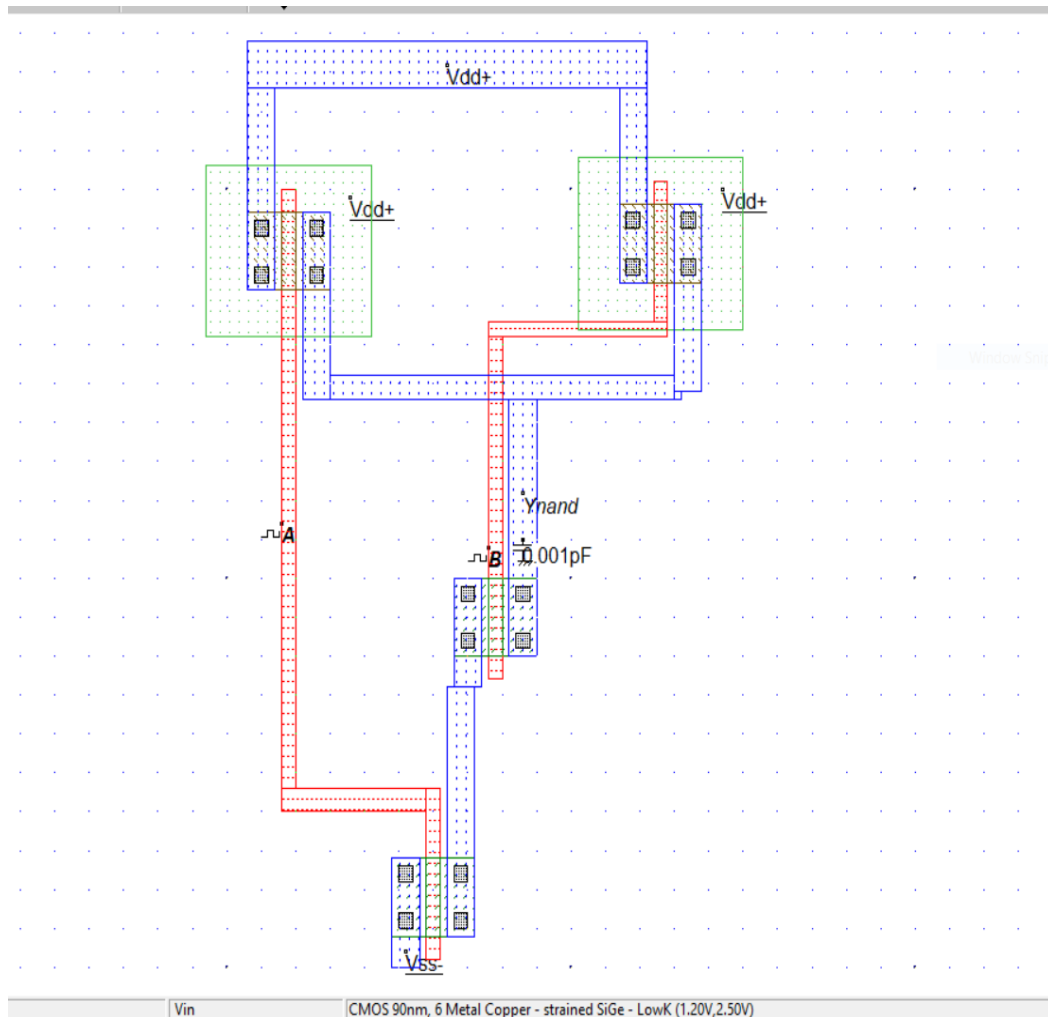
<b>A_nor</b>	<b>B_nor</b>	<b>Ynor</b>
<b>0</b>	<b>0</b>	<b>S-1</b>
<b>0</b>	<b>1</b>	<b>S-0</b>
<b>1</b>	<b>0</b>	<b>S-0</b>
<b>1</b>	<b>1</b>	<b>S-0</b>

**4) 2 i/p OR Gate :**

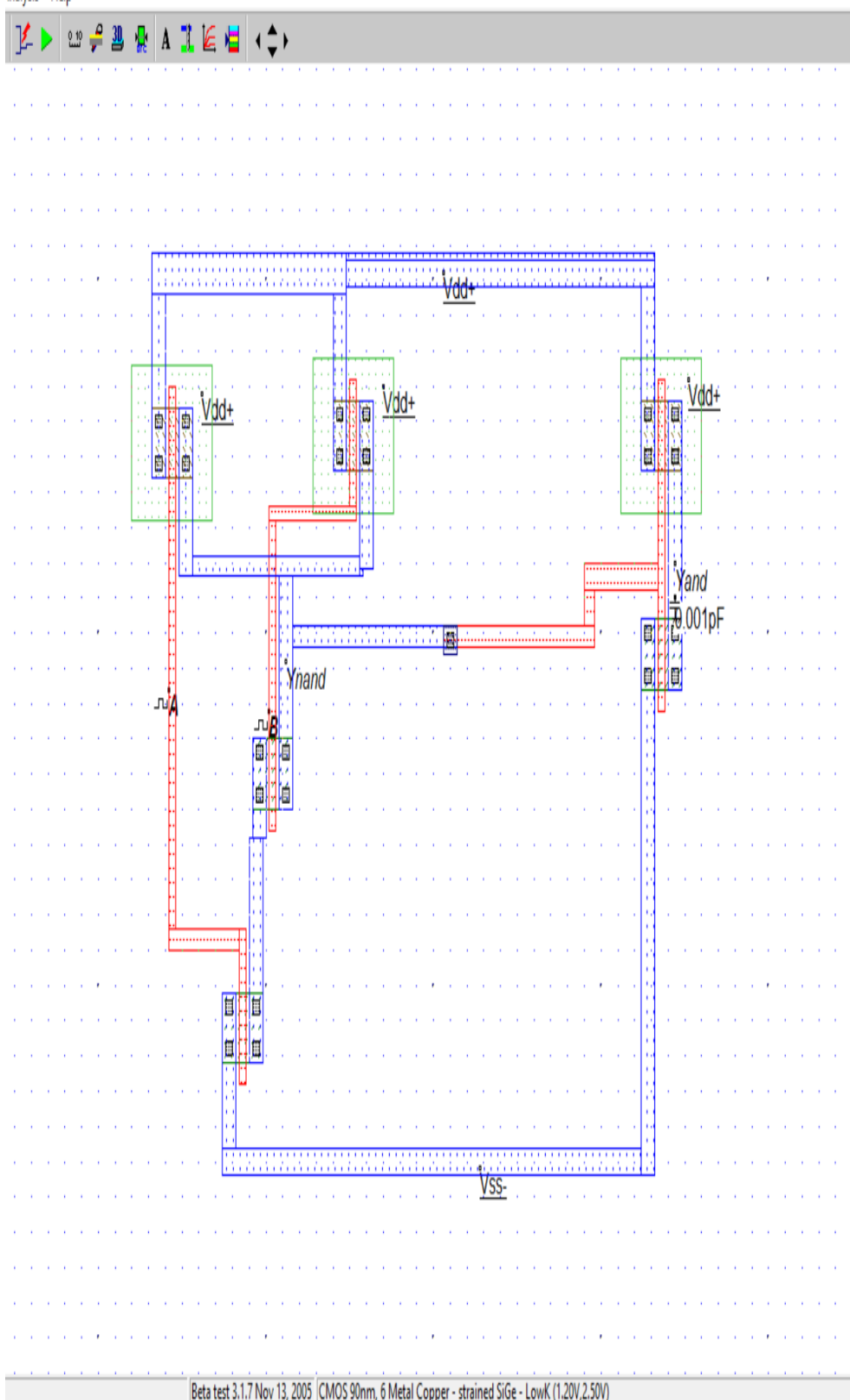
<b>A_nor</b>	<b>B_nor</b>	<b>Yor</b>
<b>0</b>	<b>0</b>	<b>S-0</b>
<b>0</b>	<b>1</b>	<b>S-1</b>
<b>1</b>	<b>0</b>	<b>S-1</b>
<b>1</b>	<b>1</b>	<b>S-1</b>

## Layout (90 nm Foundry ) : ( $V_{dd} = 1.2\text{ V}$ )

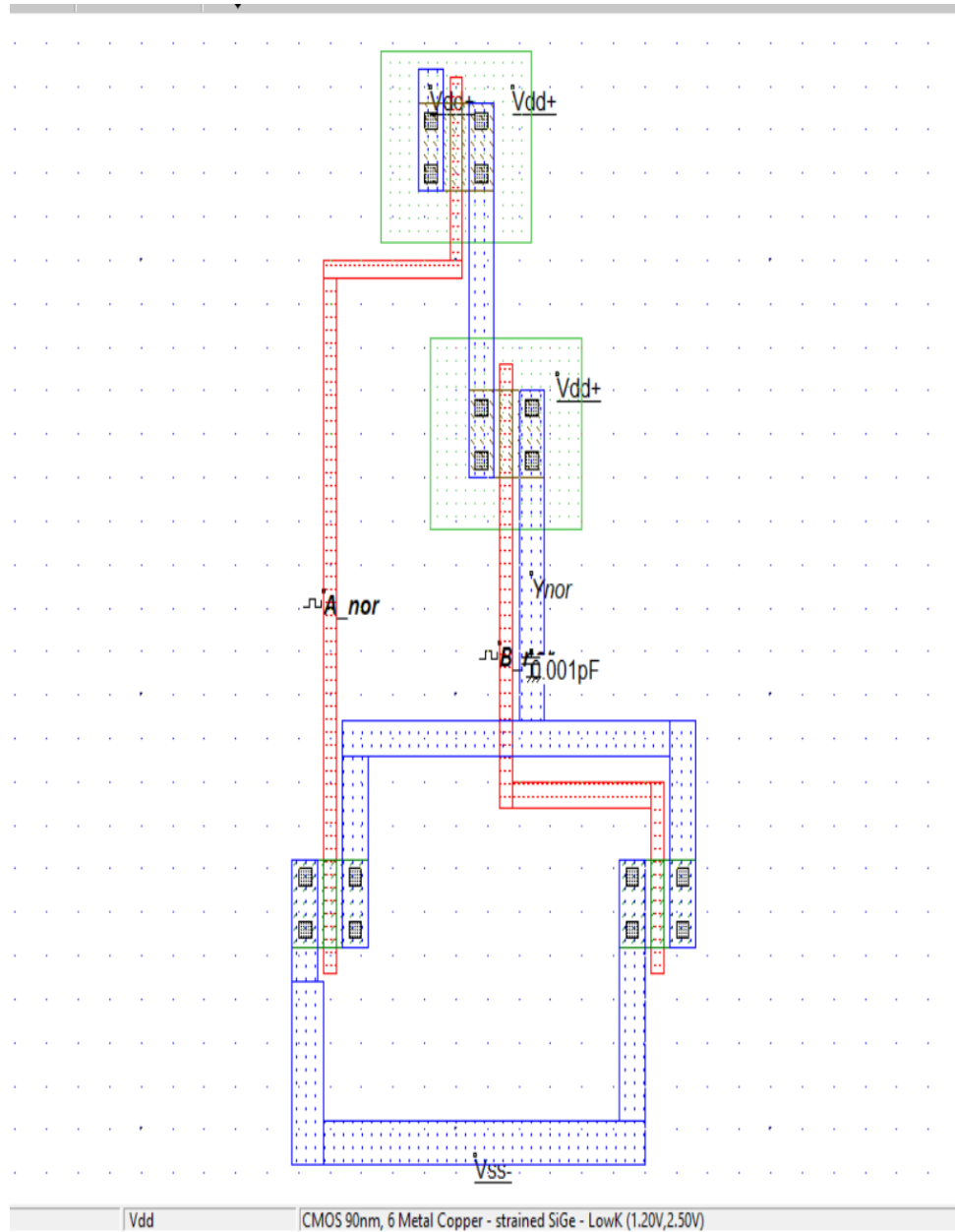
### 1) 2 i/p NAND Gate



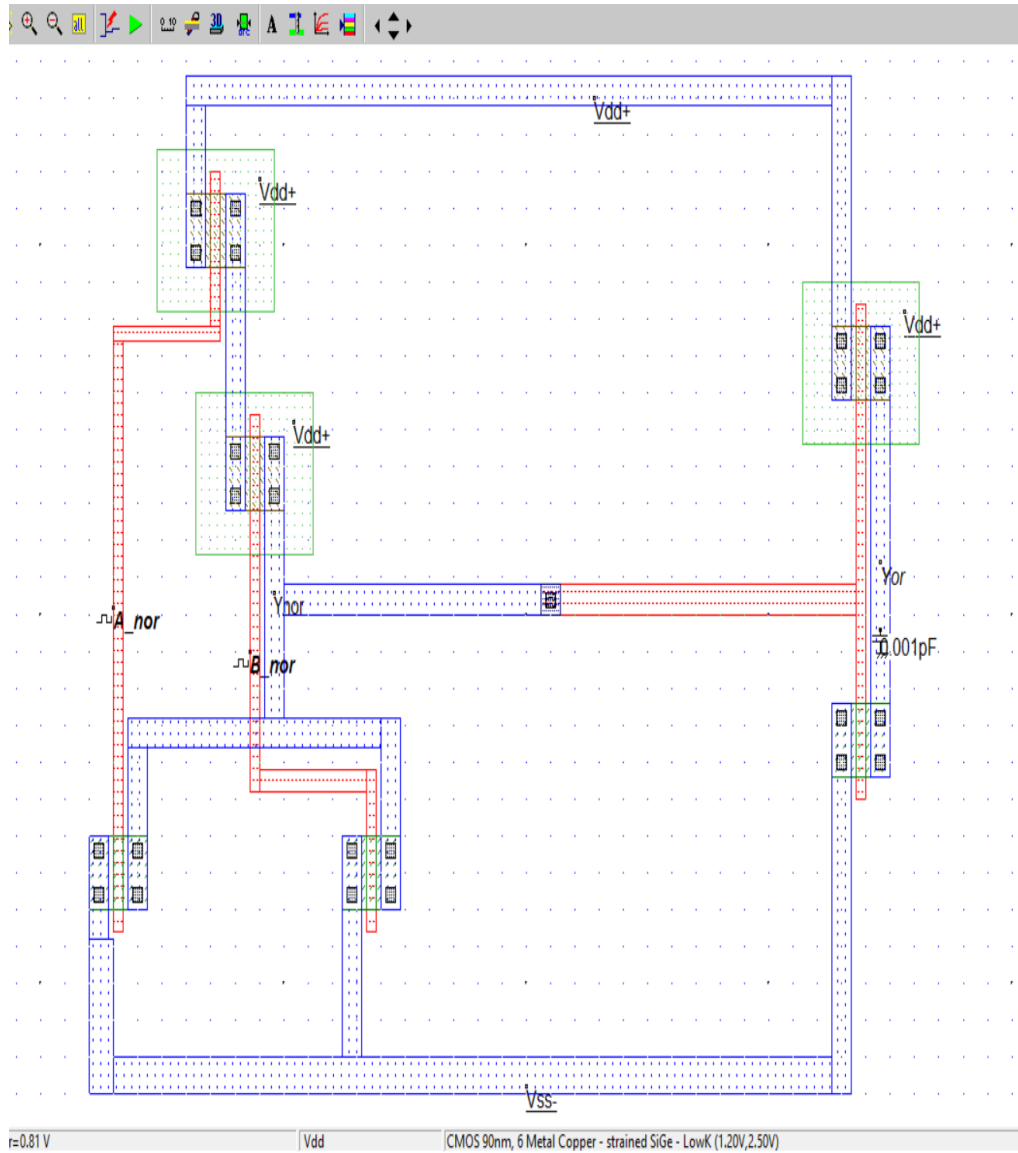
## 2) 2 i/p AND Gate



### 3) 2 i/p NOR Gate

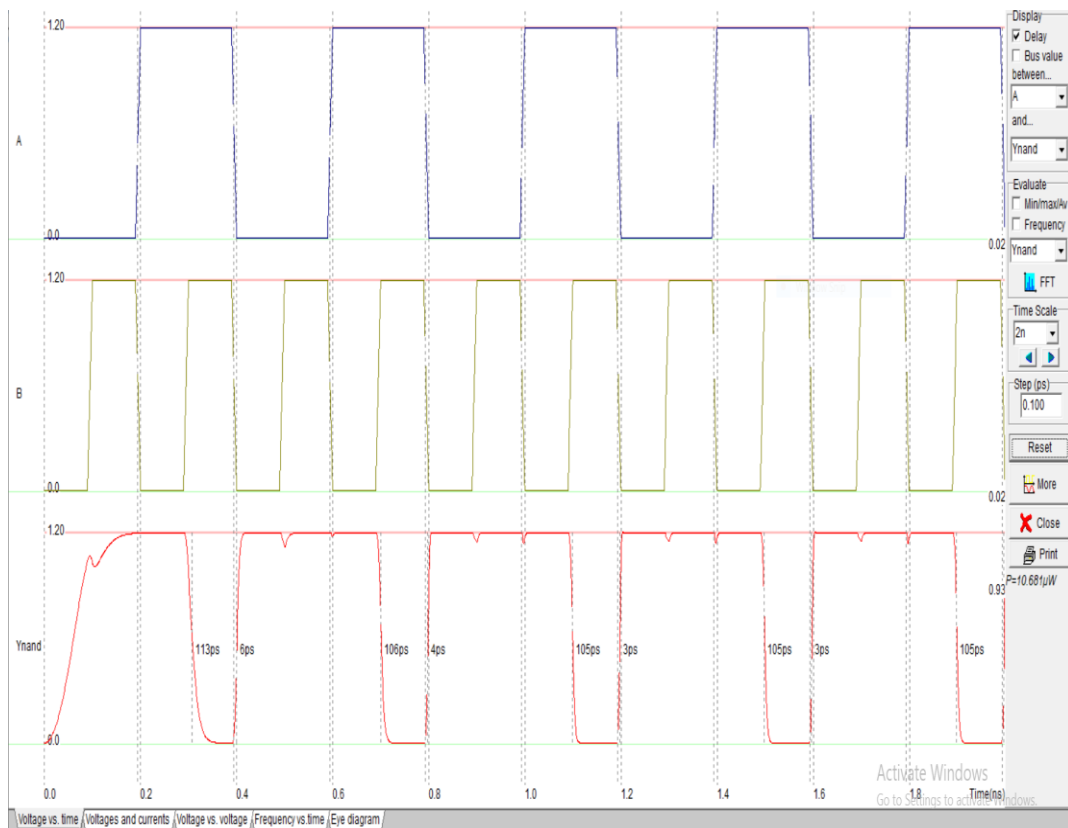


#### 4) 2 i/p OR Gate

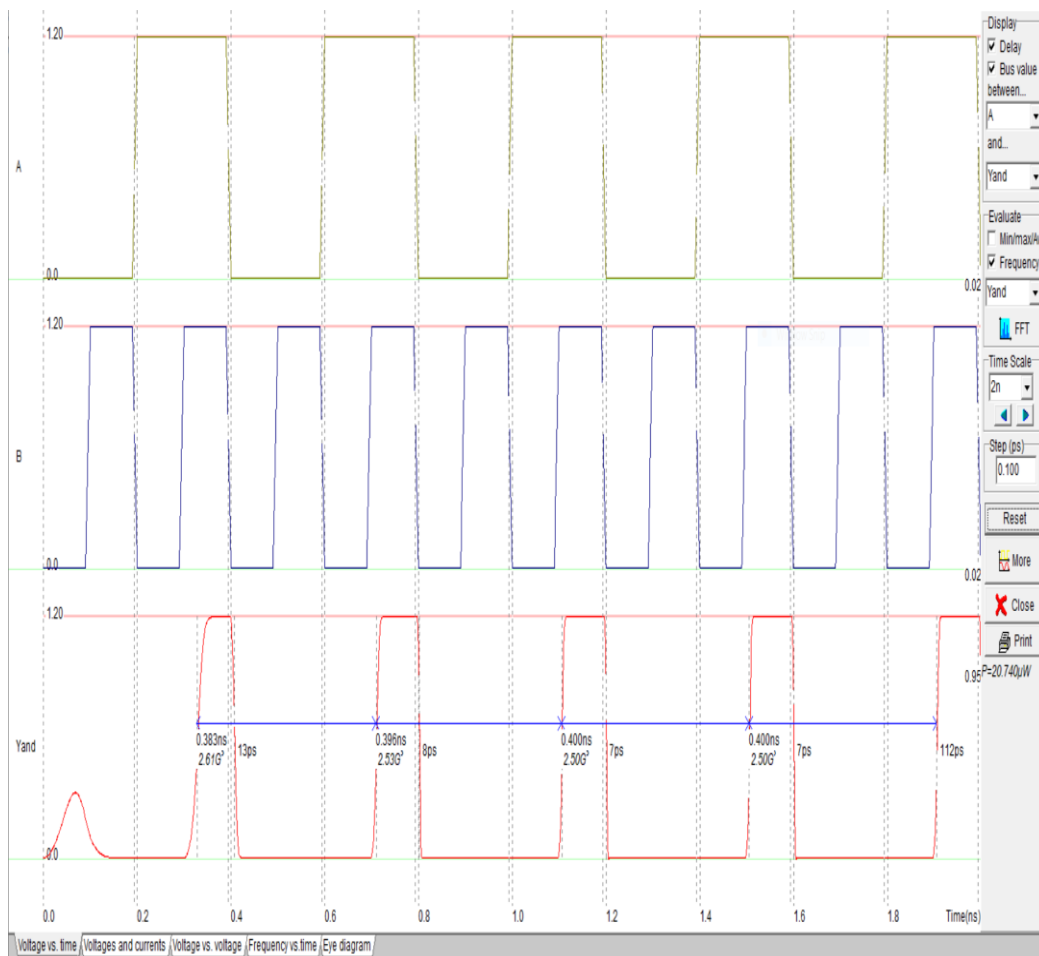


## Waveforms:

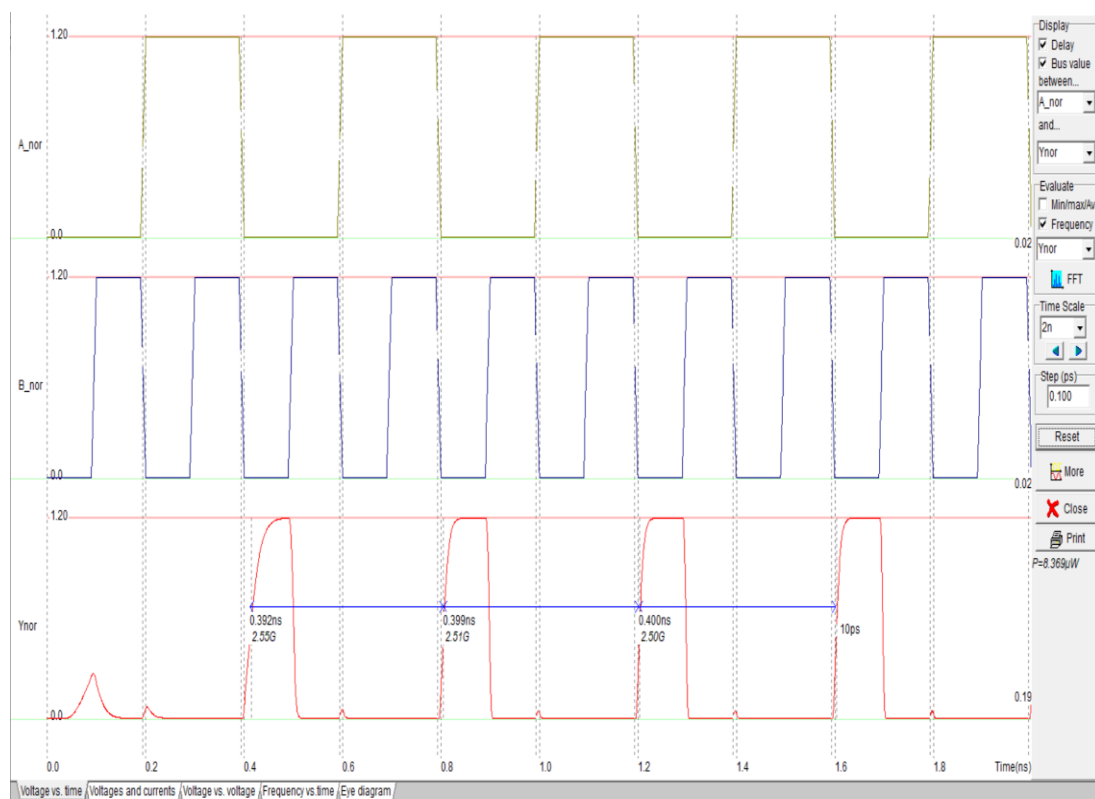
### 1) 2 i/p NAND Gate



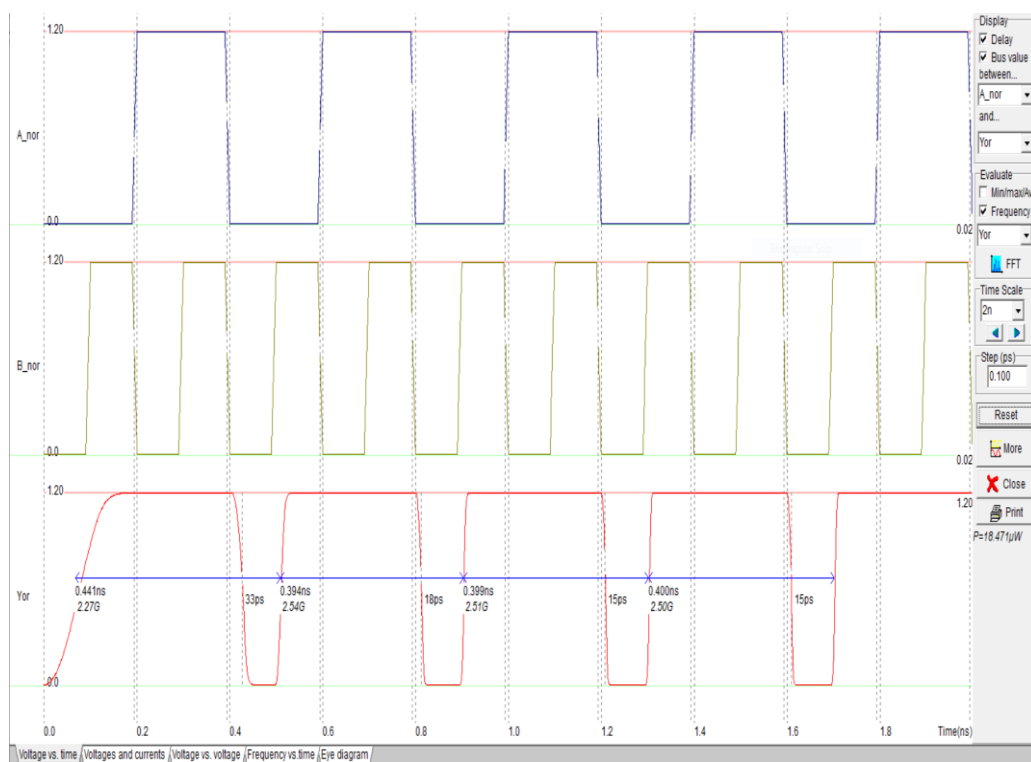
## 2) 2 i/p AND Gate



### 3) 2 i/p NOR Gate



#### 4) 2 i/p OR Gate



## **Conclusion:-**

- 1) Drawn the LAYOUT for CMOS 2 i/p NAND , AND , NOR , OR Gates using 90 nm Foundry.
- 2) NAND , NOR Gates have 2 P-channel Devices in PARALLEL , SERIES in PUN , PDN, respectively.
- 3) NAND , NOR Gates have 2 N-channel Devices in SERIES , PARALLEL in PUN , PDN, respectively.
- 4) AND , OR Gates are obtained by cascading NAND , NOR gates with NOT gate.
- 5) **O/P** of NAND , NOR Gate (On **METAL-1 Layer** ) is connected to **I/P** of NOT gate ( on **PolySilicon Layer** ) using **METAL-1 To PolySilicon Contact**.
- 6) Kept Frequency of 1<sup>st</sup> i/p ( A ) half that of frequency of 2<sup>nd</sup> i/p ( B ).
- 7) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.
- 8) Being a **Pure-CMOS System** ( PMOS // NMOS & CMOS INVERTER ) , it gives both **S-1 & S-0** as O/P.