

| | | |
|---------------------|---|--|
| Class | : | |
| Batch | : | |
| Roll. No | : | |
| ABC ID | : | |
| Assignment No. | : | B.1.b , B.1.c |
| Assignment Name | : | CMOS 2 i/p NAND-AND , CMOS NOR-OR Logic Gates (90nm Foundry) |
| Date Of Performance | : | |

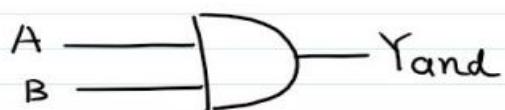
BLOCK DIAGRAM / SYMBOLS :-

2 i/p NAND Gate



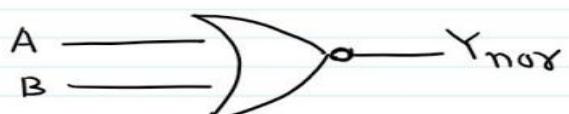
$$Y_{nand} = \overline{A \cdot B}$$

2 i/p AND Gate



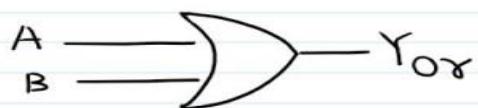
$$Y_{and} = A \cdot B$$

2 i/p NOR Gate



$$Y_{nor} = \overline{A + B}$$

2 i/p OR Gate



$$Y_{or} = A + B$$

MOSFET LEVEL SCHEMATIC & THEORY

Truth Tables :-

I/P's are **ALWAYS STRONG**

O/P :: S-1 = **STRONG -1** , S-0 = **STRONG - 0**

1) 2 i/p NAND Gate :

| A | B | Y _{nand} |
|---|---|-------------------|
| 0 | 0 | S-1 |
| 0 | 1 | S-1 |
| 1 | 0 | S-1 |
| 1 | 1 | S-0 |

2) 2 i/p AND Gate :

| A | B | Y _{and} |
|---|---|------------------|
| 0 | 0 | S-0 |
| 0 | 1 | S-0 |
| 1 | 0 | S-0 |
| 1 | 1 | S-1 |

3) 2 i/p NOR Gate

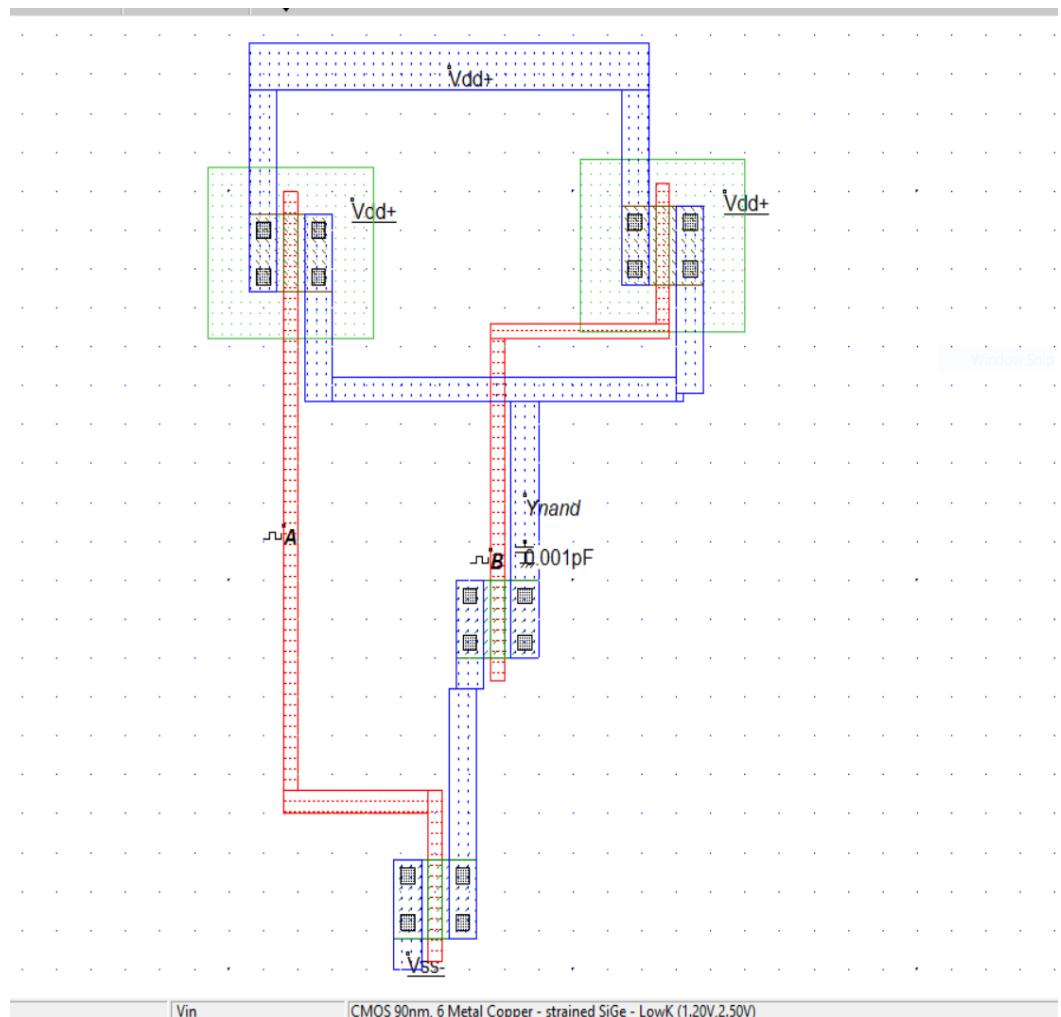
| A _{_nor} | B _{_nor} | Y _{nor} |
|-------------------|-------------------|------------------|
| 0 | 0 | S-1 |
| 0 | 1 | S-0 |
| 1 | 0 | S-0 |
| 1 | 1 | S-0 |

4) 2 i/p OR Gate :

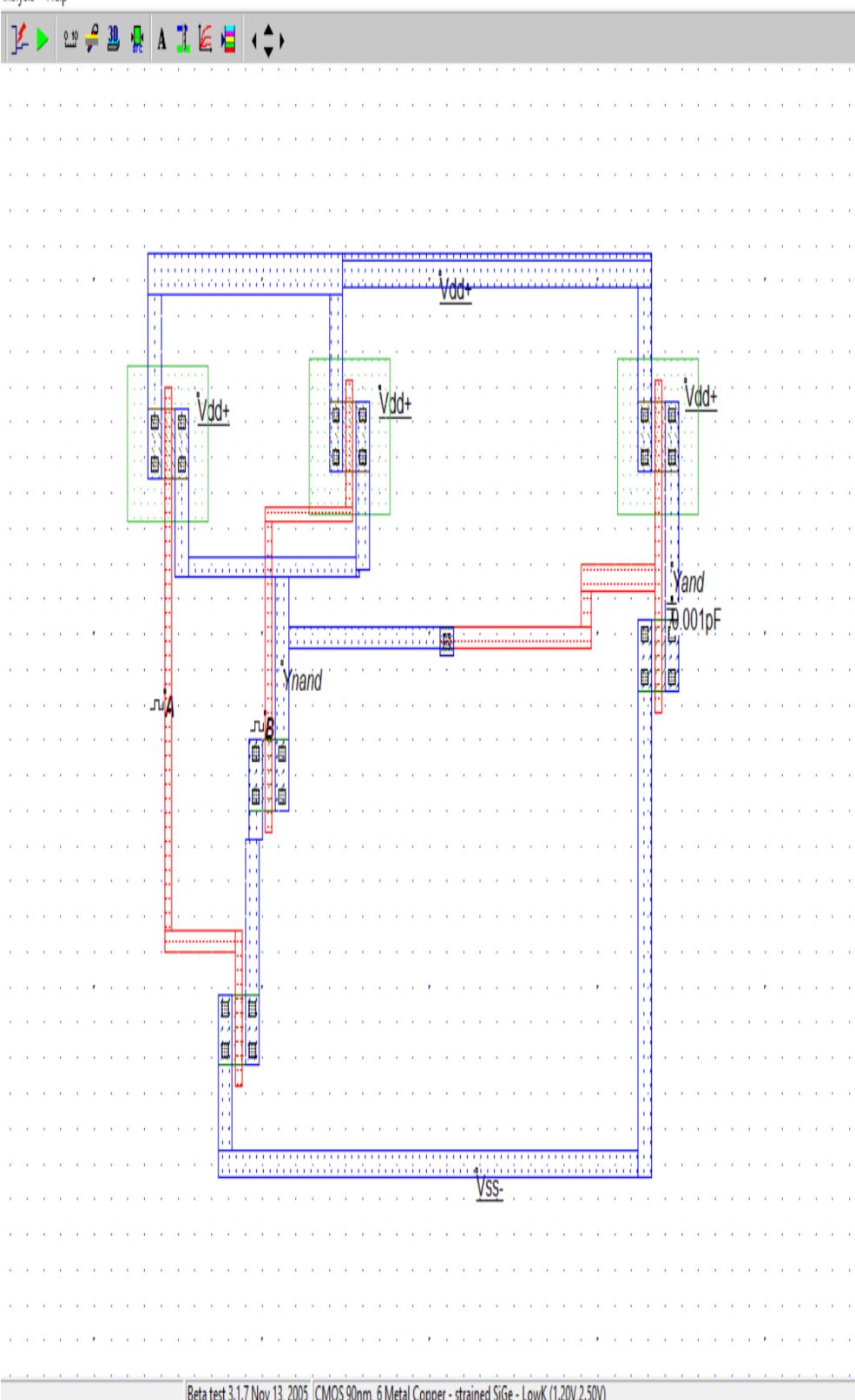
| A _{_nor} | B _{_nor} | Y _{or} |
|-------------------|-------------------|-----------------|
| 0 | 0 | S-0 |
| 0 | 1 | S-1 |
| 1 | 0 | S-1 |
| 1 | 1 | S-1 |

Layout (90 nm Foundry) : (V_{dd} = 1.2 V)

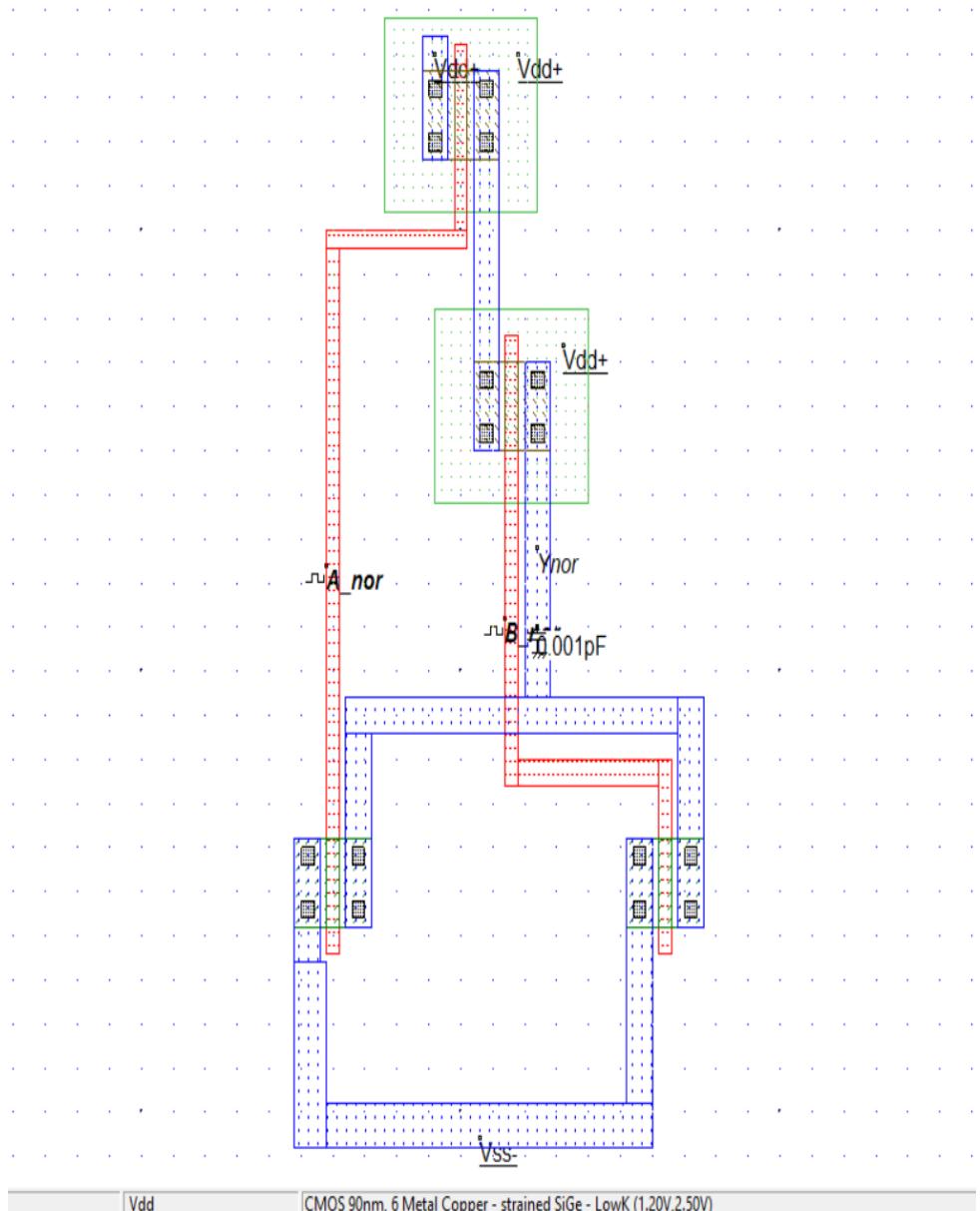
1) 2 i/p NAND Gate



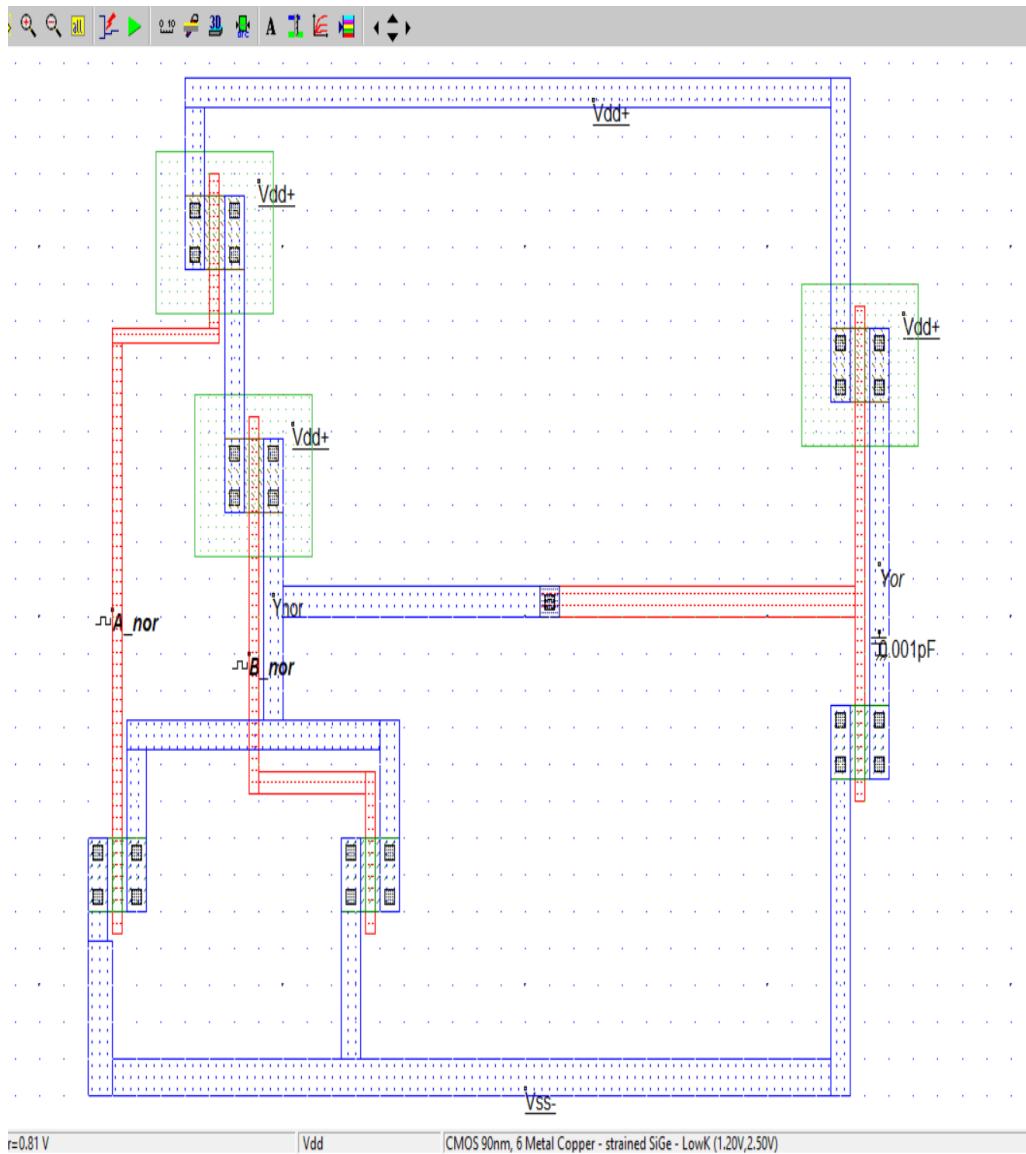
2) 2 i/p AND Gate



3) 2 i/p NOR Gate

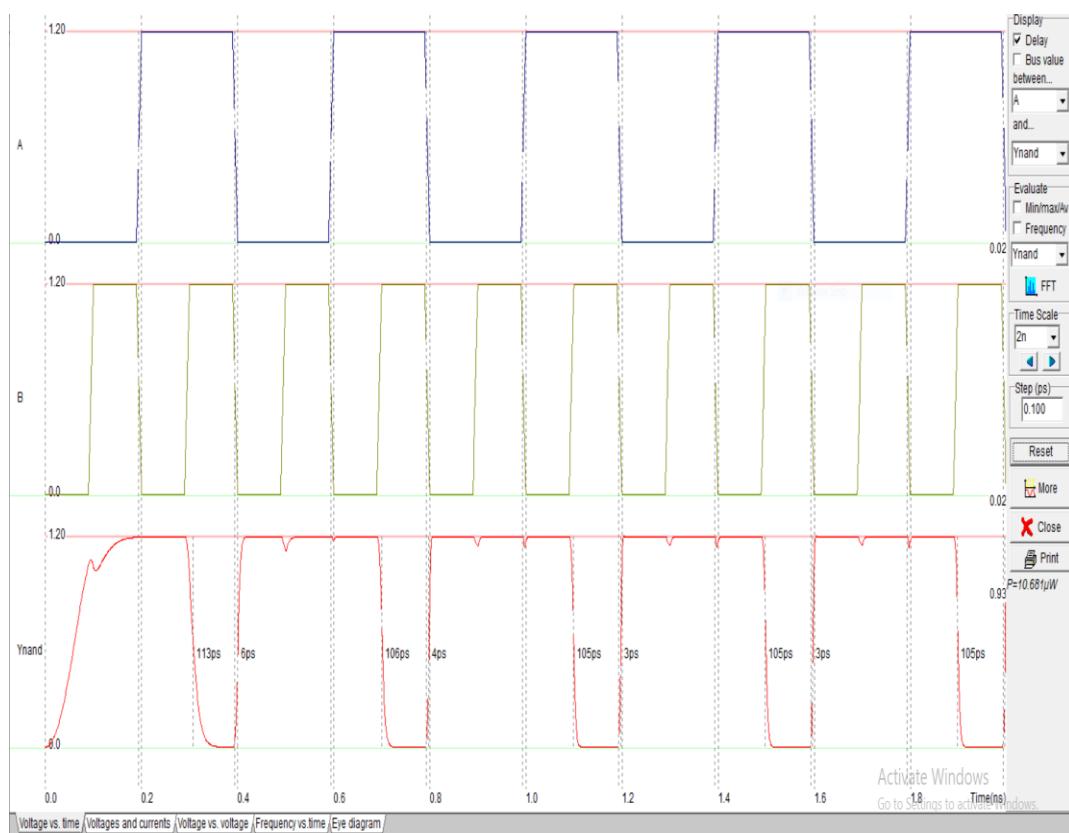


4) 2 i/p OR Gate

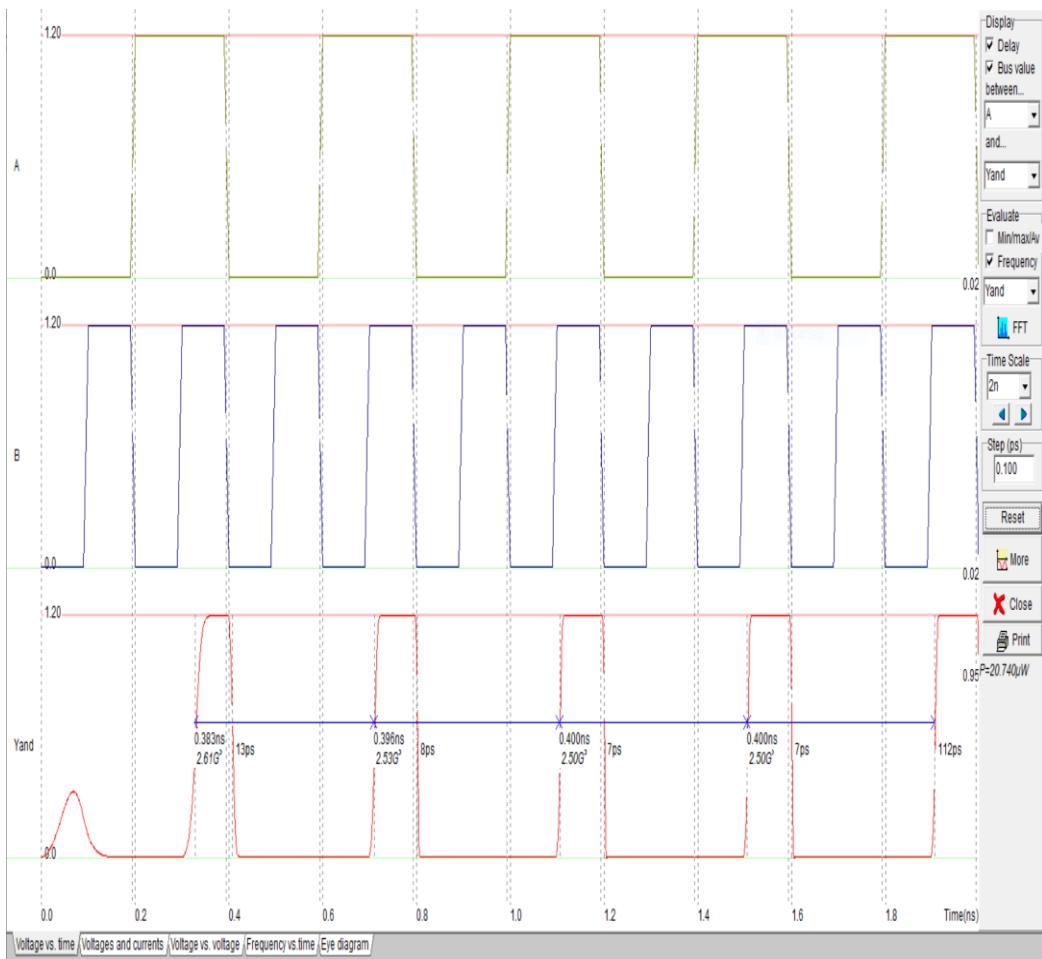


Waveforms:

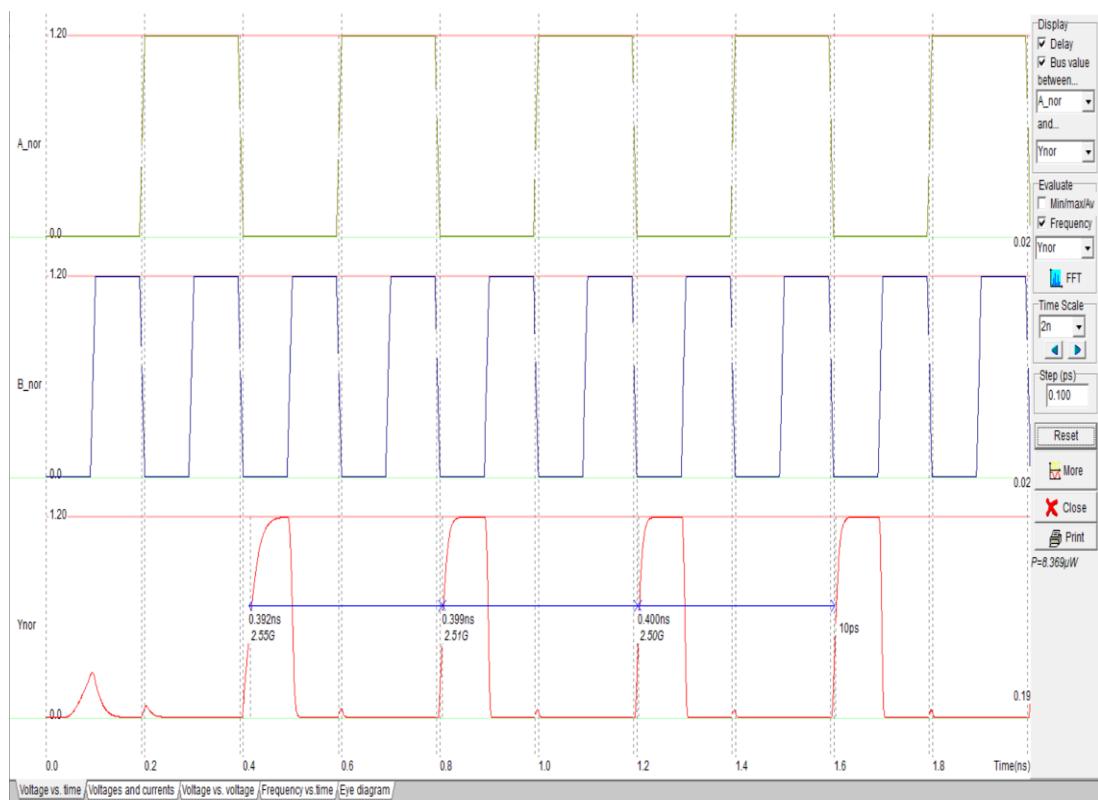
1) 2 i/p NAND Gate



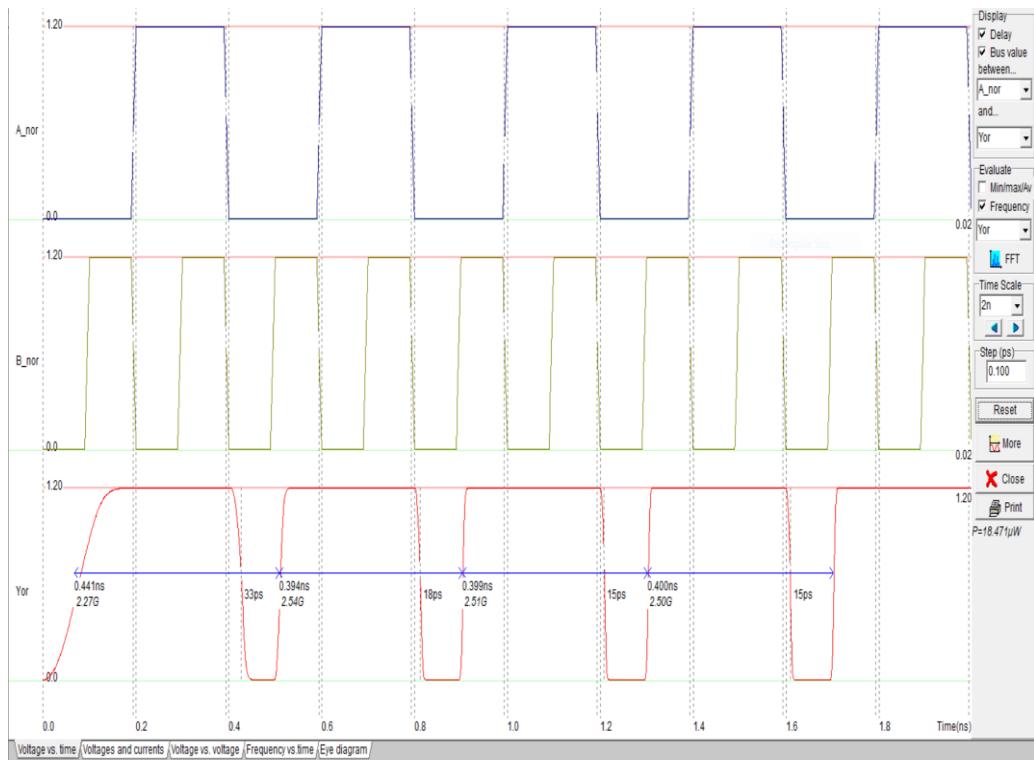
2) 2 i/p AND Gate



3) 2 i/p NOR Gate



4) 2 i/p OR Gate



Conclusion:-

- 1) Drawn the LAYOUT for CMOS 2 i/p NAND , AND , NOR , OR Gates using 90 nm Foundry.
- 2) NAND , NOR Gates have 2 P-channel Devices in PARALLEL , SERIES in PUN , PDN, respectively.
- 3) NAND , NOR Gates have 2 N-channel Devices in SERIES , PARALLEL in PUN , PDN, respectively.
- 4) AND , OR Gates are obtained by cascading NAND , NOR gates with NOT gate.
- 5) **O/P** of NAND , NOR Gate (On **METAL-1 Layer**) is connected to **I/P** of NOT gate (on **PolySilicon Layer**) using **METAL-1 To PolySilicon Contact**.
- 6) Kept Frequency of 1st i/p (A) half that of frequency of 2nd i/p (B).
- 7) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.
- 8) Being a **Pure-CMOS System** (PMOS // NMOS & CMOS INVERTER) , it gives both **S-1 & S-0** as O/P.