

Class	:	
Batch	:	
Roll. No	:	
ABC ID	:	
Assignment No.	:	B.2
Assignment Name	:	2:1 MULTIPLEXER Using TRANSMISSION GATE (TG)
Date Of Performance	:	

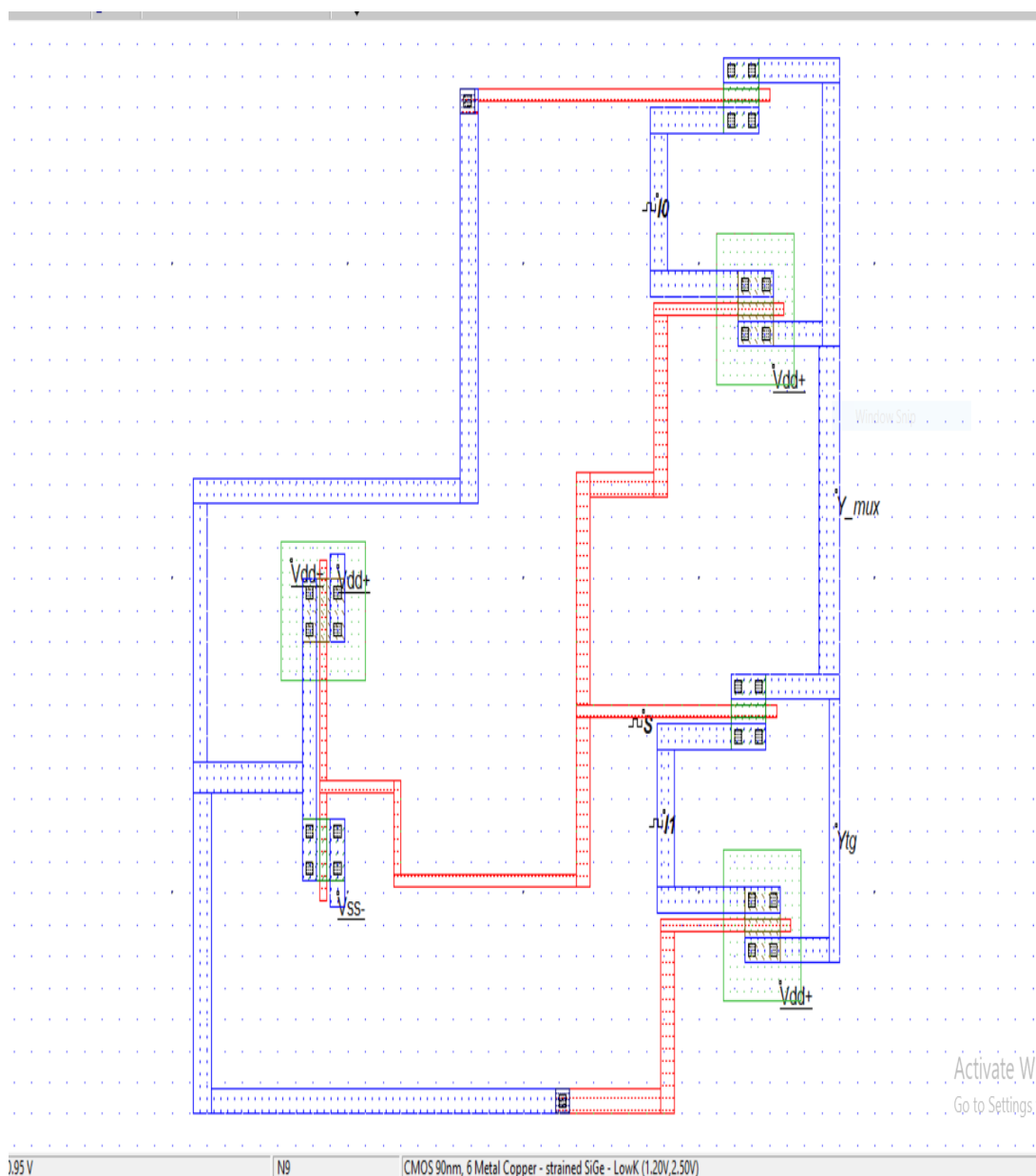
SYMBOL , TRUTH-TABLE , SYMBOL-LEVEL SCHEMATIC

MOSFET-LEVEL SCHEMATIC of 2:1 MUX Using TG

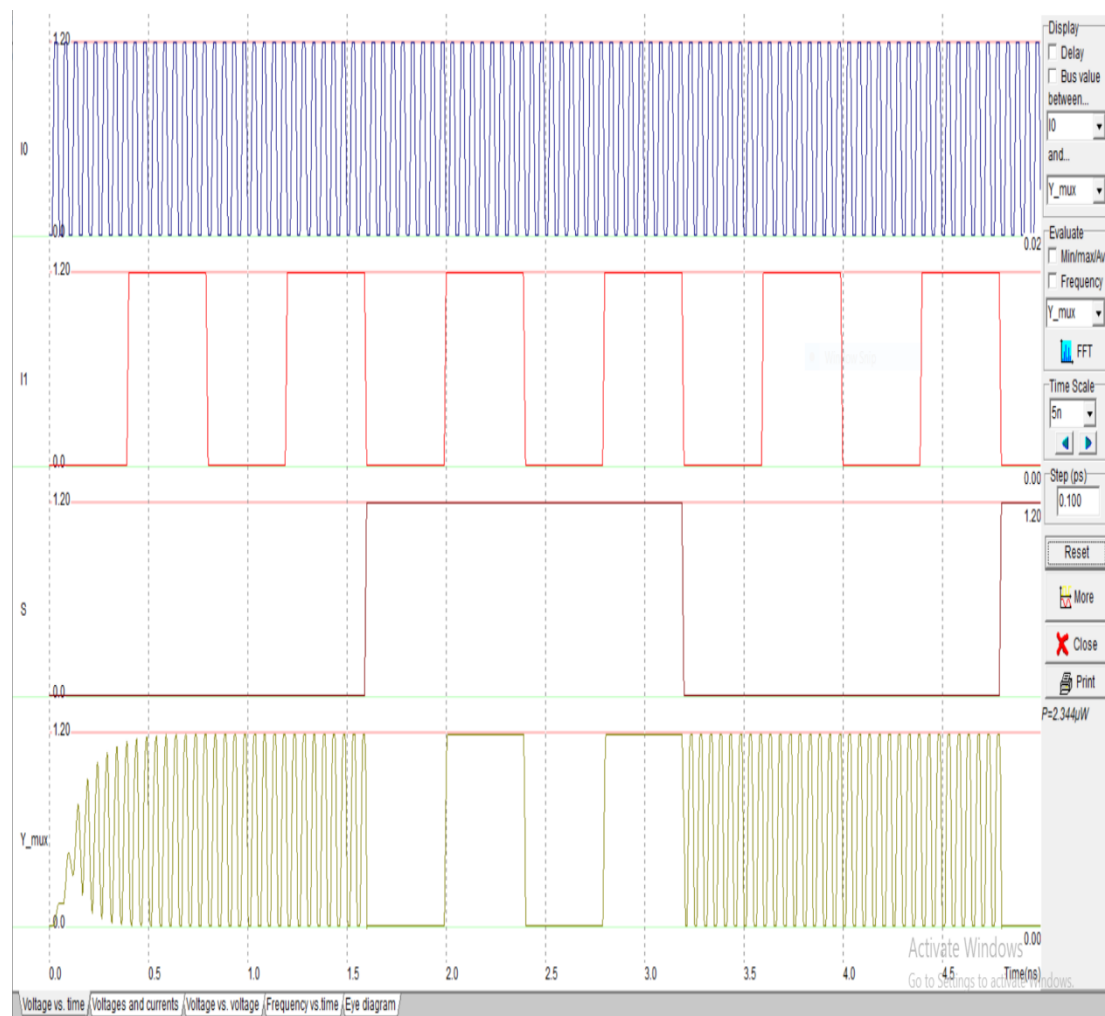
TRUTH TABLE :-

S	Ymux
0	I0
1	I1

Layout (90 nm Foundry) : ($V_{dd} = 1.2\text{ V}$)



WAVEFORMS :



CONCLUSIONS :

- 1) Drawn the LAYOUT of 2:1 MULTIPLEXER USING TRANSMISSION GATE (TG) for 90 nm Foundry.
- 2) MOSFET Count for 2:1 MULTIPLEXER using Conventional CMOS Logic would be **20 MOSFETs** ($Y_{mux} = S.I0 + S.I1$)
- 3) Using the TG → MUX Approach , we reduced the MOSFET count to just **6 MOSFETs** as seen in the LAYOUT.
- 4) **Power Dissipation** in is just **2.344μW** thus exhibiting the Merit of Very Low Power Dissipation of CMOS Logic Family.
- 5) "I0" , "I1" are chosen as **VH-Frequency & Relatively Lower Frequency Clocks** ,while **LF-Clock** is chosen as "S"
- 6) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.
- 7) Being a **Pure-CMOS System** (PMOS // NMOS & CMOS INVERTER) , it gives both **S-1 & S-0** as O/P.