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Part B → can be summarised as following three steps:

1. Draw layout of given CMOS system (1st on paper, then EDA tool)
2. Simulating the layout,
3. observing input and output waveforms, interpreting the Result and drawing meaningful conclusion.

Name of EDA tool: microwind (V.3.1) → IC layout editor, VLSI Backend tool
↳ USA company.
↑ VLSI Software.

D: | Software | microwave. 3.1. → 7.28 size.
System | microwave 31. exe → Double click.

List of Exp

1st. Ass.

B.1.a → CMOS Inverter and analysis
B.1.b → two input (Nand, and) (nor, Or).
B.1.c → Transmission gate (TG – Unit 4)
] B.1.

B.2 → 2:1 mux using TG logic] B.2.

B.3.a → Half Adder] B.3
B.3.b → full Adder.

B.4.a → one bit SRAM cell using NMOS switch
B.4.b → one bit SRAM cell using TG switch
] B.4

Generic Step for Part B assignments.

1) Draw the correct mosfet level schematic for given CMOS system.
   ON Paper → than on EDA.
2) Terminalise above schematic. → Indicate D, S, G on each constituent mosfet.
3) Tool usage Start :-
   pick and drop the necessary no. of mosfet as per Step no. (1) into tools workspace. using 'palet of layers'.
4) Connect the mosfets as shown in Step (2). Using following Rules

   D ↔ D
   D ↔ S
   S ↔ S
   } → Blue metal 1

   G ↔ G → Red polysilicon

   D/S → G → ⊠ → metal1 polysilicon contact.

   # metal 1 and polysilicon → too layers.

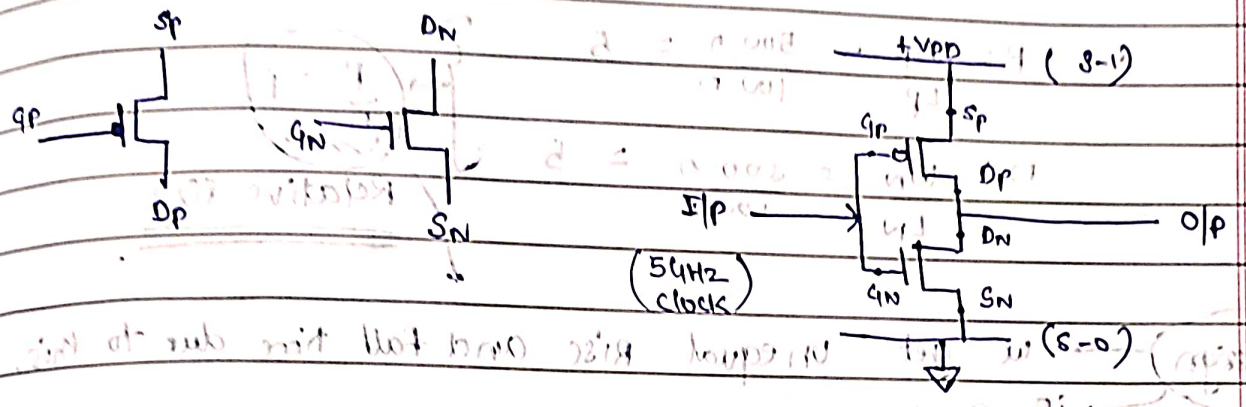
   Gate → I/P
   D, S → O/P

5) Apply all i/p signals to appropriate gate terminals as shown in Step (2)
6) Define all o/p terminals as 'visible node' → element in palet.
7) Run Design Rule Check (DRC)
8) Polarise all N-well's in layout by connecting them to +VDD.
   is a region in which pmos is fabricated. → generate electrical Rule check error if not done.
   (ie) polarise all pmos devices.

9) Run Simulation
10) observe i/p and o/p waveform → Relate to TT or funtn Table, interprate meaningfull conclusion.

Draw layout of CMOS inverter using 90nm foundry perform analysis of dependency of delay dynamic power dissipation (P_{dyne})

active low → PMOS → good to transmit 1
active high → NMOS → good to transmit 0
→ for pull up ckts. (VDD and Vss)



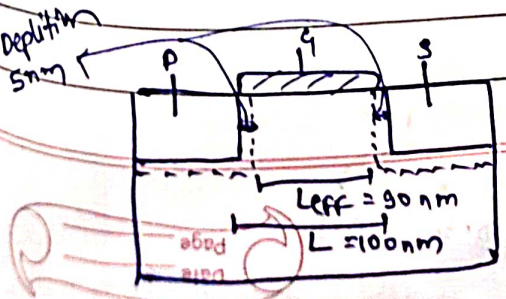
VDD → 1.2V → decided by 90nm foundry (cant change)
→ 2V → ~~180nm foundry~~

file > select foundry > CMOS 018 → 180nm
CMOS 90 → 90nm

from scale.
- 5 lambda = 0.250um = 250nm
- $5\lambda = 250nm$
- $\lambda = 50nm$
- $2\lambda = 100nm$ → foundry. But we want 90nm.

10nm diff

⇒ Difference is bcz depletion Region found in mosfet.



∴ Same width / Length.

pmos → mos generator → W_p = 500 nm → width.
→ L_p = 100 nm → length.

Nmos → —— → W_N = 500 nm → ——
L_N = 100 nm. → ——

Size of mosfet = $\frac{W}{L}$

$P = \frac{W_P}{L_P} = \frac{500\,n}{100\,n} = 5$

$n = \frac{W_N}{L_N} = \frac{500\,n}{100\,n} = 5$

$\frac{P}{n} = 1$ → Relative size

Bad design → we get unequal Rise and fall time due to this.
→ iF P=N
if P = 2.5 N → then equal (Study in Unit 4)
due to Resistance and mobility of e⊖.

$t_1 + t_r + t_h + t_f = t = (90 + 10 + 90 + 10)$ psec = 200 psec

Clock: $\frac{1}{200\,psec} = 5\,GHz$

$P_{dyn} = f_{clk} \cdot C_L \cdot (V_{DD})^2$ → dynamic power decepation

add → 0.001 → pf capacitor

$= 5GHz \cdot 1ff \cdot (1.2)^2$

1 femtofarad

obs table.

① $P_{dyn} = f^n(f_{clk})$ ← function.

$C_L = 1fF$ $V_{DD} = 1.2V$

f_{clk} (GHz)	P_{dyn} (uw)
10	24 ≈ 23.8
5	12
2.5	6.712 ≈ 6

② $P_{dyn} = f^n(C_L)$

$F_{clk} = 5\,GHz$.

layout have parasatic capacitor

C_L (FF)	P_{dyn} (uw)
2	18.7
1	12.5
0.5	9.5

1.5 times

③ $P_{dyn} = f^n(V_{DD})$

$f_{clk} = 5GHz$, $C_L = 1fF$.

VDD	P_{dyn} (uw)
1.2	12.5
2	39.64

1.67 times

3.12 times

→ as non linear (square)

TON = 0.09 ns

TOFF = 0.01 ns