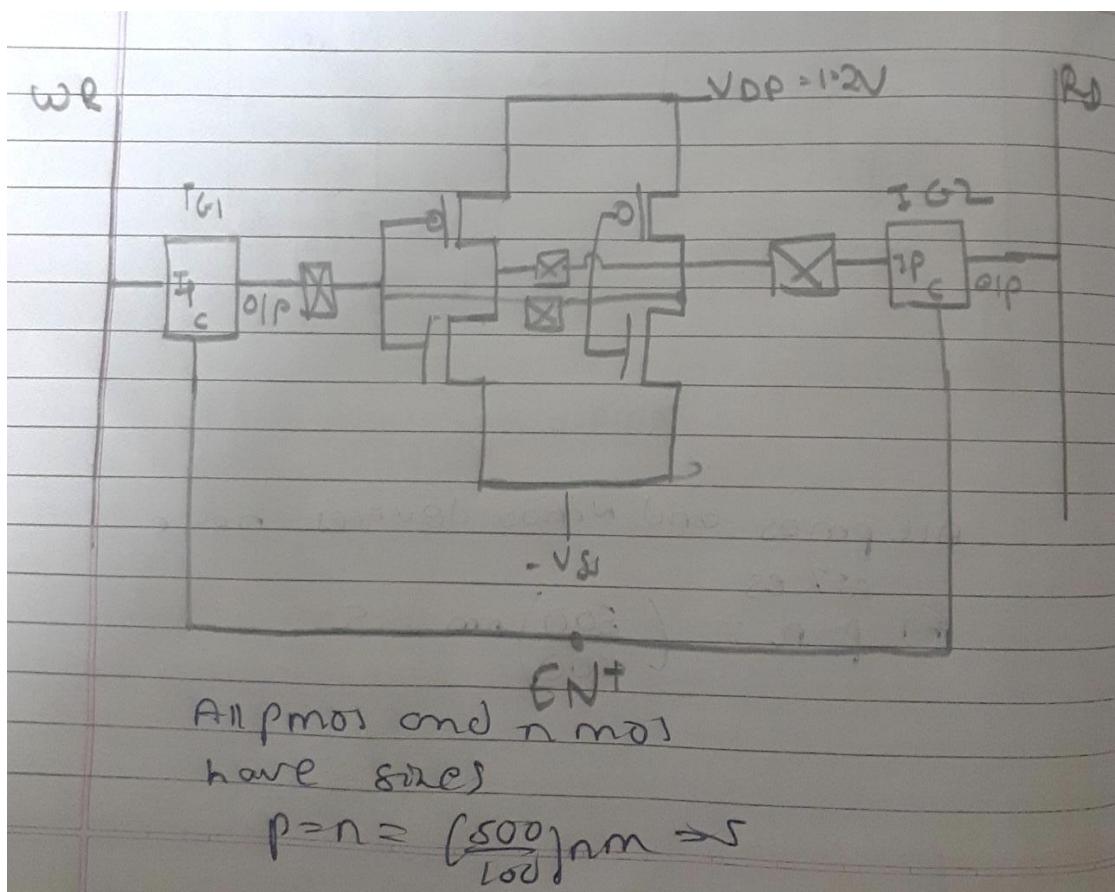


Class	:	
Batch	:	
Roll. No	:	
ABC ID	:	
Assignment No.	:	B.4.b
Assignment Name	:	1-bit SRAM ( Using TG S/W )
Date Of Performance	:	

## MOSFET-LEVEL SCHEMATIC of 1-bit SRAM Cell Using TG S/W :-



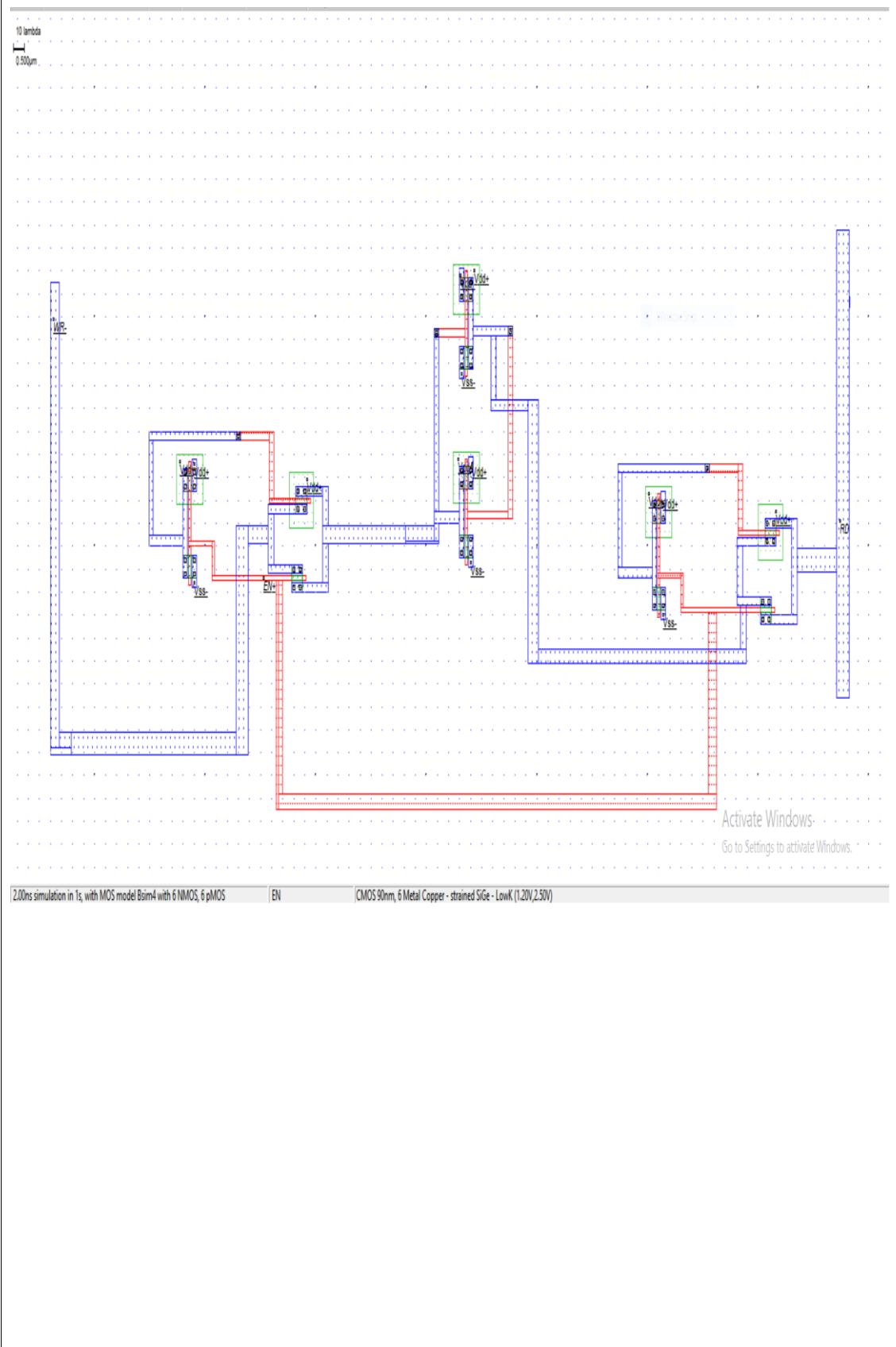
In the above Schematic :

- ✚ TG1 , TG2 : TG S/W's
- ✚ I1 , I2 : CROSS – COUPLED CMOS INVERTERS
- ✚ System is a PURE CMOS SYSTEM
- ✚ WR-line gets connected to RD line through TG1 , TG2 & I1-I2 pair
- ✚ TG1 = TG2 = ON / OFF , for C = EN = 1 / 0
- ✚ TG1 , TG2 Transmit "1" as STRONG-1 & "0" as STRONG-0
- ✚ I1 , I2 Transmit "1" as STRONG-0 , "0" as STRONG-1

Truth Table:-

EN	WR	RD
1	0	STRONG-1
1	1	STRONG-0
0	X	HOLD

## Layout (90 nm Foundry) : ( V<sub>dd</sub> = 1.2 V )

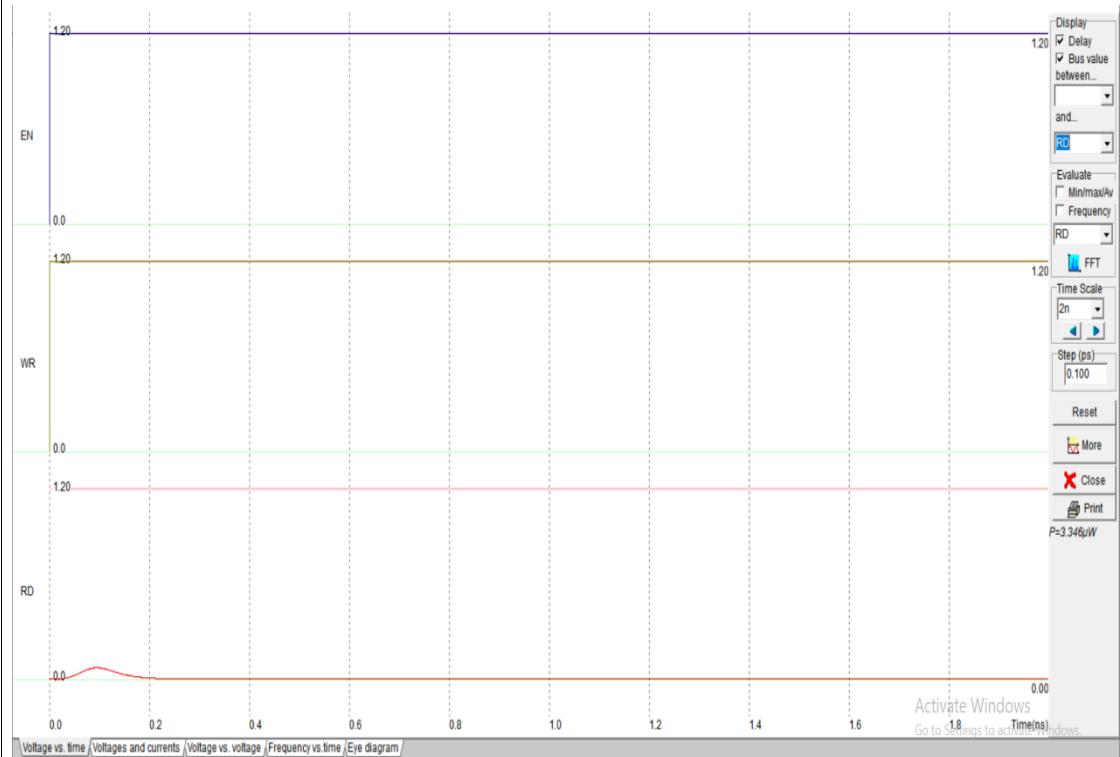


## Waveform:

1) EN=1, WR = 0, RD = **STRONG-1** ( RD = V<sub>dd</sub> = 1.2 V )



2) EN=1, WR = 1, RD = **STRONG-0** ( RD = -V<sub>ss</sub> = 0 V )



### 3) EN=0, WR = 0 / 1 , RD = HOLD ( NO CHANGE )



### Conclusion :-

- 1) Drawn the LAYOUT of 1-bit SRAM Cell Using TG S/W's for 90 nm Foundry.
- 2) Being a **Pure-CMOS System** ( TG S/W's & CMOS INVERTERS ) , it gives  
 $RD = S-1 / S-0$  for  $WR = 0 / 1$  respectively.
- 3) So , "0" is READ as S-1 ( Acceptable ) & "1" is READ as S-0 ( Acceptable )
- 4) *The reason for above is the Presence of TG S/W's on both sides of CMOS INVERTERS ( A Pure CMOS System )*