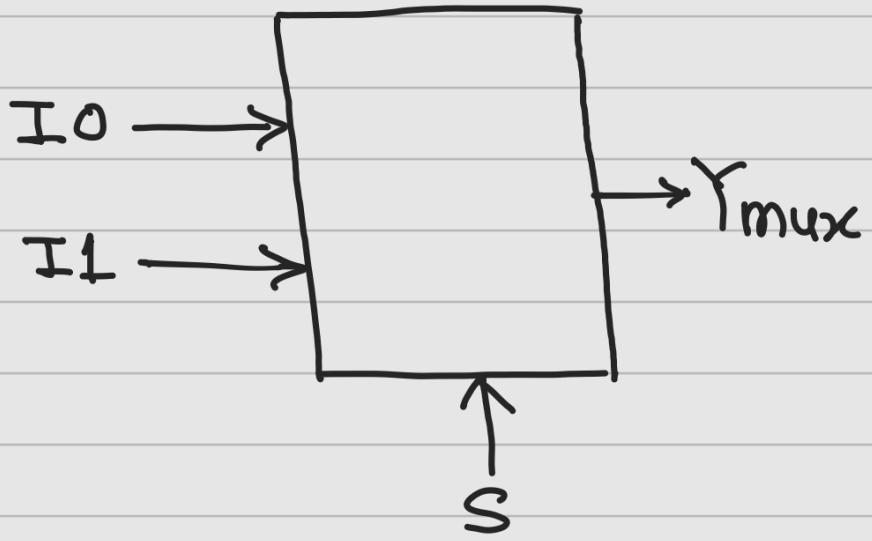
MOSFET- LEVEL SCHEMATIC OF 2:1 MUX (USING TG)

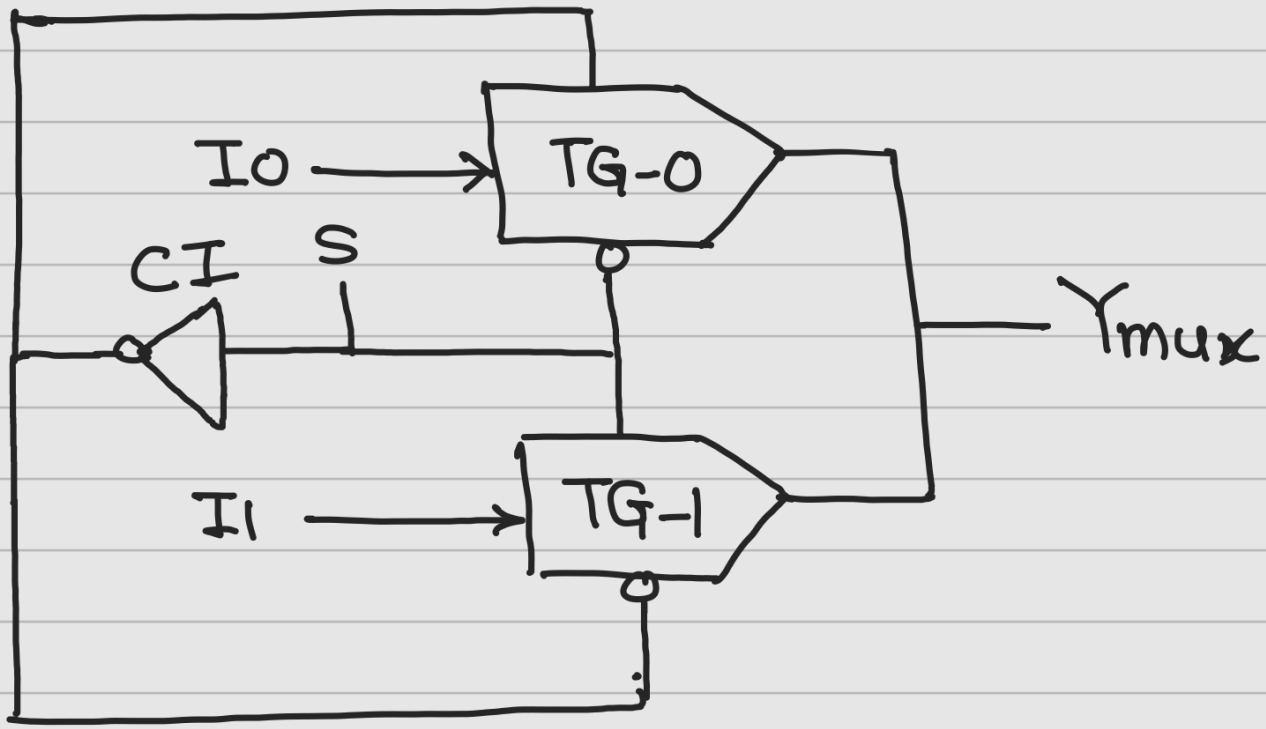
2:1 MUX



Truth-Table

S	Ymux
0	I0
1	I1

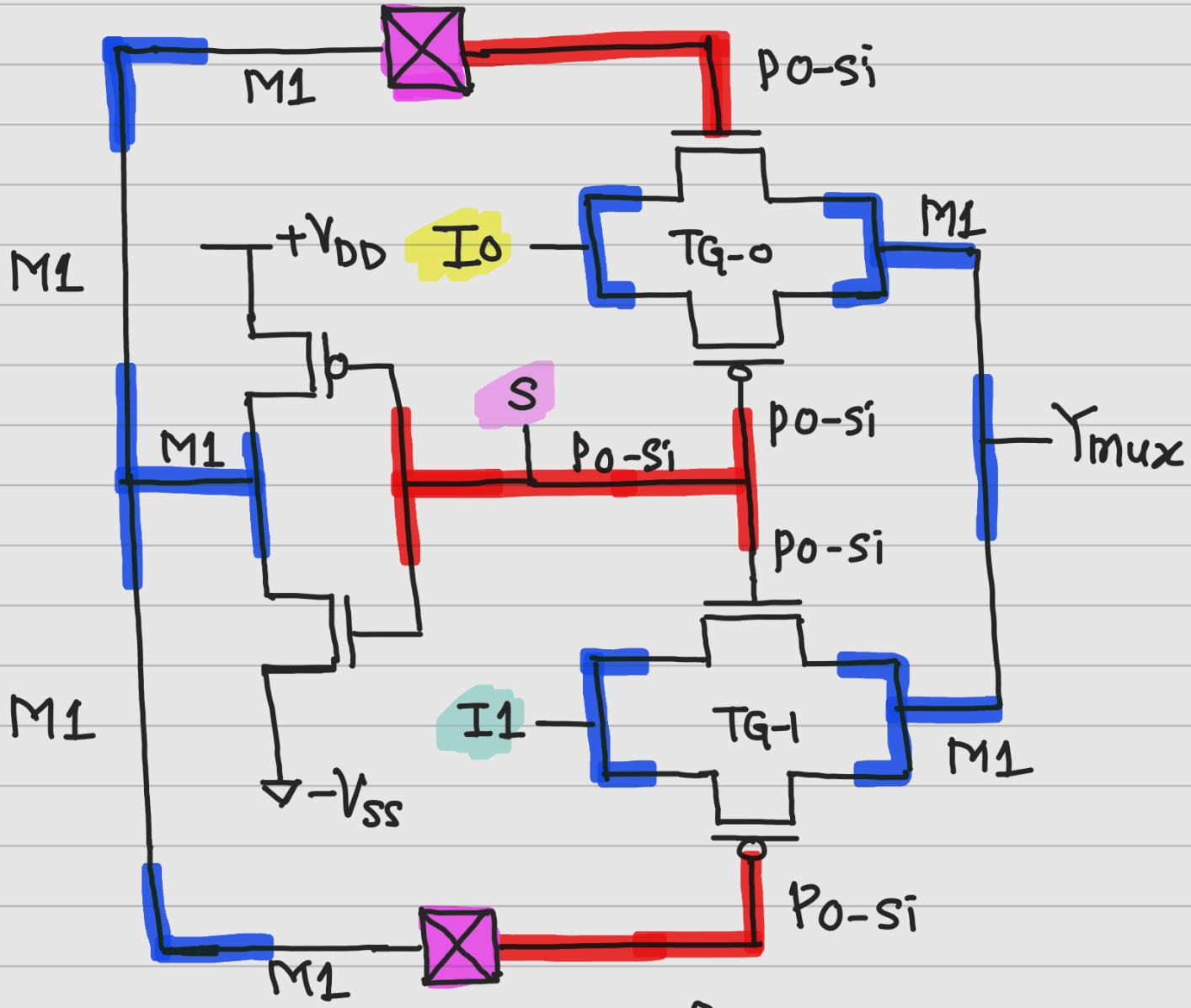
Symbol-Level Schematic



CI = CMOS Inverter

⊛ MOSFET-Level Schematic

Above Schematic Redrawn



$f_{Io} \simeq 4 \cdot f_{I1}$, $f_S \simeq f_{I1}/4$

⊠ ⇒ Metal-1 to Polysilicon contact

M1 ⇒ Metal-1 Layer

Po-Si ⇒ Polysilicon Layer

PMOS: $\frac{W_P}{L_P} = \left(\frac{500}{100}\right) nm = 5 = p$

NMOS: $\frac{W_N}{L_N} = \left(\frac{500}{100}\right) nm = 5 = n$

$\frac{p}{n} = 1$