Class	:	
Batch	:	
Roll. No	:	
ABC ID	:	
Assignment No.	:	B.1.d
Assignment Name	:	CMOS TRANSMISSION-GATE (TG)
Date Of Performance	:	

CONSTRUCTION & SYMBOLS OF TG

C = Control Signal (Applied to Gate of NMOS)
$\overline{C}$ = Inverted Control Signal (Applied to Gate of PMOS)
C= 1 : NMOS = PMOS = ON
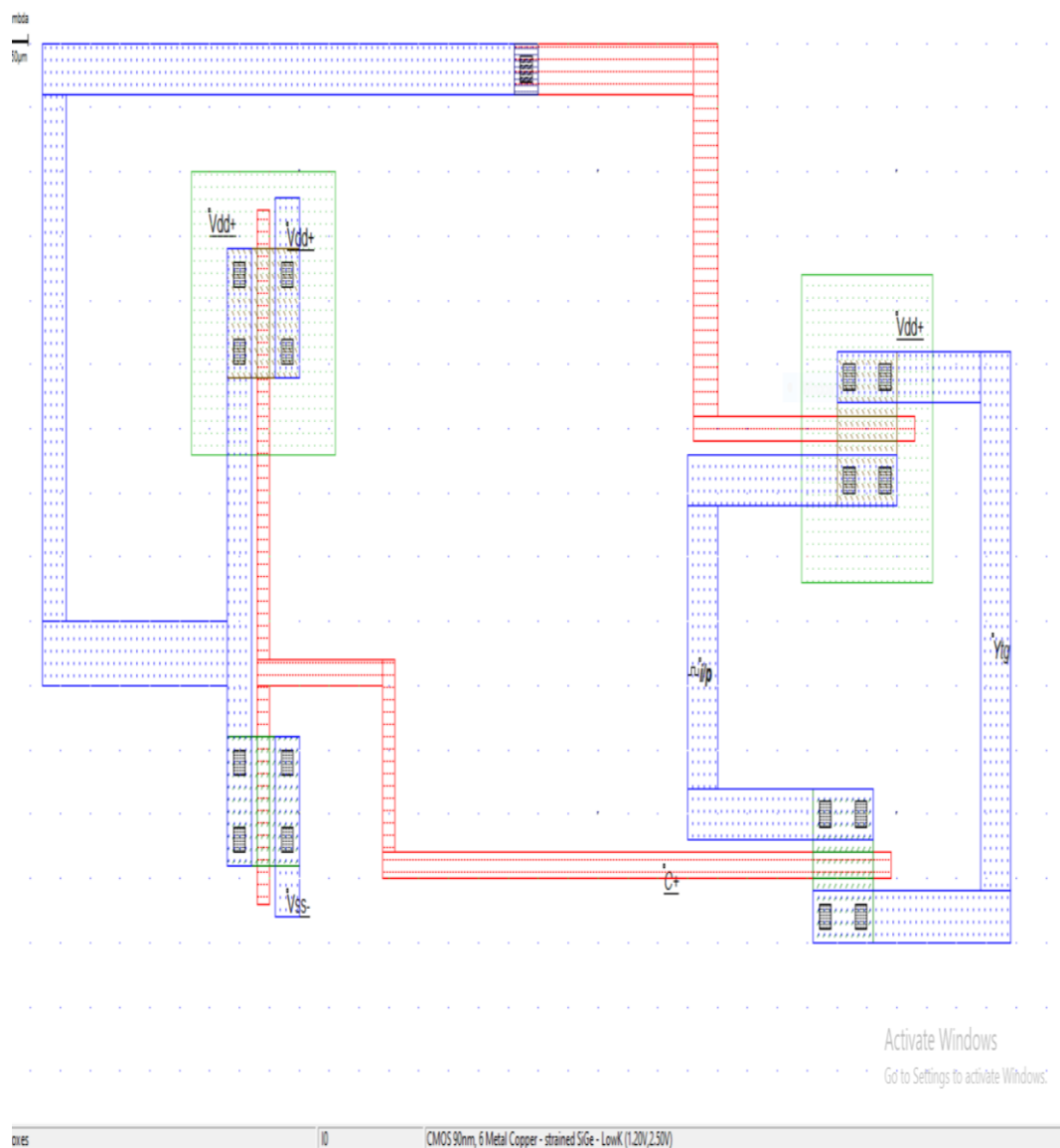O/P Node is Connected to I/P Node
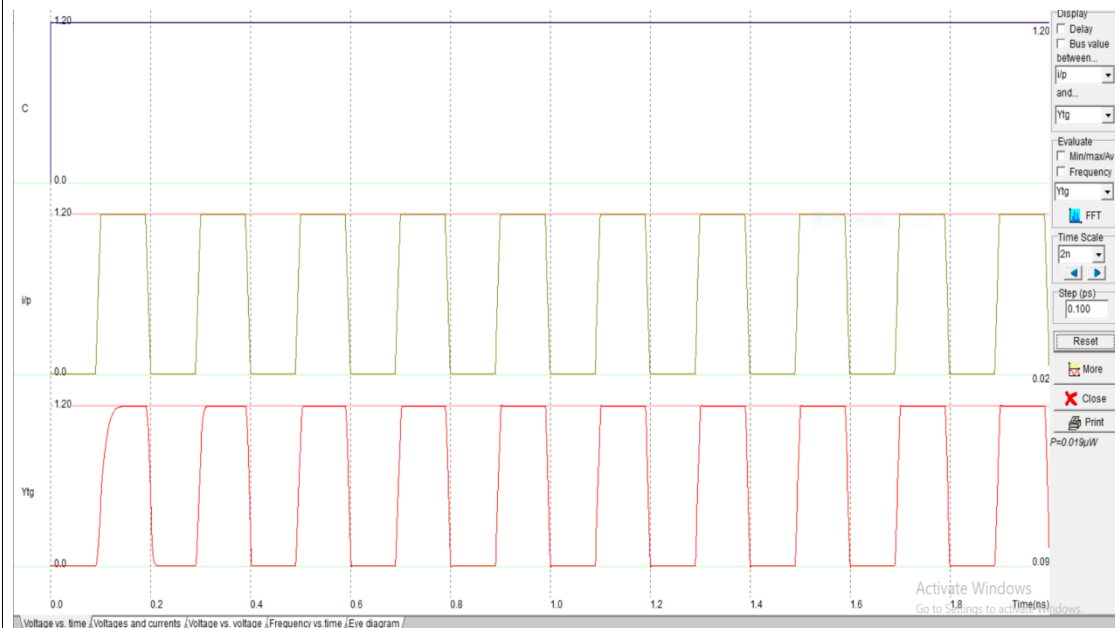
MOSFET-LEVEL SCHEMATIC of TG

TRUTH TABLE :

C	Y_{tg}
1	I/P
0	NO CHANGE

Layout (90 nm Foundry) : (V_{dd} = 1.2 V)

CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

WAVEFORMS:
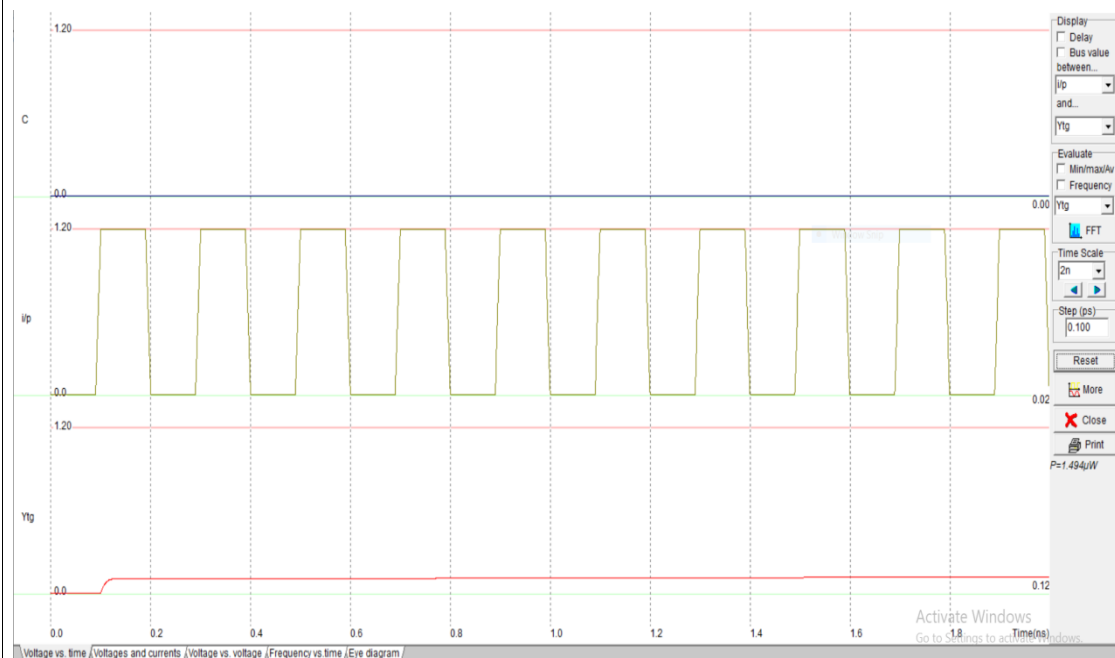
1) For C=1

O/P = S-1 (For I/P = 1)
O/P = S-0 (For I/P = 0)

2) For C=0

O/P Shows NO CHANGE in spite of Changes in I/P ,as O/P Node is DISCONNECTED from I/P Node

CONCLUSIONS :

1) Drawn the LAYOUT for CMOS TRANSMISSION GATE (TG) using 90 nm Foundry.
2) Being a **Pure-CMOS System** (PMOS // NMOS & CMOS INVERTER) , it gives both **S-1** & **S-0** as O/P.
3) **Power Dissipation** in Enabled Condition (C = 1) is just **0.019μW** thus exhibiting the Merit of Very Low Power Dissipation of CMOS Logic Family.
4) Power Dissipation in Disabled Condition (C = 0) is Very High (**1.494μW**)
5) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.