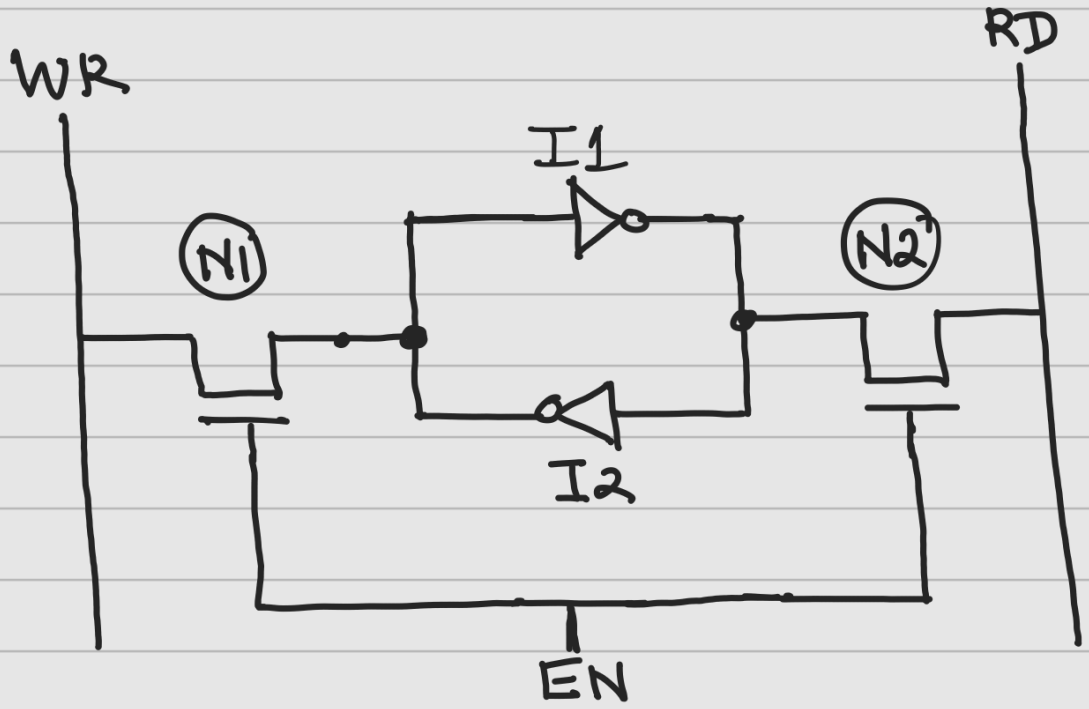
SYMBOL - LEVEL SCHEMATIC :-



I1, I2 : CMOS Inverter's
N1, N2 : NMOS switches
WR : Write- Line
RD : Read– Line
EN : Write - enable

✱ Operation :-

Case - 1 :- **EN = 1** ⟹ N1 = N2 = ON

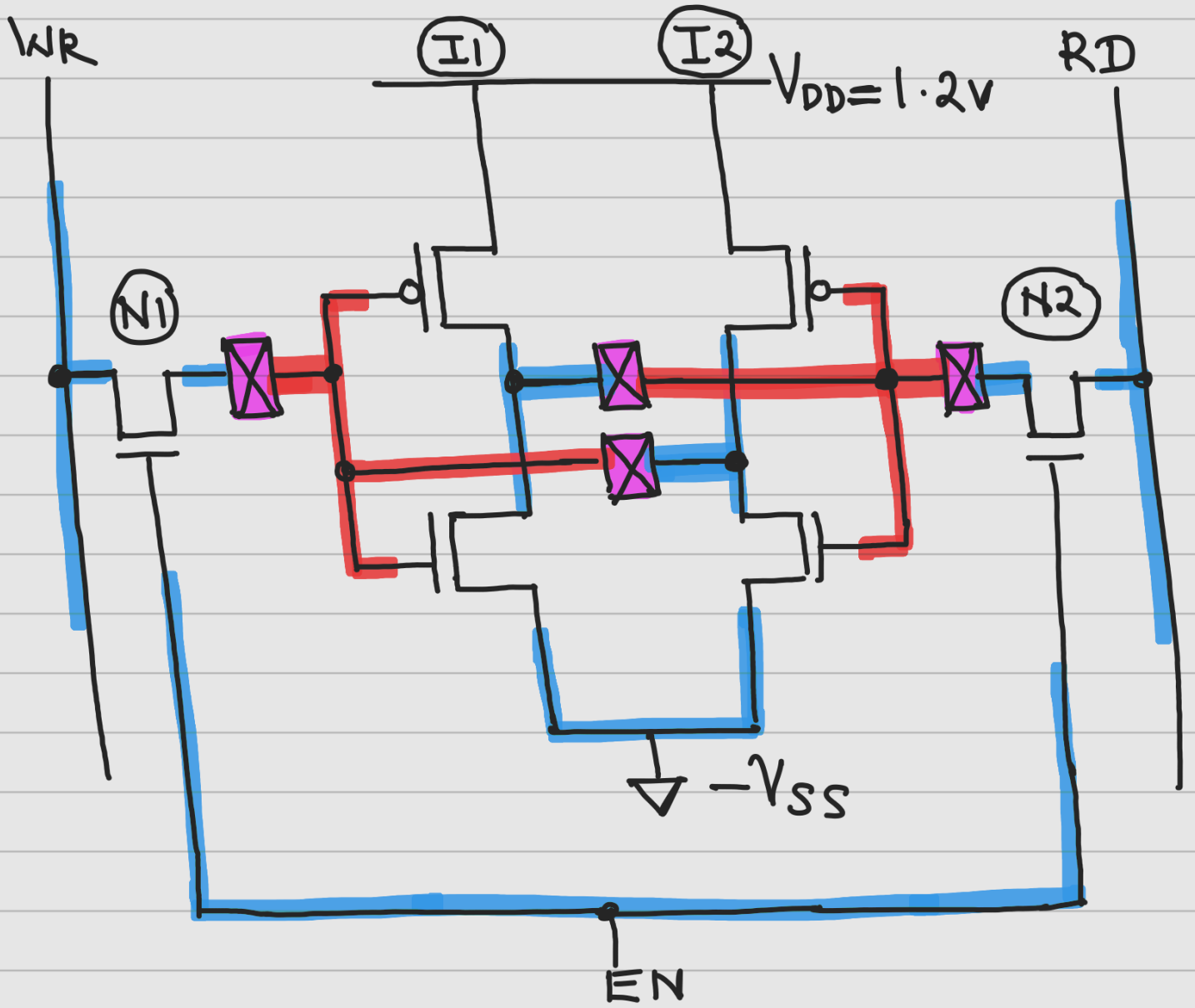
(a) **WR = 1** :
O/p of N1 = W-1
O/p of I1 = S-0
O/p of N2 = RD = **S-0**

(b) WR = 0
O/p of N1 = S-0
O/p of I1 = S-1
O/p of N2 = RD = **W-1**

Case -2 :- EN = 0 ⟹ N1 = N2 = OFF

RD- Line is disconnected from WR - line
∴ NO CHAGE condition.

✱ MOSFET-level Schematic:-



Metal-1 Layer

polysilicon Layer

✱ $\frac{W_P}{L_P} = \left(\frac{500}{100}\right)nm = 5 = p$

✱ $\frac{W_N}{L_N} = \left(\frac{500}{100}\right)nm = 5 = n$

✱ $\frac{p}{n} = \frac{5}{5} = 1 \Rightarrow$ Relative size.