High-Speed USB Converter Chip CH347

Datasheet

Version: 1B

http://wch.cn

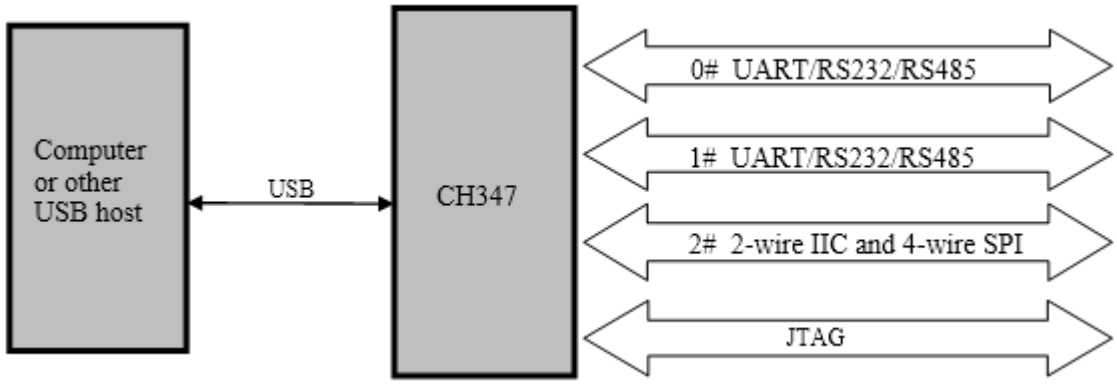
1. Overview

CH347 is a high-speed USB bus converter chip that provides UART, I2C and SPI synchronous serial interface and JTAG interface through USB bus.

In UART mode, CH347 provides two high-speed serial ports, supports RS485 UART transceiver enable control, hardware flow control, and common MODEM signals, used to extend serial ports for computer, or upgrade directly from normal serial devices or MCU to USB bus.

In synchronous serial interface mode, CH347 provides one 2-line I2C interface (SCL, SDA) and one 4-line SPI interface (SCS, SCK/CLK, MISO/SDI/DIN, MOSI/SDO/DOUT) to extend 2-line or 4-line synchronous serial port for computer to operate EEPROM, FLASH, sensors, etc.

In JTAG mode, CH347 provides a JTAG interface that supports either a 4-line or 5-line interface (TMS, TCK, TDI, TDO, and TRST) for extending JTAG interface for computer to operate devices such as CPU, DSP, FPGA, and CPLD.



2. Features

2.1. Introduction

- 480Mbps high-speed USB device interface, peripheral components only need crystal oscillator and capacitor.
- Built-in EEPROM with configurable parameters such as working mode, the chip of VID, PID, maximum current value, vendor and product information string.
- Supports only 3.3V power supply voltage.
- RoHS compliant TSSOP-20 lead free package.
- Multiple working modes, suitable for high-speed USB converter applications.
- Functional customization can be carried out according to industry batch requirements.

2.2. UART

- Built-in firmware, emulate standard UART interface, used to upgrade the original serial peripheral or expand additional UART via USB.
- Original serial applications are totally compatible without any modification in Windows operating system.
- Hardware full duplex UART interface, integrated independent transmit-receive buffer, supports communication baud rate varies from 1200bps to 9Mbps.
- UART supports 8 data bits, supports odd, even, and none parity, supports 1 or 2 stop bits.
- Built-in 12K bytes RX-FIFO and 4K bytes TX-FIFO for each UART.
- Supports common MODEM signals RTS, DTR, DCD, RI, DSR and CTS.
- Supports CTS and RTS hardware automatic flow control.
- Supports half-duplex, provides sending status TNOW which supports RS485 switching.
- Supports up to 8-channel GPIO input and output function.
- Supports RS232, RS485, RS422 interface, through external voltage converter chip.

2.3. I2C synchronous serial interface

- Works in Host/Master Host mode.
- 2 signal lines, SCL and SDA, supports 4 transmission speeds.
- With the cooperation of computer API, flexible operation of 2-line interface A/D, D/A, EEPROM and sensor components.

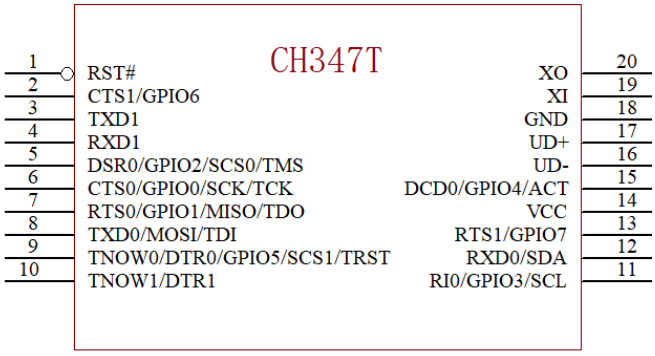
2.4. SPI synchronizes serial interface

- Works in Host/Master Host mode.
- Provide SCS, SCK/CLK, MISO/SDI/DIN, MOSI/SDO/DOUT four signal lines.
- Supports 2 chip select signal lines and can operate two SPI interface devices by time-sharing.
- Supports 8 bit /16 bit data structure, supports MSB and LSB transmission.
- Supports SPI mode 0/1/2/3, and supports transmission frequency configuration up to 60MHz.
- Supports hardware DMA sending and receiving.
- With the cooperation of computer API, flexible operation of FLASH, MCU, sensor and other components with 4-line interface.

2.5. JTAG interface

- Works in Host/Master Host mode.
- JTAG provides TMS, TCK, TDI, TDO, and TRST lines (optional).
- Supports high-speed USB data transfer.
- With the cooperation of computer API, flexible operation of CPU, DSP, FPGA, CPLD, MCU and other components.

3. Package



Package	Body size		Lead pitch		Description	Part No.
TSSOP-20	4.4mm	173mil	0.65mm	25mil	Thin small 20 pin patch	CH347T

Note: USB transceiver of CH347 is designed according to the built-in design of USB2.0. UD+ and UD- pins cannot be connected in series with resistors, otherwise the signal quality will be affected.

4. Pin definitions

4.1. General description

CH347 has multiple working modes, and the function and definition of the same pin in different working modes may be different. CH347 automatically configures the working mode by detecting the configuration pin status during power-up reset or external reset.

Note: FT indicates pin withstands 5V when used as an input.

4.2. Standard common pins

Pin No.	Pin Name	Pin Type	Pin Description
14	VCC	POWER	Power supply voltage input, requires an external decoupling capacitor
18	GND	POWER	Ground, connected to ground of USB bus directly
1	RST#	IN	Input of external reset, active low, built-in pull-up resistor
17	UD+	USB signal	Connect to USB D+ Signal directly, do not connect resistor in series
16	UD-	USB signal	Connect to USB D- Signal directly, do not connect resistor in series
19	XI	IN	Input of crystal oscillator
20	XO	OUT	Inverted output of crystal oscillator

4.3. Working mode configuration pins

Pin No.	Pin Name	Pin Type	Pin Description
10	DTR1/TNOW1	Input during reset (FT)	MODE0 configuration pin 0 for working mode when the chip is reset. Used with MODE1 pin, built-in pull-up resistor
13	RTS1/GPIO7	Input during reset (FT)	MODE1 configuration pin 1 for working mode when the chip is reset. Used with MODE0 pin, built-in pull-up resistor

4.4. Working mode 0 pins

Pin No.	Pin Name	Pin Type	Pin Description
8	TXD0	OUT	Transmit asynchronous data output of UART0, high when idle
12	RXD0	IN(FT)	Receive asynchronous data input of UART0, built-in pull-up resistor
3	TXD1	OUT	Transmit asynchronous data output of UART1, high when idle
4	RXD1	IN(FT)	Receive asynchronous data input of UART1, built-in pull-up resistor
9	DTR0/TNOW0 /GPIO5	OUT	MODEM output signal of UART0, data terminal ready, active low; RS485 transmit and receive control pin of UART0; General purpose GPIO5, used for IO input or output. During power-on, if DTR0 detects an external pull-down resistor, DTR0 and DTR1 switch to TNOW0 and TNOW1 respectively
10	DTR1/TNOW1	OUT	MODEM output signal of UART1, data terminal ready, active low; RS485 transmit and receive control pin of UART1
6	CTS0/GPIO0	IN(FT)	MODEM input signal for UART0, clear to send, active low; General GPIO0, used for IO port input or output

7	RTS0/GPIO1	OUT	MODEM output signal of UART0, request to send, active low; General GPIO1, used for IO port input or output. During power-on, if RTS0 detects an external pull-down resistor, disable the configuration parameters in the internal EEPROM and enable the default parameters delivered with the chip
2	CTS1/GPIO6	IN(FT)	MODEM input signal of UART1, clear to send, active low; General GPIO6, used for IO port input or output
13	RTS1/GPIO7	OUT	MODEM output signal of UART1, request to send, active low; General GPIO7, used for IO port input or output
11	RI0/GPIO3	IN(FT)	MODEM input signal for UART0, ring indicator, active low; General GPIO3, used for IO port input or output
15	DCD0/GPIO4	IN(FT)	MODEM input signal for UART0, data carrier detect, active low; General GPIO4, used for IO port input or output
5	DSR0/GPIO2	IN(FT)	MODEM input signal of UART0, data set ready, active low; General GPIO2, used for IO port input or output

4.5. Working mode 1/2 pins

Pin No.	Pin Name	Pin Type	Pin Description
3	TXD1	OUT	Transmit asynchronous data output of UART1, idle state is high level
4	RXD1	IN(FT)	Receive asynchronous data input of UART1, built-in pull-up resistor
10	DTR1/TNOW1	OUT	MODEM output signal of UART1, data terminal ready, active low; RS485 transmit and receive control pin of UART1
2	CTS1	IN(FT)	MODEM input signal of UART1, clear to send, active low
13	RTS1	OUT	MODEM output signal of UART1, requests to sent, active low
7	MISO	IN(FT)	4-line serial port data input, alias DIN or SDI,

			built-in pull-up resistor
8	MOSI	OUT	4-line serial port data output, alias DOUT or SDO
6	SCK	OUT	4-line serial port clock output, alias DCK
5	SCS0	OUT	4-line serial port chip selection output 0
9	SCS1	OUT	4-line serial port chip selection output 1
12	SDA	OUT IN(FT)	2-line serial port data input and output, built-in pull-up resistor
11	SCL	OUT	2-line serial port clock output, built-in pull-up resistor
15	ACT	OUT	USB configuration completed status output, active low

4.6. Working mode 3 pins

Pin No.	Pin Name	Pin Type	Pin Description
3	TXD1	OUT	Transmit asynchronous data output of UART1, idle state is high level
4	RXD1	IN(FT)	Receive asynchronous data input of UART1, built-in pull-up resistor
10	DTR1/TNOW1	OUT	MODEM output signal of UART1, data terminal ready, active low; RS485 transmit and receive control of UART1
2	CTS1	IN(FT)	MODEM input signal of UART1, clear to send, active low
13	RTS1	OUT	MODEM output signal of UART1, requests to sent, active low
8	TDI	OUT	Data output of JTAG interface
7	TDO	IN(FT)	Data input of JTAG interface, built-in pull-up resistor
6	TCK	OUT	Clock output of JTAG interface
9	TRST	OUT	Reset output of JTAG interface
5	TMS	OUT	Mode selection of JTAG interface
11, 12	GPIO	IN/OUT	General GPIO, used for IO port input or output
15	ACT	OUT	USB configuration completed status output, active low

5. Functional description

5.1. General description

CH347 is a high-speed USB bus converter chip that provides UART, common 2-line I2C and 4-line SPI synchronous serial interface, JTAG interface, etc.

VCC pin is the input of power supply, which requires 3.3V power supply voltage. The power pin VCC should be connected to an external power decoupling capacitor of about 0.1uF.

CH347 chip has a built-in power-on reset circuit. When the chip is operating, it needs to provide an external

8MHz clock signal to the XI pin. The clock signal can be generated by the built-in inverter of CH347 through crystal frequency stabilization oscillation. The peripheral circuit needs to connect an 8MHz crystal between the XI and XO pins, and the both pins connect to the ground with an oscillation capacitor of about 22pF.

CH347 has built-in all peripheral circuits required by the USB bus, including the embedded USB controller and USB-PHY, the series matching resistor of the USB signal line, and the 1.5K pull-up resistor required for the Device. The UD+ and UD- pins should be connected directly to the USB bus.

5.2. Working mode configuration

When CH347 is reset, the chip detects the level status of DTR1 (PIN10) and RTS1 (PIN13) pins. Chip working modes and their switching functions are described in the following table.

Working Mode	DTR1 and RTS1 Pin Status	Chip Function	Default Product ID
Mode 0	DTR1 is floating or high level, RTS1 is floating or high level	USB to high-speed dual UARTs. UART0 supports full MODEM signals, UART1 supports partial MODEM signals	55DAH
Mode 1	DTR1 is floating or high level, RTS1 is pulled down to low level	Vendor driver mode 3-in-1: USB to high-speed single UART + USB to 2-line I2C + USB to 4-line SPI	55DBH
Mode 2	DTR1 is pulled down to low level, RTS1 is floating or high level	HID Driver-free mode 3-in-1: USB to high-speed single UART + USB to 2-line I2C + USB to 4-line SPI	55DCH
Mode 3	DTR1 is pulled down to low level, RTS1 is pulled down to low level	2-in-1: USB to high-speed single UART + USB to JTAG interface	55DDH

Working Mode 0: USB to high-speed dual UARTs. On the computer, it will be recognized as two standard USB serial ports, suitable for the simultaneous use of dual UARTs requirements. UART0 supports full MODEM signals, and UART1 supports partial MODEM signals. Both UARTs support hardware flow control and RS485 serial port transmit/receive enable control.

Working Mode 1: Vendor driver mode 3-in-1, USB to high-speed single UART, USB to 2-line I2C and USB to 4-line SPI synchronous serial interface. On the computer, it will be recognized as a standard USB serial port and a custom interface for 2-line and 4-line synchronous serial interface communication, suitable for the simultaneous use of UART and 2-line or 4-line synchronous serial interface requirements. UART1 supports partial MODEM signals, hardware flow control, and RS485 serial port transmit/receive enable control. 4-line synchronous serial interface supports configurations such as mode, data bits, and data sequence.

Working Mode 2: HID Driver-free mode 3-in-1, USB to high-speed single UART, USB to 2-line I2C and

USB to 4-line SPI synchronous serial port. On the computer, it will be recognized as a class composite device with two customized HID interfaces (interface 0 is used for UART data upload and download, and interface 1 is used for 2-line and 4-line synchronous serial interface communication), suitable for the simultaneous use of UART and 2-line or 4-line synchronous serial interface, and it is not convenient to install the vendor's driver requirements. UART1 supports partial MODEM signals, hardware flow control, and RS485 serial port transmit/receive enable control. 4-line synchronous serial interface supports mode (Mode 0/1/2/3), data bits (8-bit/16-bit), and data sequence (MSB/LSB).

Working Mode 3: 2-in-1, USB to high-speed single UART and USB to JTAG interface. On the computer, it will be recognized as one standard USB serial port and one JTAG interface, suitable for the simultaneous use of UART and JTAG interface requirements.

5.3. UART

CH347 provides one or two UART, each UART includes TXD, RXD, CTS, RTS, and DTR pin, etc. UART0 supports all MODEM signals, and UART1 supports partial MODEM signal lines.

In UART mode, CH347 contains: data transfer pins, MODEM interface signal pins and auxiliary pins.

Data transfer pins contain: TXD0, TXD1 and RXD0, RXD1. RXDx is high when UART transmission is idle. TXDx is high when UART reception is idle.

MODEM interface signal pins and RS485 transmit and receive control pins contain: CTS0, RTS0, DTR0, CTS1, RTS1, and DTR1.

UART of CH347 has intergrated separate transmit and receive buffer, which supports simplex, half-duplex or full-duplex asynchronous serial communication.

Serial data of CH347 contains 1 low-level start bit, 8 data bits, 1/2 high level stop bits, and none/odd /even parity. Supports common baud rate: 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, 460800, 921600, 1M, 1.5M, 2M, 3M, 4M, 5M, 6M, 7M, 8M, 9M, etc. In working mode 0, the serial port baud rate supports up to 9M; while in other working modes, the serial port baud rate supports up to 7.5M.

Dual UARTs of CH347 both support CTSx and RTSx hardware automatic flow control which is not enabled by default, and can be enabled by VCP driver. If enabled, UART continues to send the next packet of data only when CTSx pin input is detected to be valid (active low), otherwise UART transmission is paused; UART automatically validates RTSx pin (active low) when the receive buffer is empty, invalidates RTSx pin until the receive buffer is nearly full, and then validates RTSx pin again when buffer is empty. With hardware automatic rate control, you can connect your CTSx pins to RTSx pins of the other side and your RTSx pins to CTSx pins of the other side.

The allowable baud rate error of CH347 UART receiving signal is not more than 2%, the baud rate error of UART transmitting signal is less than 1%.

In the Windows OS, after installing high-speed VCP vendor driver, it can emulate standard UART, so the mostly original serial applications are totally compatible, without any modification.

CH347 can supports up to 8-channel GPIO input and output function.

CH347 can be used to upgrade the original UART peripheral devices, or expand extra serial ports for computer via USB bus. Through external level conversion chip provides RS232, RS485, RS422 and other interface can

be further.

5.4. I2C synchronous serial interface

I2C/IIC synchronous serial interface of CH347 works in Host/Master host mode, includes SCL and SDA signal lines. SCL is used for unidirectional output synchronous clock, open-drain output and built-in pull-up resistor, SDA is used for bidirectional data input and output, open-drain output and input and built-in pull-up resistor.

The basic operation elements of I2C interface include: start bits, stop bits, bit output, and bit input.

Start bit is defined as SCL outputs falling edge when SDA is high level.

Stop bits is defined as SCL outputs rising edge when SDA is high level.

Bit output is defined as SDA outputs bit data when SCL is low level, and then SCL outputs high level pulse.

Bit input is defined as when SCL outputs high level pulse, SDA inputs bit data before falling edge.

I2C interface of CH347 supports 4 transmission speeds and can flexibly operate 2-line A/D, D/A, EEPROM and sensor components with the cooperation of computer API.

5.5. SPI synchronizes serial interface

4-line SPI synchronous serial interface of CH347 works in Host/Master Host mode, includes four signal lines SCSx, SCK(CLK), MISO(SDI/DIN) and MOSI(SDO/DOUT). SCSx includes SCS0 and SCS1, which can operate two SPI interface devices in time-sharing mode. Support 8-bit / 16-bit data structure, support MSB and LSB transmission, support SPI mode 0/1/2/3, support transmission frequency configuration, etc. Built-in hardware DMA, batch data can be quickly sent and read. With the cooperation of computer API, flexible operation of FLASH, MCU, sensor and other devices with 4-line interface.

5.6. JTAG interface

JTAG interface of CH347 works in Host/Master Host mode, includes five signal lines TMS, TCK, TDI, TDO, and TRST. TRST is an optional signal line. Supports the fast mode and bit-bang mode of user-defined protocol, transmission rate up to 30Mbit/S.

Provide computer USB high-speed driver and USB to JTAG TAP function library, support secondary development and 1.8V, 2.5V interface level of the single chip scheme, used to build customized USB to high-speed JTAG debugger, FPGA downloader, CPU programmer and other products.

5.7. Chip parameter configuration

In larger batch applications, vendor identification code (VID) and product identification code (PID) and product information of CH347 can be customized.

In less batch applications, it can use the built-in EEPROM for parameter configuration. After user installs VCP vendor driver, through configuration tool CH34xSerCfg.exe provided by chip vendor, it can be flexibly configured the vendor identification code (VID), product identification code (PID), maximum current value, BCD version number, vendor information and product information string and other descriptor, etc.

6. Parameters

6.1. Absolute maximum ratings

Critical state or exceeding maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter Description	Min	Max	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-40	125	℃
VCC	Supply voltage (VCC connects to power, GND to ground)	-0.3	4.0	V
VUSB	USB signal voltage	-0.5	3.8	V
VIO5	Input voltage on the pin withstanding 5V	-0.5	5.6	V
VIO3	Input voltage on other pins	-0.5	VCC+0.3	V

6.2. Electrical characteristics

Test conditions: TA=25℃, VCC=3.3V, exclude pins connected to USB bus.

Name	Parameter Description	Min	Typ	Max	Unit
VCC	Supply voltage (VCC power supply, GND connects to ground)	3.0	3.3	3.6	V
ICC	Supply current when the chip is working normally	28	38	50	mA
ISLP	Supply current (USB suspend)	180	260	350	uA
VIL	Low level input voltage	0	/	0.8	V
VIH3	High level input voltage on the pin not withstanding 5V	2.0	/	VCC	V
VIH5	High level input voltage on the pin withstanding 5V	2.0	/	5.0	V
VOL	Low level output voltage (8mA sunk current)	/	/	0.4	V
VOH	High level output voltage (8mA output current)	VCC-0.4	/	/	V
RPU	Built-in pull-up equivalent resistor	30	40	60	KΩ
VPOR	Threshold voltage for power-up/power-off reset	1.9	2.2	2.5	V
VESD	ESD electrostatic withstand voltage (HBM)	4	/	/	KV

6.3. Timing parameters

Test conditions: TA=25℃, VCC= 3.3V.

Name	Parameter Description	Min	Typ	Max	Unit
TRSTD	Reset delay after power-up or external reset input	15	28	40	mS
TSUSP	Detect the USB automatic suspension time	3	5	9	mS
TWAKE	Wake-up completion time after chip sleep	0.3	0.5	2	mS

7. Applications

7.1. USB to dual UARTs

The figure below is the USB to dual-channel high-speed TTL converter circuit realized by CH347, which works in mode 0.

The signal lines in the figure can only be connected to RXDx, TXDx, and public ground. CTSx, RTSx, DTRx can be selected as needed, and all can be not connected when not needed.

If DTR0 is connected to a 4.7KΩ pull-down resistor, DTR0 and DTR1 functions as TNOW0 and TNOW1 respectively, indicating UART sending status and controlling RS485 transceiver switching.

P1 is USB interface, and USB bus contains a pair of 5V power lines and a pair of data signal lines. Usually, the color of +5V power line is red, the black is ground. D+ signal line is green and the D- is white. The supply current provided by USB bus can up to 500mA.

P2 and P3 are TTL connection pins of two serial ports, including 3.3V, GND, RXDx, TXDx, RTSx, CTSx, and DTRx pins. Level conversion chip can be added to realize signal conversion (must support high baud rate) from TTL to RS232, RS485 and RS422, etc.

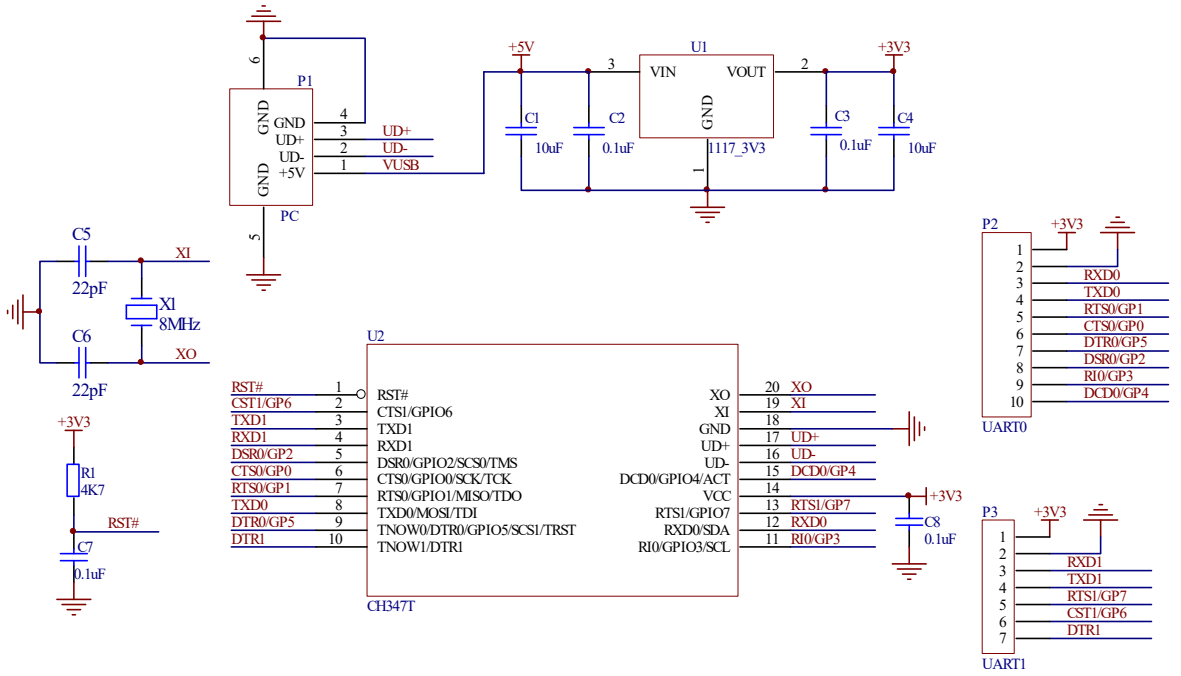
VCC pin of CH347 inputs 3.3V power supply voltage, each power pin should be connected to a power decoupling capacitor with a capacity of about 0.1uF. In the image, C8 is power decoupling capacitors.

Crystal X1, capacitors C5 and C6 are used in clock oscillation circuit of CH347. The frequency of X1 is 8MHz± 0.4%, C5 and C6 are monolith or high-frequency ceramic capacitors with a capacity of about 22pF. R1 and C7 are optional components.

It is recommended to add ESD protection device for USB signal line. The parasitic capacitance of ESD chip should be less than 2pF, such as CH412k.

It is recommended that the serial port peripherals and CH347 use the same power supply. Otherwise, the I/O pin reverse current when the serial port peripherals are powered separately must be considered.

When designing the PCB, pay attention to: the decoupling capacitor C8 gets as close to the connected power pin of CH347 as possible. The D+ and D- signal lines of the USB interface are routed close to parallel according to the high-speed USB specification to ensure the characteristic impedance, and providing ground or copper on both sides to reduce signal interference from the outside.

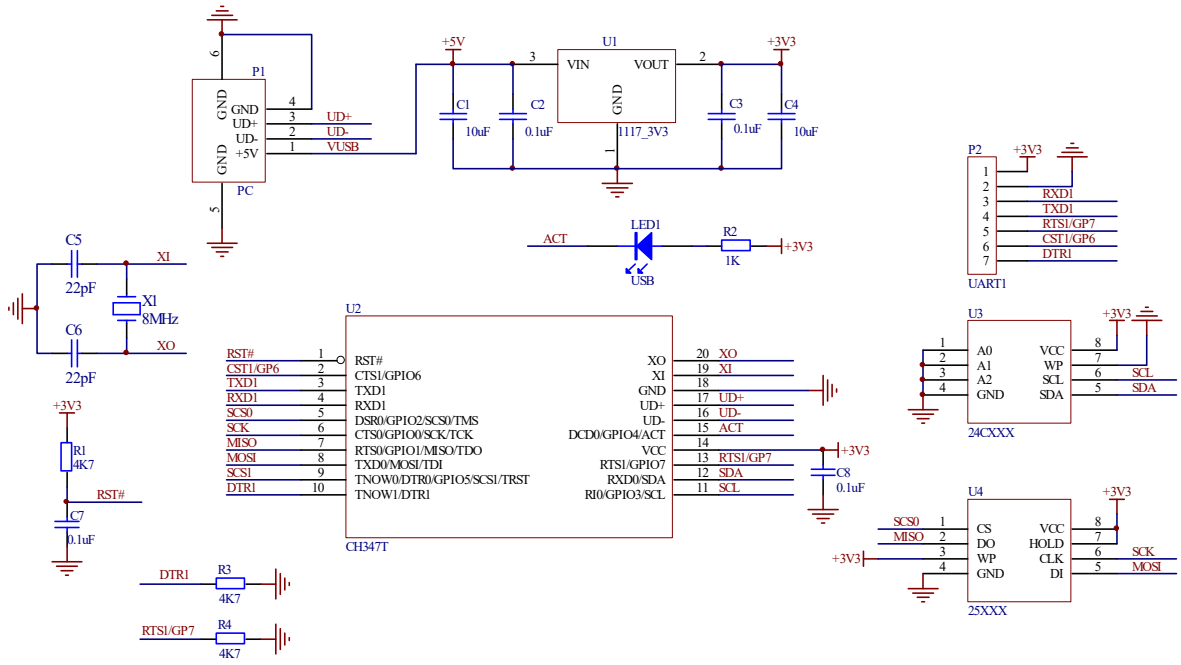


7.2. USB to SPI, USB to I2C, USB to UART 3-in-1

The figure below is the reference circuit diagram of USB to high-speed single UART and 2-line and 4-line synchronous serial interface realized by CH347. Removing R3 but keeping R4 to set the chip to work in mode 1, removing R4 but keeping R3 to set the chip to work in mode 2.

P1 is USB interface, and P2 is TTL connection pin of UART, including VCC, GND, RXD1, TXD1, RTS1, CTS1 and DTR1 pins. TTL to RS232, RS485, RS422 and other signal conversions can be achieved by adding level conversion components.

U3 is a 2-line synchronous serial interface I2C device. U4 is a 4-line synchronous serial interface SPI device. It is recommended that the peripherals use the same power supply as CH347.



7.3. USB to JTAG, USB to UART 2-in-1

The figure below is the reference circuit diagram of USB to high-speed single UART and JTAG interface realized by CH347. Resistors R3 and R4 set the chip to work in mode 3.

P1 is USB interface, and P2 is TTL connection pin of UART, including VCC, GND, RXD1, TXD1, RTS1, CTS1 and DTR1 pins. TTL to RS232, RS485, RS422 and other signal conversions can be achieved by adding level conversion components.

P3 is a JTAG interface, directly connected to FPGA, CPU and other chips, can also be customized to provide 1.8V or 2.5V interface level of the single chip scheme.