Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges

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***Abstract*— Gallium nitride (GaN) power devices are an emerging technology that have only recently become available commercially. This new technology enables the design of converters at higher frequencies and efficiencies than those achievable with conventional Si devices. This paper reviews the characteristics and commercial status of both vertical and lateral GaN power devices, providing the background necessary to understand the significance of these recent developments. In addition, the challenges encountered in GaN-based converter design are considered, such as the consequences of faster switching on gate driver design and board layout. Other issues include the unique reverse conduction behavior, dynamic $R_{ds,on}$, breakdown mechanisms, thermal design, device availability, and reliability qualification. This review will help prepare the reader to effectively design GaN-based converters, as these devices become increasingly available on a commercial scale.**

***Index Terms*— Gallium nitride (GaN), heterojunction field-effect transistor (HFET), high-electron mobility transistor (HEMT), wide bandgap (WBG).**

I. Introduction

WIDE bandgap (WBG) devices are an enabling technology for high-frequency, high-efficiency power electronics. WBG semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), provide advantages over conventional silicon power devices, as shown in Fig. 1. The higher breakdown field of a WBG semiconductor allows for devices to be optimized with thinner drift regions, resulting in power devices with lower specific ON-resistance. The high mobility of GaN further reduces the ON-resistance. This allows a smaller die size to achieve a given current capability, and therefore lower input and output capacitances. Higher saturation velocity and lower capacitances enable faster switching transients. In total, the material properties of WBG semiconductors result in a device with lower ON-resistance and switching losses than a Si device with comparable voltage and current capabilities [1]–[5]. Though SiC excels in high-temperature applications, the material characteristics of GaN are superior in high-efficiency, high-frequency converters. GaN power devices rated up to the 650 V have recently become commercially available, and GaN-based converter design has become a popular topic.

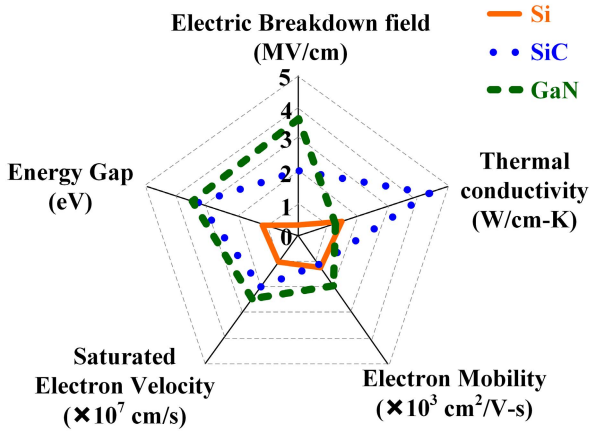

Fig. 1. Comparison of Si, SiC, and GaN for power semiconductor applications [1], [2].

Before designing power electronics with GaN power devices, it is useful to understand their characteristics and the challenges that typically accompany such a project. Several review and survey papers have been published on the relative characteristics of WBG devices, including the benefits and design challenges associated with each [1]–[6]. Other reviews, such as [7]–[11], have specifically provided background on GaN power devices and GaN-based converter design. Some of these reviews focus on one particular GaN technology or research direction, rather than covering the full range of commercial devices available today. In addition, the significant developments in the past few years require an update to these prior works. Therefore, this review aims to cover the aspects of GaN power devices that are relevant to the converter designer, as the landscape of commercially available devices continues to change. This includes the explanation of device physics properties to an audience who may not have device physics backgrounds, as well as exploring converter design elements that are not commonly required for Si-based power electronics.

Section II covers the fundamental technology of vertical GaN devices, as well as their commercial status and some of the remaining challenges left to overcome. Section III similarly discusses the basic structures and commercial status of lateral GaN devices and some of their unique properties. Section IV

Manuscript received January 10, 2016; revised May 25, 2016; accepted June 9, 2016. Date of publication June 21, 2016; date of current version July 29, 2016. This work was supported in part by the Engineering Research Center Program within the National Science Foundation and the Department of Energy under Award EEC-1041877, in part by the CURENT Industry Partnership Program, and in part by the Bredesen Center for Interdisciplinary Research and Graduate Education. This paper was presented at the 2014 IEEE Workshop on Wide-Bandgap Power Devices and Applications, Knoxville, TN, USA, October 2014. Recommended for publication by Associate Editor Jin Wang.

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Digital Object Identifier 10.1109/JESTPE.2016.2582685

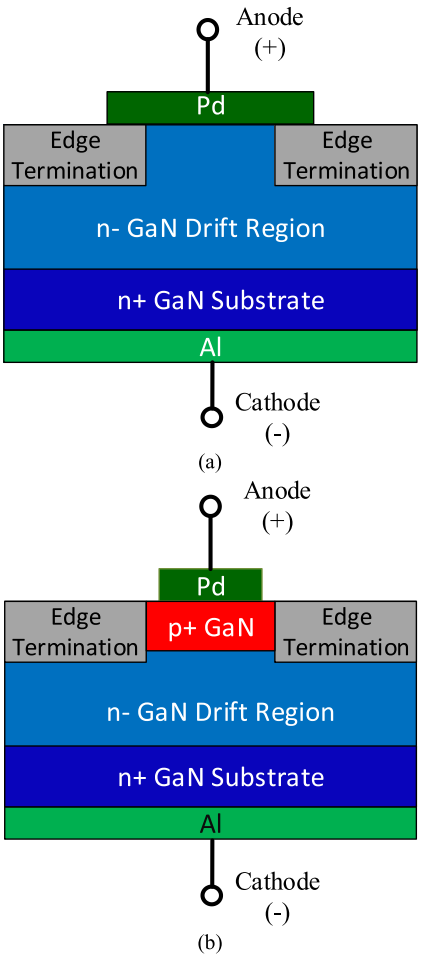

Fig. 2. Vertical GaN-on-GaN diodes, including (a) Schottky and (b) p-n junction [13].

reviews several important design challenges for GaN-based converters.

II. Vertical Devices

Vertical GaN devices, using structures similar to their Si and SiC counterparts, can take greatest advantage of the superior GaN material properties. However, the lack of availability of high-quality, low-cost GaN wafers has limited these prospects. This section will review the recent progress in the commercialization of vertical GaN devices.

A. GaN-on-GaN Vertical Devices

Avogy and HRL have publicly disclosed efforts to develop and commercialize vertical devices through the Strategies for Wide Bandgap, Inexpensive Transistors for Controlling High-Efficiency Systems (SWITCHES) program, funded by ARPA-E [12]. HRL has yet to announce any new vertical devices from this research, but Avogy has published some of its recent progress.

The first vertical structures published by Avogy were diodes, including the Schottky and p-n diodes shown in Fig. 2. Schottky diodes have been developed with blocking voltages up to 600 V, as well as p-n diodes up to 1700 V [13].

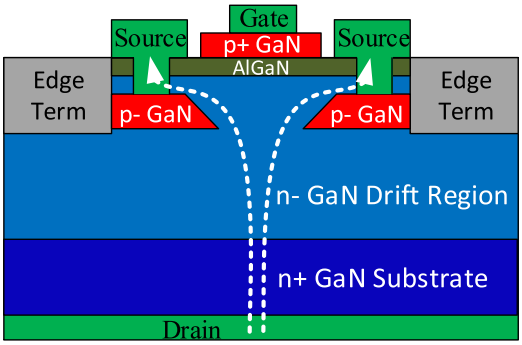

Fig. 3. Vertical GaN-on-GaN normally-OFF JFET [16].

The p-n junction diodes have also been fabricated with relatively large die areas, up to 16 mm^2, able to block 700 V and handle pulsed currents up to 400 A [14]. Samples have been announced on the Avogy website for 600, 1200, and 1700 V diodes with rated average current up to 5 A, in TO-220 packages [15].

Avogy has also developed a vertical GaN FET with 1.5-kV blocking capability and 2.3-A saturation current. The device, shown in Fig. 3, is a combination of the conventional JFET structure and the heterojunction AlGaN/GaN structure used in lateral devices. With a threshold voltage of 0.5 V, this device is enhancement-mode (e-mode) and therefore normally-OFF [16]. However, this device is not yet commercially available.

B. GaN-on-Si Vertical Devices

Vertical devices generally require homoepitaxial fabrication, meaning that the substrate and epitaxial layers are fabricated with the same type of semiconductor (i.e., GaN-on-GaN). However, MIT has developed a method of vertical MOSFET and diode fabrication using a heteroepitaxial GaN-on-Si structure, by etching through the Si substrate on the bottom side of the device to expose the GaN drift region [17]. Cambridge Electronics, Inc. (CEI) has recently begun commercializing some of the GaN technology developed by MIT. Samples of CEI's GaN FETs have been announced at voltage ratings of 200 and 650 V, with ON-resistances of 550 and 290 mΩ [18].

Although the exact structure of the CEI devices has not been published, this device may utilize one of the patented vertical structures from [17], such as the GaN-on-Si MOSFET shown in Fig. 4. In order to achieve a fully vertical current path, the drain contact is metallized in a recess that is etched completely through the substrate and buffer layers, so that it directly contacts the bottom side of the GaN epitaxial layer [17]. This technique combines the performance benefits of vertical GaN MOSFETs with the lower cost of Si wafers. With the current challenges to produce GaN wafers at costs competitive with Si or SiC, this presents an interesting alternative to vertical GaN-on-GaN devices.

C. GaN Wafer Fabrication

Although wafer fabrication itself is not relevant in the converter design process, affordable GaN wafers are an important step toward the commercialization of vertical GaN devices.

TABLE I
COMPARISON OF GaN WAFER FABRICATION METHODS [19]

Fabrication Method	Approximate Growth Rates		Largest Crystal Size		Defect Density	Challenges
	μm/hr	mm/day	On Substrate	Boule	cm^{-2}	
HVPE	100	2.4	> 6 inch	--	10^5-10^6	Stresses, wafer curvature, growth front breakdown, growth direction
HNPSG	3	0.07	2 inch	Few mm	10^1-10^2	Scaling, growth rates, purity
Na-Flux	30	0.7	4 inch	Few mm	10^2-10^5	Scaling, sustained growth rates
Ammonothermal	4	0.1	--	> 2 inch	10^4	Growth rates, purity

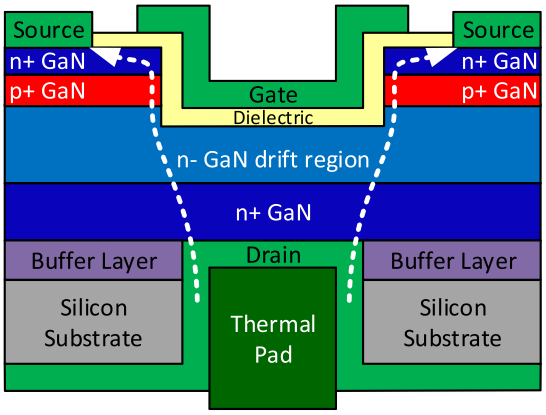

Fig. 4. Vertical GaN-on-Si MISFET [17].

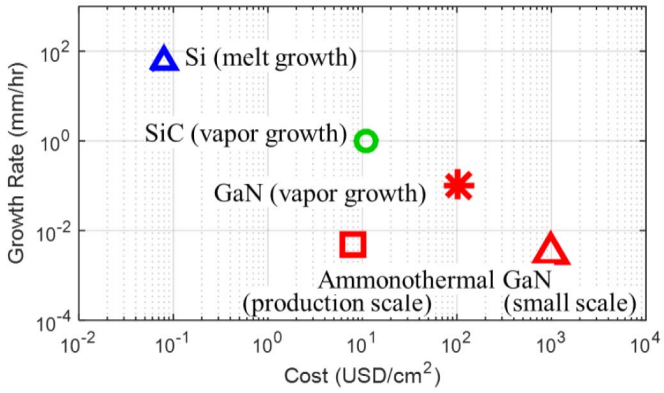

Fig. 5. Cost and growth rate comparison of wafers with different growth techniques [19].

These wafers form the substrate of a GaN-on-GaN device, on which the drift region is epitaxially deposited. As opposed to the melt-growth method used to produce Si wafers, GaN wafers are typically produced using hybrid vapor-phase epitaxy (HVPE) or chemical vapor deposition on a foreign material such as sapphire. The foreign material is then removed, leaving only the GaN layer of the wafer. This process is sometimes referred to as pseudobulk wafer fabrication, and presents many challenges due to the lattice mismatch between GaN and the foreign material [19].

Other technologies are currently being researched to fabricate true bulk GaN wafers, without the need for foreign substrates. The three most promising technologies are high nitrogen pressure solution growth (HNPSG), low pressure solution growth with sodium flux (Na-flux), and ammonothermal growth. HNPSG and Na-flux methods have been used to produce GaN on foreign substrates with several inches in diameter, and more limited success in producing true bulk GaN. Ammonothermal growth has been the most successful in the production of bulk GaN, with over 2 in in diameter fabricated in boule form. Each of these methods has its own challenges, as listed in Table I.

Fig. 5 shows the relative cost and growth rates of GaN wafers from vapor and ammonothermal methods based on current predictions, as compared with Si wafers produced with seeded melt-growth and SiC wafers produced with seeded sublimation. The ammonothermal method has the potential to drastically reduce the cost of GaN wafer fabrication at the production scale, but the current cost for small-scale ammonothermal GaN growth cannot compete with more established HVPE [19].

III. LATERAL DEVICES

Because vertical GaN devices have not yet been produced on a commercial level, most of the GaN devices available today are lateral heterojunction field-effect transistors (HFETs), also known as high electron mobility transistors (HEMTs). These devices are typically rated at 600–650 V, although higher voltage devices have been announced by manufacturers. Because of the lateral heterojunction structure, these devices are fundamentally different from MOSFETs and have unique characteristics.

A. Fundamental HFET Structure

Fig. 6 shows the basic structure of the GaN HFET. The principle feature of this structure is the AlGaN/GaN heterojunction. At the interface between these two layers, a layer of high-mobility electrons called "two-dimensional electron gas" (2DEG) forms as a result of the crystal polarity, and is also augmented by piezoelectric crystal strain due to the lattice mismatch between AlGaN and GaN. The 2DEG forms a native channel between the source and drain of the device.

The substrate is typically Si, but other materials such as SiC, sapphire, and diamond can be used. In order to deposit the GaN layer on the substrate, a buffer layer must be deposited that provides strain relief between the GaN and the foreign material. This buffer often includes several thin layers of GaN, AlGaN, and AlN.

Because of the native 2DEG channel, the HFET is inherently a depletion-mode (normally-ON) device. This is not desirable for voltage-source converters, because of the potential for shoot-through during startup or loss of control power. Several methods have, therefore, been used to fabricate normally-OFF GaN HFETs [7].

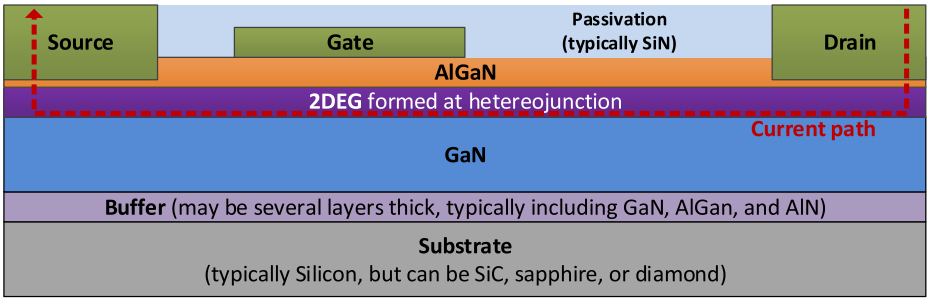

Fig. 6. Basic structure of depletion-mode lateral GaN HFET (not drawn to scale) [7].

TABLE II
COMMERCIAL CASCODE DEVICES

Manufacturer	Voltage Rating (V)	Current Rating (A)	$R_{ds,on}$ (mΩ)	Q_g (nC)	Package	Availability
Transphorm [23]	600	9	290	6.2	PQFN/ TO-220	Online ordering
		17	150	6.2		
		34	52	19	TO-247	
International Rectifier / Infineon [20]	600	10	125	--	PQFN	Samples
MicroGaN [22]	600	--	320	--	TO-263	Samples
RFMD/Qorvo [24],[25]	650	25	85	16.2	PQFN	Discontinued
		30	45	15.7	TO-247	
Fujitsu [26]	500	--	100	14	TO-220	Unknown
VisIC [27],[28]	650	50	15	35	PQFN	Samples
Texas Instruments [29]	600	--	70	--	PQFN	Unknown

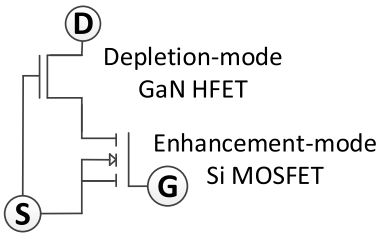

Fig. 7. Device structure for the normally-OFF GaN cascode.

B. Cascode Devices

A normally-OFF GaN device can be made with a depletion-mode HFET, using the cascode structure shown in Fig. 7. A cascode device requires copackaging of the depletion-mode HFET with a low-voltage e-mode MOSFET, typically Si. The two dies are connected in such a way that the output (drain–source) voltage of the MOSFET determines the input (gate–source) voltage of the HFET. Both devices share the same channel current while on, and the blocking voltage is distributed between them while off.

The two dies are connected inside the package with wire bonds or in a planar architecture. The switching performance of the cascode device relies heavily on the parasitic inductances in the package, especially between the two dies, and also on how well the junction capacitances of the two are matched. If the inductances are too high, or the capacitances are not matched well, the switching losses can increase significantly.

Table II shows the commercial status of cascode GaN devices. Transphorm is the only vendor currently selling cascodes on a large scale, although International Rectifier and MicroGaN have produced engineering samples. All three are rated at 600 V and use GaN-on-Si HFETs. MicroGaN has also produced a version of their cascode that acts as a diode rather than an active FET [20]–[23].

RFMD was selling engineering samples of their 650 V GaN-on-SiC device in 2014, but has since discontinued this product line. The use of a SiC substrate allows for improved performance over GaN-on-Si cascodes, but this is not as common as GaN-on-Si due to the higher cost of SiC wafers.

Texas Instruments and VisIC were also included in Table II, but it is important to note that they do not use the cascode circuit described in Fig. 7. However, these devices utilize the same concept, where a depletion-mode GaN HFET is connected in series with other electronics inside the package to create a normally-OFF device. The key difference between these devices and a cascode is that the gate driver for VisIC and TI connects directly to the gate terminal of the GaN HFET, but not directly to the source terminal, whereas a cascode allows connection to the GaN gate but not its source. In either case, the gate–source voltage is controlled by additional electronics inside the package. The VisiC device can be driven by a conventional MOSFET gate driver, and the TI device includes an integrated gate driver inside the device package [27]–[29].

C. Enhancement-Mode Devices

Although the 2DEG makes the lateral HFET natively depletion-mode, the gate can be modified to shift the threshold voltage positively and thereby make an e-mode device. Several companies have produced e-mode GaN devices, and Table III

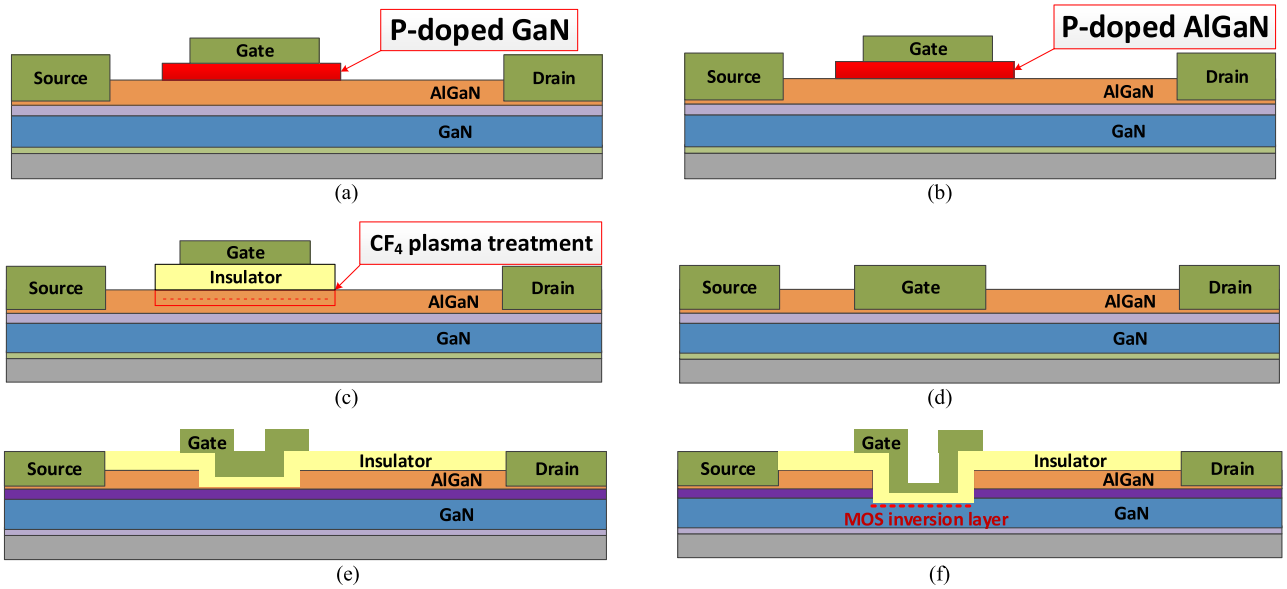

Fig. 8. Gate modification techniques for e-mode GaN HFETs. (a) p-doped GaN. (b) p-doped AlGaN. (c) Plasma treatment. (d) Recessed gate. (e) Insulated recessed gate. (f) Hybrid MIS-HFET [9], [11], [33], [36], [37], [44].

TABLE III
COMMERCIAL e-MODE DEVICES

Manufacturer	Voltage Rating (V)	Current Rating (A)	$R_{ds,on}$ (mΩ)	Q_g (nC)	Package	Availability
EPC [30]	30	60	1.3	20	Near-chipscale, LGA	Online ordering
	40		1.5	19		
	60		2.2	16		
	80		2.5	15		
	100		3.2	13		
	200	9	43	1.8		
GaN Systems [31]	650	7	220	1.5	Near-chipscale	Online ordering
		15	110	3.0		
		22	73	4.6		
		30	55	5.8		
		60	27	12		
	100	90	7.4	12		
		45	15	6.6		
Panasonic [32-35]	600	15	65	11	TO-220, DFN	Online ordering
		10	155	--	DFN	
HRL [36],[37]	1200	10	500	--	--	Samples
	600	10	350	--	--	
Navitas [38],[39]	650	--	160	2.5	PQFN	Samples
Exagan [40]	600	100	--	--	--	Unknown
	1200	100	--	--	--	
Powdec [41]	1200	16	--	--	--	Unknown
Sanken [42]	600	10	100	24	PQFN	Unknown
		20	50	30		

lists a selection of these as well as their commercial availability at this time.

Most of these companies have published papers that show their device structure, and explain how their devices achieve a positive threshold voltage. Fig. 8 shows some of these published techniques, which are used to deplete the 2DEG carriers beneath the gate when no voltage is applied. A positive voltage above the threshold is then required to enhance this depleted 2DEG beneath the gate and complete the channel.

EPC uses a p-doped layer of GaN beneath the gate, as shown in Fig. 8(a), which creates a diode-like characteristic on the gate that shifts the threshold up by the magnitude of the diode voltage drop [9]. Panasonic also uses a p-doped layer of GaN in their latest x-GaN gate injection transistors (GITs), although an earlier version of the GIT used p-doped AlGaN rather than GaN, as shown in Fig. 8(b) [33], [43]. One key difference between these two methods is the forward voltage drop on the gate before steady-state gate current begins to flow, which may be due to the etching depth beneath the p-doped GaN layer. The EPC diode knee occurs at ~5 V, whereas the Panasonic diode knee occurs at ~3 V. The EPC device is typically driven with 4.5–5 V, just below the knee when diode current

begins to increase. The Panasonic GIT is typically driven above the knee, where several milliamperes of steady-state current flow into the gate. This intentional injection of minority carriers enhances the conductivity of the 2DEG and reduces ON-resistance, but it also increases the complexity of gate drive design [30], [33], [34].

HRL first used plasma treatment to deposit fluorine ions beneath the gate, as shown in Fig. 8(c), effectively depleting the 2DEG until it is re-enhanced by a positive gate voltage [36]. However, HRL's later devices replaced the plasma treatment with a recessed gate, as shown in Fig. 8(e) [37]. This technique involves etching away the AlGaN beneath the gate to a precise depth, then replacing it with an insulating material. HRL chose AlN as the gate insulating layer. In 2015, HRL licensed its lateral GaN portfolio to Navitas Semiconductor [45].

Recessed gates are used by several other manufacturers as well, including Exagan and NEC, usually in conjunction with other modifications to further increase the threshold voltage [40], [46]. Sanken has developed devices using a non-insulated recessed gate, as shown in Fig. 8(d) [44], [47]. However, Sanken has not published whether this technique is used in the device it is currently sampling.

Fig. 8(f) shows another option for e-mode devices, a hybrid MIS-HFET. This structure requires etching past the AlGaN layer, and permanently removing the 2DEG beneath the gate. The 2DEG remains on the drain-side and source-side of the channel, but the two sides must be connected by a MISFET inversion layer beneath the gate in order to turn on the device [11].

Powdec has published an e-mode structure that is similar to a cascode, but the lower voltage device is fabricated on the top surface of the GaN device next to the HFET gate [41]. GaN Systems has not published its gate structure, but these devices appear to have an insulated gate, as shown in Fig. 8(c), (e), or (f) [31], [48], [49].

D. Reverse Conduction Behavior

A conventional power MOSFET's body diode provides a path for reverse conduction through the p-n doping of the body and drift regions. The GaN HFET does not have a body region or doping in the drift region, so there is no body diode. However, there are reverse conduction mechanisms in both cascode and e-mode GaN devices.

In a cascode device, the body diode of the low-voltage Si MOSFET will turn on when the cascode is reverse biased. The Si body diode will then turn on the channel of the GaN device. In this way, the cascode approximates the behavior of a body diode. The reverse recovery charge of the low-voltage MOSFET is much less than that of a power MOSFET, so the additional switching losses due to reverse recovery are relatively low.

An e-mode HFET has no body diode at all, but it demonstrates a mechanism sometimes called self-commutated reverse conduction (SCRC) or diode-like behavior. The key to this mechanism is the symmetry of the device. The channel will turn on when the gate–source voltage $V_{\rm gs}$ exceeds its threshold, $V_{\rm gs,th}$, and it will also turn on when the gate–drain voltage $V_{\rm gd}$ exceeds its own threshold voltage, $V_{\rm gd,th}$. If the output of the device is reverse biased, the gate–drain voltage will be

$$V_{\rm gd} = V_{\rm gs} - V_{\rm ds}. \tag{1}$$

When this voltage exceeds the threshold voltage $V_{\rm gd,th}$, which is typically approximately the same as the specified $V_{\rm gs,th}$, the e-mode device channel will turn on and allow reverse current to flow. The voltage drop in the SCRC mode will then be

$$V_{\rm sd} = V_{\rm gd,th} - V_{\rm gs} + I_d R_{\rm sd,rev} \tag{2}$$

where $R_{\rm sd,rev}$ is the effective channel resistance during SCRC. $R_{\rm sd,rev}$ is typically higher than $R_{{\rm ds},on}$ and varies with T_j, $V_{\rm gs}$, and I_d. When $V_{\rm gs} < V_{\rm gs,th}$, reverse current forces the device into saturation, but only just past the knee between ohmic and saturation regions. A more negative $V_{\rm gs}$ drives the device even further into saturation, and $R_{\rm sd,rev}$ becomes more dominated by the reverse transconductance rather than the ohmic ON-resistance. Therefore, negative OFF-state driving voltage is generally undesirable for e-mode GaN devices, because the SCRC voltage drop and resistance will increase. Fig. 9 shows a typical output characteristic for an e-mode device, including the SCRC behavior with 0 and −2 V on $V_{\rm gs}$ [49].

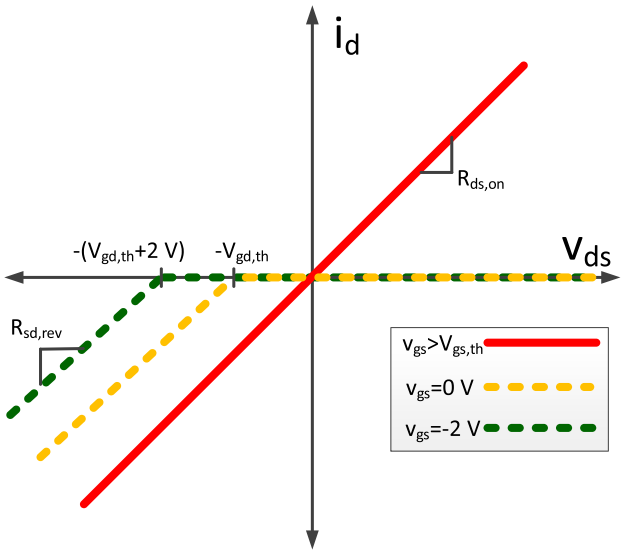

Fig. 9. Reverse conduction characteristic of an e-mode GaN HFET.

Compared with the voltage drop on a MOSFET body diode, the total SCRC forward voltage is often quite high (3–5 V). The e-mode GaN reverse conduction losses may become excessive during long dead times. However, this diode-like behavior does not actually contain a diode, so there are no reverse recovery losses during switching. The lack of reverse recovery also reduces the dead time required to ensure Zero Voltage Switching (ZVS), which is especially useful in soft switching applications [50].

Another option for either cascode or e-mode devices is to pair the HFET with an antiparallel Schottky diode, as is common with Insulated Gate Bipolar Transistors (IGBTs). This will increase the output capacitance of the device, and therefore increase switching loss, but it may be a practical

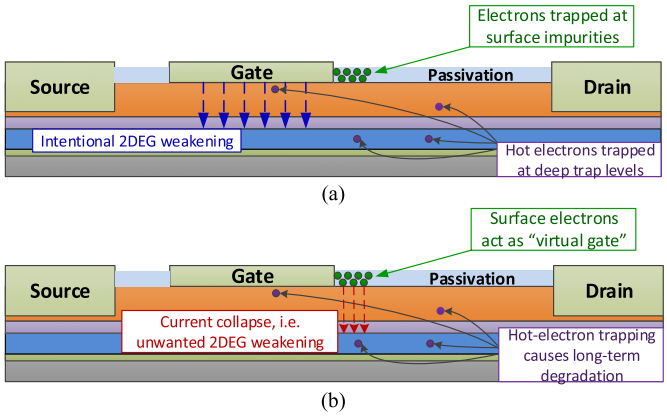

Fig. 10. Mechanisms causing dynamic $R_{\mathrm{ds},on}$ in lateral GaN HFETs. (a) Trapping of charges when blocking voltage in OFF-state. (b) Consequences of trapped charges during following ON-state.

solution for some applications. In such a case, it is beneficial to package the diode with the HFET to minimize parasitics and reduce overall size [51].

E. Dynamic $R_{ds,ON}$

Current collapse has been a widely reported phenomenon for lateral GaN devices, causing a temporary increase in ON-resistance that is proportional to blocking voltage. This dynamic $R_{\mathrm{ds},on}$ occurs primarily through two mechanisms, shown in Fig. 10. The first is the trapping of surface charges near the drain edge of the gate terminal when the device is in its OFF-state. The lateral structure causes the gate–drain electric field to be strongest near the edge, and impurities in the surface passivation and interface trap these charges temporarily. During the following ON-state, these trapped charges act as a virtual gate, weakening the 2DEG until they are released. The second mechanism is the injection of hot electrons into even deeper traps within the device, particularly in traps caused by carbon doping in the buffer layer. These trapped charges weaken the 2DEG and increase $R_{\mathrm{ds},on}$, and may also cause long-term degradation to the device. Both of these effects are proportional to blocking voltage, and the hot electron effect has also been shown to increase with higher switching energy loss [52]–[54].

Measurement and characterization of dynamic $R_{\mathrm{ds},on}$ is challenging, because it requires accurate measurement of V_{ds} in the 0.1 V scale immediately after falling from several hundreds of volts. This can be accomplished by clamping the measurement node at a low voltage during the OFF-state, using a diode-based or active clamping circuit, then unclamping the measurement node voltage after turn-on. However, this clamping action causes ringing in the measurement that may require several hundred nanoseconds to dampen. Because dynamic $R_{\mathrm{ds},on}$ is a very time-dependent phenomenon, it is important to capture this measurement as early as possible. A comprehensive study of dynamic $R_{\mathrm{ds},on}$ over several operating conditions was performed in [55] using this clamping technique. Temperature, load current, and bus voltage are all significant factors. In addition, switching frequency and duty cycle have a major effect on the overall increase in dynamic

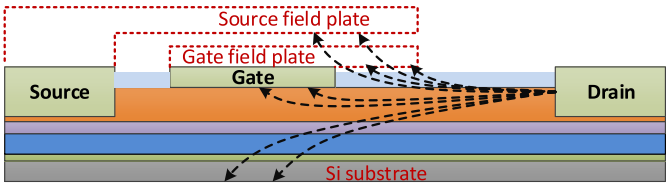

Fig. 11. Field plates reshaping the gate–drain electric field to mitigate current collapse.

$R_{\mathrm{ds},on}$ during a switching period. Therefore, additional conduction losses due to this phenomenon could be easily misdiagnosed as switching loss.

GaN device manufacturers have made much progress in mitigating current collapse, primarily through the use of field plates. Source and gate field plates help to redistribute the gate–drain electric field away from the gate edge. An example of basic field-plate structure is shown in Fig. 11. The Si substrate can also act as a bottom field plate if it is connected to the source. Some manufacturers internally connect the substrate and source of their GaN HFETs, while others choose to electrically isolate the Si substrate to prevent current from flowing through it. If a separate thermal pad is provided in the device package, the manufacturer may recommend that the substrate be externally source-connected to help mitigate current collapse [56], [57]. Panasonic's x-GaN GIT uniquely adds a second p-doped drain contact next to the ohmic drain to counteract dynamic $R_{\mathrm{ds},on}$ [44].

F. Breakdown Mechanisms

Voltage-source converter design often relies on a MOSFET's ability to survive a limited exposure to voltages over the device rating, according to the specified avalanche energy rating. However, lateral GaN HFETs do not have the potential for avalanche breakdown, because they do not rely on a p-n junction for voltage blocking. Vertical GaN MOSFETs have avalanche capabilities, but lateral HFETs experience catastrophic dielectric breakdown when exposed to sufficient overvoltage [58]. This breakdown is destructive and nonrecoverable. For this reason, GaN devices are typically rated much lower than the actual breakdown voltage. The dielectric may be designed at twice the rating to prevent lateral breakdown along surface states. While source-connecting the substrate is beneficial for current collapse mitigation, this also provides a vertical path for leakage current to flow, which is a second breakdown mechanism for some devices [59].

The gate in lateral HFETs is also susceptible to rupture. This failure mechanism may present as a gradual increase in steady-state current until the gate dielectric or Schottky junction completely breaks down [60]. Steady-state gate current is expected during normal operation for e-mode HFETs with p-doped gate caps. However, this has also been observed for insulated gate devices when exposed to excessive voltage and elevated temperatures, even when both of these conditions are within the ratings of the device [49]. For this reason, it is useful to periodically check the health of devices under test by measuring steady-state gate current, with a simple test setup using a dc power supply and current meter.

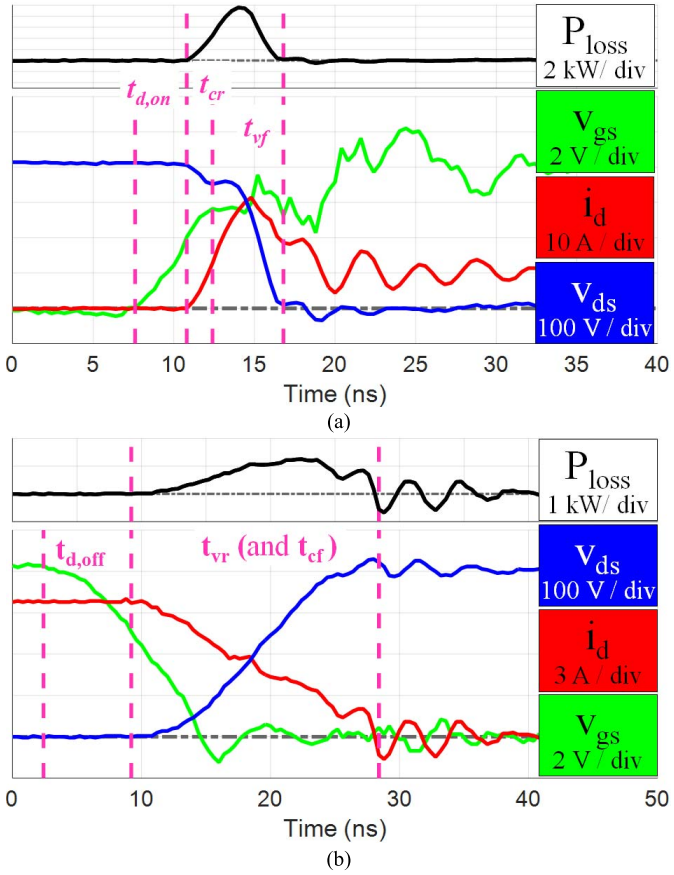

Fig. 12. Experimental waveforms of GaN Systems GS66508P, showing (a) turn-on and (b) turn-OFF with delay times, current rise time, voltage fall time, and voltage rise time [49].

IV. Converter Design Considerations

Because of the faster switching and unique characteristics of HFETs, common design practices for Si-based converters may not take full advantage of GaN. In fact, simply replacing a Si MOSFET with a GaN HFET will likely cause a converter to stop functioning, and may even destroy the GaN device itself. This section will cover the critical differences between Si and GaN devices, and important considerations for GaN-based converter design.

A. Switching Characteristics

GaN devices switch much faster than Si devices with similar voltage and current ratings. The input capacitance C_{iss} and gate charge Q_g are lower for GaN HFETs than Si MOSFETs. The output capacitance C_{oss} is also lower for GaN due to the smaller die size, as mentioned previously. Compared with a super junction MOSFET, the output capacitance of GaN devices at high drain-to-source voltage is often roughly the same, but is several orders of magnitude lower at low voltage. This means that the switching speed can exceed 200 V/ns, and the turn-on and turn-OFF delay times can be under 10 ns at 400 V. Examples of GaN switching waveforms are shown in Fig. 12, from experimental results using GaN Systems GS66508P [49]. However, switching waveforms will vary significantly in both shape and total loss with a different GaN device or board design.

In hard-switched converters, the two significant sources of switching energy losses are the energy related to stored charge in the output capacitors (C_{oss} loss) and the loss from conduction of the load current through a saturated device channel (overlap loss). In [61], it was shown that two selected e-mode devices experienced lower C_{oss}-related loss than a selected cascode with similar ratings, but higher overlap loss during turn-OFF. This paper concluded that the cascode was better for soft switching, and the two e-modes were more suitable for hard switching. However, such a comparison is very difficult to make in a universal sense, because of differences in die size and current ratings from device to device.

The switching behavior for a given device depends on the gate driver IC, converter topology, and board layout. Switching losses and speeds are difficult to approximate from device datasheets. The approximate capabilities of a given device can be determined experimentally with a double pulse test (DPT). Performing a DPT for WBG devices is a challenge in itself [62], but DPT results for many commercial GaN devices have been published, such as those in [32], [49], [61], and [63]–[65]. Although these characterizations are not very accurate when applied to a different converter, they may allow for approximation of the overall converter loss for the purposes of device selection and thermal design.

B. Device Packaging and PCB Layout

Fast switching transients magnify the impact of parasitic inductances in device packaging and printed circuit board (PCB) traces, because the voltage drop across any stray inductance is equal to

$$v_{\text{stray}} = L_{\text{stray}} \frac{di}{dt}. \tag{3}$$

Package parasitics, such as L_d, L_s, and L_g, worsen the ringing that occurs during and after the switching transient, which limits the switching speed and may cause damage to the device. The common-source inductance L_{cs} couples the high di/dt from the power loop into the lower voltage gate loop. The voltage drop across L_{cs} reduces the applied gate voltage during turn-on and increases it during turn-OFF, thereby slowing down both switching transients and worsening the switching loss. It is crucial that common-source inductance be minimized, in the package as well as board layout. Some devices provide a Kelvin source connection, which is a separate connection to the source metallization that is only used by the gate loop, decoupling it more effectively from power loop transient effects [65]–[68].

Overall parasitics can be reduced by combining the high-side and low-side devices in a single module, with decoupling capacitors and optimized internal connections [69]. Integrating the gate driver into the module provides additional benefits, as demonstrated in [70] and [71]. TI's LMG5200 is the first commercially available GaN intelligent power module, built with EPC devices and rated at 80 V. Sanken and TI both also make a driver-integrated module, with a single device and gate driver combined in a surface-mount package, but these are not yet available to order [29], [42].

Lateral GaN devices offer the unique opportunity to monolithically integrate high-side and low-side devices on the same die and nearly eliminate package parasitics. This has been accomplished at 12 V by EPC and Panasonic, although isolation of the two devices on a shared die may be difficult to accomplish at higher voltage [72], [73]. Furthermore, a GaN-based gate driver can be monolithically integrated on the same die as the HFET for ultrafast switching capabilities. Navitas has demonstrated success with monolithic integration of a single device and GaN-based gate driver, and GaN Systems has also published work toward this aim [38], [39], [74].

C. Gate Driver Requirements

Gate driver design for cascode devices is similar to driving conventional Si MOSFETs, because the input of a GaN cascode is a rugged Si MOSFET gate. However, e-mode GaN HFETs have more specific gate driver requirements. The threshold voltage of an e-mode HFET is typically 1–2 V, and the recommended driving voltage is typically around 5 V. This only allows a few volts of ringing before spurious switching events occur, during both turn-on and turn-OFF transients. Gate rupture is also a known issue with e-mode GaN devices. Even a small gate voltage overshoot may destroy the device.

Relatively, a few gate driver ICs on the market are designed for the requirements of GaN devices. The LM5113 from TI is a dual driver designed for GaN that can drive both high-side and low-side devices, and can isolate the high-side driver up to 100 V. However, this driver is not suitable for higher voltage applications. The LM5114 can drive any single GaN device, but it does not provide signal isolation [75].

Silicon Labs also makes a series of isolated gate driver ICs that are optimized for GaN devices, compatible with driving voltages from 3 to 30 V and bus voltages in the kilovolt range. These devices use digital isolators based on RF modulation as opposed to optical, capacitive, or transformer-based isolators, providing superior common-mode transient immunity (CMTI). Insufficient CMTI may allow spurious switching events when *dv/dt* exceeds the CMTI specification [76]. While several isolated drivers have specified typical CMTI of 50–100 kV/μs, this characteristic varies due to process variation and temperature. The actual CMTI may be as low as the specified minimum, rather than the typical value. Available isolation methods have been reviewed for several GaN-based converters [77], [78], and it is generally concluded that these RF-based digital isolators tolerate higher *dv/dt* than alternatives. The newer Si827x family has a specified minimum CMTI of 200 kV/μs, much higher than any other available isolated gate driver [79]. Of course, even with a sufficient CMTI-rated gate driver IC, the PCB layout must be designed very carefully to prevent common-mode interference through stray impedances. To further improve CMTI, other techniques may be implemented in the gate drive circuit, such as a common-mode choke or differential connection of the digital signal inputs [80], [81].

D. Cross-talk

Another source of spurious switching events is interference between high-side and low-side devices due to the Miller effect. This may cause cross-talk, also known as cross-conduction or Miller turn-on, a phenomenon in which one device is inadvertently turned on due to the *dv/dt* on its Miller capacitance when the complementary device in the same phase leg is intentionally turned on. This cross-talk allows a shoot-through current to flow from the dc bus across the saturated channels of both devices, incurring additional switching losses. In a phase leg configuration, cross-talk losses may be especially noticeable during light load operation, when the overlap losses are nearly zero and the turn-on switching speed is highest [82].

Cross-talk can be prevented by slowing down the turn-on transient, e.g., with a higher turn-on gate resistance, but this will also increase the overlap losses. The tradeoff between overlap and cross-talk loss will be different for every converter, based on the device, driver, switching speed, and operating conditions. One common method to prevent cross-talk for SiC devices is to use a negative voltage supply for the OFF-state. However, this is nonideal for e-mode GaN devices, because it increases the reverse conduction losses during dead time. Another method to mitigate cross-talk is adding an external capacitor in parallel with the internal device C_{gs}, slowing the switching transients to limit dv_{ds}/dt while also providing a low-impedance path for the C_{gd} displacement current. However, this is also not desirable due to increased overlap and driving losses.

The simplest cross-talk mitigation method for GaN may be to use a low-resistance turn-OFF path and a higher resistance for the turn-on path; however, this will also increase overlap losses somewhat. Some drivers provide separate paths for gate current during turn-on and turn-OFF. If the driver does not provide separate paths, a Schottky diode can be added in parallel with the gate resistor [48], [82]. The most effective solution for this problem may be an active gate driver with cross-talk suppression as demonstrated for SiC, but this has not yet been developed commercially [83].

E. Steady-State Gate Current

The Panasonic GIT is somewhat unique in its steady-state gate current requirement. Although the device is voltage-driven, full enhancement of the channel requires a small steady-state gate current in the milliampere range. The diode characteristic of the gate limits the input voltage below 5 V, but a higher driving voltage is desirable during the turn-on transient to enable faster switching. This can be accomplished with an *RC*-type gate driving circuit, or a multistage driver as demonstrated in [84]. Panasonic has recently released a commercial driver IC for their device that includes this feature [85].

F. Operating Temperature and Thermal Design

GaN devices exhibit a positive temperature coefficient for $R_{\mathrm{ds},on}$, similar to that of Si. Fig. 13 shows the trend of $R_{\mathrm{ds},on}$ over temperature for several commercial GaN HFETs. These trends are derived variously from data sheets and published papers. The threshold voltage of most GaN devices is relatively stable over temperature. According to [86], the e-mode

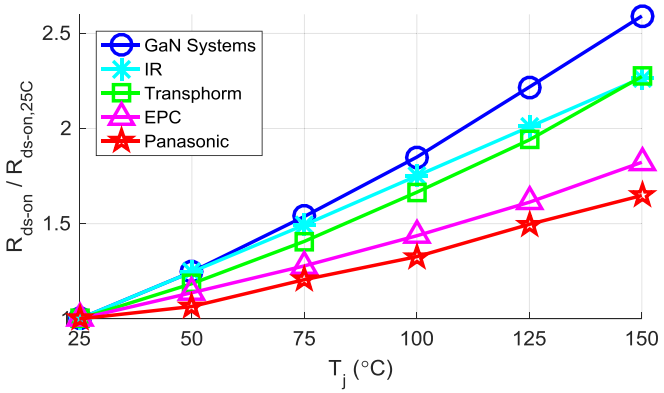

Fig. 13. Normalized ON-resistance of commercial GaN HFETs [20], [23], [30]–[32].

devices exhibit increasing switching loss with higher temperature due to the decreasing transconductance. This was also shown experimentally in [32] and [63] for other GaN devices. According to the published literature, Panasonic has the best reported performance at higher temperature of these devices.

Thermal design for some GaN devices can be challenging, depending on the package type. Surface-mount devices with bottom-side cooling require a connection to a heatsink through the board, using thermal vias [87]. Top-cooled devices are also available from some vendors, and others use TO-220 packages that make thermal design easier. As compared with SiC, thermal design is especially critical for GaN-based converter design, because of the potential thermal runaway from both conduction loss and switching loss.

G. Reliability and Qualification

Power transistors, such as MOSFETs and IGBTs, are typically tested according to published JEDEC standards, and thereby qualified for particular reliability specifications. Testing for Si MOSFETS generally includes high-temperature reverse bias, high temperature gate bias, high temperature storage, temperature cycling, high temperature high humidity reverse bias, unbiased autoclave, moisture sensitivity level, and electrostatic discharge testing. Reliability data based on these tests have been published for EPC and Transphorm devices [88]–[90].

However, because these JEDEC standards were written for Si MOSFETs, different reliability qualification standards may be required for GaN HFETs. One of the main challenges for new devices is the accelerated lifetime testing. Conventional Si devices are tested for accelerated lifetime based on well-established models and years of experience. GaN devices may not respond the same way in the same test conditions, and there have not been as many years with practical field reliability experience to back up the accelerated lifetime models [91]. A path to developing new standards specifically designed for GaN devices has been proposed in [92]–[94]. The unique breakdown mechanisms discussed in Section III-F must be addressed, and the qualification process will likely be different for lateral and vertical GaN power devices.

H. Device Availability

As with any new technology, the relatively low availability of GaN power devices poses a barrier to widespread adoption [6]. Therefore, several of the leading GaN manufacturers have established industry partnerships and taken steps to increase availability of their devices. Transphorm has established agreements with both Fujitsu and ON Semiconductor, to mass produce and cobrand their cascode devices [95], [96]. Panasonic has a licensing agreement with Infineon to establish dual sourcing of the GIT [97]. GaN Systems has recently ramped up its production ten times at their foundry, TMSC [98]. With these recent steps toward mass production, the availability of GaN power devices may not be a barrier to industrial adoption for long.

V. Conclusion

The basic structures and characteristics of GaN power devices have been reviewed, including both vertical and lateral devices. The commercial status and specifications of normally-OFF GaN power devices were summarized. Currently, three manufacturers produce e-mode GaN HFETs for open online ordering, as well as one cascode. Several lateral device manufacturers are providing samples of their e-mode and cascode devices, and vertical device samples may also be available soon. As the availability and performance of commercial GaN devices continues to improve, GaN-based converter design skills will need to keep pace with these device developments. Here, GaN-based converter design considerations were reviewed, including switching characterization, packaging, board layout, gate driver design, reverse conduction mechanisms, dynamic $R_{\mathrm{ds},on}$, and thermal design. The breakdown mechanisms and reliability concerns were also discussed, as well as the qualification process to characterize the reliability of commercial GaN devices. This review provided an introduction to GaN-based power devices, in order to help readers effectively use GaN to design high-frequency and high-efficiency converters.

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