DAQ OF ELECTRICAL SIGNALS

PC BASED DAQ

MEASUREMENT AND DATA ACQUISITION

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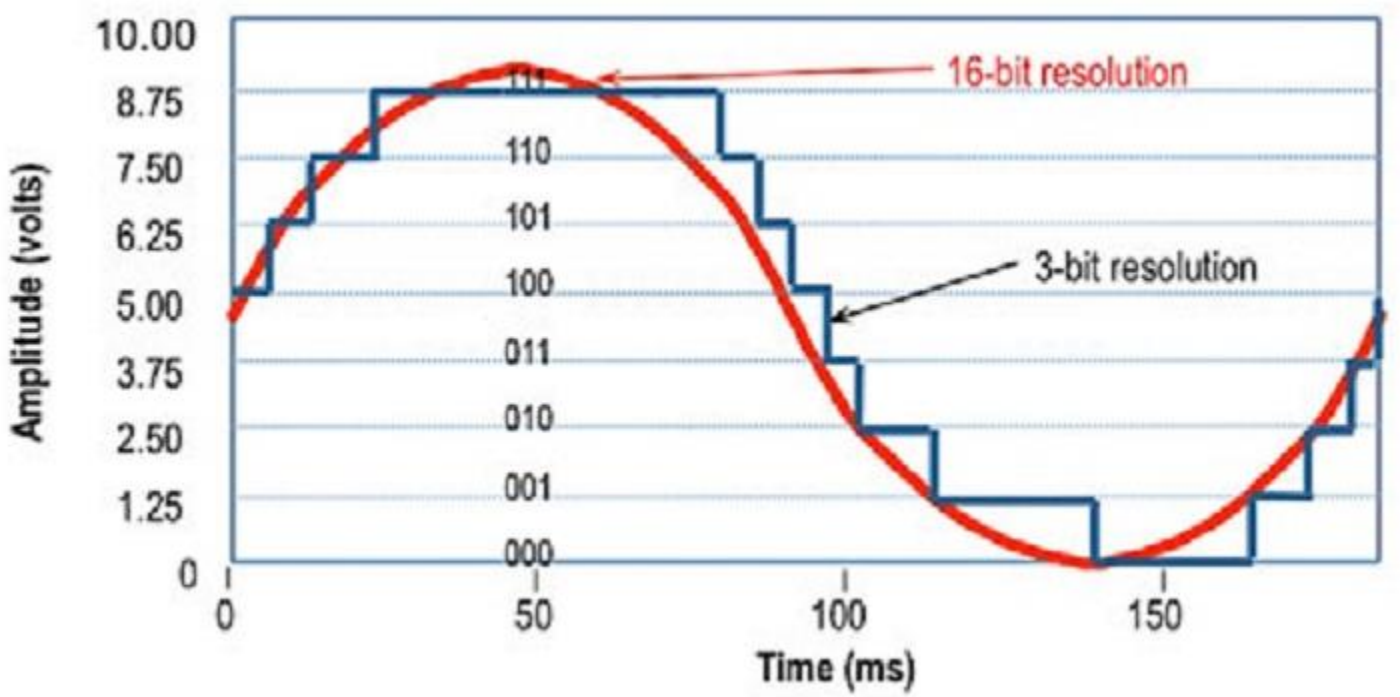
ADC

- Figure below compares a 3-bit ADC and a 16-bit ADC
- A 3-bit ADC can represent eight (23) discrete voltage levels.
- A 16-bit ADC can represent 65,536 (216) discrete voltage levels.



SAMPLING THEORY - Sample Rate

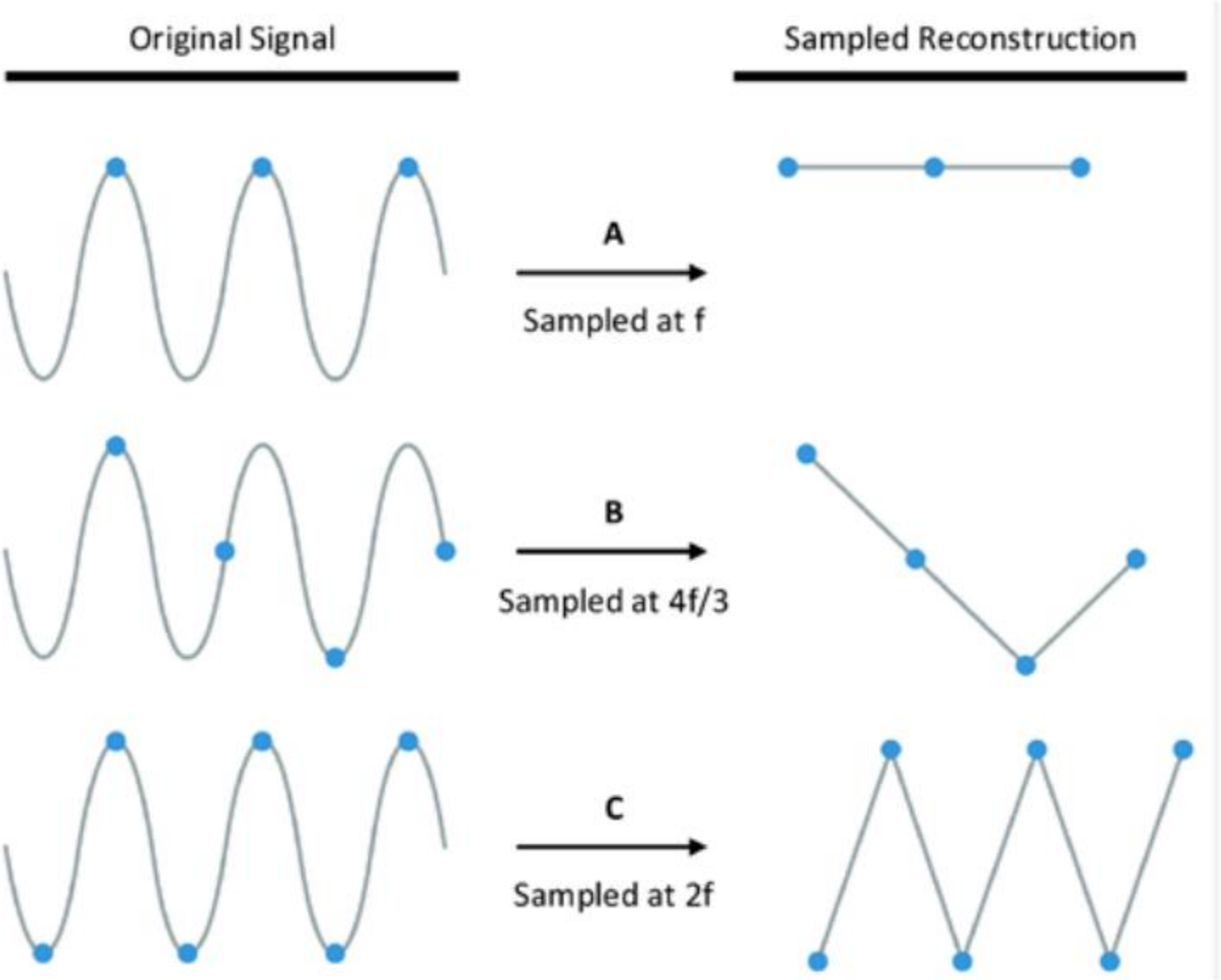
- The sample rate is the rate at which the ADC converts the analog input waveform to digital data.
- It is frequently a key specifiation in the selection of a digitizer because it inversely correlates measurement timing precision to sample resolution. That is, sample rate generally increases at the expense of the number of bits of resolution.
- This is a logical trade-off because slower sampling provides more time for a high-resolution ADC to perform its digitization as well as any signal conditioning that may occur prior to that point.

SAMPLING THEORY - Nyquist Sampling Theorem and Aliasing

- The Nyquist Sampling Theorem determines the minimum sampling speeds you need in an application to ensure a faithful reproduction of the original signal.
- It states that as long as the sample rate, fs , in any system exceeds twice the maximum signal frequency, the original signal can be reconstructed in the receiver with minimal distortion. This frequency is often referred to as the Nyquist frequency, f_N .

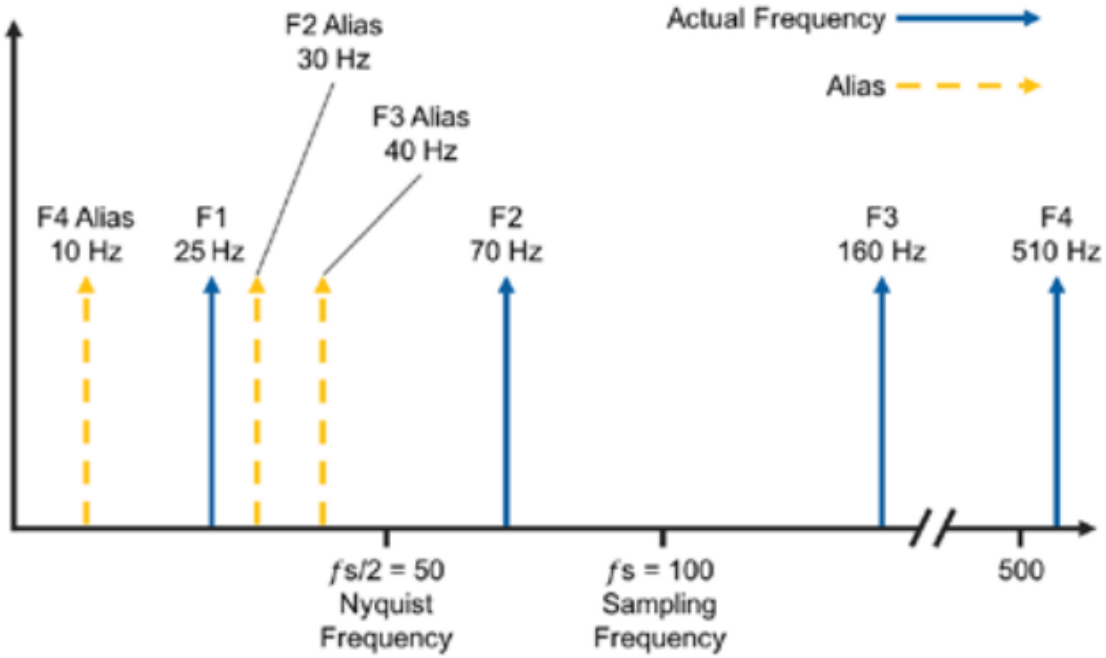
- $f_s > 2 * f_N$

SAMPLING THEORY - Nyquist Sampling Theorem and Aliasing



SAMPLING THEORY- ALIASING

- If frequency components in the system are higher than the Nyquist frequency, false lower frequency components may appear in the sampled data. This phenomenon is referred to as aliasing.
- Consider a signal with a sample frequency of 100 Hz, and the input signal contains the following frequencies: 25 Hz, 70 Hz, 160 Hz, and 510 Hz. Frequencies below the Nyquist frequency of 50 Hz are sampled correctly; those over 50 Hz appear as alias.



OVERSAMPLING

- Oversampling, or sampling at a rate beyond twice the Nyquist frequency, is recommended to help prevent aliasing and preserve the shape of the original signal.
- Because real-world signals are not perfectly fitered, they often contain frequency components greater than twice the critical frequency of interest.
- You can use oversampling to increase the Nyquist frequency (one half the sample rate) and reduce the possibility of aliasing in these higher frequency components.
- Oversampling is also necessary when you want to capture fast edges, transients, and one-time events.

DAQ CARD EXAMPLE

Low-Cost E Series Multifunction DAQ
12-Bit, 200 kS/s, 16 Analog Inputs

NI 6023E, NI 6024E, NI 6025E

- 16 analog inputs at 200 kS/s, 12-bit resolution
- Up to 2 analog outputs, 12-bit resolution
- 8 digital I/O lines (5 V/TTL/CMOS); two 24-bit counter/timers
- Digital triggering
- 4 analog input signal ranges
- NI-DAQ driver simplifies configuration and measurements

Models

- NI PCI-6023E
- NI PCI-6024E
- NI DAQCard-6024E for PCMCIA
- NI PCI-6025E
- NI PXI-6025E

*See ordering information

Operating Systems

- Windows 2000/NT/XP/Me/9x
- Mac OS 9*
- Real-time performance with LabVIEW (page 134)
- Others such as Linux (page 187)

Recommended Software

- LabVIEW
- LabWindows/CVI
- Measurement Studio for Visual Basic
- VI Logger

Other Compatible Software

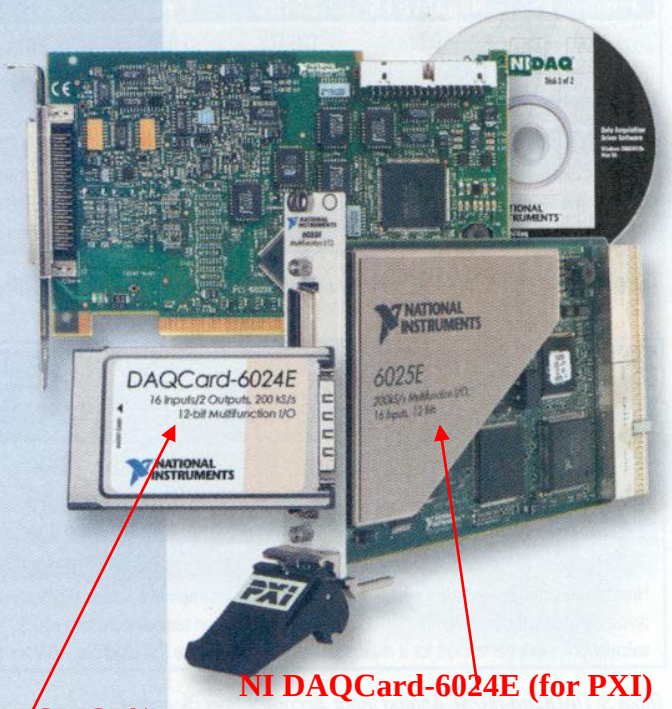
- Visual Basic
- C/C++

Driver Software (included)

- NI-DAQ

Calibration Certificate Included

See page 21



NI DAQCard-6024E (for PCMCIA)

NI DAQCard-6024E (for PXI)

Low-Cost E Series 12-Bit Multifunction DAQ

DAQ CARD EXAMPLE

NI PCI-6120

16-Bit, 1 MS/s/ch, Simultaneous Sampling Multifunction DAQ

S Series Multifunction DAQ 12 or 16-Bit, 1 to 10 MS/s, 4 Analog Inputs

NI 6120, NI 6115, NI 6110, NI 6111

- 2 or 4 analog inputs; dedicated A/D converter per channel
- 1 to 10 MS/s per channel maximum sample rate
- Analog and digital triggering
- AC or DC coupling
- 8 input ranges from ±200 mV to ±42 V
- 2 analog outputs at 4 MS/s single channel or 2.5 MS/s dual channel
- 8 digital I/O lines (5 V TTL/CMOS)
- Two 24-bit counter/timers
- Measurement services that simplify configuration and measurements

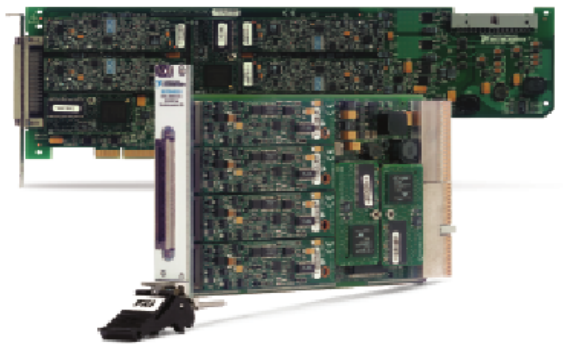
Operating Systems
- Windows 2000/NT/XP
- Mac OS X
- Linux

Recommended Software
- LabVIEW 7.x or higher
- LabWindows/CVI 7.x or higher
- Measurement Studio 7.x or higher
- Digital Waveform Editor
- SignalExpress 1.x or higher

Other Compatible Software
- VI Logger 2.x or higher
- Visual Studio .NET
- Visual Basic, C/C++, and C#

Measurement Services Software (included)[1]
- NI-DAQmx driver software
- Measurement & Automation Explorer configuration utility
- VI Logger Lite data-logging software

[1]Mac OS X and Linux applications must use NI-DAQmx Base driver software.



Calibration Certificate Available

Family	Bus	Analog Inputs	Input Resolution (bits)	Sampling Rate (MS/s)	Input Range (V)	Analog Outputs	Max Output Rate (MS/s)	Output Range (V)	Digital I/O	Counter/ Timers	Triggers
NI 6120	PCI, PXI	4	16	1[3]	±0.2 to ±42	2	4[1]	±10	8[2]	2, 24-bit	Analog, digital
NI 6115	PCI, PXI	4	12	10	±0.2 to ±42	2	4[1]	±10	8[2]	2, 24-bit	Analog, digital
NI 6110	PCI	4	12	5	±0.2 to ±42	2	4[1]	±10	8	2, 24-bit	Analog, digital
NI 6111	PCI	2	12	5	±0.2 to ±42	2	4[1]	±10	8	2, 24-bit	Analog, digital

[1]4 MS/s single channel; 2.5 MS/s on two channels [2]Hardware-timed up to 10 MB/s [3]800 kS/s with NI-DAQmx, 1 MS/s with additional download. Special conditions apply.

PXI Multifunction Reconfigurable I/O Module

PXI Multifunction Reconfigurable I/O Module

Model	Price	Bus Connector	FPGA	Maximum Sample Rate	Number of Analog Input Channels	Number of Analog Output Channels	Number of Bidirectional Digital Channels	Analog Input Voltage Range	Digital I/O Logic Levels	Maximum Clock Rate	Dynamic RAM (DRAM)
		Select	Select	Select	Select	Select	Select	Select	Select	Select	Select
PXI-7853	Ft 2.576.800,00	PXI Hybrid	Virtex-5 LX85	750 kS/s	8	8	96	-10 V to 10 V	3.3V, 5V	40 MHz	0 MB
PXI-7854	Ft 3.335.400,00	PXI Hybrid	Virtex-5 LX110	750 kS/s	8	8	96	-10 V to 10 V	3.3V, 5V	40 MHz	0 MB
PXIe-7846	Ft 1.118.400,00	PXIe	Kintex-7 160T	500 kS/s	8	8	48	-1 V to 1 V, -2 V to 2 V, -5 V to 5 V, -10 V to 10 V	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	80 MHz	0 MB
PXIe-7847	Ft 1.376.700,00	PXIe	Kintex-7 160T	500 kS/s	8	8	48	-1 V to 1 V, -2 V to 2 V, -5 V to 5 V, -10 V to 10 V	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	80 MHz	512 MB
PXIe-7856	Ft 1.487.900,00	PXIe	Kintex-7 160T	1 MS/s	8	8	48	-1 V to 1 V, -2 V to 2 V, -5 V to 5 V, -10 V to 10 V	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	80 MHz	0 MB
PXIe-7857	Ft 1.749.500,00	PXIe	Kintex-7 160T	1 MS/s	8	8	48	-1 V to 1 V, -2 V to 2 V, -5 V to 5 V, -10 V to 10 V	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	80 MHz	512 MB
PXIe-7858	Ft 2.606.200,00	PXIe	Kintex-7 325T	1 MS/s	8	8	48	-1 V to 1 V, -2 V to 2 V, -5 V to 5 V, -10 V to 10 V	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	80 MHz	512 MB

DAQ CARD EXAMPLE

NI PXIe-5665
High-Performance Vector Signal Analyzer up to 14 GHz

20 Hz to 3.6 GHz / 14 GHz frequency range
25/50 MHz instantaneous bandwidth
129 dBc/Hz typical phase noise at 10 kHz offset at 800 MHz
±0.35 dB typical flatness within 20 MHz bandwidth
±0.1 dB typical amplitude accuracy

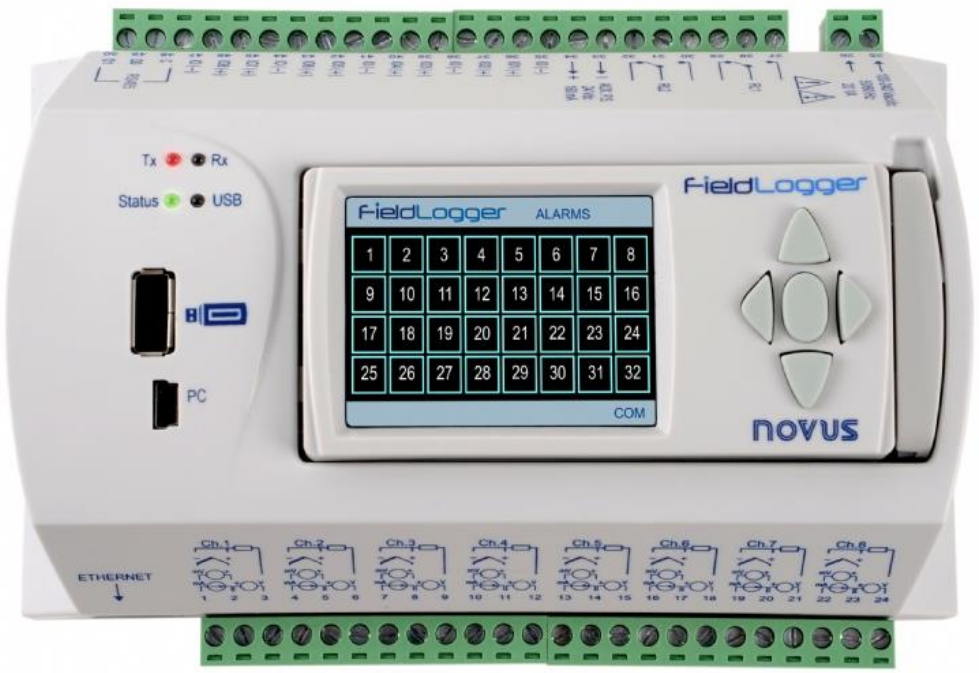
DATA STORAGE

750 MB/s sustained read and write speeds for 80 percent of the storage capacity
Three storage capacities available: 6TB (12 x 500GB), 12TB (12 x 1TB) and 24TB (12 x 2TB)
Supports various RAID modes (RAID-0/1/10/5/6)
Programmatic control and monitoring of hard drives and RAID partitions
Supports hot swap of hard drives
Offers Endless record mode

DATA STORAGE

Model	Price	Bus Connector	Sustained Throughput	Storage Capacity	Drive Type	Module Width	Number of Drives
		Select	Select	Select	Select	Select	Select
HDD-8261	Ft 1.174.000,00	PXIe	250 MB/s	4 TB	HDD	3	4
HDD-8261	Ft 2.177.900,00	PXIe	2 GB/s	2.9 TB	SSD	3	6

FIELDLOGGER



- 8 universal analog channels per module
- Accepts t/c J, K, T, E, N, R, S, B; 4-20 mA, Pt100, 0-50 mV without hardware change
- Internal memory (optional) for 32,000 to 128,000 recordings and real time clock
- Input resolution: 12,000 levels
- Accuracy: 0.1 % of full scale (FS)
- Scanning: 8 channels in 0.5 seconds
- Reading rate: from 0.2s to 1 day
- Power: 100-240 Vac, optional 24 Vdc/ac
- Alarms: 2 relays 3 A for the 8 channels
- Digital input for remote START/STOP
- RS-485, MODBUS - RTU, 19200 bps
- 35 mm DIN rail mounting

STANDALONE KEYSIGHT DAQ SYSTEM

MAINFRAME

PLUG-IN-MODULES

34970A Plug-in Modules	Description	Scan ch/sec	Max Voltage	Max Current	Comments
34901A	20 ch. multiplexer (2/4-wire)	60	300 V	1 A	2 current channels (22 ch. total); built-in cold junction reference; connects to internal DMM
34902A	16 ch. multiplexer (2/4 wire)	250	300 V	50 mA	Built-in cold junction reference; reed relays multi-plex inputs to internal DMM
34903A	20-ch. actuator/GP switch	120	300 V	1 A	Form C (SPDT) switches; no connection to internal DMM
34904A	4x8 matrix	120	300 V	1 A	2-wire, full crosspoint; no connection to internal DMM
34905A	2 GHz dual 1:4 RF mux 50Ω	60	42 V	0.7 A	1 GHz through provided BNC-to-SMB adapter cables; no connection to internal DMM
34906A	2 GHz dual 1:4 RF mux 75Ω	60	42 V	0.7 A	1 GHz through provided BNC-to-SMB adapter cables; no connection to internal DMM
34907A	2, 8-bit digital I/O ports 26-bit, 100 kHz event counter 2,16-bit analogue outputs	NA	42 V 42 ±12 V	400 mA 10 mA	Open drain Gated, selectable input threshold; Earth referenced; calibrated; no connection to internal DMM
34908A	40-ch. single-ended mux	60	300 V	1 A	Common low, no 4-wire meas. Built-in cold junction reference; connects to internal DMM

CONNECTOR BLOCKS

BNC CONNECTOR BLOCK

SCREW TERMINAL BLOCK

SMB TERMINAL BLOCK

RACK MOUNTED BNC CONNECTOR

DAQ DEVICE

DAQ hardware acts as the interface between a computer and signals from the outside world. It primarily functions as a device that translates incoming analog signals so that a computer can interpret them. The three key components of a DAQ device used for measuring a signal are:

1. The signal conditioning circuitry
2. The analog-to-digital converter (ADC)
3. The computer bus

Hardware Architectures for Digitization

- Though you can choose from many architectures to digitize analog signals to digital codes, a few are by far the most common: SAR, delta sigma (ΔΣ), and pipeline
- Each has specific advantages and disadvantages, but all perform fundamentally the same task: characterizing an analog voltage with a digital representation.

Successive-Approximation Register (SAR)

Cost	Sample Rate	Resolution	Noise	Latency
Moderate	Moderate (<10 MS/s)	Moderate	Moderate	Low

- SAR ADCs feature one of the more common architectures used for data acquisition
- Most notably, SAR-based DAQ devices can take measurements with minimal latency, meaning they can precisely place measurements in time
- You digitize analog signals with SAR-based devices by using a method like a binary search: you capture and compare the input voltage with successively smaller references until a precise measurement results.
- Additionally, the SAR architecture lends itself well to the inclusion of multiple inputs in the same ADC circuitry at the expense of sample rate per channel.

Delta Sigma (ΔΣ)

Cost	Sample Rate	Resolution	Noise	Latency
Moderate	Lower (<1 MS/s)	High	Low	High

- Delta-sigma-based DAQ devices have the primary advantages of noise and alias rejection with exceptional resolution, but they provide a lower effective sample rate, lower bandwidth, and increased latency

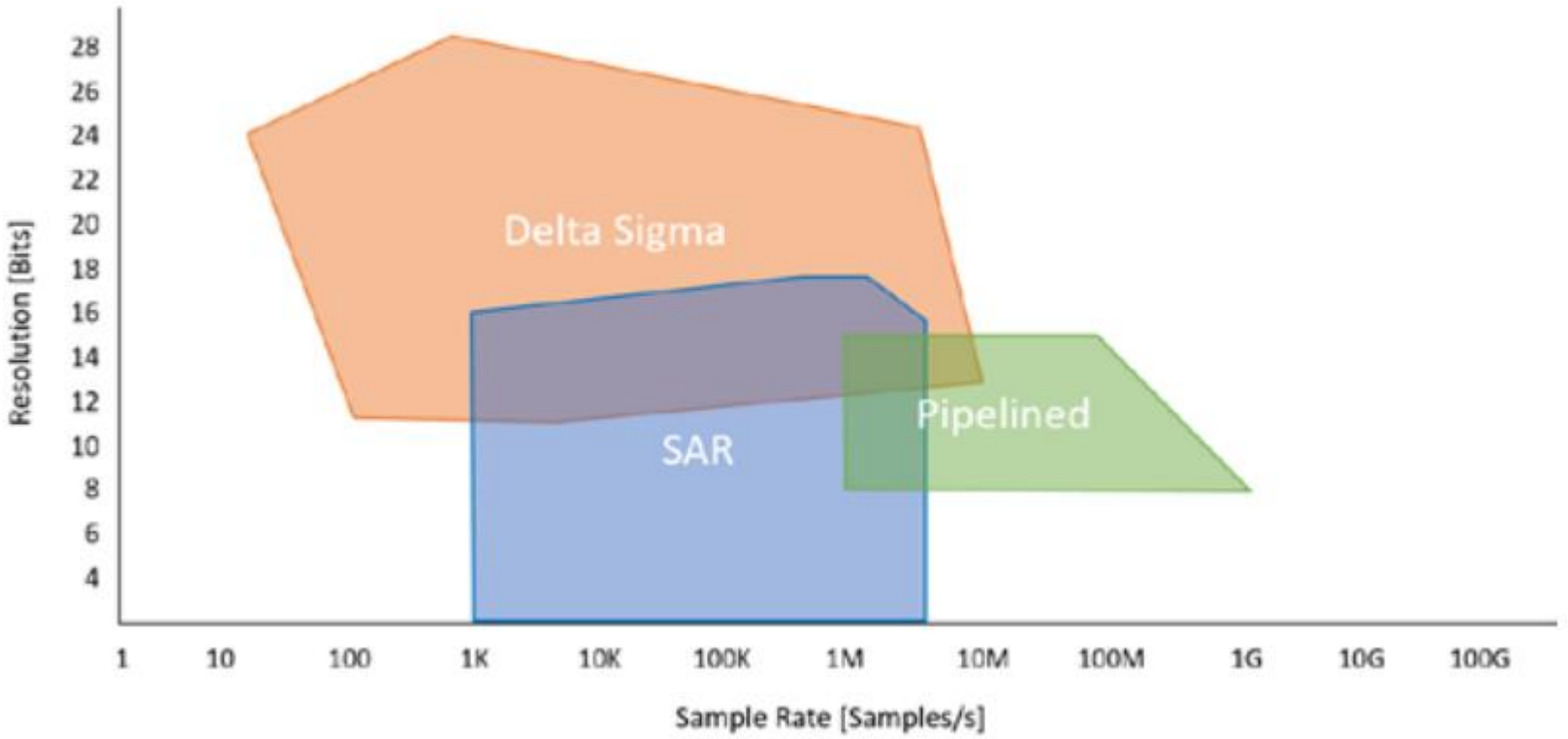
Pipeline

Cost	Sample Rate	Resolution	Noise	Latency
High	High (1 GS/s)	Moderate	Moderate	Moderate

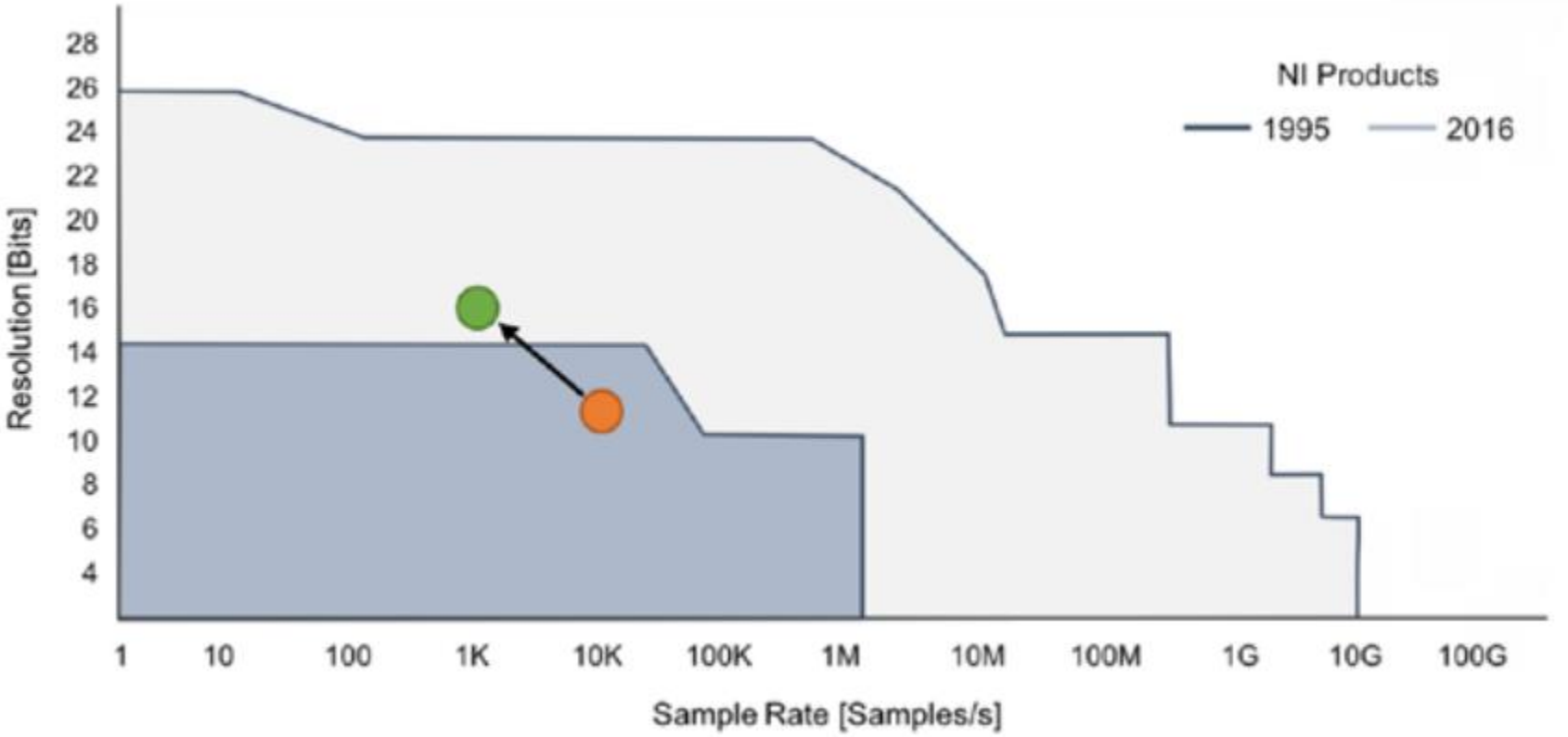
- Pipeline-based ADCs use a collection of low-resolution ADCs in sequential stages to achieve exceptionally fast acquisition rates at a moderate resolution. Generally, faster sample rates correspond with lower resolution and vice versa.

Architecture Comparison

	Cost	Sample Rate	Resolution	Noise	Latency
SAR	Low to Moderate	Moderate (<10 MS/s)	Moderate	Moderate	Low
ΔΣ	Moderate	Lower (<1 MS/s)	High	Low	High
Pipelined	High	High (1 GS/s)	Moderate	Moderate	Moderate

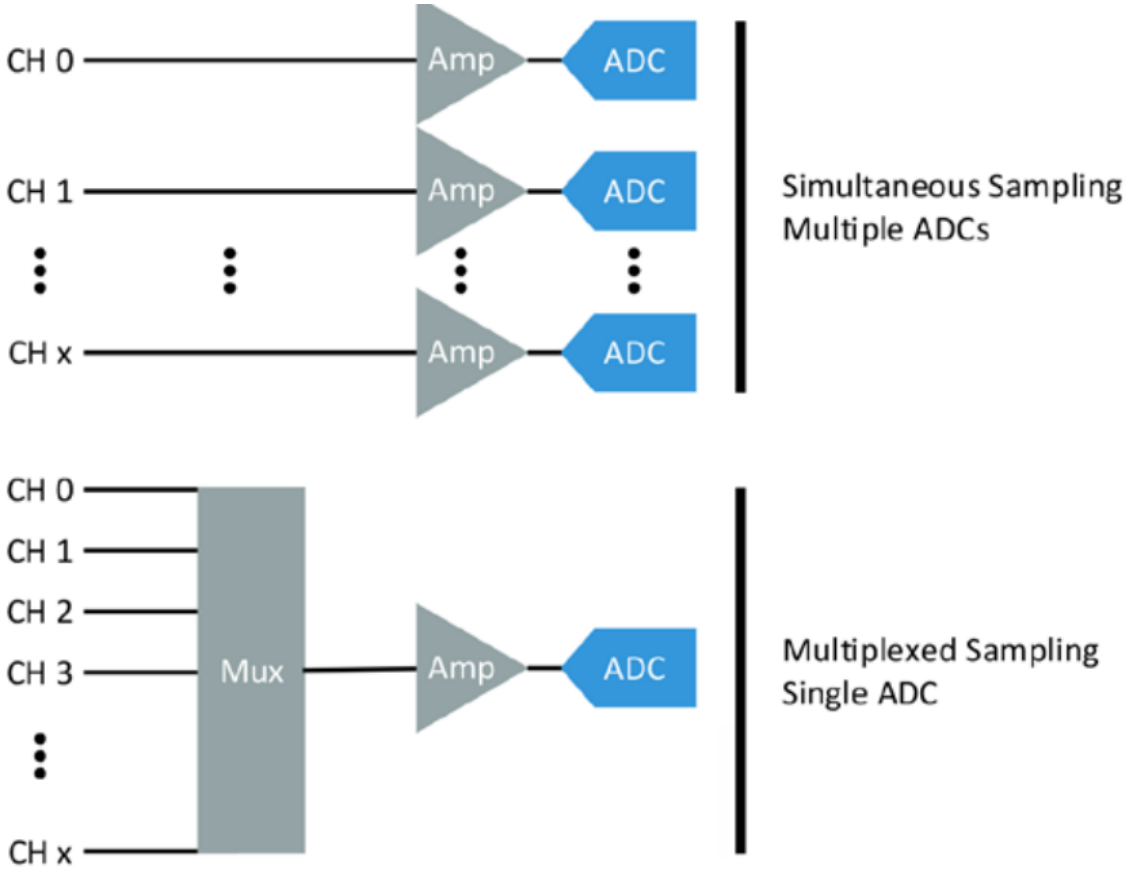


Architecture Comparison



Digitization Timing

- The two most common architectures are simultaneous and multiplexed DAQ devices



Digitization Timing

Simultaneous architectures use one ADC per input channel. This has several implications:

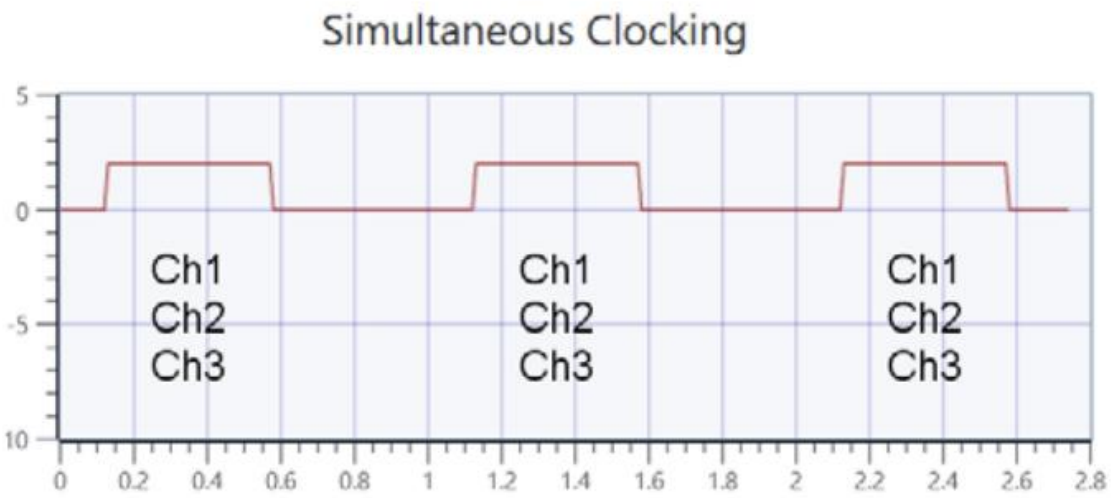
1. You can achieve the full sample rate on all channels regardless of how many channels you are using
2. You can acquire samples in parallel at precisely the same moment in time
3. Space limitations curb the number of channels that can fi on a DAQ device
4. Device cost tends to be greater due to the extra ADC and analog front-end components

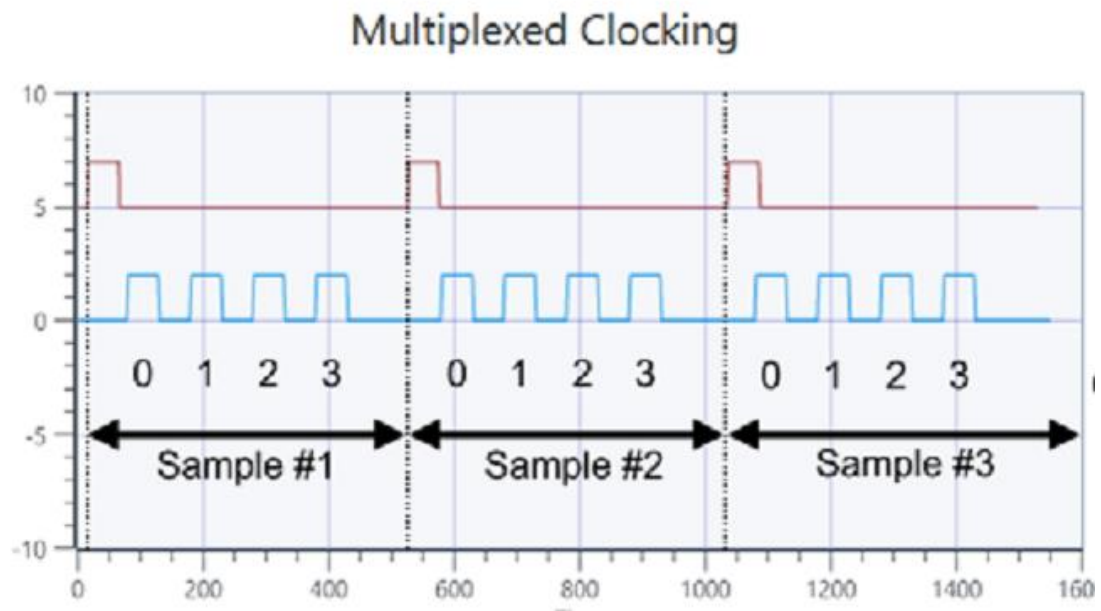
Digitization Timing

Multiplexed architectures use one ADC and analog front end for all channels and a multiplexer —or switch—to scan the input channels. This also has several implications:

1. The full sample rate is shared among all channels, meaning the maximum rate per channel decreases as more channels are added to the acquisition
2. Samples are acquired in series with a precise delay between channel
3. You can achieve greater channel densities on a single DAQ device
4. Cost per channel tends to be less

Digitization Timing





Bus Choice and Buffering

- All PC buses have a limit to the amount of data that can be transferred in a certain period of time. Known as the bus bandwidth, this limit is often specifid in megabytes per second (MB/s). If dynamic waveform measurements are important in your application, be sure to consider a bus with enough bandwidth
- The PCI bus, for example, has a theoretical bandwidth of 132 MB/s that is shared among all PCI boards in the computer.
- Gigabit Ethernet offers 125 MB/s shared across devices on a subnet or network.

Bus Choice and Buffering

● = Best | ◐ = Better | ○ = Good

Bus	Waveform Streaming	Latency	Portability	Distributed Measurements
PCI	132 MB/s (shared)	●	○	○
PCI Express	250 MB/s (per lane)	●	○	○
PXI	132 MB/s (shared)	●	◐	◐
PXI Express	250 MB/s (per lane)	●	◐	◐
USB	60 MB/s	◐	●	◐
Ethernet	125 MB/s (shared)	○	●	●
Wireless	6.75 MB/s (per 802.11g channel)	○	●	●

The four main data transfer mechanisms

- Direct Memory Access (DMA)—DMA transfers data between the device and computer memory without the involvement of the CPU. Because of this, DMA is the fastest data transfer mechanism. The usage of DMA hardware and software technology is to achieve high throughput rates and increase system utilization. It is the default data transfer method for DAQ devices that support it. However, each device typically has a limited number of DMA channels.
- Interrupt Request (IRQ)—IRQ transfers rely on the CPU to service data transfer requests. The device notifies the CPU when it is ready to transfer data. The data transfer speed depends on the rate at which the CPU can service the interrupt requests. If you are using interrupts to acquire data at a rate faster than the CPU can service the interrupts, system performance may be reduced.
- Programmed I/O—Programmed I/O does not use a buffer; instead, the computer reads and writes directly to the device. Software-timed (on-demand) operations typically use programmed I/O.

4. USB Bulk—USB Bulk is a buffered, message-based streaming mechanism for data transfer.
This high-speed method is the default transfer mechanism for USB devices