SIGNAL ACQUSITION OF ELECTRICAL SIGNALS II.

(FREQUENCY MEASUREMENT) COMPUTER BASED DAQ SYSTEMS

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RS-232, RS-422, RS-485 Serial Communication General Concepts

Serial Communication

- The concept of serial communication is simple. The serial port sends and receives bytes of information one bit at a time.
- Typically, serial is used to transmit ASCII data. Communication is completed using 3 transmission lines: (1) Ground, (2) Transmit, and (3) Receive.
- Since serial is asynchronous, the port is able to transmit data on one line while receiving data on another. This is referred to as Full-Duplex transmission
- The important serial characteristics are baud rate, data bits, stop bits, and parity.

Serial Communication

Baud rate is a speed measurement for communication. It indicates the number of bit transfers per second

Data bits are a measurement of the actual data bits in a transmission

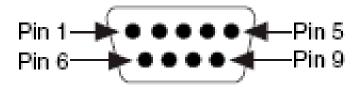
Stop bits are used to signal the end of communication for a single packet. Typical values are 1, 1.5, and 2 bits

Parity is a simple form of error checking that is used in serial communication. There are four types of parity: even, odd, marked, and spaced.

RS232

- RS-232 (ANSI/EIA-232 Standard) is the serial connection historically found on IBM-compatible PCs.
- RS-232 is limited to point-to-point connections between PC serial ports and devices.
- RS-232 hardware can be used for serial communication up to distances of 50 feet.

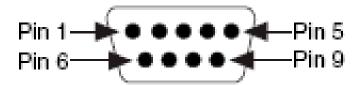
DB-9 Male



RS422

- RS-422 (EIA RS-422-A Standard) is the serial connection historically used on Apple Macintosh computers
- Differential transmission uses two lines each for transmit and receive signals which results in greater noise immunity and longer distances as compared to the RS-232

DB-9 Male



RS485

- RS-485 (EIA-485 Standard) is an improvement over RS-422, because it increases the number of devices from 10 to 32
- can create networks of devices connected to a single RS-485 serial port
- The noise immunity and multi-drop capability make RS-485 the serial connection of choice in industrial applications requiring many distributed devices networked to a PC or other controller for data collection, HMI, or other operations.
- all RS-422 devices may be controlled by RS-485. RS-485 hardware may be used for serial communication with up to 4000 feet of cable.

GPIB (IEEE 488)

Origin of GPIB

- The original GPIB was developed in the late 1960s by Hewlett-Packard (where it is called the HP-IB) to connect and control programmable instruments that Hewlett-Packard manufactured.
- With the introduction of digital controllers and programmable test equipment, the need arose for a standard, high-speed interface for communication between instruments and controllers from **various vendors**.
- In 1990, the IEEE 488.2 specification included the Standard Commands for Programmable Instrumentation (SCPI) document. SCPI defines specific commands that each instrument class (which usually includes instruments from various vendors) must obey. Thus, SCPI guarantees complete system compatibility and configurability among these instruments

GPIB controllers (PXI and External)

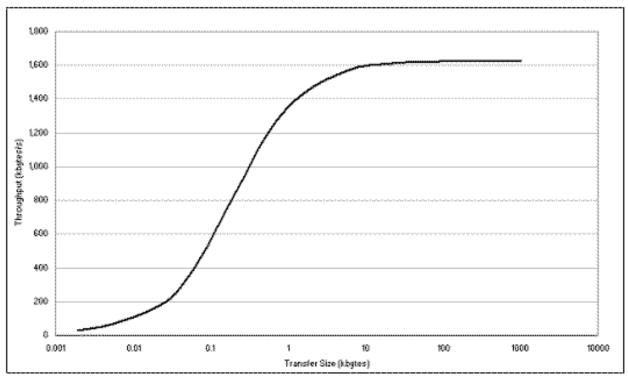




GPIB connector



Performance of a PCI-GPIB Board



It can be seen how fast a GPIB board can transfer data under differing transfer sizes. For example, does the board perform as well using small data blocks and large data blocks? How consistent is the throughput response of the board over a range of data transfer block sizes? Figure shows the performance of the NI <u>PCI-GPIB</u> for various data block sizes.

VXI OVERVIEW

A Proven High Performance Instrument Architecture

VXIbus (VMEbus Extensions for Instrumentation) (IEEE-STD-1155)

Intended to provide:

- High-density platform through shared resources
- Precise timing coordination between instruments
- Longer system support through multi-vendor solutions
- Capability to address high-performance requirements



A VXIbus system or subsystem consists of a mainframe, VXIbus devices, a slot 0 card, resource manager, and host controller.

VXIbus Devices:

Typically message-based or register-based devices

VXIbus Mainframe:

Houses the VXIbus devices (4,5,6 and 13 slot mainframes) Contains the power and cooling mechanism Contains the communication backplane

Slot 0 Interface:

Backplane management and (Shared) System Clock sources Arbitration

Remote control through various comm interfaces

Resource Manager:

Configures the modules for proper operation at power-up and reset

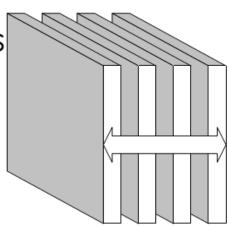
Host Controller:

Controls the operations of the ATE system and environment

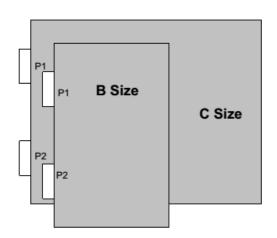


The VXIbus specifies has two primary backplane connectors (P1 and P2). The P1 connector, (mandatory in VME or VXIbus), carries the data transfer bus. The P2 connector, expands the data transfer bus to a full 32-bit size, and adds:

- Four additional power supply voltages
- The local bus
- Analog sumbus
- TTL and ECL trigger buses
- 10 MHz differential ECL clock signal



- P1 16-bit data VMEbus 24-bit addressing + 5, + /-12 Volts
- P2 32-bit data VMEbus 10 MHz clock bus Analog sumbus 12-pin local bus TIL/ECL trigger buses -5.2, -2, +/-24 Volts

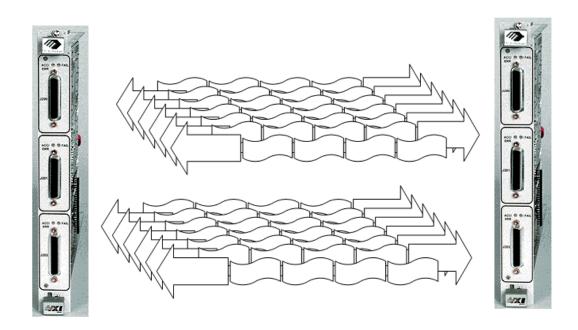


	Size	Spacing
C Size	23.3 x 34 cm (9.2 x 13.4 in.)	3 cm (1.2 in.)
B Size (VME)	23.3 x 16 cm (9.2 x 6.3 in.)	2 cm (0.8 in.)

- C-size cards allow for the addition of EMC/EMI shielding
- Industry's most common and widely supported modular footprint is the Csize card
- One unique logical address (LA) per VXIbus device, allowing for 256 LAs in a single VXIbus system
- Other platforms (i.e. M-modules, PMC, PXI, VME) can be accommodated through the use of adapters

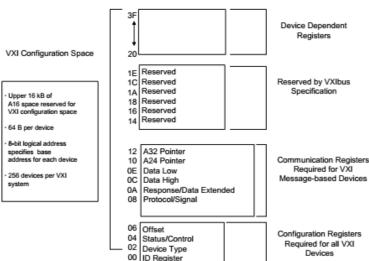
The VXIbus specifies radiated and conducted EMC limits for both generation and susceptibility. This ensures that modules containing sensitive electronic circuits perform to

expectations without interference from any other module operating in the system.



Hardware Communications:

- External computer to VXIbus chassis interface:
 GPIB/VXI, MXI2/VXI, USB 2.0/VXI, Firewire/VXI, LAN/VXI, PCIe/VXI, etc.
 PC-platform and OS independent
- Embedded computer:
 Resides in the slot 0, generally PC- or PPC based



Two main ways to communicate with a VXIbus device:

Message-based devices

The message-based device has a Word Serial Protocol to allow ASCII-level communications. SCPI builds upon this. Relatively low throughput

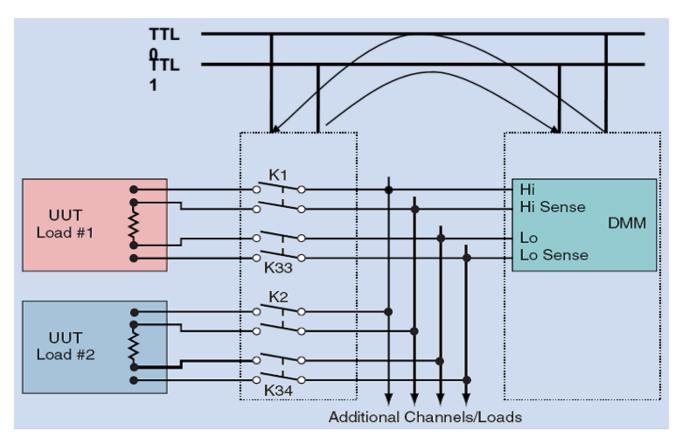
Register-based devices

The register-based device communicates only through register reads and writes. Configuration is controlled by VXIbus-defined configuration registers but programmed through device dependent registers. Up to 320MB/sec throughput

VXI plug&play drivers use the VISA protocol to provide an API that is communications bus agnostic.

Using the Trigger Bus (Application)

- TTL0 DMM measure complete, close next relay channel
- TTL1 Relay has settled, initiate DMM measurement



 Highly deterministic asynchronous handshaking significantly reduces test time by removing any dependency on host controller to manage the switch/measure sequencing

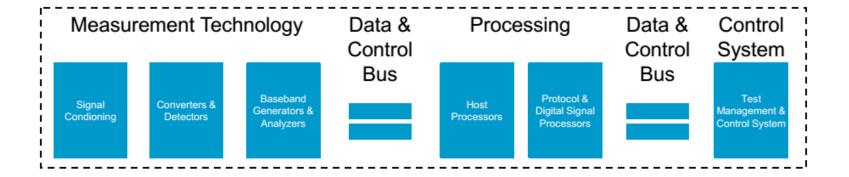
Flexible Remote Control

The VXIbus can attribute its longevity in part to its ability to adapt to newer communication bus architectures for remote control without affecting backward compatibility

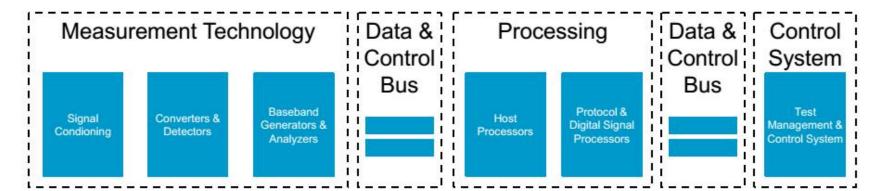


INTRODUCTION TO PXI

Test & Measurement Equipment Consist of Several Building Blocks



Optimized Test & Measurement Architecture for Multichannel and MIMO



Controller

- Test management, control and processing
- Built on latest COTS processors & software
- Upgradable hard drive and memory
- Instant performance upgrade by swapping controller

Peripheral Modules

- Modular measurement technology
- Build-up functional system



Chassis & Backplane

- Data and control bus
- Low latency
- · High bandwidth
- Multiple peripheral slots

PXI – Open Modular Platform for Test & Measurement

Capable T&M Platform

- Foundation adapted from consumer products
- Robust, mature technologies

Current PXI Implementations

- PXI adopts CompactPCI and CompactPCI Express
- Engineering requirements for infrastructure

PXI in Industry

1,500+ products 70+ vendors 100k+ systems deployed



Strengths of PXI in Shared Resources

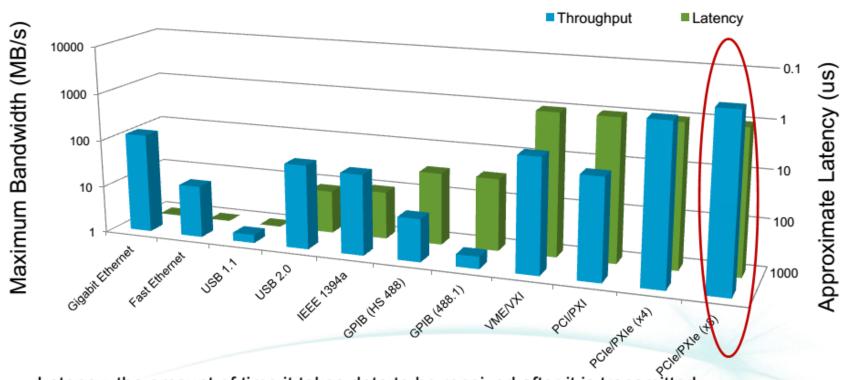
- Instrumentation Clocks
 - 10 MHz and 100 MHz
 - Capable of High Quality
- Trigger Buses
 - Parallel PXI_TRIG
 - Matched STAR and DSTAR Lines
- Data Communication
 - PCI Parallel Bus
 - PCIe Point-to-Point Architecture







Importance of Bandwidth and Latency in T&M Buses



- · Latency: the amount of time it takes data to be received after it is transmitted
- Bandwidth: a measure of the rate of data transferred on a bus over time, measured in MB/s

Goal of System: ↑ bandwidth & ↓ latency

Differences Between PXI and Standalone Box

Modular

- Greater flexibility/scalability
- Integrated system
- Higher throughput
- Smaller footprint
- Lower power
- More cost effective



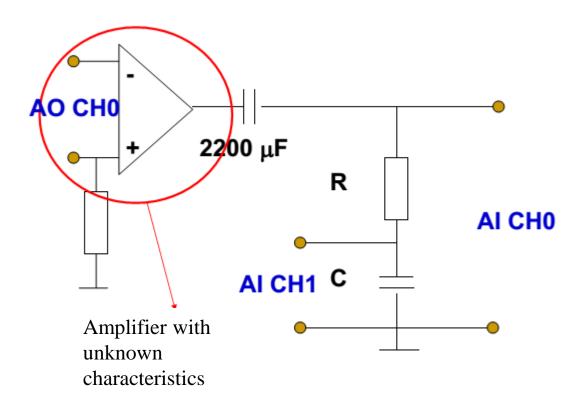


Standalone Box

- Interactive measurement
- Time to first measurement
- Predictable system performance
- Lower software investment
- No infrastructure investment



Frequency response measurement



Frequency response measurement

- The RC is a low-pass filter. It means that on low frequency it has a gain ~1 on high frequencies the gain ~0
- It can be represented by the cut-off frequency (ω_{v})
- Example 1 ($R=1k\Omega$, $C=1\mu F$):

$$\omega_{v} = \frac{1}{RC} = \frac{1}{10^{3}10^{-6}} = 10^{3} \, rad \, / \, S; f_{v} = \frac{\omega_{v}}{2\pi} = \frac{10^{3}}{2\pi} = 159 Hz$$

• Example 2 ($R=1k\Omega$, $C=100\mu F$):

$$\omega_{v} = \frac{1}{RC} = \frac{1}{10^{3}10^{2}10^{-6}} = 10 \, rad \, / \, S; f_{v} = \frac{\omega_{v}}{2\pi} = \frac{10}{2\pi} = 1.59 \, Hz$$

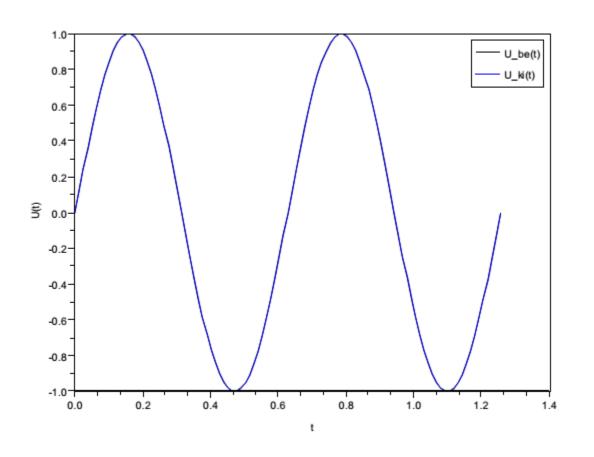
Transfer Characteristics:

$$\xrightarrow{A_1 \cos(\omega t + \varphi_1)} \mathbf{W(j\omega)} \xrightarrow{A_2 \cos(\omega t + \varphi_2)}$$

$$A(\omega_x) = \frac{A_2}{A_1}$$

$$\varphi(\omega_x) = \varphi_2 - \varphi_1$$

Transfer Characteristics (EXAMPLE1):



 ω =10 rad/s

f=1.59 Hz

RC=0.001

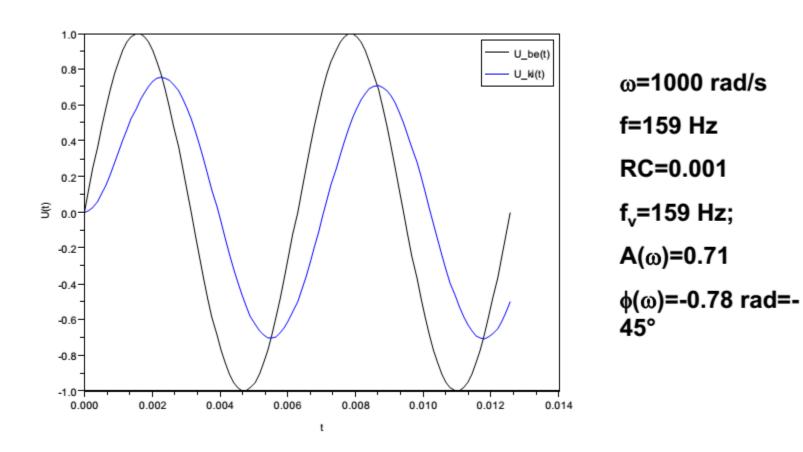
f_v=159 Hz;

 $A(\omega)=0.99$

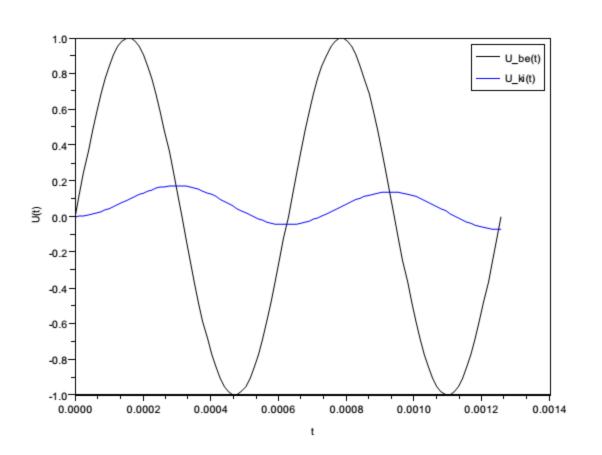
 $\phi(\omega) = -0.0099$

rad=-0.57°

Transfer Characteristics (EXAMPLE2):



Transfer Characteristics (EXAMPLE3):



 ω =10000 rad/s

f=1591 Hz

RC=0.001

f_v=159 Hz;

 $A(\omega)=0.099$

φ(ω)=-1.47 rad=-84.28°

Bode Diagram

