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FACULTY OF COMPUTER SCIENCE AND ENGINEERING

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LOGIC DESIGN PROJECT

SPORTS STOPWATCH DESIGN

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COMMITMENT

We pledge that this project is based on our supervisors' ideas and knowledge. All studies and data have not been published. The references, numbers and statistics are reliable and honest. The group completed the thesis requirements set by faculty of computer science and engineering - department of Computer Engineering.

Sincerely,

Hoàng Vương Vũ Hoàng
Nguyễn Hoàng Minh
Nguyễn Tôn Minh

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Finally, we would like to wish you good health and success in your academic endeavors.

ABSTRACT

Accurate timing plays a vital role in sports, serving as a critical metric for performance evaluation and determining winners.This thesis focuses on the design and implementation of a user-friendly sports stopwatch that meets the specific requirements of athletes, coaches, and sports enthusiasts.

The objective of this research is to develop a stopwatch that provides precise timekeeping down to milliseconds and offers additional functionalities such as lap and split timing. The design process involves gathering requirements, concept development, and prototype creation. The selected components, including a core microcontroller, display module, and input controls, are integrated to create a cohesive system. The stopwatch is designed to be durable, resistant to environmental factors, and optimized for usability. Through testing and evaluation, the performance, accuracy, and usability of the designed stopwatch are assessed. The results demonstrate the effectiveness of the design in enhancing performance tracking and training analysis for athletes and coaches across different sports disciplines.

This research contributes to the field of sports timing devices by providing a practical and reliable tool that enhances the overall sporting experience.

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CHAPTER 1

INTRODUCTION

Accurate timing is paramount in sports for performance evaluation and determining winners. As sports become increasingly competitive, there is a growing demand for innovative and user-friendly sports stopwatches that can meet specific timing requirements. This thesis aims to design and implement a state-of-the-art sports stopwatch that provides precise timing down to milliseconds and offers tailored functionalities for athletes and coaches. In order to establish a solid foundation for the design process, a comprehensive literature review will be conducted to explore the theoretical basis and existing knowledge in the field of sports stopwatches.

The literature review will encompass an in-depth examination of scholarly articles, research papers, and relevant sources related to sports timing devices. It will delve into the theoretical frameworks, models, and concepts that underpin the design and functionality of sports stopwatches. This review will also analyze existing technologies, features, and advancements in the field, identifying gaps and potential areas for improvement.

By synthesizing the findings from the literature review, the research will gain valuable insights into the theoretical underpinnings and practical considerations in designing an advanced sports stopwatch. These insights will inform the decision-making process in selecting the appropriate components, determining the required functionalities, and establishing evaluation criteria for the designed stopwatch.

Overall, the literature review will serve as a crucial step in this thesis, establishing the theoretical basis and existing knowledge in the field of sports stopwatches. It will provide a comprehensive understanding of the current state-of-the-art, identify research gaps, and guide the design and implementation of an innovative and efficient sports stopwatch that meets the specific timing requirements of various sports disciplines.

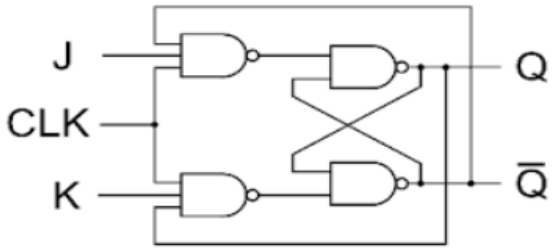
CHAPTER 2

METHODOLOGY

2.1 Theoretical Basis

2.1.1 Flip Flop

Flip-flop is a circuit that maintains a state until directed by input to change the state. A basic flip-flop can be constructed using four-NAND or four-NOR gates.



TRUTH TABLE

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

When receiving a clock pulse at the CLK input, the flip-flop will change its state once. The new state will depend on the logic level of the functional inputs and the truth table specific to each type of flip-flop.
Therefore, the applications of Flip-flops are specified as: counter, Data transfer, Registers,...

2.1.2 Transcoding

Binary-coded decimal (BCD) is a class of binary encodings of decimal numbers where each digit is represented by a fixed number of bits, usually four or eight. It is a fast and efficient system that converts the decimal numbers into binary numbers as compared to the existing binary system.

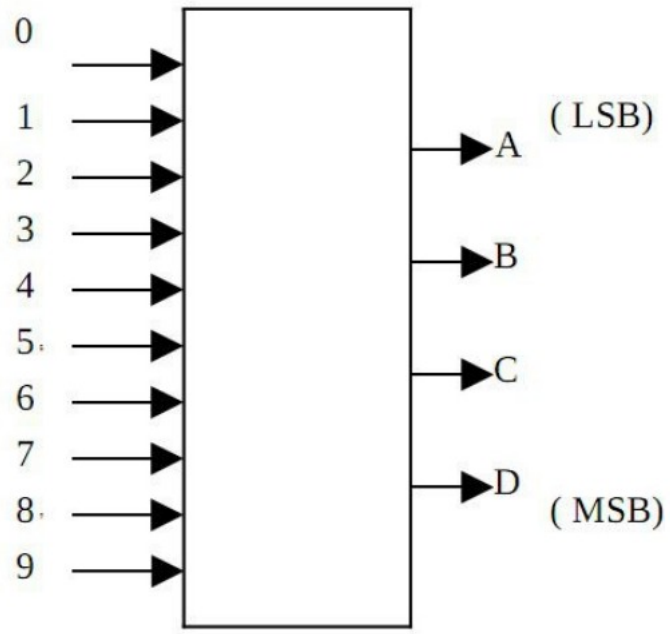
In Binary to BCD conversion, each 4-bit binary number is converted into its corresponding 4-bit BCD representation. The BCD representation represents each decimal digit (0-9) with a 4-bit binary code. Here's a truth table for a 4-bit Binary to BCD (Binary-Coded Decimal) conversion:

Binary(4-bit)				BCD				
X4	X3	X2	X1	Y5	Y4	Y3	Y2	Y1
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	0
0	0	1	1	0	0	0	1	1
0	1	0	0	0	0	1	0	0
0	1	1	1	0	0	1	0	1
0	1	1	0	0	0	1	1	0
0	1	1	1	0	0	1	1	1
1	0	0	0	0	1	0	0	0
1	0	0	1	0	1	0	0	1
1	0	1	0	1	0	0	0	0
1	0	1	1	1	0	0	0	1
1	1	0	0	1	0	0	1	0
1	1	0	1	1	0	0	1	1
1	1	1	0	1	0	1	0	0
1	1	1	1	1	0	1	0	1

2.1.3 Encoding and Decoding

a) **Encoding**

There is some features about decimal encoding to binary



0	1	2	3	4	5	6	7	8	9	D	C	B	A
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	0	0	1	1	0
0	0	0	0	0	0	0	1	0	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1	1	0	0	1

Figure 2.1.3.1: Truth table

Logic Equation:

$D = 8 + 9$

$C = 4 + 5 + 6 + 7$

$B = 2 + 3 + 6 + 7$

$A = 1 + 3 + 5 + 7 + 9$

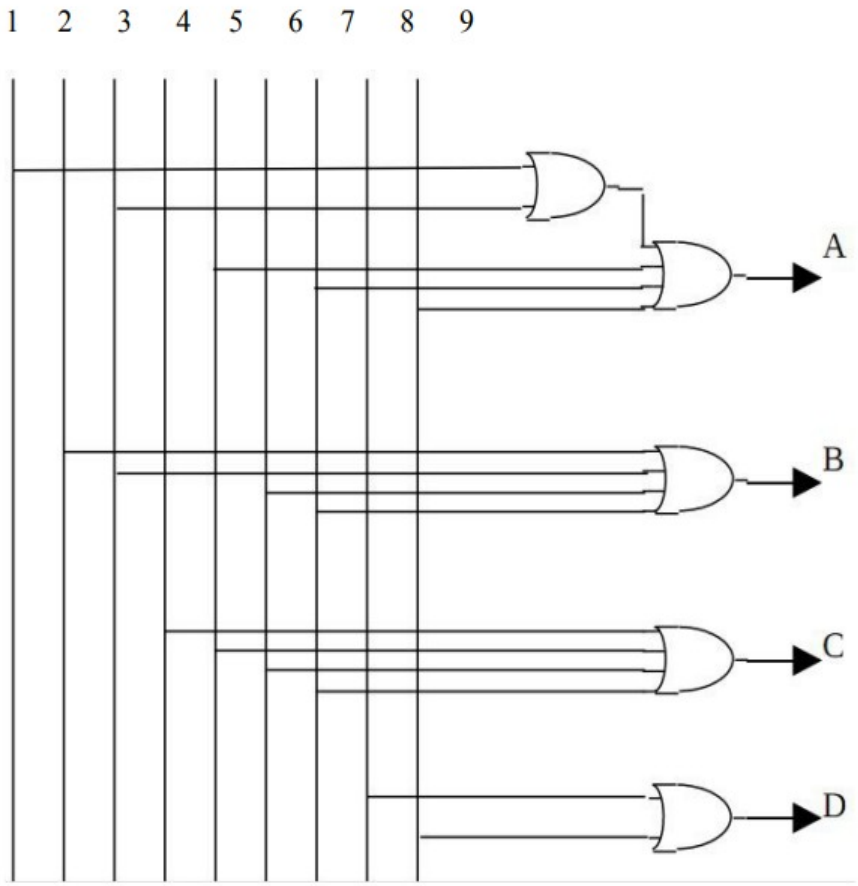
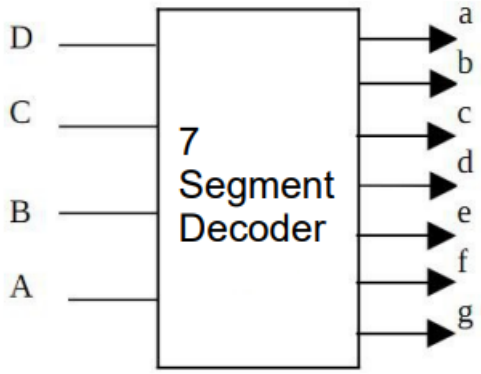


Figure 2.1.3.2: Logic Circuit Diagram:

b) **Decoding**



A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

Figure: 2.1.3.3: Truth Table – For common cathode type BCD to seven segment decoder

Logic equation:

a= $\bar{B}\bar{D} + C + BD + A$

b = $\bar{B} + \bar{C}\bar{D} + CD$

c = $\bar{C} + D + B$

d = $\bar{B}\bar{D} + \bar{B}C + B\bar{C}D + C\bar{D} + A$

e = $\bar{B}\bar{D} + C\bar{D}$

f = $\bar{C}\bar{D} + B\bar{C} + B\bar{D} + A$

g = $\bar{B}C + B\bar{C} + A + B\bar{D}$

2.1.4 Counting System

a) **Definition**

Sequential Counter: In a sequential counter, the output of each flip-flop is connected to the clock input of the next flip-flop in a chain. The counting sequence propagates from one flip-flop to the next, making it a serial or sequential process.

Parallel Counter: In a parallel counter, all flip-flops receive the same clock signal simultaneously. Each flip-flop operates independently and updates its output based on its current state and the input clock signal. The counting operation occurs in parallel, allowing for faster counting

speeds compared to a sequential counter.

Asynchronous Counter: In an asynchronous counter, the flip-flops change state independently of each other. Each flip-flop triggers based on its own clock input, which may result in timing uncertainties and potential glitches in the output signals.

Synchronous Counter: In a synchronous counter, all flip-flops receive the same clock signal simultaneously, ensuring that they change state at the same time. The flip-flops are synchronized to the clock signal, providing a more stable and reliable counting operation.

To create a couting system we use JK Flip-flops. With n-FF, we can create a counting system up to 2^n.

b) **N-counting system**

Assume that:

N is number of states of N-counting system

n is number of counting bit

We have: $2^{(n-1)} < N < 2^n$

For example, A decade counter counts ten different states(from 0 to 9) and then reset to its initial states. Then, $2^3 < 10 < 2^4$. Therefore, we use 4 Flip-flops

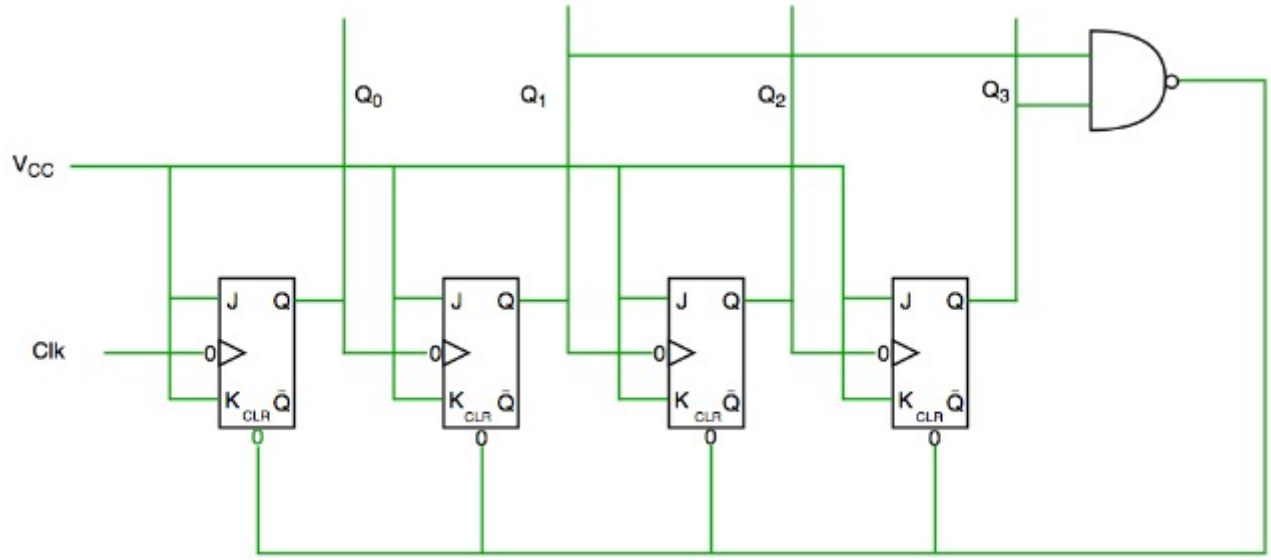


Figure 2.1.4.1: Decade Counter Circuit diagram

Clock pulse	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

Figure 2.1.4.2: Truth table

If we have N-counter and M-counter, we can combine it together. Then, we will have N*M-counting system.

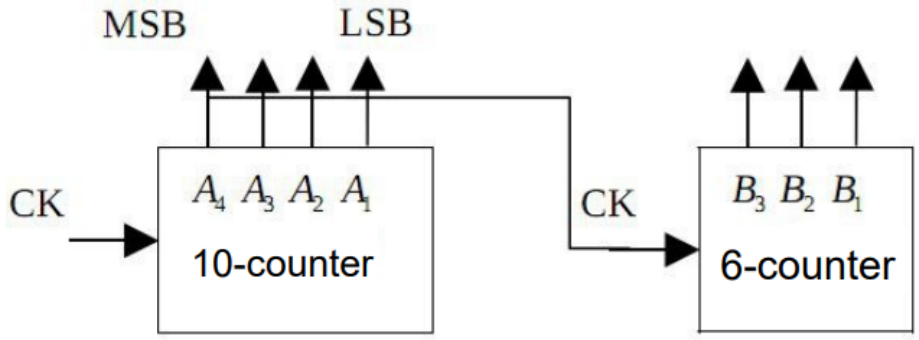


Figure 2.1.4.3: 60-counting system

2.2 Introduction to components

2.2.1 IC NE555

The NE555 is a popular integrated circuit (IC) that is widely used in electronic circuits for various timing, oscillator, and pulse generation applications. Its simplicity and ease of use make it a popular choice.

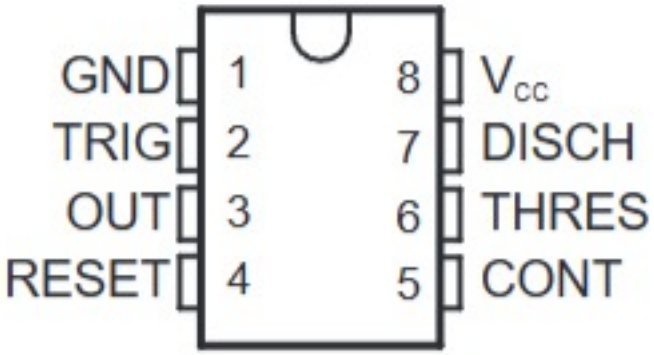


Figure 2.2.1.1: Pin configuration

Pin functions:

NO.1: Ground
NO.2: Trigger Input (Start of timing input)
NO.3: Output
NO.4: Active low reset input
NO.5: Controls comparator thresholds
NO.6: End of timing input.
NO.7: Discharge
NO.8: Input Voltage supply

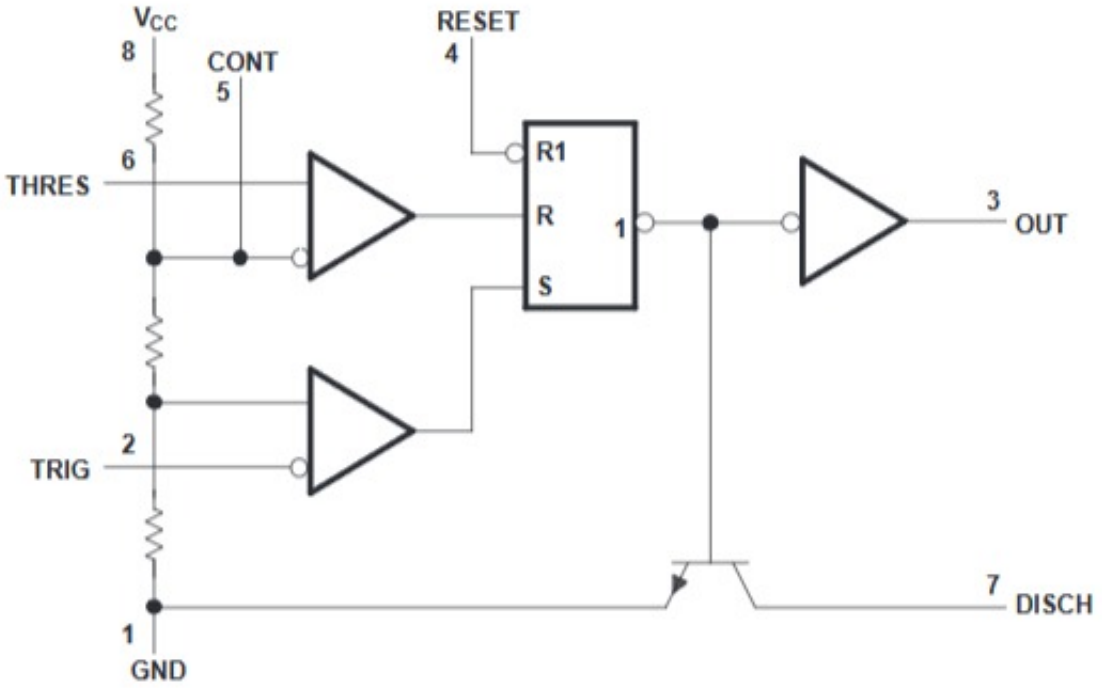


Figure 2.2.1.2: Inside Schema

Inside IC555, it has more than 20 transistors and resistors with the following functionalities:

- Voltage divider consists of 3 resistors $R_1 = R_2 = R_3 = 5k\Omega$ connected from VCC to ground, resulting in two standard Voltage levels of 1/3 V_{CC} and 2/3 V_{CC}.
- COMP1, as a comparator circuit with its $V_{in}^{+} = 1/3V_{CC}$ output connected to pin 6 and V_{in}^{-} referenced through pin 2. Depending on whether the voltage at pin 2 compared to the $1/3V_{CC}$ standard voltage, then COMP1 will generate a HIGH or LOW signal to control the operation of the Flip Flop (FF) through the **S signal**.
- COMP2, as a comparator circuit with $V_{in}^{+} = 2/3V_{CC}$ output connected to pin 6. Depending on whether the voltage at pin 6 compared to $2/3V_{CC}$ standard voltage, then COMP2 will generate a HIGH or LOW voltage to **R signal** control the operation of FF.
- The Flip Flop (FF) circuit is a type of bistable circuit that changes its state when the S input is at a high voltage. This voltage transition triggers the FF, causing the output Q to go to a high level, $\bar{Q} = 0$. When the S input transitions from a high level to a low level, the FF does not

change its state.

$S = 1$	$Q = 1$	$\bar{Q} = 0$
$S = 1$	$Q = 0$	FF does not change its state

- When the R input has a high voltage, it triggers a state change in the Flip Flop (FF) such that $\bar{Q} = 0$ and $Q = 0$. When the R input transitions from a high level to a low level, the FF does not change its state.
- The inverting amplifier circuit is used to amplify the current supplied to the load. It has an input connected to $\bar{Q}$ of the Flip Flop (FF), so when $\bar{Q}$ is at a high level, the output at pin 3 has a low voltage of 0V, and vice versa.
- T-transistor is a transistor with an open C-terminal, connecting to pin 7.Because the base terminal(B) is biased by the output voltage $\bar{Q}$ of the Flip Flop (FF), when the base voltage is high, T_2 becomes saturated, and the collector terminal(C) of T_2 is effectively connected to ground. At that time, the output at pin 3 is at a low level. When $\bar{Q}$ is LOW, T_2 is in cut-off state and C-terminal of T_2 is left open, then the output at pin 3 is at a high level. According to the above principle, the C-terminal of T_2 at pin 7 can generate an output that is dependent on the same voltage levels as the output at pin 4.

2.2.2 IC 74LS90

IC 7490 is a decade counter integrated circuit that consists of two separate divide-by-5 and divide-by-2 counter sections. Each counter section can independently divide the input clock signal by 5 or 2, depending on the control inputs.

- The divide-by-2 counter section is controlled by the input signal $\overline{CP_0}$ to give output Q_A.
- The divide-by-5 counter section is controlled by the input signal $\overline{CP_1}$ to give output Q_B, Q_C, Q_D.

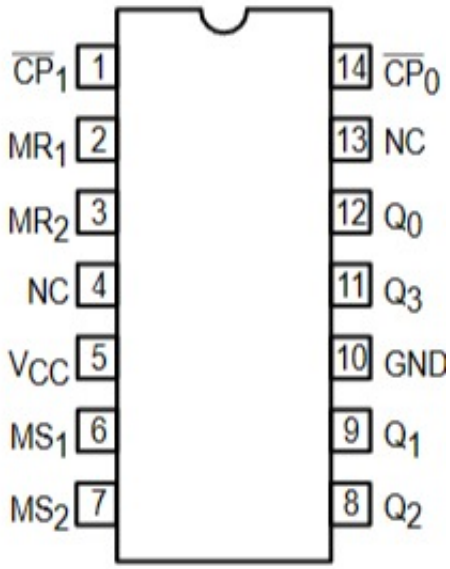


Figure 2.2.2.1: Connection Diagram DIP (Top view)

Pin names:

$\overline{CP_0}, \overline{CP_1}$	: Clock (Active LOW going edge)
Q_0, Q_1, Q_2, Q_3	: Output
MS_1, MS_2	: Master Set
NC	: No Internal Connection

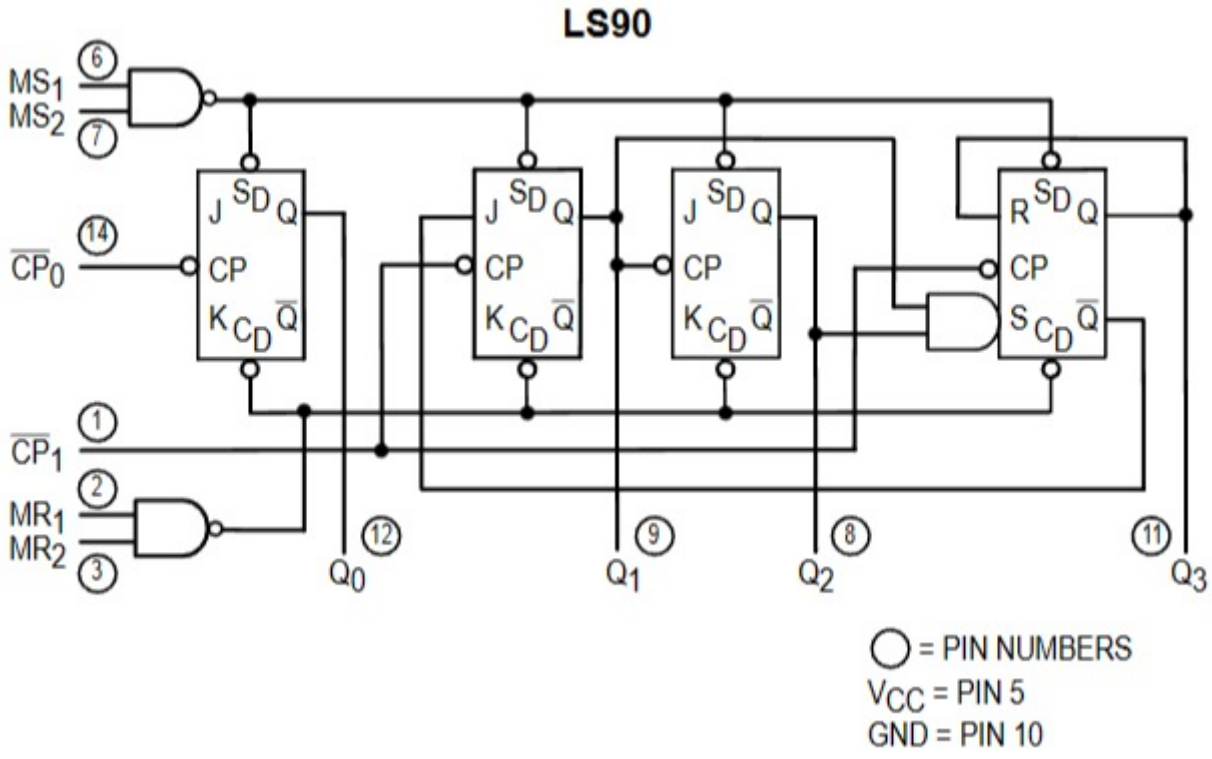


Figure 2.2.2.2: Logic Diagram

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Figure 2.2.2.3: Status table

2.2.3 IC CD4511

The CD4511 is a BCD to 7-segment LED display decoder IC (Integrated Circuit). It is designed to convert binary-coded decimal (BCD) input signals into the corresponding 7-segment LED display output.

The CD4511 is commonly used in applications requiring the decoding of BCD signals for driving 7-segment LED displays. It provides a convenient and efficient solution for displaying decimal numbers or characters in digital circuits, counters, timers, calculators, and other similar projects.

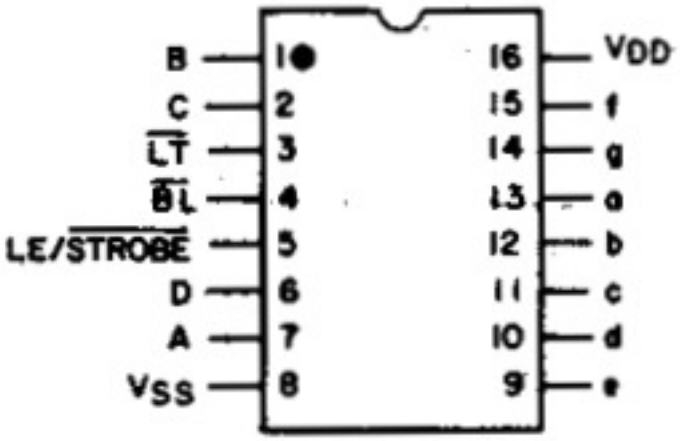


Figure 2.2.3.1: Connection Diagram

Pin Descriptions:

A,B,C,D: BCD inputs

$\overline{BL}$: Blanking Input (Active LOW)

$\overline{LT}$: Lamp Test Input (Active LOW)

$\overline{LE}/\overline{STROBE}$: Latch Enable or Strobe input is used for storing BCD code

V_{SS}: Ground

V_{DD}: Positive power supply

$a - g$: 7 Segment Outputs

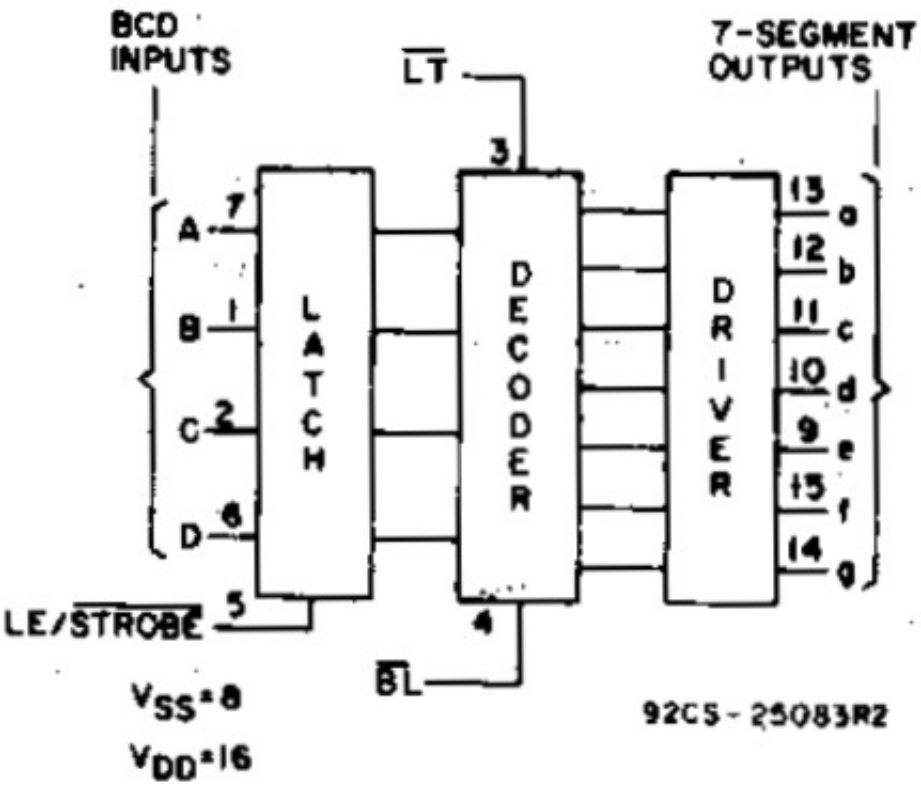


Figure 2.2.3.2: Functional Diagram

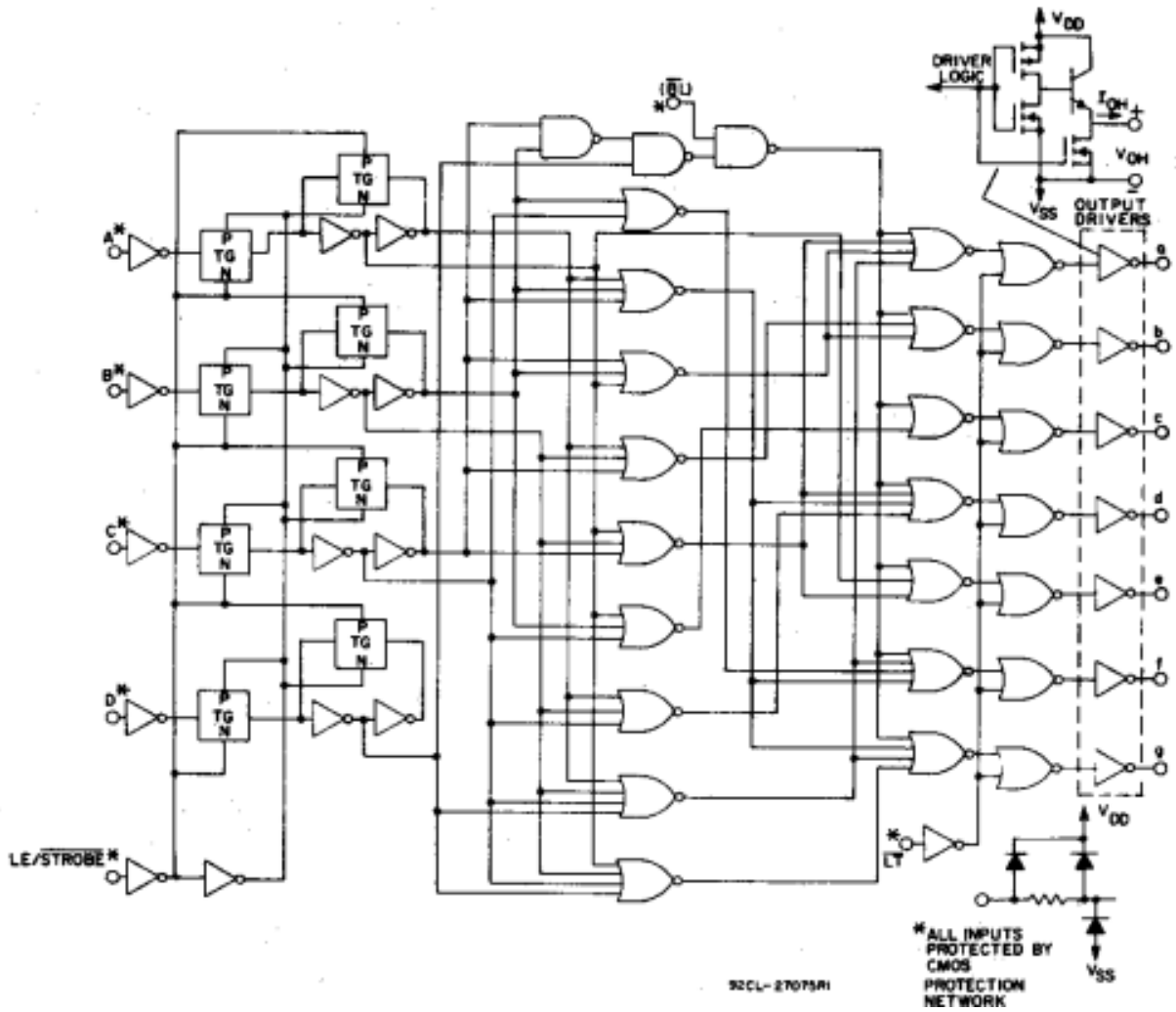


Figure 2.2.3.3: Logic Diagram

CHAPTER 3

CIRCUIT DESIGN

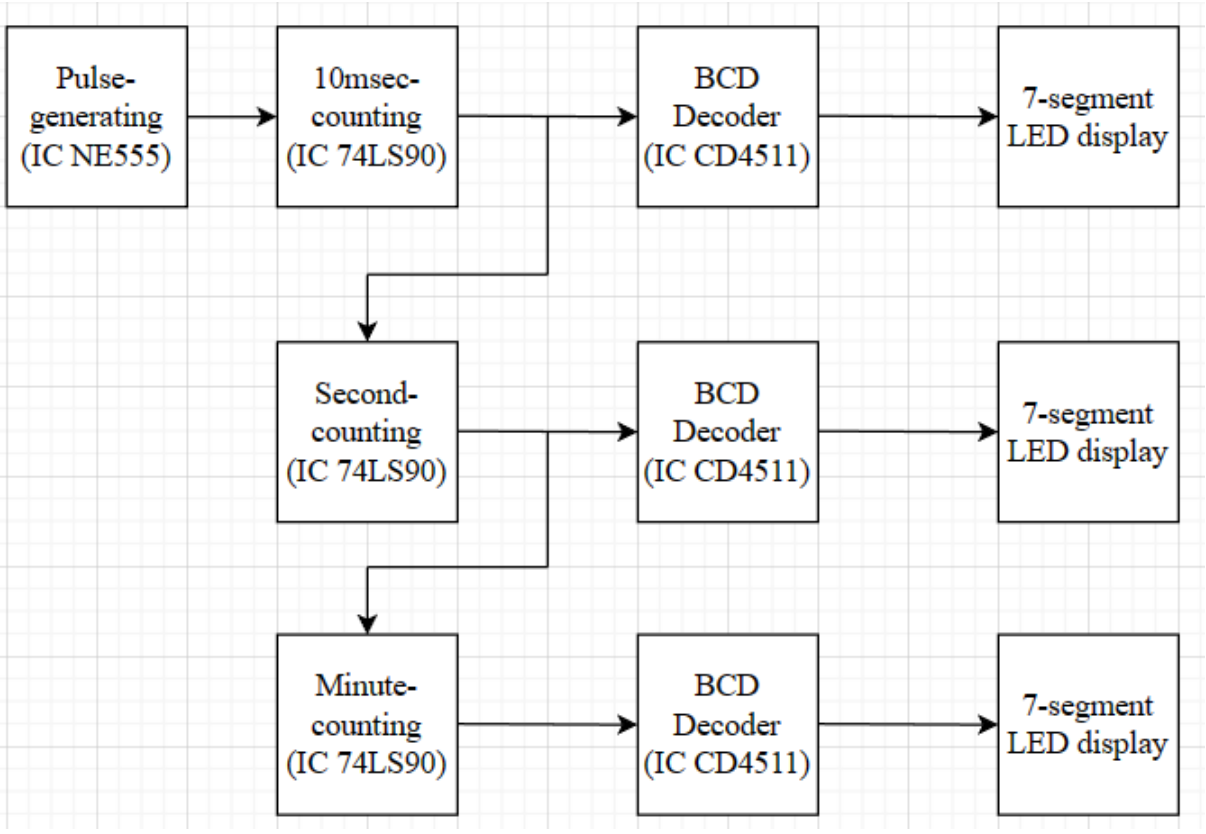


Figure 3.1: Block Diagram

a) **Pulse-generating block**

The pulse generator is the most important component of the system, especially for the counter, as it determines the output states of the counter. There are many circuits used for generating oscillations, but we are primarily interested in the 555 timer IC-based oscillator circuit due to its widespread use. The 555 timer IC is a dedicated timing integrated circuit

that can be configured as a monostable or astable multivibrator circuit.

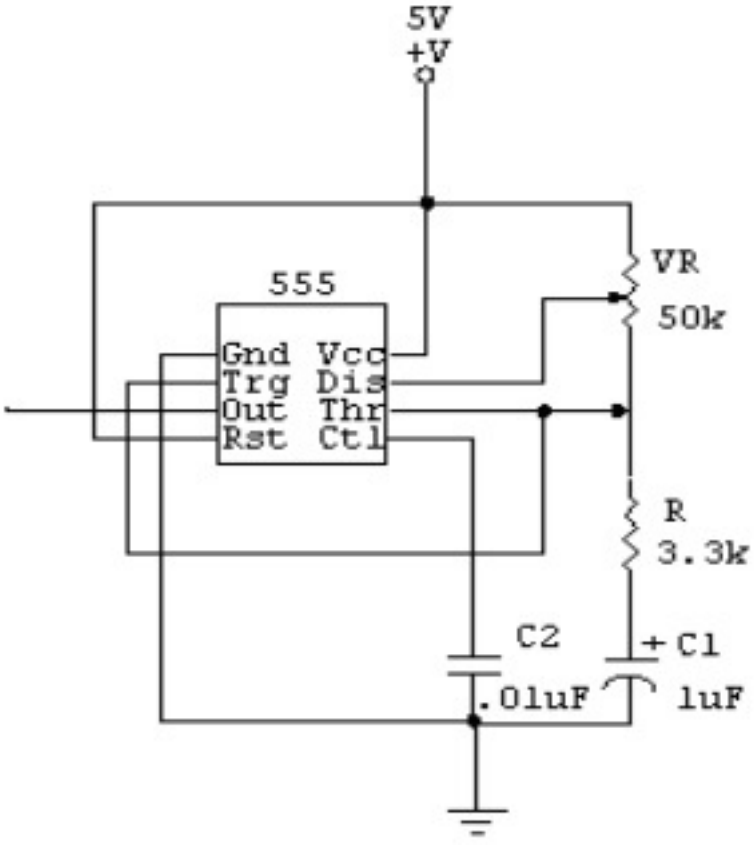


Figure 3.2: Pulse-generating circuit diagram

When Vcc is initially applied, the capacitor starts charging from 0V upwards:

OP-AMP 1: $V_{in}^{+} < V_{in}^{-} \quad => \quad R = 0$
OP-AMP 2: $V_{in}^{+} > V_{in}^{-} \quad => \quad S = 1$
$=> Q = 1, \bar{Q} = 0, V_0 = 1$: LED is ON

When the voltage at the base terminal of transistor Q_2 (U_B) is 0, it turns off Q_2. The capacitor C continues to charge through resistors R_1 and R_2, with a constant time $\quad T_{charge} = (R_1 + R_2)\mathrm{C}$

When the voltage V_C increase to be greater than $1/3V_{CC}$,then:

OP-AMP 1: $V_{in}^{+} < V_{in}^{-} \quad => \quad R = 0$
OP-AMP 2: $V_{in}^{+} < V_{in}^{-} \quad => \quad S = 0$

$=> Q = 1, \bar{Q} = 0, V_0 = 1$: LED is ON, FF's state does not change

When the voltage V_C increase to be greater than $2/3V_{CC}$,then:

OP-AMP 1: $V_{in}^+ > V_{in}^-$ => $R = 1$
OP-AMP 2: $V_{in}^+ < V_{in}^-$ => $S = 0$
$=> Q = 0, \bar{Q} = 1, V_0 = 0$: LED is OFF

Since $\bar{Q}$ is equal to 1, Q_2 gradually saturates, causing pin 7 to be at 0V. As a result, capacitor C is discharged through resistor R_2, via the junction between the collector and emitter (CE) of Q_2, and towards ground.

The time constant of the discharge process for the capacitor is

$$T_{discharge} = R_2 C$$

When $V_C < 2/3V_{CC} : R = 0, S = 0$: the state of the system remains unchanged.

When $V_C < 1/3V_{CC} : R = 0, S = 1 => Q = 1, \bar{Q} = 0, V_0 = 1$: LED is ON

When $\bar{Q} = 0$, Q_2 is turned off, ending the discharge process of capacitor C. As a result, the circuit returns to its initial state, and the capacitor starts charging again. This phenomenon occurs continuously and cyclically.

Because we count to 10ms, we need NE555 generate a clock pulse with 100Hz.

Astable mode examples with common values

Frequency	C	R_1	R_2	Duty cycle
0.1 Hz (+0.048%)	100 µF	8.2 kΩ	68 kΩ	52.8%
1 Hz (+0.048%)	10 µF	8.2 kΩ	68 kΩ	52.8%
10 Hz (+0.048%)	1 µF	8.2 kΩ	68 kΩ	52.8%
100 Hz (+0.048%)	100 nF	8.2 kΩ	68 kΩ	52.8%
1 kHz (+0.048%)	10 nF	8.2 kΩ	68 kΩ	52.8%
10 kHz (+0.048%)	1 nF	8.2 kΩ	68 kΩ	52.8%
100 kHz (+0.048%)	100 pF	8.2 kΩ	68 kΩ	52.8%

Figure 3.3: Frequency Table with respective component value

b) **Couting block**

To create a decade counter, we connect the output of the 4-bit counter(Q_A) to the $\overline{CP_1}$ input to generate the clock pulse for the 5-bit counter. This configuration allows the 4-bit counter to count up to 9 (decimal), and when it reaches 9, it triggers the $\overline{CP_1}$ input of the 5-bit counter, causing it to increment by one and reset the 4-bit counter back to 0. This way, the combined counters form a 10-bit counter capable of counting from 0 to 9 in a cyclic manner.

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

Figure 3.4: BCD Count Sequence

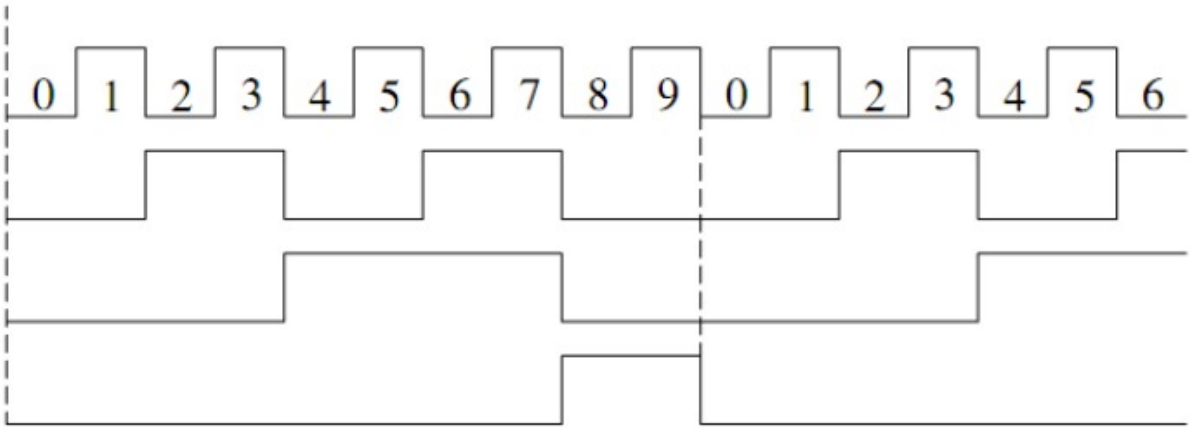


Figure 3.5: Output Q_A, Q_B, Q_C, Q_D

c) **Decoding block**

TRUTH TABLE.

LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X ≡ Don't Care

* Depends on BCD code previously applied when LE = 0

Note: Display is blank for all illegal input codes (BCD > 1001).

Figure 3.6: Truth table

In the case of IC CD4511, since it is a high-level active IC, its logic level 0 outputs are turned off (LED segments are not illuminated), and logic level 1 outputs are turned on (LED segments are illuminated). These outputs correspond to the segments a, b, c, d, e, f, g of the 7-segment LED display. The states of the outputs also correspond to decimal numbers (excluding numbers 10 to 15).

The input pin $\overline{BI}$ is used to enable or disable the decoding operation. When $\overline{BI}$ is connected to logic 1, the decoding operation is enabled and the outputs function normally according to their respective states. However, if $\overline{BI}$ is connected to logic 0 , all the output segments will be turned off regardless of their individual states.

The CD4511 also features a lamp test input pin called LT. When LT is connected to logic 0, all the output segments will be turned on, allowing for testing and verification of the LED display.

When a 4-bit BCD input value is applied to the CD4511, representing decimal numbers from 0 to 9, the corresponding LED segments will be illuminated to display the respective numbers. The CD4511 does not support numbers 10 to 15, and the corresponding LED display will be turned off for these values.

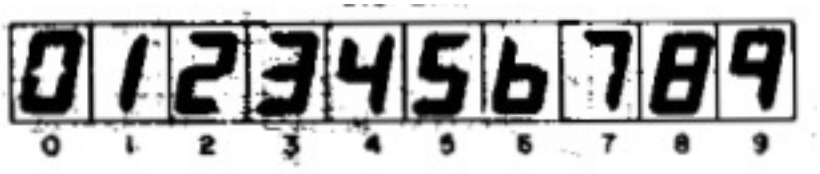


Figure 3.7: Numerical Designations — Resultant Displays

d) **Display block**

The display is implemented using a common anode 7-segment LED configuration because the output of IC CD4511 is active low (logic 0 is the active state). In a common anode configuration, the anodes of the LED segments are connected to the +5V power supply. To turn on a specific segment, the corresponding cathode is connected to logic low (ground) through a current-limiting resistor. Pin 3 and Pin 8 are connected together.

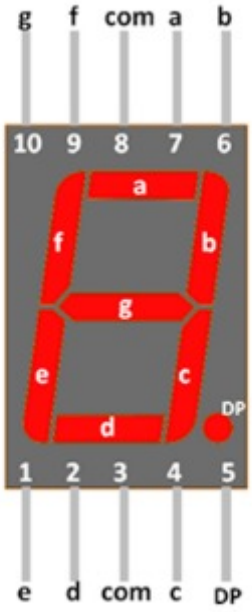


Figure 3.8: 7 Segment Display Pinout

CHAPTER 4

RESULTS

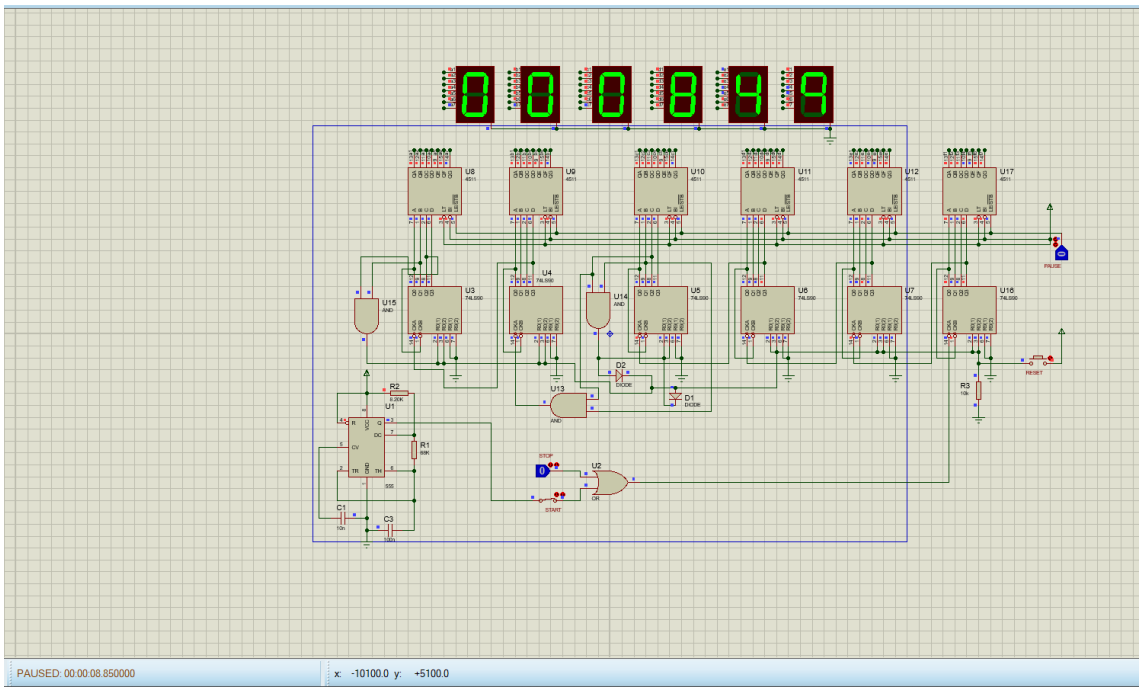


Figure 4.1: Simulation result

a) **Result**

The circuit work well in Proteus simulation. There is a small delay between the time on the LED display and the simulation time of the Proteus tool due to the trigger button must be clicked manually.

b) **User handout** To ensure a seamless user experience, we have prepared a comprehensive user handout that serves as a guide for operating the sport timer.

1. Start/Pause Button: When the timer is in the initial state or reset, pressing the start/pause button initiates the timing process. The

timer begins counting up from 00:00:00, indicating the elapsed time. The button also serves as a pause button. Pressing it while the timer is running will temporarily halt the time count, freezing the displayed time. Pressing the start/pause button again resumes the timing process from the paused time.

2. Reset Button: The reset button clears the timer's current state and resets the time count. If the timer is running, pressing the reset button stops the time count and sets it back to 00:00:00. If the timer is paused, pressing the reset button clears the paused time, and the timer reverts to the initial state with a displayed time of 00:00:00.

CHAPTER 5

CONCLUSION

In conclusion, this project focused on the implementation of a BCD to 7-segment LED display decoder using the CD 4511 IC. The objective was to accurately decode BCD input signals and showcase the corresponding decimal numbers or characters on the 7-segment LED display.

Throughout the project, the CD 4511 IC proved to be a reliable and suitable choice for the decoding process. By properly connecting the IC to the 7-segment LED display and providing the necessary BCD input signals, the desired information was successfully displayed.

The project not only demonstrated the functionality of the CD 4511 IC but also allowed for practical learning in terms of IC selection, circuit design, and understanding the principles of BCD decoding and LED display operation.

Overall, the project achieved its objectives by effectively utilizing the CD 4511 IC to decode BCD signals and provide accurate visual representations on the 7-segment LED display. It provided valuable insights into digital electronics and expanded knowledge in circuit design and IC integration.

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