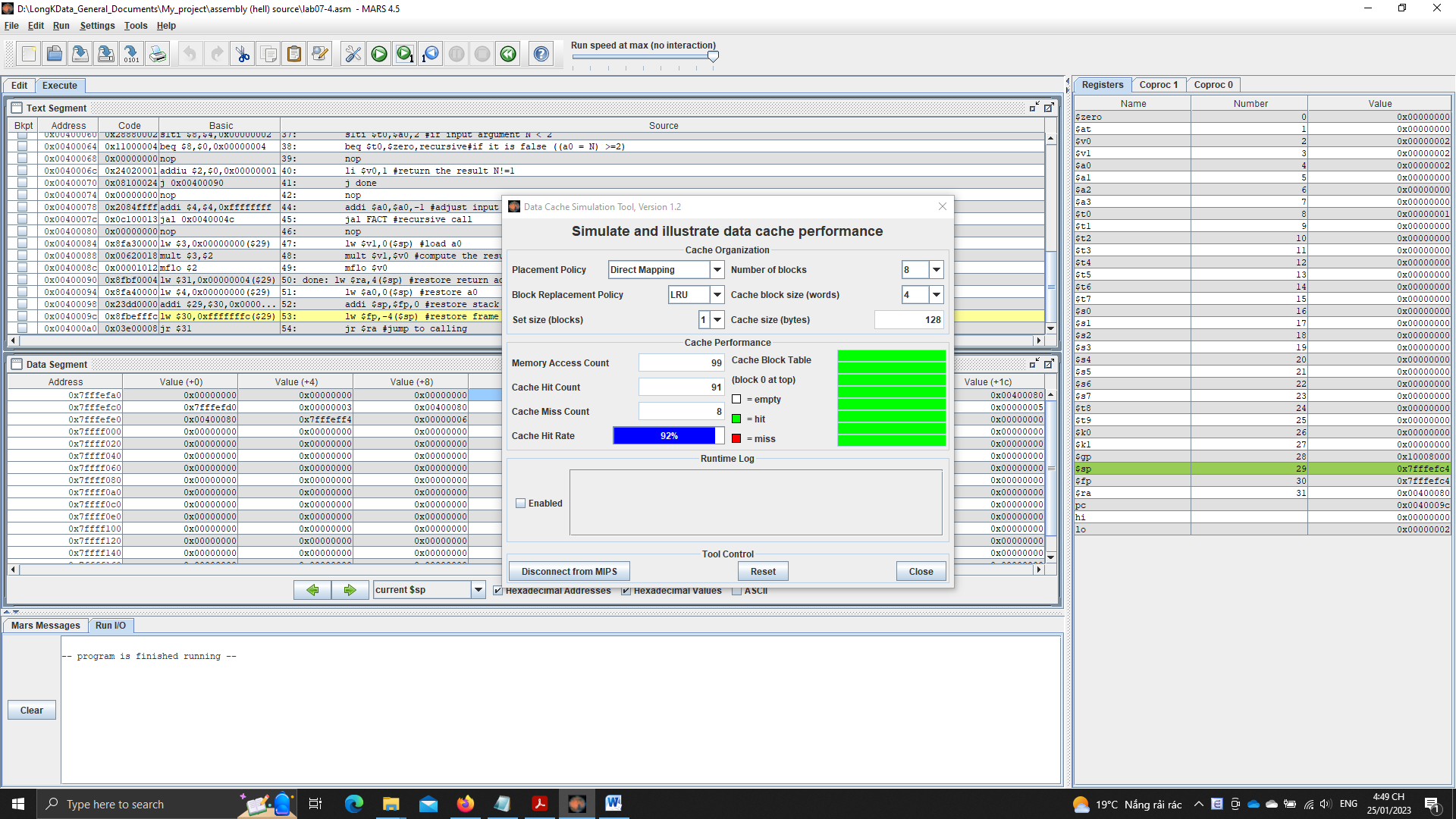
Name: Dang Hoang Long

Class: ICT-02 K65

**Lab 12**

**Assignment 1:**

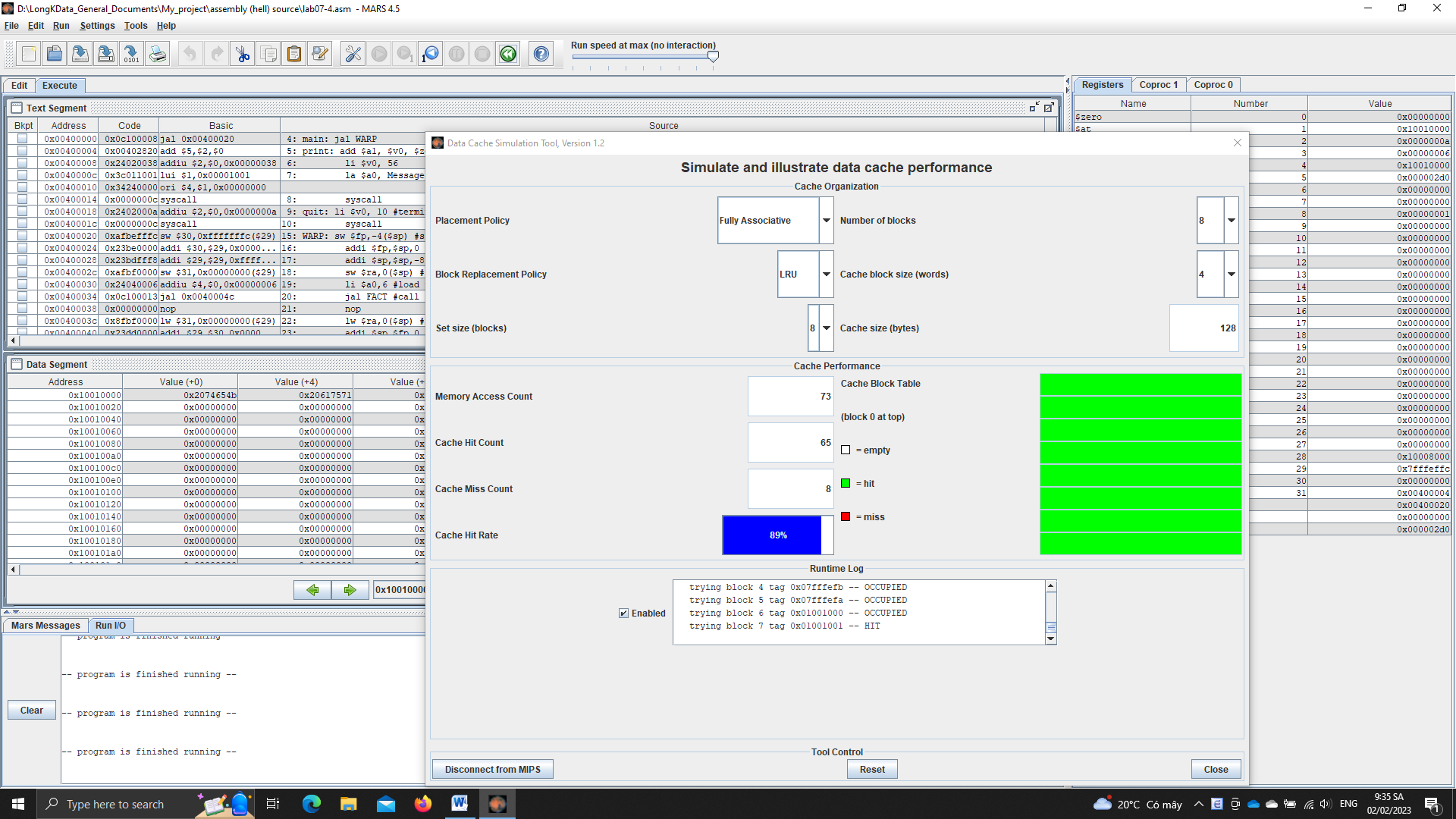


**Assignment 2:**

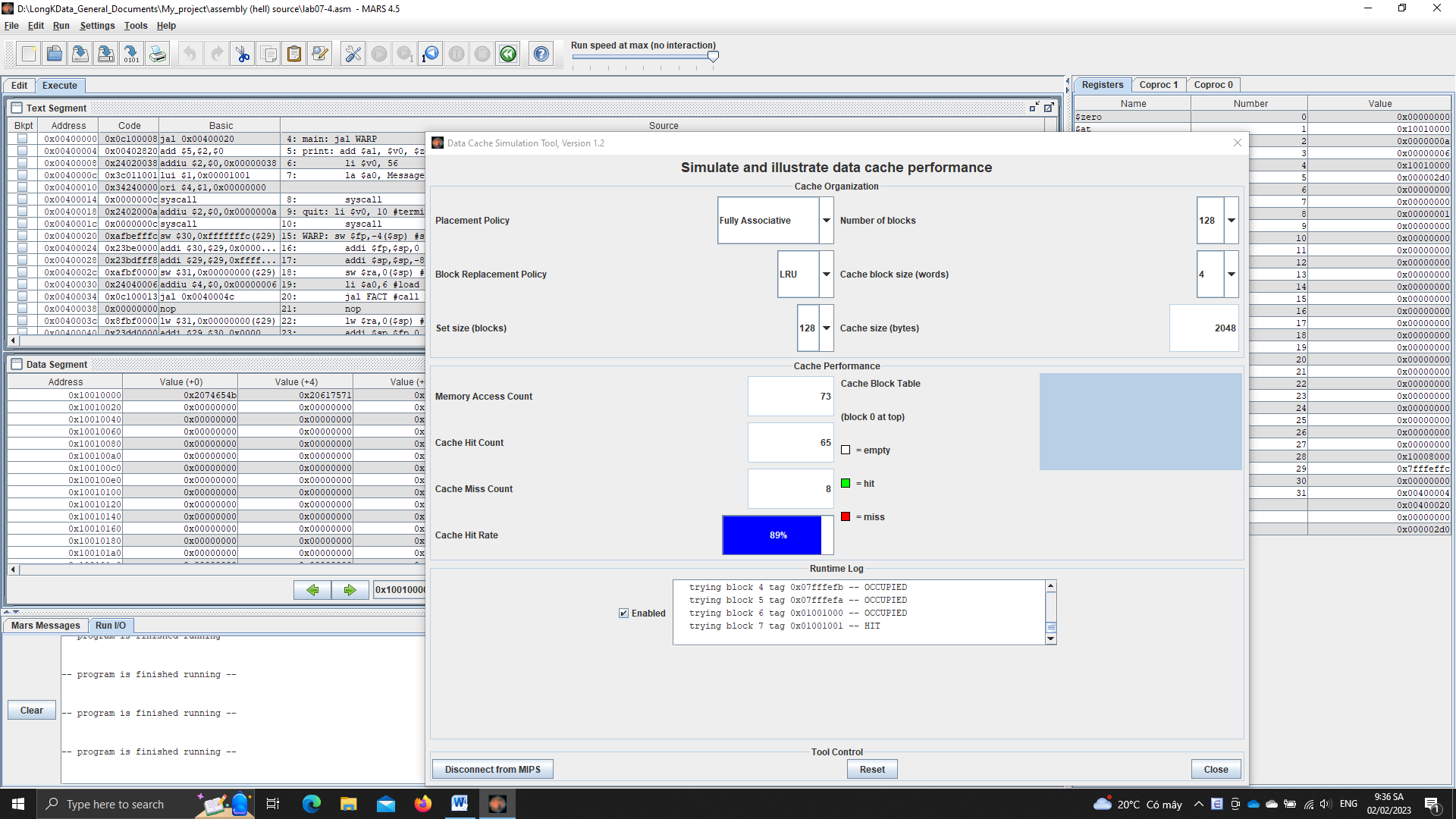
* A full 32-bit address in cache memory is used in some principles:
  + The least significant bits of the address are used to specify the byte within the block.
  + The next set of bits are used to specify the block number within the cache.
  + The remaining bits, known as the tag, are used to identify the main memory location of the block.
* When there is a cache miss, the processor must access the main memory to retrieve the requested data
* When there is a cache hit, the processor can access the requested data from the cache, which is much faster than accessing the main memory
* The block size is 4 words ~ 16 bytes
* The tag is used to identify the main memory location of the block stored in the cache

**Assignment 3:**

* Answer the questions:
  + Cache size: total size of the cache (128 bytes)
  + Block size: size of each cache line (4 words = 16 bytes)
  + Set size: size of each set (apply for set associative placement policies) (1 block – no set split)
  + Write policy: the policy to determine which memory block should be placed in the cache (Direct, fully associative,…)
  + Replacement policy: the policy to determine which cache line should be replaced when the cache is full (LRU, LFU, random, FIFO,…)
* The miss rate is the same when changing the block size



**(**8 blocks**)**



(128 blocks)

The cache miss rate is the same, 8. So, there’s no good or bad.

* Nothing shoud be changed, since when increasing size of cache, te miss rate and the performance is the same.