Session 1 - homework

Homework 1:

Prove the below expressions are equivalent !!!

(1) $x'yz' + x'yz + xy'z' + xy'z + xyz' + xyz = (x+y+z).(x+y+z')$

$VT = x'y(z'+z) + xy'(z'+z) + xy(z'+z)$

$= x'y + xy' + xy$

$= x'y + x(y'+y)$

$= x'y + x = x'y + x(1+y) = x'y + x + xy = x + y(x'+x)$

$= x + y$

$VP = (x+y+z)(x+y+z')$

$= x + xy + xz' + xy + y + yz' + xz + yz$

$= x + xy + y + xz' + xz + yz' + yz$

$= x + y(1+x) + x(z'+z) + y(z'+z)$

$= x + y + x + y$

$= x + y$

$\Rightarrow VT = VP \Rightarrow$ đpcm

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(2) $A' + A.B' + A.B.C' = A' + B' + C'$

$VT = A' + A(B' + BC')$

$= A' + A(B' + C')$

$= A' + (B' + C') = A' + B' + C' = VP \Rightarrow$ dpcm

Homework 2 (*) (advanced level)

"The output of an XOR gate is high (1) when the number of true inputs is odd, and it is low (0) when the number of true inputs is even."

=) Truth table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

SOP $\rightarrow$ $Y = \bar{A}B + A\bar{B} = A \oplus B$

CMOS diagram: $\rightarrow$