HOMEWORK 1:

```
huugiap@ictc-eda-ldap-1:~/07_ss07/decoder_3to8/rtl$ cat decoder_2to4.v
module decoder_2to4 (
 input E,
 input [1:0] A,
 output reg [3:0] Y
);

always @(*) begin
 if (E == 1'b0) begin
   Y = 4'b0000;
 end else begin
   case(A)
     2'b00: Y = 4'b0001;
     2'b01: Y = 4'b0010;
     2'b10: Y = 4'b0100;
     2'b11: Y = 4'b1000;
   default: Y = 4'b0000;
   endcase
   end
end

endmodule
```

```
huugiap@ictc-eda-ldap-1:~/07_ss07/decoder_3to8/rtl$ cat decoder_3to8.v
module decoder_3to8 (
 input [2:0] X,
 output [7:0] Y
);

wire enable_lower;
wire [3:0] y_lower_out;
wire [3:0] y_upper_out;

assign enable_lower = ~X[2];

decoder_2to4 decoder_lower (
 .E(enable_lower),
 .A(X[1:0]),
 .Y(y_lower_out)
);

decoder_2to4 decoder_upper (
 .E(X[2]),
 .A(X[1:0]),
 .Y(y_upper_out)
);

assign Y = {y_upper_out, y_lower_out};

endmodule
```

```
huugiap@ictc-eda-ldap-1:~/07_ss07/decoder_3to8/sim$ make build
vlib work
** Warning: (vlib-34) Library already exists at "work".
Errors: 0, Warnings: 1
vmap work work
Questa Intel Starter FPGA Edition-64 vmap 2023.3 Lib Mapping Utility 2023.07 Jul 17 2023
vmap work work
Modifying modelsim.ini
vlog -f compile.f | tee compile.log
Questa Intel Starter FPGA Edition-64 vlog 2023.3 Compiler 2023.07 Jul 17 2023
Start time: 00:04:38 on Mar 31,2025
vlog -f compile.f
-- Compiling module decoder_2to4
-- Compiling module decoder_3to8
-- Compiling module test_bench

Top level modules:
        test_bench
End time: 00:04:38 on Mar 31,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
```

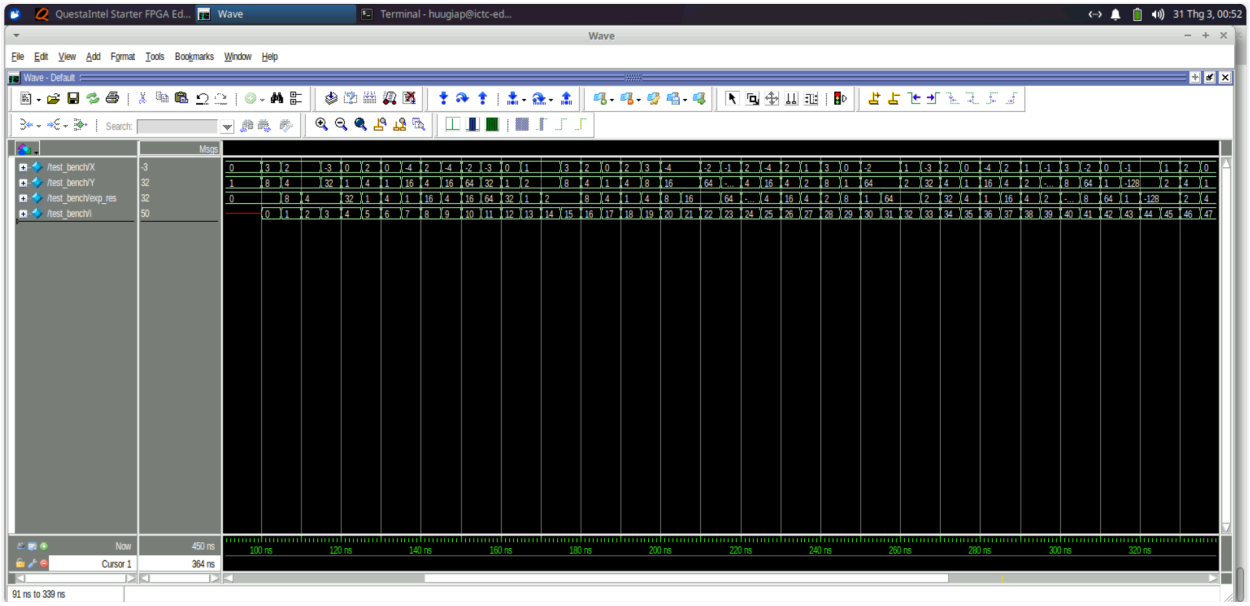
```
huugiap@ictc-eda-ldap-1:~/07_ss07/decoder_3to8/sim$ make run
vsim -debugDB -l test_adder.log -voptargs="+acc" -assertdebug -c test_bench -do "log -r /*;run -all;"
Reading pref.tcl

# 2023.3

# vsim -debugDB -l test_adder.log -voptargs="+acc" -assertdebug -c test_bench -do "log -r /*;run -all;"
# Start time: 00:11:00 on Mar 31,2025
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# ** Note: (vsim-8611) Generating debug db.
# ** Warning: (vopt-10587) Some optimizations are turned off because the +acc switch is in effect. This will cause your simulation to run slowly. Please use -access/-debug to maintain needed visibility.
# ** Note: (vsim-12126) Error and warning message counts have been restored: Errors=0, Warnings=1.
# //  Questa Intel Starter FPGA Edition-64
# //  Version 2023.3 linux_x86_64 Jul 17 2023
# //
# //  Copyright 1991-2023 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  QuestaSim and its associated documentation contain trade
# //  secrets and commercial or financial information that are the property of
# //  Mentor Graphics Corporation and are privileged, confidential,
# //  and exempt from disclosure under the Freedom of Information Act,
# //  5 U.S.C. Section 552. Furthermore, this information
# //  is prohibited from disclosure under the Trade Secrets Act,
# //  18 U.S.C. Section 1905.
# //
# Loading work.test_bench(fast)
# Loading work.decoder_3to8(fast)
# Loading work.decoder_2to4(fast)
# ** Note: (vsim-8900) Creating design debug database vsim.dbg.
# log -r /*
# run -all
```

```
# ====================================
# ==== Case: 0 X = 3    =======
# ====================================
# Exp:   8 Actual:   8
# >>>>>>>>>>>  PASS <<<<<<<<<<<
#
# ====================================
# ==== Case: 1 X = 2    =======
# ====================================
# Exp:   4 Actual:   4
# >>>>>>>>>>>  PASS <<<<<<<<<<<
#
# ====================================
# ==== Case: 2 X = 2    =======
# ====================================
# Exp:   4 Actual:   4
# >>>>>>>>>>>  PASS <<<<<<<<<<<
#
# ====================================
# ==== Case: 3 X = 5    =======
# ====================================
# Exp:  32 Actual:  32
# >>>>>>>>>>>  PASS <<<<<<<<<<<
#
# ====================================
# ==== Case: 4 X = 0    =======
# ====================================
# Exp:   1 Actual:   1
# >>>>>>>>>>>  PASS <<<<<<<<<<<
#
# ====================================
# ==== Case: 5 X = 2    =======
# ====================================
# Exp:   4 Actual:   4
# >>>>>>>>>>>  PASS <<<<<<<<<<<
```

```
# Exp: 128 Actual: 128
# >>>>>>>>>>>  PASS <<<<<<<<<<<
#
# ====================================
# ==== Case:44 X = 7    =======
# ====================================
# Exp: 128 Actual: 128
# >>>>>>>>>>>  PASS <<<<<<<<<<<
#
# ====================================
# ==== Case:45 X = 1    =======
# ====================================
# Exp:   2 Actual:   2
# >>>>>>>>>>>  PASS <<<<<<<<<<<
#
# ====================================
# ==== Case:46 X = 2    =======
# ====================================
# Exp:   4 Actual:   4
# >>>>>>>>>>>  PASS <<<<<<<<<<<
#
# ====================================
# ==== Case:47 X = 0    =======
# ====================================
# Exp:   1 Actual:   1
# >>>>>>>>>>>  PASS <<<<<<<<<<<
#
# ====================================
# ==== Case:48 X = 7    =======
# ====================================
# Exp: 128 Actual: 128
# >>>>>>>>>>>  PASS <<<<<<<<<<<
#
# ====================================
# ==== Case:49 X = 5    =======
# ====================================
# Exp:  32 Actual:  32
# >>>>>>>>>>>  PASS <<<<<<<<<<<
#
# ** Note: $finish    : ../tb/test_bench.v(36)
#    Time: 450 ns  Iteration: 0  Instance: /test_bench
# End time: 00:11:01 on Mar 31,2025, Elapsed time: 0:00:01
# Errors: 0, Warnings: 1
```


QuestaIntel Starter FPGA Ed...
Wave
Terminal - huugiap@ictc-ed...
31 Thg 3, 00:52
Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/test_bench/X
/test_bench/Y
/test_bench/exp_res
/test_bench/i
-3
32
32
50
Now
450 ns
Cursor 1
364 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns
220 ns
240 ns
260 ns
280 ns
300 ns
320 ns
91 ns to 339 ns

HOMEWORK 2:

```
 1 module alu (
 2  input [7:0] a,
 3  input [7:0] b,
 4  input [2:0] ctrl,
 5
 6  output reg [7:0] y,
 7  output reg carry,
 8  output reg negative,
 9  output reg zero
10 );
11  reg [8:0] result_ext;
12  always @(*) begin
13   y = 8'b0;
14   carry = 1'b0;
15   negative = 1'b0;
16   zero = 1'b0;
17   result_ext = 9'b0;
18
19   case (ctrl)
20    3'b000: begin
21         y = a & b;
22    end
23
24    3'b001: begin
25          y = a | b;
26     end
27
28   3'b010: begin
29        result_ext  = {1'b0, a} + {1'b0, b};
30        y = result_ext[7:0];
31        carry = result_ext[8];
32        negative = y[7];
33      end
34
35   3'b110: begin
36        result_ext  = {1'b0, a} - {1'b0, b};
37        y = result_ext[7:0];
38        carry = result_ext[8];
39        negative = y[7];
40      end
41  default: begin
42          y = 8'b0;
43     end
"alu.v" 56L, 867B
```

```
 43     end
 44 endcase
 45
 46 if (ctrl == 3'b000 || ctrl == 3'b001 || ctrl == 3'b010 || ctrl == 3'b110) begin
 47         if (y == 8'b0) begin
 48                 zero = 1'b1;
 49         end
 50 end
 51
 52 end
 53
 54 endmodule
 55
 56
```

```
huugiap@ictc-eda-ldap-1:~/07_ss07/alu/sim$ make build
vlib work
** Warning: (vlib-34) Library already exists at "work".
Errors: 0, Warnings: 1
vmap work work
Questa Intel Starter FPGA Edition-64 vmap 2023.3 Lib Mapping Utility 2023.07 Jul 17 2023
vmap work work
Modifying modelsim.ini
vlog -f compile.f | tee compile.log
Questa Intel Starter FPGA Edition-64 vlog 2023.3 Compiler 2023.07 Jul 17 2023
Start time: 00:45:38 on Mar 31,2025
vlog -f compile.f
-- Compiling module alu
-- Compiling module test_bench

Top level modules:
        test_bench
End time: 00:45:38 on Mar 31,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
```

```
huugiap@ictc-eda-ldap-1:~/07_ss07/alu/sim$ make run
vsim -debugDB -l test_adder.log -voptargs=+acc -assertdebug -c test_bench -do "log -r /*;run -all;"
Reading pref.tcl

# 2023.3

# vsim -debugDB -l test_adder.log -voptargs="+acc" -assertdebug -c test_bench -do "log -r /*;run -all;"
# Start time: 00:45:41 on Mar 31,2025
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# ** Note: (vsim-8611) Generating debug db.
# ** Warning: (vopt-10587) Some optimizations are turned off because the +acc switch is in effect. This will cause your simulation to run slowly. Please use -access/-debug to maintain needed visibility.
# ** Note: (vsim-12126) Error and warning message counts have been restored: Errors=0, Warnings=1.
# //  Questa Intel Starter FPGA Edition-64
# //  Version 2023.3 linux_x86_64 Jul 17 2023
# //
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# //  5 U.S.C. Section 552. Furthermore, this information
# //  is prohibited from disclosure under the Trade Secrets Act,
# //  18 U.S.C. Section 1905.
# //
# Loading work.test_bench(fast)
# Loading work.alu(fast)
# ** Note: (vsim-8900) Creating design debug database vsim.dbg.
# log -r /*
# run -all
# --------------- Case:   0 ctrl = 010 a =  35, b =  50 --------------
# a + b = 01010101, y = 01010101
# --------------- Case:   1 ctrl = 010 a =  29, b = 184 --------------
# a + b = 11010101, y = 11010101
# --------------- Case:   2 ctrl = 010 a = 192, b = 172 --------------
# a + b = 01101100, y = 01101100
# --------------- Case:   3 ctrl = 101 a =  28, b = 190 --------------
# --------------- Case:   4 ctrl = 001 a = 216, b =  73 --------------
# a | b = 11011001, y = 11011001
```

```
# a | b = 11111110, y = 11111110
# -------------- Case:  13 ctrl = 110 a = 239, b = 227 --------------
# a - b = 00001100, y = 00001100
# -------------- Case:  14 ctrl = 111 a = 216, b =  39 --------------
# -------------- Case:  15 ctrl = 000 a =  73, b = 170 --------------
# a & b = 00001000, y = 00001000
# -------------- Case:  16 ctrl = 101 a = 175, b = 253 --------------
# -------------- Case:  17 ctrl = 110 a = 128, b = 154 --------------
# a - b = 11100110, y = 11100110
# -------------- Case:  18 ctrl = 011 a =  97, b = 230 --------------
# -------------- Case:  19 ctrl = 010 a =  84, b = 239 --------------
# a + b = 01000011, y = 01000011
# -------------- Case:  20 ctrl = 001 a = 186, b =  58 --------------
# a | b = 10111010, y = 10111010
# -------------- Case:  21 ctrl = 111 a = 131, b = 113 --------------
# -------------- Case:  22 ctrl = 000 a =  95, b = 146 --------------
# a & b = 00010010, y = 00010010
# -------------- Case:  23 ctrl = 101 a = 119, b = 138 --------------
# -------------- Case:  24 ctrl = 001 a = 139, b =  55 --------------
# a | b = 10111111, y = 10111111
# -------------- Case:  25 ctrl = 001 a = 176, b = 110 --------------
# a | b = 11111110, y = 11111110
# -------------- Case:  26 ctrl = 111 a =  51, b =  93 --------------
# -------------- Case:  27 ctrl = 101 a =  36, b = 249 --------------
# -------------- Case:  28 ctrl = 101 a =   2, b = 232 --------------
# -------------- Case:  29 ctrl = 000 a =  42, b =  18 --------------
# a & b = 00000010, y = 00000010
# -------------- Case:  30 ctrl = 000 a = 159, b =  45 --------------
# a & b = 00001101, y = 00001101
# -------------- Case:  31 ctrl = 110 a = 123, b = 159 --------------
# a - b = 11011100, y = 11011100
# -------------- Case:  32 ctrl = 101 a = 123, b =  48 --------------
# -------------- Case:  33 ctrl = 011 a = 130, b =  36 --------------
# -------------- Case:  34 ctrl = 001 a = 120, b = 170 --------------
# a | b = 11111010, y = 11111010
# -------------- Case:  35 ctrl = 110 a = 232, b = 199 --------------
# a - b = 00100001, y = 00100001
# -------------- Case:  36 ctrl = 100 a = 130, b = 120 --------------
# -------------- Case:  37 ctrl = 011 a = 161, b = 101 --------------
# -------------- Case:  38 ctrl = 001 a = 200, b =  82 --------------
# a | b = 11011010, y = 11011010
```

```
# --------------- Case:  46 ctrl = 111 a =  58, b = 134 ---------------
# --------------- Case:  47 ctrl = 000 a =  22, b =  28 ---------------
# a & b = 00010100, y = 00010100
# --------------- Case:  48 ctrl = 000 a = 192, b = 132 ---------------
# a & b = 10000000, y = 10000000
# --------------- Case:  49 ctrl = 110 a =  18, b =  14 ---------------
# a - b = 00000100, y = 00000100
# --------------- Case:  50 ctrl = 010 a =  41, b = 185 ---------------
# a + b = 11100010, y = 11100010
# --------------- Case:  51 ctrl = 101 a = 204, b = 233 ---------------
# --------------- Case:  52 ctrl = 000 a = 178, b =  87 ---------------
# a & b = 00010010, y = 00010010
# --------------- Case:  53 ctrl = 111 a = 127, b = 185 ---------------
# --------------- Case:  54 ctrl = 101 a =  68, b = 186 ---------------
# --------------- Case:  55 ctrl = 010 a =  71, b = 139 ---------------
# a + b = 11010010, y = 11010010
# --------------- Case:  56 ctrl = 101 a = 242, b =  39 ---------------
# --------------- Case:  57 ctrl = 110 a = 135, b =  77 ---------------
# a - b = 00111010, y = 00111010
# --------------- Case:  58 ctrl = 001 a = 110, b = 135 ---------------
# a | b = 11101111, y = 11101111
# --------------- Case:  59 ctrl = 110 a = 163, b =  15 ---------------
# a - b = 10010100, y = 10010100
# Negative flag is mismatched
# Exp:0
# Act:1
# ** Note: $finish    : ../tb/test_bench.v(111)
#    Time: 1200 ns  Iteration: 0  Instance: /test_bench
# End time: 00:45:42 on Mar 31,2025, Elapsed time: 0:00:01
# Errors: 0, Warnings: 1
huugiap@ictc-eda-ldap-1:~/07_ss07/alu/sim$
```