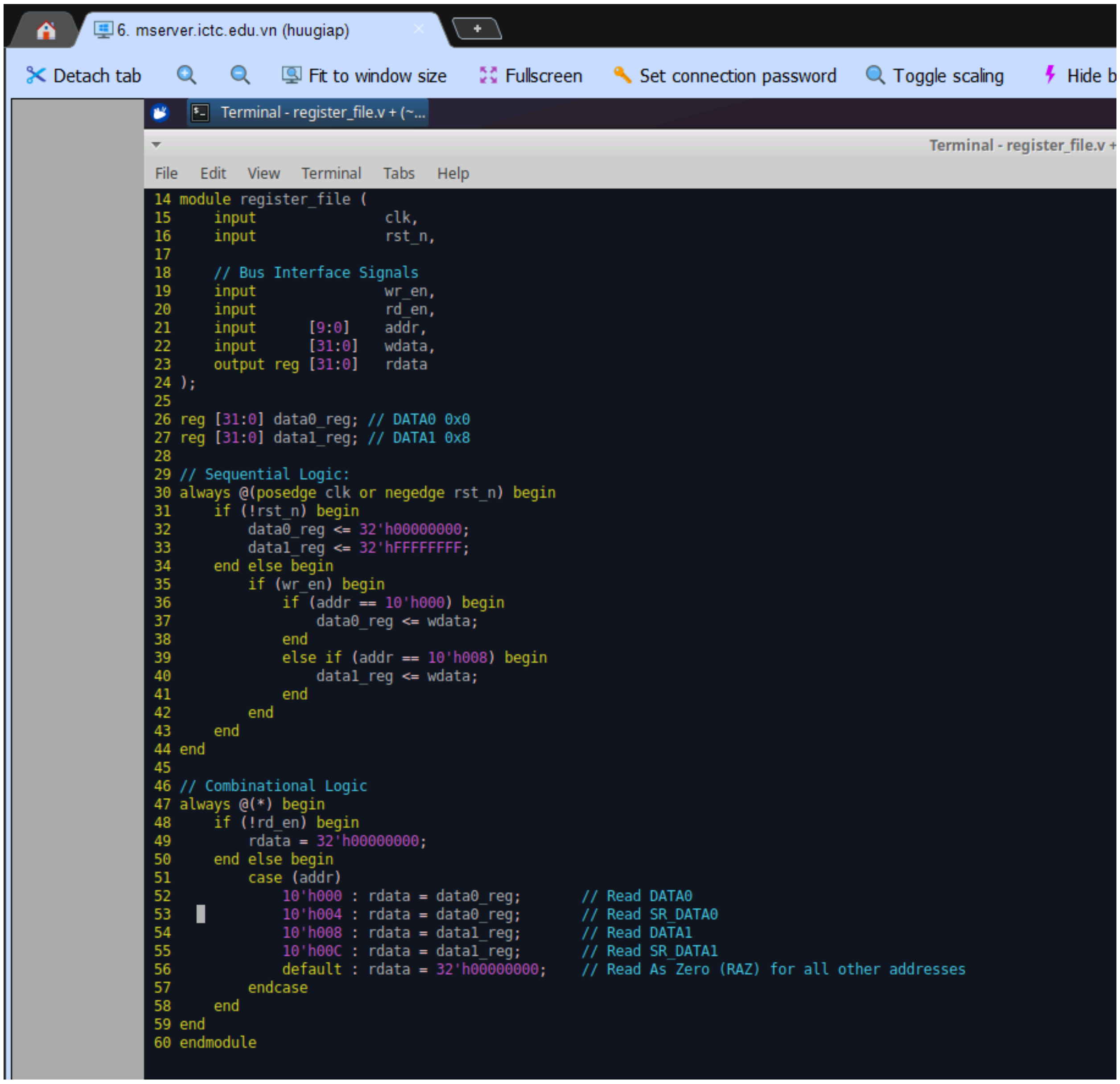
HOMEWORK 1:

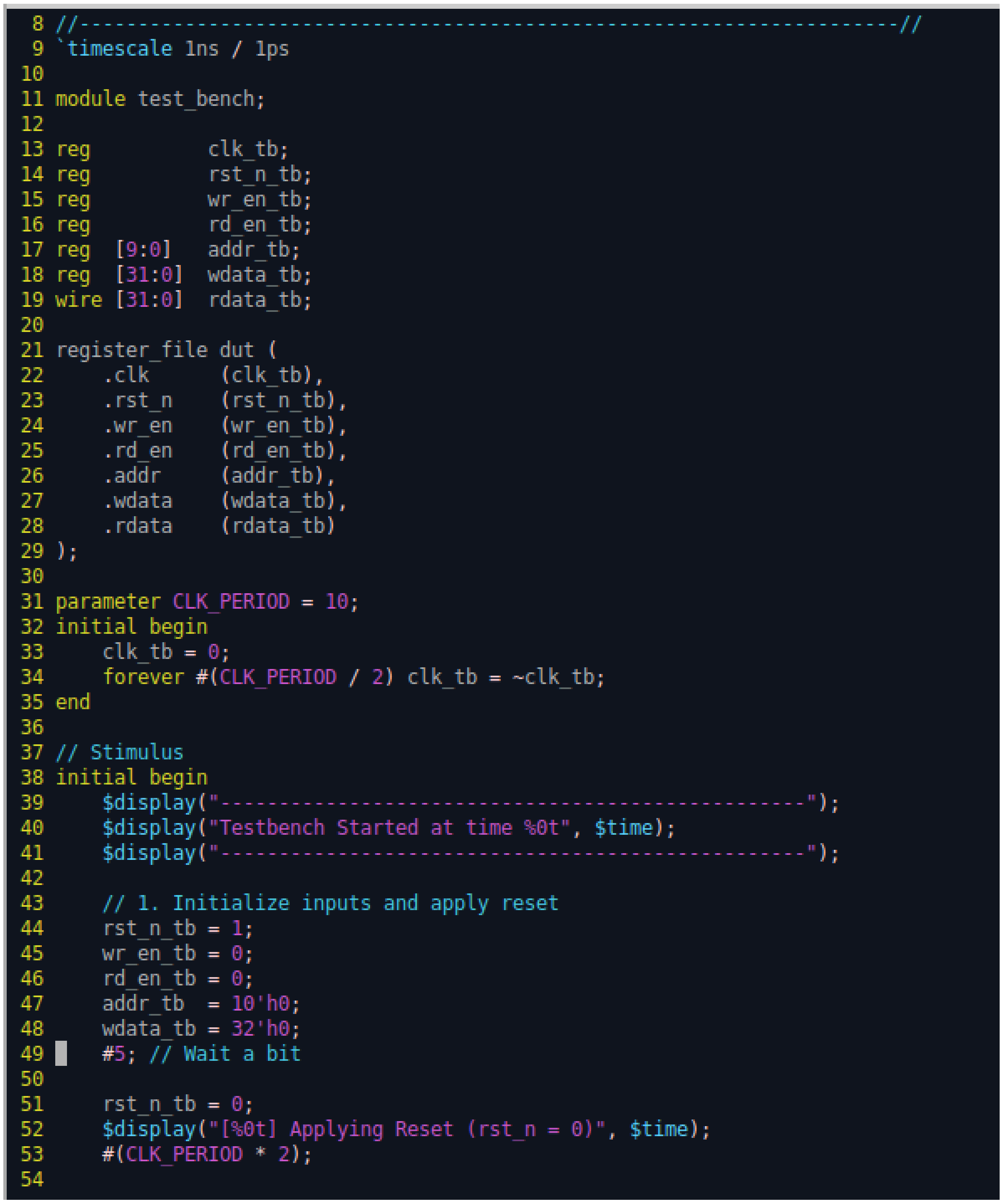
Code RTL:

register_file.v:

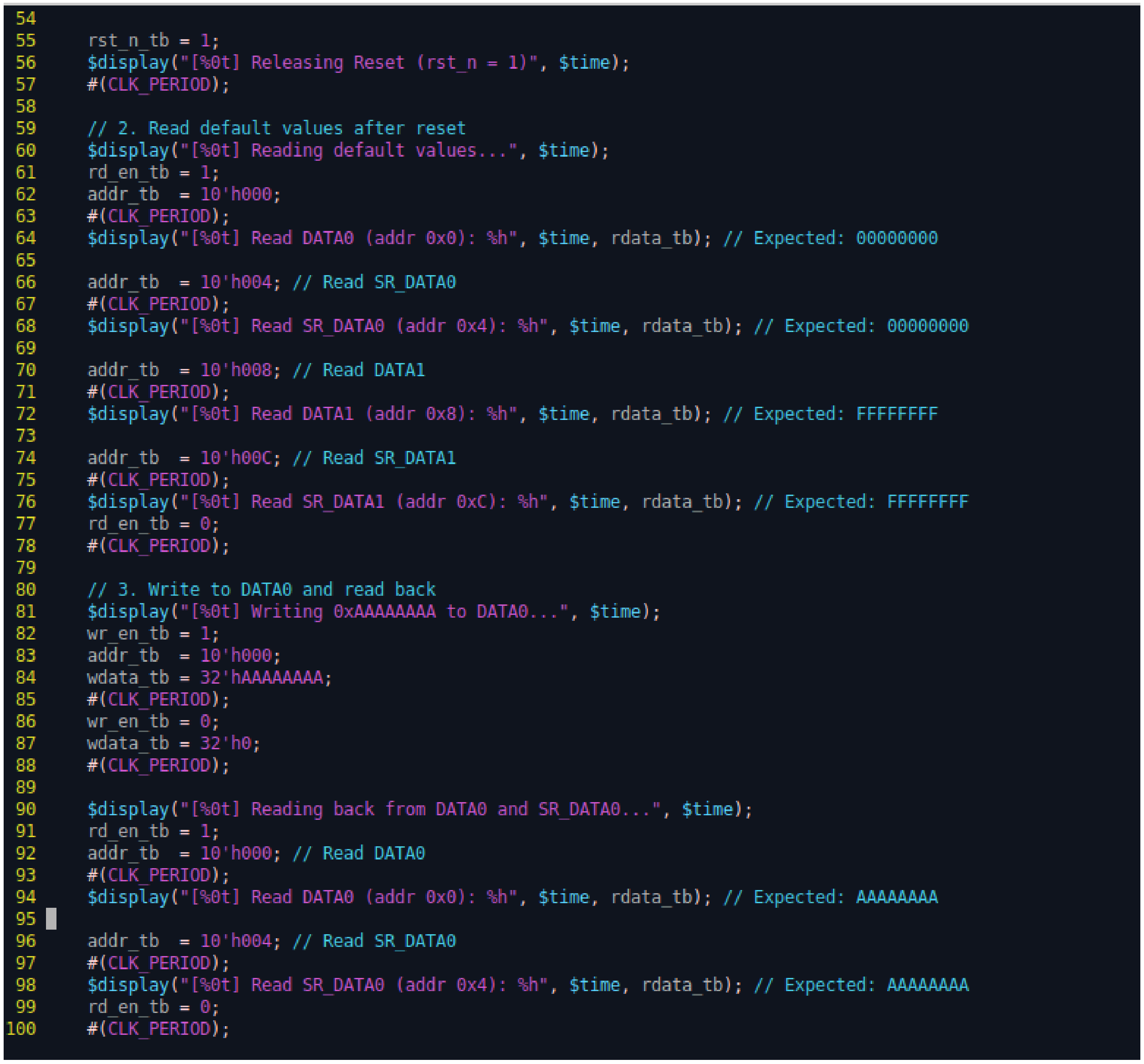

6. mserver.ictc.edu.vn (huugiap)
Detach tab
Fit to window size
Fullscreen
Set connection password
Toggle scaling
Hide b
Terminal - register_file.v + (~...
Terminal - register_file.v +
File Edit View Terminal Tabs Help

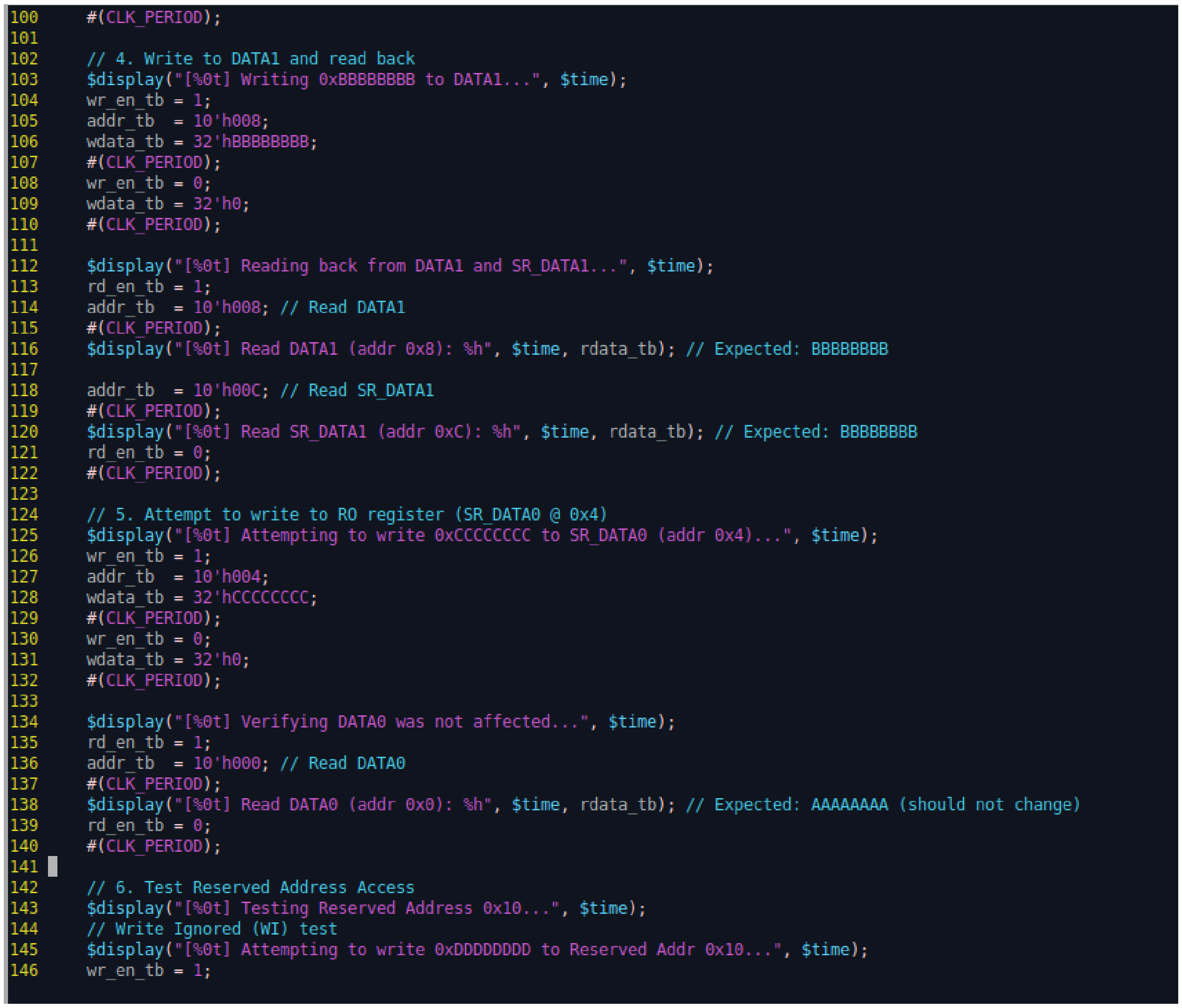
```
module register_file (
    input               clk,
    input               rst_n,

    // Bus Interface Signals
    input               wr_en,
    input               rd_en,
    input       [9:0]   addr,
    input       [31:0]  wdata,
    output reg  [31:0]  rdata
);

reg [31:0] data0_reg; // DATA0 0x0
reg [31:0] data1_reg; // DATA1 0x8

// Sequential Logic:
always @(posedge clk or negedge rst_n) begin
    if (!rst_n) begin
        data0_reg <= 32'h00000000;
        data1_reg <= 32'hFFFFFFFF;
    end else begin
        if (wr_en) begin
            if (addr == 10'h000) begin
                data0_reg <= wdata;
            end
            else if (addr == 10'h008) begin
                data1_reg <= wdata;
            end
        end
    end
end

// Combinational Logic
always @(*) begin
    if (!rd_en) begin
        rdata = 32'h00000000;
    end else begin
        case (addr)
            10'h000 : rdata = data0_reg;        // Read DATA0
            10'h004 : rdata = data0_reg;        // Read SR_DATA0
            10'h008 : rdata = data1_reg;        // Read DATA1
            10'h00C : rdata = data1_reg;        // Read SR_DATA1
            default : rdata = 32'h00000000;     // Read As Zero (RAZ) for all other addresses
        endcase
    end
end
endmodule
```

Code testbench:

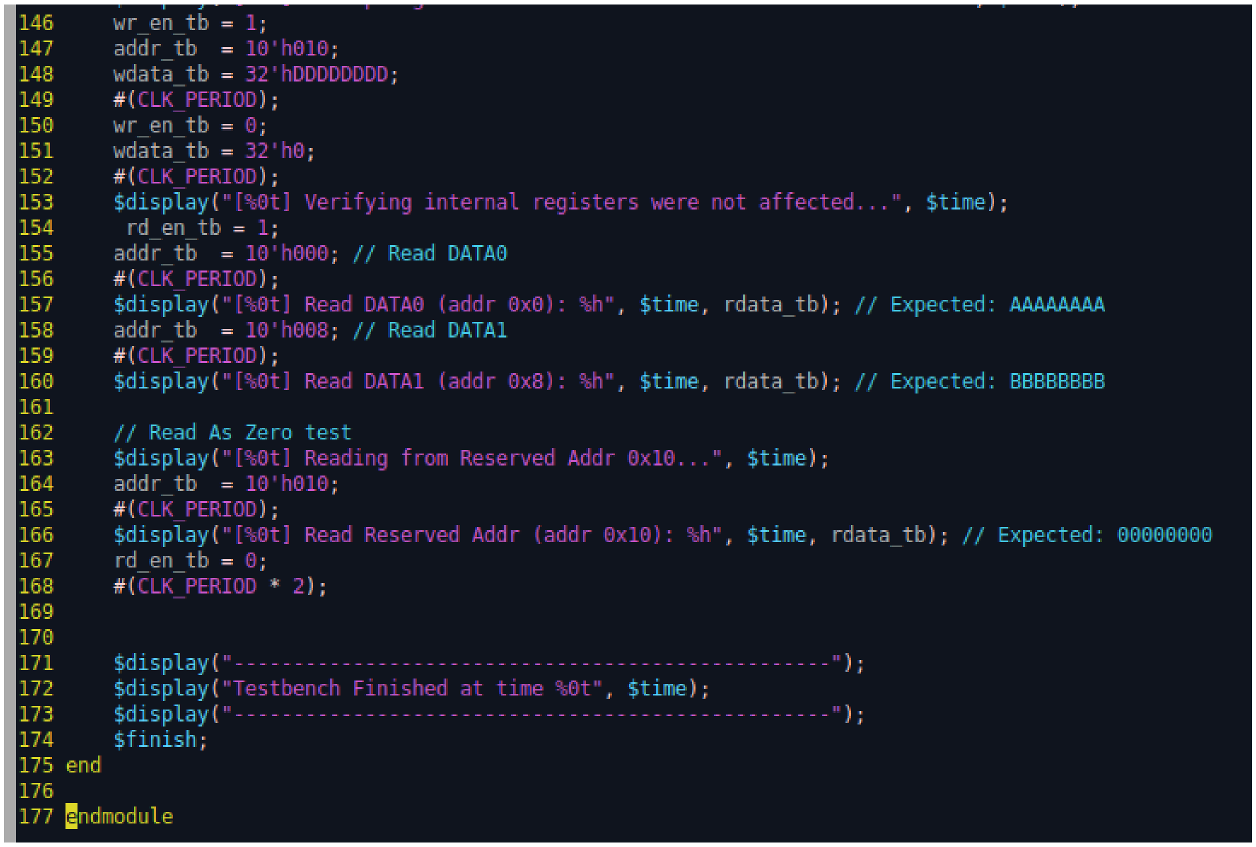


```verilog
//------------------------------------------------------------------------//
`timescale 1ns / 1ps

module test_bench;

reg          clk_tb;
reg          rst_n_tb;
reg          wr_en_tb;
reg          rd_en_tb;
reg  [9:0]   addr_tb;
reg  [31:0]  wdata_tb;
wire [31:0]  rdata_tb;

register_file dut (
    .clk      (clk_tb),
    .rst_n    (rst_n_tb),
    .wr_en    (wr_en_tb),
    .rd_en    (rd_en_tb),
    .addr     (addr_tb),
    .wdata    (wdata_tb),
    .rdata    (rdata_tb)
);

parameter CLK_PERIOD = 10;
initial begin
    clk_tb = 0;
    forever #(CLK_PERIOD / 2) clk_tb = ~clk_tb;
end

// Stimulus
initial begin
    $display("---------------------------------------------------");
    $display("Testbench Started at time %0t", $time);
    $display("---------------------------------------------------");

    // 1. Initialize inputs and apply reset
    rst_n_tb = 1;
    wr_en_tb = 0;
    rd_en_tb = 0;
    addr_tb  = 10'h0;
    wdata_tb = 32'h0;
    #5; // Wait a bit

    rst_n_tb = 0;
    $display("[%0t] Applying Reset (rst_n = 0)", $time);
    #(CLK_PERIOD * 2);

```

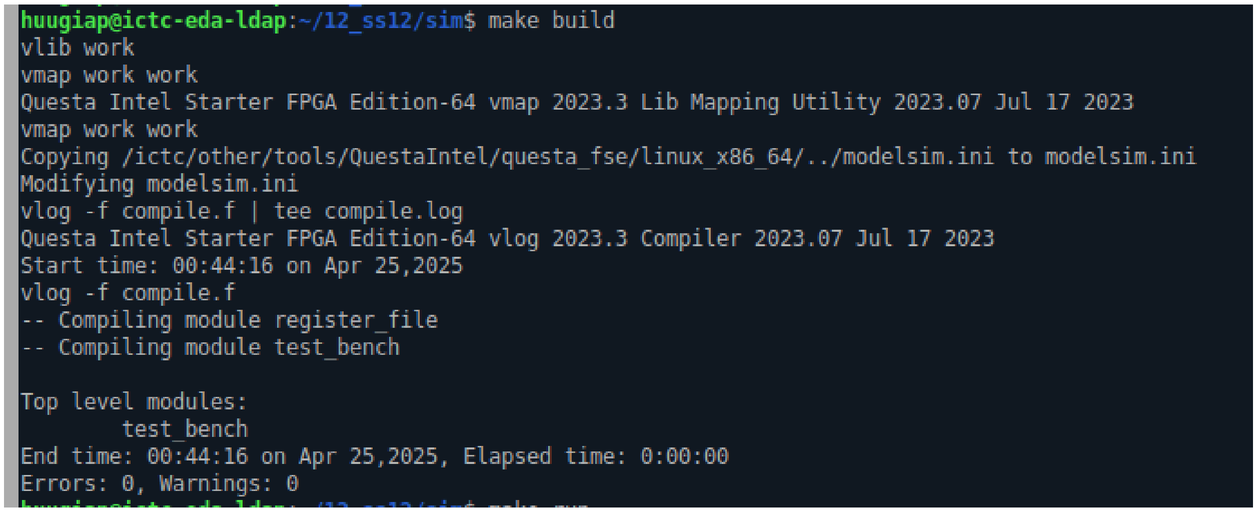

```verilog

    rst_n_tb = 1;
    $display("[%0t] Releasing Reset (rst_n = 1)", $time);
    #(CLK_PERIOD);

    // 2. Read default values after reset
    $display("[%0t] Reading default values...", $time);
    rd_en_tb = 1;
    addr_tb  = 10'h000;
    #(CLK_PERIOD);
    $display("[%0t] Read DATA0 (addr 0x0): %h", $time, rdata_tb); // Expected: 00000000

    addr_tb  = 10'h004; // Read SR_DATA0
    #(CLK_PERIOD);
    $display("[%0t] Read SR_DATA0 (addr 0x4): %h", $time, rdata_tb); // Expected: 00000000

    addr_tb  = 10'h008; // Read DATA1
    #(CLK_PERIOD);
    $display("[%0t] Read DATA1 (addr 0x8): %h", $time, rdata_tb); // Expected: FFFFFFFF

    addr_tb  = 10'h00C; // Read SR_DATA1
    #(CLK_PERIOD);
    $display("[%0t] Read SR_DATA1 (addr 0xC): %h", $time, rdata_tb); // Expected: FFFFFFFF
    rd_en_tb = 0;
    #(CLK_PERIOD);

    // 3. Write to DATA0 and read back
    $display("[%0t] Writing 0xAAAAAAAA to DATA0...", $time);
    wr_en_tb = 1;
    addr_tb  = 10'h000;
    wdata_tb = 32'hAAAAAAAA;
    #(CLK_PERIOD);
    wr_en_tb = 0;
    wdata_tb = 32'h0;
    #(CLK_PERIOD);

    $display("[%0t] Reading back from DATA0 and SR_DATA0...", $time);
    rd_en_tb = 1;
    addr_tb  = 10'h000; // Read DATA0
    #(CLK_PERIOD);
    $display("[%0t] Read DATA0 (addr 0x0): %h", $time, rdata_tb); // Expected: AAAAAAAA

    addr_tb  = 10'h004; // Read SR_DATA0
    #(CLK_PERIOD);
    $display("[%0t] Read SR_DATA0 (addr 0x4): %h", $time, rdata_tb); // Expected: AAAAAAAA
    rd_en_tb = 0;
    #(CLK_PERIOD);
```



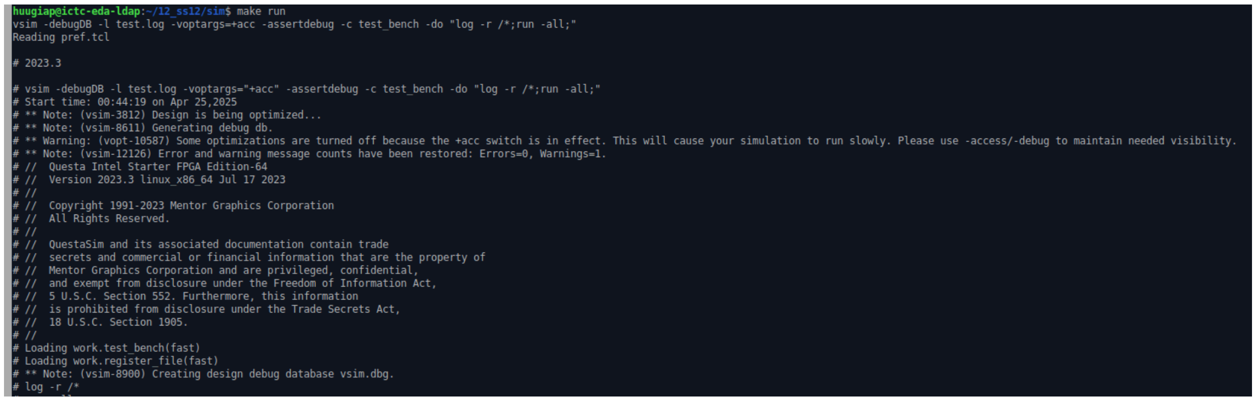
```
    #(CLK_PERIOD);

    // 4. Write to DATA1 and read back
    $display("[%0t] Writing 0xBBBBBBBB to DATA1...", $time);
    wr_en_tb = 1;
    addr_tb  = 10'h008;
    wdata_tb = 32'hBBBBBBBB;
    #(CLK_PERIOD);
    wr_en_tb = 0;
    wdata_tb = 32'h0;
    #(CLK_PERIOD);

    $display("[%0t] Reading back from DATA1 and SR_DATA1...", $time);
    rd_en_tb = 1;
    addr_tb  = 10'h008; // Read DATA1
    #(CLK_PERIOD);
    $display("[%0t] Read DATA1 (addr 0x8): %h", $time, rdata_tb); // Expected: BBBBBBBB

    addr_tb  = 10'h00C; // Read SR_DATA1
    #(CLK_PERIOD);
    $display("[%0t] Read SR_DATA1 (addr 0xC): %h", $time, rdata_tb); // Expected: BBBBBBBB
    rd_en_tb = 0;
    #(CLK_PERIOD);

    // 5. Attempt to write to RO register (SR_DATA0 @ 0x4)
    $display("[%0t] Attempting to write 0xCCCCCCCC to SR_DATA0 (addr 0x4)...", $time);
    wr_en_tb = 1;
    addr_tb  = 10'h004;
    wdata_tb = 32'hCCCCCCCC;
    #(CLK_PERIOD);
    wr_en_tb = 0;
    wdata_tb = 32'h0;
    #(CLK_PERIOD);

    $display("[%0t] Verifying DATA0 was not affected...", $time);
    rd_en_tb = 1;
    addr_tb  = 10'h000; // Read DATA0
    #(CLK_PERIOD);
    $display("[%0t] Read DATA0 (addr 0x0): %h", $time, rdata_tb); // Expected: AAAAAAAA (should not change)
    rd_en_tb = 0;
    #(CLK_PERIOD);

    // 6. Test Reserved Address Access
    $display("[%0t] Testing Reserved Address 0x10...", $time);
    // Write Ignored (WI) test
    $display("[%0t] Attempting to write 0xDDDDDDDD to Reserved Addr 0x10...", $time);
    wr_en_tb = 1;
```



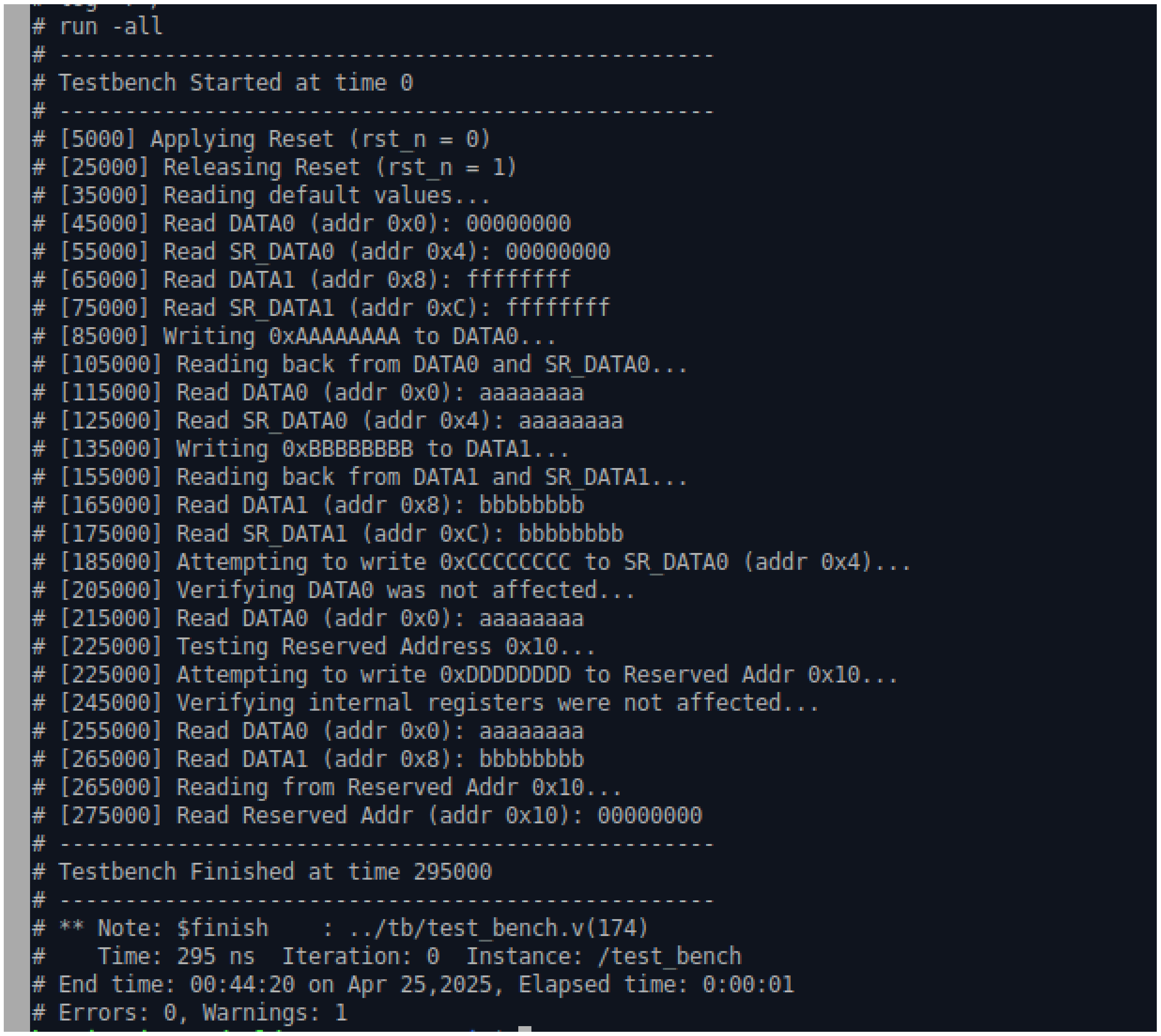
```
    wr_en_tb = 1;
    addr_tb  = 10'h010;
    wdata_tb = 32'hDDDDDDDD;
    #(CLK_PERIOD);
    wr_en_tb = 0;
    wdata_tb = 32'h0;
    #(CLK_PERIOD);
    $display("[%0t] Verifying internal registers were not affected...", $time);
     rd_en_tb = 1;
    addr_tb  = 10'h000; // Read DATA0
    #(CLK_PERIOD);
    $display("[%0t] Read DATA0 (addr 0x0): %h", $time, rdata_tb); // Expected: AAAAAAAA
    addr_tb  = 10'h008; // Read DATA1
    #(CLK_PERIOD);
    $display("[%0t] Read DATA1 (addr 0x8): %h", $time, rdata_tb); // Expected: BBBBBBBB

    // Read As Zero test
    $display("[%0t] Reading from Reserved Addr 0x10...", $time);
    addr_tb  = 10'h010;
    #(CLK_PERIOD);
    $display("[%0t] Read Reserved Addr (addr 0x10): %h", $time, rdata_tb); // Expected: 00000000
    rd_en_tb = 0;
    #(CLK_PERIOD * 2);


    $display("--------------------------------------------------");
    $display("Testbench Finished at time %0t", $time);
    $display("--------------------------------------------------");
    $finish;
end

endmodule
```



```
huugiap@ictc-eda-ldap:~/12_ss12/sim$ make build
vlib work
vmap work work
Questa Intel Starter FPGA Edition-64 vmap 2023.3 Lib Mapping Utility 2023.07 Jul 17 2023
vmap work work
Copying /ictc/other/tools/QuestaIntel/questa_fse/linux_x86_64/../modelsim.ini to modelsim.ini
Modifying modelsim.ini
vlog -f compile.f | tee compile.log
Questa Intel Starter FPGA Edition-64 vlog 2023.3 Compiler 2023.07 Jul 17 2023
Start time: 00:44:16 on Apr 25,2025
vlog -f compile.f
-- Compiling module register_file
-- Compiling module test_bench

Top level modules:
        test_bench
End time: 00:44:16 on Apr 25,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
```



```
huugiap@ictc-eda-ldap:~/12_ss12/sim$ make run
vsim -debugDB -l test.log -voptargs=+acc -assertdebug -c test_bench -do "log -r /*;run -all;"
Reading pref.tcl

# 2023.3

# vsim -debugDB -l test.log -voptargs="+acc" -assertdebug -c test_bench -do "log -r /*;run -all;"
# Start time: 00:44:19 on Apr 25,2025
# ** Note: (vsim-3812) Design is being optimized...
# ** Note: (vsim-8611) Generating debug db.
# ** Warning: (vopt-10587) Some optimizations are turned off because the +acc switch is in effect. This will cause your simulation to run slowly. Please use -access/-debug to maintain needed visibility.
# ** Note: (vsim-12126) Error and warning message counts have been restored: Errors=0, Warnings=1.
# //  Questa Intel Starter FPGA Edition-64
# //  Version 2023.3 linux_x86_64 Jul 17 2023
# //
# //  Copyright 1991-2023 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  QuestaSim and its associated documentation contain trade
# //  secrets and commercial or financial information that are the property of
# //  Mentor Graphics Corporation and are privileged, confidential,
# //  and exempt from disclosure under the Freedom of Information Act,
# //  5 U.S.C. Section 552. Furthermore, this information
# //  is prohibited from disclosure under the Trade Secrets Act,
# //  18 U.S.C. Section 1905.
# //
# Loading work.test_bench(fast)
# Loading work.register_file(fast)
# ** Note: (vsim-8900) Creating design debug database vsim.dbg.
# log -r /*
```

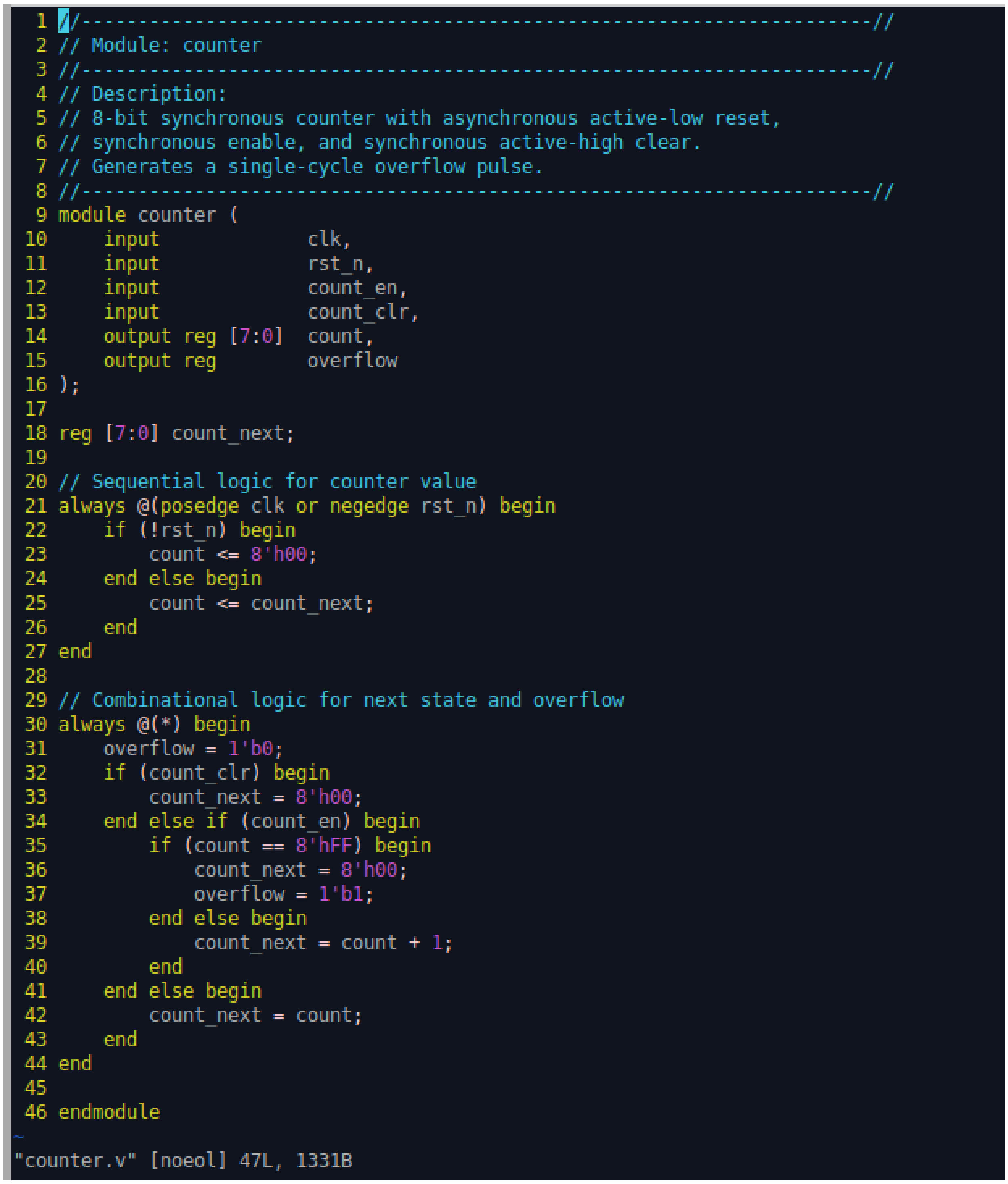


```
# run -all
# --------------------------------------------------
# Testbench Started at time 0
# --------------------------------------------------
# [5000] Applying Reset (rst_n = 0)
# [25000] Releasing Reset (rst_n = 1)
# [35000] Reading default values...
# [45000] Read DATA0 (addr 0x0): 00000000
# [55000] Read SR_DATA0 (addr 0x4): 00000000
# [65000] Read DATA1 (addr 0x8): ffffffff
# [75000] Read SR_DATA1 (addr 0xC): ffffffff
# [85000] Writing 0xAAAAAAAA to DATA0...
# [105000] Reading back from DATA0 and SR_DATA0...
# [115000] Read DATA0 (addr 0x0): aaaaaaaa
# [125000] Read SR_DATA0 (addr 0x4): aaaaaaaa
# [135000] Writing 0xBBBBBBBB to DATA1...
# [155000] Reading back from DATA1 and SR_DATA1...
# [165000] Read DATA1 (addr 0x8): bbbbbbbb
# [175000] Read SR_DATA1 (addr 0xC): bbbbbbbb
# [185000] Attempting to write 0xCCCCCCCC to SR_DATA0 (addr 0x4)...
# [205000] Verifying DATA0 was not affected...
# [215000] Read DATA0 (addr 0x0): aaaaaaaa
# [225000] Testing Reserved Address 0x10...
# [225000] Attempting to write 0xDDDDDDDD to Reserved Addr 0x10...
# [245000] Verifying internal registers were not affected...
# [255000] Read DATA0 (addr 0x0): aaaaaaaa
# [265000] Read DATA1 (addr 0x8): bbbbbbbb
# [265000] Reading from Reserved Addr 0x10...
# [275000] Read Reserved Addr (addr 0x10): 00000000
# --------------------------------------------------
# Testbench Finished at time 295000
# --------------------------------------------------
# ** Note: $finish    : ../tb/test_bench.v(174)
#    Time: 295 ns  Iteration: 0  Instance: /test_bench
# End time: 00:44:20 on Apr 25,2025, Elapsed time: 0:00:01
# Errors: 0, Warnings: 1
```

HOMEWORK 2:

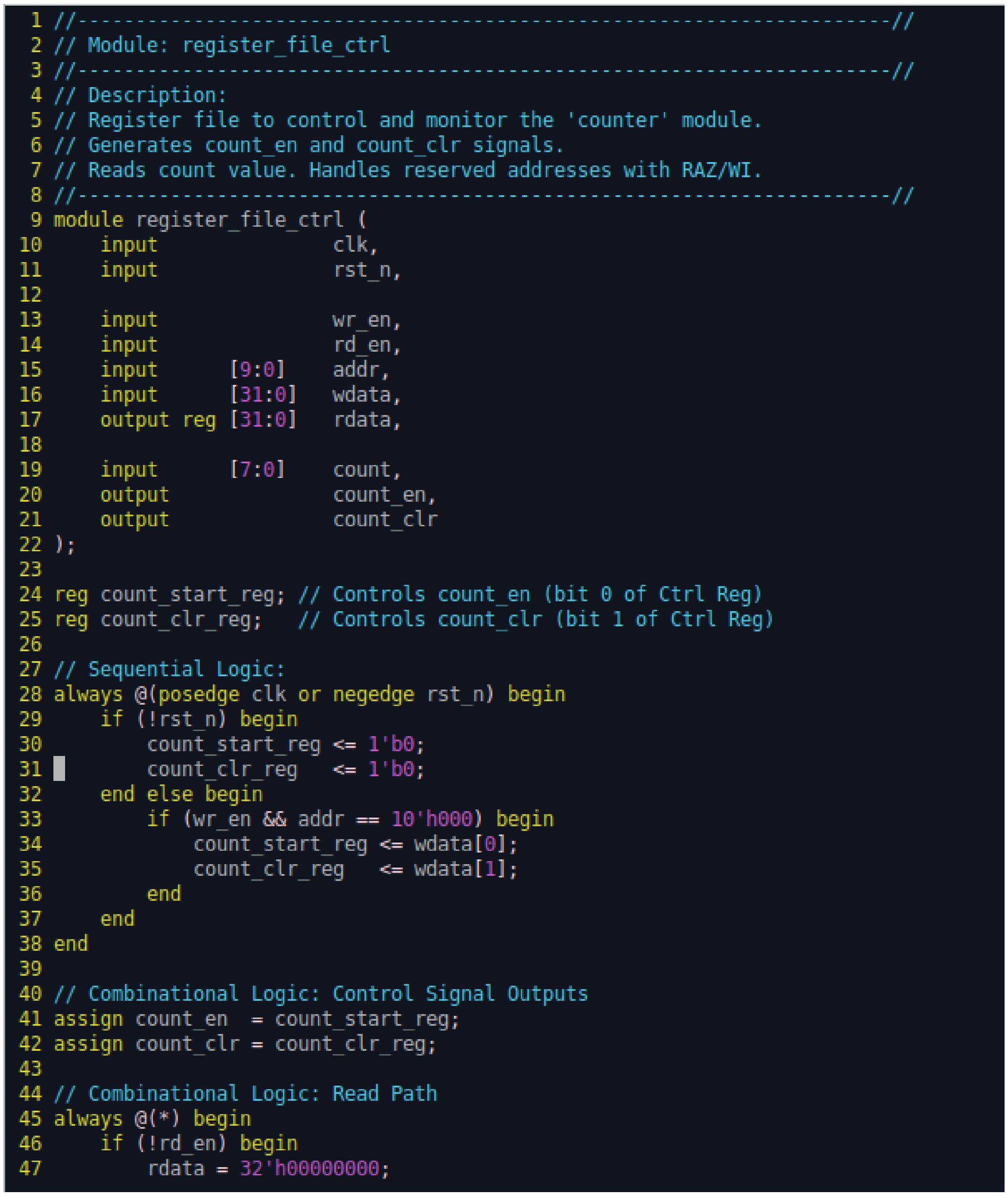
Code RTL:

- **counter.v:**

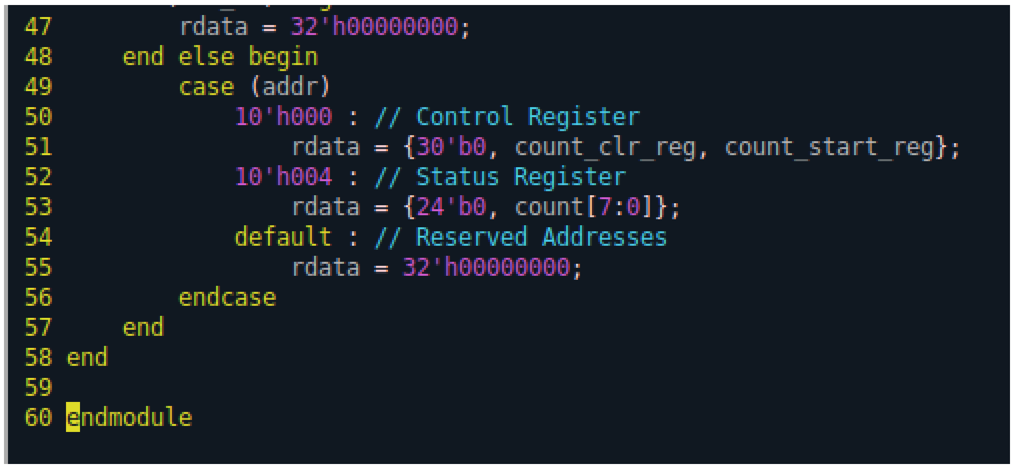


```
//------------------------------------------------------------------------//
// Module: counter
//------------------------------------------------------------------------//
// Description:
// 8-bit synchronous counter with asynchronous active-low reset,
// synchronous enable, and synchronous active-high clear.
// Generates a single-cycle overflow pulse.
//------------------------------------------------------------------------//
module counter (
    input               clk,
    input               rst_n,
    input               count_en,
    input               count_clr,
    output reg [7:0]    count,
    output reg          overflow
);

reg [7:0] count_next;

// Sequential logic for counter value
always @(posedge clk or negedge rst_n) begin
    if (!rst_n) begin
        count <= 8'h00;
    end else begin
        count <= count_next;
    end
end

// Combinational logic for next state and overflow
always @(*) begin
    overflow = 1'b0;
    if (count_clr) begin
        count_next = 8'h00;
    end else if (count_en) begin
        if (count == 8'hFF) begin
            count_next = 8'h00;
            overflow = 1'b1;
        end else begin
            count_next = count + 1;
        end
    end else begin
        count_next = count;
    end
end

endmodule
~
"counter.v" [noeol] 47L, 1331B
```

- **register_file_ctrl.v:**



```verilog
//-----------------------------------------------------------------------//
// Module: register_file_ctrl
//-----------------------------------------------------------------------//
// Description:
// Register file to control and monitor the 'counter' module.
// Generates count_en and count_clr signals.
// Reads count value. Handles reserved addresses with RAZ/WI.
//-----------------------------------------------------------------------//
module register_file_ctrl (
    input                   clk,
    input                   rst_n,

    input                   wr_en,
    input                   rd_en,
    input       [9:0]       addr,
    input       [31:0]      wdata,
    output reg  [31:0]      rdata,

    input       [7:0]       count,
    output                  count_en,
    output                  count_clr
);

reg count_start_reg; // Controls count_en (bit 0 of Ctrl Reg)
reg count_clr_reg;   // Controls count_clr (bit 1 of Ctrl Reg)

// Sequential Logic:
always @(posedge clk or negedge rst_n) begin
    if (!rst_n) begin
        count_start_reg <= 1'b0;
        count_clr_reg   <= 1'b0;
    end else begin
        if (wr_en && addr == 10'h000) begin
            count_start_reg <= wdata[0];
            count_clr_reg   <= wdata[1];
        end
    end
end

// Combinational Logic: Control Signal Outputs
assign count_en  = count_start_reg;
assign count_clr = count_clr_reg;

// Combinational Logic: Read Path
always @(*) begin
    if (!rd_en) begin
        rdata = 32'h00000000;
```

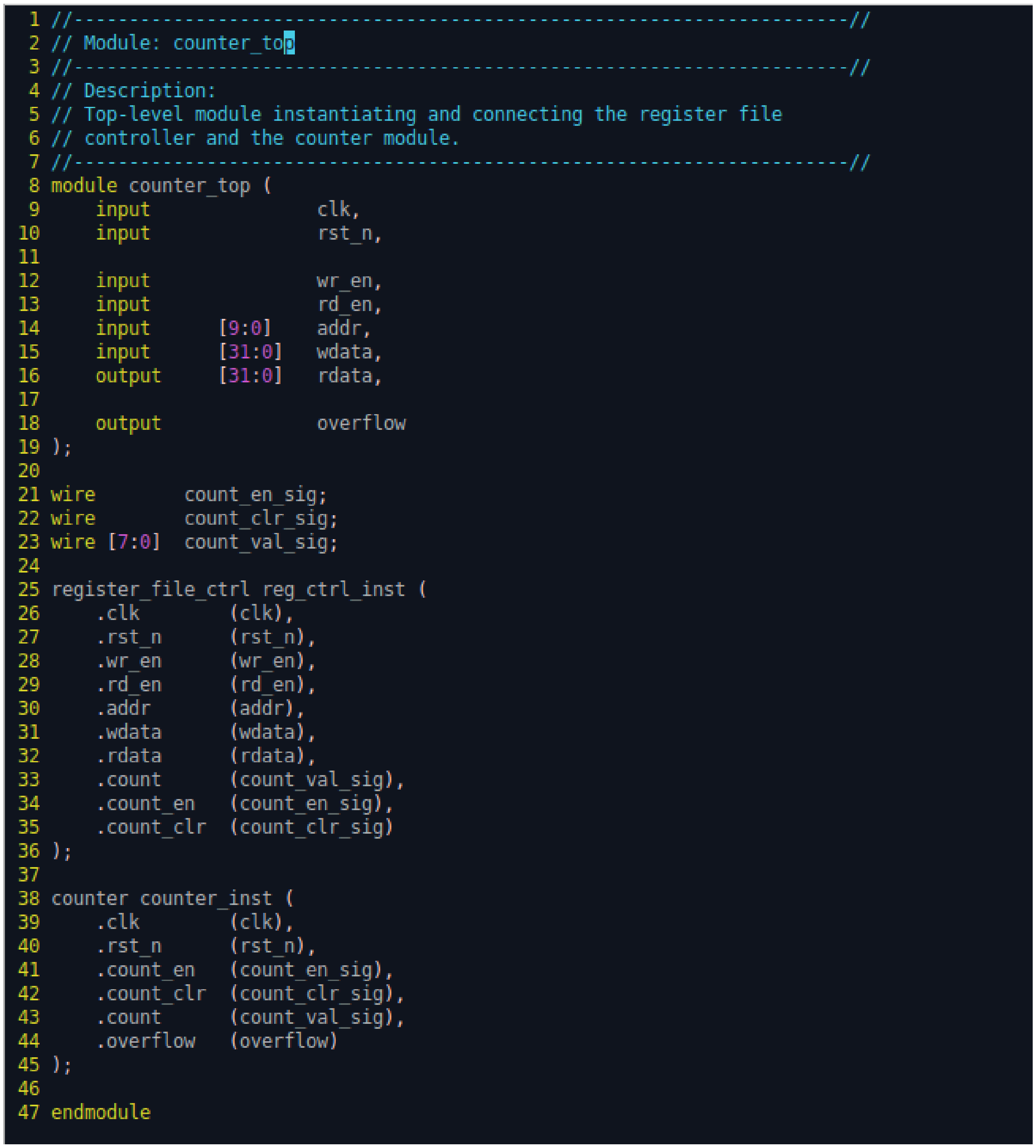


```verilog
        rdata = 32'h00000000;
```

```verilog
    end else begin
        case (addr)
            10'h000 : // Control Register
                rdata = {30'b0, count_clr_reg, count_start_reg};
            10'h004 : // Status Register
                rdata = {24'b0, count[7:0]};
            default : // Reserved Addresses
                rdata = 32'h00000000;
        endcase
    end
end

endmodule
```

- **counter_top.v:**



```
//--------------------------------------------------------------------------//
// Module: counter_top
//--------------------------------------------------------------------------//
// Description:
// Top-level module instantiating and connecting the register file
// controller and the counter module.
//--------------------------------------------------------------------------//
module counter_top (
    input                   clk,
    input                   rst_n,

    input                   wr_en,
    input                   rd_en,
    input         [9:0]     addr,
    input         [31:0]    wdata,
    output        [31:0]    rdata,

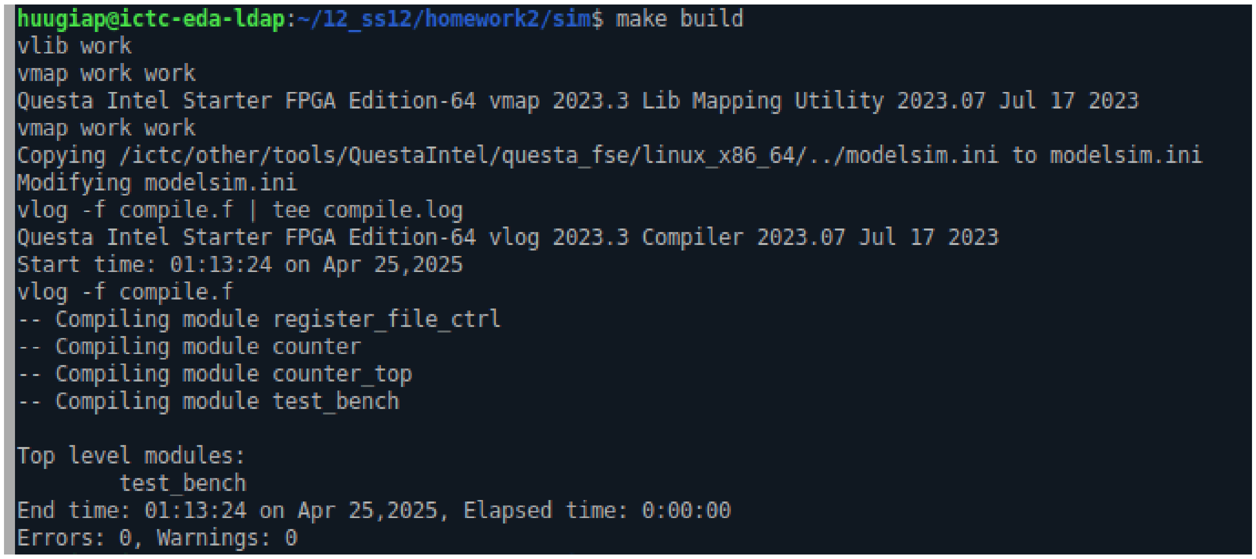
    output                  overflow
);

wire         count_en_sig;
wire         count_clr_sig;
wire [7:0]   count_val_sig;

register_file_ctrl reg_ctrl_inst (
    .clk         (clk),
    .rst_n       (rst_n),
    .wr_en       (wr_en),
    .rd_en       (rd_en),
    .addr        (addr),
    .wdata       (wdata),
    .rdata       (rdata),
    .count       (count_val_sig),
    .count_en    (count_en_sig),
    .count_clr   (count_clr_sig)
);

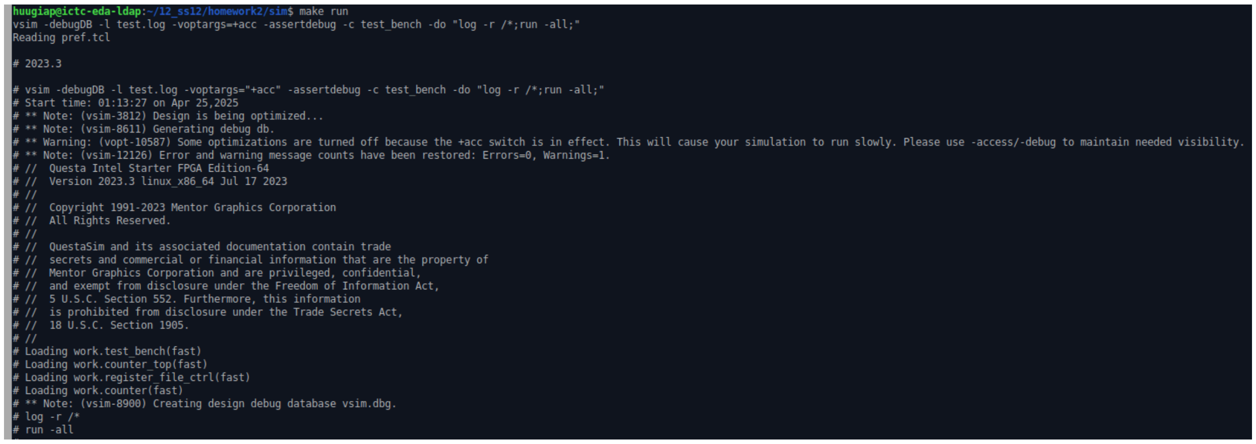
counter counter_inst (
    .clk         (clk),
    .rst_n       (rst_n),
    .count_en    (count_en_sig),
    .count_clr   (count_clr_sig),
    .count       (count_val_sig),
    .overflow    (overflow)
);

endmodule
```



```
huugiap@ictc-eda-ldap:~/12_ss12/homework2/sim$ make build
vlib work
vmap work work
Questa Intel Starter FPGA Edition-64 vmap 2023.3 Lib Mapping Utility 2023.07 Jul 17 2023
vmap work work
Copying /ictc/other/tools/QuestaIntel/questa_fse/linux_x86_64/../modelsim.ini to modelsim.ini
Modifying modelsim.ini
vlog -f compile.f | tee compile.log
Questa Intel Starter FPGA Edition-64 vlog 2023.3 Compiler 2023.07 Jul 17 2023
Start time: 01:13:24 on Apr 25,2025
vlog -f compile.f
-- Compiling module register_file_ctrl
-- Compiling module counter
-- Compiling module counter_top
-- Compiling module test_bench

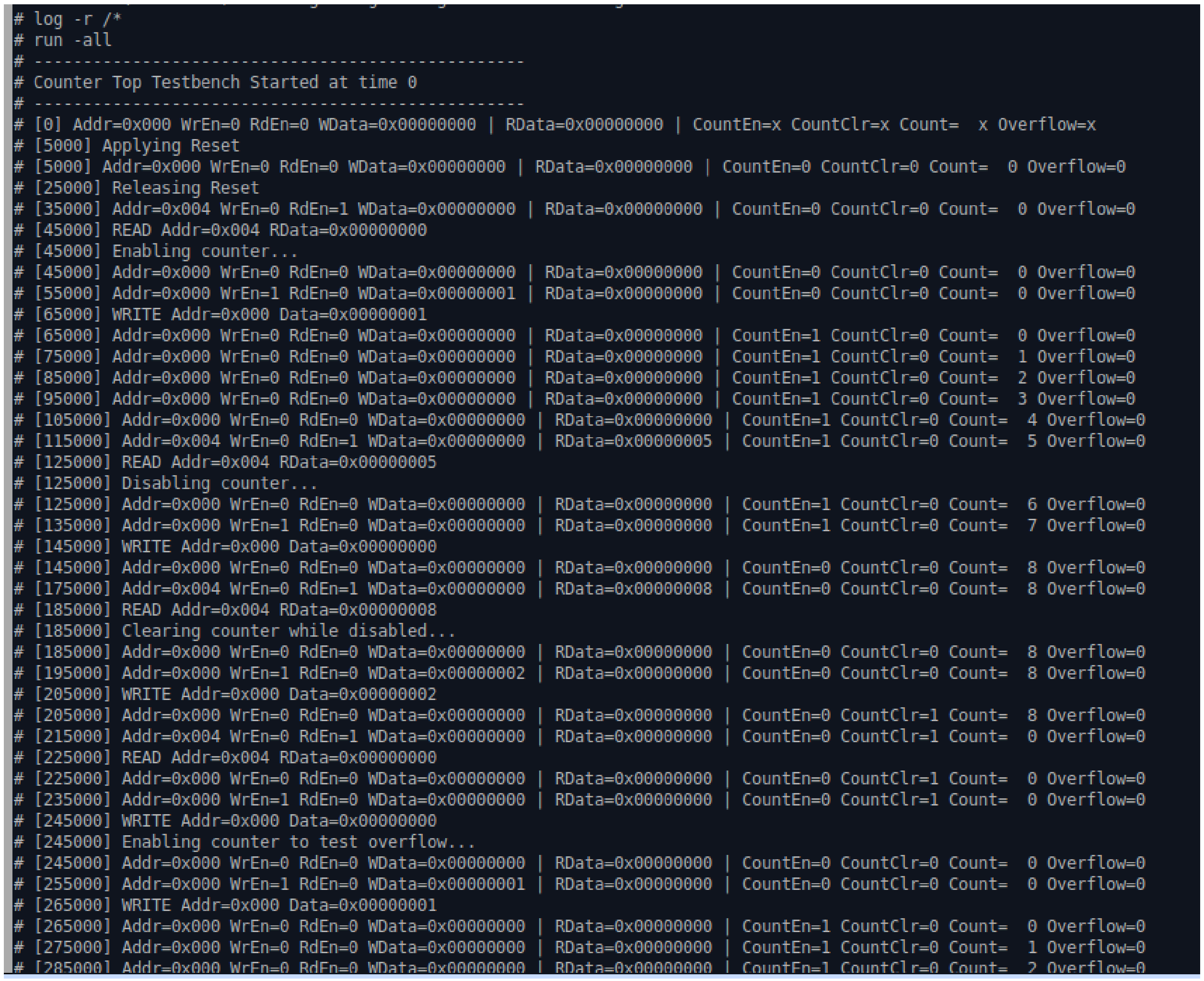
Top level modules:
        test_bench
End time: 01:13:24 on Apr 25,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
```



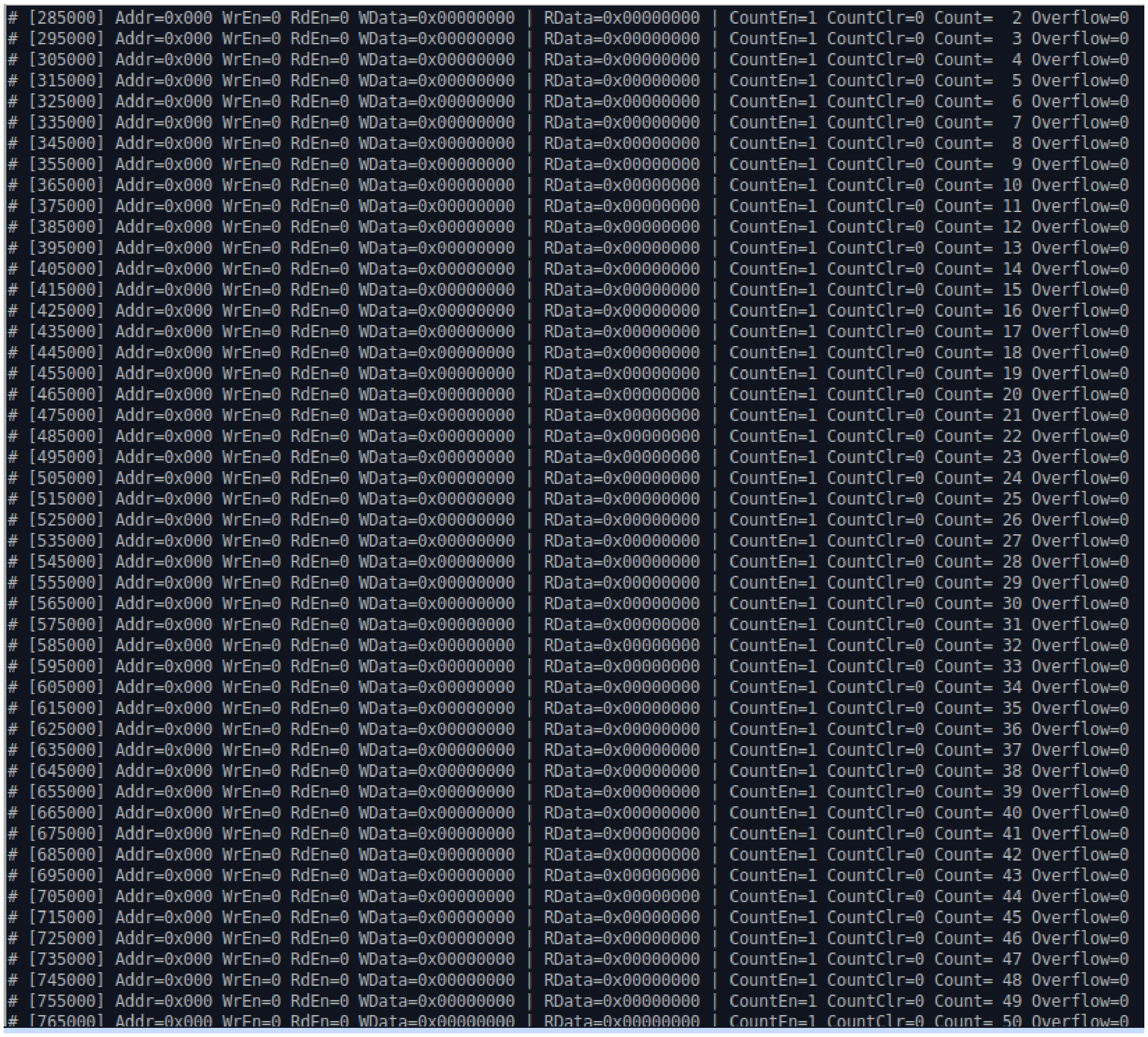
```
huugiap@ictc-eda-ldap:~/12_ss12/homework2/sim$ make run
vsim -debugDB -l test.log -voptargs=+acc -assertdebug -c test_bench -do "log -r /*;run -all;"
Reading pref.tcl

# 2023.3

# vsim -debugDB -l test.log -voptargs="+acc" -assertdebug -c test_bench -do "log -r /*;run -all;"
# Start time: 01:13:27 on Apr 25,2025
# ** Note: (vsim-3812) Design is being optimized...
# ** Note: (vsim-8611) Generating debug db.
# ** Warning: (vopt-10587) Some optimizations are turned off because the +acc switch is in effect. This will cause your simulation to run slowly. Please use -access/-debug to maintain needed visibility.
# ** Note: (vsim-12126) Error and warning message counts have been restored: Errors=0, Warnings=1.
# //  Questa Intel Starter FPGA Edition-64
# //  Version 2023.3 linux_x86_64 Jul 17 2023
# //
# //  Copyright 1991-2023 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  QuestaSim and its associated documentation contain trade
# //  secrets and commercial or financial information that are the property of
# //  Mentor Graphics Corporation and are privileged, confidential,
# //  and exempt from disclosure under the Freedom of Information Act,
# //  5 U.S.C. Section 552. Furthermore, this information
# //  is prohibited from disclosure under the Trade Secrets Act,
# //  18 U.S.C. Section 1905.
# //
# Loading work.test_bench(fast)
# Loading work.counter_top(fast)
# Loading work.register_file_ctrl(fast)
# Loading work.counter(fast)
# ** Note: (vsim-8900) Creating design debug database vsim.dbg.
# log -r /*
# run -all
```



```
# log -r /*
# run -all
# -------------------------------------------------
# Counter Top Testbench Started at time 0
# -------------------------------------------------
# [0] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=x CountClr=x Count=  x Overflow=x
# [5000] Applying Reset
# [5000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  0 Overflow=0
# [25000] Releasing Reset
# [35000] Addr=0x004 WrEn=0 RdEn=1 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  0 Overflow=0
# [45000] READ Addr=0x004 RData=0x00000000
# [45000] Enabling counter...
# [45000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  0 Overflow=0
# [55000] Addr=0x000 WrEn=1 RdEn=0 WData=0x00000001 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  0 Overflow=0
# [65000] WRITE Addr=0x000 Data=0x00000001
# [65000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  0 Overflow=0
# [75000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  1 Overflow=0
# [85000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  2 Overflow=0
# [95000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  3 Overflow=0
# [105000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  4 Overflow=0
# [115000] Addr=0x004 WrEn=0 RdEn=1 WData=0x00000000 | RData=0x00000005 | CountEn=1 CountClr=0 Count=  5 Overflow=0
# [125000] READ Addr=0x004 RData=0x00000005
# [125000] Disabling counter...
# [125000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  6 Overflow=0
# [135000] Addr=0x000 WrEn=1 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  7 Overflow=0
# [145000] WRITE Addr=0x000 Data=0x00000000
# [145000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  8 Overflow=0
# [175000] Addr=0x004 WrEn=0 RdEn=1 WData=0x00000000 | RData=0x00000008 | CountEn=0 CountClr=0 Count=  8 Overflow=0
# [185000] READ Addr=0x004 RData=0x00000008
# [185000] Clearing counter while disabled...
# [185000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  8 Overflow=0
# [195000] Addr=0x000 WrEn=1 RdEn=0 WData=0x00000002 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  8 Overflow=0
# [205000] WRITE Addr=0x000 Data=0x00000002
# [205000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=1 Count=  8 Overflow=0
# [215000] Addr=0x004 WrEn=0 RdEn=1 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=1 Count=  0 Overflow=0
# [225000] READ Addr=0x004 RData=0x00000000
# [225000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=1 Count=  0 Overflow=0
# [235000] Addr=0x000 WrEn=1 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=1 Count=  0 Overflow=0
# [245000] WRITE Addr=0x000 Data=0x00000000
# [245000] Enabling counter to test overflow...
# [245000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  0 Overflow=0
# [255000] Addr=0x000 WrEn=1 RdEn=0 WData=0x00000001 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  0 Overflow=0
# [265000] WRITE Addr=0x000 Data=0x00000001
# [265000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  0 Overflow=0
# [275000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  1 Overflow=0
# [285000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  2 Overflow=0
```



```
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# [295000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  3 Overflow=0
# [305000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  4 Overflow=0
# [315000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  5 Overflow=0
# [325000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  6 Overflow=0
# [335000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  7 Overflow=0
# [345000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  8 Overflow=0
# [355000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  9 Overflow=0
# [365000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 10 Overflow=0
# [375000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 11 Overflow=0
# [385000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 12 Overflow=0
# [395000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 13 Overflow=0
# [405000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 14 Overflow=0
# [415000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 15 Overflow=0
# [425000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 16 Overflow=0
# [435000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 17 Overflow=0
# [445000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 18 Overflow=0
# [455000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 19 Overflow=0
# [465000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 20 Overflow=0
# [475000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 21 Overflow=0
# [485000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 22 Overflow=0
# [495000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 23 Overflow=0
# [505000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 24 Overflow=0
# [515000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 25 Overflow=0
# [525000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 26 Overflow=0
# [535000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 27 Overflow=0
# [545000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 28 Overflow=0
# [555000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 29 Overflow=0
# [565000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 30 Overflow=0
# [575000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 31 Overflow=0
# [585000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 32 Overflow=0
# [595000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 33 Overflow=0
# [605000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 34 Overflow=0
# [615000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 35 Overflow=0
# [625000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 36 Overflow=0
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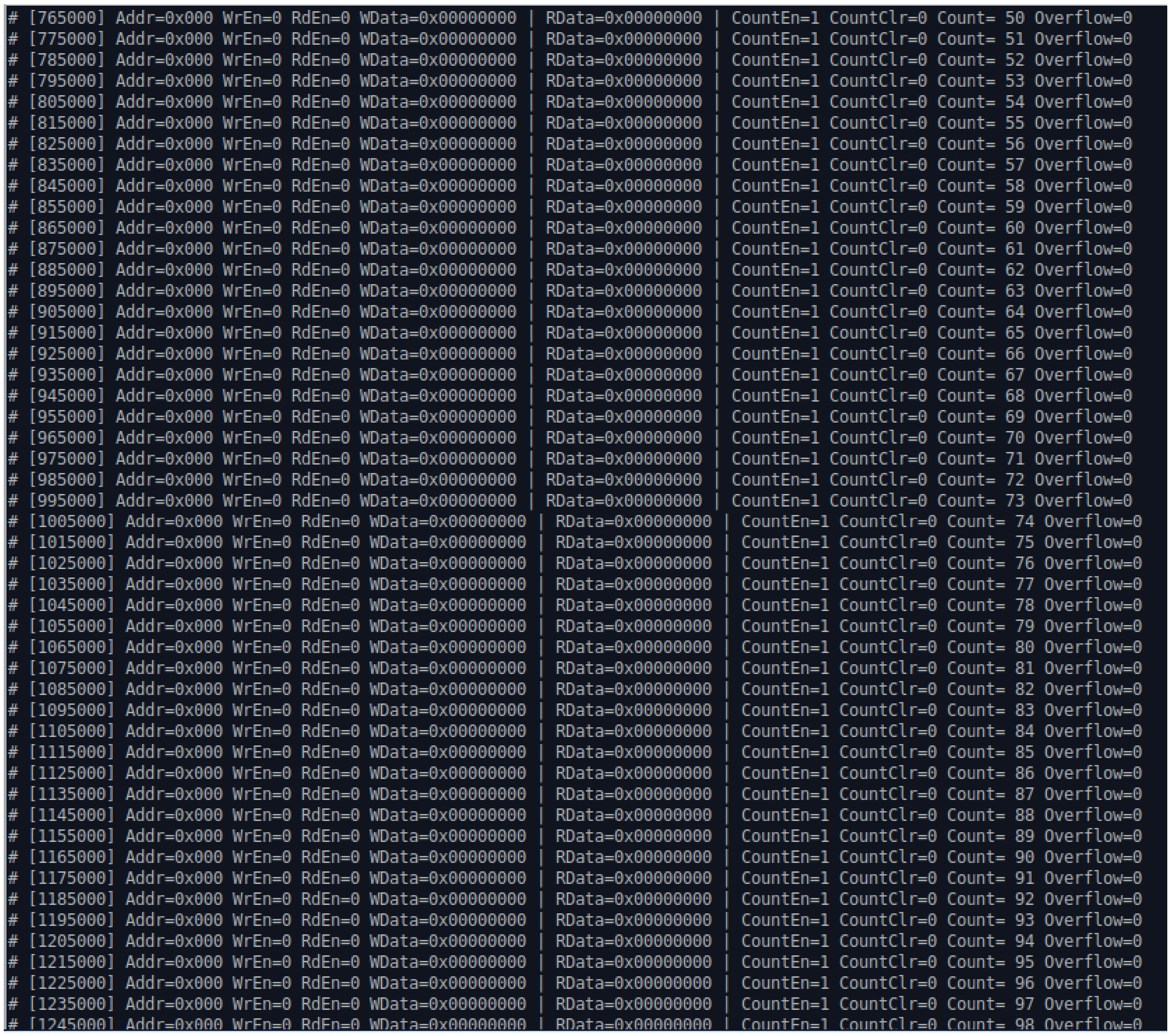
# [655000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 39 Overflow=0
# [665000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 40 Overflow=0
# [675000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 41 Overflow=0
# [685000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 42 Overflow=0
# [695000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 43 Overflow=0
# [705000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 44 Overflow=0
# [715000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 45 Overflow=0
# [725000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 46 Overflow=0
# [735000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 47 Overflow=0
# [745000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 48 Overflow=0
# [755000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 49 Overflow=0
# [765000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 50 Overflow=0
```



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# [775000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 51 Overflow=0
# [785000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 52 Overflow=0
# [795000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 53 Overflow=0
# [805000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 54 Overflow=0
# [815000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 55 Overflow=0
# [825000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 56 Overflow=0
# [835000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 57 Overflow=0
# [845000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 58 Overflow=0
# [855000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 59 Overflow=0
# [865000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 60 Overflow=0
# [875000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 61 Overflow=0
# [885000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 62 Overflow=0
# [895000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 63 Overflow=0
# [905000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 64 Overflow=0
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# [925000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 66 Overflow=0
# [935000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 67 Overflow=0
# [945000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 68 Overflow=0
# [955000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 69 Overflow=0
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# [975000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 71 Overflow=0
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# [995000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 73 Overflow=0
# [1005000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 74 Overflow=0
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# [1035000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 77 Overflow=0
# [1045000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 78 Overflow=0
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# [1085000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 82 Overflow=0
# [1095000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 83 Overflow=0
# [1105000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 84 Overflow=0
# [1115000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 85 Overflow=0
# [1125000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 86 Overflow=0
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# [1145000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 88 Overflow=0
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# [1185000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 92 Overflow=0
# [1195000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count= 93 Overflow=0
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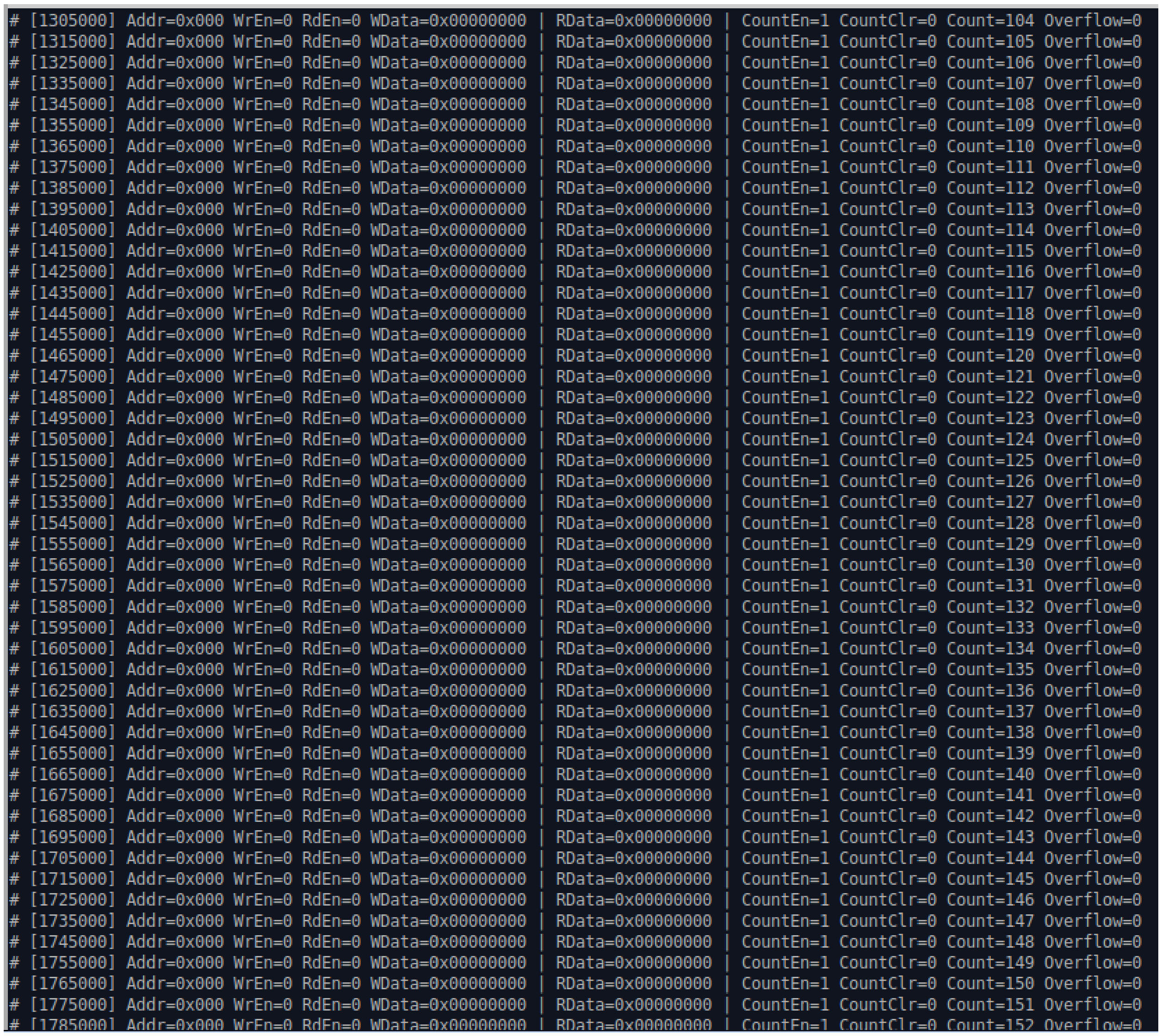

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# [1325000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=106 Overflow=0
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# [1375000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=111 Overflow=0
# [1385000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=112 Overflow=0
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# [1405000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=114 Overflow=0
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# [1425000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=116 Overflow=0
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# [1485000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=122 Overflow=0
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# [1505000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=124 Overflow=0
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# [1525000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=126 Overflow=0
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# [1545000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=128 Overflow=0
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# [1585000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=132 Overflow=0
# [1595000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=133 Overflow=0
# [1605000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=134 Overflow=0
# [1615000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=135 Overflow=0
# [1625000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=136 Overflow=0
# [1635000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=137 Overflow=0
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# [1765000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=150 Overflow=0
# [1775000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=151 Overflow=0
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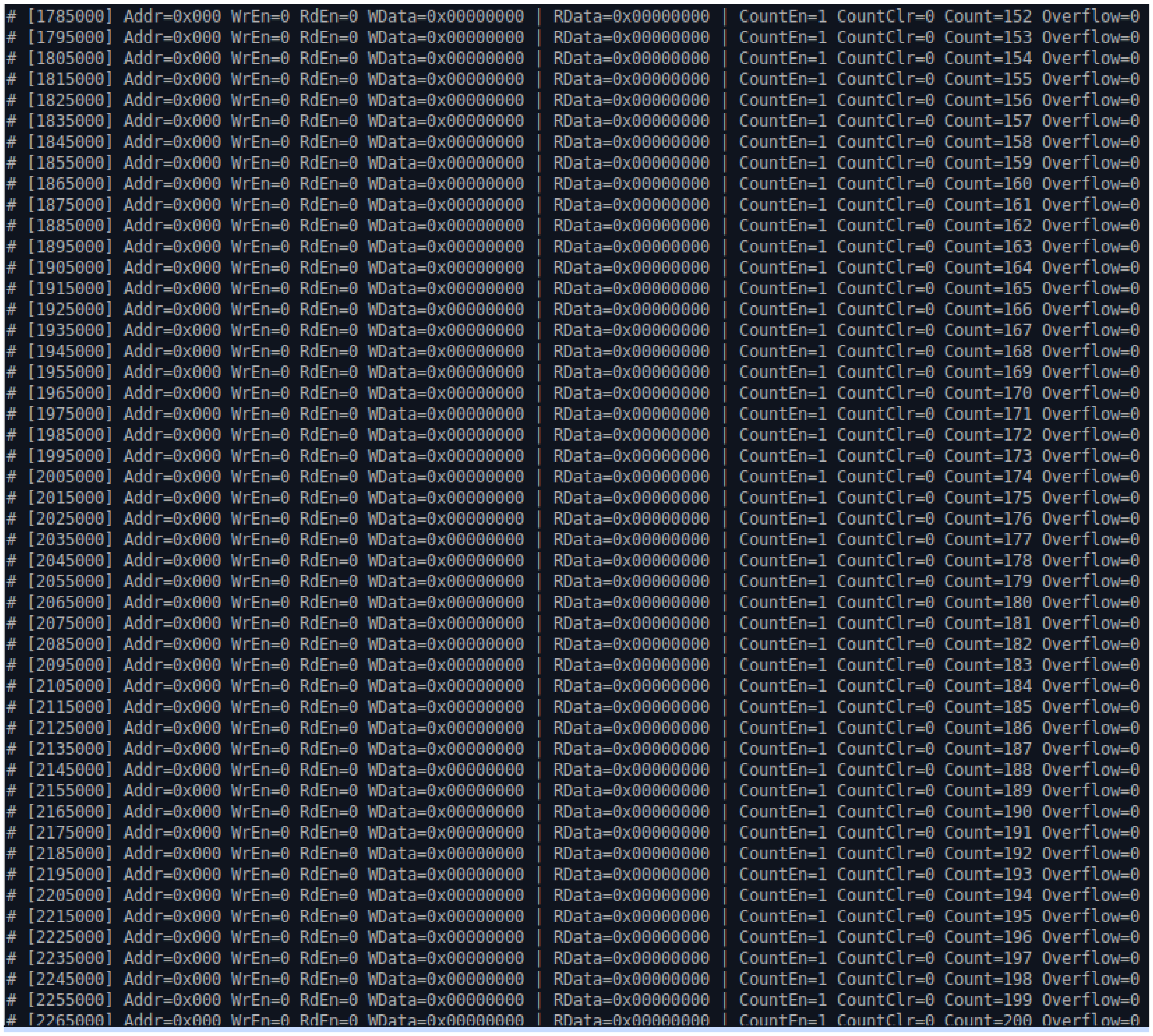

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# [1805000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=154 Overflow=0
# [1815000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=155 Overflow=0
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# [1865000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=160 Overflow=0
# [1875000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=161 Overflow=0
# [1885000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=162 Overflow=0
# [1895000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=163 Overflow=0
# [1905000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=164 Overflow=0
# [1915000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=165 Overflow=0
# [1925000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=166 Overflow=0
# [1935000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=167 Overflow=0
# [1945000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=168 Overflow=0
# [1955000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=169 Overflow=0
# [1965000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=170 Overflow=0
# [1975000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=171 Overflow=0
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# [1995000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=173 Overflow=0
# [2005000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=174 Overflow=0
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# [2175000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=191 Overflow=0
# [2185000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=192 Overflow=0
# [2195000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=193 Overflow=0
# [2205000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=194 Overflow=0
# [2215000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=195 Overflow=0
# [2225000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=196 Overflow=0
# [2235000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=197 Overflow=0
# [2245000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=198 Overflow=0
# [2255000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=199 Overflow=0
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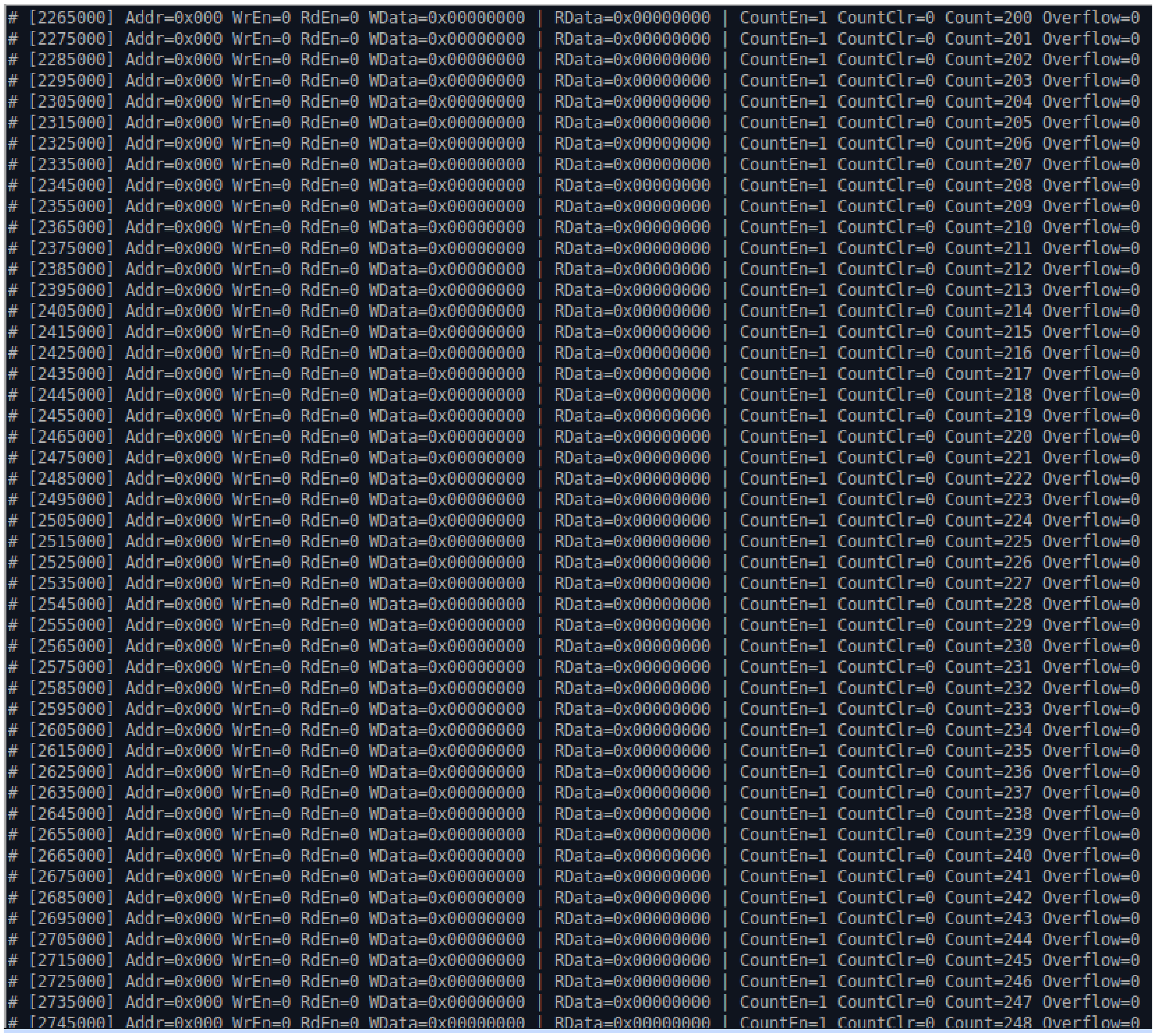

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# [2285000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=202 Overflow=0
# [2295000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=203 Overflow=0
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# [2395000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=213 Overflow=0
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# [2415000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=215 Overflow=0
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# [2475000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=221 Overflow=0
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# [2495000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=223 Overflow=0
# [2505000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=224 Overflow=0
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# [2585000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=232 Overflow=0
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# [2675000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=241 Overflow=0
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# [2725000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=246 Overflow=0
# [2735000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=247 Overflow=0
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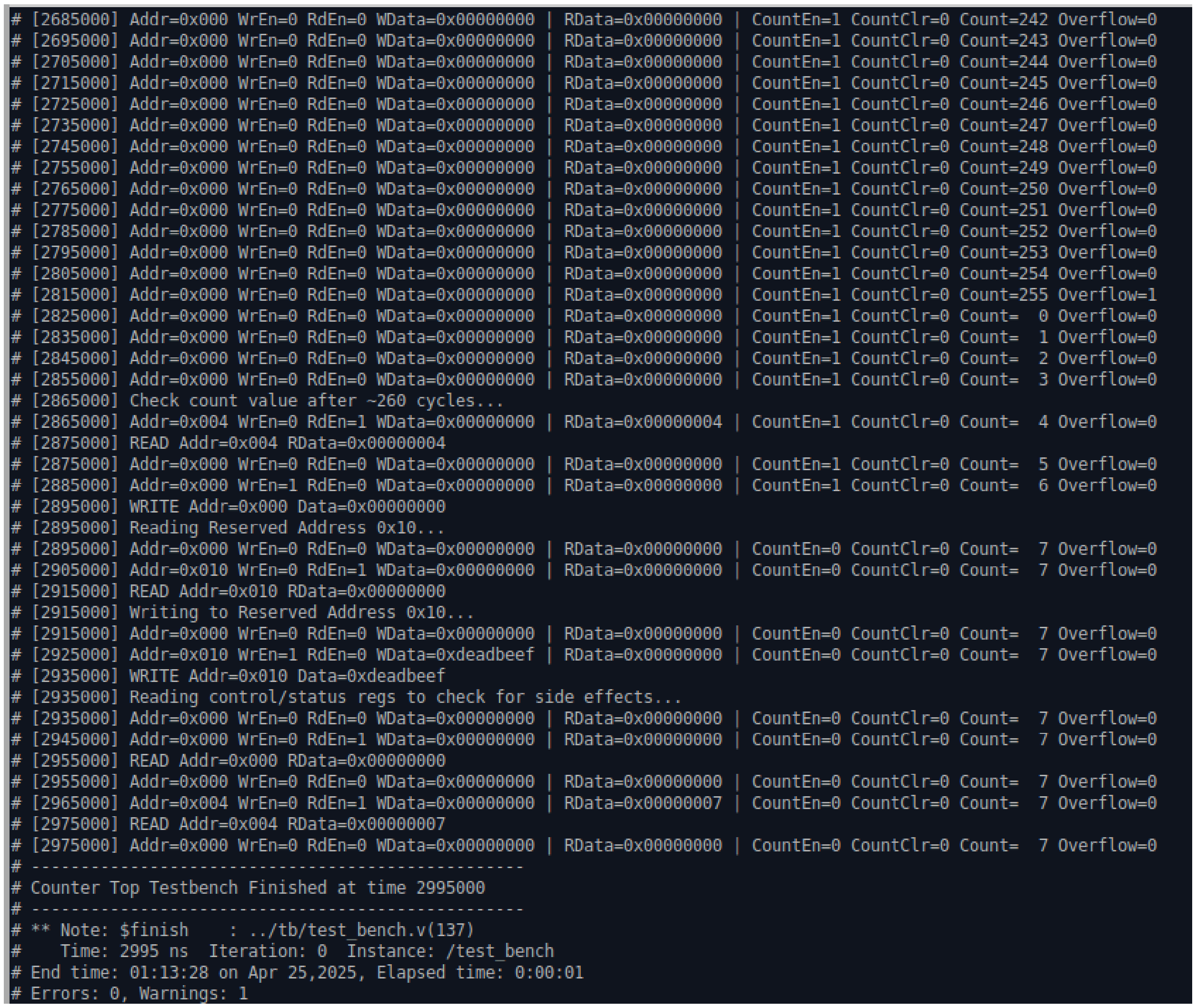

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# [2715000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=245 Overflow=0
# [2725000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=246 Overflow=0
# [2735000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=247 Overflow=0
# [2745000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=248 Overflow=0
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# [2765000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=250 Overflow=0
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# [2805000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=254 Overflow=0
# [2815000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=255 Overflow=1
# [2825000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  0 Overflow=0
# [2835000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  1 Overflow=0
# [2845000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  2 Overflow=0
# [2855000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  3 Overflow=0
# [2865000] Check count value after ~260 cycles...
# [2865000] Addr=0x004 WrEn=0 RdEn=1 WData=0x00000000 | RData=0x00000004 | CountEn=1 CountClr=0 Count=  4 Overflow=0
# [2875000] READ Addr=0x004 RData=0x00000004
# [2875000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  5 Overflow=0
# [2885000] Addr=0x000 WrEn=1 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=1 CountClr=0 Count=  6 Overflow=0
# [2895000] WRITE Addr=0x000 Data=0x00000000
# [2895000] Reading Reserved Address 0x10...
# [2895000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  7 Overflow=0
# [2905000] Addr=0x010 WrEn=0 RdEn=1 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  7 Overflow=0
# [2915000] READ Addr=0x010 RData=0x00000000
# [2915000] Writing to Reserved Address 0x10...
# [2915000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  7 Overflow=0
# [2925000] Addr=0x010 WrEn=1 RdEn=0 WData=0xdeadbeef | RData=0x00000000 | CountEn=0 CountClr=0 Count=  7 Overflow=0
# [2935000] WRITE Addr=0x010 Data=0xdeadbeef
# [2935000] Reading control/status regs to check for side effects...
# [2935000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  7 Overflow=0
# [2945000] Addr=0x000 WrEn=0 RdEn=1 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  7 Overflow=0
# [2955000] READ Addr=0x000 RData=0x00000000
# [2955000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  7 Overflow=0
# [2965000] Addr=0x004 WrEn=0 RdEn=1 WData=0x00000000 | RData=0x00000007 | CountEn=0 CountClr=0 Count=  7 Overflow=0
# [2975000] READ Addr=0x004 RData=0x00000007
# [2975000] Addr=0x000 WrEn=0 RdEn=0 WData=0x00000000 | RData=0x00000000 | CountEn=0 CountClr=0 Count=  7 Overflow=0
# -------------------------------------------------
# Counter Top Testbench Finished at time 2995000
# -------------------------------------------------
# ** Note: $finish    : ../tb/test_bench.v(137)
#    Time: 2995 ns  Iteration: 0  Instance: /test_bench
# End time: 01:13:28 on Apr 25,2025, Elapsed time: 0:00:01
# Errors: 0, Warnings: 1
```

[2815000] Khi Count = 255 -> Overflow = 1 (Counter hoạt động chính xác)