HOMEWORK 1:

```
huugiap@ictc-eda-ldap-1:~/08_ss8/counter_hw/rtl$ cat counter.v
module counter (
input clk,
input rst_n,
input count_en,
input count_clr,

output reg [7:0] count,
output reg overflow
);

always @(posedge clk or negedge rst_n) begin
        if (!rst_n) begin
                count <= 8'b00;
        end else begin
                if (count_clr) begin
                        count <= 8'b00;
                end else if (count_en) begin
                        count <= count + 1;
                end
        end
assign overflow = (count == 8'hFF);

end
endmodule
```

```
huugiap@ictc-eda-ldap-1:~/08_ss8/counter_hw/sim$ make build
vlib work
** Warning: (vlib-34) Library already exists at "work".
Errors: 0, Warnings: 1
vmap work work
Questa Intel Starter FPGA Edition-64 vmap 2023.3 Lib Mapping Utility 2023.07 Jul 17 2023
vmap work work
Modifying modelsim.ini
vlog -f compile.f | tee compile.log
Questa Intel Starter FPGA Edition-64 vlog 2023.3 Compiler 2023.07 Jul 17 2023
Start time: 14:57:34 on Mar 31,2025
vlog -f compile.f
-- Compiling module counter
-- Compiling module test_bench

Top level modules:
        test_bench
End time: 14:57:34 on Mar 31,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
```

```
huugiap@ictc-eda-ldap-1:~/08_ss8/counter_hw/sim$ make run
vsim -debugDB -l test_adder.log -voptargs=+acc -assertdebug -c test_bench -do "log -r /*;run -all;"
Reading pref.tcl

# 2023.3

# vsim -debugDB -l test_adder.log -voptargs="+acc" -assertdebug -c test_bench -do "log -r /*;run -all;"
# Start time: 14:57:38 on Mar 31,2025
# ** Note: (vsim-3812) Design is being optimized...
# ** Note: (vsim-8611) Generating debug db.
# ** Warning: (vopt-10587) Some optimizations are turned off because the +acc switch is in effect. This wi
# ** Note: (vsim-12126) Error and warning message counts have been restored: Errors=0, Warnings=1.
# //  Questa Intel Starter FPGA Edition-64
# //  Version 2023.3 linux_x86_64 Jul 17 2023
# //
# //  Copyright 1991-2023 Mentor Graphics Corporation
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# //
# //  QuestaSim and its associated documentation contain trade
# //  secrets and commercial or financial information that are the property of
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# //  5 U.S.C. Section 552. Furthermore, this information
# //  is prohibited from disclosure under the Trade Secrets Act,
# //  18 U.S.C. Section 1905.
# //
# Loading work.test_bench(fast)
# Loading work.counter(fast)
# ** Note: (vsim-8900) Creating design debug database vsim.dbg.
# log -r /*
# run -all
# ------------------------------------------------
# t=       100 PASS: the init value of counter is 8'h00.
# ------------------------------------------------
# ------------------------------------------------
# t=      5211 PASS: counter value is correct,8'hff
# ------------------------------------------------
# ------------------------------------------------
```
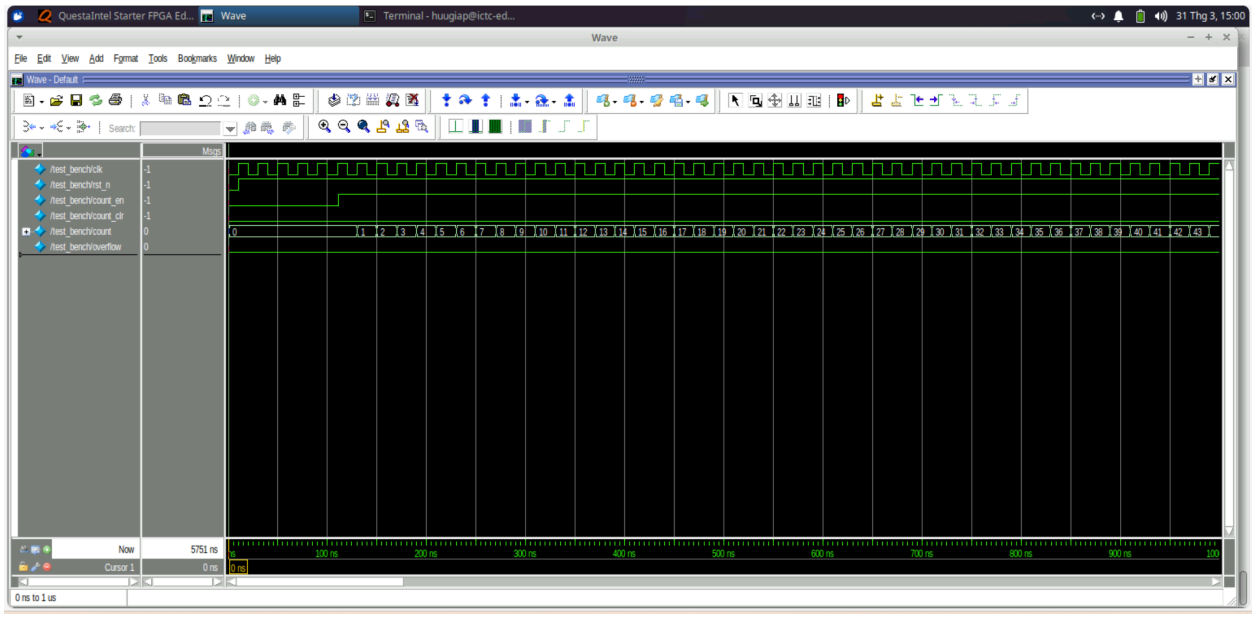
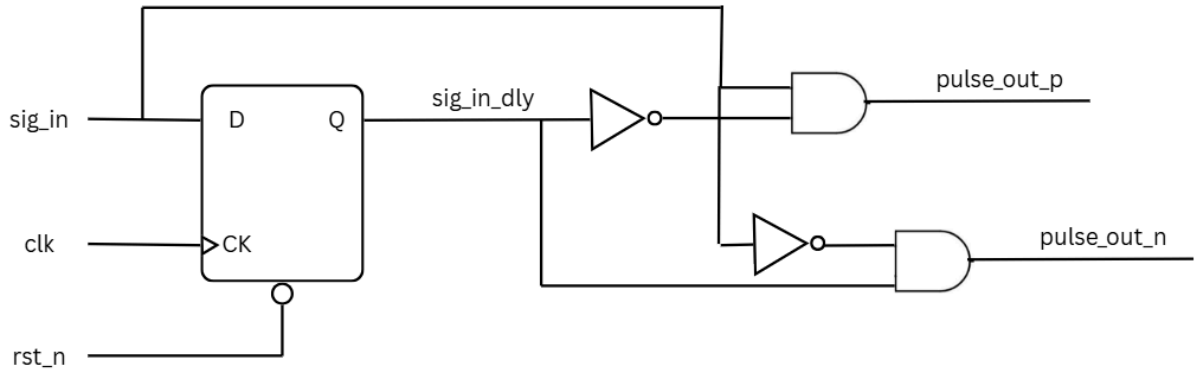

```
# Loading work.test_bench(fast)
# Loading work.counter(fast)
# ** Note: (vsim-8900) Creating design debug database vsim.dbg.
# log -r /*
# run -all
# ------------------------------------------------
# t=       100 PASS: the init value of counter is 8'h00.
# ------------------------------------------------
# ------------------------------------------------
# t=      5211 PASS: counter value is correct,8'hff
# ------------------------------------------------
# ------------------------------------------------
# t=      5211 PASS: overflow is asserted
# ------------------------------------------------
# ------------------------------------------------
# t=      5231 PASS: overflow is negated
# ------------------------------------------------
# ------------------------------------------------
# t=      5231 PASS: counter value is 8'h00 after overflow
# ------------------------------------------------
# ------------------------------------------------
# t=      5431 PASS: counter value is correct - 8'ha
# ------------------------------------------------
# ------------------------------------------------
# t=      5451 PASS: counter value is cleared when count_clr is 1'b1
# ------------------------------------------------
# ------------------------------------------------
# t=      5651 PASS: counter does not start counting when counter_en is 1'b0
# ------------------------------------------------
# ** Note: $finish    : ../tb/test_bench.v(151)
#    Time: 5751 ns  Iteration: 0  Instance: /test_bench
# End time: 14:57:38 on Mar 31,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 1
```



HOMEWORK 2:

Logic diagram edge detector:




```
huugiap@ictc-eda-ldap-1:~/08_ss8/edge_detector/rtl$ cat edge_detector.v
module edge_detector (
 input clk,
 input rst_n,
 input sig_in,

 output pulse_out_p,
 output pulse_out_n
);

reg sig_in_dly;

always @(posedge clk or negedge rst_n) begin
if (!rst_n) begin
        sig_in_dly <= 1'b0;
end else begin
        sig_in_dly <= sig_in;
end
end

assign pulse_out_p = sig_in & ~sig_in_dly;
assign pulse_out_n = ~sig_in & sig_in_dly;

endmodule
```

```
huugiap@ictc-eda-ldap-1:~/08_ss8/edge_detector/tb$ cat test_bench.v
`timescale 1ns / 1ps

module test_bench;

    parameter CLK_PERIOD = 20;

    reg clk;
    reg rst_n;
    reg sig_in;

    wire pulse_out_p;
    wire pulse_out_n;

    edge_detector dut (
        .clk(clk),
        .rst_n(rst_n),
        .sig_in(sig_in),
        .pulse_out_p(pulse_out_p),
        .pulse_out_n(pulse_out_n)
    );

    initial begin
        clk = 1'b0;
        forever #(CLK_PERIOD / 2) clk = ~clk;
    end

    initial begin
        $display("----------------------------------------------------");
        $display(" Bat dau Testbench cho Edge Detector ");
        $display(" Chu ky Clock (CLK_PERIOD) = %0d ns", CLK_PERIOD);
        $display("----------------------------------------------------");

        // 1. Reset ban đầu
        rst_n = 1'b0;
        sig_in = 1'b0;
        repeat(2) @(posedge clk);
        rst_n = 1'b1;
        $display("t=%0t: Reset da duoc go bo.", $time);
        @(posedge clk);
```

```
        // 2. Kiểm tra: Không có cạnh (sig_in thấp)
        $display("t=%0t: Test - Khong co canh (sig_in = 0)", $time);
        sig_in = 1'b0;
        repeat(3) begin
             @(posedge clk);
             if (pulse_out_p !== 1'b0 || pulse_out_n !== 1'b0) begin
                 $display("ERROR @ t=%0t: Phat hien xung sai khi sig_in = 0!", $time);
                 $finish;
             end
        end

        // 3. Kiểm tra: Sườn lên
        $display("t=%0t: Test - Tao suon len", $time);
        @(posedge clk);
        sig_in = 1'b1;
        @(posedge clk);
        $display("t=%0t: Kiem tra xung suon len...", $time);
        if (pulse_out_p !== 1'b1 || pulse_out_n !== 1'b0) begin
            $display("ERROR @ t=%0t: Phat hien suon len sai! (p=%b, n=%b)", $time, pulse_out_p, pulse_out_n);
            $finish;
        end
         @(posedge clk);
        $display("t=%0t: Kiem tra xung suon len da tat...", $time);
         if (pulse_out_p !== 1'b0 || pulse_out_n !== 1'b0) begin
            $display("ERROR @ t=%0t: Xung suon len khong tat dung luc! (p=%b, n=%b)", $time, pulse_out_p, pulse_out_n);
            $finish;
        end

        // 4. Kiểm tra: Không có cạnh (sig_in cao)
        $display("t=%0t: Test - Khong co canh (sig_in = 1)", $time);
        sig_in = 1'b1;
        repeat(3) begin
             @(posedge clk);
             if (pulse_out_p !== 1'b0 || pulse_out_n !== 1'b0) begin
                 $display("ERROR @ t=%0t: Phat hien xung sai khi sig_in = 1!", $time);
                 $finish;
             end
        end
```

```
        // 5. Kiểm tra: Sườn xuống
        $display("t=%0t: Test - Tao suon xuong", $time);
        @(posedge clk);
        sig_in = 1'b0;
        @(posedge clk);
        $display("t=%0t: Kiem tra xung suon xuong...", $time);
        if (pulse_out_p !== 1'b0 || pulse_out_n !== 1'b1) begin
            $display("ERROR @ t=%0t: Phat hien suon xuong sai! (p=%b, n=%b)", $time, pulse_out_p, pulse_out_n);
            $finish;
        end
         @(posedge clk);
        $display("t=%0t: Kiem tra xung suon xuong da tat...", $time);
         if (pulse_out_p !== 1'b0 || pulse_out_n !== 1'b0) begin
            $display("ERROR @ t=%0t: Xung suon xuong khong tat dung luc! (p=%b, n=%b)", $time, pulse_out_p, pulse_out_n);
            $finish;
        end

        // 6. Kiểm tra: Sườn lên lần nữa
        $display("t=%0t: Test - Tao suon len lan nua", $time);
        @(posedge clk);
        sig_in = 1'b1;
        @(posedge clk);
        $display("t=%0t: Kiem tra xung suon len...", $time);
        if (pulse_out_p !== 1'b1 || pulse_out_n !== 1'b0) begin
            $display("ERROR @ t=%0t: Phat hien suon len lan 2 sai! (p=%b, n=%b)", $time, pulse_out_p, pulse_out_n);
            $finish;
        end
        @(posedge clk);
        $display("t=%0t: Kiem tra xung suon len da tat...", $time);
         if (pulse_out_p !== 1'b0 || pulse_out_n !== 1'b0) begin
            $display("ERROR @ t=%0t: Xung suon len lan 2 khong tat dung luc! (p=%b, n=%b)", $time, pulse_out_p, pulse_out_n);
            $finish;
        end

        $display("-------------------------------------------------");
        $display(" Tat ca kiem tra da PASS! Ket thuc mo phong. ");
        $display("-------------------------------------------------");
        # (CLK_PERIOD * 2);
        $finish;
    end

endmodule
```

```
huugiap@ictc-eda-ldap-1:~/08_ss8/edge_detector/sim$ make build
vlib work
** Warning: (vlib-34) Library already exists at "work".
Errors: 0, Warnings: 1
vmap work work
Questa Intel Starter FPGA Edition-64 vmap 2023.3 Lib Mapping Utility 2023.07 Jul 17 2023
vmap work work
Modifying modelsim.ini
vlog -f compile.f | tee compile.log
Questa Intel Starter FPGA Edition-64 vlog 2023.3 Compiler 2023.07 Jul 17 2023
Start time: 16:17:02 on Mar 31,2025
vlog -f compile.f
-- Compiling module edge_detector
-- Compiling module test_bench

Top level modules:
        test_bench
End time: 16:17:03 on Mar 31,2025, Elapsed time: 0:00:01
Errors: 0, Warnings: 0
```

```
huugiap@ictc-eda-ldap-1:~/08_ss8/edge_detector/sim$ make run
vsim -debugDB -l test_adder.log -voptargs=+acc -assertdebug -c test_bench -do "log -r /*;run -all;"
Reading pref.tcl

# 2023.3

# vsim -debugDB -l test_adder.log -voptargs="+acc" -assertdebug -c test_bench -do "log -r /*;run -all;"
# Start time: 16:17:17 on Mar 31,2025
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# ** Note: (vsim-8611) Generating debug db.
# ** Warning: (vopt-10587) Some optimizations are turned off because the +acc switch is in effect. This wi
# ** Note: (vsim-12126) Error and warning message counts have been restored: Errors=0, Warnings=1.
# //  Questa Intel Starter FPGA Edition-64
# //  Version 2023.3 linux_x86_64 Jul 17 2023
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# //  5 U.S.C. Section 552. Furthermore, this information
# //  is prohibited from disclosure under the Trade Secrets Act,
# //  18 U.S.C. Section 1905.
# //
# Loading work.test_bench(fast)
# Loading work.edge_detector(fast)
# ** Note: (vsim-8900) Creating design debug database vsim.dbg.
# log -r /*
# run -all
# ------------------------------------------------
#  Bat dau Testbench cho Edge Detector
#  Chu ky Clock (CLK_PERIOD) = 20 ns
# ------------------------------------------------
# t=30000: Reset da duoc go bo.
# t=50000: Test - Khong co canh (sig_in = 0)
# t=110000: Test - Tao suon len
# t=150000: Kiem tra xung suon len...
# t=170000: Kiem tra xung suon len da tat...
# t=170000: Test - Khong co canh (sig_in = 1)
# t=230000: Test - Tao suon xuong
```

```
# ------------------------------------------------
#  Bat dau Testbench cho Edge Detector
#  Chu ky Clock (CLK_PERIOD) = 20 ns
# ------------------------------------------------
# t=30000: Reset da duoc go bo.
# t=50000: Test - Khong co canh (sig_in = 0)
# t=110000: Test - Tao suon len
# t=150000: Kiem tra xung suon len...
# t=170000: Kiem tra xung suon len da tat...
# t=170000: Test - Khong co canh (sig_in = 1)
# t=230000: Test - Tao suon xuong
# t=270000: Kiem tra xung suon xuong...
# t=290000: Kiem tra xung suon xuong da tat...
# t=290000: Test - Tao suon len lan nua
# t=330000: Kiem tra xung suon len...
# t=350000: Kiem tra xung suon len da tat...
# ------------------------------------------------
#  Tat ca kiem tra da PASS! Ket thuc mo phong.
# ------------------------------------------------
# ** Note: $finish    : ../tb/test_bench.v(118)
#    Time: 390 ns  Iteration: 0  Instance: /test_bench
# End time: 16:17:17 on Mar 31,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 1
```