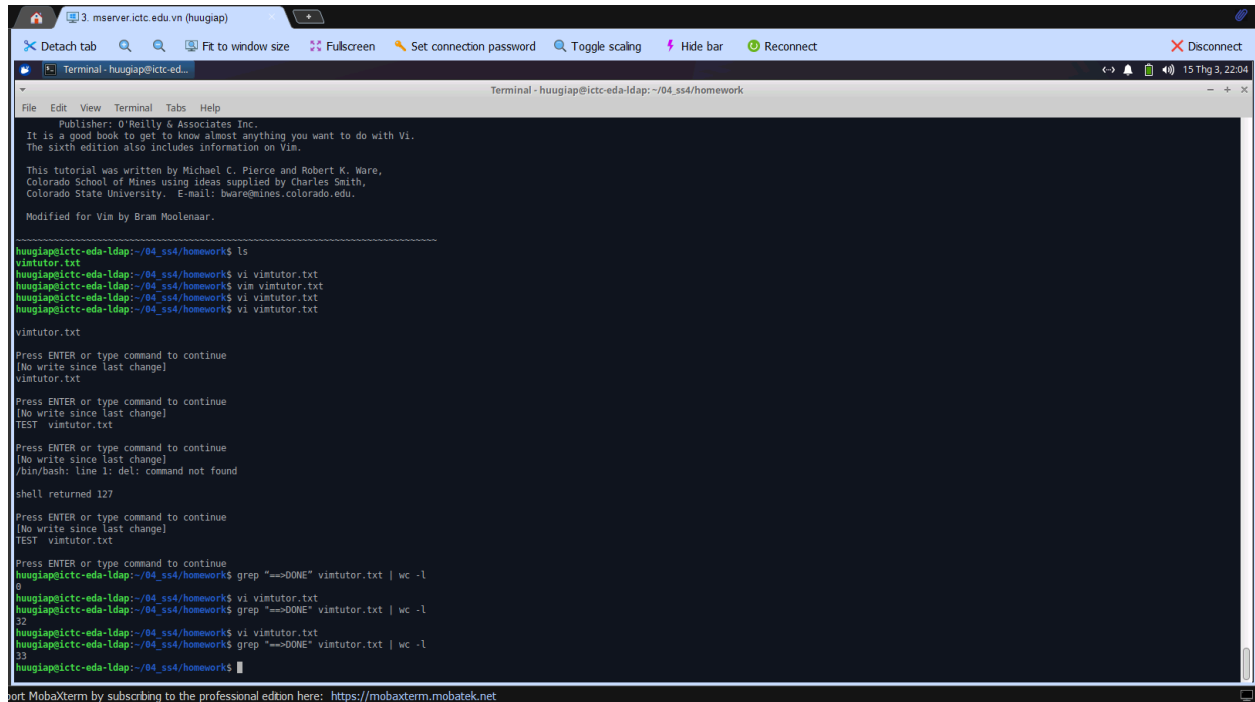


Homework 1:



```
msrvr.icctc.edu.vn (huugiap)
Detach tab  Fit to window size  Fullscreen  Set connection password  Toggle scaling  Hide bar  Reconnect  Disconnect
Terminal - huugiap@icctc-ed... 15 Thg 3, 22:04
File Edit View Terminal Tabs Help
Publisher: O'Reilly & Associates Inc.
It is a good book to get to know almost anything you want to do with Vi.
The sixth edition also includes information on Vim.

This tutorial was written by Michael C. Pierce and Robert K. Ware,
Colorado School of Mines using ideas supplied by Charles Smith,
Colorado State University. E-mail: bware@mines.colorado.edu.

Modified for Vim by Bram Moolenaar.

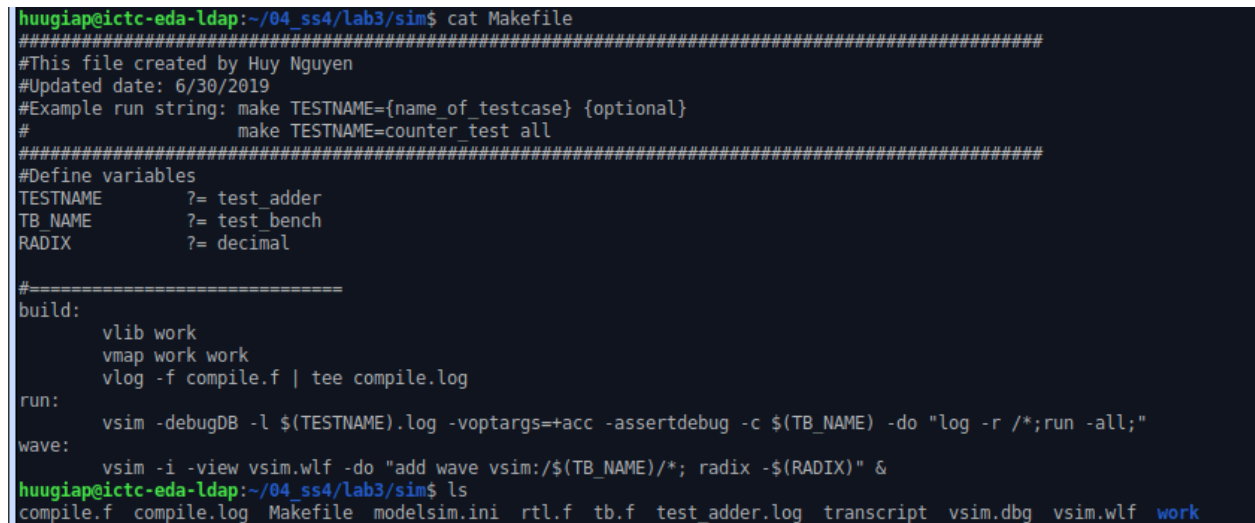
-----
huugiap@icctc-eda-ldap:~/04_ss4/homework$ ls
vintutor.txt
huugiap@icctc-eda-ldap:~/04_ss4/homework$ vi vintutor.txt
huugiap@icctc-eda-ldap:~/04_ss4/homework$ vim vintutor.txt
huugiap@icctc-eda-ldap:~/04_ss4/homework$ vi vintutor.txt
huugiap@icctc-eda-ldap:~/04_ss4/homework$ vi vintutor.txt

vintutor.txt
Press ENTER or type command to continue
[No write since last change]
vintutor.txt
Press ENTER or type command to continue
[No write since last change]
TEST vintutor.txt
Press ENTER or type command to continue
[No write since last change]
/bin/bash: line 1: del: command not found
shell returned 127
Press ENTER or type command to continue
[No write since last change]
TEST vintutor.txt
Press ENTER or type command to continue
huugiap@icctc-eda-ldap:~/04_ss4/homework$ grep "==>DONE" vintutor.txt | wc -l
0
huugiap@icctc-eda-ldap:~/04_ss4/homework$ vi vintutor.txt
huugiap@icctc-eda-ldap:~/04_ss4/homework$ grep "==>DONE" vintutor.txt | wc -l
32
huugiap@icctc-eda-ldap:~/04_ss4/homework$ vi vintutor.txt
huugiap@icctc-eda-ldap:~/04_ss4/homework$ grep "==>DONE" vintutor.txt | wc -l
33
huugiap@icctc-eda-ldap:~/04_ss4/homework$
```

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Homework 2:

File Makefile ban đầu trong lab3:



```
huugiap@icctc-eda-ldap:~/04_ss4/lab3/sim$ cat Makefile
#####
#This file created by Huy Nguyen
#Updated date: 6/30/2019
#Example run string: make TESTNAME={name_of_testcase} {optional}
#                      make TESTNAME=counter_test all
#####
#Define variables
TESTNAME      ?= test_adder
TB_NAME       ?= test_bench
RADIX         ?= decimal

#=====
build:
    vlib work
    vmap work work
    vlog -f compile.f | tee compile.log

run:
    vsim -debugDB -l $(TESTNAME).log -voptargs=+acc -assertdebug -c $(TB_NAME) -do "log -r /*;run -all;"

wave:
    vsim -i -view vsim.wlf -do "add wave vsim:/$(TB_NAME)/*; radix -$(RADIX)" &
huugiap@icctc-eda-ldap:~/04_ss4/lab3/sim$ ls
compile.f compile.log Makefile modelsim.ini rtl.f tb.f test_adder.log transcript vsim.dbg vsim.wlf work
```

Chỉnh sửa file Makefile:

```
huugiap@ictc-eda-ldap:~/04_ss4/lab3/sim$ vi Makefile
huugiap@ictc-eda-ldap:~/04_ss4/lab3/sim$ cat Makefile
#####
#This file created by Huy Nguyen
#Updated date: 6/30/2019
#Example run string: make TESTNAME={name_of_testcase} {optional}
#                      make TESTNAME=counter_test all
#####
#Define variables
TESTNAME      ?= test_adder
TB_NAME       ?= test_bench
RADIX         ?= decimal

#=====
build:
    vlib work
    vmap work work
    vlog -f compile.f | tee compile.log

run:
    vsim -debugDB -l $(TESTNAME).log -voptargs==acc -assertdebug -c $(TB_NAME) -do "log -r /*;run -all;"

wave:
    vsim -i -view vsim.wlf -do "add wave vsim:/$(TB_NAME)/*; radix -$(RADIX)" &

clean:
    rm -rf work transcript *.log *.wlf *.vcd

all: build run

help:
    @echo "*****"
    @echo "** make clean : clean all compiled data"
    @echo "** make build : build the design"
    @echo "** make run  : run simulation"
    @echo "** make all  : build and run simulation"
    @echo "** make wave : open waveform"
    @echo "*****"
```

Chạy make help, make clean, make build:

```
huugiap@ictc-eda-ldap:~/04_ss4/lab3/sim$ make help
*****
** make clean : clean all compiled data
** make build : build the design
** make run   : run simulation
** make all   : build and run simulation
** make wave  : open waveform
*****
huugiap@ictc-eda-ldap:~/04_ss4/lab3/sim$ make clean
rm -rf work transcript *.log *.wlf *.vcd
huugiap@ictc-eda-ldap:~/04_ss4/lab3/sim$ make build
vlib work
vmap work work
Questa Intel Starter FPGA Edition-64 vmap 2023.3 Lib Mapping Utility 2023.07 Jul 17 2023
vmap work work
Modifying modelsim.ini
vlog -f compile.f | tee compile.log
Questa Intel Starter FPGA Edition-64 vlog 2023.3 Compiler 2023.07 Jul 17 2023
Start time: 23:39:10 on Mar 15,2025
vlog -f compile.f
-- Compiling module top
-- Compiling module test_bench

Top level modules:
    test_bench
End time: 23:39:10 on Mar 15,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
```

Chạy make run:

```
huugiapi@ictc-eda-ldap:~/04_ss4/lab3/sim$ make run
vsim -debugDB -l test_adder.log -voptargs="+acc" -assertdebug -c test_bench -do "log -r /*;run -all;"
Reading pref.tcl

# 2023.3

# vsim -debugDB -l test_adder.log -voptargs="+acc" -assertdebug -c test_bench -do "log -r /*;run -all;"
# Start time: 23:39:18 on Mar 15,2025
# ** Note: (vsim-3812) Design is being optimized...
# ** Note: (vsim-8611) Generating debug db.
# ** Warning: (vopt-10587) Some optimizations are turned off because the +acc switch is in effect. This will cause your simulation to run slowly. Please use -access/-debug to maintain needed visibility.
# ** Note: (vsim-12126) Error and warning message counts have been restored: Errors=0, Warnings=1.
# // Questa Intel Starter FPGA Edition-64
# // Version 2023.3 Linux_x86_64 Jul 17 2023
# //
# // Copyright 1991-2023 Mentor Graphics Corporation
# // All Rights Reserved.
# //
# // QuestaSim and its associated documentation contain trade
# // secrets and commercial or financial information that are the property of
# // Mentor Graphics Corporation and are privileged, confidential,
# // and exempt from disclosure under the Freedom of Information Act,
# // 5 U.S.C. Section 552. Furthermore, this information
# // is prohibited from disclosure under the Trade Secrets Act,
# // 18 U.S.C. Section 1905.
# //
# Loading work.test_bench(fast)
# Loading work.top(fast)
# ** Note: (vsim-8900) Creating design debug database vsim.dbg.
# log -r /*
# run -all
#
# =====
# === Case 1: a = 0, b = 0 ===
# =====
# t=      100 PASS: a=0 b=0 z=0
# -----
#
# === Case 2: a = 0, b = 1 ===
# =====
# t=      201 PASS: a=0 b=1 z=1
# -----
#
# =====
```

```
# =====
# === Case 3: a = 1, b = 0 ===
# =====
# t=      302 PASS: a=1 b=0 z=1
# -----
#
# === Case 4: a = 1, b = 1 ===
# =====
# t=      403 PASS: a=1 b=1 z=0
# -----
#
# ** Note: $finish      : ../tb/test_bench.v(87)
# Time: 503 ns Iteration: 0 Instance: /test_bench
# End time: 23:39:19 on Mar 15,2025, Elapsed time: 0:00:01
# Errors: 0, Warnings: 1
```

Chạy make all:

```
huugiapi@ictc-eda-ldap:~/04_ss4/lab3/sim$ make all
vlib work
** Warning: (vlib-34) Library already exists at "work".
Errors: 0, Warnings: 1
vmap work work
Questa Intel Starter FPGA Edition-64 vmap 2023.3 Lib Mapping Utility 2023.07 Jul 17 2023
vmap work work
Modifying modelsim.ini
vlog -f compile.f | tee compile.log
Questa Intel Starter FPGA Edition-64 vlog 2023.3 Compiler 2023.07 Jul 17 2023
Start time: 23:39:29 on Mar 15,2025
vlog -f compile.f
-- Compiling module top
-- Compiling module test_bench

Top level modules:
    test_bench
End time: 23:39:29 on Mar 15,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vsim -debugDB -l test_adder.log -voptargs="+acc" -assertdebug -c test_bench -do "log -r /*;run -all;"
Reading pref.tcl

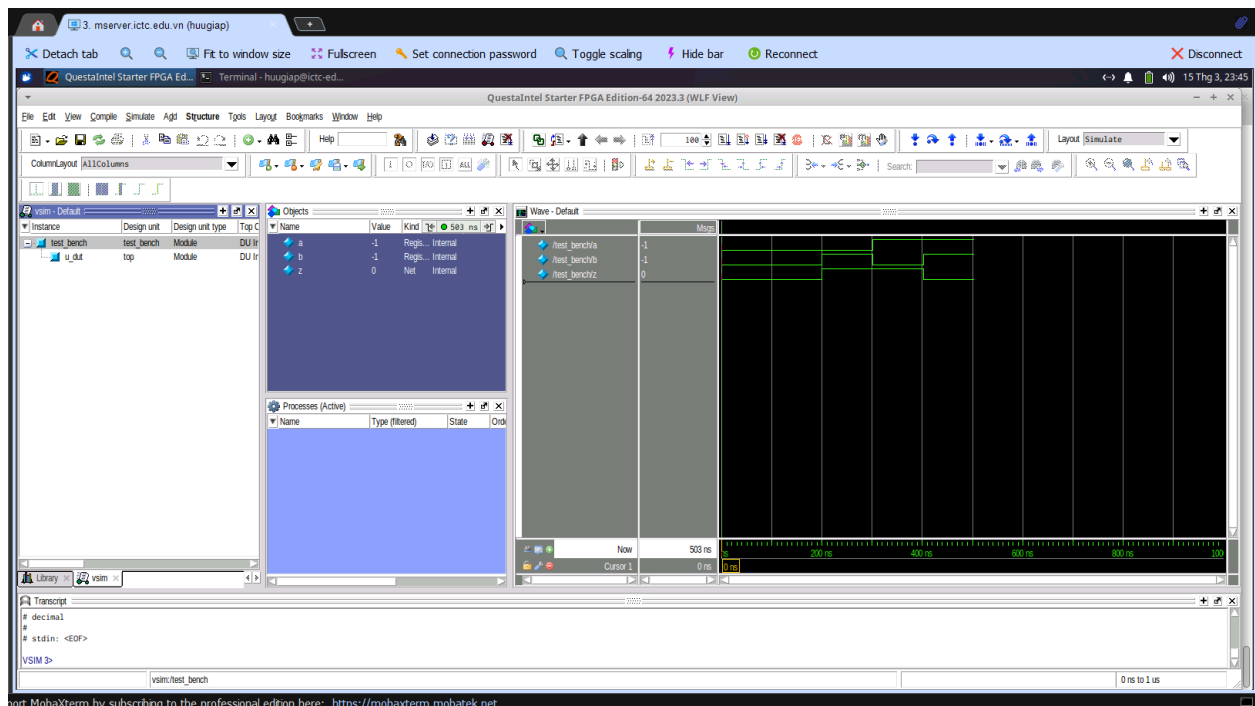
# 2023.3

# vsim -debugDB -l test_adder.log -voptargs="+acc" -assertdebug -c test_bench -do "log -r /*;run -all;"
# Start time: 23:39:30 on Mar 15,2025
# ** Note: (vsim-8009) Loading existing optimized design _opt
# // Questa Intel Starter FPGA Edition-64
# // Version 2023.3 linux_x86_64 Jul 17 2023
# //
# // Copyright 1991-2023 Mentor Graphics Corporation
# // All Rights Reserved.
# //
# // QuestaSim and its associated documentation contain trade
# // secrets and commercial or financial information that are the property of
# // Mentor Graphics Corporation and are privileged, confidential,
# // and exempt from disclosure under the Freedom of Information Act,
# // 5 U.S.C. Section 552. Furthermore, this information
# // is prohibited from disclosure under the Trade Secrets Act,
# // 18 U.S.C. Section 1905.
# //
```

```
# Loading work.test_bench(fast)
# Loading work.top(fast)
# ** Note: (vsim-8716) Reusing existing debug database vsim.dbg.
# log -r /*
# run -all
#
# =====
# Case 1: a = 0, b = 0
# =====
# t=      100 PASS: a=0 b=0 z=0
# -----
# Case 2: a = 0, b = 1
# =====
# t=      201 PASS: a=0 b=1 z=1
# -----
# Case 3: a = 1, b = 0
# =====
# t=      302 PASS: a=1 b=0 z=1
# -----
# Case 4: a = 1, b = 1
# =====
# t=      403 PASS: a=1 b=1 z=0
# -----
# ** Note: $finish      : ../tb/test_bench.v(87)
# Time: 503 ns Iteration: 0 Instance: /test_bench
# End time: 23:39:30 on Mar 15,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
```

Chạy make wave:

```
huugiap@ictc-eda-ldap:~/04_ss4/lab3/sim$ make wave
vsim -i -view vsim.wlf -do "add wave vsim:/test_bench/*; radix -decimal" &
huugiap@ictc-eda-ldap:~/04_ss4/lab3/sim$ Reading pref.tcl
```



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