Homework 1:

```
huugiap@ictc-eda-ldap:~/06_ss6/full_adder_2b/sim$ cd ../rtl/
huugiap@ictc-eda-ldap:~/06_ss6/full_adder_2b/rtl$ vi full_adder_2b.v
huugiap@ictc-eda-ldap:~/06_ss6/full_adder_2b/rtl$ cat full_adder_2b.v
module full_adder_2b (
    input wire [1:0] a,
    input wire [1:0] b,
    output wire [1:0] sum,
    output wire carry
);

wire c1;


full_adder fa0 (
    .a(a[0]),
    .b(b[0]),
    .c(1'b0),
    .sum(sum[0]),
    .carry(c1)
);

full_adder fa1 (
    .a(a[1]),
    .b(b[1]),
    .c(c1),
    .sum(sum[1]),
    .carry(carry)
);

endmodule
```

```
huugiap@ictc-eda-ldap:~/06_ss6/full_adder_2b/sim$ make build
vlib work
** Warning: (vlib-34) Library already exists at "work".
Errors: 0, Warnings: 1
vmap work work
Questa Intel Starter FPGA Edition-64 vmap 2023.3 Lib Mapping Utility 2023.07 Jul 17 2023
vmap work work
Modifying modelsim.ini
vlog -f compile.f | tee compile.log
Questa Intel Starter FPGA Edition-64 vlog 2023.3 Compiler 2023.07 Jul 17 2023
Start time: 07:35:13 on Mar 23,2025
vlog -f compile.f
-- Compiling module half_adder
-- Compiling module full_adder
-- Compiling module full_adder_2b
-- Compiling module test_bench

Top level modules:
        test_bench
End time: 07:35:13 on Mar 23,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
```

```
huugiap@ictc-eda-ldap:~/06_ss6/full_adder_2b/sim$ make run
vsim -debugDB -l test_adder.log -voptargs=+acc -assertdebug -c test_bench -do "log -r /*;run -all;"
Reading pref.tcl

# 2023.3

# vsim -debugDB -l test_adder.log -voptargs="+acc" -assertdebug -c test_bench -do "log -r /*;run -all;"
# Start time: 07:35:16 on Mar 23,2025
# ** Note: (vsim-3812) Design is being optimized...
# ** Note: (vsim-8611) Generating debug db.
# ** Warning: (vopt-10587) Some optimizations are turned off because the +acc switch is in effect. This will cause your simulation to run slowly. Please use -access/-debug to maintain needed visibility.
# ** Note: (vsim-12126) Error and warning message counts have been restored: Errors=0, Warnings=1.
# //  Questa Intel Starter FPGA Edition-64
# //  Version 2023.3 linux_x86_64 Jul 17 2023
# //
# //  Copyright 1991-2023 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  QuestaSim and its associated documentation contain trade
# //  secrets and commercial or financial information that are the property of
# //  Mentor Graphics Corporation and are privileged, confidential,
# //  and exempt from disclosure under the Freedom of Information Act,
# //  5 U.S.C. Section 552. Furthermore, this information
# //  is prohibited from disclosure under the Trade Secrets Act,
# //  18 U.S.C. Section 1905.
# //
# Loading work.test_bench(fast)
# Loading work.full_adder_2b(fast)
# Loading work.full_adder(fast)
# Loading work.half_adder(fast)
# ** Note: (vsim-8900) Creating design debug database vsim.dbg.
# log -r /*
# run -all
# ====================================
# ==== Case: 0 a = 3, b = 2 =======
# ====================================
# Exp: 5 Actual: 5
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case: 1 a = 2, b = 1 =======
# ====================================
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
```

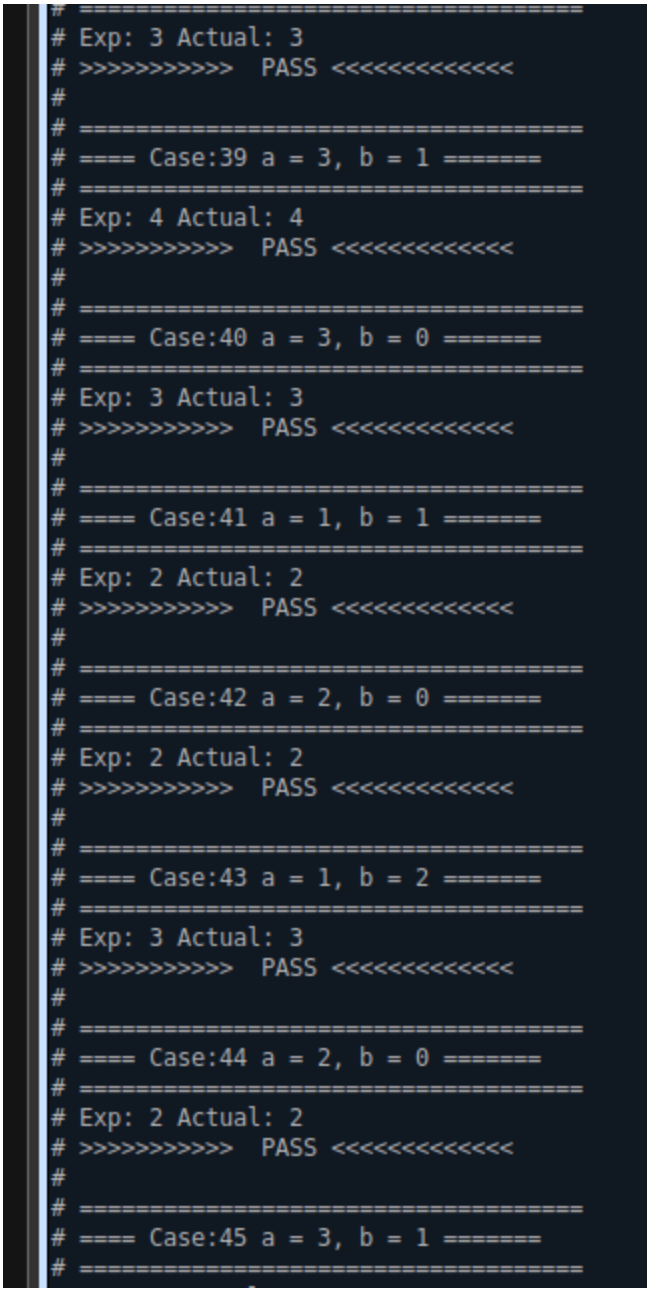
```
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case: 2 a = 0, b = 2 =======
# ====================================
# Exp: 2 Actual: 2
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case: 3 a = 0, b = 0 =======
# ====================================
# Exp: 0 Actual: 0
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case: 4 a = 2, b = 0 =======
# ====================================
# Exp: 2 Actual: 2
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case: 5 a = 2, b = 1 =======
# ====================================
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case: 6 a = 0, b = 1 =======
# ====================================
# Exp: 1 Actual: 1
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case: 7 a = 1, b = 3 =======
# ====================================
# Exp: 4 Actual: 4
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case: 8 a = 2, b = 0 =======
# ====================================
# Exp: 2 Actual: 2
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
```

```
# Exp: 2 Actual: 2
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case: 9 a = 2, b = 3 =======
# ====================================
# Exp: 5 Actual: 5
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:10 a = 0, b = 0 =======
# ====================================
# Exp: 0 Actual: 0
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:11 a = 2, b = 3 =======
# ====================================
# Exp: 5 Actual: 5
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:12 a = 2, b = 0 =======
# ====================================
# Exp: 2 Actual: 2
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:13 a = 2, b = 1 =======
# ====================================
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:14 a = 3, b = 0 =======
# ====================================
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:15 a = 2, b = 2 =======
# ====================================
```

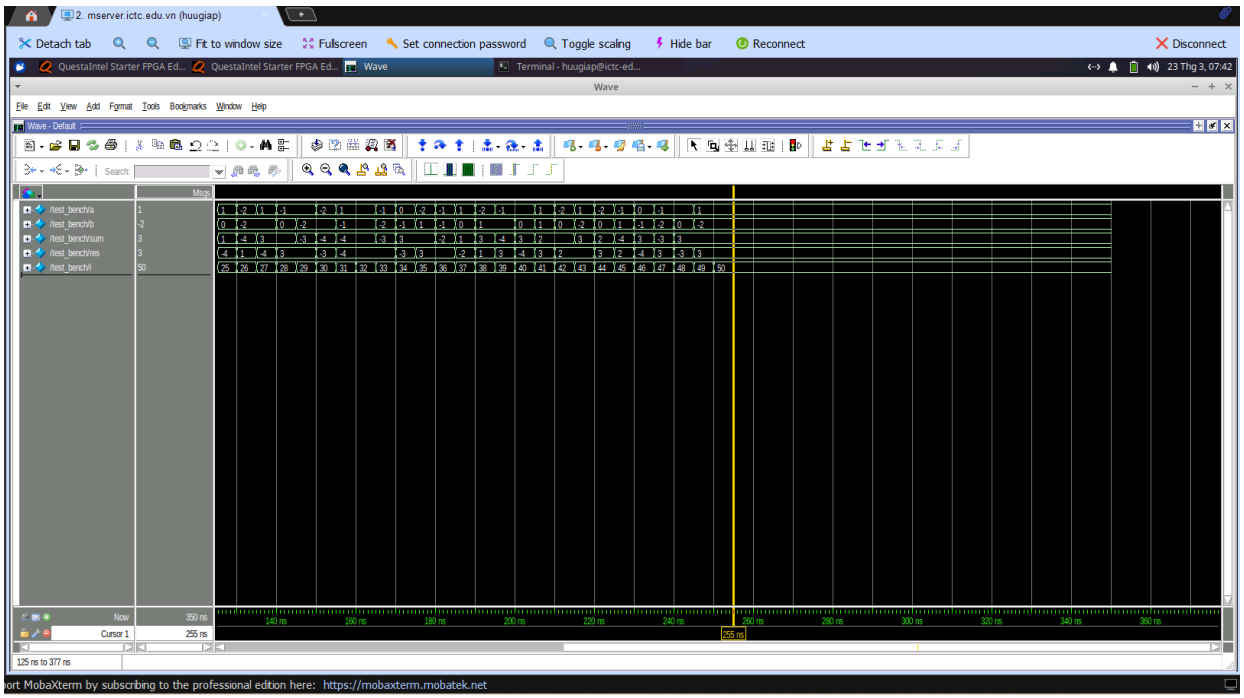
```
# Exp: 4 Actual: 4
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:16 a = 1, b = 1 =======
# ====================================
# Exp: 2 Actual: 2
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:17 a = 2, b = 0 =======
# ====================================
# Exp: 2 Actual: 2
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:18 a = 0, b = 2 =======
# ====================================
# Exp: 2 Actual: 2
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:19 a = 1, b = 3 =======
# ====================================
# Exp: 4 Actual: 4
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:20 a = 3, b = 2 =======
# ====================================
# Exp: 5 Actual: 5
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:21 a = 0, b = 3 =======
# ====================================
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:22 a = 3, b = 1 =======
# ====================================
```

```
# Exp: 4 Actual: 4
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:25 a = 1, b = 0 =======
# ====================================
# Exp: 1 Actual: 1
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:26 a = 2, b = 2 =======
# ====================================
# Exp: 4 Actual: 4
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:27 a = 1, b = 2 =======
# ====================================
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:28 a = 3, b = 0 =======
# ====================================
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:29 a = 3, b = 2 =======
# ====================================
# Exp: 5 Actual: 5
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:30 a = 2, b = 2 =======
# ====================================
# Exp: 4 Actual: 4
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ====================================
# ==== Case:31 a = 1, b = 3 =======
# ====================================
```

```
# ======================================
# Exp: 4 Actual: 4
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ======================================
# ==== Case:32 a = 1, b = 3 =======
# ======================================
# Exp: 4 Actual: 4
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ======================================
# ==== Case:33 a = 3, b = 2 =======
# ======================================
# Exp: 5 Actual: 5
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ======================================
# ==== Case:34 a = 0, b = 3 =======
# ======================================
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ======================================
# ==== Case:35 a = 2, b = 1 =======
# ======================================
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ======================================
# ==== Case:36 a = 3, b = 3 =======
# ======================================
# Exp: 6 Actual: 6
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ======================================
# ==== Case:37 a = 1, b = 0 =======
# ======================================
# Exp: 1 Actual: 1
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ======================================
# ==== Case:38 a = 2, b = 1 =======
# ======================================
```


==================================
Exp: 3 Actual: 3
>>>>>>>>>>> PASS <<<<<<<<<<<<
#
==================================
==== Case:39 a = 3, b = 1 =======
==================================
Exp: 4 Actual: 4
>>>>>>>>>>> PASS <<<<<<<<<<<<
#
==================================
==== Case:40 a = 3, b = 0 =======
==================================
Exp: 3 Actual: 3
>>>>>>>>>>> PASS <<<<<<<<<<<<
#
==================================
==== Case:41 a = 1, b = 1 =======
==================================
Exp: 2 Actual: 2
>>>>>>>>>>> PASS <<<<<<<<<<<<
#
==================================
==== Case:42 a = 2, b = 0 =======
==================================
Exp: 2 Actual: 2
>>>>>>>>>>> PASS <<<<<<<<<<<<
#
==================================
==== Case:43 a = 1, b = 2 =======
==================================
Exp: 3 Actual: 3
>>>>>>>>>>> PASS <<<<<<<<<<<<
#
==================================
==== Case:44 a = 2, b = 0 =======
==================================
Exp: 2 Actual: 2
>>>>>>>>>>> PASS <<<<<<<<<<<<
#
==================================
==== Case:45 a = 3, b = 1 =======
==================================

```
# ==== Case:44 a = 2, b = 0 =======
# ==================================
# Exp: 2 Actual: 2
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ==================================
# ==== Case:45 a = 3, b = 1 =======
# ==================================
# Exp: 4 Actual: 4
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ==================================
# ==== Case:46 a = 0, b = 3 =======
# ==================================
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ==================================
# ==== Case:47 a = 3, b = 2 =======
# ==================================
# Exp: 5 Actual: 5
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ==================================
# ==== Case:48 a = 3, b = 0 =======
# ==================================
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ==================================
# ==== Case:49 a = 1, b = 2 =======
# ==================================
# Exp: 3 Actual: 3
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ** Note: $finish    : ../tb/test_bench.v(29)
#    Time: 350 ns  Iteration: 0  Instance: /test_bench
# End time: 07:35:17 on Mar 23,2025, Elapsed time: 0:00:01
# Errors: 0, Warnings: 1
```



Homework 2:

```
huugiap@ictc-eda-ldap:~/06_ss6/full_adder_16b/rtl$ cat full_adder_16b.v
module full_adder_16b (
    input  wire [15:0] a,
    input  wire [15:0] b,
    output wire [15:0] sum,
    output wire carry
);

    wire [15:0] c;


    full_adder FA0 (
        .a(a[0]),
        .b(b[0]),
        .c(1'b0),
        .sum(sum[0]),
        .carry(c[0])
    );


    genvar i;
    generate
        for (i = 1; i < 16; i = i + 1) begin : adder_chain
            full_adder FA (
                .a(a[i]),
                .b(b[i]),
                .c(c[i-1]),
                .sum(sum[i]),
                .carry(c[i])
            );
        end
    endgenerate

    assign carry = c[15];

endmodule
```

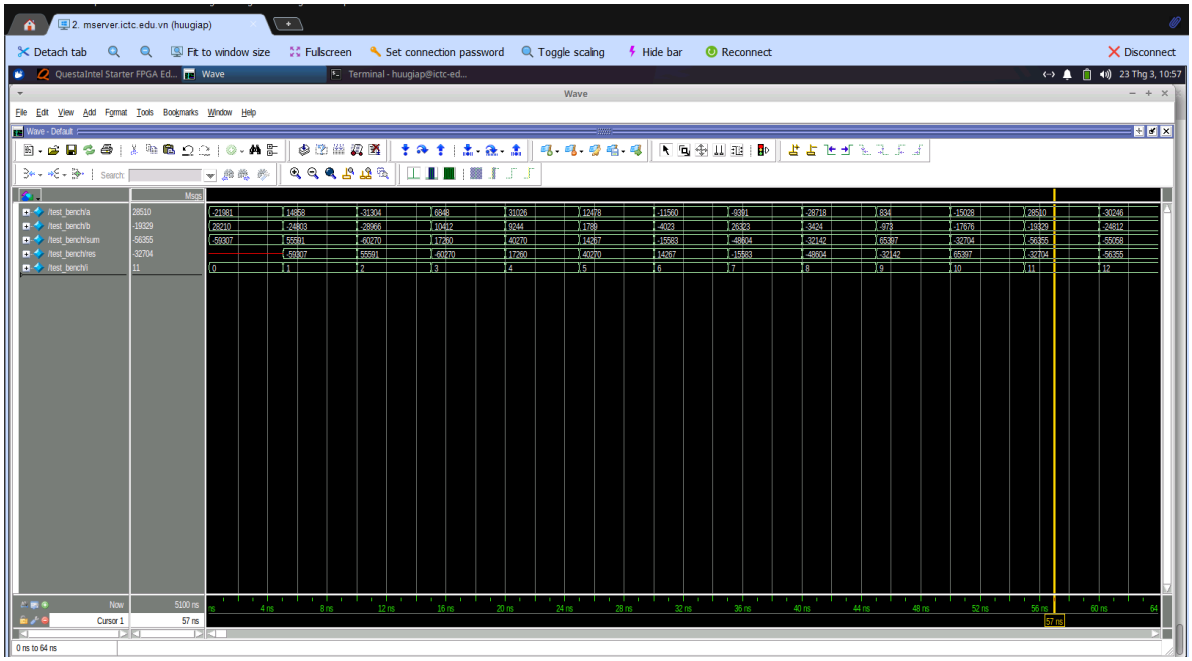
```
huugiap@ictc-eda-ldap:~/06_ss6/full_adder_16b/rtl$ cd ../sim/
huugiap@ictc-eda-ldap:~/06_ss6/full_adder_16b/sim$ make build
vlib work
** Warning: (vlib-34) Library already exists at "work".
Errors: 0, Warnings: 1
vmap work work
Questa Intel Starter FPGA Edition-64 vmap 2023.3 Lib Mapping Utility 2023.07 Jul 17 2023
vmap work work
Modifying modelsim.ini
vlog -f compile.f | tee compile.log
Questa Intel Starter FPGA Edition-64 vlog 2023.3 Compiler 2023.07 Jul 17 2023
Start time: 10:59:45 on Mar 23,2025
vlog -f compile.f
-- Compiling module half_adder
-- Compiling module full_adder
-- Compiling module full_adder_16b
-- Compiling module test_bench

Top level modules:
        test_bench
End time: 10:59:45 on Mar 23,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
```

- **make run:**

```
# ================================================
# ============== Case:        834 a = 22183, b = 35730 ==============
# ================================================
# Exp:  57913 Actual:  57913
# >>>>>>>>>>>  PASS <<<<<<<<<<<<<
#
# ================================================
# ============== Case:        835 a = 32422, b = 22655 ==============
# ================================================
# Exp:  55077 Actual:  55077
# >>>>>>>>>>>  PASS <<<<<<<<<<<<<
#
# ================================================
# ============== Case:        836 a = 21412, b = 11079 ==============
# ================================================
# Exp:  32491 Actual:  32491
# >>>>>>>>>>>  PASS <<<<<<<<<<<<<
#
# ================================================
# ============== Case:        837 a = 24282, b = 13318 ==============
# ================================================
# Exp:  37600 Actual:  37600
# >>>>>>>>>>>  PASS <<<<<<<<<<<<<
#
# ================================================
# ============== Case:        838 a = 59641, b = 36614 ==============
# ================================================
# Exp:  96255 Actual:  96255
# >>>>>>>>>>>  PASS <<<<<<<<<<<<<
#
# ================================================
# ============== Case:        839 a = 10076, b = 63042 ==============
# ================================================
# Exp:  73118 Actual:  73118
# >>>>>>>>>>>  PASS <<<<<<<<<<<<<
#
# ================================================
# ============== Case:        840 a = 37345, b = 28020 ==============
# ================================================
# Exp:  65365 Actual:  65365
# >>>>>>>>>>>  PASS <<<<<<<<<<<<<
#
# ================================================
# ============== Case:        841 a = 45404, b =  5434 ==============
# ================================================
# Exp:  50838 Actual:  50838
# >>>>>>>>>>>  PASS <<<<<<<<<<<<<
#
# ================================================
```

...

```
#
# ================================================
# ============== Case:        993 a = 22200, b = 47484 ==============
# ================================================
# Exp:  69684 Actual:  69684
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ================================================
# ============== Case:        994 a = 24576, b = 25723 ==============
# ================================================
# Exp:  50299 Actual:  50299
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ================================================
# ============== Case:        995 a = 53331, b = 30020 ==============
# ================================================
# Exp:  83351 Actual:  83351
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ================================================
# ============== Case:        996 a = 22493, b = 50733 ==============
# ================================================
# Exp:  73226 Actual:  73226
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ================================================
# ============== Case:        997 a = 44404, b = 29913 ==============
# ================================================
# Exp:  74317 Actual:  74317
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ================================================
# ============== Case:        998 a = 61410, b = 24828 ==============
# ================================================
# Exp:  86238 Actual:  86238
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ================================================
# ============== Case:        999 a = 65535, b = 65535 ==============
# ================================================
# Exp: 131070 Actual: 131070
# >>>>>>>>>>>  PASS <<<<<<<<<<<<
#
# ** Note: $finish    : ../tb/test_bench.v(34)
#    Time: 5100 ns  Iteration: 0  Instance: /test_bench
# End time: 11:00:11 on Mar 23,2025, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
```



Extra homework: This homework is not counted toward your ranking. It is for practice purposes only.

Prove that full_adder can be generated from 2 half-adder (as the diagram in previous practice) by logic equivalent.

Bài làm

Full-Adder is used to perform the binary addition of three binary numbers.

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1