

LQFP100	Type	5 V	Function Used	Main function	STM32 F4 Discovery Problem	Alternative 1	Alternative 2	Alternative 3	Alternative 4	Alternative 5	Alternative 6	Alternative 7	Alternative 8	Alternative 9	Alternative 10	Additional 1
1	I/O	OK	CAN1_SWITCH	PE2		TRACECLK	FSMC_A23	ETH_MII_TXD3								
2	I/O	OK	CAN1_TERMINATION	PE3		TRACED0	FSMC_A19									
3	I/O	OK	CAN2_SWITCH	PE4		TRACED1	FSMC_A20	DCMI_D4								
4	I/O	OK	CAN2_TERMINATION	PE5		TRACED2	FSMC_A21	TIM9_CH1	DCMI_D6							
5	I/O	OK	RS232_SWITCH	PE6		TRACED3	FSMC_A22	TIM9_CH2	DCMI_D7							
6	S		Vbat	Vbat												
7	I/O	OK		PC13												RTC_AF1
8	I/O	OK	PC14-OSC32_IN	PC14-OSC32_IN												OSC32_IN
9	I/O	OK	PC15- OSC32_OUT	PC15- OSC32_OUT												OSC32_OUT
10	S		Vss_5	Vss_5												
11	S		Vdd_5	Vdd_5												
12	I/O	OK	PH0-OSC_IN	PH0-OSC_IN												OSC_IN
13	I/O	OK	PH1-OSC_OUT	PH1-OSC_OUT												OSC_OUT
14	I/O		NRST	NRST												
15	I/O	OK	USART1_SWITCH	PC0		OTG_HS_ULPI_STP										ADC123_IN10
16	I/O	OK	USART2_SWITCH	PC1		ETH_MDC										ADC123_IN11
17	I/O	OK	I2C2_SWITCH	PC2		SPI2_MISO	OTG_HS_ULPI_DIR	ETH_MII_TXD2	I2Sext_SD							ADC123_IN12
18	I/O	OK	I2C2_PULLUP	PC3		SPI2_MOSI	I2S2_SD	OTG_HS_ULPI_NXT	ETH_MII_TX_CLK							ADC123_IN13
19	S		Vdd	Vdd												
20	S		Vss_a	Vss_a												
21	S		Vref_+	Vref_+												
22	S		Vdd_a	Vdd_a												
23	I/O	OK	UART4_TX	PA0-WKUP		USART2_CTS	UART4_TX	ETH_MII_CRS	TIM2_CH1_ETR	TIM5_CH1	TIM8_ETR					ADC123_IN0
24	I/O	OK	UART4_RX	PA1		USART2_RTS	UART4_RX	ETH_RMII_REF_CLK	ETH_MII_RX_CLK	TIM5_CH2	TIMM2_CH2					ADC123_IN1
25	I/O	OK	USART2_TX	PA2		USART2_TX	TIM5_CH3	TIM9_CH1	TIM2_CH3	ETH_MDIO						ADC123_IN2
26	I/O	OK	USART2_RX	PA3		USART2_RX	TIM5_CH4	TIM9_CH2	TIM2_CH4	OTG_HS_ULPI_D0	ETH_MII_COL					ADC123_IN3
27	S		Vss_4	Vss_4												
28	S		Vdd_4	Vdd_4												
29	I/O		SPI1_NSS	PA4		SPI1_NSS	SPI3_NSS	USART2_CK	DCMI_HSYNC	OTG_HS_SOF	I2S3_WS					ADC12_IN4
30	I/O		SPI1_SCK	PA5		SPI1_SCK	OTG_HS_ULPI_CK	TIM2_CH1_ETR	TIM8_CHIN							ADC12_IN5
31	I/O	OK	SPI1_MISO	PA6		SPI1_MISO	TIM8_BKIN	TIM13_CH1	DCMI_PIXCLK	TIM3_CH1	TIM1_BKIN					ADC12_IN6
32	I/O	OK	SPI1_MOSI	PA7		SPI1_MOSI	TIM8_CH1N	TIM14_CH1	TIM3_CH2	ETH_MII_RX_DV	TIM1_CH1N	RMII_CRS_DV				ADC12_IN7
33	I/O	OK	LED1	PC4		ETH_RMII_RX_D0	ETH_MII_RX_D0									ADC12_IN14
34	I/O	OK	LED2	PC5		ETH_RMII_RX_D1	ETH_MII_RX_D1									ADC12_IN15
35	I/O	OK	LED3	PB0		TIM3_CH3	TIM8_CH2N	OTG_HS_ULPI_D1	ETH_MII_RXD2	TIM1_CH2N						ADC12_IN8
36	I/O	OK	LED4	PB1		TIM3_CH4	TIM8_CH3N	OTG_HS_ULPI_D2	ETH_MII_RXD3	TIM1_CH3N						ADC12_IN9
37	I/O	OK		PB2-BOOT1												
38	I/O	OK	FSMC_D4	PE7		FSMC_D4	TIM1_ETR									
39	I/O	OK	FSMC_D5	PE8		FSMC_D5	TIM1_CH1N									
40	I/O	OK	FSMC_D6	PE9		FSMC_D6	TIM1_CH1									
41	I/O	OK	FSMC_D7	PE10		FSMC_D7	TIM1_CH2N									
42	I/O	OK	FSMC_D8	PE11		FSMC_D8	TIM1_CH2									
43	I/O	OK	FSMC_D9	PE12		FSMC_D9	TIM1_CH3N									
44	I/O	OK	FSMC_D10	PE13		FSMC_D10	TIM1_CH3									
45	I/O	OK	FSMC_D11	PE14		FSMC_D11	TIM1_CH4									
46	I/O	OK	FSMC_D12	PE15		FSMC_D12	TIM1_BKIN									
47	I/O	OK	I2C2_SCL	PB10		SPI2_SCK	I2S2_CK	I2C2_SCL	USART3_TX	OTG_HS_ULPI_D3	ETH_MII_RX_ER	TIM2_CH3				
48	I/O	OK	I2C2_SDA	PB11		I2C2_SDA	USART3_RX	OTG_HS_ULPI_D4	ETH_RMII_TX_EN	ETH_MII_TX_EN	TIM2_CH4					
49	S		Vcap_1	Vcap_1												
50	S		Vdd_1	Vdd_1												
51	I/O	OK	MEM_CS	PB12		SPI2_NSS	I2S2_WS	I2C2_SMBA	USART3_CK	TIM1_BKIN	CAN2_RX	OTG_HS_ULPI_D5	ETH_RMII_TXD0	ETH_MII_TXD0	OTG_HS_ID	
52	I/O	OK	SPI2_SCK	PB13		SPI2_SCK	I2S2_CK	USART3_CTS	TIM1_CH1N	CAN2_TX	OTG_HS_ULPI_D6	ETH_RMII_TXD1	ETH_MII_TXD1			OTG_HS_VBUS
53	I/O	OK	SPI2_MISO	PB14		SPI2_MISO	TIM1_CH2N	TIM12_CH1	OTG_HS_DM	USART3_RTS	TIM8_CH2N/	I2S2ext_SD				
54	I/O	OK	SPI2_MOSI	PB15		SPI2_MOSI	I2S2_SD	TIM1_CH3N	TIM8_CH3N	TIM12_CH2	OTG_HS_DP					
55	I/O	OK	FSMC_D13	PD8		FSMC_D13	USART3_TX									
56	I/O	OK	FSMC_D14	PD9		FSMC_D14	USART3_RX/									
57	I/O	OK	FSMC_D15	PD10		FSMC_D15	USART3_CK/									
58	I/O	OK	LCD_WAIT	PD11		FSMC_CLE	FSMC_A16	USART3_CTS								
59	I/O	OK	LCD_INT	PD12		FSMC_ALE	FSMC_A17	TIM4_CH1	USART3_RTS							
60	I/O	OK	FSMC_A18	PD13		FSMC_A18	TIM4_CH2									
61	I/O	OK	FSMC_D0	PD14		FSMC_D0	TIM4_CH3									
62	I/O	OK	FSMC_D1	PD15		FSMC_D1	TIM4_CH4									
63	I/O	OK	USART6_TX	PC6		I2S2_MCK	TIM8_CH1	SDIO_D6	USART6_TX	DCMI_D0	TIM3_CH1					
64	I/O	OK	USART6_RX	PC7		I2S3_MCK	TIM8_CH2	SDIO_D7	USART6_RX	DCMI_D1	TIM3_CH2					
65	I/O	OK	SDIO_D0	PC8		TIM8_CH3	SDIO_D0	TIM3_CH3	USART6_CK	DCMI_D2						
66	I/O	OK	SDIO_D1	PC9		I2S_CKIN	MCO2	TIM8_CH4	SDIO_D1	I2C3_SDA	DCMI_D3	TIM3_CH4				
67	I/O	OK	I2C2_PWR_MEASURE	PA8		MCO1	USART1_CK	TIM1_CH1	I2C3_SCL	OTG_FS_SOF						
68	I/O	OK	USART1_TX	PA9		USART1_TX	TIM1_CH2	I2C3_SMBA	DCMI_D0							OTG_FS_VBUS
69	I/O	OK	USART1_RX	PA10		USART1_RX	TIM1_CH3	OTG_FS_ID	DCMI_D1							
70	I/O	OK	CAN1_RX	PA11		USART1_CTS	CAN1_RX	TIM1_CH4	OTG_FS_DM							
71	I/O	OK	CAN1_TX	PA12		USART1_RTS	CAN1_TX	TIM1_ETR	OTG_FS_DP							
72	I/O	OK	PA13 (JTMS-SWDIO)	PA13 (JTMS-SWDIO)		JTMS-SWDIO										
73	S		Vcap_2	Vcap_2												
74	S		Vss_2	Vss_2												
75	S		Vdd_2	Vdd_2												
76	I/O	OK	PA14 (JTCK-SWCLK)	PA14 (JTCK-SWCLK)		JTCK-SWCLK										
77	I/O	OK	PA15 (JTDI)	PA15 (JTDI)		JTDI	SPI3_NSS	I2S3_WS	TIM2_CH1_ETR	SPI1_NSS						
78	I/O	OK	SDIO_D2	PC10		SPI3_SCK	I2S3_CK	UART4_TX	SDIO_D2	DCMI_D8	USART3_TX					
79	I/O	OK	SDIO_D3	PC11		UART4_RX	SPI3_MISO	SDIO_D3	DCMI_D4	USART3_RX	I2S3ext_SD					
80	I/O	OK	SDIO_CK	PC12		UART5_TX	SDIO_CK	DCMI_D9	SPI3_MOSI	I2S3_SD	USART3_CK					
81	I/O	OK	FSMC_D2	PD0		FSMC_D2	CAN1_RX									
82	I/O	OK	FSMC_D3	PD1		FSMC_D3	CAN1_TX									
83	I/O	OK	SDIO_CMD	PD2		TIM3_ETR	UART5_RX	SDIO_CMD	DCMI_D11							
84	I/O	OK		PD3		FSMC_CLK	USART2_CTS									
85	I/O	OK	FSMC_NOE	PD4		FSMC_NOE	USART2_RTS									
86	I/O	OK	FSMC_NWE	PD5		FSMC_NWE	USART2_TX									
87	I/O	OK	CTP_INT	PD6		FSMC_NWAIT	USART2_RX									
88	I/O	OK	FSMC_NE1	PD7		USART2_CK	FSMC_NE1	FSMC_NCE2								
89	I/O	OK	PB3 (JTDO/ TRACESWO)	PB3 (JTDO/ TRACESWO)		JTDO	TRACESWO	SPI3_SCK	I2S3_CK	TIM2_CH2	SPI1_SCK					
90	I/O	OK	PB4 (NJTRST)	PB4 (NJTRST)		NJTRST	SPI3_MISO	TIM3_CH1	SPI1_MISO	I2S3ext_SD						
91	I/O	OK	CAN2_RX	PB5		I2C1_SMBA	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	TIM3_CH2	SPI1_MOSI	SPI3_MOSI	DCMI_D10	I2S3_SD		
92	I/O	OK	CAN2_TX	PB6		I2C1_SCL	TIM4_CH1	CAN2_TX	DCMI_D5	USART1_TX						
93	I/O	OK		PB7		I2C1_SDA	FSMC_NL	DCMI_VSYNC	USART1_RX	TIM4_CH2						
94	I		BOOT0	BOOT0												VPP
95	I/O	OK	I2C1_SCL	PB8		TIM4_CH3	SDIO_D4	TIM10_CH1	DCMI_D6	ETH_MII_TXD3	I2C1_SCL	CAN1_RX				
96	I/O	OK	I2C1_SDA	PB9		SPI2_NSS	I2S2_WS	TIM4_CH4	TIM11_CH1	SDIO_D5	DCMI_D7	I2C1_SDA	CAN1_TX			
97	I/O	OK		PE0		TIM4_ETR	FSMC_NBL0	DCMI_D2								
98	I/O	OK		PE1		FSMC_NBL1	DCMI_D3									
99	S		Vss_3	Vss_3												
100	S		Vdd_3	Vdd_3												