Notes

Calculations

Important Note

Software Note

Mounting Note

SPI_UI_nCS_P — R10 100R — SPI_UI_nCS_N

SPI_UI_SCK_P — R11 100R — SPI_UI_SCK_N

SPI_UI_MOSI_P — R12 100R — SPI_UI_MOSI_N

IC3A

Bank 1 2.5V

C2	IO/DIFFIO_L1p	IO/VREFB1N0	F3	
D1	IO/DIFFIO_L2n	IO1_0	D4	
SPI_UI_MOSI_P F2	IO/DIFFIO_L3p	IO1_1	E5	TD4
SPI_UI_MOSI_N F1	IO/DIFFIO_L3n	IO1_2	F5	TE5
SPI_UI_MISO_P G2	IO/DIFFIO_L4p	IO1_3	B1	
SPI_UI_MISO_N G1	IO/DIFFIO_L4n	IO1_4	G5	TB1
	CLK1/DIFFCLK_0n		E1	

EP4CE6F17C8N — GND

IC3B

Bank 2 2.5V

SPI_UI_SCK_P J2	IO/DIFFIO_L5p	IO/VREFB2N0	L3	
SPI_UI_SCK_N J1	IO/DIFFIO_L5n			
K6	IO/DIFFIO_L6p	IO2_0	J6	
L6	IO/DIFFIO_L6n	IO2_1	R1	
SPI_UI_nCS_P K2	IO/DIFFIO_L7p			
SPI_UI_nCS_N K1	IO/DIFFIO_L7n			
L2	IO/DIFFIO_L8p			
L1	IO/DIFFIO_L8n	IO/RUP1	K5	
N2	IO/DIFFIO_L9p	IO/RDN1	L4	
N1	IO/DIFFIO_L9n			
P2	IO/DIFFIO_L10p	CLK2/DIFFCLK_1p	M2	
P1	IO/DIFFIO_L10n	CLK3/DIFFCLK_1n	M1	

TP2, TP1 — EP4CE6F17C8N — GND

IC3C

Bank 3 3.3V

N3	IO/DIFFIO_B1p	IO/VREFB3N0	P6	TP6
SPI1_SCK P3	IO/DIFFIO_B1n			
SPI1_MOSI R3	IO/DIFFIO_B2p	IO3_0	T2	FPGA_nCS
SPI1_MISO T3	IO/DIFFIO_B2n	IO3_1	M6	
N5	IO/DIFFIO_B4p	IO3_2	L7	
I2C_SDA N6	IO/DIFFIO_B4n			
DIP_SW0 M7	IO/DIFFIO_B5p			
K8	IO/DIFFIO_B5n			
R5	IO/DIFFIO_B6p			
FPGA_INTERRUPT T5	IO/DIFFIO_B6n			
DEBUG_0 R6	IO/DIFFIO_B7p			
DEBUG_1 T6	IO/DIFFIO_B7n			
I/O_3E_P R7	IO/DIFFIO_B8p			
I/O_3E_N T7	IO/DIFFIO_B8n			
L8	IO/DIFFIO_B9p			
DIP_SW1 M8	IO/DIFFIO_B9n			
I/O_3D_P N8	IO/DIFFIO_B10p			
I/O_3D_N P8	IO/DIFFIO_B10n			
I/O_3A_P R8	IO/DIFFIO_B11p	IO/PLL1_CLKOUTn	R4	
I/O_3A_N T8	IO/DIFFIO_B11n	IO/PLL1_CLKOUTp	T4	

EP4CE6F17C8N

IC3D

Bank 4 3.3V

I/O_2E_P R9	IO/DIFFIO_B12p	IO/VREFB4N0	P11	
I/O_2E_N T9	IO/DIFFIO_B12n			
K9	IO/DIFFIO_B13p	IO4_0	P9	
L9	IO/DIFFIO_B13n	IO4_1	R14	SPI_AD_CS
I/O_2B M9	IO/DIFFIO_B14p			
I/O_3B N9	IO/DIFFIO_B14n	IO/RUP2	M10	I/O_1B
I/O_2D_P R10	IO/DIFFIO_B15p	IO/RDN2	N11	
I/O_2D_N T10	IO/DIFFIO_B15n			
I/O_2A_P R11	IO/DIFFIO_B16p			
I/O_2A_N T11	IO/DIFFIO_B16n			
I/O_1E_P R12	IO/DIFFIO_B17p			
I/O_1E_N T12	IO/DIFFIO_B17n			
K10	IO/DIFFIO_B18p			
I2C_SCL L10	IO/DIFFIO_B18n			
I/O_1D_P R13	IO/DIFFIO_B19p			
I/O_1D_N T13	IO/DIFFIO_B19n			
I/O_1A_P T14	IO/DIFFIO_B20p			
I/O_1A_N T15	IO/DIFFIO_B20n			
SPI_AD_MOSI P14	IO/DIFFIO_B21p			
L11	IO/DIFFIO_B21n			
M11	IO/DIFFIO_B22p			
SPI_AD_SCLK N12	IO/DIFFIO_B22n			

EP4CE6F17C8N

IC3E

Bank 5 3.3V

SDRAM_A0 P16	IO/DIFFIO_R11n	IO/VREFB5N0	L14	SDRAM_DQM0
SDRAM_A1 R16	IO/DIFFIO_R11p			
SDRAM_A10 N16	IO/DIFFIO_R10n	IO5_0	N13	SDRAM_nCS
SDRAM_BA1 N15	IO/DIFFIO_R10p	IO5_1	M12	
SDRAM_nRAS L16	IO/DIFFIO_R9n	IO5_2	L12	TL12
SDRAM_nCAS L15	IO/DIFFIO_R9p	IO5_3	K12	SDRAM_D5
SDRAM_D7 K16	IO/DIFFIO_R8n	IO5_4	K11	
SDRAM_D6 K15	IO/DIFFIO_R8p	IO5_5	L13	SDRAM_nWE
SDRAM_D4 J16	IO/DIFFIO_R7n/DEV_OE	IO5_6	J11	
SDRAM_D3 J15	IO/DIFFIO_R7p/DEV_CLRn	IO5_7	J13	SDRAM_D0
SDRAM_D1 J14	IO/DIFFIO_R6n			
SDRAM_D2 J12	IO/DIFFIO_R6p	IO/RUP3	N14	SDRAM_BA0
		IO/RDN3	P15	SPI_AD_MISO
	CLK7/DIFFCLK_3n		M16	CLK_50M
	CLK6/DIFFCLK_3p		M15	

EP4CE6F17C8N

IC3F

Bank 6 3.3V

SDRAM_A2 G16	IO/DIFFIO_R4n/INIT_DONE	IO/VREFB6N0	F14	SDRAM_A6
SDRAM_A3 G15	IO/DIFFIO_R4p/CRC_ERROR			
SDRAM_A4 F16	IO/DIFFIO_R3n/nCEO	IO6_0	F13	SDRAM_A7
SDRAM_A5 F15	IO/DIFFIO_R3p/CLKUSR	IO6_1	B16	SDRAM_D8
SDRAM_A8 D16	IO/DIFFIO_R2n	IO6_2	G11	
SDRAM_A9 D15	IO/DIFFIO_R2p			
SDRAM_A11 C16	IO/DIFFIO_R1n	CLK4/DIFFCLK_2p	E15	
SDRAM_CKE C15	IO/DIFFIO_R1p	CLK5/DIFFCLK_2n	E16	

EP4CE6F17C8N — GND

IC3G

Bank 7 3.3V

SDRAM_DQM1 C14	IO/DIFFIO_T21n	IO/VREFB7N0	C11	I/O_4A_N
SDRAM_A12 D14	IO/DIFFIO_T21p			
I/O_4A_P D11	IO/DIFFIO_T20n	IO7_0	E9	I/O_4D_P
SDRAM_D11 D12	IO/DIFFIO_T20p			
SDRAM_D12 A13	IO/DIFFIO_T19n	IO/RUP4	E11	
SDRAM_D13 B13	IO/DIFFIO_T19p	IO/RDN4	E10	
SDRAM_D14 A12	IO/DIFFIO_T18n			
SDRAM_D15 B12	IO/DIFFIO_T18p			
I/O_4E_N A11	IO/DIFFIO_T17n			
I/O_4E_P B11	IO/DIFFIO_T17p			
I/O_4D_N F10	IO/DIFFIO_T16n			
F9	IO/DIFFIO_T16p			
I/O_4B F11	IO/DIFFIO_T15n			
SDRAM_D9 A15	IO/DIFFIO_T15p			
I/O_5A_N A10	IO/DIFFIO_T14n			
I/O_5A_P B10	IO/DIFFIO_T14p			
I/O_5B C9	IO/DIFFIO_T13n			
I/O_6A_P D9	IO/DIFFIO_T13p			
I/O_5D_N A9	IO/DIFFIO_T12n	IO/PLL2_CLKOUTn	A14	SDRAM_D10
I/O_5D_P B9	IO/DIFFIO_T12p	IO/PLL2_CLKOUTp	B14	R22 33R SDRAM_CLK

EP4CE6F17C8N

IC3H

Bank 8 3.3V

I/O_5E_N A8	IO/DIFFIO_T11n	IO/VREFB8N0	C6	
I/O_5E_P B8	IO/DIFFIO_T11p			
E8	IO/DIFFIO_T10n/DATA2	IO8_0	C8	I/O_6A_N
F8	IO/DIFFIO_T10p/DATA3	IO8_1	D8	I/O_6B
A7	IO/DIFFIO_T9n	IO8_2/DATA5	E7	
B7	IO/DIFFIO_T9p/DATA4	IO8_3/DATA6	E6	
F6	IO/DIFFIO_T8n			
F7	IO/DIFFIO_T8p			
I/O_6D_N A6	IO/DIFFIO_T7n			
I/O_6D_P B6	IO/DIFFIO_T7p			
TA5 A5	IO/DIFFIO_T6n/DATA7			
LED_2 A2	IO/DIFFIO_T5n			
LED_7 B5	IO/DIFFIO_T5p			
LED_6 A4	IO/DIFFIO_T4n			
LED_5 B4	IO/DIFFIO_T4p			
I/O_6E_N D5	IO/DIFFIO_T3n			
I/O_6E_P D6	IO/DIFFIO_T3p			
LED_4 A3	IO/DIFFIO_T2n			
LED_3 B3	IO/DIFFIO_T2p			
LED_1 C3	IO/DIFFIO_T1n			
LED_0 D3	IO/DIFFIO_T1p			

EP4CE6F17C8N

IC3J

Configuration

TCK H3	TCK	MSEL0	H13	
TMS J5	TMS	MSEL1	H12	
TDI H4	TDI	MSEL2	G12	
TDO J4	TDO			
SPI2_SCK H1	DCLK	ASDO	C1	
		nCSO	D2	
nSTATUS F4	nSTATUS	DATA0	H2	SPI2_MOSI
nCONFIG H5	nCONFIG			
J3	nCE	CONF_DONE	H14	CONF_DONE

EP4CE6F17C8N

VCCA — R48 nf — R49 0R — GND — GND

Passive Serial (PS) configuration.
R49: Standard POR Delay
R48: Fast POR Delay

VCCA — R40 1k — R41 10k — R42 10k — JTAG (TCK 1, TDO 3, TMS 5, TDI 9; 2, 4, 6, 7, 8, 10) Male — VCCA — GND — GND

I/O Connectors

3.3V — I/O_1 Male — GND

I/O_1A_P	1	2	I/O_1A_N
I/O_1B	3	4	ID_1
I/O_1D_P	5	6	I/O_1D_N
I/O_1E_P	7	8	I/O_1E_N
	9	10	
I/O_2A_P	11	12	I/O_2A_N
I/O_2B	13	14	ID_2
I/O_2D_P	15	16	I/O_2D_N
I/O_2E_P	17	18	I/O_2E_N
	19	20	
I/O_3A_P	21	22	I/O_3A_N
I/O_3B	23	24	ID_3
I/O_3D_P	25	26	I/O_3D_N
I/O_3E_P	27	28	I/O_3E_N
	29	30	

3.3V — I/O_2 Male — GND

I/O_4A_P	1	2	I/O_4A_N
I/O_4B	3	4	ID_4
I/O_4D_P	5	6	I/O_4D_N
I/O_4E_P	7	8	I/O_4E_N
	9	10	
I/O_5A_P	11	12	I/O_5A_N
I/O_5B	13	14	ID_5
I/O_5D_P	15	16	I/O_5D_N
I/O_5E_P	17	18	I/O_5E_N
	19	20	
I/O_6A_P	21	22	I/O_6A_N
I/O_6B	23	24	ID_6
I/O_6D_P	25	26	I/O_6D_N
I/O_6E_P	27	28	I/O_6E_N
	29	30	

Data Connector

Data — Male

SPI_UI_nCS_P	1	2	SPI_UI_nCS_N
SPI_UI_SCK_P	3	4	SPI_UI_SCK_N
SPI_UI_MISO_P	5	6	SPI_UI_MISO_N
SPI_UI_MOSI_P	7	8	SPI_UI_MOSI_N

Title: Data Processor Board		
Size: A3	Number: 1	Revision: Rev 1
Date: 6/16/2015	Time: 10:15:20 PM	Sheet 1 of 4
File: Serial Monitor Data Processor Board Schematic.SchDoc		

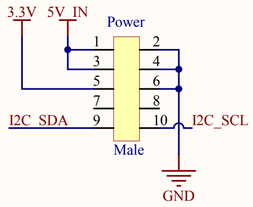
Notes

Calculations

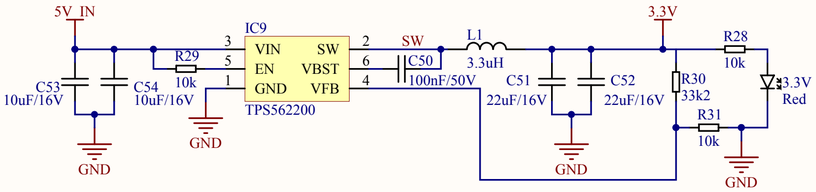
Important Note

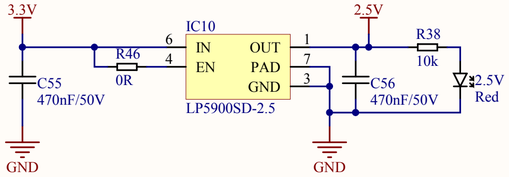
Software Note

Mounting Note



3.3V, 2A

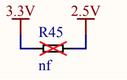




2.5V, 150mA

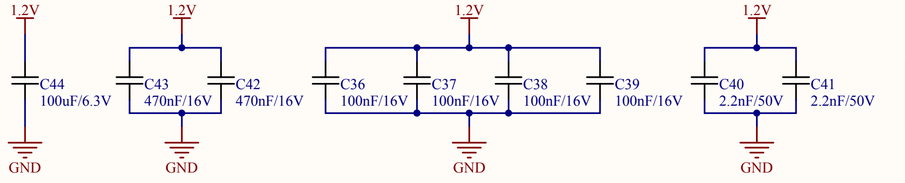
1.2V, 1.5A

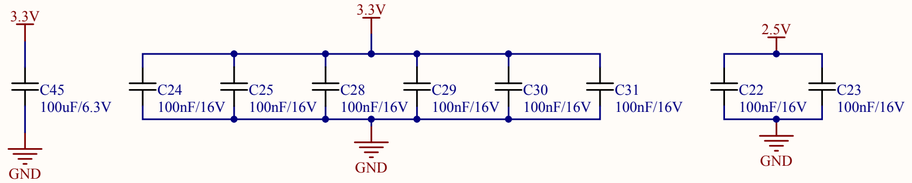
Vout = Vadj(1+R1/R2)+Iadj*R1
Vadj = 0.605 V
Iadj = 50-750 nA
R1=R2=4k7 -> 1.21 V

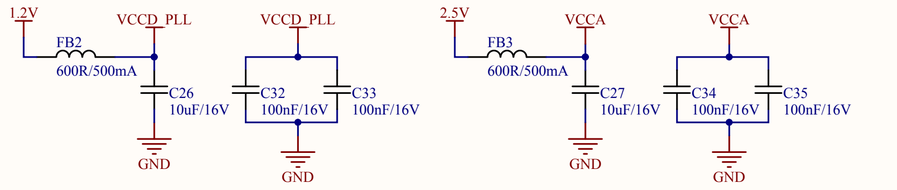


Do NOT mount R45 as standard! This jumper is there in case you want to power the whole board using 2.5V. To do this you need to:
- Change R30 to 22.6k to get 2.5V output of TPS562200
- Disable LP5900SD-2.5 by removing R46
- Mount 0R jumper on R45
- ADC108S022 will not work on 2.5V and has to be removed if mounted
- The standard SDRAM has to be replaced with a 2.5V capable one or be removed
- The FLASH for the config MCU has to be replaced with a 2.5V capable one or be removed
- The micro SD-card will probably not work on 2.5V as it's specified for 2.7-3.6V

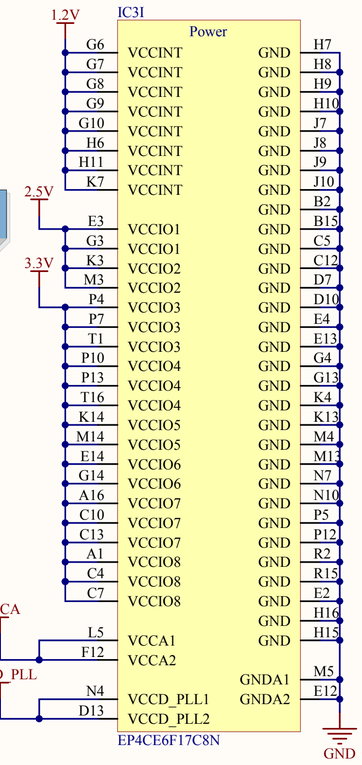
Note that by doing this VCCA will be powered by a switching regulator instead of a linear.







Bank 1 and 2 have LVDS signals so VCCIO need to be 2.5V



Title: Power		
Size: A3	Number: 2	Revision: Rev 1
Date: 6/16/2015	Time: 10:15:20 PM	Sheet 2 of 4
File: Power Schematic.SchDoc		

Notes

Calculations

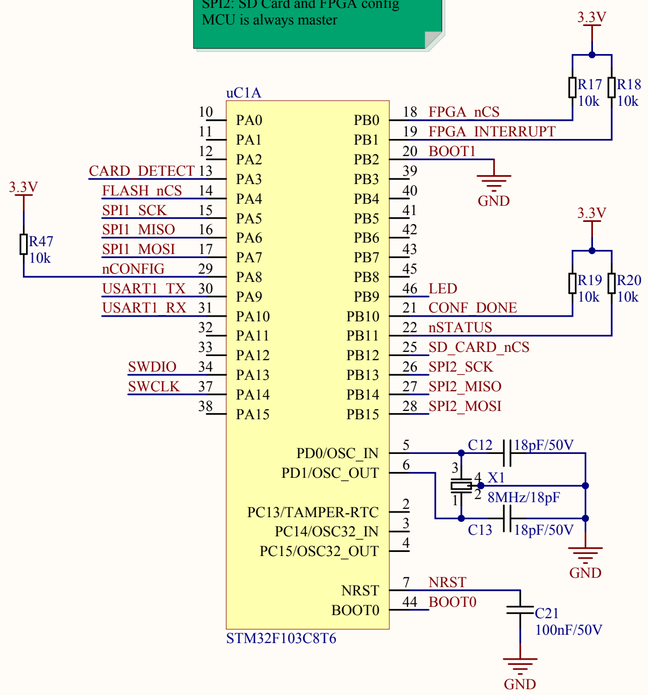
Important Note

Software Note

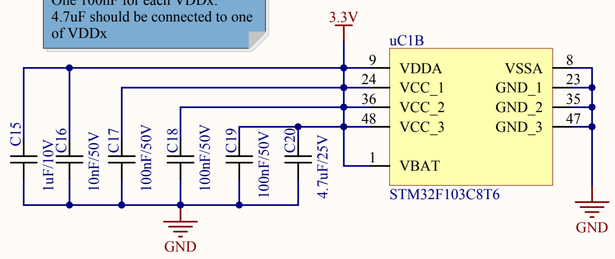
Mounting Note

Config MCU

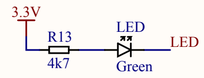
SPI1: FLASH and FPGA data
SPI2: SD Card and FPGA config
MCU is always master



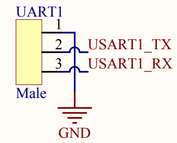
One 100nF for each VDDx.
4.7uF should be connected to one of VDDx



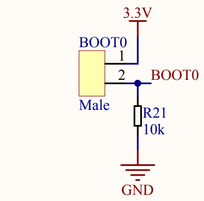
LED



UART1



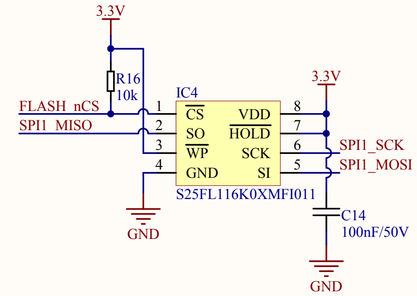
BOOT



Boot modes:

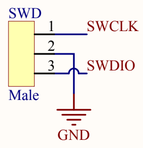
BOOT1	BOOT0	Mode
x	0	Flash
0	1	ST Bootloader

FLASH

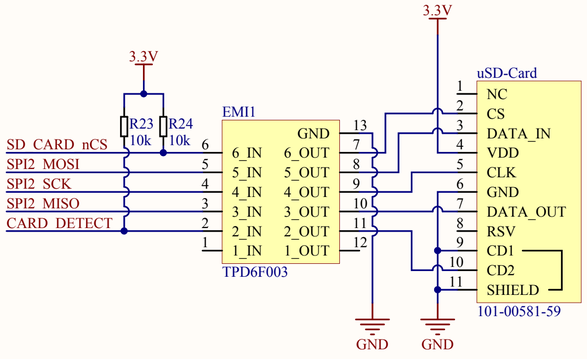


FPGA (EP4CE6) requires 2 944 088 bits -> in 16Mbit flash we can fit 5 configuration files

DEBUG



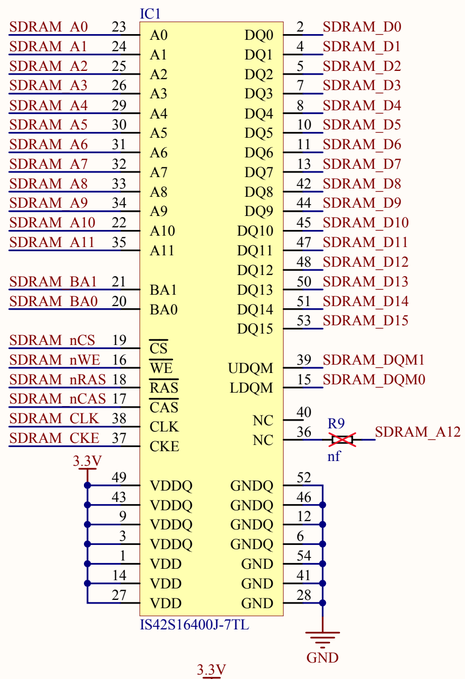
MicroSD-Card

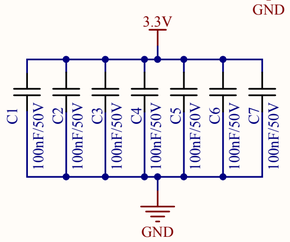


Title: Config MCU		
Size: A3	Number: 3	Revision: Rev 1
Date: 6/16/2015	Time: 10:15:21 PM	Sheet 3 of 4
File: Config MCU Schematic.SchDoc		

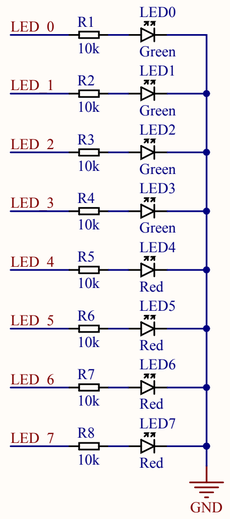
Notes
Calculations
Important Note
Software Note
Mounting Note

SDRAM

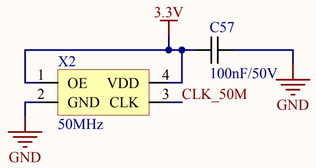




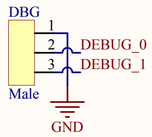
LEDs



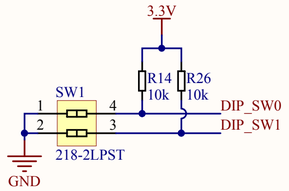
Clock



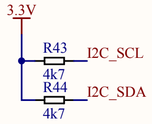
Debug



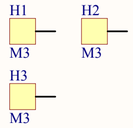
DIP Switch



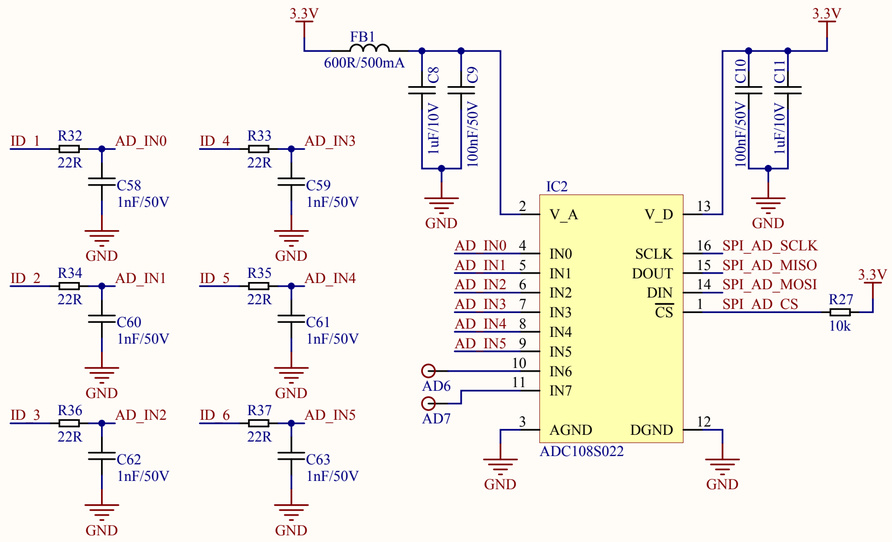
I2C



Mechanical



ADC



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Size: A3	Number: 4	Revision: Rev 1
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File: Peripherals Schematic.SchDoc		