7. Pin Function (PFC/GPIO)

7.1 Overview Tổng quan

Bộ điều khiển chức năng chân (PFC) là một mô-đun bao gồm các thanh ghi để chọn chức năng của các chân ghép kênhvà điều khiển điện trở kéo lên trên mỗi chân LSI.

The pin function controller (PFC) is a module that consists of registers for selecting the function of the multiplexed pins and controlling the pull-up resistor on each LSI pin.

(There are 10 port groups. GPIO group 0-7, System group 0-1.)

(Có 10 nhóm cổng. Nhóm GPIO 0-7, Nhóm hệ thống 0-1.)

7.1.1 Features Đặc trưng

Cài đặt các chức năng chân ghép kênh cho các chân LSI

- Setting multiplexed pin functions for LSI pins

  Function of the R-Car S4 pin selectable by setting the registers in the PFC module

  (The function of the LSI pin can be selected by the GPIO/peripheral function select registers 0 to 9 (GPSR0 to GPSR9) and peripheral function select registers 0 to 3 (IPSR0 to IPSR3) in each port group of each PFC module. For details, see sections 7.2.4, GPIO/Peripheral Function Select Register 0-9 (GPSRn) through 7.2.5, Peripheral Function Select Register 0-3 (IPiSRn i = 0 - 3).)
- Bus Domain access: Please refer section 15 – AXI-bus
- DRV control for each LSI pin

  DRV control resistors can control the driving abilities of pins.

  DRV control resistors on each LSI pin can be controlled by setting the registers in the PFC module. (Selection is handled by the output drive select register (DRVCTRL0-3). For details, see sections 7.2.6, DRV Control Register 0-3 (DRViCTRLn i = 0 - 1 / DRVjCTRLSYS j = 0 - 1). POWER Condition control for each LSI pin.

  POWER Condition control registers must be set according to IO voltage level that is supplied to the pin.

  POWER Condition control resistors on each LSI pin can be controlled by setting the registers in the PFC module. (Selection is handled by the IO voltage level select registers POWER Condition. For details, see sections 7.2.7, POWER Condition Control Register (POCn).
- TDSEL control for each LSI pin

  TDSEL control registers can control the driving abilities of pins in use for the SDHI.

  TDSEL control resistors on each LSI pin can be controlled by setting the registers in the PFC module. (Selection is handled by the return path for SDHI clock drive select register TDSEL0-1. For details, see sections 7.2.11, TDSEL Control Register 0-1 (TDiSELn).
- Pull-up/down control for each LSI pin.

  PUEN registers can on/off control of the pull resistors.

  On/off of the pull resistors on each LSI pin can be controlled by setting the registers in the PFC module.

  (Selection is handled by the Pull-on/off select registers PUEN. For details, see sections 7.2.8, LSI pin pull-enable register (PUENn).

  PUD registers can pull-up/pull-down control of the pull resistors.

  Pull-up/Pull-down control resistors on each LSI pin can be controlled by setting the registers in the PFC module.

  (Selection is handled by the Pull-up/down select registers PUD. For details, see sections 7.2.9, LSI pin pull-up/down control Register (PUDn / PUDSYS)).
- Module selection

  Module Select Register can select the group for multiple LSI pins with multiplexed pin functions.

  Enable and disable the functions of R-Car S4 LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module.

  (Selection is handled by the module select register (MODSELn). For details, see sections 7.2.10, Module Select Register (MODSELn).
- Notes on configuring multiplexed pin functions

  The multiplexed LSI pins (MODSELn, GPSRn, IPiSRn i = 0 - 3) must be set in the initial sequence (*).

  Switching multiplexed LSI pins during operation is not guaranteed.

  * : The initial sequence is Appendix B.(3)

- R-Car S4 product have up to ten GPIO blocks, each of which is a functional block that supports up to 32 port pins for general input/output and interrupt input. (A maximum of 233 ports pins for R-Car S4 in total can be used. Note that the port pins are multiplexed.) When the relevant register is written to, a signal is output via the corresponding general output port pin. When a signal is input via the general input port pin, the corresponding register indicates the value of the input signal; specifically, when an interrupt is input via a general port pin, the relevant register indicates that it is currently receiving an interrupt input, and an interrupt is also requested to the CPU core via the interrupt control block. The functions (modes) can be assigned to each port pin as desired by some setting the corresponding registers. It is also possible to select the signal polarity (positive or negative logic) and the interrupt detection condition (one edge/both edge or level) for each port. In this LSI, general output data mode of GPIO can be set in normal mode (outputting data as normal) or high/low level data output mode. Particularly, a filtering function to prevent external chattering is also available for port pins 0 to 3 in input modes for each GPIO block.
- In R-CarS4 product, to keep safe operating state (Port Safe State) in case of failure, and then stop it. Furthermore, because it is supposed to control the domain with S4, we handle failure processing for each domain. Therefore, PFC module receive fault information from ECM and make Pin for Port Safe State for each domain.

  Type of Port Safe State:

  1.It follows the state of each pin PRESET_N = Low. (output enable and input enable off)

  2.HiZ: Output enable and input enable off, Pull enable off, Don't care pull up/down

  3.PD: Output enable and input enable off, Pull enable on, Pull-Down

  4.PU: Output enable and input enable off, Pull enable on, Pull-Up

  Registers (PS0SRn , PS1SRn) that select 4 types of Port Safe State with 2 bits. For detail, see section 7.2.48, Port Safe state Select Register 0-1 (PSiSRn i = 0 - 1)

  Provide a register (PSER) to enable / disable this register. For detail, see section 7.2.49, Port Safe state Enable Register (PSERn)
- ICUMHB Select Function

  Target pins: GP4_11, GP4_14, GP4_15, GP4_16.

  The ICUMHB Select Function takes highest priority in port functions to control output value of these target pins.

  For more details how to use the ICUMHB function, refer to Security User's Manual: Hardware.
- PRESETOUT1# Function

  PRESETOUT1# has RESETOUT function to handshake with external device. To support this, PRESETOUT1# will drive out low level to external device during and after reset which is effective for any kind of resets (except DeepSTOP Reset, Module Reset and JTAG Reset).

  This function is realized by having a special reset value of INOUTSEL6[31] which are inverted in contrast to the others.

  PRESETOUT1# keeps driving out low level until the related registers are changed by user program.
- Module clock

  Module clock is CPϕ.

  In PFC1 and PFC_SYS1, CPϕ represents CLK_LSB.

7.1.2 Block Diagram

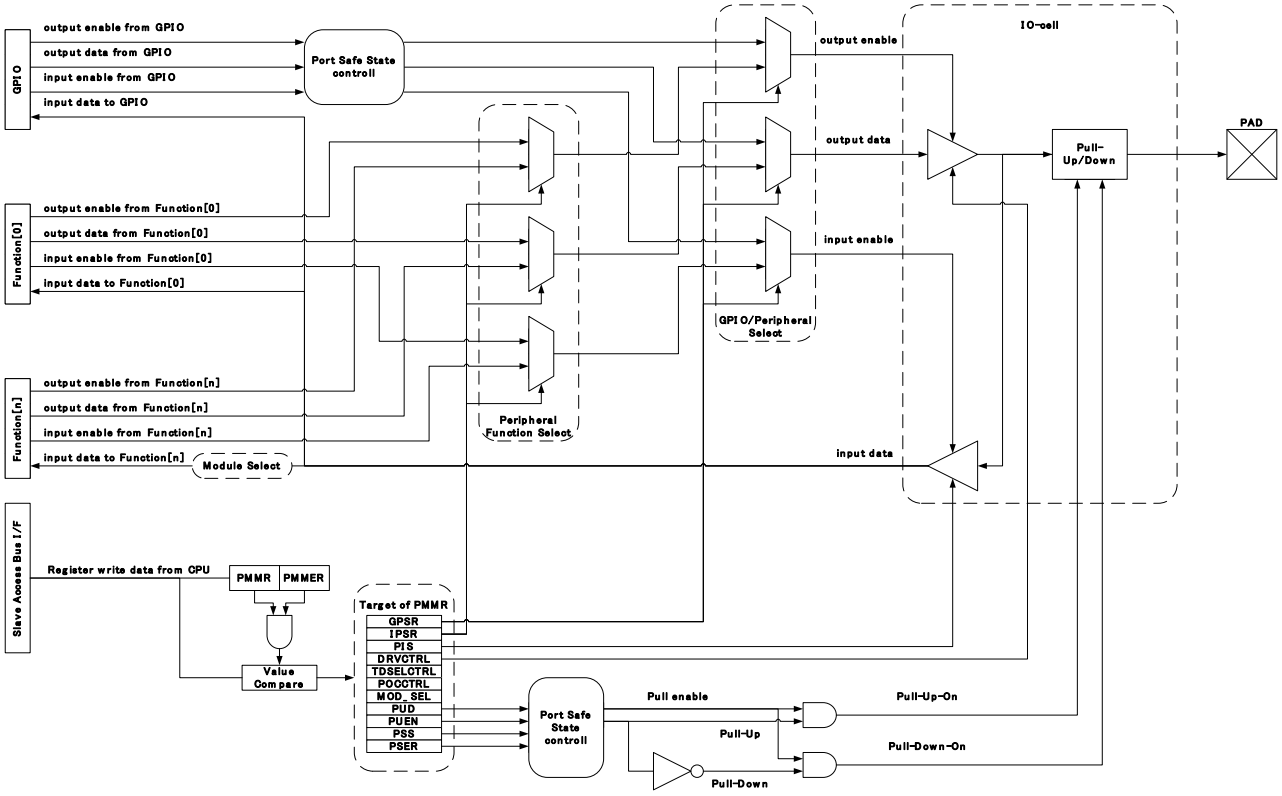


Figure 7.1 PFC Block Configuration

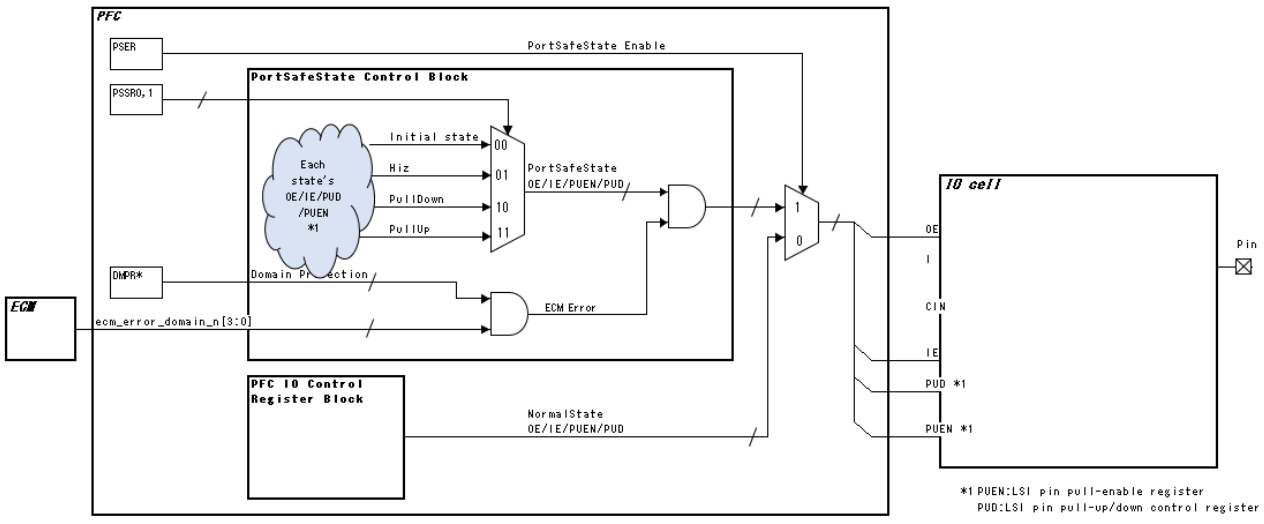


Figure 7.2 Port Safe State block

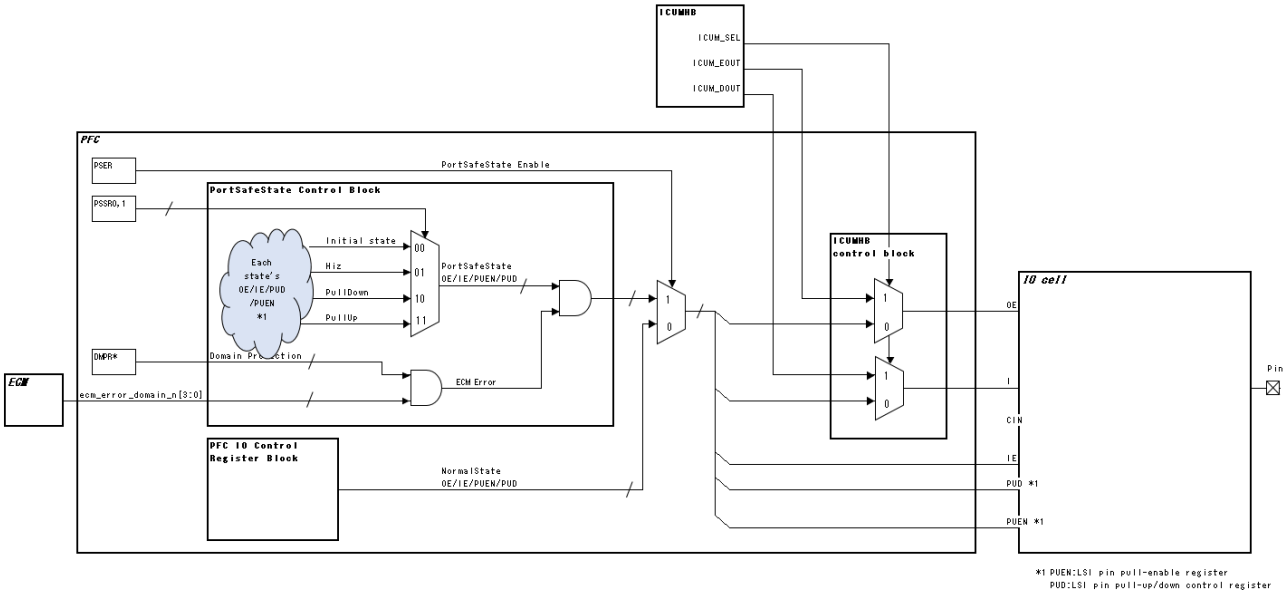


Figure 7.3 Block Diagram of ICUMHB Select Function

7.1.3 External Pins

Table 7.1 shows the pin configuration of the GPIO.

Table 7.1 Pin Configuration

	I/O	Function	Description
GP0_00 to GP7_31	I/O	IO/interrupt input ports	General input/output and interrupt input

Pin name	GPIO	Pin name	GPIO	Pin name	GPIO	Pin name	GPIO
SCIF_CLK	GP0_00	GP1_00	GP1_00	RPC_INT#	GP2_00	TSN1_MDIO	GP3_00
HSCK0	GP0_01	GP1_01	GP1_01	RPC_WP#	GP2_01	TSN2_MDIO	GP3_01
HRX0	GP0_02	GP1_02	GP1_02	RPC_RESET#	GP2_02	TSN0_MDIO	GP3_02
HTX0	GP0_03	GP1_03	GP1_03	QSPI1_SSL	GP2_03	TSN2_MDC	GP3_03
HCTS0#	GP0_04	GP1_04	GP1_04	QSPI1_IO3	GP2_04	TSN0_MDC	GP3_04
HRTS0#	GP0_05	GP1_05	GP1_05	QSPI1_MISO_IO1	GP2_05	TSN1_MDC	GP3_05
RX0	GP0_06	GP1_06	GP1_06	QSPI1_IO2	GP2_06	TSN1_LINK	GP3_06
TX0	GP0_07	GP1_07	GP1_07	QSPI1_MOSI_IO0	GP2_07	TSN2_LINK	GP3_07
SCK0	GP0_08	GP1_08	GP1_08	QSPI1_SPCLK	GP2_08	TSN0_LINK	GP3_08
RTS0#	GP0_09	GP1_09	GP1_09	QSPI0_MOSI_IO0	GP2_09	TSN2_PHY_INT	GP3_09
CTS0#	GP0_10	GP1_10	GP1_10	QSPI0_SPCLK	GP2_10	TSN0_PHY_INT	GP3_10
MSIOF0_SYNC	GP0_11	GP1_11	GP1_11	QSPI0_IO2	GP2_11	TSN1_PHY_INT	GP3_11
MSIOF0_RXD	GP0_12	MMC_SD_CLK	GP1_12	QSPI0_MISO_IO1	GP2_12	TSN0_MAGIC	GP3_12
MSIOF0_TXD	GP0_13	MMC_SD_D0	GP1_13	QSPI0_SSL	GP2_13	TSN1_AVTP_PPS	GP3_13
MSIOF0_SCK	GP0_14	MMC_SD_D1	GP1_14	QSPI0_IO3	GP2_14	TSN1_AVTP_MATCH	GP3_14
MSIOF0_SS1	GP0_15	MMC_SD_D2	GP1_15	PCIE0_CLKREQ#	GP2_15	TSN1_AVTP_CAPTURE	GP3_15
MSIOF0_SS2	GP0_16	MMC_SD_D3	GP1_16	PCIE1_CLKREQ#	GP2_16	TSN0_AVTP_PPS	GP3_16
IRQ0	GP0_17	MMC_D5	GP1_17			TSN0_AVTP_MATCH	GP3_17
IRQ1	GP0_18	MMC_D4	GP1_18			TSN0_AVTP_CAPTURE	GP3_18
IRQ2	GP0_19	MMC_D6	GP1_19				
IRQ3	GP0_20	MMC_DS	GP1_20				
		MMC_D7	GP1_21				
		MMC_SD_CMD	GP1_22				
		SD_CD	GP1_23				
		SD_WP	GP1_24				

Pin name	GPIO	Pin name	GPIO	Pin name	GPIO	Pin name	GPIO
GP4_00	GP4_00	RIIC0SCL	GP5_00	RLIN37TX	GP6_00	CAN0TX	GP7_00
GP4_01	GP4_01	RIIC0SDA	GP5_01	RLIN37RX/INTP23	GP6_01	CAN0RX/INTP0	GP7_01
GP4_02	GP4_02	ETNB0MD	GP5_02	RLIN36TX	GP6_02	CAN1TX	GP7_02
GP4_03	GP4_03	ETNB0WOL	GP5_03	RLIN36RX/INTP22	GP6_03	CAN1RX/INTP1	GP7_03
GP4_04	GP4_04	ETNB0LINKSTA	GP5_04	RLIN35TX	GP6_04	CAN2TX	GP7_04
GP4_05	GP4_05	ETNB0MDC	GP5_05	RLIN35RX/INTP21	GP6_05	CAN2RX/INTP2	GP7_05
GP4_06	GP4_06	ETNB0RXER	GP5_06	RLIN34TX	GP6_06	CAN3TX	GP7_06
GP4_07	GP4_07	ETNB0RXD3	GP5_07	RLIN34RX/INTP20	GP6_07	CAN3RX/INTP3	GP7_07
GP4_08	GP4_08	ETNB0RXD1	GP5_08	RLIN33TX	GP6_08	CAN4TX	GP7_08
GP4_09	GP4_09	ETNB0RXD2	GP5_09	RLIN33RX/INTP19	GP6_09	CAN4RX/INTP4	GP7_09
GP4_10	GP4_10	ETNB0RXDV	GP5_10	RLIN32TX	GP6_10	CAN5TX	GP7_10
GP4_11	GP4_11	ETNB0RXD0	GP5_11	RLIN32RX/INTP18	GP6_11	CAN5RX/INTP5	GP7_11
GP4_12	GP4_12	ETNB0RXCLK	GP5_12	RLIN31TX	GP6_12	CAN6TX	GP7_12
GP4_13	GP4_13	ETNB0TXER	GP5_13	RLIN31RX/INTP17	GP6_13	CAN6RX/INTP6	GP7_13
GP4_14	GP4_14	ETNB0TXD3	GP5_14	RLIN30TX	GP6_14	CAN7TX	GP7_14
GP4_15	GP4_15	ETNB0TXCLK	GP5_15	RLIN30RX/INTP16	GP6_15	CAN7RX/INTP7	GP7_15
GP4_16	GP4_16	ETNB0TXD1	GP5_16	INTP37	GP6_16	CAN8TX	GP7_16
GP4_17	GP4_17	ETNB0TXD2	GP5_17	INTP36	GP6_17	CAN8RX/INTP8	GP7_17
GP4_18	GP4_18	ETNB0TXEN	GP5_18	INTP35	GP6_18	CAN9TX	GP7_18
GP4_19	GP4_19	ETNB0TXD0	GP5_19	INTP34	GP6_19	CAN9RX/INTP9	GP7_19
MSPI0SC	GP4_20			INTP33	GP6_20	CAN10TX	GP7_20
MSPI0SI	GP4_21			INTP32	GP6_21	CAN10RX/INTP10	GP7_21
MSPI0SO/MSPI0DCS	GP4_22			NMI1	GP6_22	CAN11TX	GP7_22
MSPI0CSS1	GP4_23			—	—	CAN11RX/INTP11	GP7_23
MSPI0CSS0	GP4_24			—	—	CAN12TX	GP7_24
MSPI1SI	GP4_25			—	—	CAN12RX/INTP12	GP7_25
MSPI1SO/MSPI1DCS	GP4_26			—	—	CAN13TX	GP7_26
MSPI1CSS0	GP4_27			—	—	CAN13RX/INTP13	GP7_27
MSPI1SC	GP4_28			—	—	CAN14TX	GP7_28
MSPI1CSS2	GP4_29			—	—	CAN14RX/INTP14	GP7_29
MSPI1CSS1	GP4_30			—	—	CAN15TX	GP7_30
				PRESETOUT1#	GP6_31	CAN15RX/INTP15	GP7_31

7.1.4 Register Configuration

All the registers in the PFC are mapped into the APB bus space. Table 7.2 shows the configuration of the registers provided in the PFC. Details on each register in the PFC are given in sections 7.2.

The register configurations of R/W registers area, SET registers area and CLR registers area in GPIO group 0 to 7 are the same. Also, the register configurations of R/W registers area, SET registers area and CLR registers area in System group are tha same.

Table 7.2 Configuration of Registers in PFC

	Bus Domain	Group	Registers Area	Access Type	Address
	Bus Domain 0 (APS0)	GPIO Group 0	R/W registers area	Read or Write	H'E605 0000 to H'E605 01FF
			SET register area	Set	H'E605 0200 to H'E605 03FF
			CLR register area	Clear	H'E605 0400 to H'E605 05FF
			Reserved	—	H'E605 0600 to H'E605 07FF
		GPIO Group 1	R/W registers area	Read or Write	H'E605 0800 to H'E605 09FF
			SET register area	Set	H'E605 0A00 to H'E605 0BFF
			CLR register area	Clear	H'E605 0C00 to H'E605 0DFF
			Reserved	—	H'E605 0E00 to H'E605 0FFF
		GPIO Group 2	R/W registers area	Read or Write	H'E605 1000 to H'E605 11FF
			SET register area	Set	H'E605 1200 to H'E605 13FF
			CLR register area	Clear	H'E605 1400 to H'E605 15FF
			Reserved	—	H'E605 1600 to H'E605 17FF
		GPIO Group 3	R/W registers area	Read or Write	H'E605 1800 to H'E605 19FF
			SET register area	Set	H'E605 1A00 to H'E605 1BFF
			CLR register area	Clear	H'E605 1C00 to H'E605 1DFF
			Reserved	—	H'E605 1E00 to H'E605 1FFF
	Bus Domain 1 (APS0)	GPIO Group 0	R/W registers area	Read or Write	H'E605 2000 to H'E605 21FF
			SET register area	Set	H'E605 2200 to H'E605 23FF
			CLR register area	Clear	H'E605 2400 to H'E605 25FF
			Reserved	—	H'E605 2600 to H'E605 27FF
		GPIO Group 1	R/W registers area	Read or Write	H'E605 2800 to H'E605 29FF
			SET register area	Set	H'E605 2A00 to H'E605 2BFF
			CLR register area	Clear	H'E605 2C00 to H'E605 2DFF
			Reserved	—	H'E605 2E00 to H'E605 2FFF
		GPIO Group 2	R/W registers area	Read or Write	H'E605 3000 to H'E605 31FF
			SET register area	Set	H'E605 3200 to H'E605 33FF
			CLR register area	Clear	H'E605 3400 to H'E605 35FF
			Reserved	—	H'E605 3600 to H'E605 37FF
		GPIO Group 3	R/W registers area	Read or Write	H'E605 3800 to H'E605 39FF
			SET register area	Set	H'E605 3A00 to H'E605 3BFF
			CLR register area	Clear	H'E605 3C00 to H'E605 3DFF
			Reserved	—	H'E605 3E00 to H'E605 3FFF
	Bus Domain 2 (APS0)	GPIO Group 0	R/W registers area	Read or Write	H'E605 4000 to H'E605 41FF
			SET register area	Set	H'E605 4200 to H'E605 43FF
			CLR register area	Clear	H'E605 4400 to H'E605 45FF
			Reserved	—	H'E605 4600 to H'E605 47FF
		GPIO Group 1	R/W registers area	Read or Write	H'E605 4800 to H'E605 49FF
			SET register area	Set	H'E605 4A00 to H'E605 4BFF
			CLR register area	Clear	H'E605 4C00 to H'E605 4DFF
			Reserved	—	H'E605 4E00 to H'E605 4FFF
		GPIO Group 2	R/W registers area	Read or Write	H'E605 5000 to H'E605 51FF
			SET register area	Set	H'E605 5200 to H'E605 53FF
			CLR register area	Clear	H'E605 5400 to H'E605 55FF
			Reserved	—	H'E605 5600 to H'E605 57FF
		GPIO Group 3	R/W registers area	Read or Write	H'E605 5800 to H'E605 59FF
			SET register area	Set	H'E605 5A00 to H'E605 5BFF
			CLR register area	Clear	H'E605 5C00 to H'E605 5DFF
			Reserved	—	H'E605 5E00 to H'E605 5FFF
	Bus Domain 3 (APS0)	GPIO Group 0	R/W registers area	Read or Write	H'E605 6000 to H'E605 61FF
			SET register area	Set	H'E605 6200 to H'E605 63FF
			CLR register area	Clear	H'E605 6400 to H'E605 65FF
			Reserved	—	H'E605 6600 to H'E605 67FF
		GPIO Group 1	R/W registers area	Read or Write	H'E605 6800 to H'E605 69FF
			SET register area	Set	H'E605 6A00 to H'E605 6BFF
			CLR register area	Clear	H'E605 6C00 to H'E605 6DFF
			Reserved	—	H'E605 6E00 to H'E605 6FFF
		GPIO Group 2	R/W registers area	Read or Write	H'E605 7000 to H'E605 71FF
			SET register area	Set	H'E605 7200 to H'E605 73FF

	Bus Domain	Group	Registers Area	Access Type	Address
			CLR register area	Clear	H'E605 7400 to H'E605 75FF
			Reserved	—	H'E605 7600 to H'E605 77FF
		GPIO Group 3	R/W registers area	Read or Write	H'E605 7800 to H'E605 79FF
			SET register area	Set	H'E605 7A00 to H'E605 7BFF
			CLR register area	Clear	H'E605 7C00 to H'E605 7DFF
			Reserved	—	H'E605 7E00 to H'E605 7FFF
	Bus Domain 0 (P-Bus)	GPIO Group 4	R/W registers area	Read or Write	H'FFD9 0000 to H'FFD9 01FF
			SET register area	Set	H'FFD9 0200 to H'FFD9 03FF
			CLR register area	Clear	H'FFD9 0400 to H'FFD9 05FF
			Reserved	—	H'FFD9 0600 to H'FFD9 07FF
		GPIO Group 5	R/W registers area	Read or Write	H'FFD9 0800 to H'FFD9 09FF
			SET register area	Set	H'FFD9 0A00 to H'FFD9 0BFF
			CLR register area	Clear	H'FFD9 0C00 to H'FFD9 0DFF
			Reserved	—	H'FFD9 0E00 to H'FFD9 0FFF
		GPIO Group 6	R/W registers area	Read or Write	H'FFD9 1000 to H'FFD9 11FF
			SET register area	Set	H'FFD9 1200 to H'FFD9 13FF
			CLR register area	Clear	H'FFD9 1400 to H'FFD9 15FF
			Reserved	—	H'FFD9 1600 to H'FFD9 17FF
		GPIO Group 7	R/W registers area	Read or Write	H'FFD9 1800 to H'FFD9 19FF
			SET register area	Set	H'FFD9 1A00 to H'FFD9 1BFF
			CLR register area	Clear	H'FFD9 1C00 to H'FFD9 1DFF
			Reserved	—	H'FFD9 1E00 to H'FFD9 1FFF
	Bus Domain 0 (APS0)	System Group 0 [for PRESETOUT#, DCURDY#/LPDCLKOUT, DCUTDO/LPDO, DCUTMS]	R/W registers area	Read or Write	H'E607 8000 to H'E607 81FF
			SET register area	Set	H'E607 8200 to H'E607 83FF
			CLR register area	Clear	H'E607 8400 to H'E607 85FF
			Reserved	—	H'E607 8600 to H'E607 87FF
	Bus Domain 0 (P-Bus)	System Group 1	R/W registers area	Read or Write	H'FFD9 8000 to H'FFD9 81FF
			SET register area	Set	H'FFD9 8200 to H'FFD9 83FF
			CLR register area	Clear	H'FFD9 8400 to H'FFD9 85FF
			Reserved	—	H'FFD9 8600 to H'FFD9 87FF

Table 7.3 Base address of Registers in PFC

Bus Domain	Group	Base address
Bus Domain 0 (APS0)	GPIO Group 0 (Port Group 0)	H'E605 0000
	GPIO Group 1 (Port Group 1)	H'E605 0800
	GPIO Group 2 (Port Group 2)	H'E605 1000
	GPIO Group 3 (Port Group 3)	H'E605 1800
Bus Domain 0 (P-Bus)	GPIO Group 4 (Port Group 4)	H'FFD9 0000
	GPIO Group 5 (Port Group 5)	H'FFD9 0800
	GPIO Group 6 (Port Group 6)	H'FFD9 1000
	GPIO Group 7 (Port Group 7)	H'FFD9 1800
Bus Domain 0 (APS0)	System Group 0	H'E607 8000
Bus Domain 0 (P-Bus)	System Group 1	H'FFD9 8000

Note : The related Bus of port groups, please confirm attachment document and each section.

Reference :

001_R-CarS4_Bus Architecture_r0p70.pptx (for both domain "Application domain" and "Control domain")

002_R-Car S4 series Address Map_r0p82.xlsx (for Application domain)

"Section 4 Address Space" in "158. Control Domain Parts" (for Control domain)

Table 7.4 Offset table

		R/W registers area	+H'200 SET registers area	+H'400 CLR registers area
	Bus Domain 0	Substitute from Table 7.3	+H'0200	+H'0400
+H'2000	Bus Domain 1	+H'2000	+H'2200	+H'2400
+H'4000	Bus Domain 2	+H'4000	+H'4200	+H'4400
+H'6000	Bus Domain 3	+H'6000	+H'6200	+H'6400

Attaching to this UM the excel files that have the register configuration information.
Refer to the following files too.

- R-CarS4_UM_007_PFC_GPIO_for_GP0_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP1_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP2_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP3_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP4_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP5_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP6_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP7_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_SYS0_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_SYS1_r0p70.xlsx

Table 7.5 Configuration of R/W Registers in GPIO group n

Name	Abbr.	R/W	Initial Value	Offset Address [lower 9bits]	Access Size [bits]	Condition
LSI Multiplexed Pin Setting Mask Register	PMMRn	R/W	H'0000 0000	H'000	32	-
LSI Multiplexed Pin Setting Mask Enable Register	PMMERn	R/W	H'0000 0001	H'004	32	-
Domain protection register 0	DM0PRn	R/W	H'FFFF FFFF	H'020	32	be able to write only from Bus Domain 0
Domain protection register 1	DM1PRn	R/W	H'0000 0000	H'024	32	be able to write only from Bus Domain 0
Domain protection register 2	DM2PRn	R/W	H'0000 0000	H'028	32	be able to write only from Bus Domain 0
Domain protection register 3	DM3PRn	R/W	H'0000 0000	H'02C	32	be able to write only from Bus Domain 0
GPIO/Peripheral Function Select register	GPSRn	R/W	Port group 0: H'001F FFFF Port group 1: H'01FF F07F Port group 2: H'0000 7FFF Port group 3: H'0007 FFFF Port group 4, 5, 7: H'0000 0000 Port group 6: H'8000 0000	H'040	32	-
Peripheral Function Select register 0	IP0SRn	R/W	Port group 0: H' 7777 7777 Port group 1: H'0777 7777 Port group 2, 3, 4, 5, 6, 7: H'0000 0000	H'060	32	-
Peripheral Function Select register 1	IP1SRn	R/W	Port group 0: H'7777 7777 Port group 1, 2, 3, 4, 5, 6, 7: H'0000 0000	H'064	32	-
Peripheral Function Select register 2	IP2SRn	R/W	Port group 0: H'0007 7777 Port group 1, 2, 3, 4, 5, 6, 7: H'0000 0000	H'068	32	-
Peripheral Function Select register 3	IP3SRn	R/W	H'0000 0000	H'06C	32	-
DRV control register 0	DRV0CTRLn	R/W	Port group 0, 1, 3, 4, 5, 6, 7: H'6666 6666 Port group 2: H'2222 2222	H'080	32	-
DRV control register 1	DRV1CTRLn	R/W	Port group 0, 1, 3, 4, 5, 6, 7: H'6666 6666 Port group 2: H'6222 2222	H'084	32	-

Name	Abbr.	R/W	Initial Value	Offset Address [lower 9bits]	Access Size [bits]	Condition
DRV control register 2	DRV2CTRLn	R/W	Port group 0: H'0006 6666 Port group 1, 4, 7: H'6666 6666 Port group 2: H'0000 0006 Port group 3: H'0000 0666 Port group 5: H'0000 6666 Port group 6: H'0666 6666	H'088	32	-
DRV control register 3	DRV3CTRLn	R/W	Port group 0, 2, 5: H'0000 0000 Port group 1: H'0000 0006 Port group 4: H'0666 6666 Port group 6: H'6000 0000 Port group 7: H'6666 6666	H'08C	32	-
POWER Condition control register	POCn	R/W	Port group 0: H'001F FFFF Port group 1: H'01FF FFFF Port group 2, 4, 5, 6, 7: H'0000 0000 Port group 3: H'0007 FFFF	H'0A0	32	-
LSI pin pull-enable register	PUENn	R/W	Port group 0, 2: H'0000 0001 Port group 1, 4, 5, 6, 7: H'0000 0000 Port group 3: H'0006 CFC7	H'0C0	32	-
LSI pin pull-up/down control register	PUDn	R/W	Port group 0, 2: H'0000 0001 Port group 1, 4, 5, 6, 7: H'0000 0000 Port group 3: H'0004 8000	H'0E0	32	-
Module select register	MODSELn	R/W	H'0000 0000	H'100	32	-
TDSEL Control Register 0	TD0SELn	R/W	H'0000 0000	H'120	32	-
TDSEL Control Register 1	TD1SELn	R/W	H'0000 0000	H'124	32	-
Port Safe state Enable Register	PSERn	R/W	H'0000 0000	H'160	32	-
Port Safe state Select Register 0	PS0SRn	R/W	H'0000 0000	H'164	32	-
Port Safe state Select Register 1	PS1SRn	R/W	H'0000 0000	H'168	32	-
General IO/interrupt switching register	IOINTSELn	R/W	H'0000 0000	H'180	32	-
General input/output switching register	INOUTSELn	R/W	H'0000 0000	H'184	32	-
General output register	OUTDTn	R/W	H'0000 0000	H'188	32	-
General input register	INDTn	R	-	H'18C	32	-
Interrupt display register	INTDTn	R	-	H'190	32	-
Interrupt clear register	INTCLRn	R/W	H'0000 0000	H'194	32	-

Name	Abbr.	R/W	Initial Value	Offset Address [lower 9bits]	Access Size [bits]	Condition
Interrupt mask register	INTMSKn	R/W	H'0000 0000	H'198	32	-
Interrupt Mask Clear Register	MSKCLRn	R/W	H'0000 0000	H'19C	32	-
Positive/negative logic select register	POSNEGn	R/W	H'0000 0000	H'1A0	32	-
Edge/level select register 0	EDGLEVELn	R/W	H'0000 0000	H'1A4	32	-
Chattering prevention on/off register	FILONOFFn	R/W	H'0000 0000	H'1A8	32	-
Chattering prevention clock select register	FILCLKSELn	R/W	H'0000 411B	H'1AC	32	-
Output data select register	OUTDTSELn	R/W	H'0000 0000	H'1C0	32	-
Output data high register	OUTDTHn	R/W	H'0000 0000	H'1C4	32	-
Output data low register	OUTDTLn	R/W	H'0000 0000	H'1C8	32	-
One edge/both edge select register	BOTHEDGEn	R/W	H'0000 0000	H'1CC	32	-
General input enable register	INENn	R/W	H'0000 0000	H'1D0	32	-

Table 7.6 Configuration of R/W Registers in System Group

Name	Abbr.	R/W	Initial Value	Offset Address [lower 9bits]	Access Size [bits]	Condition
Domain protection register0	DM0PRSYS0	R/W	H'FFFF FFFF	H'020	32	-
DRV control register 0	DRV0CTRLSYS0	R/W	H'0000 0006	H'080	32	-
DRV control register 1	DRV1CTRLSYS1	R/W	H'2222 2222	H'084	32	-
DRV control register 2	DRV2CTRLSYS1	R/W	H'0002 2222	H'088	32	-
LSI pin pull-enable register	PUENSYS0-1	R/W	SYS0: H'0000 0000 SYS1: H'0000 07FE	H'0C0	32	-
LSI pin pull-up/down control register	PUDSYS0-1	R/W	SYS0: H'0000 0000 SYS1: H'0000 07F8	H'0E0	32	-

Table 7.7 Configuration of R/W Additional Registers (for GP4, 5, 6, 7 only)

Name	Abbr.	R/W	Initial Value	Offset Address [lower 9bits]	Access Size [bits]	Condition
Port NOT Register	PNOTn	W	H'0000 0000	H'1D4	32	-
Port Output Value Inversion Register	PINVn	R/W	H'0000 0000	H'16C	32	-
Port Input Buffer Selection Register	PISn	R/W	H'0000 0000	H'170	32	-

7.1.5 Connected Module

Table 7.8 Connected module

Module name	Connected module name	Function of connected module
PFC	AP-System Core (GP0,1,2,3, System0) Control Domain CPU Core (GP4,5,6,7, System1)	Access the Registers
	CPG	Output clocks
	Module Standby	Control to stop clocks

	Software Reset	Execute software reset
	Error Management Module	Output error signals
	INTC-AP, INTC-RT	Control to interrupt

7.2 Register Description

Attaching to this UM the excel files that have the register description information.
Refer to the following files too.

- R-CarS4_UM_007_PFC_GPIO_for_GP0_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP1_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP2_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP3_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP4_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP5_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP6_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_GP7_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_SYS0_r0p70.xlsx
- R-CarS4_UM_007_PFC_GPIO_for_SYS1_r0p70.xlsx

[Legend]

Initial value:	Register value after a reset
- :	Undefined value
R/W:	Readable/writable. The written value can be read.
R:	Read-only. The write value should always be 0.
W:	Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.
n:	Number of GPIO Group, it’s value is in the range 0 to 7.

All the bits are active high unless otherwise specified, and deactivated on reset.
All access to registers is made in longword units.
The write value to a reserved bit should always be 0.
[Register access type and access mode]
Register access type is decoded by address offset, and selected by address check.

- R/W : Read-Write enabled register.

  Offset: H’000
- SET : Controled per bit. Write case, applied bit is "1" then "1", or applied bit is "0" then keep value. Read case, return Reg value. (HWM described as WriteOnly)

  Offset: H’200
- CLR : Controled per bit. Write case, applied bit is "1" then "0", or applied bit is "0" then keep value. Read case, return Reg value. (HWM described WriteOnly)

  Offset: H’400
- Reserved:

  Offset: H’600

Note :
The Register or Bits related pins not in Pin Assignment, these have to keep initial value. For detail of Pin Assignment, refer to Attachment document “003_004_R-Car S4 series User's Manual(Pin Assignment,Pin Multiplex Table)_r0p80.xlsx”.

7.2.1 LSI Multiplexed Pin Setting Mask Register (PMMRn)

Function: PMMRn / PMMRSYS enables / disables writing to the multiplexed pin setting registers.

PMMRn / PMMRSYS bật/tắt ghi vào các thanh ghi cài đặt chân ghép kênh.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PMMRn[31:16] / PMMRSYS[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PMMRn[15:0] / PMMRSYS[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PMMRn[31:0]	H'0000 0000	R/W	Multiplexed Pin Setting Mask Writing a value to any register from among the GPIO/peripheral function select register GPSR, peripheral function select registers IPSR, DRV control registers, TDSEL control register, POWER Condition control register, LSI pin pull-enable register PUEN, LSI pin pull-up/down control register PUD, module select register MODSEL, bus domain protection register DMPR, port safe state enable register PSER, port safe state select register PSSR, port output value inversion register PINV and port input buffer selection register PIS is enabled by writing the inverse of the value to this register.

Note: This register must be set before setting each of the GPIO / peripheral function select register GPSR, peripheral function select registers IPSR, DRV control register, TDSEL control register, LSI pin pull-enable register PUEN, LSI pin pull-up/down control register PUD, module select register MODSEL, bus domain protection register DMPR, POC control register, port safe state enable register PSER, port safe state select register PSSR, port output value inversion register PINV and port input buffer selection register PIS.

Thanh ghi này phải được thiết lập trước khi thiết lập từng thanh ghi lựa chọn chức năng GPIO / ngoại vi bao gồm thanh ghi lựa chọn chức năng GPSR, các thanh ghi điều khiển chức năng ngoại vi IPSR, thanh ghi điều khiển DRV, thanh ghi điều khiển TDSEL, thanh ghi cho phép kéo của chân LSI PUEN, thanh ghi điều khiển kéo lên / kéo xuống của chân LSI PUD, thanh ghi lựa chọn module MODSEL, thanh ghi bảo vệ miền bus DMPR, thanh ghi điều khiển POC, thanh ghi cho phép trạng thái an toàn của cổng PSER, thanh ghi lựa chọn trạng thái an toàn của cổng PSSR, thanh ghi đảo giá trị đầu ra của cổng PINV và thanh ghi lựa chọn bộ đệm đầu vào của cổng PIS.

7.2.2 LSI Multiplexed Pin Setting Mask Enable Register (PMMERn)

Function: PMMERn / PMMERSYS performs enables / disables control of the PMMR.

PMMERn/PMMERSYS thực hiện cho phép/không cho phép điều khiển PMMR

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PMMERn[0] / PMMERSYS[0]
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

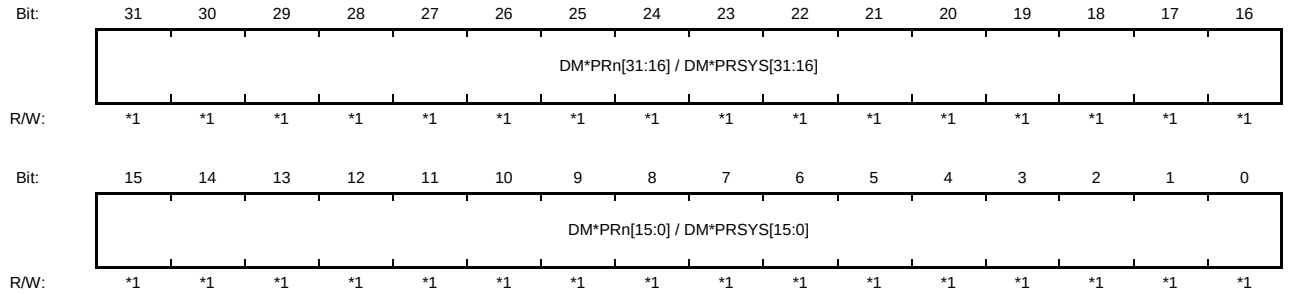
Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	—	R	—
0	PMMERn	1	R/W	Multiplexed Pin Setting Mask Enable 0: PMMR function is disabled. 1: PMMR function is enabled.

7.2.3 Bus Domain Protection Register 0-3 (DM0PRn , DM1PRn , DM2PRn , DM3PRn / DM0PRSYS) (n = 0 to 7)

Thêm DM0PRSYS, DM1PRSYS, DM2PRSYS

Function: DM*PRn / DM*PRSYS enables / disables writing to the registers from bus domain.

Note: * 0 to 3 DM*PRn / DM*PRSYS cho phép / không cho phép ghi vào thanh ghi từ miền bus.



Note: *1 R/W. Be able to write only from Bus domain 0. *1 R/W. Chỉ có thể ghi từ miền Bus 0

Configuration of Registers for n = 0 - 3

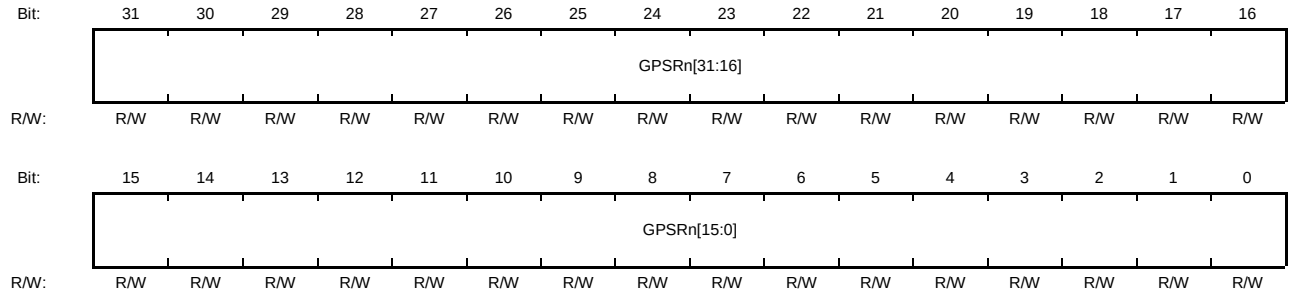
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DM0PRn[31:0], DM0PRSYS[31:0]	H'FFFF FFFF	R/W	Bus Domain Protection Bảo vệ Bus Domain 0: Disable write to register 1: Enable write to register
	DM1PRn[31:0], DM2PRn[31:0], DM3PRn[31:0], DM1PRSYS[31:0], DM2PRSYS[31:0], DM3PRSYS[31:0]	H'0000 0000	R/W	DMiPRn / DMiPRSYS and FILCLKSEL are not include in the potection target. DMiPRn / DMiPRSYS và FILCLKSEL không được bao gồm trong mục tiêu bảo vệ

Configuration of Registers for n = 4 - 7

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DM1PRn[31:0]	H'0000 0000	R/W	Error Trigger selection for Port Safe State function 0: Error Trigger 0 is not selected. 1: Error Trigger 0 is selected.
	DM2PRn[31:0]	H'0000 0000	R/W	Error Trigger selection for Port Safe State function 0: Error Trigger 1 is not selected. 1: Error Trigger 1 is selected.

7.2.4 GPIO / Peripheral Function Select Register (GPSRn)

Function: GPSRn selects the functions of the multiplexed LSI pins.



Bit	Bit Name	R/W	Description
31 to 0	GPSRn[31:0]	R/W	0: GPIO 1: Peripheral function The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Table 7.9 Configuration of Registers in GPSR0-2

	GPSR0			GPSR1			GPSR2		
	Pin name	Initial value (MD[4:1] =B'0000)	Initial value (MD[4:1] ≠B'0000)	Pin name	Initial value (MD[4:1] =B'0000)	Initial value (MD[4:1] ≠B'0000)	Pin name	Initial value (MD[4:1] =B'0000)	Initial value (MD[4:1] ≠B'0000)
bit31	—	—	—	—	—	—	—	—	—
bit30	—	—	—	—	—	—	—	—	—
bit29	—	—	—	—	—	—	—	—	—
bit28	—	—	—	—	—	—	—	—	—
bit27	—	—	—	—	—	—	—	—	—
bit26	—	—	—	—	—	—	—	—	—
bit25	—	—	—	—	—	—	—	—	—
bit24	—	—	—	SD_WP	1	1	—	—	—
bit23	—	—	—	SD_CD	1	1	—	—	—
bit22	—	—	—	MMC_SD_CMD	1	1	—	—	—
bit21	—	—	—	MMC_D7	1	1	—	—	—
bit20	IRQ3	1	0	MMC_DS	1	1	—	—	—
bit19	IRQ2	1	0	MMC_D6	1	1	—	—	—
bit18	IRQ1	1	0	MMC_D4	1	1	—	—	—
bit17	IRQ0	1	0	MMC_D5	1	1	—	—	—
bit16	MSIOF0_SS2	1	0	MMC_SD_D3	1	1	PCIE1_CLKREQ#	0	0
bit15	MSIOF0_SS1	1	0	MMC_SD_D2	1	1	PCIE0_CLKREQ#	0	0
bit14	MSIOF0_SCK	1	0	MMC_SD_D1	1	1	QSPI0_IO3	1	1
bit13	MSIOF0_TXD	1	0	MMC_SD_D0	1	1	QSPI0_SSL	1	1
bit12	MSIOF0_RXD	1	0	MMC_SD_CLK	1	1	QSPI0_MISO_IO1	1	1
bit11	MSIOF0_SYNC	1	0	GP1_11	0	0	QSPI0_IO2	1	1
bit10	CTS0#	1	0	GP1_10	0	0	QSPI0_SPCLK	1	1
bit9	RTS0#	1	0	GP1_09	0	0	QSPI0_MOSI_IO0	1	1
bit8	SCK0	1	0	GP1_08	0	0	QSPI1_SPCLK	1	1
bit7	TX0	1	0	GP1_07	0	0	QSPI1_MOSI_IO0	1	1
bit6	RX0	1	0	GP1_06	1	0	QSPI1_IO2	1	1
bit5	HRTS0#	1	0	GP1_05	1	0	QSPI1_MISO_IO1	1	1
bit4	HCTS0#	1	0	GP1_04	1	0	QSPI1_IO3	1	1
bit3	HTX0	1	0	GP1_03	1	0	QSPI1_SSL	1	1
bit2	HRX0	1	0	GP1_02	1	0	RPC_RESET#	1	1
bit1	HSCK0	1	0	GP1_01	1	0	RPC_WP#	1	1
bit0	SCIF_CLK	1	0	GP1_00	1	0	RPC_INT#	1	1

Table 7.10 Configuration of Registers in GPSR3-5

	GPSR3			GPSR4			GPSR5		
	Pin name	Initial value (MD[4:1] =B'0000)	Initial value (MD[4:1] ≠B'0000)	Pin name	Initial value (MD[4:1] =B'0000)	Initial value (MD[4:1] ≠B'0000)	Pin name	Initial value (MD[4:1] =B'0000)	Initial value (MD[4:1] ≠B'0000)
bit31	—	—	—	—	—	—	—	—	—
bit30	—	—	—	MSPI1CSS1	0	0	—	—	—
bit29	—	—	—	MSPI1CSS2	0	0	—	—	—
bit28	—	—	—	MSPI1SC	0	0	—	—	—
bit27	—	—	—	MSPI1CSS0	0	0	—	—	—
bit26	—	—	—	MSPI1SO/MSPI1DCS	0	0	—	—	—
bit25	—	—	—	MSPI1SI	0	0	—	—	—
bit24	—	—	—	MSPI0CSS0	0	0	—	—	—
bit23	—	—	—	MSPI0CSS1	0	0	—	—	—
bit22	—	—	—	MSPI0SO/MSPI0DCS	0	0	—	—	—
bit21	—	—	—	MSPI0SI	0	0	—	—	—
bit20	—	—	—	MSPI0SC	0	0	—	—	—
bit19	—	—	—	GP4_19	0	0	ETNB0TXD0	0	0
bit18	TSN0_AVTP_CAPTURE	1	1	GP4_18	0	0	ETNB0TXEN	0	0
bit17	TSN0_AVTP_MATCH	1	1	GP4_17	0	0	ETNB0TXD2	0	0
bit16	TSN0_AVTP_PPS	1	1	GP4_16	0	0	ETNB0TXD1	0	0
bit15	TSN1_AVTP_CAPTURE	1	1	GP4_15	0	0	ETNB0TXCLK	0	0
bit14	TSN1_AVTP_MATCH	1	1	GP4_14	0	0	ETNB0TXD3	0	0
bit13	TSN1_AVTP_PPS	1	1	GP4_13	0	0	ETNB0TXER	0	0
bit12	TSN0_MAGIC	1	1	GP4_12	0	0	ETNB0RXCLK	0	0
bit11	TSN1_PHY_INT	1	1	GP4_11	0	0	ETNB0RXD0	0	0
bit10	TSN0_PHY_INT	1	1	GP4_10	0	0	ETNB0RXDV	0	0
bit9	TSN2_PHY_INT	1	1	GP4_09	0	0	ETNB0RXD2	0	0
bit8	TSN0_LINK	1	1	GP4_08	0	0	ETNB0RXD1	0	0
bit7	TSN2_LINK	1	1	GP4_07	0	0	ETNB0RXD3	0	0
bit6	TSN1_LINK	1	1	GP4_06	0	0	ETNB0RXER	0	0
bit5	TSN1_MDC	1	1	GP4_05	0	0	ETNB0MDC	0	0
bit4	TSN0_MDC	1	1	GP4_04	0	0	ETNB0LINKSTA	0	0
bit3	TSN2_MDC	1	1	GP4_03	0	0	ETNB0WOL	0	0
bit2	TSN0_MDIO	1	1	GP4_02	0	0	ETNB0MD	0	0
bit1	TSN2_MDIO	1	1	GP4_01	0	0	RIIC0SDA	0	0
bit0	TSN1_MDIO	1	1	GP4_00	0	0	RIIC0SCL	0	0

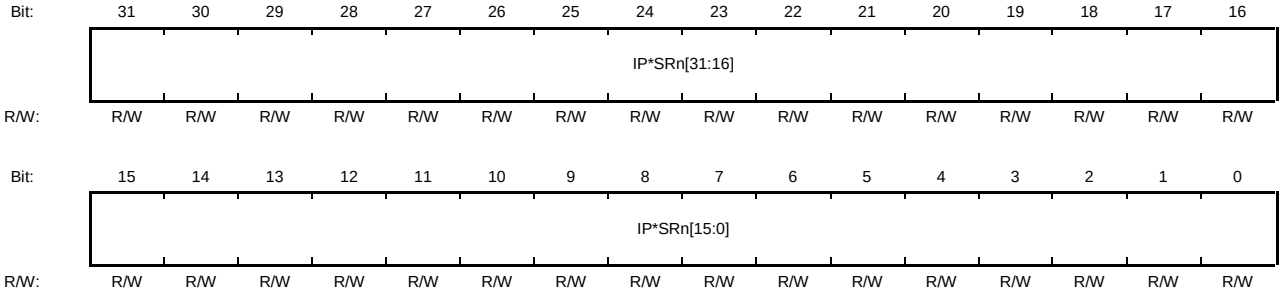
Table 7.11 Configuration of Registers in GPSR6-7

	GPSR6			GPSR7		
	Pin name	Initial value (MD[4:1] =B'0000)	Initial value (MD[4:1] ≠B'0000)	Pin name	Initial value (MD[4:1] =B'0000)	Initial value (MD[4:1] ≠B'0000)
bit31	PRESETOUT1#	1	1	CAN15RX/INTP15	0	0
bit30	—	—	—	CAN15TX	0	0
bit29	—	—	—	CAN14RX/INTP14	0	0
bit28	—	—	—	CAN14TX	0	0
bit27	—	—	—	CAN13RX/INTP13	0	0
bit26	—	—	—	CAN13TX	0	0
bit25	—	—	—	CAN12RX/INTP12	0	0
bit24	—	—	—	CAN12TX	0	0
bit23	—	—	—	CAN11RX/INTP11	0	0
bit22	NMI1	0	0	CAN11TX	0	0
bit21	INTP32	0	0	CAN10RX/INTP10	0	0
bit20	INTP33	0	0	CAN10TX	0	0
bit19	INTP34	0	0	CAN9RX/INTP9	0	0
bit18	INTP35	0	0	CAN9TX	0	0
bit17	INTP36	0	0	CAN8RX/INTP8	0	0
bit16	INTP37	0	0	CAN8TX	0	0
bit15	RLIN30RX/INTP16	0	0	CAN7RX/INTP7	0	0
bit14	RLIN30TX	0	0	CAN7TX	0	0
bit13	RLIN31RX/INTP17	0	0	CAN6RX/INTP6	0	0
bit12	RLIN31TX	0	0	CAN6TX	0	0
bit11	RLIN32RX/INTP18	0	0	CAN5RX/INTP5	0	0
bit10	RLIN32TX	0	0	CAN5TX	0	0
bit9	RLIN33RX/INTP19	0	0	CAN4RX/INTP4	0	0
bit8	RLIN33TX	0	0	CAN4TX	0	0
bit7	RLIN34RX/INTP20	0	0	CAN3RX/INTP3	0	0
bit6	RLIN34TX	0	0	CAN3TX	0	0
bit5	RLIN35RX/INTP21	0	0	CAN2RX/INTP2	0	0
bit4	RLIN35TX	0	0	CAN2TX	0	0
bit3	RLIN36RX/INTP22	0	0	CAN1RX/INTP1	0	0
bit2	RLIN36TX	0	0	CAN1TX	0	0
bit1	RLIN37RX/INTP23	0	0	CAN0RX/INTP0	0	0
bit0	RLIN37TX	0	0	CAN0TX	0	0

7.2.5 Peripheral Function Select Register 0-1 (IP0SRn , IP1SRn , IP2SRn , IP3SRn)

Function: IP*SRn selects the functions of the multiplexed LSI pins.

Note: * 0 to 3



Note: * 0 to 3

Bit	R/W	Description
31 to 0	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Table 7.12 Configuration of Registers in IP0SR0 , IP1SR0 , IP2SR0

		Register Value [4 bits]			
Pin name	Register	H'0	H'1	H'2	H'3
SCIF_CLK	IP0SR0[3:0]	SCIF_CLK	—	—	—
HSCK0	IP0SR0[7:4]	HSCK0	SCK3	MSIOF3_SCK	—
HRX0	IP0SR0[11:8]	HRX0	RX3	MSIOF3_RXD	—
HTX0	IP0SR0[15:12]	HTX0	TX3	MSIOF3_TXD	—
HCTS0#	IP0SR0[19:16]	HCTS0#	CTS3#	MSIOF3_SS1	—
HRTS0#	IP0SR0[23:20]	HRTS0#	RTS3#	MSIOF3_SS2	—
RX0	IP0SR0[27:24]	RX0	HRX1	—	MSIOF1_RXD
TX0	IP0SR0[31:28]	TX0	HTX1	—	MSIOF1_TXD
SCK0	IP1SR0[3:0]	SCK0	HSCK1	—	MSIOF1_SCK
RTS0#	IP1SR0[7:4]	RTS0#	HRTS1#	MSIOF3_SYNC	—
CTS0#	IP1SR0[11:8]	CTS0#	HCTS1#	—	MSIOF1_SYNC
MSIOF0_SYNC	IP1SR0[15:12]	MSIOF0_SYNC	HCTS3#	CTS1#	IRQ4
MSIOF0_RXD	IP1SR0[19:16]	MSIOF0_RXD	HRX3	RX1	—
MSIOF0_TXD	IP1SR0[23:20]	MSIOF0_TXD	HTX3	TX1	—
MSIOF0_SCK	IP1SR0[27:24]	MSIOF0_SCK	HSCK3	SCK1	—
MSIOF0_SS1	IP1SR0[31:28]	MSIOF0_SS1	HRTS3#	RTS1#	IRQ5
MSIOF0_SS2	IP2SR0[3:0]	MSIOF0_SS2	—	—	—
IRQ0	IP2SR0[7:4]	IRQ0	—	—	MSIOF1_SS1
IRQ1	IP2SR0[11:8]	IRQ1	—	—	MSIOF1_SS2
IRQ2	IP2SR0[15:12]	IRQ2	—	—	—
IRQ3	IP2SR0[19:16]	IRQ3	—	—	—

		Register Value [4 bits]
Pin name	Register	H'5
SCIF_CLK	IP0SR0[3:0]	—
HSCK0	IP0SR0[7:4]	TSN0_AVTP_CAPTURE
HRX0	IP0SR0[11:8]	TSN0_AVTP_MATCH
HTX0	IP0SR0[15:12]	—
HCTS0#	IP0SR0[19:16]	TSN0_MDC
HRTS0#	IP0SR0[23:20]	TSN0_MDIO
RX0	IP0SR0[27:24]	TSN1_AVTP_MATCH
TX0	IP0SR0[31:28]	TSN1_AVTP_CAPTURE
SCK0	IP1SR0[3:0]	—
RTS0#	IP1SR0[7:4]	TSN1_MDIO
CTS0#	IP1SR0[11:8]	TSN1_MDC
MSIOF0_SYNC	IP1SR0[15:12]	TSN0_LINK
MSIOF0_RXD	IP1SR0[19:16]	—
MSIOF0_TXD	IP1SR0[23:20]	—
MSIOF0_SCK	IP1SR0[27:24]	—
MSIOF0_SS1	IP1SR0[31:28]	TSN1_LINK
MSIOF0_SS2	IP2SR0[3:0]	TSN2_LINK
IRQ0	IP2SR0[7:4]	TSN0_MAGIC
IRQ1	IP2SR0[11:8]	TSN0_PHY_INT
IRQ2	IP2SR0[15:12]	TSN1_PHY_INT
IRQ3	IP2SR0[19:16]	TSN2_PHY_INT

Table 7.13 Configuration of Registers in IP0SR1

		Register Value [4 bits]			
Pin name	Register	H'0	H'1	H'2	H'3
GP1_00	IP0SR1[3:0]	GP1_00	TCLK1	HSCK2	—
GP1_01	IP0SR1[7:4]	GP1_01	TCLK4	HRX2	—
GP1_02	IP0SR1[11:8]	GP1_02	—	HTX2	MSIOF2_SS1
GP1_03	IP0SR1[15:12]	GP1_03	TCLK2	HCTS2#	MSIOF2_SS2
GP1_04	IP0SR1[19:16]	GP1_04	TCLK3	HRTS2#	MSIOF2_SYNC
GP1_05	IP0SR1[23:20]	GP1_05	MSIOF2_SCK	SCK4	—
GP1_06	IP0SR1[27:24]	GP1_06	MSIOF2_RXD	RX4	—
GP1_07	IP0SR1[31:28]	GP1_07	MSIOF2_TXD	TX4	—
GP1_08	—	GP1_08	—	—	—
GP1_09	—	GP1_09	—	—	—
GP1_10	—	GP1_10	—	—	—
GP1_11	—	GP1_11	—	—	—
MMC_SD_CLK	—	MMC_SD_CLK	—	—	—
MMC_SD_D0	—	MMC_SD_D0	—	—	—
MMC_SD_D1	—	MMC_SD_D1	—	—	—
MMC_SD_D2	—	MMC_SD_D2	—	—	—
MMC_SD_D3	—	MMC_SD_D3	—	—	—
MMC_D5	—	MMC_D5	—	—	—
MMC_D4	—	MMC_D4	—	—	—
MMC_D6	—	MMC_D6	—	—	—
MMC_DS	—	MMC_DS	—	—	—
MMC_D7	—	MMC_D7	—	—	—
MMC_SD_CMD	—	MMC_SD_CMD	—	—	—
SD_CD	—	SD_CD	—	—	—
SD_WP	—	SD_WP	—	—	—

		Register Value [4 bits]	
Pin name	Register	H'4	H'5
GP1_00	IP0SR1[3:0]	—	—
GP1_01	IP0SR1[7:4]	—	—
GP1_02	IP0SR1[11:8]	—	TSN2_MDC
GP1_03	IP0SR1[15:12]	CTS4#	TSN2_MDIO
GP1_04	IP0SR1[19:16]	RTS4#	—
GP1_05	IP0SR1[23:20]	—	—
GP1_06	IP0SR1[27:24]	—	—
GP1_07	IP0SR1[31:28]	—	—
GP1_08	—	—	—
GP1_09	—	—	—
GP1_10	—	—	—
GP1_11	—	—	—
MMC_SD_CLK	—	—	—
MMC_SD_D0	—	—	—
MMC_SD_D1	—	—	—
MMC_SD_D2	—	—	—
MMC_SD_D3	—	—	—
MMC_D5	—	—	—
MMC_D4	—	—	—
MMC_D6	—	—	—
MMC_DS	—	—	—
MMC_D7	—	—	—
MMC_SD_CMD	—	—	—
SD_CD	—	—	—
SD_WP	—	—	—

Table 7.14 Configuration of Registers in IP0SR4 , IP1SR4 , IP2SR4 , IP3SR4

		Register Value [4 bits]			
Pin name	Register	H'0	H'1	H'2	H'3
GP4_00	IP0SR4[3:0]	GP4_00	MSPI4SC	—	TAUD0I2
GP4_01	IP0SR4[7:4]	GP4_01	MSPI4SI	—	TAUD0I4
GP4_02	IP0SR4[11:8]	GP4_02	MSPI4SO/MSPI4DCS	—	TAUD0I3
GP4_03	IP0SR4[15:12]	GP4_03	MSPI4CSS1	—	TAUD0I6
GP4_04	IP0SR4[19:16]	GP4_04	MSPI4CSS0	MSPI4SSI#	TAUD0I5
GP4_05	IP0SR4[23:20]	GP4_05	MSPI4CSS3	—	TAUD0I8
GP4_06	IP0SR4[27:24]	GP4_06	MSPI4CSS2	—	TAUD0I7
GP4_07	IP0SR4[31:28]	GP4_07	MSPI4CSS5	—	TAUD0I10
GP4_08	IP1SR4[3:0]	GP4_08	MSPI4CSS4	—	TAUD0I9
GP4_09	IP1SR4[7:4]	GP4_09	MSPI4CSS7	—	TAUD0I12
GP4_10	IP1SR4[11:8]	GP4_10	MSPI4CSS6	—	TAUD0I11
GP4_11	IP1SR4[15:12]	GP4_11	ERRORIN0#	—	TAUD0I14
GP4_12	IP1SR4[19:16]	GP4_12	ERROROUT_C#	—	TAUD0I13
GP4_13	—	GP4_13	—	—	—
GP4_14	IP1SR4[27:24]	GP4_14	ERRORIN1#	—	TAUD0I15
GP4_15	IP1SR4[31:28]	GP4_15	MSPI1CSS3	—	TAUD1I1
GP4_16	IP2SR4[3:0]	GP4_16	—	—	TAUD1I0
GP4_17	IP2SR4[7:4]	GP4_17	MSPI1CSS5	—	TAUD1I3
GP4_18	IP2SR4[11:8]	GP4_18	MSPI1CSS4	—	TAUD1I2
GP4_19	IP2SR4[15:12]	GP4_19	MSPI1CSS6	—	TAUD1I4
MSPI0SC	IP2SR4[19:16]	MSPI0SC	MSPI1CSS7	—	TAUD1I5
MSPI0SI	IP2SR4[23:20]	MSPI0SI	—	—	TAUD1I7
MSPI0SO/MSPI0DCS	IP2SR4[27:24]	MSPI0SO/MSPI0DCS	—	—	TAUD1I6
MSPI0CSS1	IP2SR4[31:28]	MSPI0CSS1	—	—	TAUD1I9
MSPI0CSS0	IP3SR4[3:0]	MSPI0CSS0	MSPI0SSI#	—	TAUD1I8
MSPI1SI	IP3SR4[7:4]	MSPI1SI	—	MSPI0CSS4	TAUD1I12
MSPI1SO/MSPI1DCS	IP3SR4[11:8]	MSPI1SO/MSPI1DCS	—	MSPI0CSS3	TAUD1I11
MSPI1CSS0	IP3SR4[15:12]	MSPI1CSS0	MSPI1SSI#	MSPI0CSS5	TAUD1I13
MSPI1SC	IP3SR4[19:16]	MSPI1SC	—	MSPI0CSS2	TAUD1I10
MSPI1CSS2	IP3SR4[23:20]	MSPI1CSS2	—	MSPI0CSS7	TAUD1I15
MSPI1CSS1	IP3SR4[27:24]	MSPI1CSS1	—	MSPI0CSS6	TAUD1I14

		Register Value [4 bits]	
Pin name	Register	H'4	H'5
GP4_00	IP0SR4[3:0]	TAUD0O2	—
GP4_01	IP0SR4[7:4]	TAUD0O4	—
GP4_02	IP0SR4[11:8]	TAUD0O3	—
GP4_03	IP0SR4[15:12]	TAUD0O6	MSPI5SO/MSPI5DCS
GP4_04	IP0SR4[19:16]	TAUD0O5	MSPI5SC
GP4_05	IP0SR4[23:20]	TAUD0O8	MSPI5SSI#
GP4_06	IP0SR4[27:24]	TAUD0O7	MSPI5SI
GP4_07	IP0SR4[31:28]	TAUD0O10	MSPI5CSS1
GP4_08	IP1SR4[3:0]	TAUD0O9	MSPI5CSS0
GP4_09	IP1SR4[7:4]	TAUD0O12	MSPI5CSS3
GP4_10	IP1SR4[11:8]	TAUD0O11	MSPI5CSS2
GP4_11	IP1SR4[15:12]	TAUD0O14	—
GP4_12	IP1SR4[19:16]	TAUD0O13	—
GP4_13	—	—	—
GP4_14	IP1SR4[27:24]	TAUD0O15	—
GP4_15	IP1SR4[31:28]	TAUD1O1	—
GP4_16	IP2SR4[3:0]	TAUD1O0	—
GP4_17	IP2SR4[7:4]	TAUD1O3	—
GP4_18	IP2SR4[11:8]	TAUD1O2	—
GP4_19	IP2SR4[15:12]	TAUD1O4	—
MSPI0SC	IP2SR4[19:16]	TAUD1O5	—
MSPI0SI	IP2SR4[23:20]	TAUD1O7	—
MSPI0SO/MSPI0DCS	IP2SR4[27:24]	TAUD1O6	—
MSPI0CSS1	IP2SR4[31:28]	TAUD1O9	—
MSPI0CSS0	IP3SR4[3:0]	TAUD1O8	—
MSPI1SI	IP3SR4[7:4]	TAUD1O12	—
MSPI1SO/MSPI1DCS	IP3SR4[11:8]	TAUD1O11	—
MSPI1CSS0	IP3SR4[15:12]	TAUD1O13	—
MSPI1SC	IP3SR4[19:16]	TAUD1O10	—
MSPI1CSS2	IP3SR4[23:20]	TAUD1O15	—
MSPI1CSS1	IP3SR4[27:24]	TAUD1O14	—

Table 7.15 Configuration of Registers in IP0SR5

		Register Value [4 bits]			
Pin name	Register	H'0	H'1	H'2	H'3
RIIC0SCL	IP0SR5[3:0]	RIIC0SCL	—	—	TAUD0I0
RIIC0SDA	IP0SR5[7:4]	RIIC0SDA	—	—	TAUD0I1
ETNB0MD	IP0SR5[11:8]	ETNB0MD	MSPI1CSS1	—	MSPI0CSS6
ETNB0WOL	IP0SR5[15:12]	ETNB0WOL	MSPI1SI	—	MSPI0CSS4
ETNB0LINKSTA	IP0SR5[19:16]	ETNB0LINKSTA	MSPI1CSS0	MSPI1SSI#	MSPI0CSS5
ETNB0MDC	IP0SR5[23:20]	ETNB0MDC	MSPI1CSS2	—	MSPI0CSS7
ETNB0RXER	—	ETNB0RXER	—	—	—
ETNB0RXD3	—	ETNB0RXD3	—	—	—
ETNB0RXD1	—	ETNB0RXD1	—	—	—
ETNB0RXD2	—	ETNB0RXD2	—	—	—
ETNB0RXDV	—	ETNB0RXDV	—	—	—
ETNB0RXD0	—	ETNB0RXD0	—	—	—
ETNB0RXCLK	IP0SR5[27:24]	ETNB0RXCLK	ETNB0CRS_DV	—	—
ETNB0TXER	—	ETNB0TXER	—	—	—
ETNB0TXD3	—	ETNB0TXD3	—	—	—
ETNB0TXCLK	IP0SR5[31:28]	ETNB0TXCLK	ETNB0REFCLK	—	—
ETNB0TXD1	—	ETNB0TXD1	—	—	—
ETNB0TXD2	—	ETNB0TXD2	—	—	—
ETNB0TXEN	—	ETNB0TXEN	—	—	—
ETNB0TXD0	—	ETNB0TXD0	—	—	—

		Register Value [4 bits]	
Pin name	Register	H'4	H'5
RIIC0SCL	IP0SR5[3:0]	TAUD0O0	—
RIIC0SDA	IP0SR5[7:4]	TAUD0O1	—
ETNB0MD	IP0SR5[11:8]	TAUD1I14	TAUD1O14
ETNB0WOL	IP0SR5[15:12]	TAUD1I12	TAUD1O12
ETNB0LINKSTA	IP0SR5[19:16]	TAUD1I13	TAUD1O13
ETNB0MDC	IP0SR5[23:20]	TAUD1I15	TAUD1O15
ETNB0RXER	—	—	—
ETNB0RXD3	—	—	—
ETNB0RXD1	—	—	—
ETNB0RXD2	—	—	—
ETNB0RXDV	—	—	—
ETNB0RXD0	—	—	—
ETNB0RXCLK	IP0SR5[27:24]	—	—
ETNB0TXER	—	—	—
ETNB0TXD3	—	—	—
ETNB0TXCLK	IP0SR5[31:28]	—	—
ETNB0TXD1	—	—	—
ETNB0TXD2	—	—	—
ETNB0TXEN	—	—	—
ETNB0TXD0	—	—	—

Table 7.16 Configuration of Registers in IP0SR6 , IP1SR6 , IP2SR6

		Register Value [4 bits]			
Pin name	Register	H'0	H'1	H'2	H'3
RLIN37TX	IP0SR6[3:0]	RLIN37TX	MSPI5CSS3	—	—
RLIN37RX/INTP23	IP0SR6[7:4]	RLIN37RX/INTP23	MSPI5CSS2	—	—
RLIN36TX	IP0SR6[11:8]	RLIN36TX	MSPI5CSS1	—	—
RLIN36RX/INTP22	IP0SR6[15:12]	RLIN36RX/INTP22	MSPI5CSS0	—	—
RLIN35TX	IP0SR6[19:16]	RLIN35TX	MSPI5SSI#	—	—
RLIN35RX/INTP21	IP0SR6[23:20]	RLIN35RX/INTP21	MSPI5SI	—	—
RLIN34TX	IP0SR6[27:24]	RLIN34TX	MSPI5SO/MSPI5DCS	—	—
RLIN34RX/INTP20	IP0SR6[31:28]	RLIN34RX/INTP20	MSPI5SC	—	—
RLIN33TX	IP1SR6[3:0]	RLIN33TX	—	—	TAUJ3O3
RLIN33RX/INTP19	IP1SR6[7:4]	RLIN33RX/INTP19	—	—	TAUJ3O2
RLIN32TX	IP1SR6[11:8]	RLIN32TX	—	—	TAUJ3O1
RLIN32RX/INTP18	IP1SR6[15:12]	RLIN32RX/INTP18	—	—	TAUJ3O0
RLIN31TX	IP1SR6[19:16]	RLIN31TX	—	—	TAUJ1I3
RLIN31RX/INTP17	IP1SR6[23:20]	RLIN31RX/INTP17	—	—	TAUJ1I2
RLIN30TX	IP1SR6[27:24]	RLIN30TX	—	—	TAUJ1I1
RLIN30RX/INTP16	IP1SR6[31:28]	RLIN30RX/INTP16	—	—	TAUJ1I0
INTP37	IP2SR6[3:0]	INTP37	—	EXTCLK0O	—
INTP36	IP2SR6[7:4]	INTP36	RTCA0OUT	—	—
INTP35	—	INTP35	—	—	—
INTP34	—	INTP34	—	—	—
INTP33	—	INTP33	—	—	—
INTP32	IP2SR6[11:8]	INTP32	—	FLXA0STPWT	—
NMI1	—	NMI1	—	—	—
—	—	—	—	—	—
—	—	—	—	—	—
—	—	—	—	—	—
—	—	—	—	—	—
—	—	—	—	—	—
—	—	—	—	—	—
—	—	—	—	—	—
—	—	—	—	—	—
PRESETOUT1#	—	PRESETOUT1#	—	—	—

		Register Value [4 bits]		
Pin name	Register	H'4	H'5	H'6
RLIN37TX	IP0SR6[3:0]	—	—	—
RLIN37RX/INTP23	IP0SR6[7:4]	—	—	—
RLIN36TX	IP0SR6[11:8]	—	—	—
RLIN36RX/INTP22	IP0SR6[15:12]	—	—	—
RLIN35TX	IP0SR6[19:16]	—	—	—
RLIN35RX/INTP21	IP0SR6[23:20]	—	—	—
RLIN34TX	IP0SR6[27:24]	—	—	—
RLIN34RX/INTP20	IP0SR6[31:28]	—	—	—
RLIN33TX	IP1SR6[3:0]	TAUJ3I3	NMI1	CAN15TX
RLIN33RX/INTP19	IP1SR6[7:4]	TAUJ3I2	INTP37	CAN15RX/INTP15
RLIN32TX	IP1SR6[11:8]	TAUJ3I1	INTP36	CAN14TX
RLIN32RX/INTP18	IP1SR6[15:12]	TAUJ3I0	INTP35	CAN14RX/INTP14
RLIN31TX	IP1SR6[19:16]	TAUJ1O3	INTP34	CAN13TX
RLIN31RX/INTP17	IP1SR6[23:20]	TAUJ1O2	INTP33	CAN13RX/INTP13
RLIN30TX	IP1SR6[27:24]	TAUJ1O1	INTP32	CAN12TX
RLIN30RX/INTP16	IP1SR6[31:28]	TAUJ1O0	—	CAN12RX/INTP12
INTP37	IP2SR6[3:0]	—	—	—
INTP36	IP2SR6[7:4]	—	—	—
INTP35	—	—	—	—
INTP34	—	—	—	—
INTP33	—	—	—	—
INTP32	IP2SR6[11:8]	—	—	—
NMI1	—	—	—	—
—	—	—	—	—
—	—	—	—	—
—	—	—	—	—
—	—	—	—	—
—	—	—	—	—
—	—	—	—	—
—	—	—	—	—
PRESETOUT1#	—	—	—	—

Table 7.17 Configuration of Registers in IP0SR7 , IP1SR7 , IP2SR7 , IP3SR7

		Register Value [4 bits]			
Pin name	Register	H'0	H'1	H'2	H'3
CAN0TX	IP0SR7[3:0]	CAN0TX	RSENT0SPCO	—	MSPI2SO/MSPI2DCS
CAN0RX/INTP0	IP0SR7[7:4]	CAN0RX/INTP0	RSENT0RX	RSENT0RX/RSENT0SPCO	MSPI2SC
CAN1TX	IP0SR7[11:8]	CAN1TX	RSENT1SPCO	—	MSPI2SSI#
CAN1RX/INTP1	IP0SR7[15:12]	CAN1RX/INTP1	RSENT1RX	RSENT1RX/RSENT1SPCO	MSPI2SI
CAN2TX	IP0SR7[19:16]	CAN2TX	RSENT2SPCO	—	—
CAN2RX/INTP2	IP0SR7[23:20]	CAN2RX/INTP2	RSENT2RX	RSENT2RX/RSENT2SPCO	—
CAN3TX	IP0SR7[27:24]	CAN3TX	RSENT3SPCO	—	—
CAN3RX/INTP3	IP0SR7[31:28]	CAN3RX/INTP3	RSENT3RX	RSENT3RX/RSENT3SPCO	—
CAN4TX	IP1SR7[3:0]	CAN4TX	RSENT4SPCO	—	—
CAN4RX/INTP4	IP1SR7[7:4]	CAN4RX/INTP4	RSENT4RX	RSENT4RX/RSENT4SPCO	—
CAN5TX	IP1SR7[11:8]	CAN5TX	RSENT5SPCO	—	—
CAN5RX/INTP5	IP1SR7[15:12]	CAN5RX/INTP5	RSENT5RX	RSENT5RX/RSENT5SPCO	—
CAN6TX	IP1SR7[19:16]	CAN6TX	RSENT6SPCO	—	MSPI3SO/MSPI3DCS
CAN6RX/INTP6	IP1SR7[23:20]	CAN6RX/INTP6	RSENT6RX	RSENT6RX/RSENT6SPCO	MSPI3SC
CAN7TX	IP1SR7[27:24]	CAN7TX	RSENT7SPCO	—	MSPI3SSI#
CAN7RX/INTP7	IP1SR7[31:28]	CAN7RX/INTP7	RSENT7RX	RSENT7RX/RSENT7SPCO	MSPI3SI
CAN8TX	IP2SR7[3:0]	CAN8TX	RLIN38TX	—	MSPI3CSS1
CAN8RX/INTP8	IP2SR7[7:4]	CAN8RX/INTP8	RLIN38RX/INTP24	—	MSPI3CSS0
CAN9TX	IP2SR7[11:8]	CAN9TX	RLIN39TX	—	MSPI3CSS3
CAN9RX/INTP9	IP2SR7[15:12]	CAN9RX/INTP9	RLIN39RX/INTP25	—	MSPI3CSS2
CAN10TX	IP2SR7[19:16]	CAN10TX	RLIN310TX	—	MSPI3CSS5
CAN10RX/INTP10	IP2SR7[23:20]	CAN10RX/INTP10	RLIN310RX/INTP26	—	MSPI3CSS4
CAN11TX	IP2SR7[27:24]	CAN11TX	RLIN311TX	—	MSPI3CSS7
CAN11RX/INTP11	IP2SR7[31:28]	CAN11RX/INTP11	RLIN311RX/INTP27	—	MSPI3CSS6
CAN12TX	IP3SR7[3:0]	CAN12TX	RLIN312TX	—	—
CAN12RX/INTP12	IP3SR7[7:4]	CAN12RX/INTP12	RLIN312RX/INTP28	—	—
CAN13TX	IP3SR7[11:8]	CAN13TX	RLIN313TX	FLXA0RXDB	—
CAN13RX/INTP13	IP3SR7[15:12]	CAN13RX/INTP13	RLIN313RX/INTP29	FLXA0RXDA	—
CAN14TX	IP3SR7[19:16]	CAN14TX	RLIN314TX	FLXA0TXDB	—
CAN14RX/INTP14	IP3SR7[23:20]	CAN14RX/INTP14	RLIN314RX/INTP30	FLXA0TXDA	—
CAN15TX	IP3SR7[27:24]	CAN15TX	RLIN315TX	FLXA0TXENB	—
CAN15RX/INTP15	IP3SR7[31:28]	CAN15RX/INTP15	RLIN315RX/INTP31	FLXA0TXENA	—

		Register Value [4 bits]		
Pin name	Register	H'4	H'5	H'6
CAN0TX	IP0SR7[3:0]	—	RLIN34TX	—
CAN0RX/INTP0	IP0SR7[7:4]	—	RLIN34RX/INTP20	—
CAN1TX	IP0SR7[11:8]	MSPI2CSS0	RLIN35TX	—
CAN1RX/INTP1	IP0SR7[15:12]	—	RLIN35RX/INTP21	—
CAN2TX	IP0SR7[19:16]	MSPI2CSS2	RLIN36TX	—
CAN2RX/INTP2	IP0SR7[23:20]	MSPI2CSS1	RLIN36RX/INTP22	—
CAN3TX	IP0SR7[27:24]	MSPI2CSS4	RLIN37TX	—
CAN3RX/INTP3	IP0SR7[31:28]	MSPI2CSS3	RLIN37RX/INTP23	—
CAN4TX	IP1SR7[3:0]	MSPI2CSS6	RLIN312TX	—
CAN4RX/INTP4	IP1SR7[7:4]	MSPI2CSS5	RLIN312RX/INTP28	—
CAN5TX	IP1SR7[11:8]	—	RLIN313TX	—
CAN5RX/INTP5	IP1SR7[15:12]	MSPI2CSS7	RLIN313RX/INTP29	—
CAN6TX	IP1SR7[19:16]	—	RLIN314TX	—
CAN6RX/INTP6	IP1SR7[23:20]	—	RLIN314RX/INTP30	—
CAN7TX	IP1SR7[27:24]	—	RLIN315TX	—
CAN7RX/INTP7	IP1SR7[31:28]	—	RLIN315RX/INTP31	—
CAN8TX	IP2SR7[3:0]	—	—	—
CAN8RX/INTP8	IP2SR7[7:4]	—	—	—
CAN9TX	IP2SR7[11:8]	—	—	—
CAN9RX/INTP9	IP2SR7[15:12]	—	—	—
CAN10TX	IP2SR7[19:16]	—	—	—
CAN10RX/INTP10	IP2SR7[23:20]	—	—	—
CAN11TX	IP2SR7[27:24]	—	—	RTCA0OUT
CAN11RX/INTP11	IP2SR7[31:28]	—	—	EXTCLK0O
CAN12TX	IP3SR7[3:0]	—	—	—
CAN12RX/INTP12	IP3SR7[7:4]	—	—	—
CAN13TX	IP3SR7[11:8]	—	—	—
CAN13RX/INTP13	IP3SR7[15:12]	—	—	—
CAN14TX	IP3SR7[19:16]	—	—	—
CAN14RX/INTP14	IP3SR7[23:20]	—	—	—
CAN15TX	IP3SR7[27:24]	—	—	—
CAN15RX/INTP15	IP3SR7[31:28]	—	—	—

7.2.6 DRV Control Register 0-3 (DRV0CTRLn , DRV1CTRLn , DRV2CTRLn , DRV3CTRLn / DRV0CTRLSYS0 , DRV1CTRLSYS1 , DRV2CTRLSYS1)

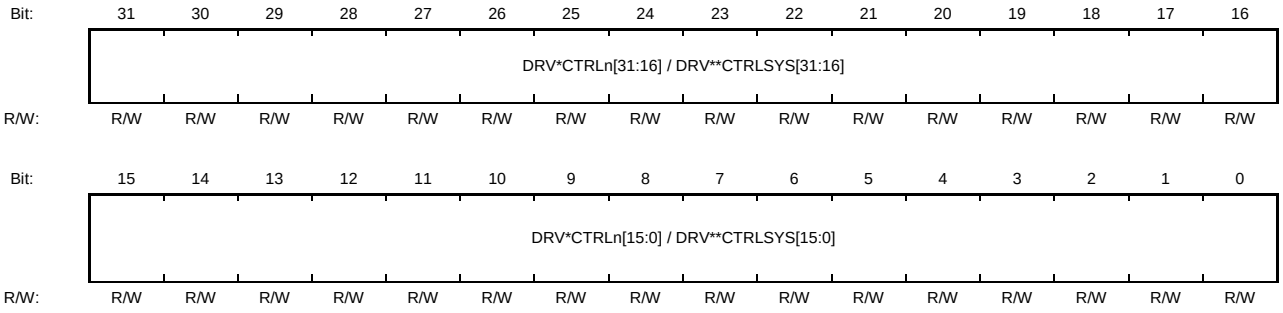
Function: DRV*CTRLn / DRV**CTRLSYS controls the driving abilities of pins. This setting is related to only the output.

Note: * 0 to 3 , ** 0 to 1

Table 7.18 DRV truth table

Output buffer					
			Drive capability		
			Voltage type		
DRV1	DRV2	DRV3	for 1.8V/3.3V	for 2.5V/3.3V	for 3.3V
L	L	L	1/8	1/8	1/8
H	L	L	2/8	2/8	2/8
L	H	L	3/8	3/8	3/8
H	H	L	4/8	4/8	4/8
L	L	H	5/8	5/8	5/8
H	L	H	6/8	6/8	6/8
L	H	H	7/8	7/8	7/8
H	H	H	Full	Full	Full

Output buffer		
		Drive capability
		Voltage type
DRV1	DRV2	for 1.8V
L	L	1/4
H	L	2/4
L	H	3/4
H	H	Full



Note: * 0 to 3 , ** 0 to 1

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Table 7.19 Configuration of Registers in DRV0CTRL0 , DRV1CTRL0 , DRV2CTRL0 , DRV3CTRL0

	DRV0CTRL0			DRV1CTRL0		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	TX0	DRV3	1	MSIOF0_SS1	DRV3	1
bit29		DRV2	1		DRV2	1
bit28		DRV1	0		DRV1	0
bit27	—	—	0	—	—	0
bit26	RX0	DRV3	1	MSIOF0_SCK	DRV3	1
bit25		DRV2	1		DRV2	1
bit24		DRV1	0		DRV1	0
bit23	—	—	0	—	—	0
bit22	HRTS0#	DRV3	1	MSIOF0_TXD	DRV3	1
bit21		DRV2	1		DRV2	1
bit20		DRV1	0		DRV1	0
bit19	—	—	0	—	—	0
bit18	HCTS0#	DRV3	1	MSIOF0_RXD	DRV3	1
bit17		DRV2	1		DRV2	1
bit16		DRV1	0		DRV1	0
bit15	—	—	0	—	—	0
bit14	HTX0	DRV3	1	MSIOF0_SYNC	DRV3	1
bit13		DRV2	1		DRV2	1
bit12		DRV1	0		DRV1	0
bit11	—	—	0	—	—	0
bit10	HRX0	DRV3	1	CTS0#	DRV3	1
bit9		DRV2	1		DRV2	1
bit8		DRV1	0		DRV1	0
bit7	—	—	0	—	—	0
bit6	HSCK0	DRV3	1	RTS0#	DRV3	1
bit5		DRV2	1		DRV2	1
bit4		DRV1	0		DRV1	0
bit3	—	—	0	—	—	0
bit2	SCIF_CLK	DRV3	1	SCK0	DRV3	1
bit1		DRV2	1		DRV2	1
bit0		DRV1	0		DRV1	0

	DRV2CTRL0			DRV3CTRL0		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	—	—	0
bit29	—	—	0	—	—	0
bit28	—	—	0	—	—	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	—	—	0	—	—	0
bit24	—	—	0	—	—	0
bit23	—	—	0	—	—	0
bit22	—	—	0	—	—	0
bit21	—	—	0	—	—	0
bit20	—	—	0	—	—	0
bit19	—	—	0	—	—	0
bit18	IRQ3	DRV3	1	—	—	0
bit17		DRV2	1	—	—	0
bit16		DRV1	0	—	—	0
bit15	—	—	0	—	—	0
bit14	IRQ2	DRV3	1	—	—	0
bit13		DRV2	1	—	—	0
bit12		DRV1	0	—	—	0
bit11	—	—	0	—	—	0
bit10	IRQ1	DRV3	1	—	—	0
bit9		DRV2	1	—	—	0
bit8		DRV1	0	—	—	0
bit7	—	—	0	—	—	0
bit6	IRQ0	DRV3	1	—	—	0
bit5		DRV2	1	—	—	0
bit4		DRV1	0	—	—	0
bit3	—	—	0	—	—	0
bit2	MSIOF0_SS2	DRV3	1	—	—	0
bit1		DRV2	1	—	—	0
bit0		DRV1	0	—	—	0

Table 7.20 Configuration of Registers in DRV0CTRL1 , DRV1CTRL1 , DRV2CTRL1 , DRV3CTRL1

	DRV0CTRL1			DRV1CTRL1		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	GP1_07	DRV3	1	MMC_SD_D2	DRV3	1
bit29		DRV2	1		DRV2	1
bit28		DRV1	0		DRV1	0
bit27	—	—	0	—	—	0
bit26	GP1_06	DRV3	1	MMC_SD_D1	DRV3	1
bit25		DRV2	1		DRV2	1
bit24		DRV1	0		DRV1	0
bit23	—	—	0	—	—	0
bit22	GP1_05	DRV3	1	MMC_SD_D0	DRV3	1
bit21		DRV2	1		DRV2	1
bit20		DRV1	0		DRV1	0
bit19	—	—	0	—	—	0
bit18	GP1_04	DRV3	1	MMC_SD_CLK	DRV3	1
bit17		DRV2	1		DRV2	1
bit16		DRV1	0		DRV1	0
bit15	—	—	0	—	—	0
bit14	GP1_03	DRV3	1	GP1_11	DRV3	1
bit13		DRV2	1		DRV2	1
bit12		DRV1	0		DRV1	0
bit11	—	—	0	—	—	0
bit10	GP1_02	DRV3	1	GP1_10	DRV3	1
bit9		DRV2	1		DRV2	1
bit8		DRV1	0		DRV1	0
bit7	—	—	0	—	—	0
bit6	GP1_01	DRV3	1	GP1_09	DRV3	1
bit5		DRV2	1		DRV2	1
bit4		DRV1	0		DRV1	0
bit3	—	—	0	—	—	0
bit2	GP1_00	DRV3	1	GP1_08	DRV3	1
bit1		DRV2	1		DRV2	1
bit0		DRV1	0		DRV1	0

	DRV2CTRL1			DRV3CTRL1		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	SD_CD	DRV3	1	—	—	0
bit29		DRV2	1	—	—	0
bit28		DRV1	0	—	—	0
bit27	—	—	0	—	—	0
bit26	MMC_SD_CMD	DRV3	1	—	—	0
bit25		DRV2	1	—	—	0
bit24		DRV1	0	—	—	0
bit23	—	—	0	—	—	0
bit22	MMC_D7	DRV3	1	—	—	0
bit21		DRV2	1	—	—	0
bit20		DRV1	0	—	—	0
bit19	—	—	0	—	—	0
bit18	MMC_DS	DRV3	1	—	—	0
bit17		DRV2	1	—	—	0
bit16		DRV1	0	—	—	0
bit15	—	—	0	—	—	0
bit14	MMC_D6	DRV3	1	—	—	0
bit13		DRV2	1	—	—	0
bit12		DRV1	0	—	—	0
bit11	—	—	0	—	—	0
bit10	MMC_D4	DRV3	1	—	—	0
bit9		DRV2	1	—	—	0
bit8		DRV1	0	—	—	0
bit7	—	—	0	—	—	0
bit6	MMC_D5	DRV3	1	—	—	0
bit5		DRV2	1	—	—	0
bit4		DRV1	0	—	—	0
bit3	—	—	0	—	—	0
bit2	MMC_SD_D3	DRV3	1	SD_WP	DRV3	1
bit1		DRV2	1		DRV2	1
bit0		DRV1	0		DRV1	0

Table 7.21 Configuration of Registers in DRV0CTRL2 , DRV1CTRL2 , DRV2CTRL2 , DRV3CTRL2

	DRV0CTRL2			DRV1CTRL2		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	PCIE0_CLKREQ#	DRV3	1
bit29	QSPI1_MOSI_IO0	DRV2	1		DRV2	1
bit28		DRV1	0		DRV1	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	QSPI1_IO2	DRV2	1	QSPI0_IO3	DRV2	1
bit24		DRV1	0		DRV1	0
bit23	—	—	0	—	—	0
bit22	—	—	0	—	—	0
bit21	QSPI1_MISO_IO1	DRV2	1	QSPI0_SSL	DRV2	1
bit20		DRV1	0		DRV1	0
bit19	—	—	0	—	—	0
bit18	—	—	0	—	—	0
bit17	QSPI1_IO3	DRV2	1	QSPI0_MISO_IO1	DRV2	1
bit16		DRV1	0		DRV1	0
bit15	—	—	0	—	—	0
bit14	—	—	0	—	—	0
bit13	QSPI1_SSL	DRV2	1	QSPI0_IO2	DRV2	1
bit12		DRV1	0		DRV1	0
bit11	—	—	0	—	—	0
bit10	—	—	0	—	—	0
bit9	RPC_RESET#	DRV2	1	QSPI0_SPCLK	DRV2	1
bit8		DRV1	0		DRV1	0
bit7	—	—	0	—	—	0
bit6	—	—	0	—	—	0
bit5	RPC_WP#	DRV2	1	QSPI0_MOSI_IO0	DRV2	1
bit4		DRV1	0		DRV1	0
bit3	—	—	0	—	—	0
bit2	—	—	0	—	—	0
bit1	RPC_INT#	DRV2	1	QSPI1_SPCLK	DRV2	1
bit0		DRV1	0		DRV1	0

	DRV2CTRL2		
	Pin name		Initial value
bit31	—	—	0
bit30	—	—	0
bit29	—	—	0
bit28	—	—	0
bit27	—	—	0
bit26	—	—	0
bit25	—	—	0
bit24	—	—	0
bit23	—	—	0
bit22	—	—	0
bit21	—	—	0
bit20	—	—	0
bit19	—	—	0
bit18	—	—	0
bit17	—	—	0
bit16	—	—	0
bit15	—	—	0
bit14	—	—	0
bit13	—	—	0
bit12	—	—	0
bit11	—	—	0
bit10	—	—	0
bit9	—	—	0
bit8	—	—	0
bit7	—	—	0
bit6	—	—	0
bit5	—	—	0
bit4	—	—	0
bit3	—	—	0
bit2	PCIE1_CLKREQ#	DRV3	1
bit1		DRV2	1
bit0		DRV1	0

Table 7.22 Configuration of Registers in DRV0CTRL3 , DRV1CTRL3 , DRV2CTRL3 , DRV3CTRL3

	DRV0CTRL3			DRV1CTRL3		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	TSN2_LINK	DRV3	1	TSN1_AVTP_CAPTURE	DRV3	1
bit29		DRV2	1		DRV2	1
bit28		DRV1	0		DRV1	0
bit27	—	—	0	—	—	0
bit26	TSN1_LINK	DRV3	1	TSN1_AVTP_MATCH	DRV3	1
bit25		DRV2	1		DRV2	1
bit24		DRV1	0		DRV1	0
bit23	—	—	0	—	—	0
bit22	TSN1_MDC	DRV3	1	TSN1_AVTP_PPS	DRV3	1
bit21		DRV2	1		DRV2	1
bit20		DRV1	0		DRV1	0
bit19	—	—	0	—	—	0
bit18	TSN0_MDC	DRV3	1	TSN0_MAGIC	DRV3	1
bit17		DRV2	1		DRV2	1
bit16		DRV1	0		DRV1	0
bit15	—	—	0	—	—	0
bit14	TSN2_MDC	DRV3	1	TSN1_PHY_INT	DRV3	1
bit13		DRV2	1		DRV2	1
bit12		DRV1	0		DRV1	0
bit11	—	—	0	—	—	0
bit10	TSN0_MDIO	DRV3	1	TSN0_PHY_INT	DRV3	1
bit9		DRV2	1		DRV2	1
bit8		DRV1	0		DRV1	0
bit7	—	—	0	—	—	0
bit6	TSN2_MDIO	DRV3	1	TSN2_PHY_INT	DRV3	1
bit5		DRV2	1		DRV2	1
bit4		DRV1	0		DRV1	0
bit3	—	—	0	—	—	0
bit2	TSN1_MDIO	DRV3	1	TSN0_LINK	DRV3	1
bit1		DRV2	1		DRV2	1
bit0		DRV1	0		DRV1	0

	DRV2CTRL3		
	Pin name		Initial value
bit31	—	—	0
bit30	—	—	0
bit29	—	—	0
bit28	—	—	0
bit27	—	—	0
bit26	—	—	0
bit25	—	—	0
bit24	—	—	0
bit23	—	—	0
bit22	—	—	0
bit21	—	—	0
bit20	—	—	0
bit19	—	—	0
bit18	—	—	0
bit17	—	—	0
bit16	—	—	0
bit15	—	—	0
bit14	—	—	0
bit13	—	—	0
bit12	—	—	0
bit11	—	—	0
bit10	TSN0_AVTP_CAPTURE	DRV3	1
bit9		DRV2	1
bit8		DRV1	0
bit7	—	—	0
bit6	TSN0_AVTP_MATCH	DRV3	1
bit5		DRV2	1
bit4		DRV1	0
bit3	—	—	0
bit2	TSN0_AVTP_PPS	DRV3	1
bit1		DRV2	1
bit0		DRV1	0

Table 7.23 Configuration of Registers in DRV0CTRL4 , DRV1CTRL4 , DRV2CTRL4 , DRV3CTRL4

	DRV0CTRL4			DRV1CTRL4		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	GP4_07	DRV3	1	GP4_15	DRV3	1
bit29		DRV2	1		DRV2	1
bit28		DRV1	0		DRV1	0
bit27	—	—	0	—	—	0
bit26	GP4_06	DRV3	1	GP4_14	DRV3	1
bit25		DRV2	1		DRV2	1
bit24		DRV1	0		DRV1	0
bit23	—	—	0	—	—	0
bit22	GP4_05	DRV3	1	GP4_13	DRV3	1
bit21		DRV2	1		DRV2	1
bit20		DRV1	0		DRV1	0
bit19	—	—	0	—	—	0
bit18	GP4_04	DRV3	1	GP4_12	DRV3	1
bit17		DRV2	1		DRV2	1
bit16		DRV1	0		DRV1	0
bit15	—	—	0	—	—	0
bit14	GP4_03	DRV3	1	GP4_11	DRV3	1
bit13		DRV2	1		DRV2	1
bit12		DRV1	0		DRV1	0
bit11	—	—	0	—	—	0
bit10	GP4_02	DRV3	1	GP4_10	DRV3	1
bit9		DRV2	1		DRV2	1
bit8		DRV1	0		DRV1	0
bit7	—	—	0	—	—	0
bit6	GP4_01	DRV3	1	GP4_09	DRV3	1
bit5		DRV2	1		DRV2	1
bit4		DRV1	0		DRV1	0
bit3	—	—	0	—	—	0
bit2	GP4_00	DRV3	1	GP4_08	DRV3	1
bit1		DRV2	1		DRV2	1
bit0		DRV1	0		DRV1	0

	DRV2CTRL4			DRV3CTRL4		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	MSPI0CSS1	DRV3	1	—	—	0
bit29		DRV2	1	—	—	0
bit28		DRV1	0	—	—	0
bit27	—	—	0	—	—	0
bit26	MSPI0SO/MSPI0D	DRV3	1	MSPI1CSS1	DRV3	1
bit25	CS	DRV2	1		DRV2	1
bit24		DRV1	0		DRV1	0
bit23	—	—	0	—	—	0
bit22	MSPI0SI	DRV3	1	MSPI1CSS2	DRV3	1
bit21		DRV2	1		DRV2	1
bit20		DRV1	0		DRV1	0
bit19	—	—	0	—	—	0
bit18	MSPI0SC	DRV3	1	MSPI1SC	DRV3	1
bit17		DRV2	1		DRV2	1
bit16		DRV1	0		DRV1	0
bit15	—	—	0	—	—	0
bit14	GP4_19	DRV3	1	MSPI1CSS0	DRV3	1
bit13		DRV2	1		DRV2	1
bit12		DRV1	0		DRV1	0
bit11	—	—	0	—	—	0
bit10	GP4_18	DRV3	1	MSPI1SO/MSPI1D	DRV3	1
bit9		DRV2	1	CS	DRV2	1
bit8		DRV1	0		DRV1	0
bit7	—	—	0		—	0
bit6	GP4_17	DRV3	1	MSPI1SI	DRV3	1
bit5		DRV2	1		DRV2	1
bit4		DRV1	0		DRV1	0
bit3	—	—	0		—	0
bit2	GP4_16	DRV3	1	MSPI0CSS0	DRV3	1
bit1		DRV2	1		DRV2	1
bit0		DRV1	0		DRV1	0

Table 7.24 Configuration of Registers in DRV0CTRL5 , DRV1CTRL5, DRV2CTRL5, DRV3CTRL5

	DRV0CTRL5			DRV1CTRL5		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	ETNB0RXD3	DRV3	1	ETNB0TXCLK	DRV3	1
bit29		DRV2	1		DRV2	1
bit28		DRV1	0		DRV1	0
bit27	—	—	0	—	—	0
bit26	ETNB0RXER	DRV3	1	ETNB0TXD3	DRV3	1
bit25		DRV2	1		DRV2	1
bit24		DRV1	0		DRV1	0
bit23	—	—	0	—	—	0
bit22	ETNB0MDC	DRV3	1	ETNB0TXER	DRV3	1
bit21		DRV2	1		DRV2	1
bit20		DRV1	0		DRV1	0
bit19	—	—	0	—	—	0
bit18	ETNB0LINKSTA	DRV3	1	ETNB0RXCLK	DRV3	1
bit17		DRV2	1		DRV2	1
bit16		DRV1	0		DRV1	0
bit15	—	—	0	—	—	0
bit14	ETNB0WOL	DRV3	1	ETNB0RXD0	DRV3	1
bit13		DRV2	1		DRV2	1
bit12		DRV1	0		DRV1	0
bit11	—	—	0	—	—	0
bit10	ETNB0MD	DRV3	1	ETNB0RXDV	DRV3	1
bit9		DRV2	1		DRV2	1
bit8		DRV1	0		DRV1	0
bit7	—	—	0	—	—	0
bit6	RIIC0SDA	DRV3	1	ETNB0RXD2	DRV3	1
bit5		DRV2	1		DRV2	1
bit4		DRV1	0		DRV1	0
bit3	—	—	0	—	—	0
bit2	RIIC0SCL	DRV3	1	ETNB0RXD1	DRV3	1
bit1		DRV2	1		DRV2	1
bit0		DRV1	0		DRV1	0

	DRV2CTRL5			DRV3CTRL5		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	—	—	0
bit29	—	—	0	—	—	0
bit28	—	—	0	—	—	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	—	—	0	—	—	0
bit24	—	—	0	—	—	0
bit23	—	—	0	—	—	0
bit22	—	—	0	—	—	0
bit21	—	—	0	—	—	0
bit20	—	—	0	—	—	0
bit19	—	—	0	—	—	0
bit18	—	—	0	—	—	0
bit17	—	—	0	—	—	0
bit16	—	—	0	—	—	0
bit15	—	—	0	—	—	0
bit14	ETNB0TXD0	DRV3	1	—	—	0
bit13		DRV2	1	—	—	0
bit12		DRV1	0	—	—	0
bit11	—	—	0	—	—	0
bit10	ETNB0TXEN	DRV3	1	—	—	0
bit9		DRV2	1	—	—	0
bit8		DRV1	0	—	—	0
bit7	—	—	0	—	—	0
bit6	ETNB0TXD2	DRV3	1	—	—	0
bit5		DRV2	1	—	—	0
bit4		DRV1	0	—	—	0
bit3	—	—	0	—	—	0
bit2	ETNB0TXD1	DRV3	1	—	—	0
bit1		DRV2	1	—	—	0
bit0		DRV1	0	—	—	0

Table 7.25 Configuration of Registers in DRV0CTRL6 , DRV1CTRL6 , DRV2CTRL6 , DRV3CTRL6

	DRV0CTRL6			DRV1CTRL6		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	RLIN34RX/INTP20	DRV3	1	RLIN30RX/INTP16	DRV3	1
bit29		DRV2	1		DRV2	1
bit28		DRV1	0		DRV1	0
bit27	—	—	0	—	—	0
bit26	RLIN34TX	DRV3	1	RLIN30TX	DRV3	1
bit25		DRV2	1		DRV2	1
bit24		DRV1	0		DRV1	0
bit23	—	—	0	—	—	0
bit22	RLIN35RX/INTP21	DRV3	1	RLIN31RX/INTP17	DRV3	1
bit21		DRV2	1		DRV2	1
bit20		DRV1	0		DRV1	0
bit19	—	—	0	—	—	0
bit18	RLIN35TX	DRV3	1	RLIN31TX	DRV3	1
bit17		DRV2	1		DRV2	1
bit16		DRV1	0		DRV1	0
bit15	—	—	0	—	—	0
bit14	RLIN36RX/INTP22	DRV3	1	RLIN32RX/INTP18	DRV3	1
bit13		DRV2	1		DRV2	1
bit12		DRV1	0		DRV1	0
bit11	—	—	0	—	—	0
bit10	RLIN36TX	DRV3	1	RLIN32TX	DRV3	1
bit9		DRV2	1		DRV2	1
bit8		DRV1	0		DRV1	0
bit7	—	—	0	—	—	0
bit6	RLIN37RX/INTP23	DRV3	1	RLIN33RX_INTP19	DRV3	1
bit5		DRV2	1		DRV2	1
bit4		DRV1	0		DRV1	0
bit3	—	—	0	—	—	0
bit2	RLIN37TX	DRV3	1	RLIN33TX	DRV3	1
bit1		DRV2	1		DRV2	1
bit0		DRV1	0		DRV1	0

	DRV2CTRL6			DRV3CTRL6		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	PRESETOUT1#	DRV3	1
bit29	—	—	0		DRV2	1
bit28	—	—	0		DRV1	0
bit27	—	—	0	—	—	0
bit26	NMI1	DRV3	1	—	—	0
bit25		DRV2	1	—	—	0
bit24		DRV1	0	—	—	0
bit23	—	—	0	—	—	0
bit22	INTP32	DRV3	1	—	—	0
bit21		DRV2	1	—	—	0
bit20		DRV1	0	—	—	0
bit19	—	—	0	—	—	0
bit18	INTP33	DRV3	1	—	—	0
bit17		DRV2	1	—	—	0
bit16		DRV1	0	—	—	0
bit15	—	—	0	—	—	0
bit14	INTP34	DRV3	1	—	—	0
bit13		DRV2	1	—	—	0
bit12		DRV1	0	—	—	0
bit11	—	—	0	—	—	0
bit10	INTP35	DRV3	1	—	—	0
bit9		DRV2	1	—	—	0
bit8		DRV1	0	—	—	0
bit7	—	—	0	—	—	0
bit6	INTP36	DRV3	1	—	—	0
bit5		DRV2	1	—	—	0
bit4		DRV1	0	—	—	0
bit3	—	—	0	—	—	0
bit2	INTP37	DRV3	1	—	—	0
bit1		DRV2	1	—	—	0
bit0		DRV1	0	—	—	0

Table 7.26 Configuration of Registers in DRVCTRL7_0-3 DRV0CTRL7, DRV1CTRL7, DRV2CTRL7, DRV3CTRL7

	DRV0CTRL7			DRV1CTRL7		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	CAN3RX/INTP3	DRV3	1	CAN7RX/INTP7	DRV3	1
bit29		DRV2	1		DRV2	1
bit28		DRV1	0		DRV1	0
bit27	—	—	0	—	—	0
bit26	CAN3TX	DRV3	1	CAN7TX	DRV3	1
bit25		DRV2	1		DRV2	1
bit24		DRV1	0		DRV1	0
bit23	—	—	0	—	—	0
bit22	CAN2RX/INTP2	DRV3	1	CAN6RX/INTP6	DRV3	1
bit21		DRV2	1		DRV2	1
bit20		DRV1	0		DRV1	0
bit19	—	—	0	—	—	0
bit18	CAN2TX	DRV3	1	CAN6TX	DRV3	1
bit17		DRV2	1		DRV2	1
bit16		DRV1	0		DRV1	0
bit15	—	—	0	—	—	0
bit14	CAN1RX/INTP1	DRV3	1	CAN5RX/INTP5	DRV3	1
bit13		DRV2	1		DRV2	1
bit12		DRV1	0		DRV1	0
bit11	—	—	0	—	—	0
bit10	CAN1TX	DRV3	1	CAN5TX	DRV3	1
bit9		DRV2	1		DRV2	1
bit8		DRV1	0		DRV1	0
bit7	—	—	0	—	—	0
bit6	CAN0RX/INTP0	DRV3	1	CAN4RX/INTP4	DRV3	1
bit5		DRV2	1		DRV2	1
bit4		DRV1	0		DRV1	0
bit3	—	—	0	—	—	0
bit2	CAN0TX	DRV3	1	CAN4TX	DRV3	1
bit1		DRV2	1		DRV2	1
bit0		DRV1	0		DRV1	0

	DRV2CTRL7			DRV3CTRL7		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	CAN11RX/INTP11	DRV3	1	CAN15RX/INTP15	DRV3	1
bit29		DRV2	1		DRV2	1
bit28		DRV1	0		DRV1	0
bit27	—	—	0	—	—	0
bit26	CAN11TX	DRV3	1	CAN15TX	DRV3	1
bit25		DRV2	1		DRV2	1
bit24		DRV1	0		DRV1	0
bit23	—	—	0	—	—	0
bit22	CAN10RX/INTP10	DRV3	1	CAN14RX_INTP14	DRV3	1
bit21		DRV2	1		DRV2	1
bit20		DRV1	0		DRV1	0
bit19	—	—	0	—	—	0
bit18	CAN10TX	DRV3	1	CAN14TX	DRV3	1
bit17		DRV2	1		DRV2	1
bit16		DRV1	0		DRV1	0
bit15	—	—	0	—	—	0
bit14	CAN9RX/INTP9	DRV3	1	CAN14RX/INTP13	DRV3	1
bit13		DRV2	1		DRV2	1
bit12		DRV1	0		DRV1	0
bit11	—	—	0	—	—	0
bit10	CAN9TX	DRV3	1	CAN13TX	DRV3	1
bit9		DRV2	1		DRV2	1
bit8		DRV1	0		DRV1	0
bit7	—	—	0	—	—	0
bit6	CAN8RX/INTP8	DRV3	1	CAN12RX/INTP12	DRV3	1

	DRV2CTRL7			DRV3CTRL7		
	Pin name		Initial value	Pin name		Initial value
bit5		DRV2	1		DRV2	1
bit4		DRV1	0		DRV1	0
bit3	—	—	0	—	—	0
bit2	CAN8TX	DRV3	1	CAN12TX	DRV3	1
bit1		DRV2	1		DRV2	1
bit0		DRV1	0		DRV1	0

Table 7.27 Configuration of Registers in DRV0CTRLSYS0, DRV1CTRLSYS0

	DRV0CTRLSYS			DRV1CTRLSYS		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	—	—	0
bit29	—	—	0	—	—	0
bit28	—	—	0	—	—	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	—	—	0	—	—	0
bit24	—	—	0	—	—	0
bit23	—	—	0	—	—	0
bit22	—	—	0	—	—	0
bit21	—	—	0	—	—	0
bit20	—	—	0	—	—	0
bit19	—	—	0	—	—	0
bit18	—	—	0	—	—	0
bit17	—	—	0	DCUTCK0	DRV2	1
bit16	—	—	0		DRV1	0
bit15	—	—	0	—	—	0
bit14	—	—	0	—	—	0
bit13	—	—	0	DCUTDO0	—	1
bit12	—	—	0		—	0
bit11	—	—	0	—	—	0
bit10	—	—	0	—	—	0
bit9	—	—	0	DCUTDI0	DRV2	1
bit8	—	—	0		DRV1	0
bit7	—	—	0	—	—	0
bit6	—	—	0	—	—	0
bit5	—	—	0	DCURDY0#	DRV2	1
bit4	—	—	0		DRV1	0
bit3	—	—	0	—	—	0
bit2	PRESETOUT0#	DRV3	1	—	—	0
bit1	—	DRV2	1	DCUTMS0	DRV2	1
bit0	—	DRV1	0		DRV1	0

7.2.7 POWER Condition Control Register (POCn)

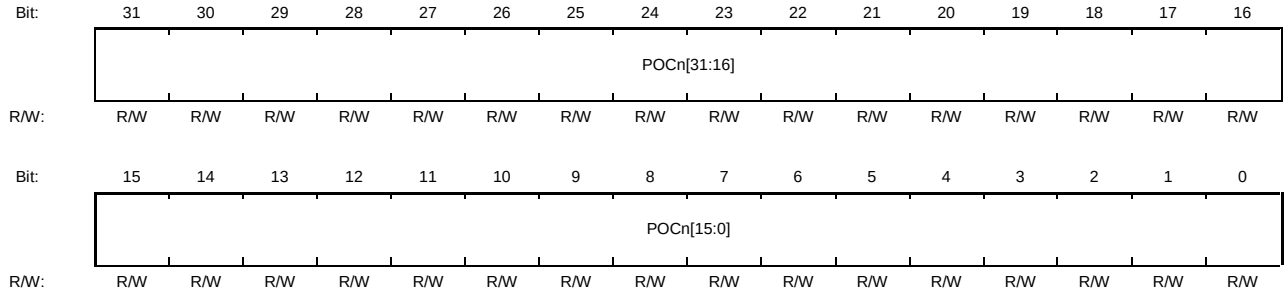
Function: Each bit in POCn / POCSYS must be set according to IO voltage level that is supplied to the pin.

0: 1.8V 1: 3.3V

Supply voltage	Setting register	Usage
1.8V	0	Possible
1.8V	1	Do not use
3.3V	0	Do not set (broken)
3.3V	1	Possible

0: 2.5V 1: 3.3V

Supply voltage	Setting register	Usage
2.5V	0	Possible
2.5V	1	Do not use
3.3V	0	Do not set (broken)
3.3V	1	Possible



Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Note: The power domain is common for each function.

When you use an unused port as GPIO, you must be careful about the voltage.

Table 7.28 Configuration of Registers in POC0 , POC1

	POC0			POC1		
	Pin name	Voltage	Initial value	Pin name	Voltage	Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	—	—	0
bit29	—	—	0	—	—	0
bit28	—	—	0	—	—	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	—	—	0	—	—	0
bit24	—	—	0	SD_WP	1.8V / 3.3V	1
bit23	—	—	0	SD_CD	1.8V / 3.3V	1
bit22	—	—	0	MMC_SD_CMD	1.8V / 3.3V	1
bit21	—	—	0	MMC_D7	1.8V / 3.3V	1
bit20	IRQ3	1.8V / 3.3V	1	MMC_DS	1.8V / 3.3V	1
bit19	IRQ2	1.8V / 3.3V	1	MMC_D6	1.8V / 3.3V	1
bit18	IRQ1	1.8V / 3.3V	1	MMC_D4	1.8V / 3.3V	1
bit17	IRQ0	1.8V / 3.3V	1	MMC_D5	1.8V / 3.3V	1
bit16	MSIOF0_SS2	1.8V / 3.3V	1	MMC_SD_D3	1.8V / 3.3V	1
bit15	MSIOF0_SS1	1.8V / 3.3V	1	MMC_SD_D2	1.8V / 3.3V	1
bit14	MSIOF0_SCK	1.8V / 3.3V	1	MMC_SD_D1	1.8V / 3.3V	1
bit13	MSIOF0_TXD	1.8V / 3.3V	1	MMC_SD_D0	1.8V / 3.3V	1
bit12	MSIOF0_RXD	1.8V / 3.3V	1	MMC_SD_CLK	1.8V / 3.3V	1
bit11	MSIOF0_SYNC	1.8V / 3.3V	1	GP1_11	1.8V / 3.3V	1
bit10	CTS0#	1.8V / 3.3V	1	GP1_10	1.8V / 3.3V	1
bit9	RTS0#	1.8V / 3.3V	1	GP1_09	1.8V / 3.3V	1
bit8	SCK0	1.8V / 3.3V	1	GP1_08	1.8V / 3.3V	1
bit7	TX0	1.8V / 3.3V	1	GP1_07	1.8V / 3.3V	1
bit6	RX0	1.8V / 3.3V	1	GP1_06	1.8V / 3.3V	1
bit5	HRTS0#	1.8V / 3.3V	1	GP1_05	1.8V / 3.3V	1
bit4	HCTS0#	1.8V / 3.3V	1	GP1_04	1.8V / 3.3V	1
bit3	HTX0	1.8V / 3.3V	1	GP1_03	1.8V / 3.3V	1
bit2	HRX0	1.8V / 3.3V	1	GP1_02	1.8V / 3.3V	1
bit1	HSCK0	1.8V / 3.3V	1	GP1_01	1.8V / 3.3V	1
bit0	SCIF_CLK	1.8V / 3.3V	1	GP1_00	1.8V / 3.3V	1

Table 7.29 Configuration of Registers in POC2 , POC3

	POC2			POC3		
	Pin name	Voltage	Initial value	Pin name	Voltage	Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	—	—	0
bit29	—	—	0	—	—	0
bit28	—	—	0	—	—	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	—	—	0	—	—	0
bit24	—	—	0	—	—	0
bit23	—	—	0	—	—	0
bit22	—	—	0	—	—	0
bit21	—	—	0	—	—	0
bit20	—	—	0	—	—	0
bit19	—	—	0	—	—	0
bit18	—	—	0	TSN0_AVTP_CAPTURE	1.8V / 3.3V	1
bit17	—	—	0	TSN0_AVTP_MATCH	1.8V / 3.3V	1
bit16	—	—	0	TSN0_AVTP_PPS	1.8V / 3.3V	1
bit15	—	—	0	TSN1_AVTP_CAPTURE	1.8V / 3.3V	1
bit14	—	—	0	TSN1_AVTP_MATCH	1.8V / 3.3V	1
bit13	—	—	0	TSN1_AVTP_PPS	1.8V / 3.3V	1
bit12	—	—	0	TSN0_MAGIC	1.8V / 3.3V	1
bit11	—	—	0	TSN1_PHY_INT	1.8V / 3.3V	1
bit10	—	—	0	TSN0_PHY_INT	1.8V / 3.3V	1
bit9	—	—	0	TSN2_PHY_INT	1.8V / 3.3V	1
bit8	—	—	0	TSN0_LINK	1.8V / 3.3V	1
bit7	—	—	0	TSN2_LINK	1.8V / 3.3V	1
bit6	—	—	0	TSN1_LINK	1.8V / 3.3V	1
bit5	—	—	0	TSN1_MDC	1.8V / 3.3V	1
bit4	—	—	0	TSN0_MDC	1.8V / 3.3V	1
bit3	—	—	0	TSN2_MDC	1.8V / 3.3V	1
bit2	—	—	0	TSN0_MDIO	1.8V / 3.3V	1
bit1	—	—	0	TSN2_MDIO	1.8V / 3.3V	1
bit0	—	—	0	TSN1_MDIO	1.8V / 3.3V	1

Table 7.30 Configuration of Registers in POC4 , POC5

	POC4			POC5		
	Pin name	Voltage	Initial value	Pin name	Voltage	Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	—	—	0
bit29	—	—	0	—	—	0
bit28	—	—	0	—	—	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	—	—	0	—	—	0
bit24	—	—	0	—	—	0
bit23	—	—	0	—	—	0
bit22	—	—	0	—	—	0
bit21	—	—	0	—	—	0
bit20	—	—	0	—	—	0
bit19	—	—	0	—	—	0
bit18	—	—	0	—	—	0
bit17	—	—	0	—	—	0
bit16	—	—	0	—	—	0
bit15	—	—	0	—	—	0
bit14	—	—	0	—	—	0
bit13	—	—	0	—	—	0
bit12	—	—	0	—	—	0
bit11	—	—	0	—	—	0
bit10	—	—	0	—	—	0
bit9	—	—	0	—	—	0
bit8	—	—	0	—	—	0
bit7	—	—	0	—	—	0
bit6	—	—	0	—	—	0
bit5	—	—	0	—	—	0
bit4	—	—	0	—	—	0
bit3	—	—	0	—	—	0
bit2	—	—	0	—	—	0
bit1	—	—	0	—	—	0
bit0	—	—	0	—	—	0

Table 7.31 Configuration of Registers in POC6 , POC7

	POC6			POC7		
	Pin name	Voltage	Initial value	Pin name	Voltage	Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	—	—	0
bit29	—	—	0	—	—	0
bit28	—	—	0	—	—	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	—	—	0	—	—	0
bit24	—	—	0	—	—	0
bit23	—	—	0	—	—	0
bit22	—	—	0	—	—	0
bit21	—	—	0	—	—	0
bit20	—	—	0	—	—	0
bit19	—	—	0	—	—	0
bit18	—	—	0	—	—	0
bit17	—	—	0	—	—	0
bit16	—	—	0	—	—	0
bit15	—	—	0	—	—	0
bit14	—	—	0	—	—	0
bit13	—	—	0	—	—	0
bit12	—	—	0	—	—	0
bit11	—	—	0	—	—	0
bit10	—	—	0	—	—	0
bit9	—	—	0	—	—	0
bit8	—	—	0	—	—	0
bit7	—	—	0	—	—	0
bit6	—	—	0	—	—	0
bit5	—	—	0	—	—	0
bit4	—	—	0	—	—	0
bit3	—	—	0	—	—	0
bit2	—	—	0	—	—	0
bit1	—	—	0	—	—	0
bit0	—	—	0	—	—	0

Table 7.32 Configuration of Registers in POCSYS

	POCSYS		
	Pin name	Voltage	Initial value
bit31	—	—	0
bit30	—	—	0
bit29	—	—	0
bit28	—	—	0
bit27	—	—	0
bit26	—	—	0
bit25	—	—	0
bit24	—	—	0
bit23	—	—	0
bit22	—	—	0
bit21	—	—	0
bit20	—	—	0
bit19	—	—	0
bit18	—	—	0
bit17	—	—	0
bit16	—	—	0
bit15	—	—	0
bit14	—	—	0
bit13	—	—	0
bit12	—	—	0
bit11	—	—	0
bit10	—	—	0
bit9	—	—	0
bit8	—	—	0
bit7	—	—	0
bit6	—	—	0
bit5	—	—	0
bit4	—	—	0
bit3	—	—	0
bit2	—	—	0
bit1	—	—	0
bit0	—	—	0

7.2.8 LSI pin pull-enable register (PUENn)

Function: PUENn / PUENSYS performs on / off control of the pull resistors.

0: Pull-up / down function is disabled.

1: Pull-up / down function is enabled.

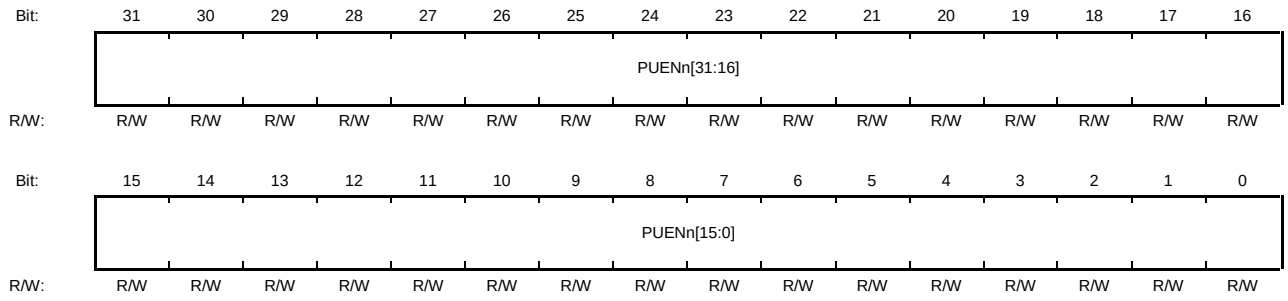


Table 7.33 Configuration of Registers in PUEN0 , PUEN1

	PUEN0		PUEN1	
	Pin name	Initial value	Pin name	Initial value
bit31	—	0	—	0
bit30	—	0	—	0
bit29	—	0	—	0
bit28	—	0	—	0
bit27	—	0	—	0
bit26	—	0	—	0
bit25	—	0	—	0
bit24	—	0	SD_WP	0
bit23	—	0	SD_CD	0
bit22	—	0	MMC_SD_CMD	0
bit21	—	0	MMC_D7	0
bit20	IRQ3	0	MMC_DS	0
bit19	IRQ2	0	MMC_D6	0
bit18	IRQ1	0	MMC_D4	0
bit17	IRQ0	0	MMC_D5	0
bit16	MSIOF0_SS2	0	MMC_SD_D3	0
bit15	MSIOF0_SS1	0	MMC_SD_D2	0
bit14	MSIOF0_SCK	0	MMC_SD_D1	0
bit13	MSIOF0_TXD	0	MMC_SD_D0	0
bit12	MSIOF0_RXD	0	MMC_SD_CLK	0
bit11	MSIOF0_SYNC	0	GP1_11	0
bit10	CTS0#	0	GP1_10	0
bit9	RTS0#	0	GP1_09	0
bit8	SCK0	0	GP1_08	0
bit7	TX0	0	GP1_07	0
bit6	RX0	0	GP1_06	0
bit5	HRTS0#	0	GP1_05	0
bit4	HCTS0#	0	GP1_04	0
bit3	HTX0	0	GP1_03	0
bit2	HRX0	0	GP1_02	0
bit1	HSCK0	0	GP1_01	0
bit0	SCIF_CLK	1	GP1_00	0

Table 7.34 Configuration of Registers in PUEN2 , PUEN3

	PUEN2		PUEN3	
	Pin name	Initial value	Pin name	Initial value
bit31	—	0	—	0
bit30	—	0	—	0
bit29	—	0	—	0
bit28	—	0	—	0
bit27	—	0	—	0
bit26	—	0	—	0
bit25	—	0	—	0
bit24	—	0	—	0
bit23	—	0	—	0
bit22	—	0	—	0
bit21	—	0	—	0
bit20	—	0	—	0
bit19	—	0	—	0
bit18	—	0	TSN0_AVTP_CAPTURE	1
bit17	—	0	TSN0_AVTP_MATCH	1
bit16	PCIE1_CLKREQ#	0	TSN0_AVTP_PPS	0
bit15	PCIE0_CLKREQ#	0	TSN1_AVTP_CAPTURE	1
bit14	QSPI0_IO3	0	TSN1_AVTP_MATCH	1
bit13	QSPI0_SSL	0	TSN1_AVTP_PPS	0
bit12	QSPI0_MISO_IO1	0	TSN0_MAGIC	0
bit11	QSPI0_IO2	0	TSN1_PHY_INT	1
bit10	QSPI0_SPCLK	0	TSN0_PHY_INT	1
bit9	QSPI0_MOSI_IO0	0	TSN2_PHY_INT	1
bit8	QSPI1_SPCLK	0	TSN0_LINK	1
bit7	QSPI1_MOSI_IO0	0	TSN2_LINK	1
bit6	QSPI1_IO2	0	TSN1_LINK	1
bit5	QSPI1_MISO_IO1	0	TSN1_MDC	0
bit4	QSPI1_IO3	0	TSN0_MDC	0
bit3	QSPI1_SSL	0	TSN2_MDC	0
bit2	RPC_RESET#	0	TSN0_MDIO	1
bit1	RPC_WP#	0	TSN2_MDIO	1
bit0	RPC_INT#	1	TSN1_MDIO	1

Table 7.35 Configuration of Registers in PUEN4 , PUEN5, PUEN6 , PUEN7

	PUEN4		PUEN5	
	Pin name	Initial value	Pin name	Initial value
bit31	—	0	—	0
bit30	MSPI1CSS1	0	—	0
bit29	MSPI1CSS2	0	—	0
bit28	MSPI1SC	0	—	0
bit27	MSPI1CSS0	0	—	0
bit26	MSPI1SO/MSPI1DCS	0	—	0
bit25	MSPI1SI	0	—	0
bit24	MSPI0CSS0	0	—	0
bit23	MSPI0CSS1	0	—	0
bit22	MSPI0SO/MSPI0DCS	0	—	0
bit21	MSPI0SI	0	—	0
bit20	MSPI0SC	0	—	0
bit19	GP4_19	0	ETNB0TXD0	0
bit18	GP4_18	0	ETNB0TXEN	0
bit17	GP4_17	0	ETNB0TXD2	0
bit16	GP4_16	0	ETNB0TXD1	0
bit15	GP4_15	0	ETNB0TXCLK	0
bit14	GP4_14	0	ETNB0TXD3	0
bit13	GP4_13	0	ETNB0TXER	0
bit12	GP4_12	0	ETNB0RXCLK	0
bit11	GP4_11	0	ETNB0RXD0	0
bit10	GP4_10	0	ETNB0RXDV	0
bit9	GP4_09	0	ETNB0RXD2	0
bit8	GP4_08	0	ETNB0RXD1	0
bit7	GP4_07	0	ETNB0RXD3	0
bit6	GP4_06	0	ETNB0RXER	0
bit5	GP4_05	0	ETNB0MDC	0
bit4	GP4_04	0	ETNB0LINKSTA	0
bit3	GP4_03	0	ETNB0WOL	0
bit2	GP4_02	0	ETNB0MD	0
bit1	GP4_01	0	RIIC0SDA	0
bit0	GP4_00	0	RIIC0SCL	0

	PUEN6		PUEN7	
	Pin name	Initial value	Pin name	Initial value
bit31	PRESETOUT1#	0	CAN15RX/INTP15	0
bit30	—	0	CAN15TX	0
bit29	—	0	CAN14RX/INTP14	0
bit28	—	0	CAN14TX	0
bit27	—	0	CAN13RX/INTP13	0
bit26	—	0	CAN13TX	0
bit25	—	0	CAN12RX/INTP12	0
bit24	—	0	CAN12TX	0
bit23	—	0	CAN11RX/INTP11	0
bit22	NMI1	0	CAN11TX	0
bit21	INTP32	0	CAN10RX/INTP10	0
bit20	INTP33	0	CAN10TX	0
bit19	INTP34	0	CAN9RX/INTP9	0
bit18	INTP35	0	CAN9TX	0
bit17	INTP36	0	CAN8RX/INTP8	0
bit16	INTP37	0	CAN8TX	0
bit15	RLIN30RX/INTP16	0	CAN7RX/INTP7	0
bit14	RLIN30TX	0	CAN7TX	0
bit13	RLIN31RX/INTP17	0	CAN6RX/INTP6	0
bit12	RLIN31TX	0	CAN6TX	0
bit11	RLIN32RX/INTP18	0	CAN5RX/INTP5	0
bit10	RLIN32TX	0	CAN5TX	0
bit9	RLIN33RX/INTP19	0	CAN4RX/INTP4	0
bit8	RLIN33TX	0	CAN4TX	0
bit7	RLIN34RX/INTP20	0	CAN3RX/INTP3	0
bit6	RLIN34TX	0	CAN3TX	0
bit5	RLIN35RX/INTP21	0	CAN2RX/INTP2	0
bit4	RLIN35TX	0	CAN2TX	0
bit3	RLIN36RX/INTP22	0	CAN1RX/INTP1	0
bit2	RLIN36TX	0	CAN1TX	0
bit1	RLIN37RX/INTP23	0	CAN0RX/INTP0	0
bit0	RLIN37TX	0	CAN0TX	0

Table 7.36 Configuration of Registers in PUENSYS0, PUENSYS1

	PUENSYS0		PUENSYS1	
	Pin name	Initial value	Pin name	Initial value
bit31	—	0	—	0
bit30	—	0	—	0
bit29	—	0	—	0
bit28	—	0	—	0
bit27	—	0	—	0
bit26	—	0	—	0
bit25	—	0	—	0
bit24	—	0	—	0
bit23	—	0	—	0
bit22	—	0	—	0
bit21	—	0	—	0
bit20	—	0	—	0
bit19	—	0	—	0
bit18	—	0	—	0
bit17	—	0	—	0
bit16	—	0	—	0
bit15	—	0	—	0
bit14	—	0	—	0
bit13	—	0	—	0
bit12	—	0	—	0
bit11	—	0	—	0
bit10	—	0	MSYN#	1
bit9	—	0	EVTI#	1
bit8	—	0	DCUTCK1	1
bit7	—	0	DCUTDI1	1
bit6	—	0	DCUTMS1	1
bit5	—	0	DCUTMS0	1
bit4	—	0	DCUTDI0	1
bit3	—	0	DCUTCK0	1
bit2	—	0	DCUTRST1#	1
bit1	EXTALR	0	DCUTRST0#	1
bit0	PRESETOUT0#	0	ERROROUT_M#	0

7.2.9 LSI pin pull-up / down control Register (PUDn / PUDSYS)

Function: PUDn / PUDSYS performs pull-up / pull-down control of the pull resistors.

0: Pull-down is enabled.

1: Pull-up is enabled.

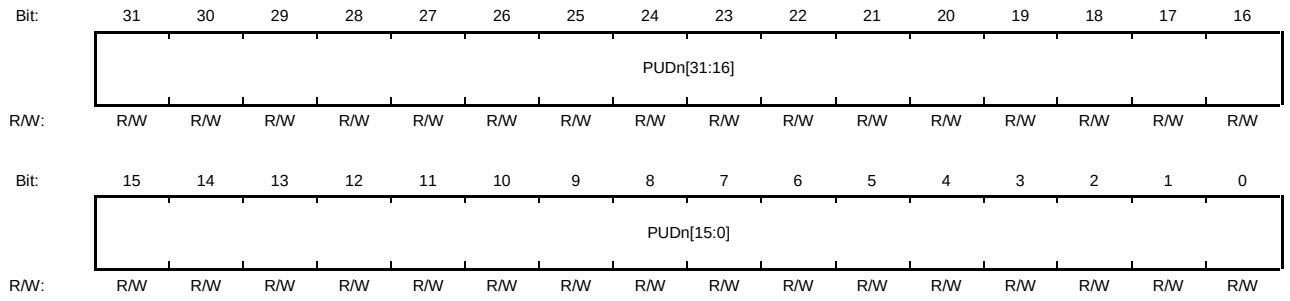


Table 7.37 Configuration of Registers in PUD0 , PUD1

	PUD0		PUD1	
	Pin name	Initial value	Pin name	Initial value
bit31	—	0	—	0
bit30	—	0	—	0
bit29	—	0	—	0
bit28	—	0	—	0
bit27	—	0	—	0
bit26	—	0	—	0
bit25	—	0	—	0
bit24	—	0	SD_WP	0
bit23	—	0	SD_CD	0
bit22	—	0	MMC_SD_CMD	0
bit21	—	0	MMC_D7	0
bit20	IRQ3	0	MMC_DS	0
bit19	IRQ2	0	MMC_D6	0
bit18	IRQ1	0	MMC_D4	0
bit17	IRQ0	0	MMC_D5	0
bit16	MSIOF0_SS2	0	MMC_SD_D3	0
bit15	MSIOF0_SS1	0	MMC_SD_D2	0
bit14	MSIOF0_SCK	0	MMC_SD_D1	0
bit13	MSIOF0_TXD	0	MMC_SD_D0	0
bit12	MSIOF0_RXD	0	MMC_SD_CLK	0
bit11	MSIOF0_SYNC	0	GP1_11	0
bit10	CTS0#	0	GP1_10	0
bit9	RTS0#	0	GP1_09	0
bit8	SCK0	0	GP1_08	0
bit7	TX0	0	GP1_07	0
bit6	RX0	0	GP1_06	0
bit5	HRTS0#	0	GP1_05	0
bit4	HCTS0#	0	GP1_04	0
bit3	HTX0	0	GP1_03	0
bit2	HRX0	0	GP1_02	0
bit1	HSCK0	0	GP1_01	0
bit0	SCIF_CLK	1	GP1_00	0

Table 7.38 Configuration of Registers in PUD2 , PUD3

	PUD2		PUD3	
	Pin name	Initial value	Pin name	Initial value
bit31	—	0	—	0
bit30	—	0	—	0
bit29	—	0	—	0
bit28	—	0	—	0
bit27	—	0	—	0
bit26	—	0	—	0
bit25	—	0	—	0
bit24	—	0	—	0
bit23	—	0	—	0
bit22	—	0	—	0
bit21	—	0	—	0
bit20	—	0	—	0
bit19	—	0	—	0
bit18	—	0	TSN0_AVTP_CAPTURE	1
bit17	—	0	TSN0_AVTP_MATCH	0
bit16	PCIE1_CLKREQ#	0	TSN0_AVTP_PPS	0
bit15	PCIE0_CLKREQ#	0	TSN1_AVTP_CAPTURE	1
bit14	QSPI0_IO3	0	TSN1_AVTP_MATCH	0
bit13	QSPI0_SSL	0	TSN1_AVTP_PPS	0
bit12	QSPI0_MISO_IO1	0	TSN0_MAGIC	0
bit11	QSPI0_IO2	0	TSN1_PHY_INT	0
bit10	QSPI0_SPCLK	0	TSN0_PHY_INT	0
bit9	QSPI0_MOSI_IO0	0	TSN2_PHY_INT	0
bit8	QSPI1_SPCLK	0	TSN0_LINK	0
bit7	QSPI1_MOSI_IO0	0	TSN2_LINK	0
bit6	QSPI1_IO2	0	TSN1_LINK	0
bit5	QSPI1_MISO_IO1	0	TSN1_MDC	0
bit4	QSPI1_IO3	0	TSN0_MDC	0
bit3	QSPI1_SSL	0	TSN2_MDC	0
bit2	RPC_RESET#	0	TSN0_MDIO	0
bit1	RPC_WP#	0	TSN2_MDIO	0
bit0	RPC_INT#	1	TSN1_MDIO	0

Table 7.39 Configuration of Registers in PUD4, PUD5, PUD6, PUD7

	PUD4		PUD5	
	Pin name	Initial value	Pin name	Initial value
bit31	—	0	—	0
bit30	MSPI1CSS1	0	—	0
bit29	MSPI1CSS2	0	—	0
bit28	MSPI1SC	0	—	0
bit27	MSPI1CSS0	0	—	0
bit26	MSPI1SO/MSPI1DCS	0	—	0
bit25	MSPI1SI	0	—	0
bit24	MSPI0CSS0	0	—	0
bit23	MSPI0CSS1	0	—	0
bit22	MSPI0SO/MSPI0DCS	0	—	0
bit21	MSPI0SI	0	—	0
bit20	MSPI0SC	0	—	0
bit19	GP4_19	0	ETNB0TXD0	0
bit18	GP4_18	0	ETNB0TXEN	0
bit17	GP4_17	0	ETNB0TXD2	0
bit16	GP4_16	0	ETNB0TXD1	0
bit15	GP4_15	0	ETNB0TXCLK	0
bit14	GP4_14	0	ETNB0TXD3	0
bit13	GP4_13	0	ETNB0TXER	0
bit12	GP4_12	0	ETNB0RXCLK	0
bit11	GP4_11	0	ETNB0RXD0	0
bit10	GP4_10	0	ETNB0RXDV	0
bit9	GP4_09	0	ETNB0RXD2	0
bit8	GP4_08	0	ETNB0RXD1	0
bit7	GP4_07	0	ETNB0RXD3	0
bit6	GP4_06	0	ETNB0RXER	0
bit5	GP4_05	0	ETNB0MDC	0
bit4	GP4_04	0	ETNB0LINKSTA	0
bit3	GP4_03	0	ETNB0WOL	0
bit2	GP4_02	0	ETNB0MD	0
bit1	GP4_01	0	RIIC0SDA	0
bit0	GP4_00	0	RIIC0SCL	0

	PUEN6		PUEN7	
	Pin name	Initial value	Pin name	Initial value
bit31	PRESETOUT1#	0	CAN15RX/INTP15	0
bit30	—	0	CAN15TX	0
bit29	—	0	CAN14RX/INTP14	0
bit28	—	0	CAN14TX	0
bit27	—	0	CAN13RX/INTP13	0
bit26	—	0	CAN13TX	0
bit25	—	0	CAN12RX/INTP12	0
bit24	—	0	CAN12TX	0
bit23	—	0	CAN11RX/INTP11	0
bit22	NMI1	0	CAN11TX	0
bit21	INTP32	0	CAN10RX/INTP10	0
bit20	INTP33	0	CAN10TX	0
bit19	INTP34	0	CAN9RX/INTP9	0
bit18	INTP35	0	CAN9TX	0
bit17	INTP36	0	CAN8RX/INTP8	0
bit16	INTP37	0	CAN8TX	0
bit15	RLIN30RX/INTP16	0	CAN7RX/INTP7	0
bit14	RLIN30TX	0	CAN7TX	0
bit13	RLIN31RX/INTP17	0	CAN6RX/INTP6	0
bit12	RLIN31TX	0	CAN6TX	0
bit11	RLIN32RX/INTP18	0	CAN5RX/INTP5	0
bit10	RLIN32TX	0	CAN5TX	0
bit9	RLIN33RX/INTP19	0	CAN4RX/INTP4	0
bit8	RLIN33TX	0	CAN4TX	0
bit7	RLIN34RX/INTP20	0	CAN3RX/INTP3	0
bit6	RLIN34TX	0	CAN3TX	0
bit5	RLIN35RX/INTP21	0	CAN2RX/INTP2	0
bit4	RLIN35TX	0	CAN2TX	0

	PUEN6		PUEN7	
	Pin name	Initial value	Pin name	Initial value
bit3	RLIN36RX/INTP22	0	CAN1RX/INTP1	0
bit2	RLIN36TX	0	CAN1TX	0
bit1	RLIN37RX/INTP23	0	CAN0RX/INTP0	0
bit0	RLIN37TX	0	CAN0TX	0

Table 7.40 Configuration of Registers in PUDSYS0, PUDSYS1

	PUDSYS0		PUDSYS1	
	Pin name	Initial value	Pin name	Initial value
bit31	—	0	—	0
bit30	—	0	—	0
bit29	—	0	—	0
bit28	—	0	—	0
bit27	—	0	—	0
bit26	—	0	—	0
bit25	—	0	—	0
bit24	—	0	—	0
bit23	—	0	—	0
bit22	—	0	—	0
bit21	—	0	—	0
bit20	—	0	—	0
bit19	—	0	—	0
bit18	—	0	—	0
bit17	—	0	—	0
bit16	—	0	—	0
bit15	—	0	—	0
bit14	—	0	—	0
bit13	—	0	—	0
bit12	—	0	—	0
bit11	—	0	—	0
bit10	—	0	MSYN#	1
bit9	—	0	EVTI#	1
bit8	—	0	DCUTCK1	1
bit7	—	0	DCUTDI1	1
bit6	—	0	DCUTMS1	1
bit5	—	0	DCUTMS0	1
bit4	—	0	DCUTDI0	1
bit3	—	0	DCUTCK0	1
bit2	—	0	DCUTRST1#	0
bit1	EXTALR	0	DCUTRST0#	0
bit0	PRESETOUT0#	0	ERROROUT_M#	0

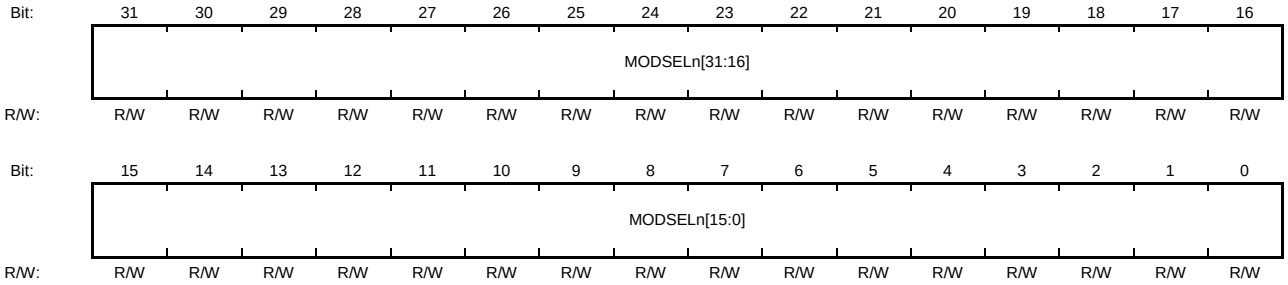
7.2.10 Module Select Register (MODSELn)

Function: MODSELn selects the group for multiple LSI pins with multiplexed pin functions.

The I2C cell uses two Pins of CLK and data, and STBN for making it unused is shared by two Pins of CLK and data, so the MODSEL1 register has 2 bits for one function.

MODSEL4 selects MSPImSC (m=0-5) clock direction as input or output. This register should be set before setting GPIO / Peripheral Function Select Register.

In order to apply domain control, bit assignment is set to Port Group (GPIO).



About MODSEL0, MODSEL2, MODSEL3, MODSEL5-7, there is no configuration.

Table 7.41 Configuration of Registers in MODSEL1

	MODSEL1	Initial value	Description
bit31	Reserved	0	-
bit30	Reserved	0	-
bit29	Reserved	0	-
bit28	Reserved	0	-
bit27	Reserved	0	-
bit26	Reserved	0	-
bit25	Reserved	0	-
bit24	Reserved	0	-
bit23	Reserved	0	-
bit22	Reserved	0	-
bit21	Reserved	0	-
bit20	Reserved	0	-
bit19	Reserved	0	-
bit18	Reserved	0	-
bit17	Reserved	0	-
bit16	Reserved	0	-
bit15	Reserved	0	-
bit14	Reserved	0	-
bit13	Reserved	0	-
bit12	Reserved	0	-
bit11	MODSEL1[11]	0	b'11=Enable I2C5 function
bit10	MODSEL1[10]	0	Other than b'11=Enable functions other than I2C5
bit9	MODSEL1[9]	0	b'11=Enable I2C4 function
bit8	MODSEL1[8]	0	Other than b'11=Enable functions other than I2C4
bit7	MODSEL1[7]	0	b'11=Enable I2C3 function
bit6	MODSEL1[6]	0	Other than b'11=Enable functions other than I2C3
bit5	MODSEL1[5]	0	b'11=Enable I2C2 function
bit4	MODSEL1[4]	0	Other than b'11=Enable functions other than I2C2
bit3	MODSEL1[3]	0	b'11=Enable I2C1 function
bit2	MODSEL1[2]	0	Other than b'11=Enable functions other than I2C1
bit1	MODSEL1[1]	0	b'11=Enable I2C0 function
bit0	MODSEL1[0]	0	Other than b'11=Enable functions other than I2C0

Table 7.42 Configuration of Registers in MODSEL4

	MODSEL4	Initial value	Description
bit31	Reserved	0	-
bit30	Reserved	0	-
bit29	Reserved	0	-
bit28	Reserved	0	-
bit27	Reserved	0	-
bit26	Reserved	0	-
bit25	Reserved	0	-
bit24	Reserved	0	-
bit23	Reserved	0	-
bit22	Reserved	0	-
bit21	Reserved	0	-
bit20	Reserved	0	-
bit19	Reserved	0	-
bit18	Reserved	0	-
bit17	Reserved	0	-
bit16	Reserved	0	-
bit15	Reserved	0	-
bit14	Reserved	0	-
bit13	Reserved	0	-
bit12	Reserved	0	-
bit11	Reserved	0	-
bit10	Reserved	0	-
bit9	Reserved	0	-
bit8	Reserved	0	-
bit7	Reserved	0	-
bit6	Reserved	0	-
bit5	MODSEL4[5]	0	1: Output mode for MSPI5SC function 0: Input mode for MSPI5SC function
bit4	MODSEL4[4]	0	1: Output mode for MSPI4SC function 0: Input mode for MSPI4SC function
bit3	MODSEL4[3]	0	1: Output mode for MSPI3SC function 0: Input mode for MSPI3SC function
bit2	MODSEL4[2]	0	1: Output mode for MSPI2SC function 0: Input mode for MSPI2SC function
bit1	MODSEL4[1]	0	1: Output mode for MSPI1SC function 0: Input mode for MSPI1SC function
bit0	MODSEL4[0]	0	1: Output mode for MSPI0SC function 0: Input mode for MSPI0SC function

7.2.11 TDSEL Control Register 0-1 (TD0SELn , TD1SELn)

Function: TD*SELn / TD*SELSYS controls the driving abilities of pins in use for the SDHI.
This function is delay adjustment of the SDHI clock return path for the LSI inside.

Note: * 0 to 1

TDSEL1*	TDSEL0*	TDOUT Target delay
L	L	10pF (@1.8V operation)
H	L	20pF (@1.8V operation)
L	H	30pF (@1.8V operation)
H	H	40pF (@1.8V operation)

Note: TDSEL1* SD0TDSEL1
TDSEL0* SD0TDSEL0

The value of these bit must be 00.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TD*SELn[31:16] / TD*SELSYS[31:16]															
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TD*SELn[15:0] / TD*SELSYS[15:0]															
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Table 7.43 Configuration of Registers in TD0SEL0 , TD1SEL0

	TD0SEL0			TD1SEL0		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	—	—	0
bit29	—	—	0	—	—	0
bit28	—	—	0	—	—	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	—	—	0	—	—	0
bit24	—	—	0	—	—	0
bit23	—	—	0	—	—	0
bit22	—	—	0	—	—	0
bit21	—	—	0	—	—	0
bit20	—	—	0	—	—	0
bit19	—	—	0	—	—	0
bit18	—	—	0	—	—	0
bit17	—	—	0	—	—	0
bit16	—	—	0	—	—	0
bit15	—	—	0	—	—	0
bit14	—	—	0	—	—	0
bit13	—	—	0	—	—	0
bit12	—	—	0	—	—	0
bit11	—	—	0	—	—	0
bit10	—	—	0	—	—	0
bit9	—	—	0	—	—	0
bit8	—	—	0	—	—	0
bit7	—	—	0	—	—	0
bit6	—	—	0	—	—	0
bit5	—	—	0	—	—	0
bit4	—	—	0	—	—	0
bit3	—	—	0	—	—	0
bit2	—	—	0	—	—	0
bit1	—	—	0	—	—	0
bit0	—	—	0	—	—	0

Table 7.44 Configuration of Registers in TD0SEL1 , TD1SEL1

	TD0SEL1				TD1SEL1			
	Pin name			Initial value	Pin name			Initial value
bit31	—	—		0	—	—		0
bit30	—	—		0	—	—		0
bit29	—	—		0	—	—		0
bit28	—	—		0	—	—		0
bit27	—	—		0	—	—		0
bit26	—	—		0	—	—		0
bit25	MMC_SD_CLK	SD0TDSEL1		0	—	—		0
bit24	—	SD0TDSEL0		0	—	—		0
bit23	—	—		0	—	—		0
bit22	—	—		0	—	—		0
bit21	—	—		0	—	—		0
bit20	—	—		0	—	—		0
bit19	—	—		0	—	—		0
bit18	—	—		0	—	—		0
bit17	—	—		0	—	—		0
bit16	—	—		0	—	—		0
bit15	—	—		0	—	—		0
bit14	—	—		0	—	—		0
bit13	—	—		0	—	—		0
bit12	—	—		0	—	—		0
bit11	—	—		0	—	—		0
bit10	—	—		0	—	—		0
bit9	—	—		0	—	—		0
bit8	—	—		0	—	—		0
bit7	—	—		0	—	—		0
bit6	—	—		0	—	—		0
bit5	—	—		0	—	—		0
bit4	—	—		0	—	—		0
bit3	—	—		0	—	—		0
bit2	—	—		0	—	—		0
bit1	—	—		0	—	—		0
bit0	—	—	—	0	—	—	—	0

Table 7.45 Configuration of Registers in TDSEL2-3

	TD0SEL2			TD1SEL3		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	—	—	0
bit29	—	—	0	—	—	0
bit28	—	—	0	—	—	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	—	—	0	—	—	0
bit24	—	—	0	—	—	0
bit23	—	—	0	—	—	0
bit22	—	—	0	—	—	0
bit21	—	—	0	—	—	0
bit20	—	—	0	—	—	0
bit19	—	—	0	—	—	0
bit18	—	—	0	—	—	0
bit17	—	—	0	—	—	0
bit16	—	—	0	—	—	0
bit15	—	—	0	—	—	0
bit14	—	—	0	—	—	0
bit13	—	—	0	—	—	0
bit12	—	—	0	—	—	0
bit11	—	—	0	—	—	0
bit10	—	—	0	—	—	0
bit9	—	—	0	—	—	0
bit8	—	—	0	—	—	0
bit7	—	—	0	—	—	0
bit6	—	—	0	—	—	0
bit5	—	—	0	—	—	0
bit4	—	—	0	—	—	0
bit3	—	—	0	—	—	0
bit2	—	—	0	—	—	0
bit1	—	—	0	—	—	0
bit0	—	—	0	—	—	0

Table 7.46 Configuration of Registers in TDSEL4-5

	TD0SEL4			TD1SEL5		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	—	—	0
bit29	—	—	0	—	—	0
bit28	—	—	0	—	—	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	—	—	0	—	—	0
bit24	—	—	0	—	—	0
bit23	—	—	0	—	—	0
bit22	—	—	0	—	—	0
bit21	—	—	0	—	—	0
bit20	—	—	0	—	—	0
bit19	—	—	0	—	—	0
bit18	—	—	0	—	—	0
bit17	—	—	0	—	—	0
bit16	—	—	0	—	—	0
bit15	—	—	0	—	—	0
bit14	—	—	0	—	—	0
bit13	—	—	0	—	—	0
bit12	—	—	0	—	—	0
bit11	—	—	0	—	—	0
bit10	—	—	0	—	—	0
bit9	—	—	0	—	—	0
bit8	—	—	0	—	—	0
bit7	—	—	0	—	—	0
bit6	—	—	0	—	—	0
bit5	—	—	0	—	—	0
bit4	—	—	0	—	—	0
bit3	—	—	0	—	—	0
bit2	—	—	0	—	—	0
bit1	—	—	0	—	—	0
bit0	—	—	0	—	—	0

Table 7.47 Configuration of Registers in TDSEL6-7

	TD0SEL6			TD1SEL7		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	—	—	0
bit29	—	—	0	—	—	0
bit28	—	—	0	—	—	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	—	—	0	—	—	0
bit24	—	—	0	—	—	0
bit23	—	—	0	—	—	0
bit22	—	—	0	—	—	0
bit21	—	—	0	—	—	0
bit20	—	—	0	—	—	0
bit19	—	—	0	—	—	0
bit18	—	—	0	—	—	0
bit17	—	—	0	—	—	0
bit16	—	—	0	—	—	0
bit15	—	—	0	—	—	0
bit14	—	—	0	—	—	0
bit13	—	—	0	—	—	0
bit12	—	—	0	—	—	0
bit11	—	—	0	—	—	0
bit10	—	—	0	—	—	0
bit9	—	—	0	—	—	0
bit8	—	—	0	—	—	0
bit7	—	—	0	—	—	0
bit6	—	—	0	—	—	0
bit5	—	—	0	—	—	0
bit4	—	—	0	—	—	0
bit3	—	—	0	—	—	0
bit2	—	—	0	—	—	0
bit1	—	—	0	—	—	0
bit0	—	—	0	—	—	0

Table 7.48 Configuration of Registers in TD0SELSYS , TD1SELSYS

	TD0SELSYS			TD1SELSYS		
	Pin name		Initial value	Pin name		Initial value
bit31	—	—	0	—	—	0
bit30	—	—	0	—	—	0
bit29	—	—	0	—	—	0
bit28	—	—	0	—	—	0
bit27	—	—	0	—	—	0
bit26	—	—	0	—	—	0
bit25	—	—	0	—	—	0
bit24	—	—	0	—	—	0
bit23	—	—	0	—	—	0
bit22	—	—	0	—	—	0
bit21	—	—	0	—	—	0
bit20	—	—	0	—	—	0
bit19	—	—	0	—	—	0
bit18	—	—	0	—	—	0
bit17	—	—	0	—	—	0
bit16	—	—	0	—	—	0
bit15	—	—	0	—	—	0
bit14	—	—	0	—	—	0
bit13	—	—	0	—	—	0
bit12	—	—	0	—	—	0
bit11	—	—	0	—	—	0
bit10	—	—	0	—	—	0
bit9	—	—	0	—	—	0
bit8	—	—	0	—	—	0
bit7	—	—	0	—	—	0
bit6	—	—	0	—	—	0
bit5	—	—	0	—	—	0
bit4	—	—	0	—	—	0
bit3	—	—	0	—	—	0
bit2	—	—	0	—	—	0
bit1	—	—	0	—	—	0
bit0	—	—	0	—	—	0

7.2.12 General IO / Interrupt Switching Register (IOINTSELn) (n = 0 to 3)

IOINTSELn selects either general input/output mode or interrupt input mode for each of the port pins 0 to 31 of the GPIO group. When general input / output mode is selected for a port, it is also necessary to select either input or output mode for the port using the corresponding bit in the general input/output switching register. When interrupt input mode is selected for a port, the setting of the general input / output switching register for the port is ignored.

[Hardware default value:H'0000 0000 = general input / output mode is selected for all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IOINTSELn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IOINTSELn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	IOINTSELn [31:0]	H'0000 0000	R/W	Selects either general input/output mode or interrupt input mode for each port using the bits corresponding to the port numbers. 0: General input/output mode. 1: Interrupt input mode.

Note: Unused bits should be set to the initial values.

	IOINTSELn		IOINTSELn
Bit	GPIO	Bit	GPIO
bit31	GPn_31	bit15	GPn_15
bit30	GPn_30	bit14	GPn_14
bit29	GPn_29	bit13	GPn_13
bit28	GPn_28	bit12	GPn_12
bit27	GPn_27	bit11	GPn_11
bit26	GPn_26	bit10	GPn_10
bit25	GPn_25	bit9	GPn_9
bit24	GPn_24	bit8	GPn_8
bit23	GPn_23	bit7	GPn_7
bit22	GPn_22	bit6	GPn_6
bit21	GPn_21	bit5	GPn_5
bit20	GPn_20	bit4	GPn_4
bit19	GPn_19	bit3	GPn_3
bit18	GPn_18	bit2	GPn_2
bit17	GPn_17	bit1	GPn_1
bit16	GPn_16	bit0	GPn_0

7.2.13 General Input/Output Switching Register (INOUTSELn)

INOUTSELn is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register. Specifically, INOUTSEL selects either general input or general output mode for a port using the bit corresponding to the port number. The INOUTSEL bits can be written to only when the corresponding bits in the general IO/interrupt switching register are 0. Note that after general input/output mode is changed to interrupt input mode, INOUTSEL retains the setting but is read as 0.

[Hardware default value: H'0000 0000 = general input mode is selected for all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INOUTSELn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INOUTSELn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INOUTSELn [31:0]	H'0000 0000	R/W	Selects either general input mode or general output mode for each port using the bits corresponding to the port numbers. 0: General input mode 1: General output mode

Note: Unused bits should be set to the initial values.

7.2.14 General Output Register (OUTDTn)

OUTDTn is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general output mode is selected by the general input/output switching register. Specifically, the value of the bit in OUTDTn corresponding to the port number is inverted or not inverted depending on the setting of the positive/negative logic select register before being output from the corresponding port pin. Note that the polarity of the output signal should previously be set using the corresponding bit in the positive/negative logic select register. This register must be set after the output data select register is appropriately set to choose level of output data.

[Hardware default value: H'0000 0000 = 0 is output from all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OUTDTn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUTDTn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	OUTDTn[31:0]	H'000 00000	R/W	Allows the port to output the value set in the bit corresponding to the port number when the port is appropriately set by IOINTSEL, INOUTSEL and OUTDTSEL. 0: 0 is output. 1: 1 is output.

Note: The values set in OUTDT are not directly output from the GPIO pins; the above set values are processed according to the settings of the positive / negative logic select register before being output.
Unused bits should be set to the initial values.
About write of output data: Output data can be selected exclusively of OUTDT or OUTDTH / OUTDTL, based on OUTDTSEL setting.
About read of output data: Either of OUTDT and OUTDTH / OUTDTL read as the actual output data.

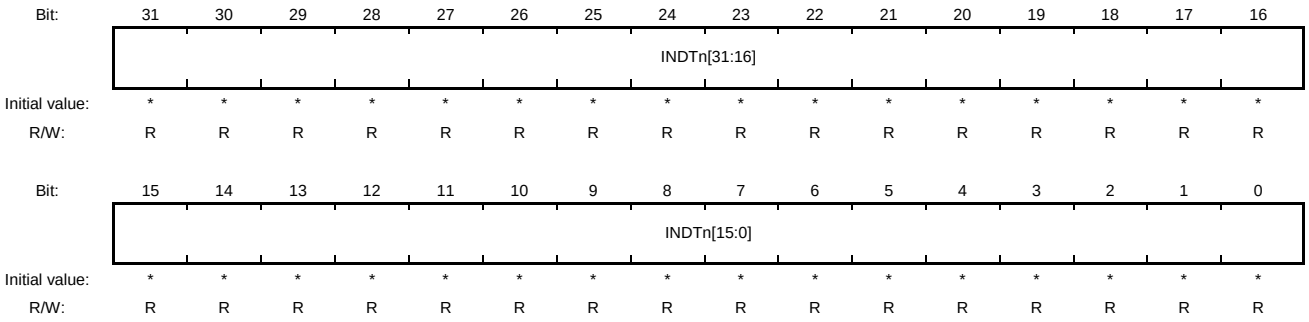
7.2.15 General Input Register (INDTn)

INDTn is a register that can read the status of General-Purpose Input / Output Ports.

Each bit reflects the value received through the corresponding port pin.

Note that when a bit in the positive / negative logic select register is 1, the corresponding bit in INDT indicates the inverted value of the input signal.

[Hardware default value: state of the signals input to the port pins.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INDTn[31:0]	*	R	Each bit reflects the value received through the corresponding port pin. 0: Input is 0. (assuming positive logic) 1: Input is 1. (assuming positive logic)

Note: Unused bits should be set to the initial values.
* State of the signals input to the port pins.

7.2.16 Interrupt Display Register (INTDTn) (n = 0 to 3)

INTDTn is valid only when interrupt input mode is selected by the general IO/interrupt switching register. Specifically, when an interrupt is input via a port pin when INTDTn is valid, the bit in INTDTn corresponding to the port indicates whether the port has received an interrupt input or not. In interrupt input mode, the polarity and detection conditions (one edge/both edge or level) of the external input signal can be set for each port pin. Before using a port pin for interrupt input, the corresponding bits in the positive/negative logic select register and edge/level select register (one edge/both edge register should be appropriately configured if edge detection mode is selected) should be set, respectively.

If a port is set for edge detection using the corresponding bit in the edge/level select register, even when an external pulse interrupt signal is input, the corresponding bit in INTDTn holds the input using the FF and allows the level interrupt signal to be output to the interrupt control block.

To stop all the interrupt signal outputs, all the bits in the interrupt clear register corresponding to the bits in INTDTn currently indicating the reception of the corresponding interrupt signals should be cleared to 0. Note that if a port is set for level detection using the corresponding bit in the edge/level select register and an external level interrupt signal is input, the corresponding bit in INTDTn does not use the FF to hold the input. Therefore, when an external input signal is stopped, the corresponding bit in INTDTn is cleared automatically. When all the bits in INTDTn are turned off (= 0), the GPIO stops outputting all the interrupt signals.

[Hardware default value: H'0000 0000 = no interrupt signals are input from ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INTDTn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTDTn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INTDTn[31:0]	H'0000 0000	R	Each bit indicates the input of an interrupt signal on the corresponding port pin. 0: No interrupt signal has been input. 1: Interrupt signal has been input.

Conditions of Indicating Interrupt Input:

1. For level-sensitive interrupt input (EDGLEVEL = 0)
   - External input signals are constantly monitored and indicated. (When the negative logic is selected, the inverted value of the external input signal is indicated.)
2. For edge-sensitive interrupt input (EDGLEVEL = 1)
   - Clearing condition: When the interrupt clear register is cleared, indication is cleared regardless of the positive / negative logic select register.
   - Setting condition: With the positive logic (POSNEG = 0), when the rising edge of an external interrupt signal is detected, the interrupt input is indicated. With the negative logic (POSNEG = 1), when the falling edge is detected, the interrupt input is indicated. With both edge mode (BOTHEDGE = 1), when either the rising or falling edge, the interrupt input is indicated.

7.2.17 Interrupt Clear Register (INTCLRn) (n = 0 to 3)

When the interrupt display register is currently indicates the reception of the interrupt input on the port for which the edge detection is selected by the edge/level select register (with configuring for one edge/both edge select register) in interrupt input mode, INTCLRn clears the indication. Specifically, writing 1 to the bits in INTCLRn corresponding to port numbers can clear the corresponding bits in the interrupt display register. However, when the interrupt display register is currently indicates the reception of the interrupt input on the port for which the level detection is selected by the edge/level select register, writing 1 to the corresponding bits in INTCLRn cannot clear the corresponding bits in the interrupt display register. Only writing 1 to INTCLRn is effective; INTCLRn is always read as 0.

[Hardware default value: H'0000 0000 = interrupt indication is cleared for no ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INTCLRn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTCLRn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INTCLRn [31:0]	H'0000 0000	R/W	Writing 1 to bits corresponding to port numbers clears the corresponding bits in the interrupt display register. 0: No effect 1: Interrupt display register bit is cleared.

Note: Unused bits should be set to the initial values.

7.2.18 Interrupt Mask Register (INTMSKn) (n = 0 to 3)

INTMSKn masks the interrupt requests indicated by the interrupt display register of GPIO.ch. Interrupts can be separately masked using the corresponding bits in INTMSKn. When all the bits currently indicating the reception of the interrupt signals are masked, no interrupt signals are output to the interrupt control block. Masks can be canceled by writing 1 to the corresponding bits in the interrupt mask clear register. Only writing 0 to this register is effective.

[Hardware default value: H'0000 0000 = all the ports are masked.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INTMSKn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTMSKn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INTMSKn [31:0]	H'0000 0000	R/W	Setting a mask to the bit disables the corresponding interrupt signal to be output to the interrupt control block. 0: Interrupt is masked. 1: Interrupt is not masked.

Note: Unused bits should be set to the initial values.

7.2.19 Interrupt Mask Clear Register (MSKCLRn) (n = 0 to 3)

MSKCLRn cancels masks that are set by the interrupt mask register of GPIO.ch*A. Each mask can be canceled (cleared) by writing 1 to the corresponding bit in MSKCLRn. Only writing 1 to MSKCLRn is effective; MSKCLRn is always read as 0.

[Hardware default value: H'0000 0000 = alternative interrupt masks are cleared for no ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSKCLRn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKCLRn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MSKCLRn [31:0]	H'0000 0000	R/W	Setting a mask to the bit disables the corresponding alternative interrupt signal to be output to the interrupt control block. 0: No effect 1: Interrupt is not masked.

Note: Unused bits should be set to the initial values. (When GPIO is not selected by the pin multiplex settings, do not cancel the alternative interrupt mask.)

7.2.20 Positive / Negative Logic Select Register (POSNEGn) (n = 0 to 3)

POSNEGn selects the polarity (positive or negative logic) of each port pin in general input mode, general output mode, or interrupt input mode. POSNEGn should be set before mode selection.

[Hardware default value: H'0000 0000 = positive logic is selected for all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	POSNEGn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	POSNEGn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	POSNEGn [31:0]	H'0000 0000	R/W	Selects the polarity (positive or negative logic) of each port pin. 0: Positive logic 1: Negative logic

Note: Unused bits should be set to the initial values.

7.2.21 Edge / level Select Register (EDGLEVELn) (n = 0 to 3)

EDGLEVELn is valid only for the ports for which interrupt input mode is selected by the general IO/interrupt switching register. Specifically, EDGLEVELn selects the detection conditions (edge or level) of the interrupt input signal on each port pin for which interrupt input mode is selected. EDGLEVELn should be set before selection of interrupt input mode.

[Hardware default value: H'0000 0000 = level detection is selected for all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EDGLEVELn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDGLEVELn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

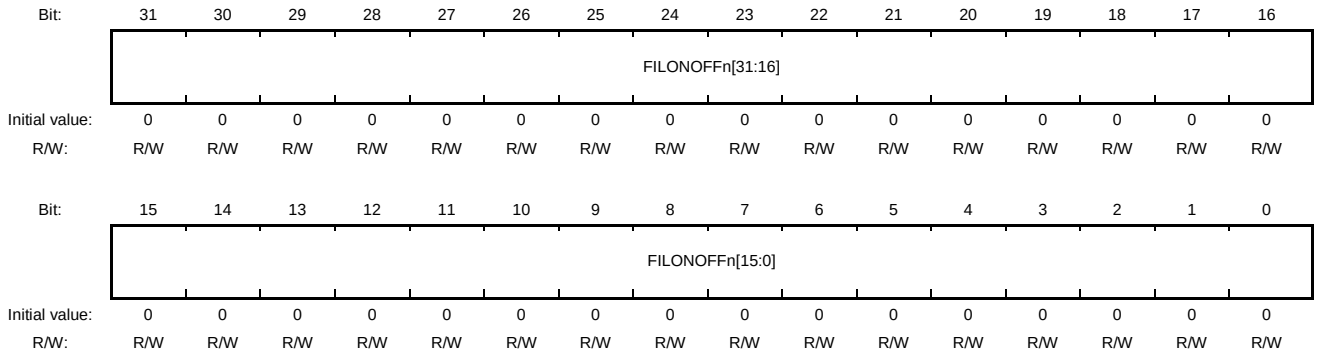
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EDGLEVELn [31:0]	H'0000 0000	R/W	Selects the level or edge as detection conditions of the interrupt input signal on each port pin for which interrupt input mode is selected. 0: Level 1: Edge

Note: Unused bits should be set to the initial values.

7.2.22 Chattering Prevention On / Off Register (FILONOFFn)

FILONOFFn prevents chattering input to the port pins of each GPIO group. For details, refer to section 7.3.6, Handling of Input Signals on Port Pins.

[Hardware default value: H'0000 0000 = chattering prevention function is turned off for all the ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	FILONOFFn [31:0]	H'0000 0000	R/W	Enables or disables the chattering prevention function. 0: Chattering prevention function is disabled. 1: Chattering prevention function is enabled

7.2.23 Chattering Prevention Clock Select Register (FILCLKSELn)

FILCLKSELn controls the division ratio of clock CPϕ for prevent chattering input to the port pin GPIO group.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

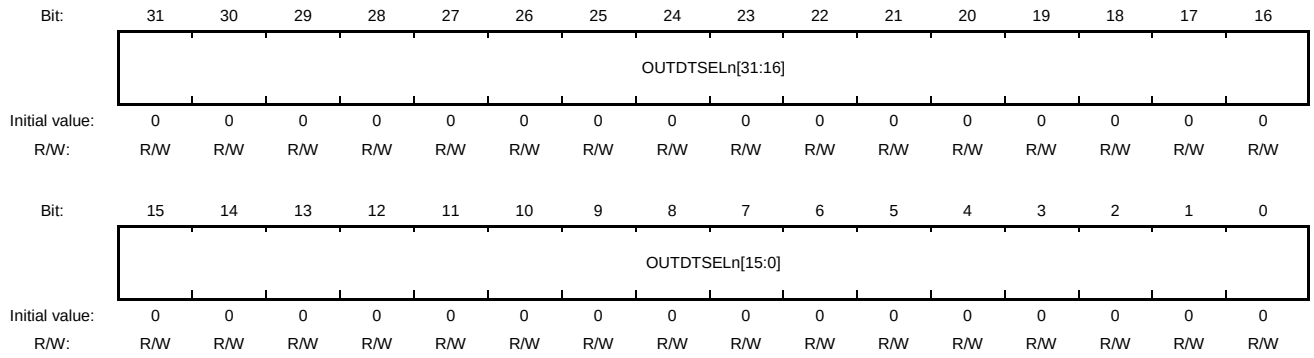
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FILCLKSELn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	FILCLKSELn [15:0]	H'0000	R/W	Set the division ratio of filter CLOCK. d: CPϕ / (d + 1) d is setting value

7.2.24 Output Data Select Register (OUTDTSELn)

OUTDTSELn is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general output mode is selected by the general input/output switching register. OUTDTSELn selects if OUTDTn or OUTDTHn / OUTDTLn will be the output data of GPIO. When choosing OUTDTn, configuration is performed as described in section 7.2.14, General Output Register (OUTDTn). When choosing OUTDTHn / OUTDTLn, output data will be output by writing the appropriate data to the corresponding bits in OUTDTHn or OUTDTLn. Note that the polarity of the output signal should be previously set using the corresponding bit in the positive/negative logic select register. Furthermore, this register should be set before writing data to OUTDTHn / OUTDTLn registers.

[Hardware default value: H'0000 0000 = Out data register is used to output data.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	OUTDTSELn [31:0]	H'0000 0000	R/W	Choosing whether output data is output by general output register OUTDTn or output data high register OUTDTHn / output data low register OUTDTLn. 0: General output register is used to output the data. 1: Output data high register and output data low register is used to output the data.

Note: Unused bits should be set to the initial values.

7.2.25 Output Data High Register (OUTDTHn)

OUTDTHn is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general output mode is selected by the general input/output switching register, and the output data select register OUTDTSELn is configured to choose OUTDTHn / OUTDTLn register to output the data of GPIO. Only writing 1 to OUTDTHn is effective. Otherwise, setting makes no changes. Reading OUTDTHn returns the values of the latest data set to OUTDTHn or OUTDTLn right before that. Note that the polarity of the output signal should be previously set using the corresponding bit in the positive/negative logic select register. Furthermore, this register should be written and read after output data select register OUTDTSELn is set. Reading OUTDTHn without appropriately configuring OUTDTSELn can return value of OUTDTn register.

[Hardware default value: H'0000 0000 = 0 is output from all the port swith setting OUTDTSELn.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OUTDTHn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUTDTHn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	OUTDTHn [31:0]	H'0000 0000	R/W	Outputting high value data. 0: Invalid data. 1: Valid data.

Note: Unused bits should be set to the initial values.

7.2.26 Output Data Low Register (OUTDTLn)

OUTDTLn is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general output mode is selected by the general input/output switching register, and the output data select register OUTDTSELn is configured to choose OUTDTHn / OUTDTLn register to output the data of GPIO. Only writing 0 to OUTDTLn is effective. Otherwise, setting makes no changes. Reading OUTDTLn returns the values of the latest data set to OUTDTLn or OUTDTHn right before that. Note that the polarity of the output signal should be previously set using the corresponding bit in the positive/negative logic select register. Furthermore, this register should be written or read after output data select registers OUTDTSELn is set. Reading OUTDTHn without appropriately configuring OUTDTSELn can return value of OUTDTn register.

[Hardware default value: H'0000 0000 = 0 is output from all the ports with setting OUTDTSELn.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OUTDTLn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUTDTLn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	OUTDTLn [31:0]	H'0000 0000	R/W	Outputting low value data. 0: Valid data. 1: Invalid data.

Note: Unused bits should be set to the initial values.

7.2.27 One Edge / Both Edge Select Register (BOTHEDGEn) (n = 0 to 3)

BOTHEDGEn is valid only when the edge detection mode is selected by the edge/level select registers. Specially, BOTHEDGEn selects the detection condition (one edge or both edges) of the interrupt input signal on each port pin for which interrupt input mode (selected by the general IO/interrupt switching registers) and edge detection mode are selected. BOTHEDGEn should be set before selection of interrupt input mode.

[Hardware default value: H'0000 0000 = both edge detection mode is disabled for all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BOTHEDGEn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BOTHEDGEn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BOTHEDGEn [31:0]	H'0000 0000	R/W	Selecting one edge or both edge detection condition of the interrupt input signal on each port pin for which interrupt input mode and edge detection mode are selected. 0: One edge. 1: Both edges.

Note: Unused bits should be set to the initial values.

7.2.28 General Input Enable register (INENn)

Create registers that can control IE in GPIO.

Assign 1 bit of register to 1 pin for IE of all pins to which GPIO is assigned. Also,as before, in order to maintain SW compatibility, set the initial value of IE to High (input ON) state.

The register specifications are shown below.

Create one register (32 bits) for each Port Group.

Setting value: 0 = Input Enable Off / 1 = Input Enable ON

Initial value: 0 = Input Enable OFF

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INENn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INENn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INENn [31:0]	H'0000 0000	R/W	0: Input disable. 1: Input enable.

7.2.29 Port Safe state Select Register0-1 (PS0SRn , PS1SRn)

Registers (PS*SRn) that select 4 types of Port Safe State (initial state or HiZ or Pull-Down or Pull-Up) with 2 bits.
Note: * 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PS*SRn[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PS*SRn[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: It applies to Pin which multiplex with GPIO function

Table 7.49 Configuration of Registers in PSiSRn

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PS*SRn[m×2+1:m×2] m = 0 to 15	b'00	R/W	b'00=initial state b'01=HiZ b'10=Pull-Down b'11=Pull-Up

Table 7.50 Configuration of Registers in PS0SRn , PS1SRn

PS0SRn				PS1SRn		
	GPIO	Description	Initial value	GPIO	Description	Initial value
bit31 bit30	GPn_15	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_31	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit29 bit28	GPn_14	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_30	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit27 bit26	GPn_13	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_29	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit25 bit24	GPn_12	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_28	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit23 bit22	GPn_11	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_27	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit21 bit20	GPn_10	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_26	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit19 bit18	GPn_9	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_25	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit17 bit16	GPn_8	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_24	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit15 bit14	GPn_7	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_23	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit13 bit12	GPn_6	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_22	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit11 bit10	GPn_5	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_21	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit9 bit8	GPn_4	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_20	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit7 bit6	GPn_3	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_19	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit5 bit4	GPn_2	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_18	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit3 bit2	GPn_1	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_17	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00
bit1 bit0	GPn_0	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00	GPn_16	b'00=initial state / b'01=HiZ b'10=Pull-Down / b'11=Pull-Up	b’00

7.2.30 Port Safe state Enable Register (PSERn)

The register (PSERn) to enable / disable PSS Rregister.

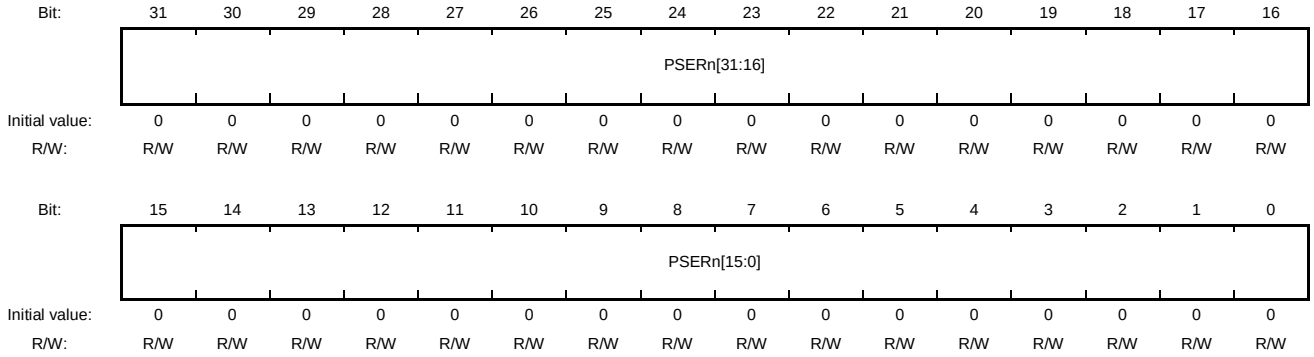


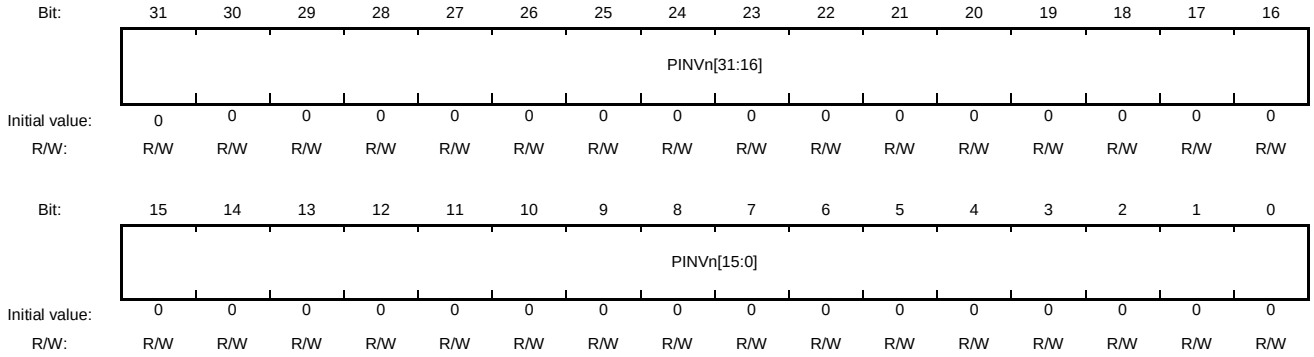
Table 7.51 Configuration of Registers in PSER

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PSERn [31:0]	H'0000 0000	R/W	0: PSSR disable. 1: PSSR enable.

	PSERn			PSERn	
Bit	**GPIO**	**Description**	**Bit**	**GPIO**	**Description**
bit31	GPn_31	0: PS1SRn[31:30] disable 1: PS1SRn[31:30] enable	**bit15**	GPn_15	0: PS0SRn[31:30] disable 1: PS0SRn[31:30] enable
bit30	GPn_30	0: PS1SRn[29:28] disable 1: PS1SRn[29:28] enable	**bit14**	GPn_14	0: PS0SRn[29:28] disable 1: PS0SRn[29:28] enable
bit29	GPn_29	0: PS1SRn[27:26] disable 1: PS1SRn[27:26] enable	**bit13**	GPn_13	0: PS0SRn[27:26] disable 1: PS0SRn[27:26] enable
bit28	GPn_28	0: PS1SRn[25:24] disable 1: PS1SRn[25:24] enable	**bit12**	GPn_12	0: PS0SRn[25:24] disable 1: PS0SRn[25:24] enable
bit27	GPn_27	0: PS1SRn[23:22] disable 1: PS1SRn[23:22] enable	**bit11**	GPn_11	0: PS0SRn[23:22] disable 1: PS0SRn[23:22] enable
bit26	GPn_26	0: PS1SRn[21:20] disable 1: PS1SRn[21:20] enable	**bit10**	GPn_10	0: PS0SRn[21:20] disable 1: PS0SRn[21:20] enable
bit25	GPn_25	0: PS1SRn[19:18] disable 1: PS1SRn[19:18] enable	**bit9**	GPn_9	0: PS0SRn[19:18] disable 1: PS0SRn[19:18] enable
bit24	GPn_24	0: PS1SRn[17:16] disable 1: PS1SRn[17:16] enable	**bit8**	GPn_8	0: PS0SRn[17:16] disable 1: PS0SRn[17:16] enable
bit23	GPn_23	0: PS1SRn[15:14] disable 1: PS1SRn[15:14] enable	**bit7**	GPn_7	0: PS0SRn[15:14] disable 1: PS0SRn[15:14] enable
bit22	GPn_22	0: PS1SRn[13:12] disable 1: PS1SRn[13:12] enable	**bit6**	GPn_6	0: PS0SRn[13:12] disable 1: PS0SRn[13:12] enable
bit21	GPn_21	0: PS1SRn[11:10] disable 1: PS1SRn[11:10] enable	**bit5**	GPn_5	0: PS0SRn[11:10] disable 1: PS0SRn[11:10] enable
bit20	GPn_20	0: PS1SRn[9:8] disable 1: PS1SRn[9:8] enable	**bit4**	GPn_4	0: PS0SRn[9:8] disable 1: PS0SRn[9:8] enable
bit19	GPn_19	0: PS1SRn[7:6] disable 1: PS1SRn[7:6] enable	**bit3**	GPn_3	0: PS0SRn[7:6] disable 1: PS0SRn[7:6] enable
bit18	GPn_18	0: PS1SRn[5:4] disable 1: PS1SRn[5:4] enable	**bit2**	GPn_2	0: PS0SRn[5:4] disable 1: PS0SRn[5:4] enable
bit17	GPn_17	0: PS1SRn[3:2] disable 1: PS1SRn[3:2] enable	**bit1**	GPn_1	0: PS0SRn[3:2] disable 1: PS0SRn[3:2] enable
bit16	GPn_16	0: PS1SRn[1:0] disable 1: PS1SRn[1:0] enable	**bit0**	GPn_0	0: PS0SRn[1:0] disable 1: PS0SRn[1:0] enable

7.2.31 Port Output Value Inversion Register (PINVn) (n = 4 to 7)

This register(PINVn) inverts the output value of the port.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PINVn[31:0]	H'0000 0000	R/W	0: Inversion disable 1: Inversion enable

About PINV0-3, there is no configuration.

Table 7.52 Configuration of Registers in PINV4, PINV5

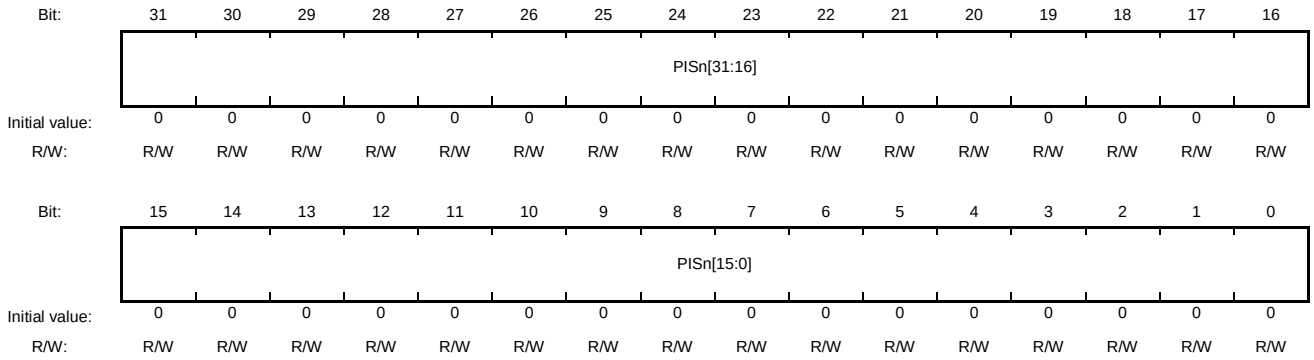
	PINV4		PINV5	
	Pin name	Initial value	Pin name	Initial value
bit31	—	0	—	0
bit30	MSPI1CSS1	0	—	0
bit29	MSPI1CSS2	0	—	0
bit28	MSPI1SC	0	—	0
bit27	MSPI1CSS0	0	—	0
bit26	MSPI1SO/MSPI1DCS	0	—	0
bit25	MSPI1SI	0	—	0
bit24	MSPI0CSS0	0	—	0
bit23	MSPI0CSS1	0	—	0
bit22	MSPI0SO/MSPI0DCS	0	—	0
bit21	MSPI0SI	0	—	0
bit20	MSPI0SC	0	—	0
bit19	GP4_19	0	ETNB0TXD0	0
bit18	GP4_18	0	ETNB0TXEN	0
bit17	GP4_17	0	ETNB0TXD2	0
bit16	GP4_16	0	ETNB0TXD1	0
bit15	GP4_15	0	ETNB0TXCLK	0
bit14	GP4_14	0	ETNB0TXD3	0
bit13	GP4_13	0	ETNB0TXER	0
bit12	GP4_12	0	ETNB0RXCLK	0
bit11	GP4_11	0	ETNB0RXD0	0
bit10	GP4_10	0	ETNB0RXDV	0
bit9	GP4_09	0	ETNB0RXD2	0
bit8	GP4_08	0	ETNB0RXD1	0
bit7	GP4_07	0	ETNB0RXD3	0
bit6	GP4_06	0	ETNB0RXER	0
bit5	GP4_05	0	ETNB0MDC	0
bit4	GP4_04	0	ETNB0LINKSTA	0
bit3	GP4_03	0	ETNB0WOL	0
bit2	GP4_02	0	ETNB0MD	0
bit1	GP4_01	0	RIIC0SDA	0
bit0	GP4_00	0	RIIC0SCL	0

Table 7.53 Configuration of Registers in PINV6, PINV7

	PINV6		PINV7	
	Pin name	Initial value	Pin name	Initial value
bit31	PRESETOUT1#	0	CAN15RX/INTP15	0
bit30	—	0	CAN15TX	0
bit29	—	0	CAN14RX/INTP14	0
bit28	—	0	CAN14TX	0
bit27	—	0	CAN13RX/INTP13	0
bit26	—	0	CAN13TX	0
bit25	—	0	CAN12RX/INTP12	0
bit24	—	0	CAN12TX	0
bit23	—	0	CAN11RX/INTP11	0
bit22	NMI1	0	CAN11TX	0
bit21	INTP32	0	CAN10RX/INTP10	0
bit20	INTP33	0	CAN10TX	0
bit19	INTP34	0	CAN9RX/INTP9	0
bit18	INTP35	0	CAN9TX	0
bit17	INTP36	0	CAN8RX/INTP8	0
bit16	INTP37	0	CAN8TX	0
bit15	RLIN30RX/INTP16	0	CAN7RX/INTP7	0
bit14	RLIN30TX	0	CAN7TX	0
bit13	RLIN31RX/INTP17	0	CAN6RX/INTP6	0
bit12	RLIN31TX	0	CAN6TX	0
bit11	RLIN32RX/INTP18	0	CAN5RX/INTP5	0
bit10	RLIN32TX	0	CAN5TX	0
bit9	RLIN33RX/INTP19	0	CAN4RX/INTP4	0
bit8	RLIN33TX	0	CAN4TX	0
bit7	RLIN34RX/INTP20	0	CAN3RX/INTP3	0
bit6	RLIN34TX	0	CAN3TX	0
bit5	RLIN35RX/INTP21	0	CAN2RX/INTP2	0
bit4	RLIN35TX	0	CAN2TX	0
bit3	RLIN36RX/INTP22	0	CAN1RX/INTP1	0
bit2	RLIN36TX	0	CAN1TX	0
bit1	RLIN37RX/INTP23	0	CAN0RX/INTP0	0
bit0	RLIN37TX	0	CAN0TX	0

7.2.32 Port Input Buffer Selection Register (PISn) (n = 4 to 7)

This register specifies the input buffer characteristics. Specific input characteristic settings may be required, depending on the pin function to be used. For details, refer to Electrical Characteristics.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PISn[31:0]	H'0000 0000	R/W	Look at table.

About PIS0-4, PIS6-7, there is no configuration.

Table 7.54 Configuration of Registers in PIS5

	PIS5	
	Pin name	Initial value
bit31	—	0
bit30	—	0
bit29	—	0
bit28	—	0
bit27	—	0
bit26	—	0
bit25	—	0
bit24	—	0
bit23	—	0
bit22	—	0
bit21	—	0
bit20	—	0
bit19	ETNB0TXD0	0
bit18	ETNB0TXEN	0
bit17	ETNB0TXD2	0
bit16	ETNB0TXD1	0
bit15	ETNB0TXCLK	0
bit14	ETNB0TXD3	0
bit13	ETNB0TXER	0
bit12	ETNB0RXCLK	0
bit11	ETNB0RXD0	0
bit10	ETNB0RXDV	0
bit9	ETNB0RXD2	0
bit8	ETNB0RXD1	0
bit7	ETNB0RXD3	0
bit6	ETNB0RXER	0
bit5	ETNB0MDC	0
bit4	ETNB0LINKSTA	0
bit3	ETNB0WOL	0
bit2	ETNB0MD	0
bit1	—	0
bit0	—	0

7.3 Operation

7.3.1 Overview

This is recomendation of Pin Function setting flow, “Figure6.3 Recomendation of Pin Function setting flow”.

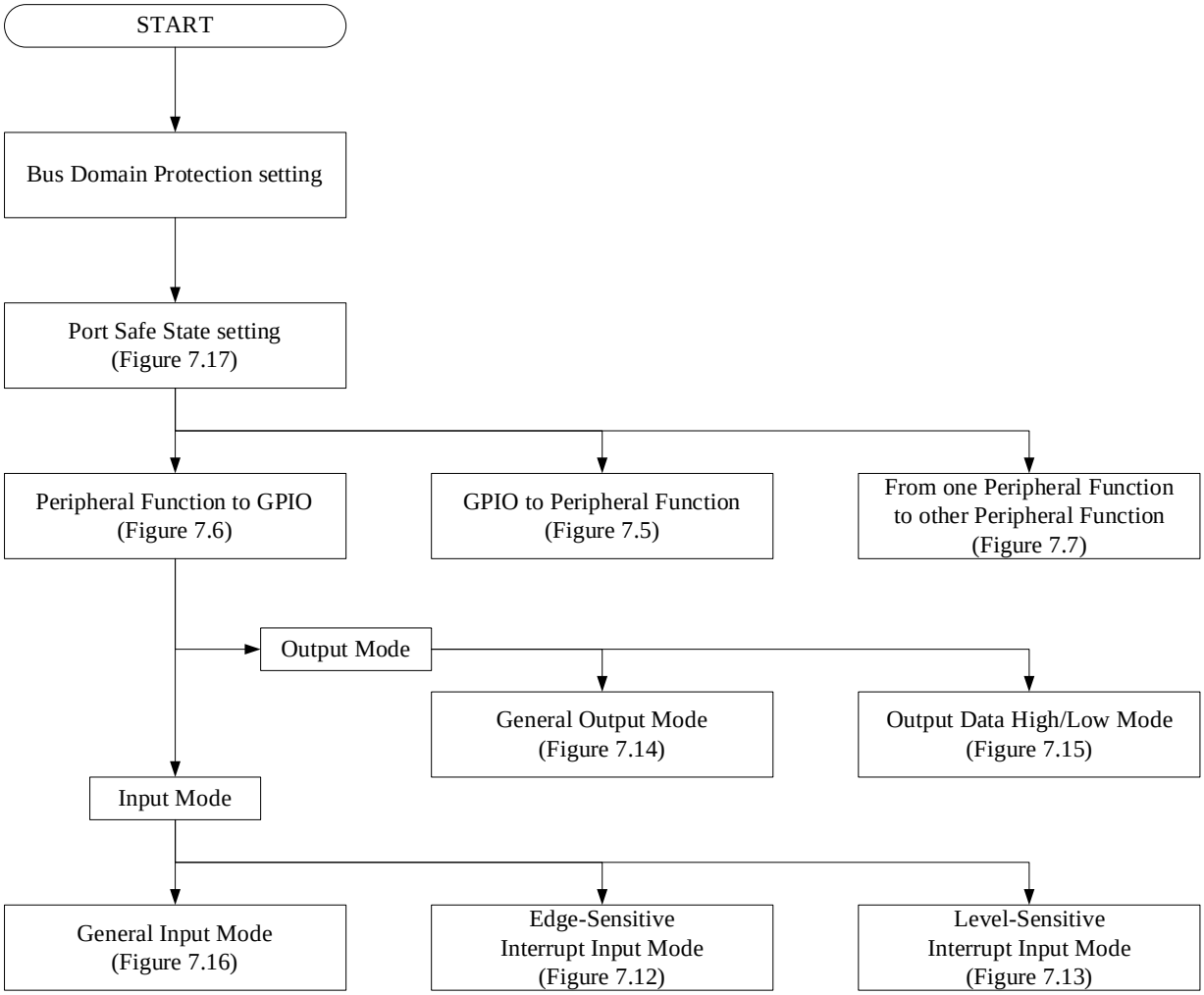


Figure 7.4 Recomendation of Pin Function setting flow

7.3.2 Function Setting for Multiplexed Pins

Setting the LSI multiplexed pin setting mask register (PMMRn) is necessary before setting each of the GPIO/peripheral function select register GPSRn, peripheral function select registers IP0SRn to IP3SRn, DRV control registers DRV0CTRLn to DRV3CTRLn, TDSEL control registers TD0SELn and TD1SELn, POWER Condition control registers POCn and Module select register MODSELn. Specifically, the inverse of the value to be set in the select register must be written to the LSI multiplexed pin setting mask register. Otherwise, the GPIO/peripheral function select register (GPSRn) and peripheral function select registers 0 to 3 (IP0SRn to IP3SRn) cannot be set.

Caution :

Some input functions are assigned to more than one pin.

Only activate one single pin to one given peripheral input function.

Do not activate the same input function on multiple pins at the same time.

Do not set peripheral selection to a place where the peripheral function is not assigned.

Ex) Regaeding MSPI_1_A and MSPI_1_B as the pin-multiplex table.

MSPI1SI input functions are assigned to this device as MSPI_1 IP.

However, MSPI1SI input function should not be activated on more than one pin.

After activating the function on one pin, do not activate it on another.

(1) Procedure for changing pin function from GPIO to peripheral function

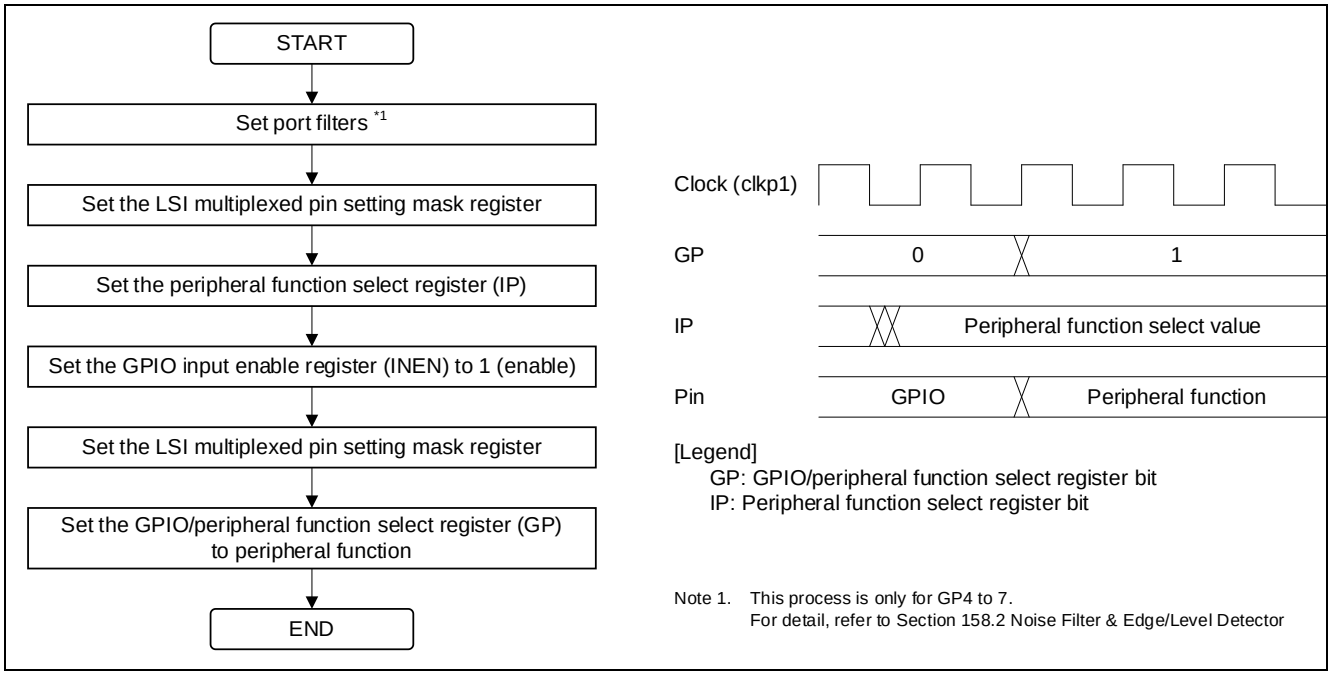


Figure 7.5 Procedure for Changing Pin Function from GPIO to Peripheral Function

(2) Procedure for changing pin function from peripheral function to GPIO

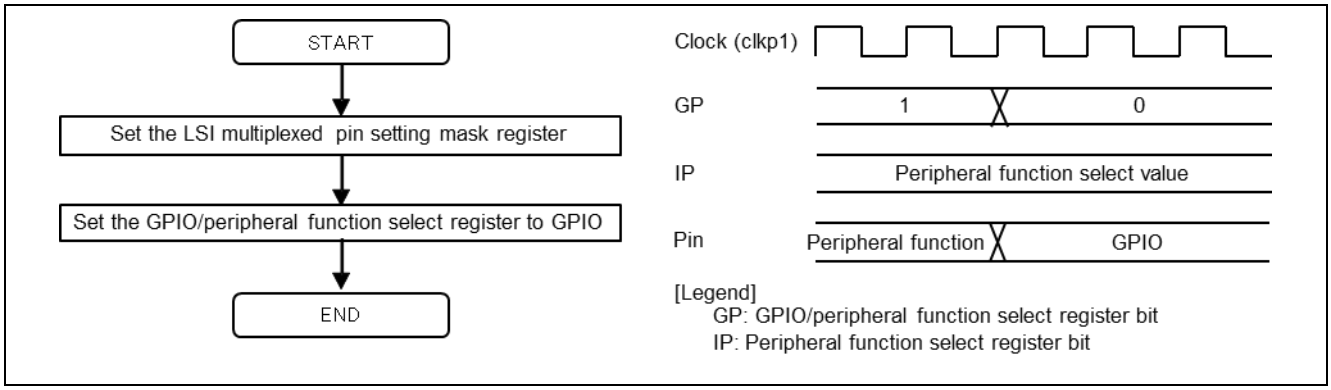


Figure 7.6 Procedure for Changing Pin Function from Peripheral functionto GPIO

(3) Procedure 1 for changing pin function from one peripheral function to another peripheral function

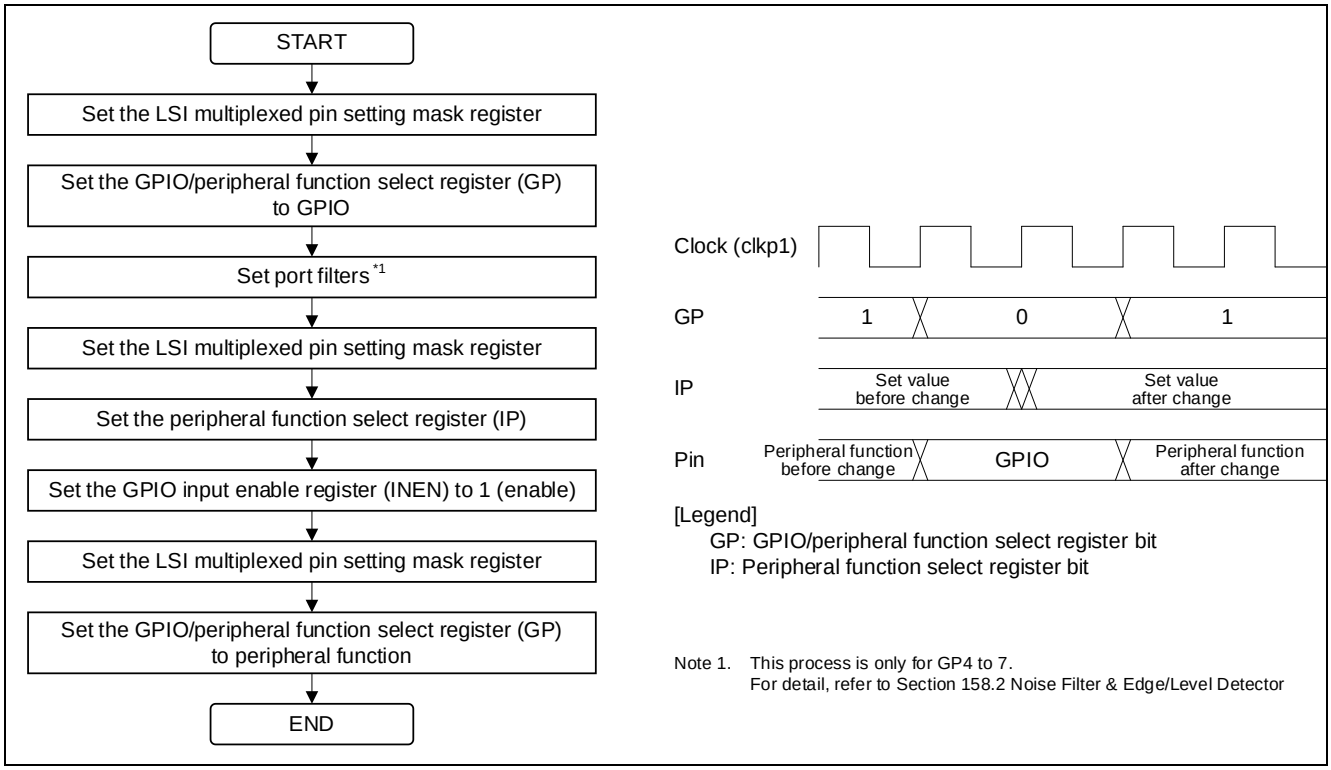


Figure 7.7 Procedure for Changing Pin Function from One Peripheral Function to Another Peripheral Function (with GPIO Setting)

7.3.3 Setting Pull-Up / Down Resistors

The LSI pin pull-on / off control register (PUENn) and pull-up / down control register (PUDn) areused.

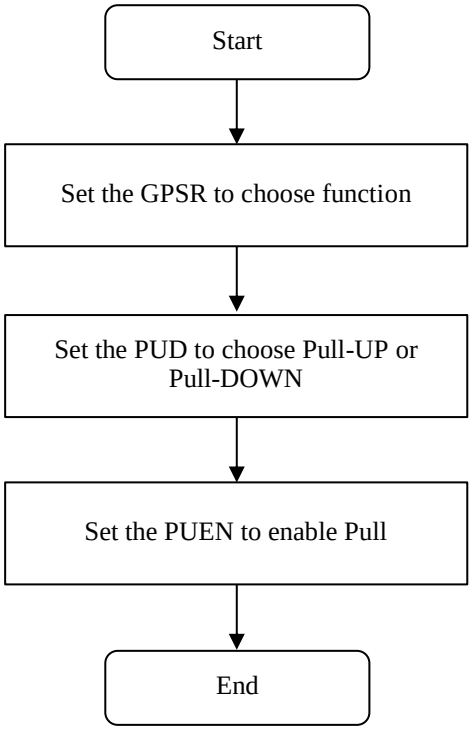


Figure 7.8 Procedure for setting Pull-UP/DOWN

7.3.4 Port Pin Specifications

Each GPIO group is provided with up to 32 port pins for general input / output and external interrupt input ports. Table 7.55 specifies these pins.

Table 7.55 Port Pin Specifications

Block	Abbreviation	Name	Descriptions
GPIO-0 Applicable registers: IOINTSEL0 INOUTSEL0 OUTDT0 INDT0 INTDT0 INTCLR0 INTMSK0 MSKCLR0 POSNEG0 EDGLEVEL0 FILONOFF0 OUTDTSEL0 OUTDTH0 OUTDTL0 BOTHEDGE0 INEN0	GP0_00	IO/interrupt input port GP0_00	● Either general input / output mode or interrupt input mode can be set for each port. ● In general input mode, the polarity of input signals can be set for each port. ● In general output mode, the polarity of output signals can be set for each port. ● In interrupt input mode, the polarity of interrupt signal can be set for each port. ● In interrupt input mode, the detection conditions of interrupt signals can be set for each port.
	GP0_01	IO/interrupt input port GP0_01	
	GP0_02	IO/interrupt input port GP0_02	
	GP0_03	IO/interrupt input port GP0_03	
	GP0_04	IO/interrupt input port GP0_04	
	GP0_05	IO/interrupt input port GP0_05	
	GP0_06	IO/interrupt input port GP0_06	
	GP0_07	IO/interrupt input port GP0_07	
	GP0_08	IO/interrupt input port GP0_08	
	GP0_09	IO/interrupt input port GP0_09	
	GP0_10	IO/interrupt input port GP0_10	
	GP0_11	IO/interrupt input port GP0_11	
	GP0_12	IO/interrupt input port GP0_12	
	GP0_13	IO/interrupt input port GP0_13	
	GP0_14	IO/interrupt input port GP0_14	
	GP0_15	IO/interrupt input port GP0_15	
	GP0_16	IO/interrupt input port GP0_16	
	GP0_17	IO/interrupt input port GP0_17	
	GP0_18	IO/interrupt input port GP0_18	
	GP0_19	IO/interrupt input port GP0_19	
	GP0_20	IO/interrupt input port GP0_20	

Block	Abbreviation	Name	Descriptions
GPIO-1 Applicable registers: IOINTSEL1 INOUTSEL1 OUTDT1 INDT1 INTDT1 INTCLR1 INTMSK1 MSKCLR1 POSNEG1 EDGLEVEL1 FILONOFF1 OUTDTSEL1 OUTDTH1 OUTDTL1 BOTHEDGE1 INEN1	GP1_00	IO/interrupt input port GP1_00	● Either general input / output mode or interrupt input mode can be set for each port. ● In general input mode, the polarity of input signals can be set for each port. ● In general output mode, the polarity of output signals can be set for each port. ● In interrupt input mode, the polarity of interrupt signals can be set for each port. ● In interrupt input mode, the detection conditions of interrupt signals can be set for each port.
	GP1_01	IO/interrupt input port GP1_01	
	GP1_02	IO/interrupt input port GP1_02	
	GP1_03	IO/interrupt input port GP1_03	
	GP1_04	IO/interrupt input port GP1_04	
	GP1_05	IO/interrupt input port GP1_05	
	GP1_06	IO/interrupt input port GP1_06	
	GP1_07	IO/interrupt input port GP1_07	
	GP1_08	IO/interrupt input port GP1_08	
	GP1_09	IO/interrupt input port GP1_09	
	GP1_10	IO/interrupt input port GP1_10	
	GP1_11	IO/interrupt input port GP1_11	
	GP1_12	IO/interrupt input port GP1_12	
	GP1_13	IO/interrupt input port GP1_13	
	GP1_14	IO/interrupt input port GP1_14	
	GP1_15	IO/interrupt input port GP1_15	
	GP1_16	IO/interrupt input port GP1_16	
	GP1_17	IO/interrupt input port GP1_17	
	GP1_18	IO/interrupt input port GP1_18	
	GP1_19	IO/interrupt input port GP1_19	
	GP1_20	IO/interrupt input port GP1_20	
	GP1_21	IO/interrupt input port GP1_21	
	GP1_22	IO/interrupt input port GP1_22	
	GP1_23	IO/interrupt input port GP1_23	
	GP1_24	IO/interrupt input port GP1_24	

Block	Abbreviation	Name	Descriptions
GPIO-2 Applicable registers: IOINTSEL2 INOUTSEL2 OUTDT2 INDT2 INTDT2 INTCLR2 INTMSK2 MSKCLR2 POSNEG2 EDGLEVEL2 FILONOFF2 OUTDTSEL2 OUTDTH2 OUTDTL2 BOTHEDGE2 INEN2	GP2_00	IO/interrupt input port GP2_00	● Either general input / output mode or interrupt input mode can be set for each port. ● In general input mode, the polarity of input signals can be set for each port. ● In general output mode, the polarity of output signals can be set for each port. ● In interrupt input mode, the polarity of interrupt signal can be set for each port. ● In interrupt input mode, the detection conditions of interrupt signals can be set for each port.
	GP2_01	IO/interrupt input port GP2_01	
	GP2_02	IO/interrupt input port GP2_02	
	GP2_03	IO/interrupt input port GP2_03	
	GP2_04	IO/interrupt input port GP2_04	
	GP2_05	IO/interrupt input port GP2_05	
	GP2_06	IO/interrupt input port GP2_06	
	GP2_07	IO/interrupt input port GP2_07	
	GP2_08	IO/interrupt input port GP2_08	
	GP2_09	IO/interrupt input port GP2_09	
	GP2_10	IO/interrupt input port GP2_10	
	GP2_11	IO/interrupt input port GP2_11	
	GP2_12	IO/interrupt input port GP2_12	
	GP2_13	IO/interrupt input port GP2_13	
	GP2_14	IO/interrupt input port GP2_14	
	GP2_15	IO/interrupt input port GP2_15	
	GP2_16	IO/interrupt input port GP2_16	

Block	Abbreviation	Name	Descriptions
GPIO-3 Applicable registers: IOINTSEL3 INOUTSEL3 OUTDT3 INDT3 INTDT3 INTCLR3 INTMSK3 MSKCLR3 POSNEG3 EDGLEVEL3 FILONOFF3 OUTDTSEL3 OUTDTH3 OUTDTL3 BOTHEDGE3 INEN3	GP3_00	IO/interrupt input port GP3_00	● Either general input / output mode or interrupt input mode can be set for each port. ● In general input mode, the polarity of input signals can be set for each port. ● In general output mode, the polarity of output signals can be set for each port. ● In interrupt input mode, the polarity of interrupt signal can be set for each port. ● In interrupt input mode, the detection conditions of interrupt signals can be set for each port.
	GP3_01	IO/interrupt input port GP3_01	
	GP3_02	IO/interrupt input port GP3_02	
	GP3_03	IO/interrupt input port GP3_03	
	GP3_04	IO/interrupt input port GP3_04	
	GP3_05	IO/interrupt input port GP3_05	
	GP3_06	IO/interrupt input port GP3_06	
	GP3_07	IO/interrupt input port GP3_07	
	GP3_08	IO/interrupt input port GP3_08	
	GP3_09	IO/interrupt input port GP3_09	
	GP3_10	IO/interrupt input port GP3_10	
	GP3_11	IO/interrupt input port GP3_11	
	GP3_12	IO/interrupt input port GP3_12	
	GP3_13	IO/interrupt input port GP3_13	
	GP3_14	IO/interrupt input port GP3_14	
	GP3_15	IO/interrupt input port GP3_15	
	GP3_16	IO/interrupt input port GP3_16	
	GP3_17	IO/interrupt input port GP3_17	
	GP3_18	IO/interrupt input port GP3_18	

Block	Abbreviation	Name	Descriptions
GPIO-4 Applicable registers: INOUTSEL4 OUTDT4 INDT4 POSNEG4 FILONOFF4 OUTDTSEL4 OUTDTH4 OUTDTL4 INEN4 PNOT4 PINV4	GP4_00	IO port GP4_00	● In general input mode, the polarity of input signals can be set for each port. ● In general output mode, the polarity of output signals can be set for each port.
	GP4_01	IO port GP4_01	
	GP4_02	IO port GP4_02	
	GP4_03	IO port GP4_03	
	GP4_04	IO port GP4_04	
	GP4_05	IO port GP4_05	
	GP4_06	IO port GP4_06	
	GP4_07	IO port GP4_07	
	GP4_08	IO port GP4_08	
	GP4_09	IO port GP4_09	
	GP4_10	IO port GP4_10	
	GP4_11	IO port GP4_11	
	GP4_12	IO port GP4_12	
	GP4_13	IO port GP4_13	
	GP4_14	IO port GP4_14	
	GP4_15	IO port GP4_15	
	GP4_16	IO port GP4_16	
	GP4_17	IO port GP4_17	
	GP4_18	IO port GP4_18	
	GP4_19	IO port GP4_19	
	GP4_20	IO port GP4_20	
	GP4_21	IO port GP4_21	
	GP4_22	IO port GP4_22	
	GP4_23	IO port GP4_23	
	GP4_24	IO port GP4_24	
	GP4_25	IO port GP4_25	
	GP4_26	IO port GP4_26	
	GP4_27	IO port GP4_27	
	GP4_28	IO port GP4_28	
	GP4_29	IO port GP4_29	
	GP4_30	IO port GP4_30	

Block	Abbreviation	Name	Descriptions
GPIO-5 Applicable registers: INOUTSEL5 OUTDT5 INDT5 POSNEG5 FILONOFF5 OUTDTSEL5 OUTDTH5 OUTDTL5 INEN5 PNOT5 PINV5	GP5_00	IO port GP5_00	● In general input mode, the polarity of input signals can be set for each port. ● In general output mode, the polarity of output signals can be set for each port.
	GP5_01	IO port GP5_01	
	GP5_02	IO port GP5_02	
	GP5_03	IO port GP5_03	
	GP5_04	IO port GP5_04	
	GP5_05	IO port GP5_05	
	GP5_06	IO port GP5_06	
	GP5_07	IO port GP5_07	
	GP5_08	IO port GP5_08	
	GP5_09	IO port GP5_09	
	GP5_10	IO port GP5_10	
	GP5_11	IO port GP5_11	
	GP5_12	IO port GP5_12	
	GP5_13	IO port GP5_13	
	GP5_14	IO port GP5_14	
	GP5_15	IO port GP5_15	
	GP5_16	IO port GP5_16	
	GP5_17	IO port GP5_17	
	GP5_18	IO port GP5_18	
	GP5_19	IO port GP5_19	

Block	Abbreviation	Name	Descriptions
GPIO-6 Applicable registers: INOUTSEL6 OUTDT6 INDT6 POSNEG6 FILONOFF6 OUTDTSEL6 OUTDTH6 OUTDTL6 INEN6 PNOT6 PINV6	GP6_00	IO port GP6_00	● In general input mode, the polarity of input signals can be set for each port. ● In general output mode, the polarity of output signals can be set for each port.
	GP6_01	IO port GP6_01	
	GP6_02	IO port GP6_02	
	GP6_03	IO port GP6_03	
	GP6_04	IO port GP6_04	
	GP6_05	IO port GP6_05	
	GP6_06	IO port GP6_06	
	GP6_07	IO port GP6_07	
	GP6_08	IO port GP6_08	
	GP6_09	IO port GP6_09	
	GP6_10	IO port GP6_10	
	GP6_11	IO port GP6_11	
	GP6_12	IO port GP6_12	
	GP6_13	IO port GP6_13	
	GP6_14	IO port GP6_14	
	GP6_15	IO port GP6_15	
	GP6_16	IO port GP6_16	
	GP6_17	IO port GP6_17	
	GP6_18	IO port GP6_18	
	GP6_19	IO port GP6_19	
	GP6_20	IO port GP6_20	
	GP6_21	IO port GP6_21	
	GP6_22	IO port GP6_22	
	GP6_31	IO port GP6_31	

Block	Abbreviation	Name	Descriptions
GPIO-7 Applicable registers: INOUTSEL7 OUTDT7 INDT7 POSNEG7 FILONOFF7 OUTDTSEL7 OUTDTH7 OUTDTL7 INEN7 PNOT7 PINV7	GP7_00	IO port GP7_00	● In general input mode, the polarity of input signals can be set for each port. ● In general output mode, the polarity of output signals can be set for each port.
	GP7_01	IO port GP7_01	
	GP7_02	IO port GP7_02	
	GP7_03	IO port GP7_03	
	GP7_04	IO port GP7_04	
	GP7_05	IO port GP7_05	
	GP7_06	IO port GP7_06	
	GP7_07	IO port GP7_07	
	GP7_08	IO port GP7_08	
	GP7_09	IO port GP7_09	
	GP7_10	IO port GP7_10	
	GP7_11	IO port GP7_11	
	GP7_12	IO port GP7_12	
	GP7_13	IO port GP7_13	
	GP7_14	IO port GP7_14	
	GP7_15	IO port GP7_15	
	GP7_16	IO port GP7_16	
	GP7_17	IO port GP7_17	
	GP7_18	IO port GP7_18	
	GP7_19	IO port GP7_19	
	GP7_20	IO port GP7_20	
	GP7_21	IO port GP7_21	
	GP7_22	IO port GP7_22	
	GP7_23	IO port GP7_23	
	GP7_24	IO port GP7_24	
	GP7_25	IO port GP7_25	
	GP7_26	IO port GP7_26	
	GP7_27	IO port GP7_27	
	GP7_28	IO port GP7_28	
	GP7_29	IO port GP7_29	
	GP7_30	IO port GP7_30	
	GP7_31	IO port GP7_31	

7.3.5 Operations in Each Mode

(1) Mode Switching

Two registers are used to switch modes of the general IO/interrupt input pins of the GPIO groups. Each register is provided with up to 32 bits each controlling one of the GPIOn* port pins. The general IO/interrupt switching register is first used to select either general input/output mode or interrupt input mode for each port pin. When general input/output mode is selected, the setting of the relevant bit in the second register, i.e., the general input/output switching register, is used. Specifically, when a bit in the general input/output switching register is set for general output mode, the corresponding port pin is turned to the output direction and the route is formed so that the set value in the corresponding bit in the general output register should be output via the pin. Likewise, when set for the general input mode, the corresponding port pin is turned to the input direction and the route is formed so that the value received via the pin should be indicated by the corresponding bit in the general input register. When interrupt input mode is selected, the corresponding port pin is turned to the input direction and the route is formed so that the reception of the signal input via the pin should be indicated by the interrupt display register. Here, the setting of the second register, i.e., the general input/output switching register, is invalid.

Note: * n = 0 to 7 (The groups GP4 to GP7 have no interrupt input mode.)

(2) General Input / Output Mode

When setting a port for general input, set high value to INEN to enable general input. When a port is set for general input/output mode using the corresponding bit in the general IO/interrupt switching register, the corresponding port serves as a general input/output pin. In general input/output mode, either mode can be selected using the corresponding bit in the general input/output switching register. When a port is set for general output mode, the port outputs the value set in the corresponding bit in the general output register or output data high/output data low register with appropriate configuring in output data select register. Here, the polarity of the actual output signal is determined by the setting of the corresponding bit in the positive/negative logic select register. When a port is set for general input mode, the polarity of the input signal is also determined by the setting of the corresponding bit in the positive/negative logic select register. The general input register indicates the value accordingly. Note that the general input register does not hold the input signal using the FF.

(3) Interrupt Input Mode

When a port is set for interrupt input mode using the corresponding bit in the general IO/interrupt switching register, the corresponding port serves as an interrupt input pin. In interrupt input mode, when the port receives an external interrupt, the corresponding bit in the interrupt display register indicates the input of an interrupt signal on the corresponding port pin, and an interrupt signal is output to the interrupt control block. In this mode, the polarity and detection conditions (edge or level) of the external input signal can be set for each port. The corresponding bits in the positive/negative logic select register and edge/level select register, one edge/both edge select register should be used to set the polarity and detection conditions, respectively.

If a port is set for edge detection using the corresponding bit in the edge/level select register, even when an external pulse interrupt signal is input, the corresponding bit in the interrupt display register holds the input using the FF and allows the level interrupt signal to be output to the interrupt control block. To stop all the interrupt signal outputs, all the bits in the interrupt clear register corresponding to the bits in the interrupt display register currently indicating the reception of the corresponding interrupt signals should be cleared to 0. Note that if a port is set for level detection using the corresponding bit in the edge/level select register and an external level interrupt signal is input, the corresponding bit in the interrupt display register does not use the FF to hold the input.

Interrupts indicated by the interrupt display register can be separately masked using the corresponding bits in the interrupt mask register. When all the bits currently indicating the reception of the interrupt signals are masked, no interrupt signals are output to the interrupt control block. Masks can be canceled by writing 1 to the corresponding bits in the interrupt mask clear register depending on the interrupt mask register is used.

7.3.6 Handling of Input Signals on Port Pins

(1) Chattering

In general input mode and interrupt input modes, a filtering function can be used for the port pins 0 to 3 of each GPIO group to prevent external chattering input. Specifically, when a bit in the chattering prevention on / off register is set to use the function, the external input to the corresponding port pin is sampled four consecutive times based on the filter clock signal, which is internally generated by the GPIO. The external input is canceled except when the active input is detected four consecutive times. Therefore, when a filtering function is used, input to the port pins 0 to 3 of each GPIO group need to be at least four sampling clock cycles long (The sampling clock is generated from peripheral clock/k, where k is determined by FILONOFFn. CLKSEL.).

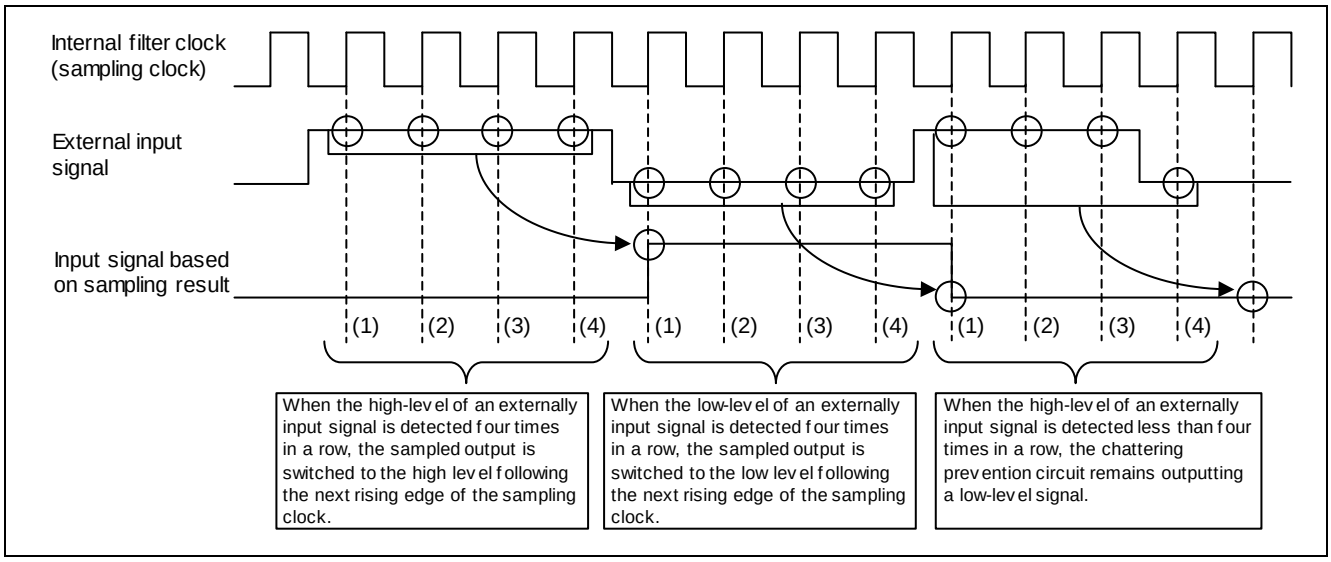


Figure 7.9 Sampling Timing Chart

(2) Input Signal Synchronization

Ingeneral input mode and interrupt input mode, external input signals on all port pins are synchronized with the GPIO clock (CPϕ).

7.3.7 Interrupt Display Timing Charts

Figure 7.9 shows the interrupt display timing and Figure 7.10 shows the note on the timing. In both figures, the positive logic and edge-sensitive input are assumed.

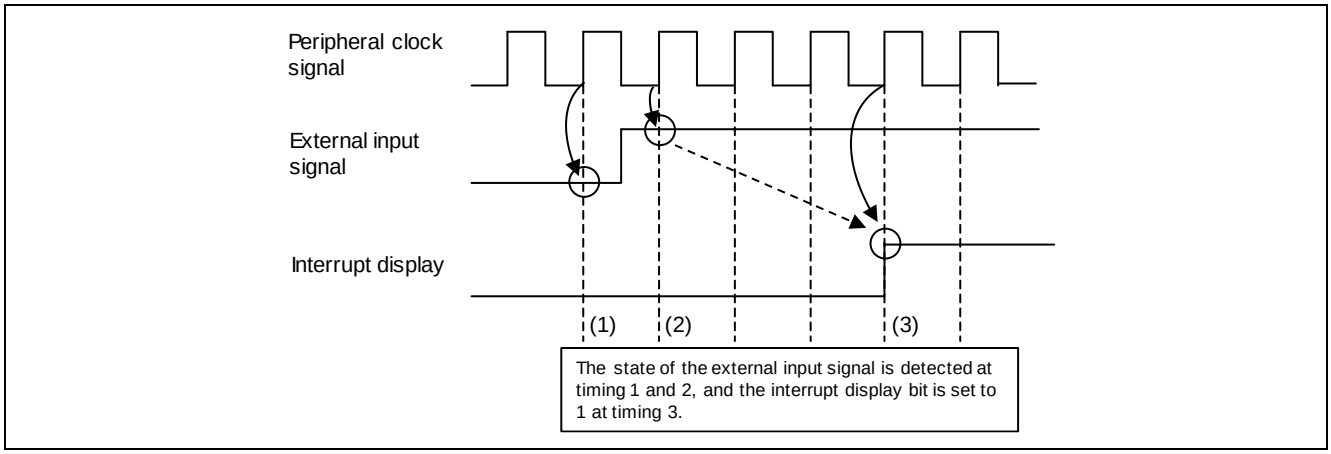


Figure 7.10 Interrupt Display Timing

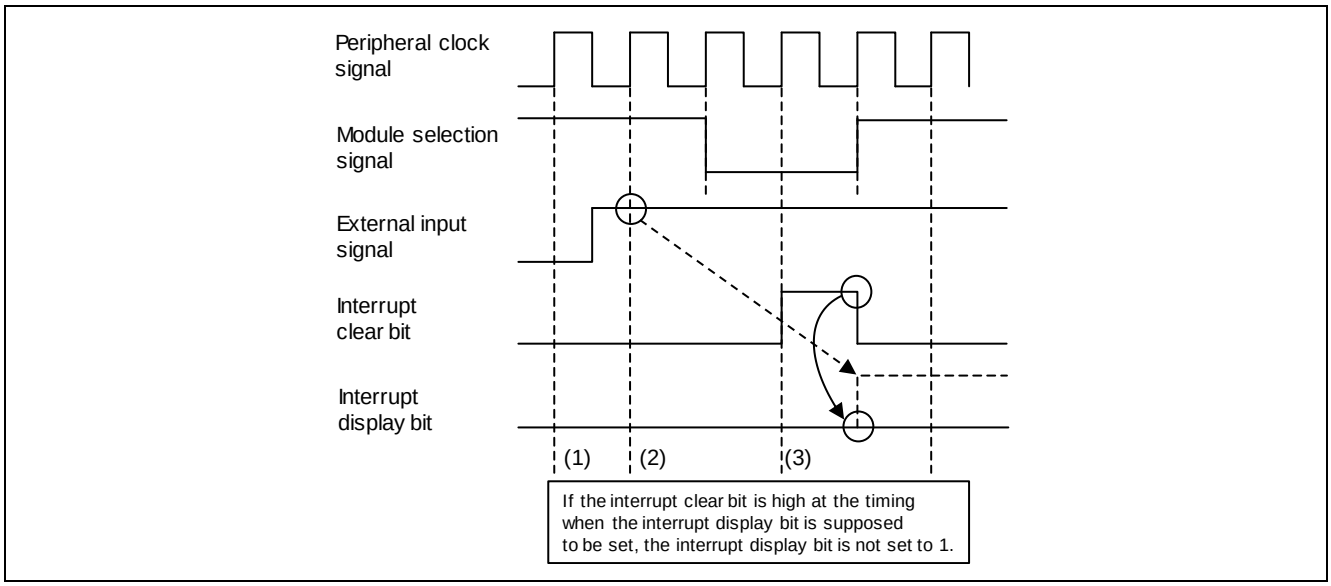


Figure 7.11 Note on Interrupt Display Timing

7.3.8 Using GPIO

The following sections describe how to use the GPIO. If the GPIO is not used according to the procedures shown here, operations are not guaranteed.

(1) Setting Edge-Sensitive Interrupt Input Mode

For setting edge-sensitive interrupt input mode, refer to the procedure shown in Figure 7.11.

Note that an unexpected interrupt might be generated in the module if setting (1), (2), (3) or (4) in the flowchart is changed. When changing the setting, (5) and (6) should be done.

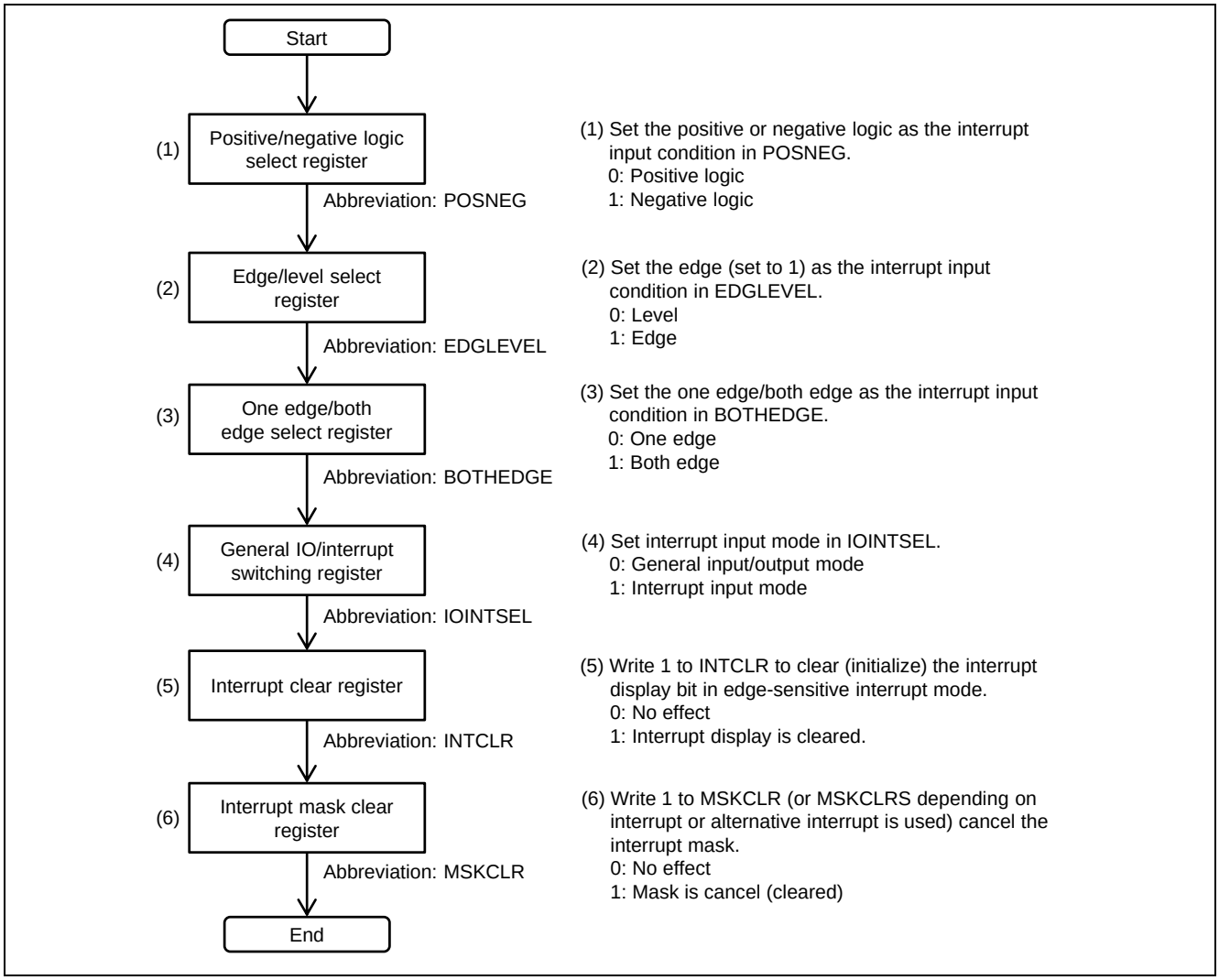


Figure 7.12 Flowchart of Setting the GPIO to Edge-Sensitive Interrupt Input Mode

(2) Setting Level-Sensitive Interrupt Input Mode

For setting level-sensitive interrupt input mode, refer to the procedure shown in Figure 7.12.

Note that when an external level-sensitive interrupt input signal is stopped, the corresponding interrupt is canceled automatically. Inlevel-sensitive interrupt input mode, the interrupt clear register is invalid.

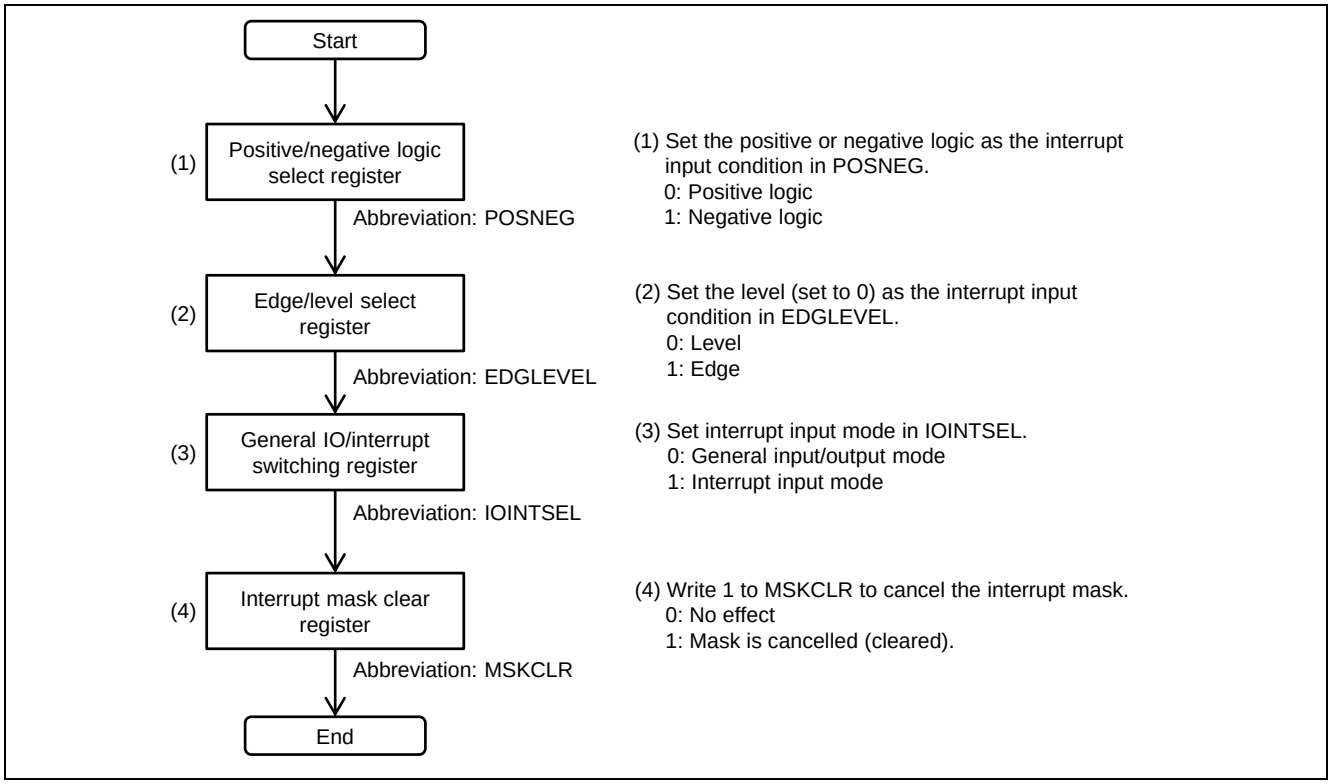


Figure 7.13 Flowchart of Setting the GPIO to Level-Sensitive Interrupt Input Mode

(3) Setting General Output Mode

For setting general output mode, refer to the procedure shown in Figure 7.13.

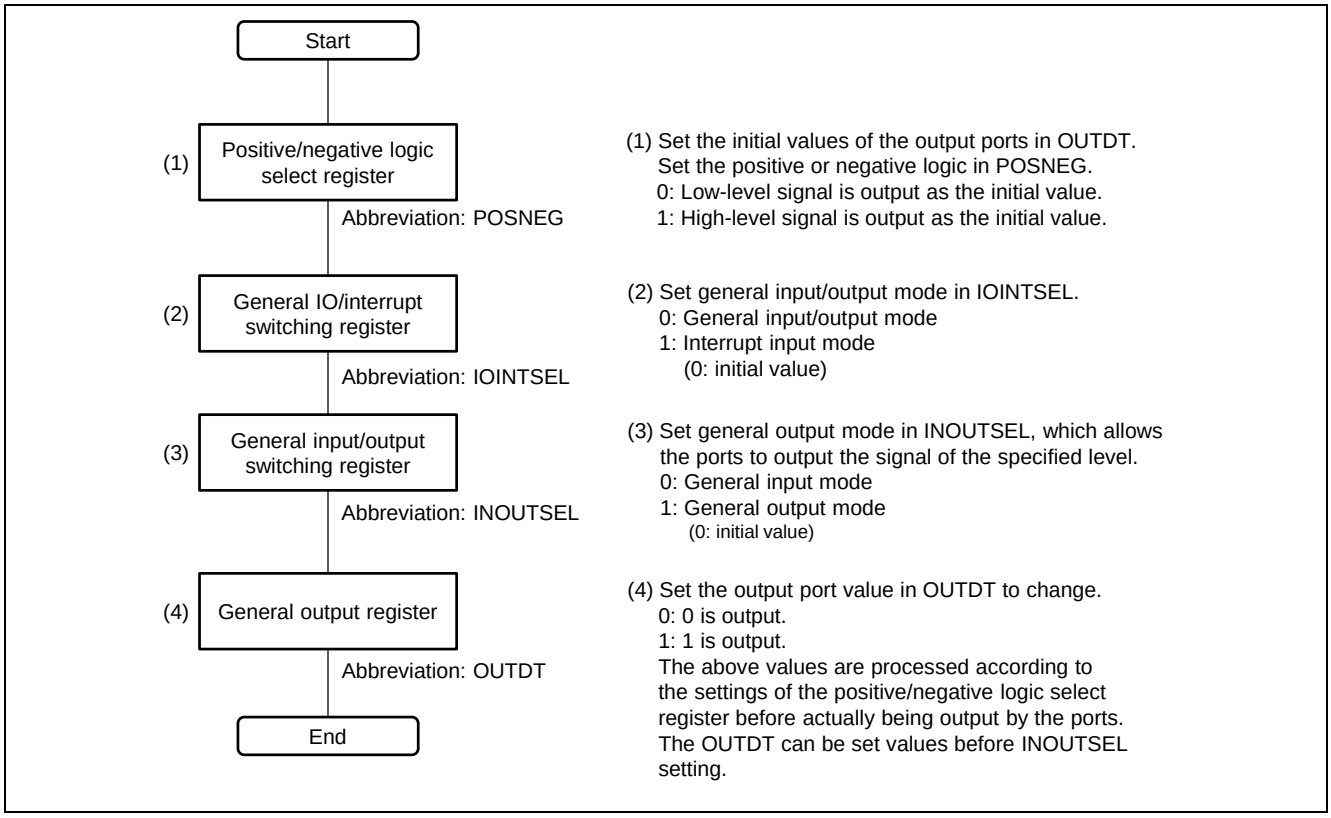


Figure 7.14 Flowchart of Setting the GPIO to General Output Mode

(4) Setting Output data high / Output data low Mode

For setting output data high / output data low mode, refer to the procedure shown in Figure 7.14.

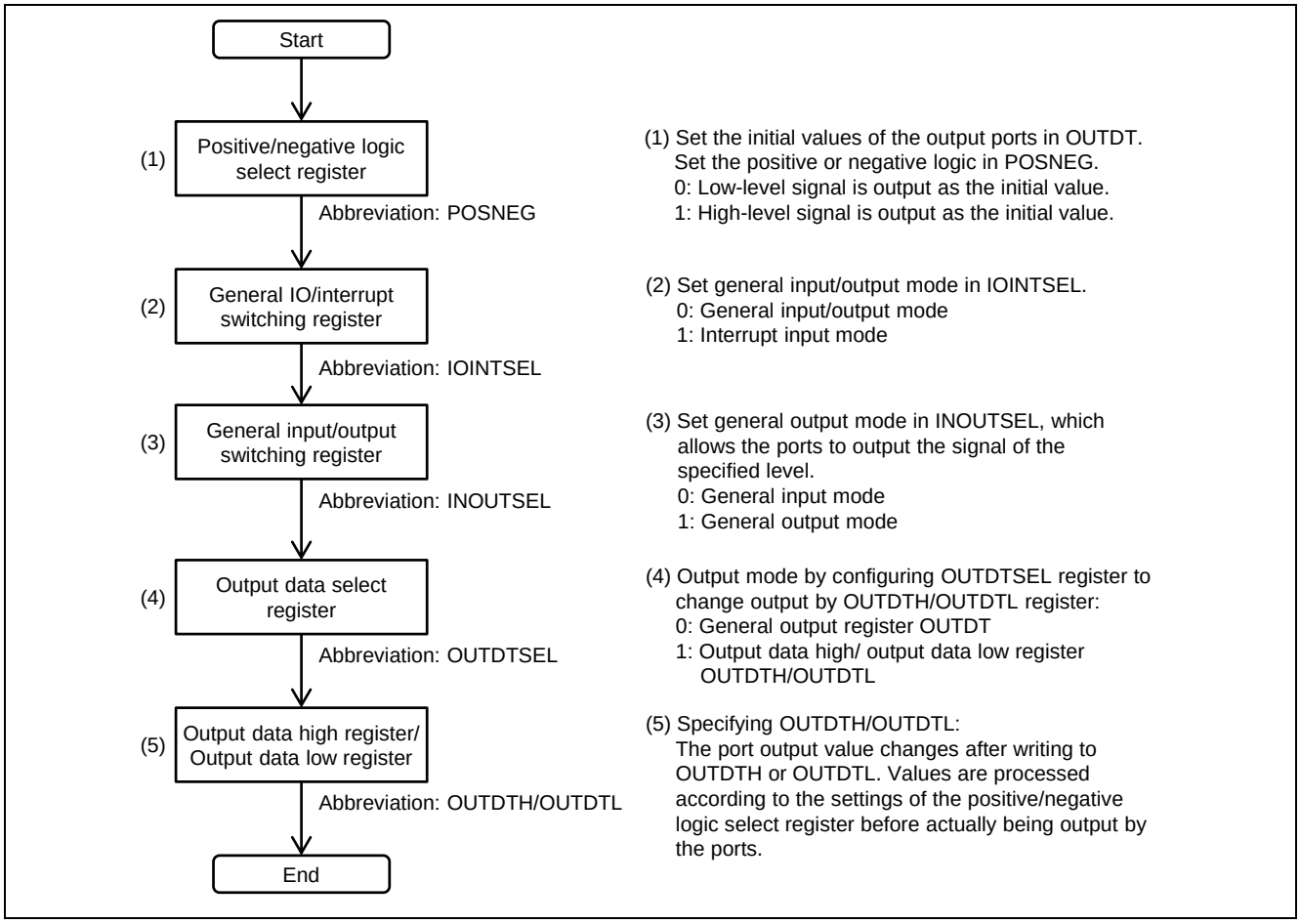


Figure 7.15 Flowchart of Setting the GPIO to Output data high / Output data low Mode

(5) Setting General Input Mode

For setting general input mode, refer to the procedure shown in Figure 7.15.

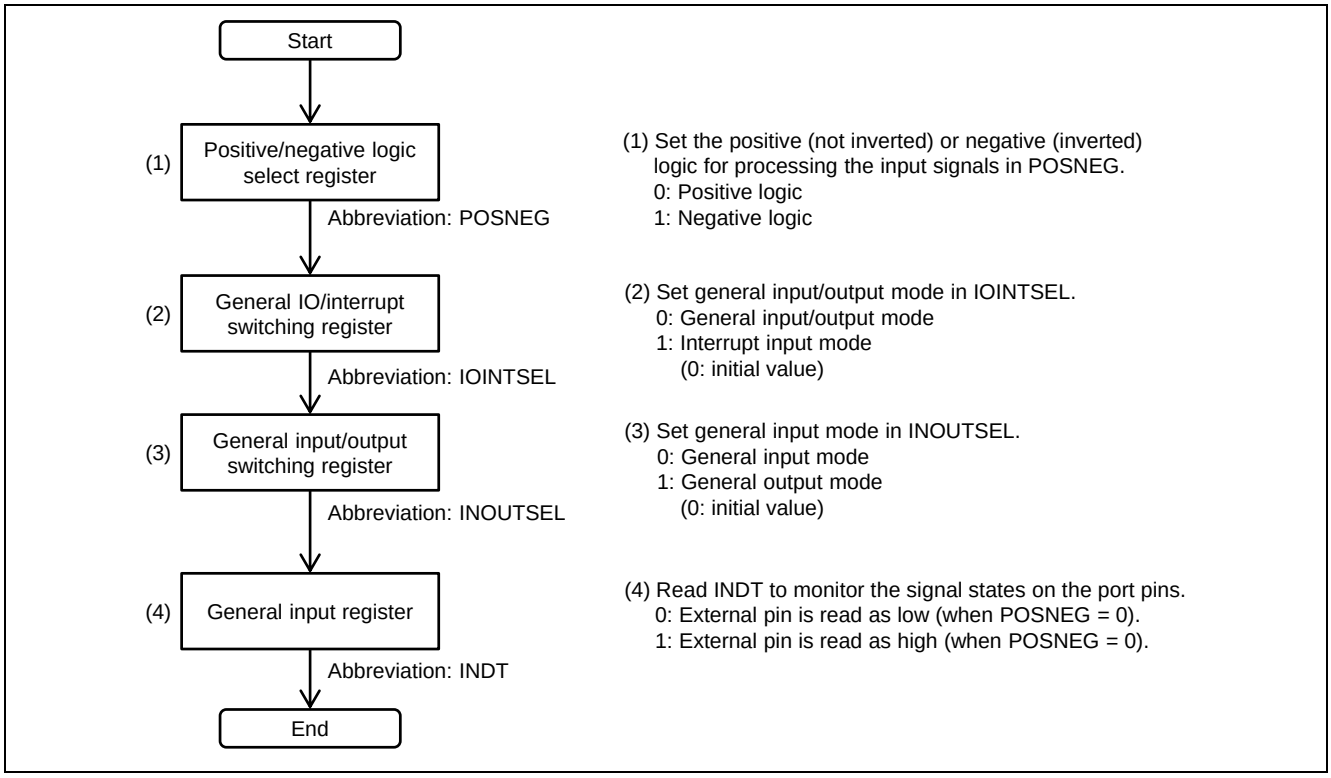
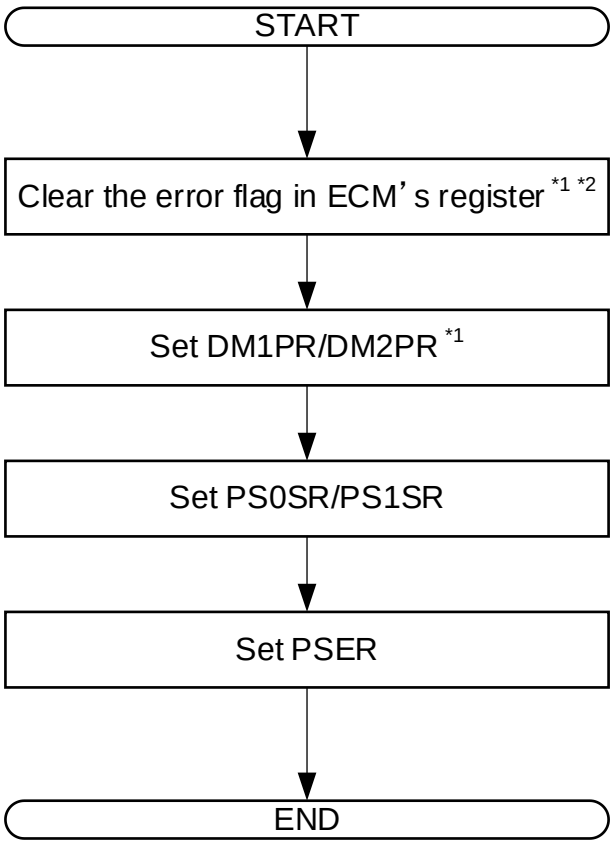


Figure 7.16 Flowchart of Setting the GPIO to General Input Mode

(6) Setting Port Safe State

For setting general input mode, refer to the procedure shown in Figure 7.16.



Note 1. This process is only for GP4 to 7.
Note 2. Refer to Section 158.45.3.5, ECMmECLRn — ECM Master/ Checker Error Clear Trigger Register n.

Figure 7.17 Flowchart of Setting the Port Safe State

(7) Switching GPIO to I2C

R-Car S4 has dedicated pin for I2C. Figure shows the example of setting flow.

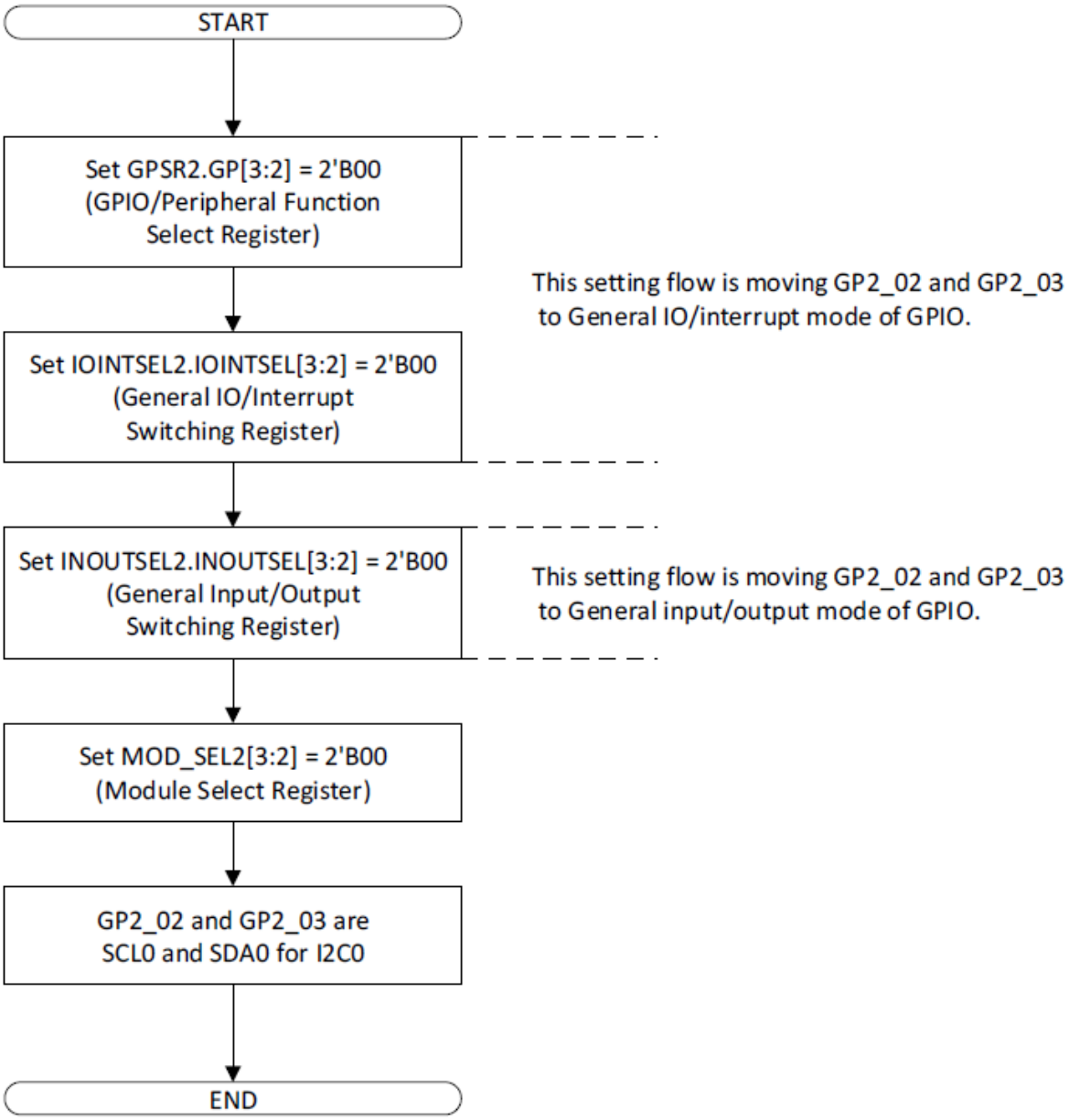


Figure 7.18 Flowchart of Setting GPIO to I2C

7.3.9 Port Safe State Function

To keep safe operating state (Port Safe State) in case of failure, and then stop it, Port Safe State operate to receive fault information from ECM and make Pin for each domain.

Output trouble information signal for each domain from ECM. This is received by the PFC, and it is controlled for each Pin so that it becomes Port Safe State.

Registers (PSSR 0, 1) that select 4 types of Port Safe State with 2 bits. Provide a register (PSER) to enable / disable this register.

Table 7.56 Port Safe State function

INPUT			OUTPUT
PSERn	PS1SRn		
bit[m*+16]	bit[m*×2+1]	bit[m*×2]	Port Safe State
0	*	*	Port Safe State is disable
1	0	0	Initial state = ON
1	0	1	HiZ = ON
1	1	0	Pull Down = ON
1	1	1	Pull Up = ON

Note: * m = 0 to 15

INPUT			OUTPUT
PSERn	PS0SRn		
bit[m*]	bit[m*×2+1]	bit[m*×2]	Port Safe State
0	*	*	Port Safe State is disable
1	0	0	Initial state = ON
1	0	1	HiZ = ON
1	1	0	Pull Down = ON
1	1	1	Pull Up = ON

Note: * m = 0 to 15

7.3.10 PRESETOUT1# Function

The following figure shows behavior of PRESETOUT#.

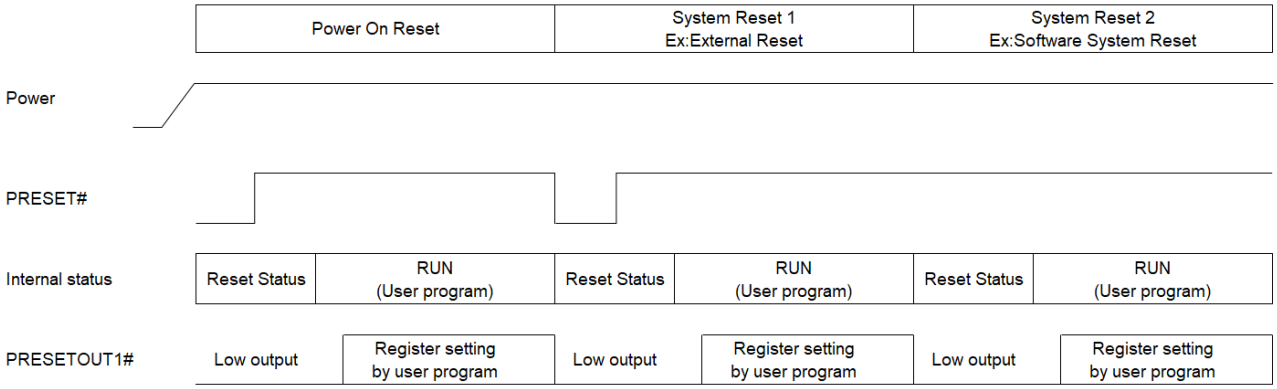


Figure 7.19 Timing Chart of PRESETOUT1# function for each reset factor

CAUTION:
To avoid data collision, the outside circuit connected to this pin must not drive in high level at any case.

7.4 Usage Notes

No description on this section.

7.5 Safety Mechanisms

No description on this section.