**ĐẠI HỌC QUỐC GIA TPHCM**

**TRƯỜNG ĐẠI HỌC BÁCH KHOA**

**KHOA ĐIỆN – ĐIỆN TỬ**





|  |  |
| --- | --- |
| **Họ và tên** | **MSSV** |
| **1. Nguyễn Thế Hoàng** | **2211102** |

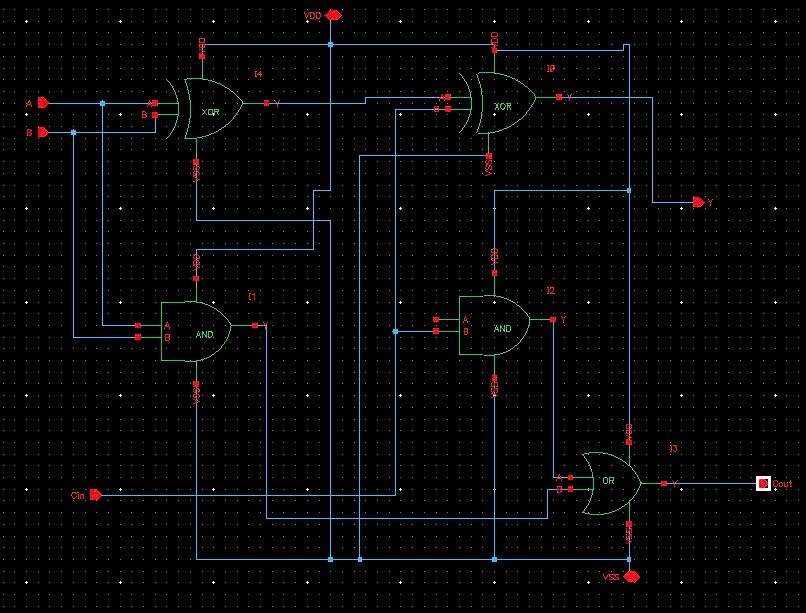
Mini project1

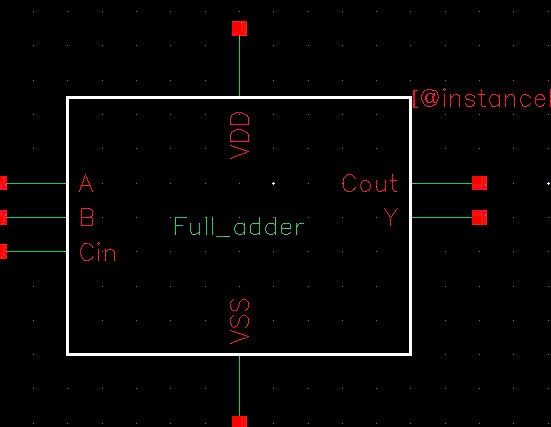
1-bit Full Adder

Truth table

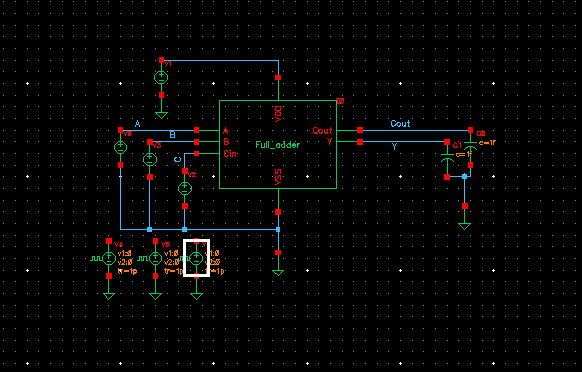
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input** | | | **Output** | |
| **A** | **B** | **Cin** | **Y** | **Cout** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Schematic



Symbol 

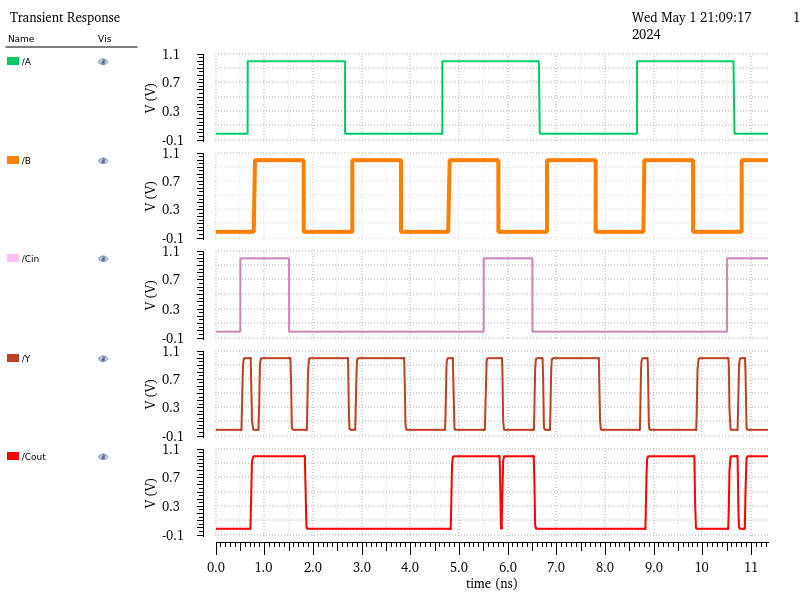
Transient simulation and DC analysis



Transient simulation

Vpulse

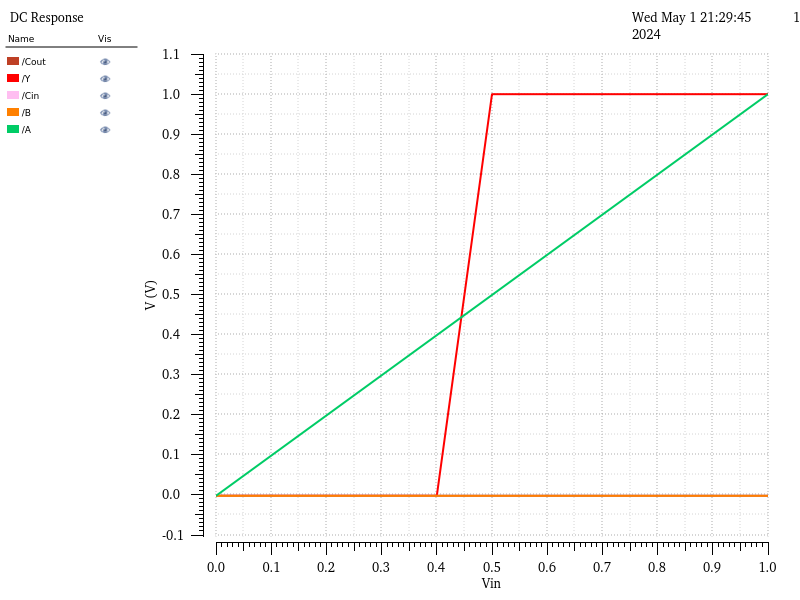
|  |  |  |  |
| --- | --- | --- | --- |
|  | A | B | Cin |
| V1 | 0 | 0 | 0 |
| V2 | 1 | 1 | 1 |
| Period | 4n | 2n | 5n |
| Delay time | 0.65n | 0.8n | 0.5n |
| Rise time | 1p | 1p | 1p |
| Fall time | 1p | 1p | 1p |
| Pulse width | 2n | 1n | 1n |



DC analysis

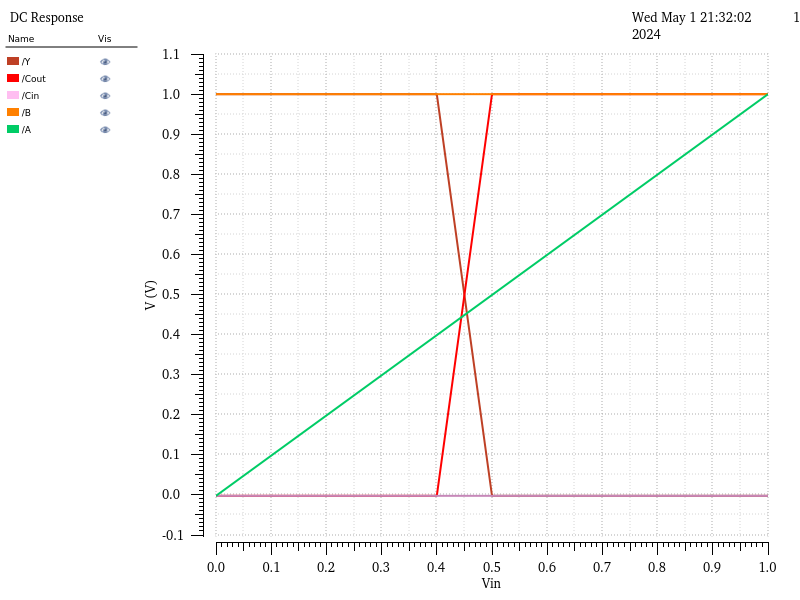
* VinA=[0,1]; B=0; Cin=0

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Vin (V) | 0 | 0.1 | 0.2 | 0.3 | 0.4 | 0.5 | 0.6 | 0.7 | 0.8 | 0.9 | 1 |
| Y (V) | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| Cout (V) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |



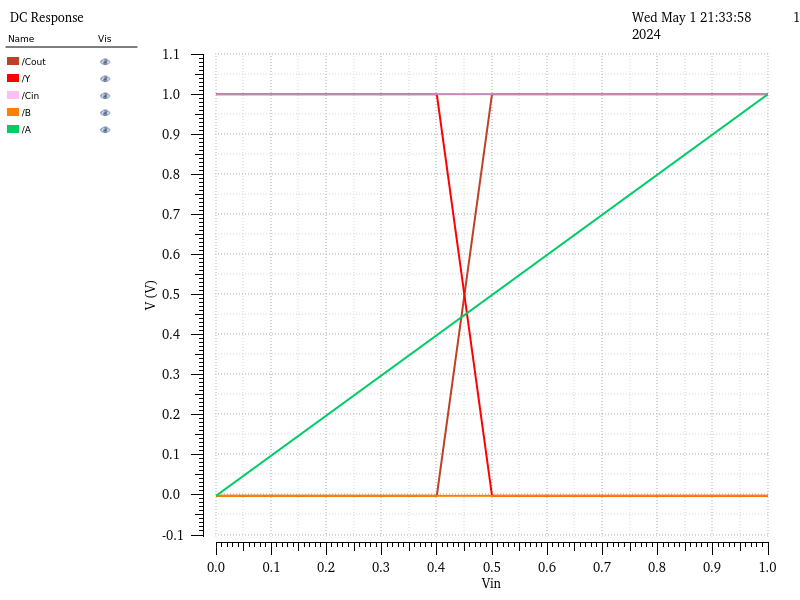
* A=[0,1]; B=1; Cin=0

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Vin (V) | 0 | 0.1 | 0.2 | 0.3 | 0.4 | 0.5 | 0.6 | 0.7 | 0.8 | 0.9 | 1 |
| Y (V) | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Cout (V) | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |



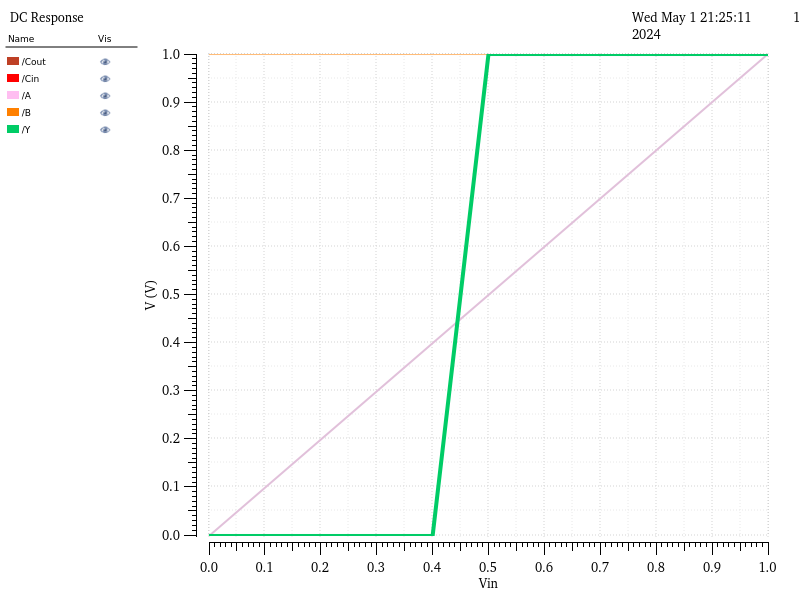
* A=[0,1]; B=0; Cin=1

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Vin (V) | 0 | 0.1 | 0.2 | 0.3 | 0.4 | 0.5 | 0.6 | 0.7 | 0.8 | 0.9 | 1 |
| Y (V) | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Cout (V) | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |



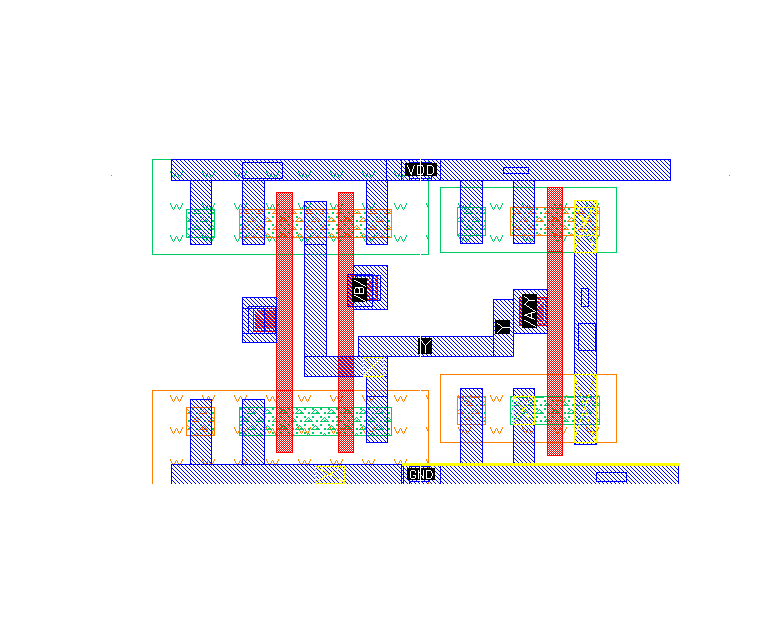
* A=[0,1]; B=1; Cin=1

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Vin (V) | 0 | 0.1 | 0.2 | 0.3 | 0.4 | 0.5 | 0.6 | 0.7 | 0.8 | 0.9 | 1 |
| Y (V) | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| Cout (V) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

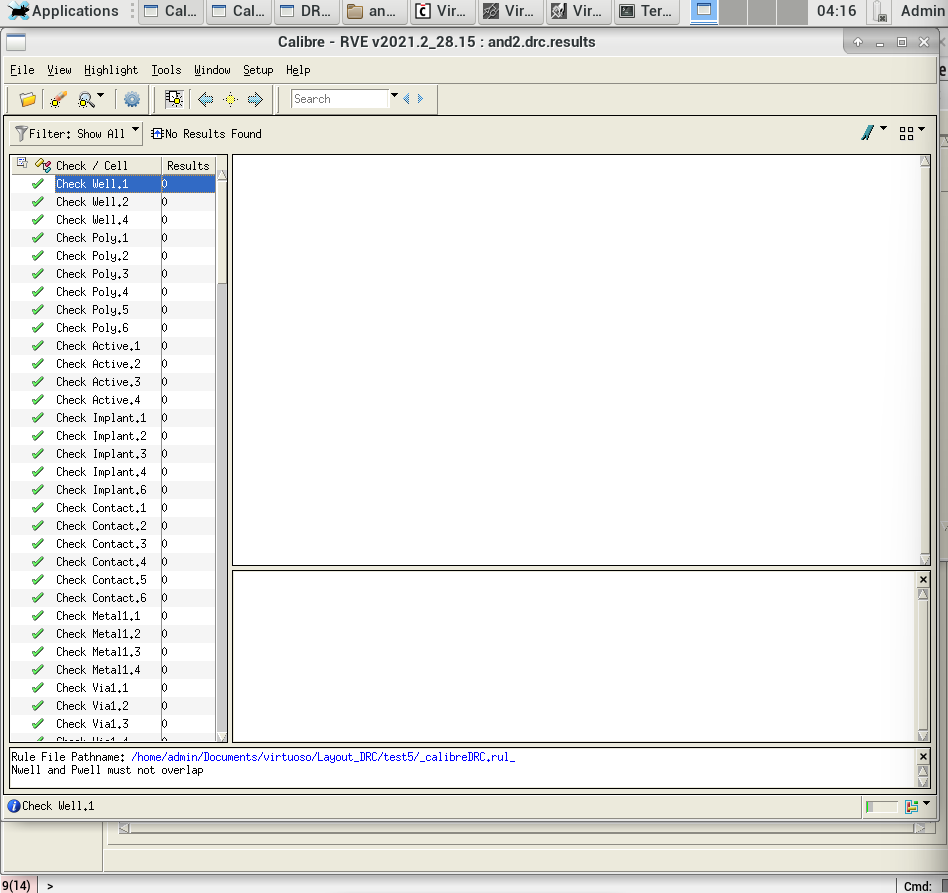


1. Layout for logic gates

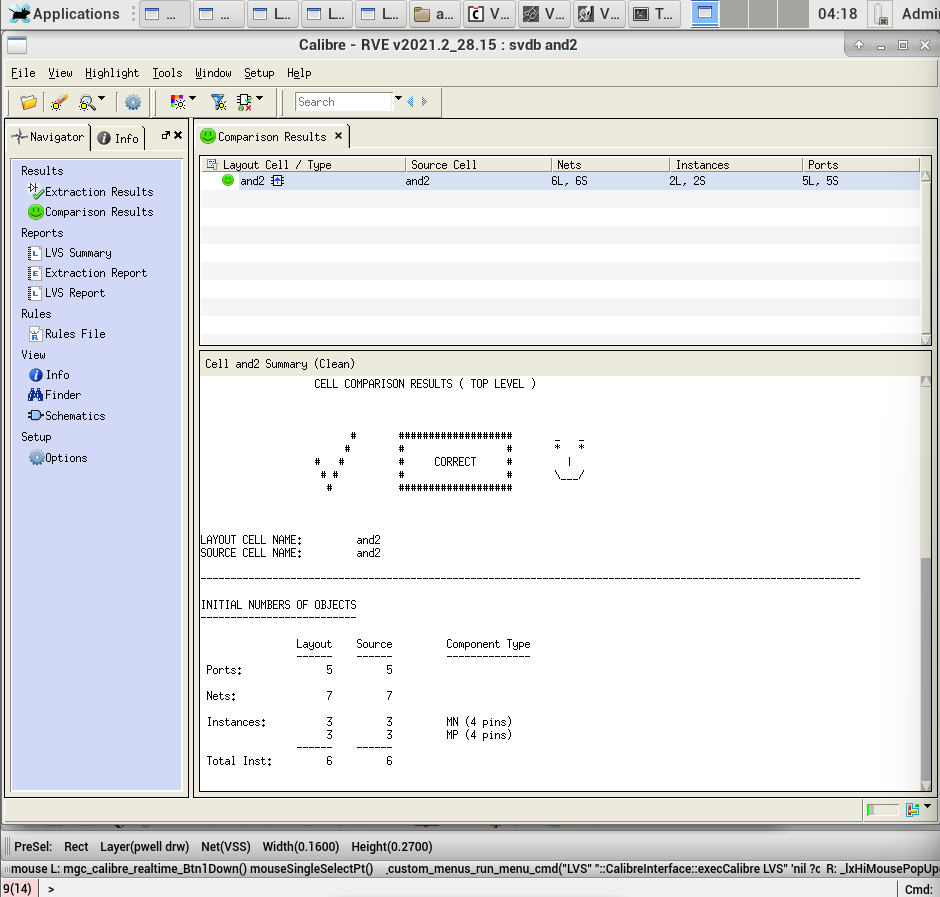
AND2



Layout

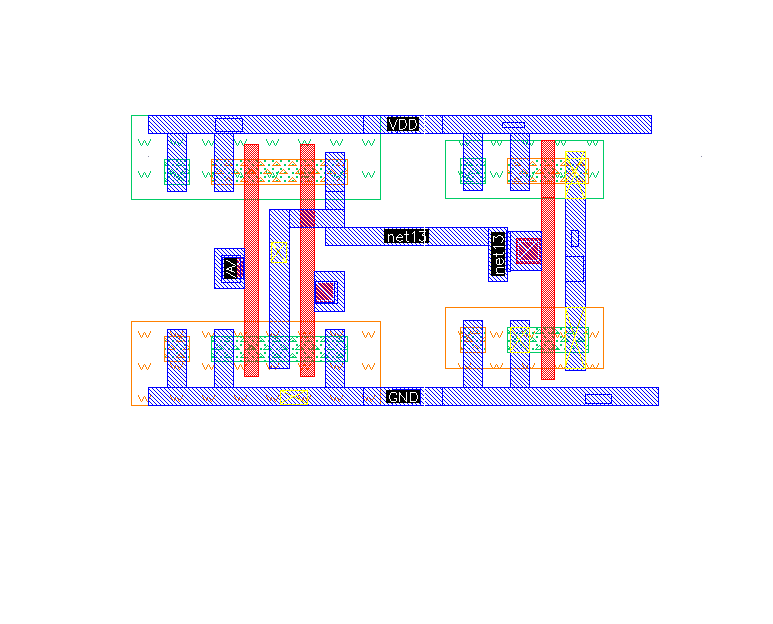


DRC check

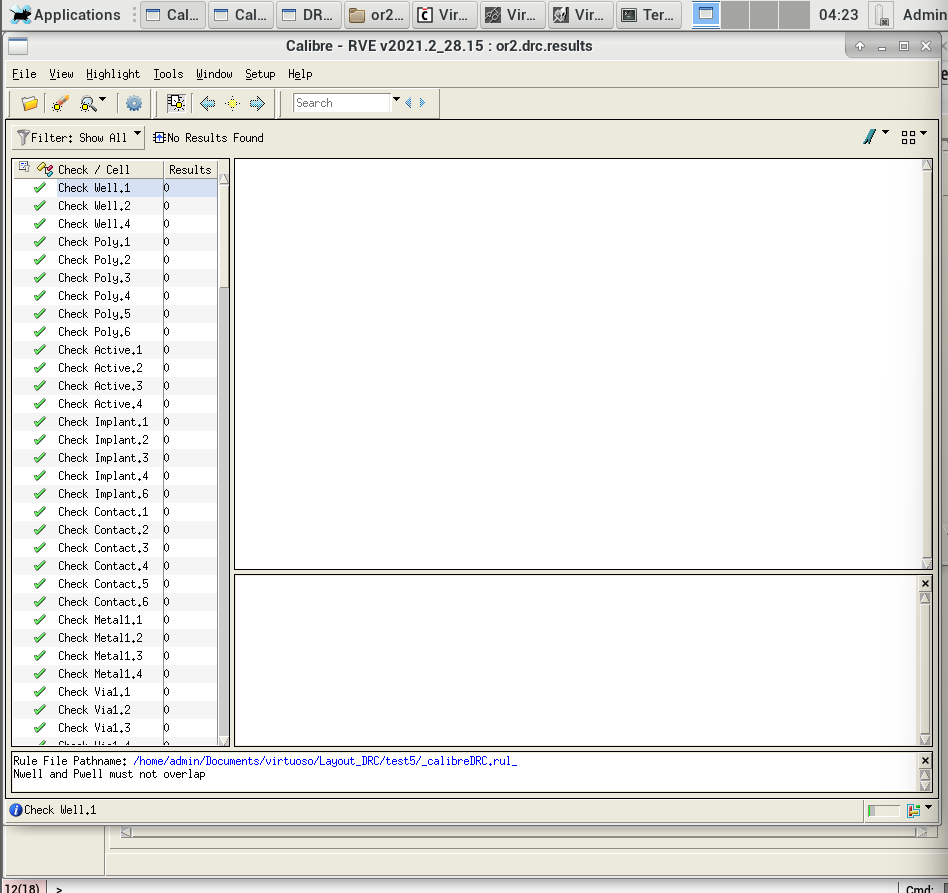


Proof of LVS

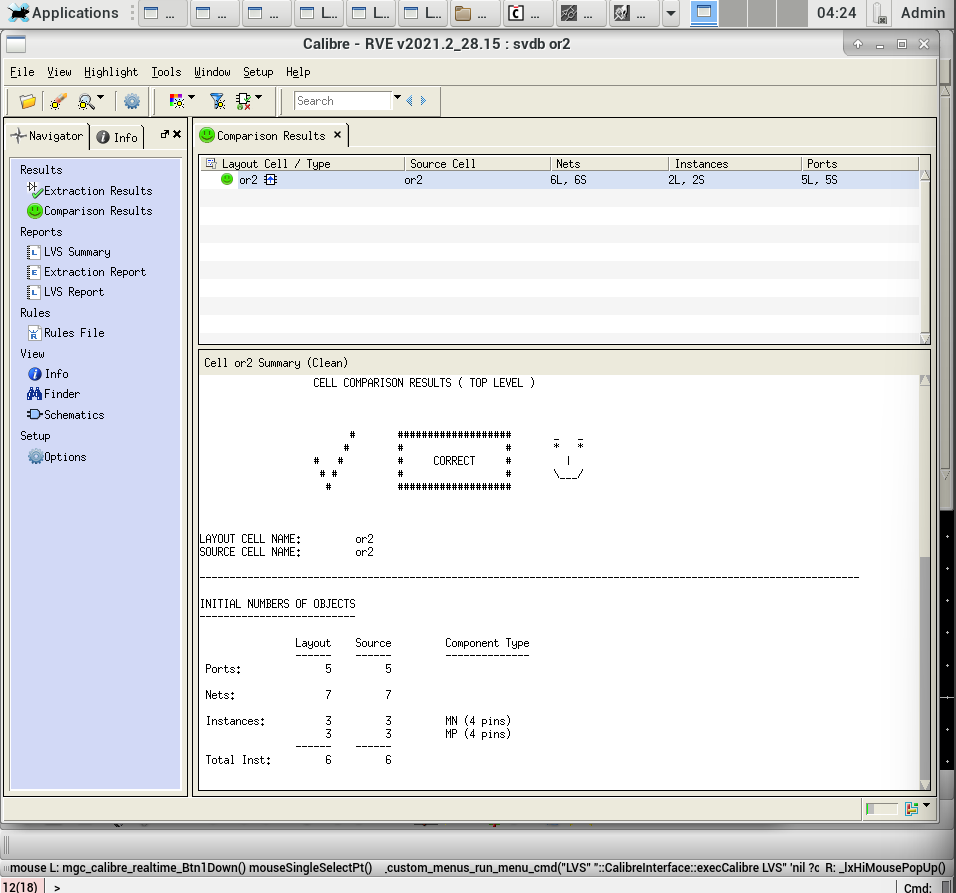
OR2



Layout

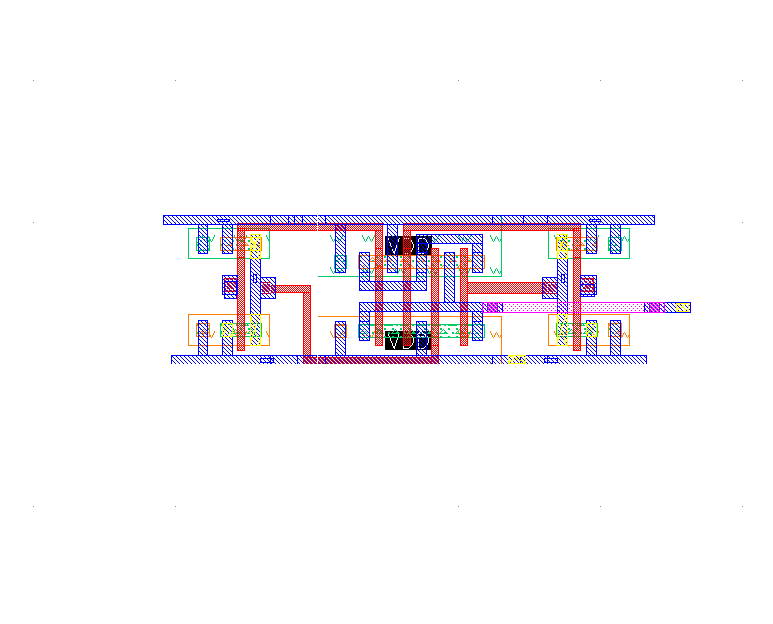


DRC check

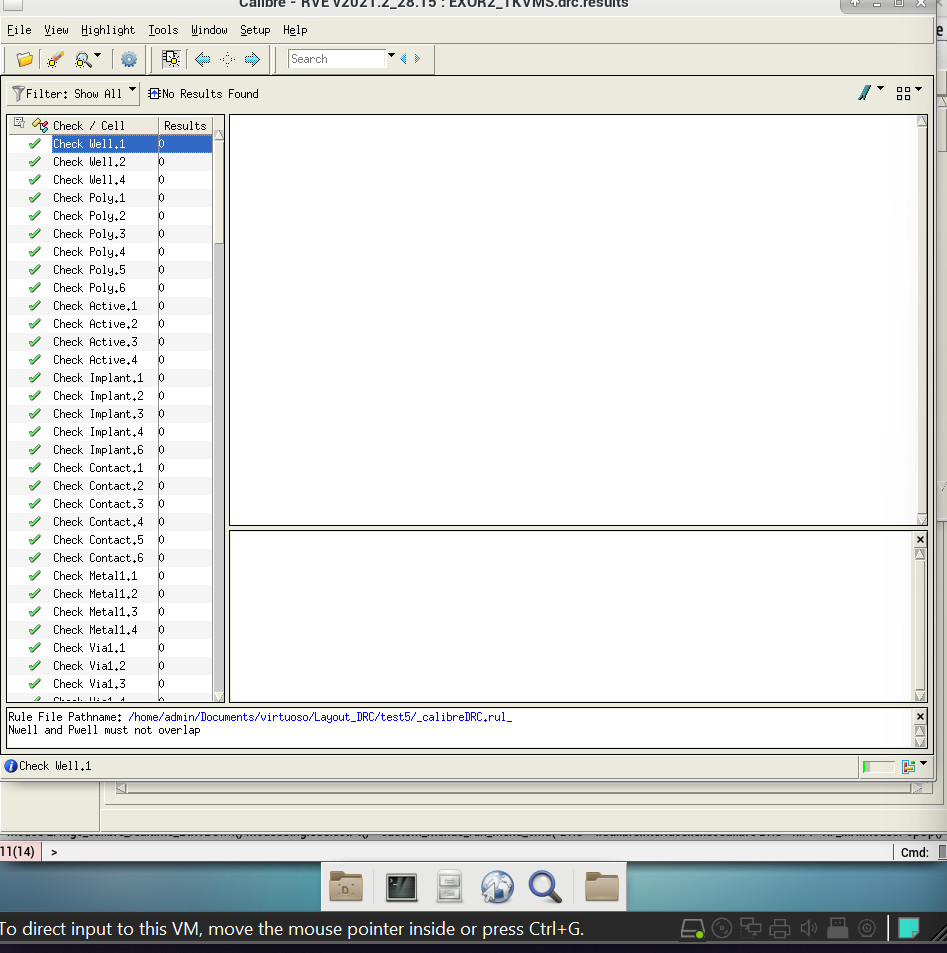


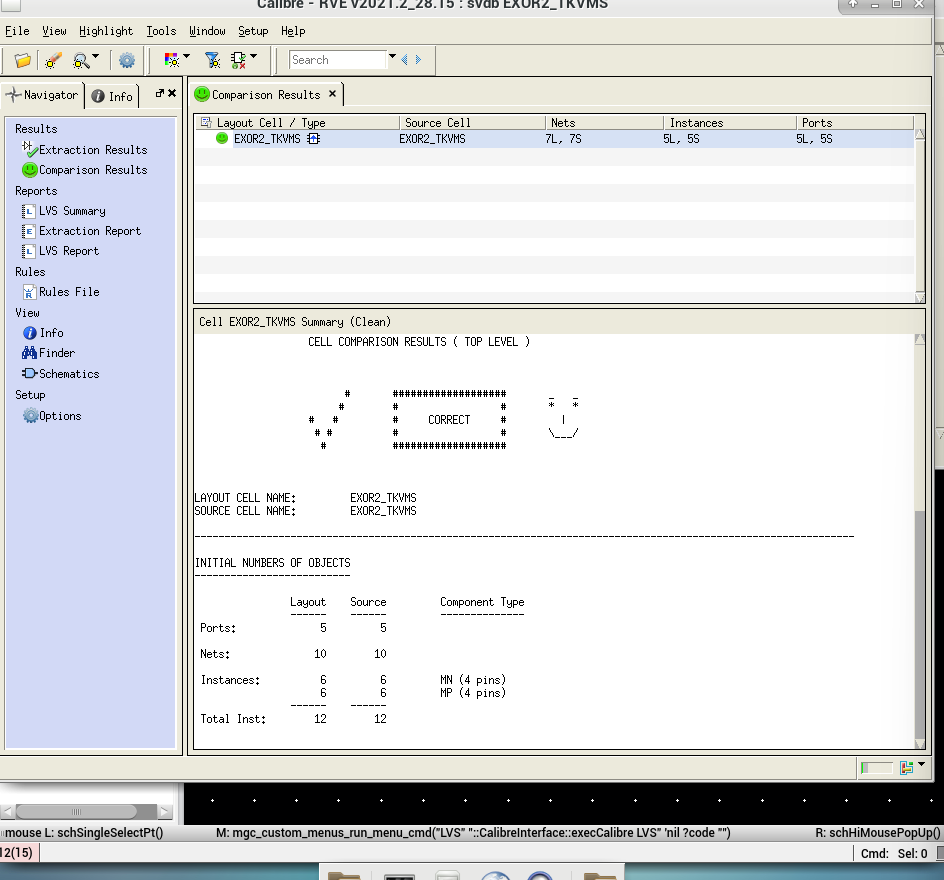
Proof of LVS

XOR



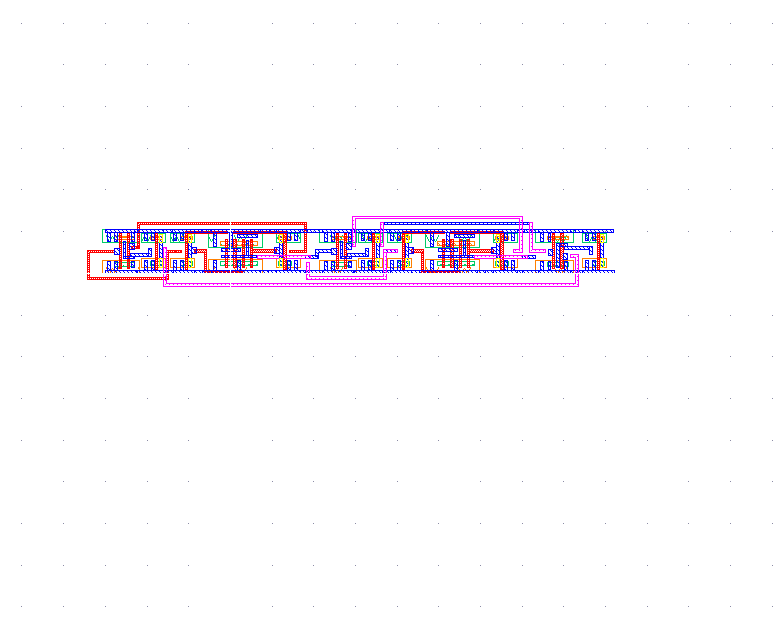
Layout

DRC check

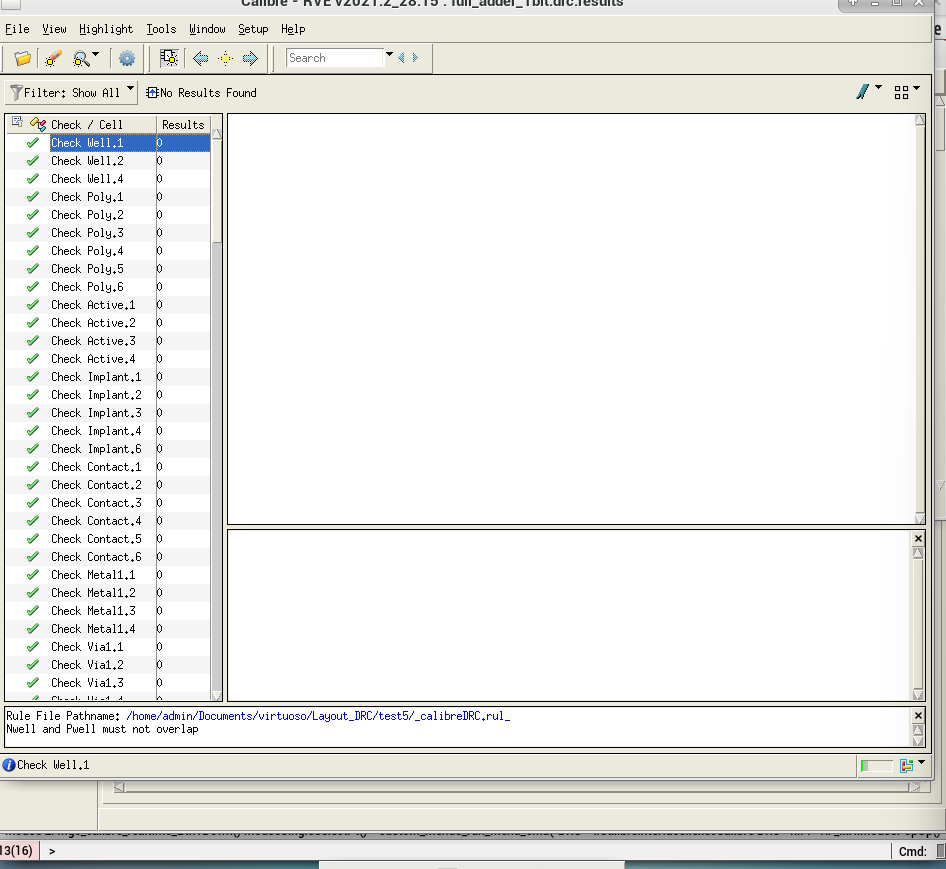


Proof of LVS

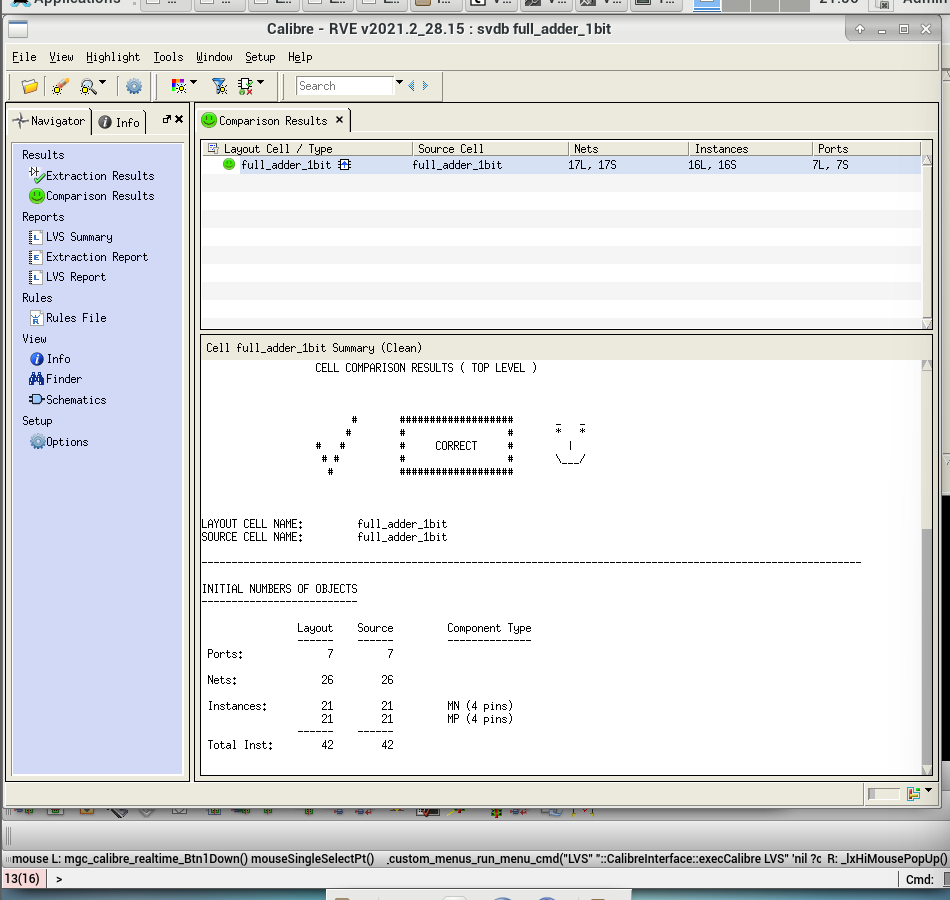
1-bit Full adder layout



Layout



DRC check



Proof of LVS