

ĐẠI HỌC QUỐC GIA TPHCM
TRƯỜNG ĐẠI HỌC BÁCH KHOA
KHOA ĐIỆN – ĐIỆN TỬ



**DIGITAL IC DESIGN
LABORATORY 4
LOGIC SYNTHESIS**

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Mentor: Nguyen Phan Thien Phuc

Class L03 - Group 35

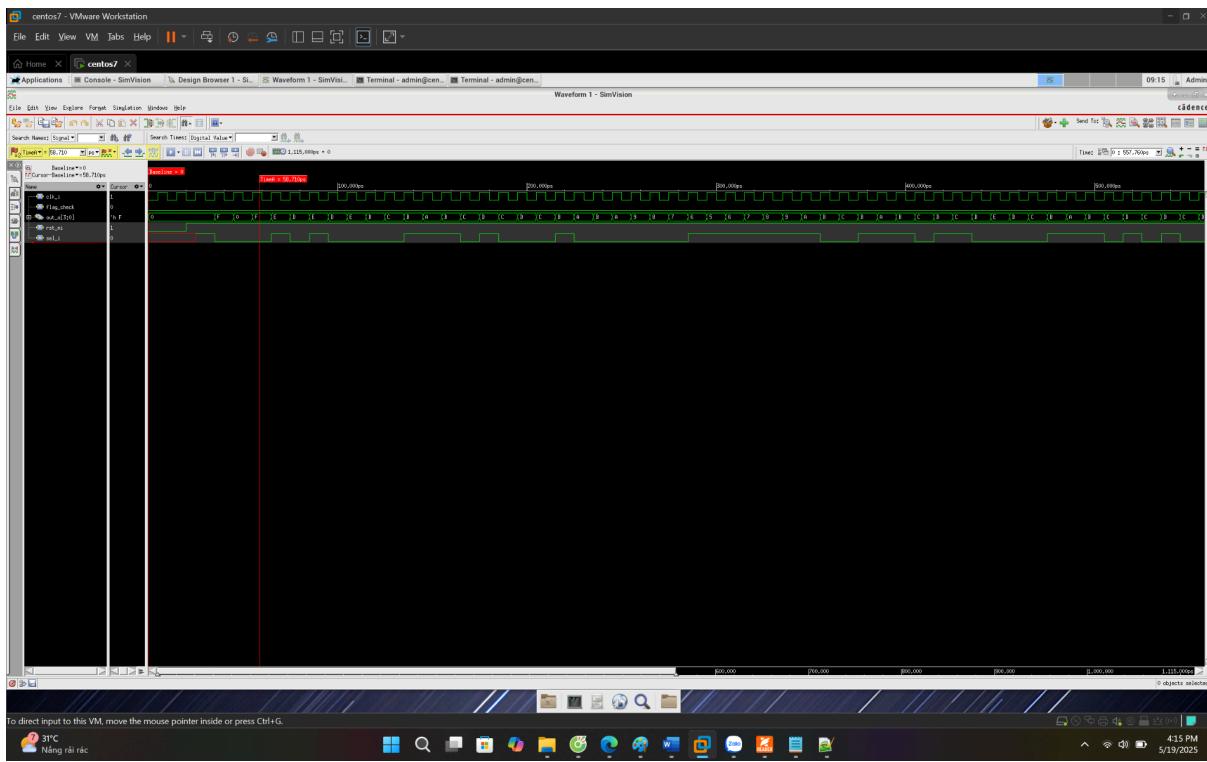
| Họ và tên | MSSV |
|---------------------|---------|
| 1. Nguyễn Thế Hoàng | 2211102 |
| 2. Nguyễn Thành Huy | 2211245 |
| 3. Nguyễn Quang Huy | 2211205 |

EXPERIMENT 1: 4 bit UP/DOWN COUNTER

Verification plan:

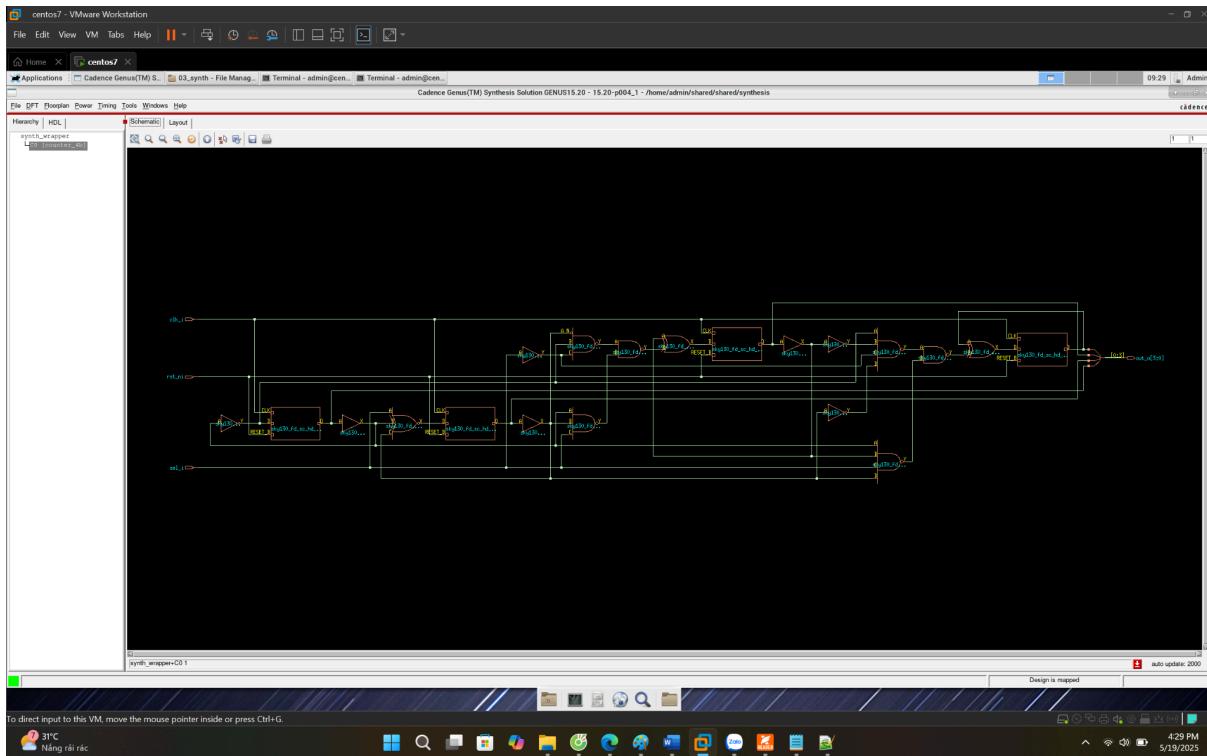
| section | item | description | Test case | status |
|---------|------------|--|-----------|--------|
| 1 | reset | When rst_n = 0 , the output is 0 . When rst_n = 1 , the output is updated on the rising edge of the clock signal; it counts up if sel = 1 , and counts down if sel = 0 | rst_test | pass |
| 2 | Max count | When the output is 4'b1111 and sel = 1 , on the next rising edge of the clock, the output will become 4'b0000 | max_test | pass |
| 3 | Min count | When the output is 4'b0000 and sel = 0 , on the next rising edge of the clock, the output will become 4'b1111 | min_test | pass |
| 4 | Count up | When rst_n = 1 and sel = 1 , the output increments by 1 on each rising edge of the clock | up_test | pass |
| 5 | Count down | When rst_n = 1 and sel = 0 , the output decrements by 1 on each rising edge of the clock | down_test | pass |

Waveform :

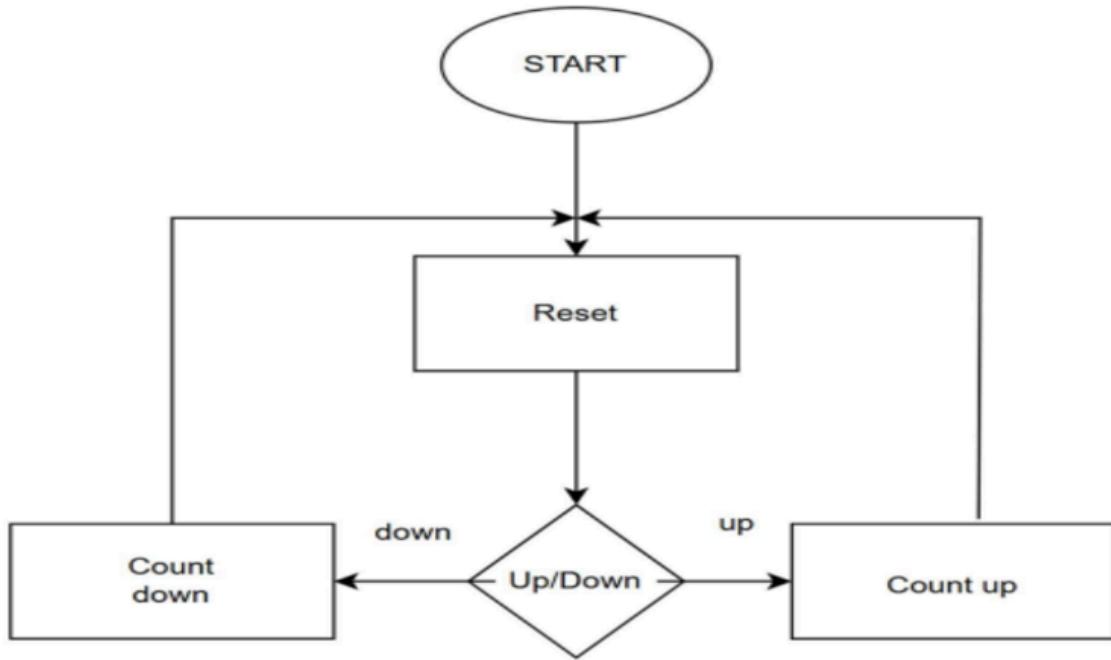


Based on the waveform, it can be concluded that the module operates as intended.

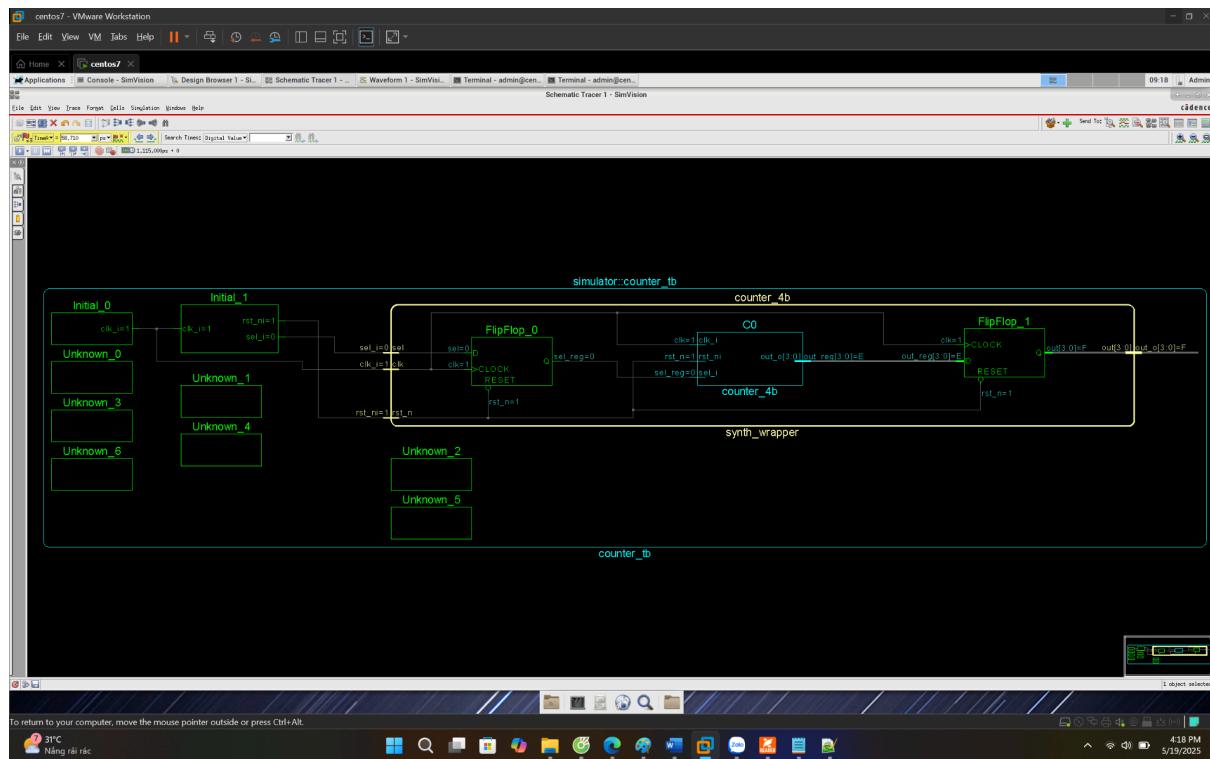
Netlist :



Flow chart :



Block diagram :



Timing MET with frequency at 1.0GHz:

Total area of the design:

The screenshot shows a Linux desktop environment with a terminal window open. The terminal window title is "synth_wrapper.area.rpt". The content of the terminal is as follows:

```
centos7 - VMware Workstation
File Edit View VM Tabs Help || Applications Home centos7 Applications synth_wrapper.gates... synth_wrapper.area.rpt 04_reports - File Mana... Terminal - admin@cen... Terminal - admin@cen...
File Edit Search View Document Help
Generated by: Genus15(TM) Synthesis Solution GENUS15.20 - 15.20-p884_1
Generated on: May 19 2025 05:25:41 am
Module: synth_wrapper
Interconnect mode: generic
Area mode: timing library
=====
Instance Cells Cell Area Net Area Total Area
synth_wrapper 25 378 128 490
C0 20 244 74 318
```

The desktop interface includes a menu bar, a dock with various icons, and a system tray at the bottom right.

Gate usage of the design:

```

centos7 - VMware Workstation
File Edit View VM Tabs Help ||| Home Applications Terminal - admin@cen... Terminal - admin@cen...
+synth_wrapper.gates.pvt - Mousepad

File Edit Search View Document Help
Generated by: Genus15.20 Synthesis Solution GENUS15.20 - 15.20 p084_1
Generated on: May 19, 2025 05:25:41 am
Module: synth_wrapper
Interconnect mode: global
Area mode: timing library

Gate Instances Area Library
sky13B_fd_sc_hd_buf_4 3 22.522 sky13B_fd_sc_hd_tt_025C_lv00
sky13B_fd_sc_hd_cinbuf_1 2 159.567 sky13B_fd_sc_hd_tt_025C_lv00
sky13B_fd_sc_hd_dfftp_1 2 175.168 sky13B_fd_sc_hd_tt_025C_lv00
sky13B_fd_sc_hd_dfftp_2 2 52.558 sky13B_fd_sc_hd_tt_025C_lv00
sky13B_fd_sc_hd_inv_1 1 1.944 sky13B_fd_sc_hd_tt_025C_lv00
sky13B_fd_sc_hd_inv_2 1 3.754 sky13B_fd_sc_hd_tt_025C_lv00
sky13B_fd_sc_hd_nand2_2 2 12.512 sky13B_fd_sc_hd_tt_025C_lv00
sky13B_fd_sc_hd_nand3_1 1 1.500 sky13B_fd_sc_hd_tt_025C_lv00
sky13B_fd_sc_hd_nand3_1 1 7.587 sky13B_fd_sc_hd_tt_025C_lv00
sky13B_fd_sc_hd_nand3_2 1 25.492 sky13B_fd_sc_hd_tt_025C_lv00
sky13B_fd_sc_hd_xor3_1 1 22.522 sky13B_fd_sc_hd_tt_025C_lv00
sky13B_fd_sc_hd_xor3_2 2 32.531 sky13B_fd_sc_hd_tt_025C_lv00
total 25 370.355

Type Instances Area Area %
-----
inverter 4 15.014 6.1
buffer 3 22.522 6.1
buffer 3 38.555 20.4
total 25 370.355 100.0

```

-Algorithm of arithmetic compute unit architecture used in the design:

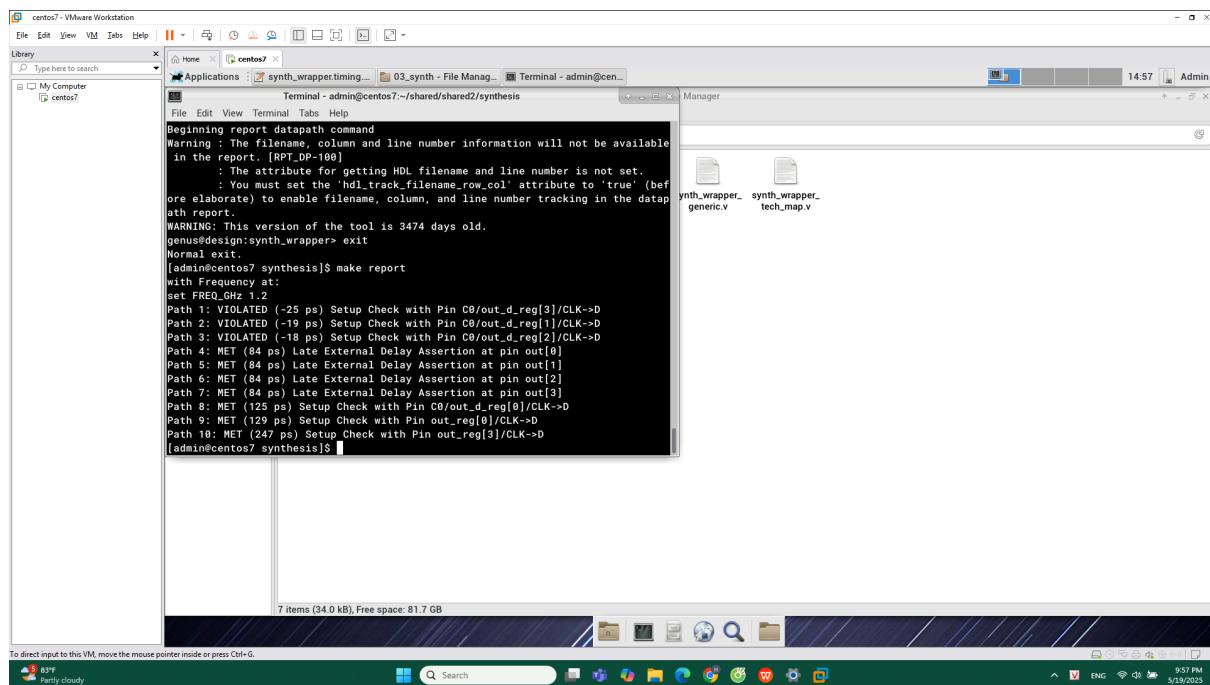
```

centos7 - VMware Workstation
File Edit View VM Tabs Help ||| Home Applications 00_src - File Manager Terminal - admin@cen... Terminal - admin@cen...
+list1 - Mousepad
File Edit Search View Document Help
00_src/full_adder.sv
00_src/full_subtractor.sv
00_src/4bit_adder.sv
00_src/subtractor_4b.sv
00_src/counter_4b.sv
00_src/synth_wrapper.v

To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

```

Highest frequency of the design : 1.1GHz is the highest frequency.(Violated at 1.2 GHz)



EXPERIMENT 2:

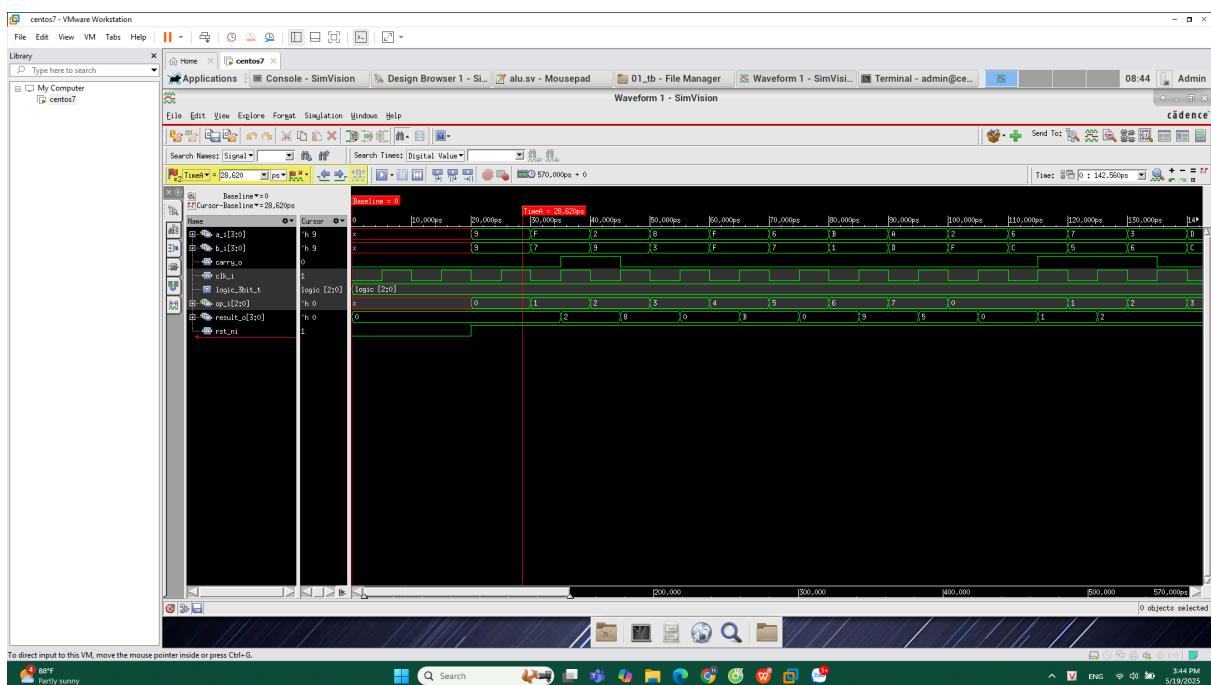
4-bit ALU

Verification plan:

| section | item | description | Test case | status |
|---------|-------------|---|-----------------------------------|--------|
| 1 | reset | If <code>rst = 0</code> , all outputs including the carry and the result will be 0. If <code>rst = 1</code> , the ALU operates normally based on the input variables. | <code>alu_RST_test</code> | pass |
| 2 | ADDITION | When <code>op = 3'b000</code> , the result is $a + b$. If a (MSB) + b (MSB) causes an overflow, a 1 will be stored in the carry flag. | <code>alu_addition_test</code> | pass |
| 3 | SUBTRACTION | When <code>op = 3'b001</code> , the result is $a - b$. If $a - b < 0$, the value will be stored in the borrow flag. | <code>alu_subtraction_test</code> | pass |
| 4 | AND | When <code>op = 3'b010</code> , the result is $a \& b$, performing a bitwise AND on two 4-bit variables. | <code>alu_and_test</code> | pass |

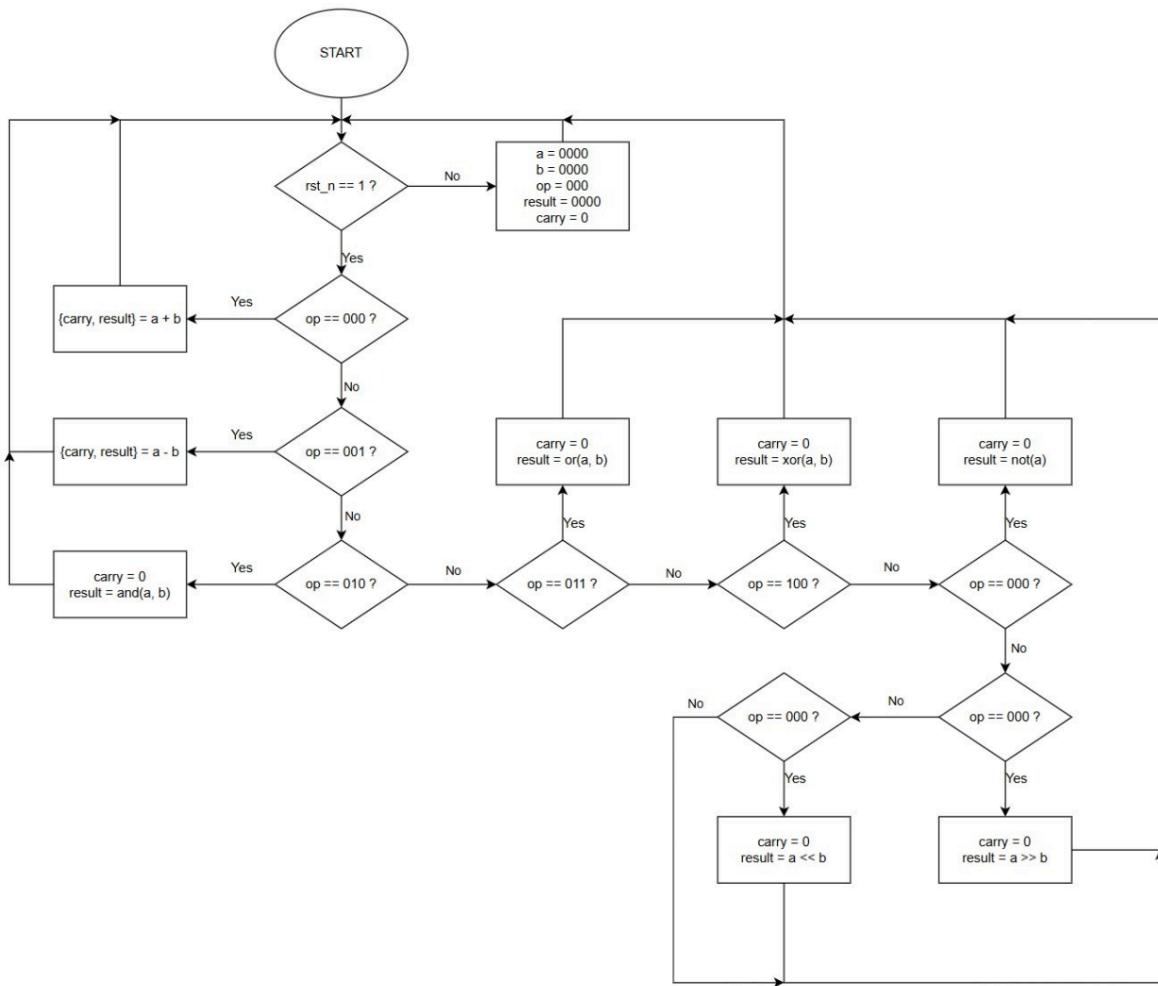
| | | | | |
|---|-------------|---|----------------------|------|
| 5 | OR | When op = 3'b011, the result is a b, performing a bitwise OR on two 4-bit variables | alu_or_test | pass |
| 6 | XOR | When op = 3'b100, performing a bitwise XOR on two 4-bit variables | alu_xor_test | pass |
| 7 | NOT | When op = 3'b101, the result is !a, performing bitwise NOT. | alu_not_test | pass |
| 8 | SHIFT RIGHT | When op = 3'b110, the result is a >> b, and the result is 0 when b is out of range | alu_shift_right_test | pass |
| 9 | SHIFT LEFT | When op = 3'b111, the result is a << b, and the result is 0 when b is out of range. | alu_shift_left_test | pass |

Waveform:

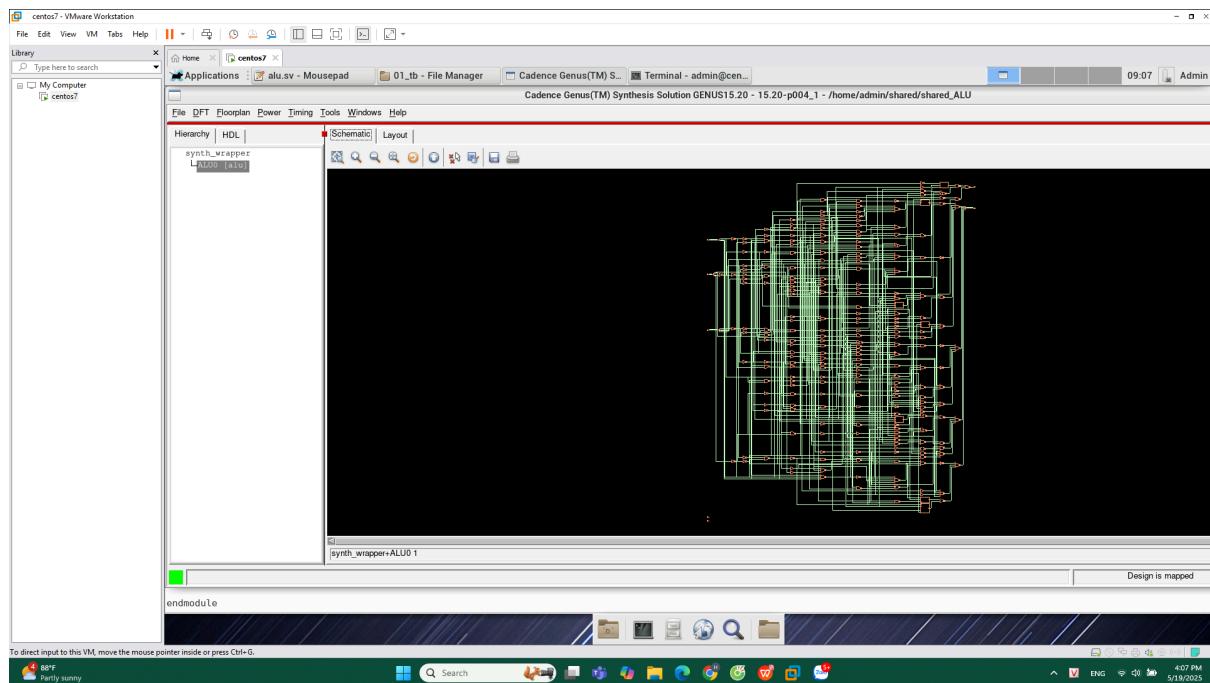


The observed waveform confirms that the module is functioning properly.

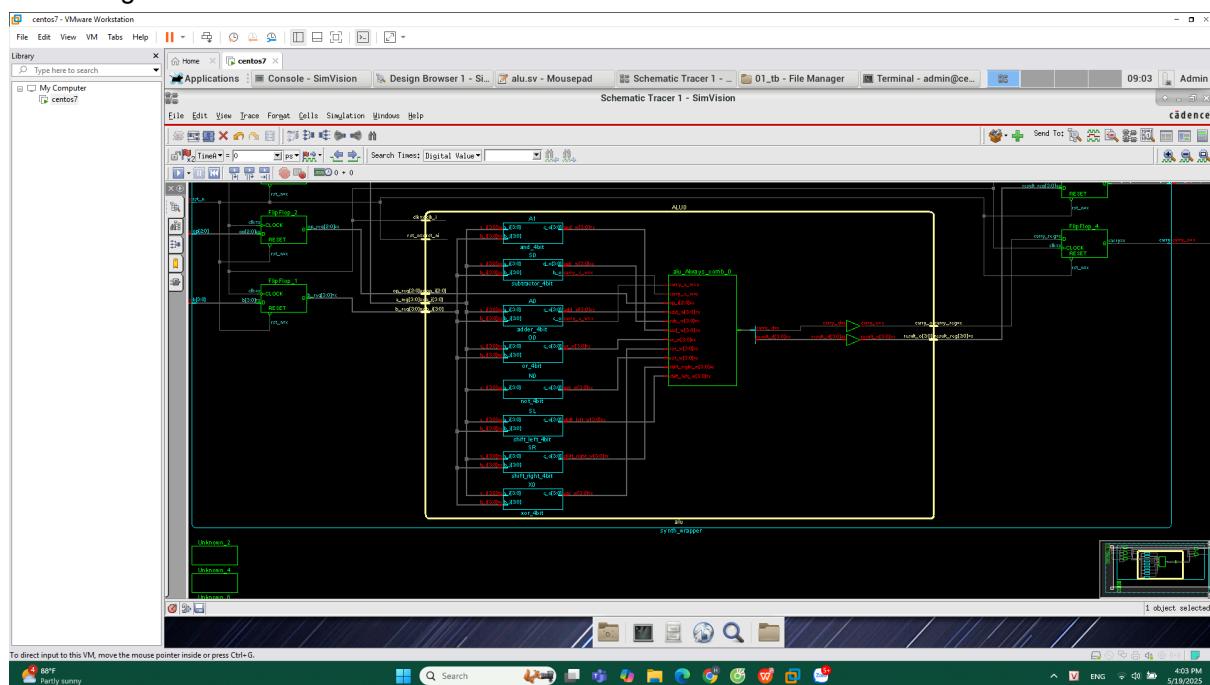
Flow chart:

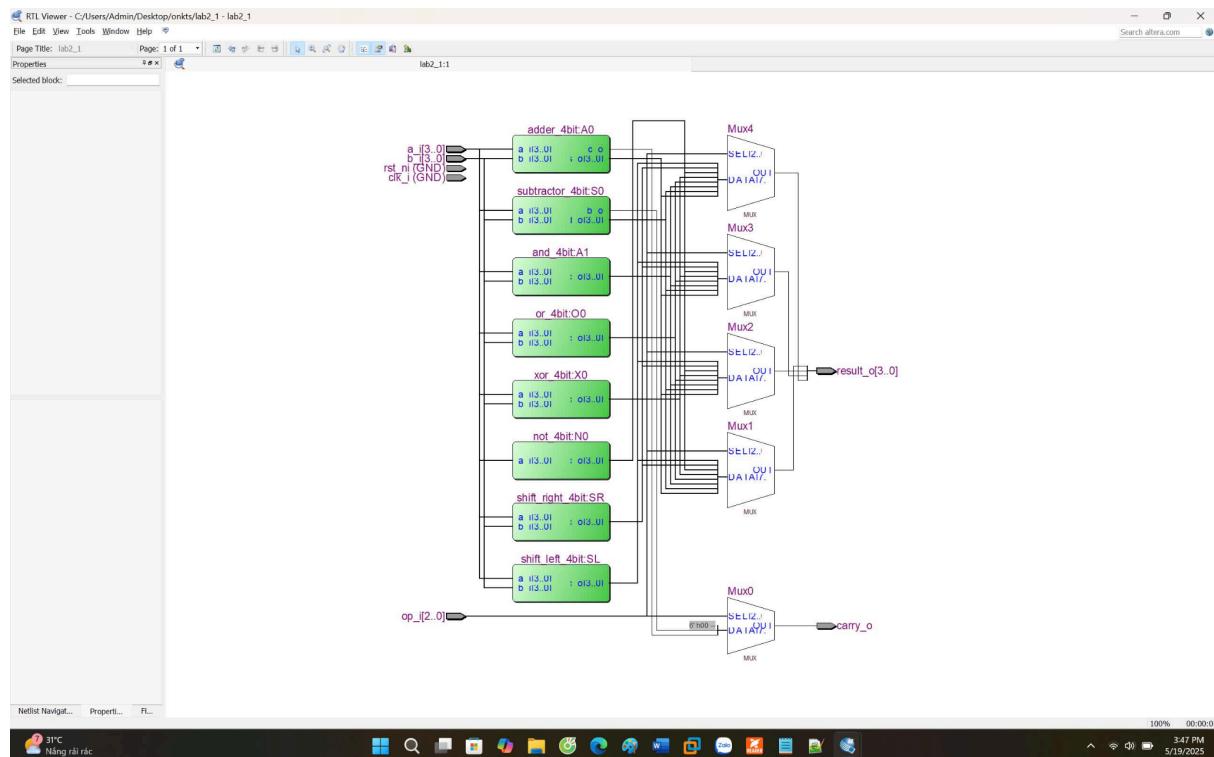


Netlist:



Block diagram:



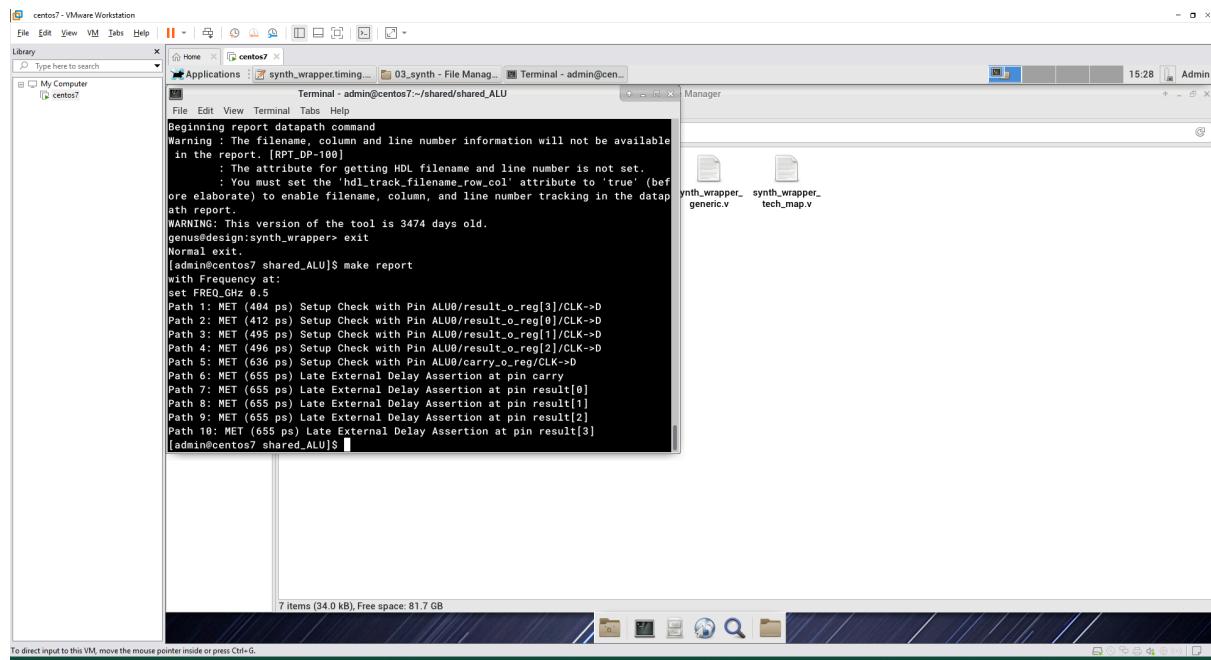


Input/output description:

| Signal | Width | Type | Description |
|--------------------|-------|-------|------------------|
| <code>clk</code> | 1 | input | Clock signal |
| <code>rst_n</code> | 1 | input | Reset signal |
| <code>a</code> | 4 | input | First argument |
| <code>b</code> | 4 | input | second argument |
| <code>op</code> | 3 | input | Select operation |

| | | | |
|--------|---|--------|---------------|
| result | 4 | output | Result of ALU |
| carry | 1 | output | Carry flag |

Timing MET with frequency at 0.5 GHz:



```

Centos7 - VMware Workstation
File Edit View VM Tabs Help
Library
Type here to search centos7
My Computer
File Edit View Terminal Tabs Help
Applications : synth_wrapper.timing... 03_synth - File Manager Terminal - admin@cen...
Terminal - admin@centos7:~/shared/shared_ALU
File Edit View Terminal Help
Beginning report datapath command
Warning : The filename, column and line number information will not be available
in the report. [RPT_DP=100]
    The attribute for getting HDL filename and line number is not set.
    : You must set the 'hdl_track_filename.row.col' attribute to 'true' (bef
ore elaborate) to enable filename, column, and line number tracking in the datap
ath report.
WARNING: This version of the tool is 3474 days old.
genusdesign:synth_wrapper> exit
Normal exit.
[admin@centos7 shared_ALU]$ make report
with Frequency at:
set FREQ_GHz 0.5
Path 1: MET (404 ps) Setup Check with Pin ALU0/result_o_reg[3]/CLK->D
Path 2: MET (412 ps) Setup Check with Pin ALU0/result_o_reg[0]/CLK->D
Path 3: MET (495 ps) Setup Check with Pin ALU0/result_o_reg[1]/CLK->D
Path 4: MET (496 ps) Setup Check with Pin ALU0/result_o_reg[2]/CLK->D
Path 5: MET (636 ps) Setup Check with Pin ALU0/carry_o_reg/CLK->D
Path 6: MET (655 ps) Late External Delay Assertion at pin carry
Path 7: MET (655 ps) Late External Delay Assertion at pin result[0]
Path 8: MET (655 ps) Late External Delay Assertion at pin result[1]
Path 9: MET (655 ps) Late External Delay Assertion at pin result[2]
Path 10: MET (655 ps) Late External Delay Assertion at pin result[3]
[admin@centos7 shared_ALU]$ 

```

To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

Total area of the design:

```

Centos7 - VMware Workstation
File Edit View VM Tabs Help
Library Type here to search
My Computer centos7
Applications synth_wrapper.timing... synth_wrapper.gates.r... synth_wrapper.area.rp... 04_reports - File Mana... Terminal - admin@cen...
synth_wrapper.area.rpt - Mousepad
File Edit Search View Document Help
Generated by: Genus(TM) Synthesis Solution GENUS15.20 - 15.20-p004_1
Generated on: May 19 2025 11:41:30 am
Module: synth wrapper
Interconnect mode: global
Area mode: timing library
-----
Instance Cells Cell Area Net Area Total Area
synth_wrapper 115 1134 679 1813
ALU0 99 729 486 1216

```

To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

Gate usage of the design:

```

Centos7 - VMware Workstation
File Edit View VM Tabs Help
Library Type here to search
My Computer centos7
Applications synth_wrapper.timing... synth_wrapper.gates.r... synth_wrapper.area.rp... 04_reports - File Mana... Terminal - admin@cen...
synth_wrapper.gates.rpt - Mousepad
File Edit Search View Document Help
Generated by: Genus(TM) Synthesis Solution GENUS15.20 - 15.20-p004_1
Generated on: May 19 2025 11:41:30 am
Module: synth wrapper
Interconnect mode: global
Area mode: timing Library
-----
Gate Instances Area Library
sky130_fd_sc_hd_a2l0_1 3 22.522 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_a2l01_1 4 20.819 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_a2l01_2 1 8.758 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_a2l01_3 1 15.754 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_a2l01_4 1 7.507 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_a2bb2o1_1 1 8.758 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_a2z01_1 1 8.758 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_a3z01_1 1 8.758 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_and2b_1 3 22.522 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_and2b_2 1 10.819 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_and3b_1 2 17.517 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_and3b_2 1 10.819 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_buf_1 1 3.754 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_cikinv_1 2 7.507 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_dffrtp_1 18 45.032 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_dffrtp_2 3 78.826 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_ha_1 1 12.512 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_inv_1 4 15.814 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_inv_2 5 18.768 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_inv_3 1 20.819 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_nand2_1 11 41.290 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_nand2b_1 6 37.538 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_nor2_1 8 30.022 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_nor2_2 2 12.512 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_nor2_3 3 18.768 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_nor3_1 10 40.708 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_nor3b_1 1 7.507 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_o2l11a1_1 1 8.758 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_o2l11a1_2 2 15.814 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_o2l11a1_3 1 3.754 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_o2l1a1_1 2 10.819 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_o2l1a1_2 3 26.275 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd_o2lba_1 1 10.819 sky130_fd_sc_hd_tt_025C_lv88

```

To direct input to this VM, move the mouse pointer inside or press Ctrl+G.

```

File Edit Search View Document Help
sky130_fd_sc_hd__ha_1 1 12.512 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__inv_1 4 15.014 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__mux2_1 5 1.763 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__mux2_1 6 20.049 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__nand2_1 11 41.290 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__nand2b_1 6 37.530 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__nor2_1 8 39.029 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__nor2_2 2 12.512 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__nor2b_1 3 18.018 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__nor3_1 2 18.018 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__nor3b_1 1 7.507 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2l1a1_1 1 8.758 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2l1a1_1 2 15.014 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2l1a1_1 3 5.370 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2l1a1_1 4 10.010 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2l1a2_1 3 26.275 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2lba_1 1 10.010 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2lba_1 2 11.261 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2lba_1 3 11.261 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2lba_1 4 35.024 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2a_1 1 8.758 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2a1_1 2 12.512 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2bb2a1_1 1 8.758 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2ba_1 2 20.049 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__o2ba_1 3 12.512 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__or3_1 1 6.256 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__or4_1 1 7.507 sky130_fd_sc_hd_tt_025C_lv88
sky130_fd_sc_hd__xnor2_1 1 8.758 sky130_fd_sc_hd_tt_025C_lv88

total 115 1133.587

```

| Type | Instances | Area | Area % |
|--------------|------------|-----------------|--------------|
| sequential | 21 | 529.258 | 46.7 |
| inverter | 11 | 41.290 | 3.6 |
| buffer | 1 | 3.754 | 0.3 |
| logic | 82 | 559.286 | 49.3 |
| total | 115 | 1133.587 | 100.0 |

Highest frequency of the design: 0.8 Ghz. (Violated at 0.9 Ghz)

```

Beginning report datapath command
Warning : The filename, column and line number information will not be available
          in the report. [RP1_DP-100]
      : The attribute for getting HDL filename and line number is not set.
      : You must set the 'hdl_track_filename_row_col' attribute to 'true' (before
        elaborate) to enable filename, column, and line number tracking in the datapath
        report.
WARNING: This version of the tool is 3474 days old.
genus@design:synth.wrapper> exit
Normal exit.
[admin@centos7 shared_ALU]$ make report
with Frequency at:
set FREQ_GHz 0.9
Path 1: VIOLATED (-32 ps) Setup Check with Pin ALU0/result_o_reg[3]/CLK->D
Path 2: VIOLATED (-28 ps) Setup Check with Pin ALU0/result_o_reg[1]/CLK->D
Path 3: VIOLATED (-27 ps) Setup Check with Pin ALU0/result_o_reg[2]/CLK->D
Path 4: VIOLATED (-13 ps) Setup Check with Pin ALU0/result_o_reg[0]/CLK->D
Path 5: VIOLATED (-12 ps) Setup Check with Pin ALU0/carry_o_reg/CLK->D
Path 6: MET (220 ps) Late External Delay Assertion at pin carry
Path 7: MET (220 ps) Late External Delay Assertion at pin result[0]
Path 8: MET (220 ps) Late External Delay Assertion at pin result[1]
Path 9: MET (220 ps) Late External Delay Assertion at pin result[2]
Path 10: MET (220 ps) Late External Delay Assertion at pin result[3]
[admin@centos7 shared_ALU]$ 
```

-Algorithm of arithmetic compute unit architecture used in the design:

