LABORATORY 5

MEMORY CIRCUIT DESIGN AND CHARACTERIZATION

OBJECTIVES

No.	Objectives	Requirements
1	Characterize the operation of SRAM – Static Random Access Memory.	▪ Simulate Read and Write operations. ▪ Apply Sense Amplifier to speed up the Read cycle. ▪ Simulate an array of SRAM sized 8 × 8.
2	Characterize the operation of TCAM – Ternary Content Addressable Memory.	▪ Simulate Writing and Compare operations. ▪ Simulate an array of TCAM sized 8 × 8.

EXPERIMENT 1

Objective: Known a specific structure of volatile memory (RAM) – SRAM 6-transistor.

Requirements:

- Simulate Read and Write operations.
- Apply Sense Amplifier to speed up the Read cycle.
- Simulate an array of SRAM sized 8 × 8.

Instructions:

- RAM (Random Access Memory) is accessed with an address and has a latency independent of the address. This is also known as volatile memory which retains its data as long as power is applied.
- Like sequencing elements, the memory cells used in volatile memories can further be divided into static structures and dynamic structures. Static cells use some form of feedback to maintain their state, while dynamic cells use charge stored on a floating capacitor through an access transistor. Charge will leak away through the access transistor even while the transistor is OFF, so dynamic cells must be periodically read and rewritten to refresh their state. Static RAMs (SRAMs) are faster and less troublesome, but require more area per bit than their dynamic counterparts (DRAMs).
- **Figure 1** above shows a standard 6-transistor SRAM. The 6T SRAM cell contains a pair of weak cross-coupled inverters holding the state and a pair of access transistors to read or write the state. A SRAM cell have two common modes: Writing mode and Reading mode. The convention is that the value of the SRAM cell will be written and read at the BL pin. The BLX pin will be used as an inverse reference value to the BL pin.

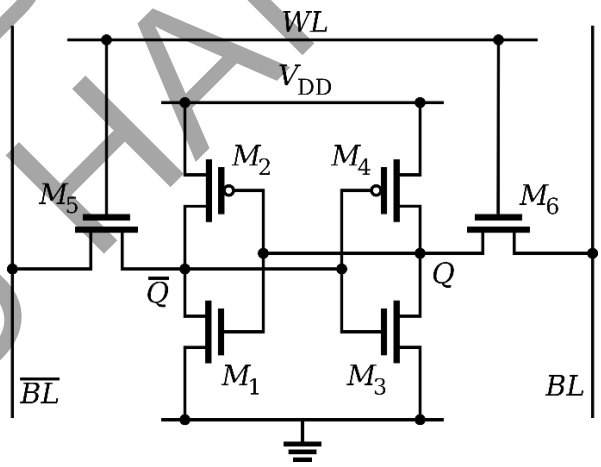

Figure 1 6T SRAM cell.

- In writing mode, the pin BL and $\overline{BL}$ (or BLX) have two opposite logic values, when WL=0, the 2 NMOS M5 and M6 are off, nothing happens to the cell. When WL=1, 2 NMOS M5 and M6 are active and the value at BL pin is stored into the cell. When we change the BL value, when WL changes to 1, the new value of BL will replace the old value inside the SRAM and be stored into the cell. When WL=1, the BL

value is stored at Q. When WL=0, the value of BL still remains at Q. When WL=1 again for new cycle, Q changes according to the value of BL pin at that time.

- In reading mode, after the cell has stored a certain value, we read that value to BL pin by using the process of charging capacitors connected to nets BL and ¯BL and to find
- the value stored in the two Q and $\overline{Q}$ points. The capacitors are charged from an external charging circuit. When the capacitor charging process is completed, the BL and BLX pins have logic level 1. At that time, the WL pin is changed to level 1, causing the 2 NMOS connected to WL to be activated. Then the value in SRAM will be read to the BL and BLX pins. If the cell has the value 1, the BL pin will remain at a logic level of 1 and the charge at the BLX pin will be completely discharged to GND after the read process ends, the value at the BLX pin is 0. Finally, the value of the SRAM cell is read out correctly at the BL pin.

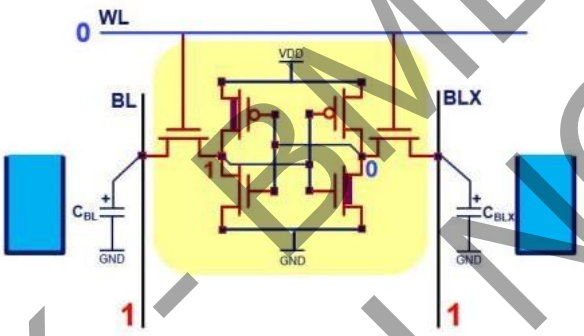

Figure 2 The SRAM cell in reading mode.

- Due to large BL/BLX capacitance, if you wait until BL or BLX discharges completely to read the data out, reading time is very long. To solve this problem, sense amplifier is used to reduce reading time (i.e. speed up the speed of memory). Sense amplifier operation can be showed in the attached documents or other references.

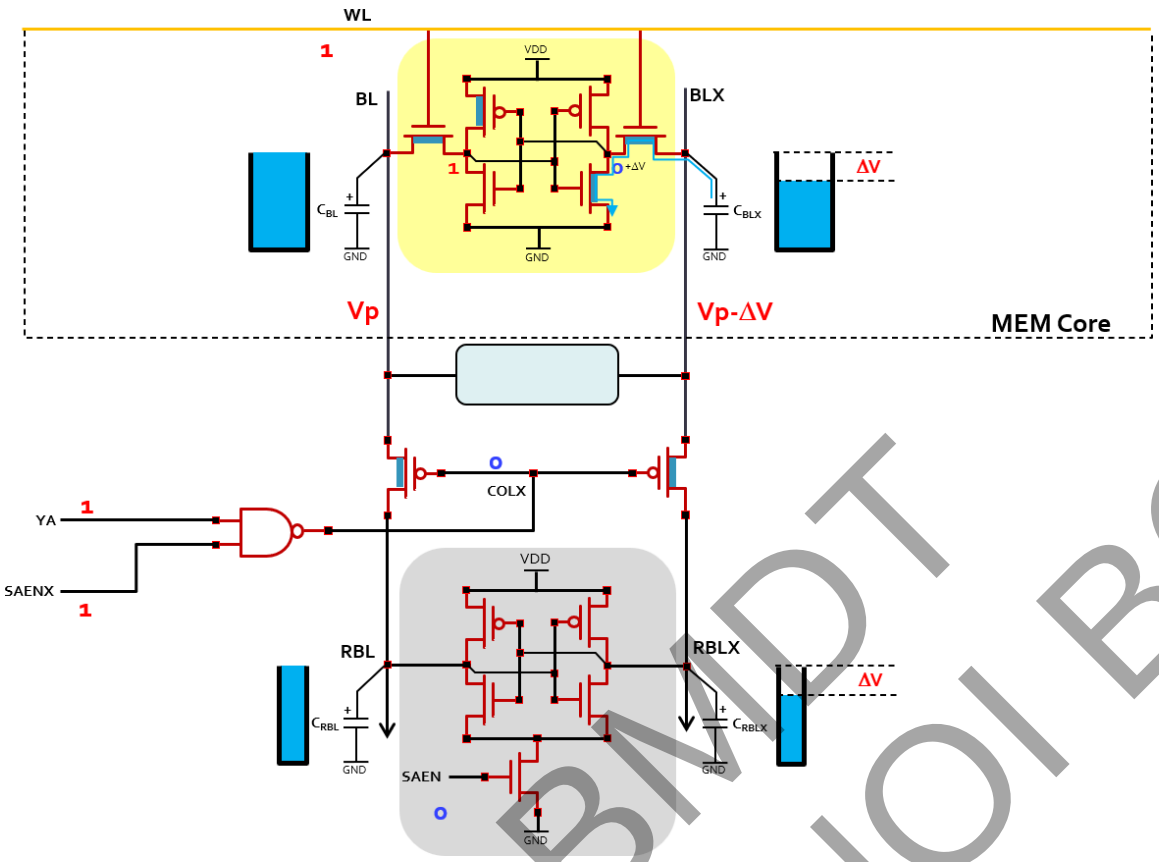

Figure 3 6T SRAM in reading operation with Sense Amplifier.

Check: Students must show in their report these results.

- Simulate the write and read process of a 6T SRAM cell, and measure its write and read time. Show a situation that 6T SRAM reads wrong data, explain why it reads wrong data?
- After measuring the read and write time of SRAM 6T, then use a sense amplifier to improve the read time. Compare the difference in the two cases of using and not using a sense amplifier, and give your comments and explanations.
- Show the simulation of the write and read process of one 6T SRAM array with size is 8x8. Describe the process of writing data into the SRAM array and get the data out, assuming each row uses a common WL line, each column uses a common BL line and a BLX line. Note: The data value for this requirement is optional but friendly remind that not use the special case like all "0" or all "1" in one row/column.

EXPERIMENT 2

Objective: Known a specific structure of CAM (Content Addressable Memory).

Requirements:

- Simulate Writing and Compare operations.
- Simulate an array of TCAM sized 8×8.

Instructions:

- TCAM (ternary content-addressable memory) is a specialized type of high-speed memory that searches its entire contents in a single clock cycle. The term "ternary" refers to the memory's ability to store and query data using three different inputs: 0, 1 and X. TCAM can perform one search each clock cycle. This is much faster than searching traditional RAM, which requires many clock cycles to query and check each memory location. To illustrate the power of TCAM for searching compared with traditional RAM, imagine you were looking for a specific sentence in a book. Searching in traditional RAM would be like looking through each page one at a time to find the sentence. CAM would be a book with an index or concordance that you could check to tell you exactly where in the book a certain word is used.
- However, CAM and TCAM do have some disadvantages. These memory cells require additional transistors to support the search feature. This makes it more expensive and less dense compared with traditional RAM. Each memory cell needs to be active on every cycle to perform the search, so it requires more power and produces additional heat. A simple TCAM cell has the structure shown in **Figure 4**.

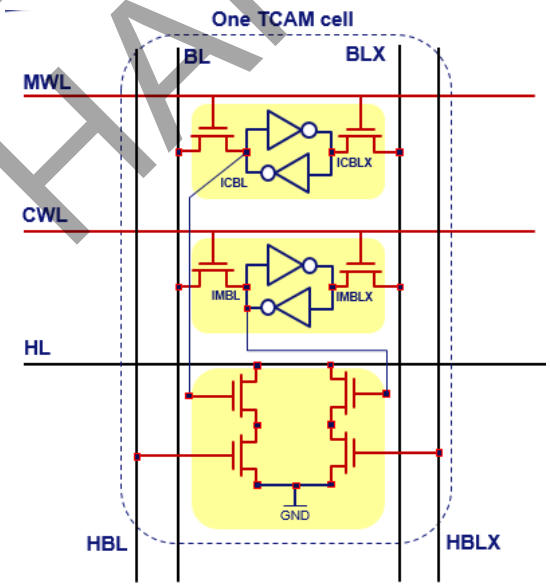

Figure 4 A TCAM cell.

- The structure of a TCAM cell can consists of 3 parts: Mask cell, Core cell and Compare circuit. Mask cell and Core cell have the same structure as SRAM cell: 2 NOT gates are connected one after another to form a bi-stable circuit, used to store data in one cell, and 2 pass-gates. transistors, used to connect BL and BLX pins to cells. Compare is made from 4 NMOS, the connection as shown above is controlled by pins HBL, HBLX, ICBL, IMBL connected from pin HL to GND. The HL pin is attached to a PMOS used for charging, controlled by the Pre-charge signal. TCAM have two common modes are writing mode and comparison mode.
- In writing mode, TCAM cell data will be written to the mask cell and core cell. The convention is that the value of TCAM will be written to the core cell, and the reverse reference value will be written to the mask cell. Because the mask cell and core cell are structured like a SRAM cell, the operation of the writing function is similar.
- in comparison mode, when data has been written to the core cell and mask cell. First, reset the signal at the Pre-charge pin to "0" to charge the HL pin (set the signal level to 1). After a certain time, set the signal at the Pre-charge pin to "1" to stop the charging process. Then, transmit the signal to be compared to pin HBL and the signal with inverted logic level to HBLX. If the value to be compared is the same as the value in the core cell, the comparator circuit does not create a path to discharge to GND, so logic level at pin HL is maintained as "1", also known as MATCH state. If the value to be compared is different from the value in the core cell, the comparator circuit creates a path to discharge to GND, so the logic level at the HL pin changes to "0", also known as the MISS state. In some special cases, it is possible to set the value for the core cell and mask cell to the same "1" or "0". If the core cell and mask cell both store the value "0", that TCAM memory cell always has the ALWAYS MATCH state. On the contrary, if the core cell and mask cell both store the value "1", that TCAM memory cell will always have the ALWAYS MISS state.
- Due to connecting many cells, the parasitic capacitor on the ML line is quite large, leading to a long discharge time. Then, to speed up the comparison process, we use the MLSA (Match Line Sense Amplifier) circuit.
- Finally, all signals from each row will go to the encoder to determine the exact address of the row that matches the comparison data.

Check:

- Simulate Writing and Compare operation of a TCAM cell. In comparison mode, simulate all 4 cases MATCH, ALWAYS MATCH, MISS, ALWAYS MISS of TCAM cell.

- Simulate an array of TCAM sized 8 × 8 in writing and comparison. Describe the process of writing data into the TCAM array and compare with the search data, assuming each row uses a common HL line, each column uses a common BL, BLX, HBL, HBLX lines. Note: The data value for this requirement is optional but friendly remind that not use the special case like all "0" or all "1" in one row/column.
- Bonus: If you can design additional MLSA and encoder, you will receive additional points for final report.

ACKNOWLEDGEMENTS

This laboratory has been developed and refined through the contributions of numerous individuals over the years. It was originally designed for the *EE3117 Digital IC Design* course at the University of Technology – VNU, HCM by *Mr. Nguyen Trung Hieu* (2015) and *Mr. Duong Quang Ho* (2018). Subsequent revisions and enhancements have been implemented for the EE3117 Digital IC Design course under the guidance of Dr. Linh Tran, with additional contributions from Doanh Bui, Tan-Khai Pham, and Phuc T. Nguyen-Phan.

Versions of this lab have been used in the following courses:

- EE3117 Digital IC Design (2023 – present) – the University of Technology – VNU, HCM.
- EE5154 Advanced Digital IC Design (2024 – present) – the University of Technology – VNU, HCM.