

# Introduction to EE3117 Laboratory

Created and edited by Phuc T. Nguyen-Phan







- 1. Meet Your Teaching Assistants
- 2. Lab Schedule
- 3. Graded Work







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## **Meet Your Teaching Assistants**





**Doanh BUI** 

Quest Global Design Vietnam Saturday: 9:00 am – 4:00 pm

203B3, Ly Thuong Kiet Campus

blqdoanh.sdh21@hcmut.edu.vn



Tan-Khai PHAM

Faraday Technology Vietnam

Saturday: 9:00 am – 4:00 pm 203B3, Ly Thuong Kiet Campus

hanspham.1970s@gmail.com



Phuc T. NGUYEN-PHAN

N/A

Wed&Thurs: 9:00 am – 4:00 pm 203B3, Ly Thuong Kiet Campus

nptphuc.sdh232@hcmut.edu.vn







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## Lab Schedule







- Laboratory 0: Introduction to VLSI Design Flow
- Laboratory 1: MOS Transistor Characterization
- Laboratory 2: Digital Logic Components
- Laboratory 3: Design of Combinational and Sequential Circuits
- Laboratory 4: Logic Synthesis
- Laboratory 5: Memory Circuit Design and Characterization







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### **Graded Work**



THÍ NGHIỆM THIẾT KẾ VI MẠCH SỐ (EE3117 & EE4521)																
Lớp	Nhóm	MSSV	Họ và tên SV	Email	Account name	Config file	Điểm thành phần									
							Lab <sub>1</sub>	Lab2	Lab3	Lab4	Lab5	Report	QA	Bonus	Pre-Final	Final
(dcds)	5	2013119 Lương Quý Hậu		hau.luongshowmesthb@hcmut.edu.vn	dcdso6	dcdso6/24	9	9	9	9	9	9	8	1	9.50	9.50
		2010251 Cao Văn Hiếu		Hieu.caoo110gl@hcmut.edu.vn			9	9	9	9	9	9	8	1	9.50	9.50
		2014390 Lưu Sinh Nhật Sư		su.luu2002@hcmut.edu.vn			9	9	9	9	9	9	8	1	9.50	9.50
	6	2012759 Đặng Phước Cường		cuong.dang2002@hcmut.edu.vn			9	9	9	9	8	8.8	8	0.75	9.15	9.00
		2015096	Trần Ngọc Vũ	vu.trantnvuo418@hcmut.edu.vn	dcds07	dcdso7/25	9	9	9	9	8	8.8	9.5	0.75	9.90	10.00
		2012778 Lê Công Danh da		danh.lemcr77@gmail.com			9	9	9	9	8	8.8	9.5	0.75	9.90	10.00
	7	2014110 Vũ Hồng Phi		phi.vu2437@hcmut.edu.vn			8	8	8	8	8.5	8.1	8	0.5	8.55	8.50
		2012950	Tiêu Tuấn Đạt	dat.tieutuan159@hcmut.edu.vn	dcdso8	dcdso8/26	8	8	8	8	8.5	8.1	8	0.5	8.55	8.50
		2012187	Nguyễn Thị Thủy tiên	tien.nguyen318@hcmut.edu.vn			8	8	8	8	8.5	8.1	8	0.5	8.55	8.50

- Your graded work will consist of:
  - 5 lab reports (50%)
  - QA session (50%)
  - Bonus (1 mark) [Topic: IC Design Flow]
  - Final = Rounding[(0.5 \* Report) + (0.5 \* QA) + Bonus]

## Additionally, ...

- Students will work in groups of 2–3 for this lab session.
  - "Your choice, your future!"
- Students must submit their reports via LMS within 2 weeks of each lab session.
  - Reports must be in .pdf format, according to the instructions on LMS.
- The QA session will be announced via email.
  - including the time and location.
- Any instance of cheating in the report will result in a zero grade.



## Enjoy and have fun!!!

Link: Virtual-Machine

Password: dhbkbmdt242