LABORATORY 1

MOS TRANSISTOR CHARACTERIZATION

OBJECTIVES

No.	Topics	Requirements
1	I-V characteristics of MOS transistors.	▪ Simulate the I_D *vs* V_{GS} and I_D *vs* V_{DS} characteristics of NMOS_VTG and PMOS_VTG transistors using FreePDK45.
2	Effects of varying VGS and device size.	▪ Simulate the I_D *vs* V_{GS} and I_D *vs* V_{DS} characteristics of NMOS_VTG and PMOS_VTG transistors using FreePDK45 and analyze the impact of these parameters.
3	Second-order effects (Body effect, Channel-length modulation).	▪ Simulate the I_D *vs* V_{GS} and I_D *vs* V_{DS} characteristics of NMOS_VTG and PMOS_VTG transistors using FreePDK45 and analyze the impact of these parameters. ▪ Measure, and analyze device characteristics: $\lambda, V_{Th0}, k_p,$ and γ.
4	Layout design for MOS transistors.	▪ Design the layout for a 120n/60n NMOS and a 50n/40n PMOS transistor. ▪ Verify the design by performing Design Rule Check (DRC) and ensuring Layout Versus Schematic (LVS) confirmation.

PREPARATIONs

- Students **must finish** laboratory 0.
- Summarize the operating regions of NMOS according to the following table (students do not need to submit before class):

Conditions		Equation current I_D of NMOS	The operating region of NMOS
$V_{GS} < V_{TH}$	V_{DS}		
$V_{GS} \geq V_{TH}$	$V_{DS} < V_{GS} - V_{TH}$		
$V_{GS} \geq V_{TH}$	$V_{DS} \geq V_{GS} - V_{TH}$		

EXPERIMENT 1

Objective: I-V characteristics of MOS transistors.

Requirements: Simulate the I_D *vs* V_{GS} and I_D *vs* V_{DS} characteristics of NMOS_VTG and PMOS_VTG transistors using FreePDK45.

Instructions: For example, design a testbench similar to **Figures 1** and **2** to characterize the devices, maintaining the default device dimensions (W/L = 90n/50n). Based on Lab 0, students should obtain results corresponding to the curves shown in **Figures 3** and **4**.

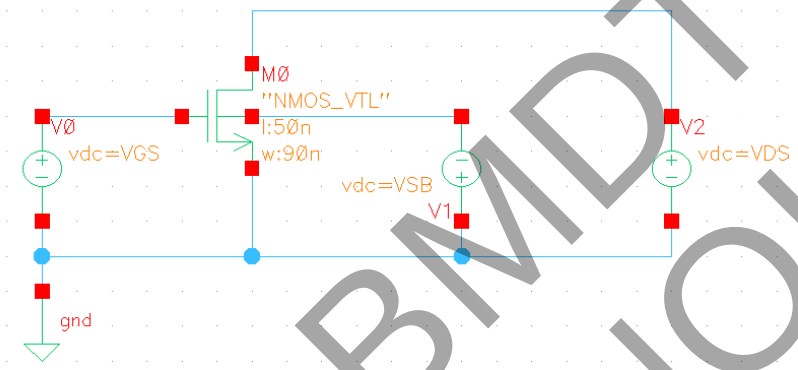

Figure 1 Test setup for the NMOS transistor.

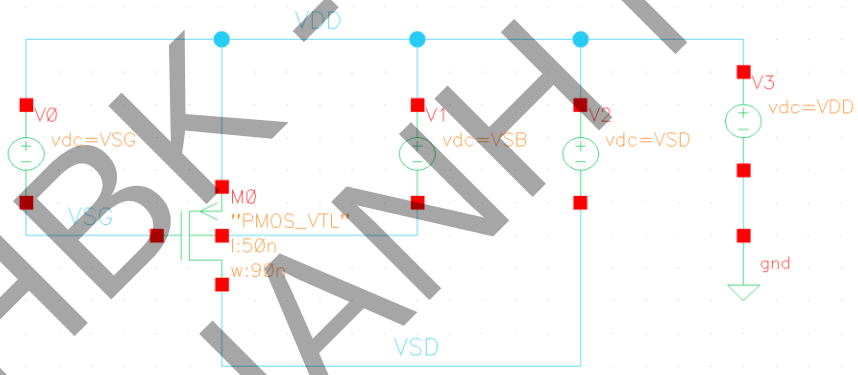

Figure 2 Test setup for PMOS transistor.

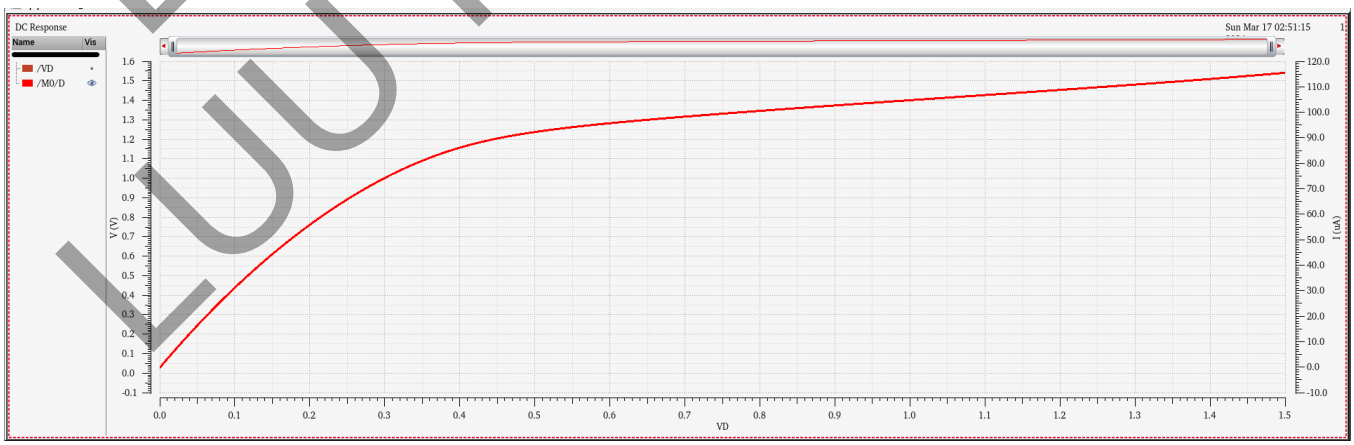

Figure 3 I_D *vs* V_{DS} of NMOS @ $V_{gs} = 1V$.

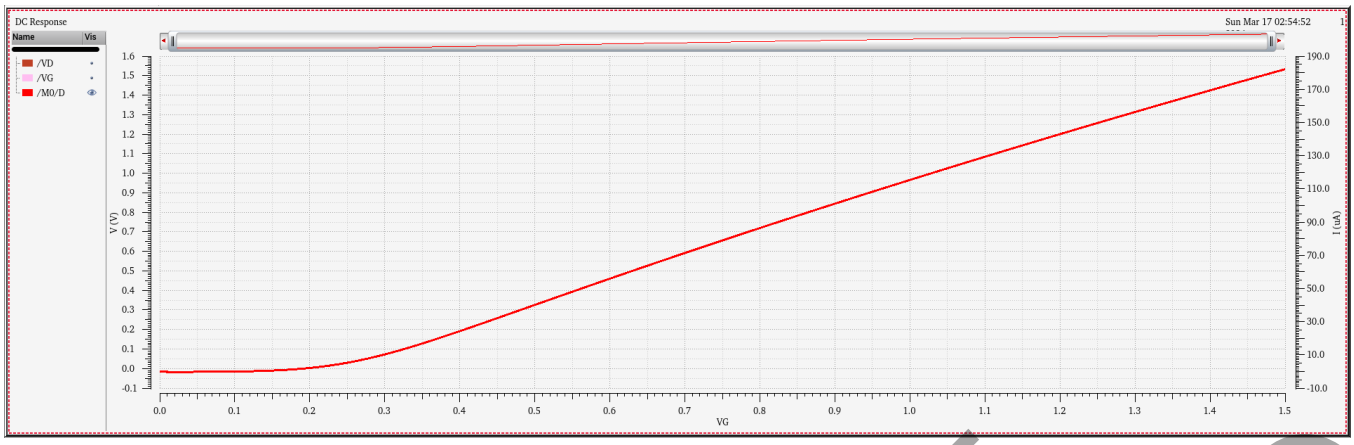

Figure 4 I_D *vs* V_{GS} of NMOS @ $V_{ds} = 1.5V$.

Check: Your report must include the results for NMOS_VTG and PMOS_VTG transistors. Additionally, provide a discussion on your simulation findings.

1. Simulate curves I_D *vs* V_{DS} @ $V_{GS} = 1V$, and sweeping variable $V_{DS} = [0,1.5]V$ step 10mV.
2. Simulate curves I_D *vs* V_{GS} @ $V_{ds} = 1.5V$, and sweeping variable $V_{gs} = [0,1.5]V$ step 10mV.

Questions:

1. Based on the I_D *vs* V_{GS} characteristics, please estimate the threshold voltage V_{GS} of the NMOS transistor.
2. Additionally, by analyzing the I_D *vs* V_{GS} characteristics, determine the conduction region of the NMOS transistor when V_{GS} exceeds V_{GS}. Specify whether the device operates in the linear (triode) region or the saturation region, and provide an explanation.
3. Based on **Figure 3**, qualitatively determine the operating regions of the NMOS transistor.
4. When the NMOS transistor is biased in the saturation region, does the drain current remain constant? Provide a theoretical explanation.
5. Propose methods to reduce the slope of the drain current when the NMOS operates in the saturation region.

EXPERIMENT 2

Objective: Effects of varying VGS and device size.

Requirements: Simulate the I_D *vs* V_{GS} and I_D *vs* V_{DS} characteristics of NMOS_VTG and PMOS_VTG transistors using FreePDK45 and analyze the impact of these parameters.

Instructions:

- Replace the default device size with variables, making the testbench parameterized. This means your testbench should include five parameters: `W`, `L`, `VGS`, `VDS`, and `VSB`, as shown in the figure below..

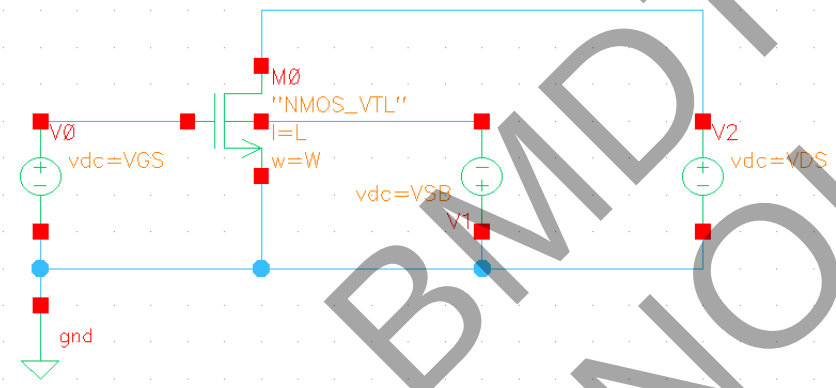

Figure 5 Testbench for experiment 2.

- In ADE-L, students open ***Parametric Analysis***[1] to sweep multiple variables:

Tool > Parametric Analysis > Run mode > Sweeps & Ranges

[1] **Parametric analysis** is used when two or more independent variables are present in a single function. Students can have the standard X-Y plot of I_D versus V_{DS} with a constant V_{GS}. But students need to plot the same X-Y plot multiple times for each of the discrete V_{GS} values. Students can refer to the settings and results in the figures below:

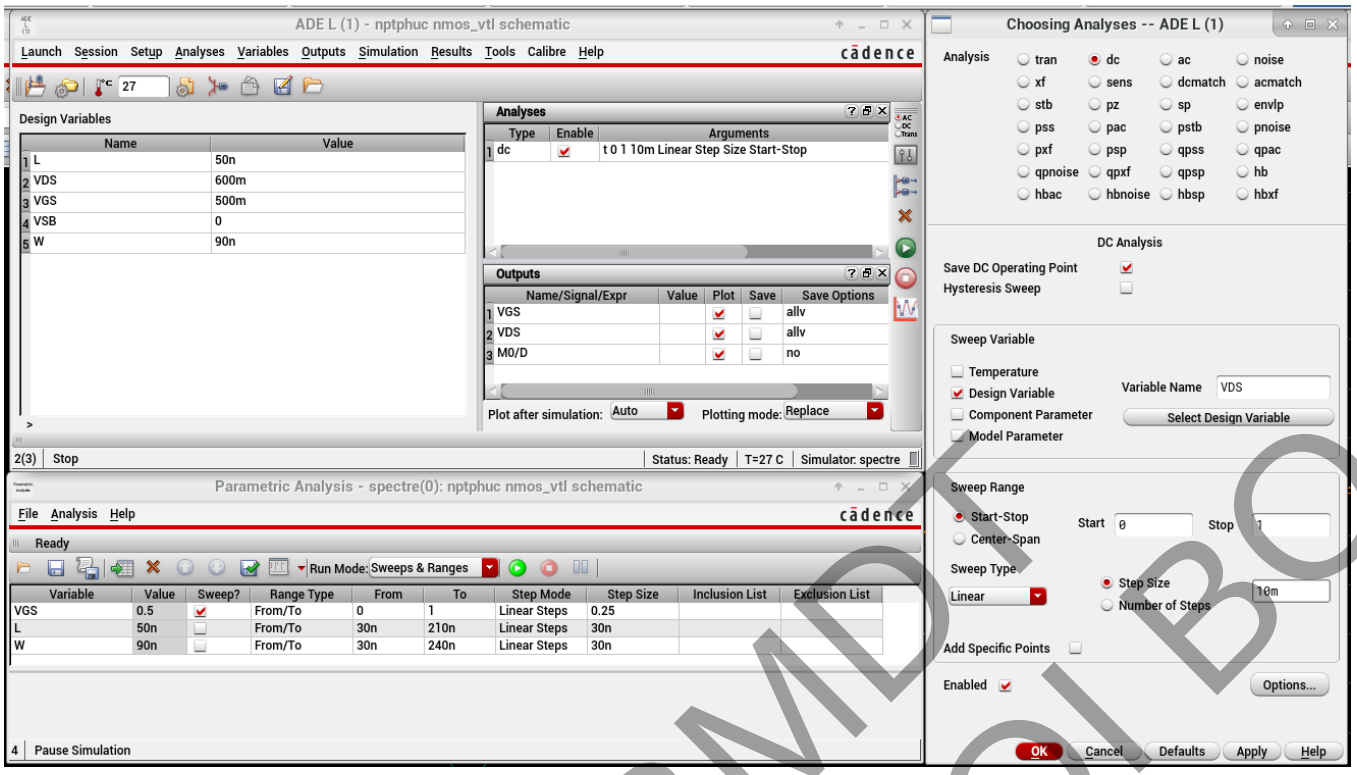

Figure 6 Setting parameters for characterizing I_D *vs* V_{DS} @ $V_{GS} = \{0, 0.25, 0.5, 0.75, 1.0\}$ V

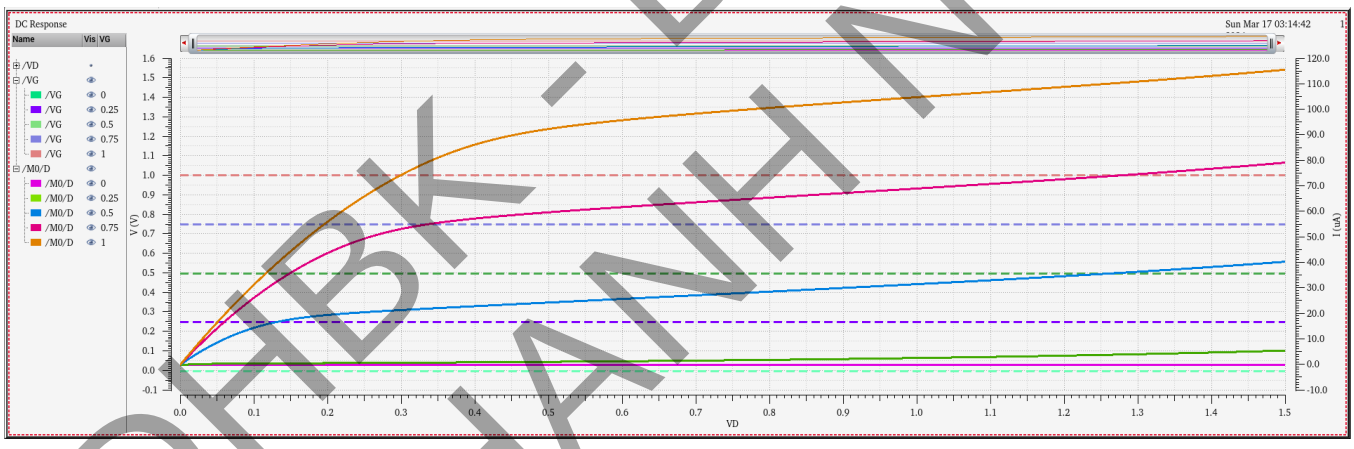

Figure 7 I_D *vs* V_{DS} @ $V_{gs} = [0,1]$ V step 0.25V.

Check: Your report must include these results. Additionally, provide a discussion on your simulation findings.

- Simulate curves I_D *vs* V_{GS} @ $V_{gs} = [0,1]$ V step 0.25V.
- Simulate curves I_D *vs* V_{DS} @ $W = [30,210]$ nm step 30nm.
- Simulate curves I_D *vs* V_{DS} @ $L = [30,240]$ nm step 30nm.

EXPERIMENT 3

Objective: Explore second-order effects (Body effect, Channel-length modulation).

Requirements:

- Simulate the I_D *vs* V_{GS} and I_D *vs* V_{DS} characteristics of NMOS_VTG and PMOS_VTG transistors using FreePDK45 and analyze the impact of these parameters.
- Measure, and analyze device characteristics: λ, V_{Th0}, k_p, and γ.

Reminds:

- The ideal I-V model neglects many effects that are important to a device. It is useful to have a qualitative understanding of second-order effects to predict their impact on circuit behavior and to be able to anticipate how devices will change in future process generations. Some effects are listed as follows:

No.	Second-order effect (Nonlinear I-V Effects)	
1	Mobility degradation and Velocity saturation	
2	Channel length modulation	
3	Threshold voltage effect	Body effect
		Drain-Induced Barrier Lowering
		Short Channel Effect
4	Leakage	Subthreshold Leakage
		Gate Leakage
		Junction Leakage
5	Temperature Dependence	
6	Geometry Dependence	

Table 1 Some second-order effects in MOS transistor.

In fact, body effect and channel length modulation are important when analyzing the small signal, and the expression determined I_D. Assemble the testbench circuit as shown in **Figure 5**.

- To characterize the MOS transistors so that hand calculations can be done in the future, simulations need to be done to measure $\boldsymbol{k_P, V_{Th0}, \lambda}$ **and** $\boldsymbol{\gamma}$. These parameters will be used in future labs, projects, and other assignments. This lab will be performing the calculation of the four parameters on two different device sizes for each of the two types of MOSFETs so that parameter variation may be

observed. The test setups for the NMOS are shown in **Figure 5**, which will produce the plots shown in **Figure 7** using parametric analysis.

- Using a curve I_D *vs* V_{DS} which each curve represents a different V_{GS} value. Any one of these curves can be used to calculate λ. Make sure that V_{bs} is 0V for this simulation. The formula for calculating λ given two points on the saturation portion of a single curve is:

$$\lambda = \frac{I_{D2} - I_{D1}}{I_{D1}V_{DS2} - I_{D2}V_{DS1}} \tag{1}$$

- V_{Th0} can also be obtained from **Figure 5**. Using the saturation portion of the two curves with equal V_{ds} then V_{Th0} can be calculated as:

$$V_{Th0} = \frac{V_{gs1} - V_{gs2}\sqrt{\frac{I_{ds1}}{I_{ds2}}}}{1 - \sqrt{\frac{I_{ds1}}{I_{ds2}}}} \tag{2}$$

➢ Knowing λ and V_{Th0}, k_P can easily be found from the equation for a MOS transistor drain current in the saturation region. A little algebra shows that k_P is:

$$k_p = \frac{2I_D}{\frac{W}{L}(V_{GS} - V_{Th0})^2(1 + \lambda V_{DS})} \tag{3}$$

➢ To obtain γ you must first give the transistor a non-zero V_{SB}. Next, calculate the new V_{Th} using the same procedure that you used to obtain V_{Th0} where $2\phi_F = 0.7$. γ is given as:

$$\gamma = \frac{V_{Th} - V_{Th0}}{\sqrt{|2\phi_F| + |V_{SB}|} - \sqrt{|2\phi_F|}} \tag{4}$$

Instructions:

➢ Sweep multiple variables in parallel using ADE-L: **Tool → Parametric Analysis → Run mode → Parametric Set**.

➢ Students can refer to the setting in Figure 6 drawing I_D *vs* V_{GS} @ $V_{DS} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\}\,V$ and sweeping $V_{GS} = [0, 1.5]\,V$ step 10mV.

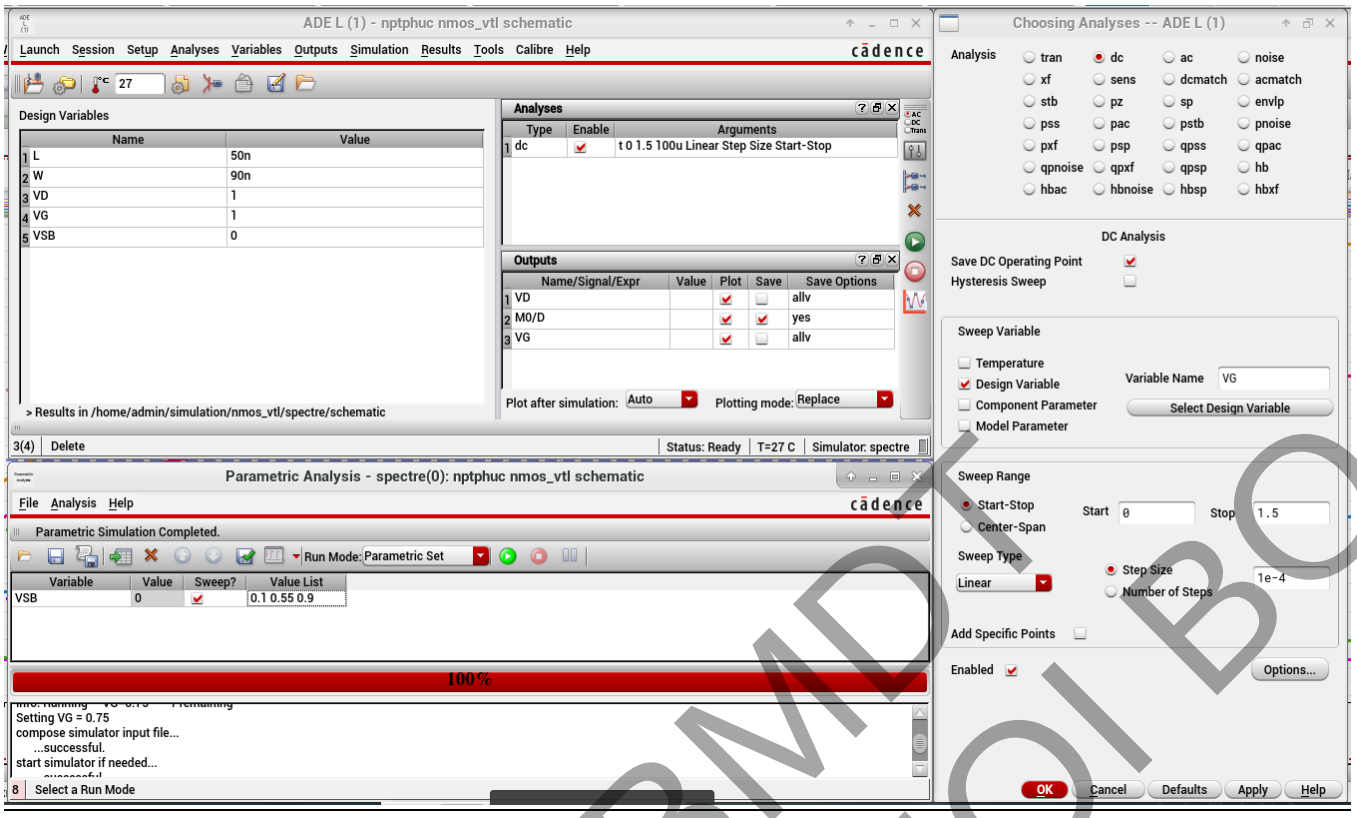

Figure 8 Setting for drawing $I_D\ vs\ V_{GS}\ @\ V_{DS} = 1V, V_{SB} = \{0.1,0.55,0.9\}\ V$ and sweeping $V_{GS} = [0,1.5]\ V$ step 10mV.

Check: Your report must show two results

- Draw curves $I_D\ vs\ V_{GS}\ @\ V_{DS} = 1V, V_{SB} = \{0.1,0.55,0.9\}\ V$, and sweeping $V_{gs} = [0,1]\ V$ with step 10mV.
- Draw curves $I_D\ vs\ V_{DS}\ @\ V_{GS} = 1V, V_{SB} = \{0.1,0.55,0.9\}\ V$ and sweeping $V_{DS} = [0,1]\ V$ with step 10mV.
- Extract the four electrical parameters (k_P, V_{Th0}, λ and γ) for NMOS_VTG, and PMOS_VTG from tool.

EXPERIMENT 4

Objective: Layout design for MOS transistors.

Requirements:

- Design the layout for a 120n/60n NMOS and a 50n/40n PMOS transistor.
- Verify the design by performing Design Rule Check (DRC) and ensuring Layout Versus Schematic (LVS) confirmation.

Instructions:

- In this experiment, students will explore the construction of transistors. A thorough understanding of the physical implementation of circuits is essential for designers, as it significantly influences performance, power consumption, and cost. This concept is best understood by examining both the top and cross-sectional views of a wafer in a simplified manufacturing process:

1. The **top view** represents the layout as seen from above the wafer.
2. The **cross-sectional view** is obtained by slicing the wafer through the middle of a transistor and observing it from the side.

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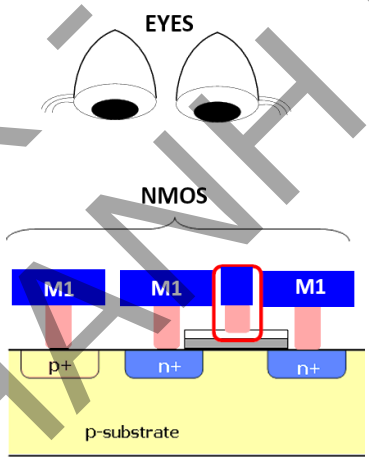

Figure 9 Cross section of an NMOS transistor.

- Students first examine the cross-section of a complete NMOS transistor, then analyze its top view and identify the set of masks used in the fabrication process.
- Following the layout guidelines from Lab 0, this lab focuses only on the layout implementation steps:

1. Add **n-active** (n-islands).
2. Add Poly (**PO**) for the gate.
3. Make drain, source, and bulk connections (contacts).
4. Create **pwell**.

5. Overlap the two active regions with the correct types of **implants**.
6. Create contacts for four terminals (**metal1**).

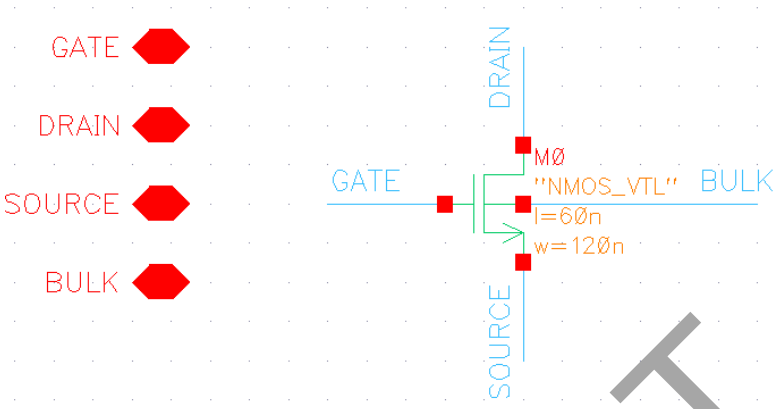

Figure 10 NMOS_VTL schematic.

Check: Your report must include these results. Additionally, provide a discussion and explanation for any modifications or optimizations you have implemented.

➢ Design the layout for an NMOS_VTL (120n/60n) and a PMOS_VTL (50n/40n), ensuring compliance with Design Rule Checks (DRC). Verify the corresponding schematic through Layout Versus Schematic (LVS) confirmation.

ACKNOWLEDGEMENTS

This laboratory has been developed and refined through the contributions of numerous individuals over the years. It was originally designed for the *EE3121 Analog and Mixed-Signal IC Design* course at the University of Technology – VNU, HCM by *Do Huy Khang* (2018) and for the *EE3165 IC Design* course by *Nguyen Thanh Trung* (2024). Subsequent revisions and enhancements have been implemented for the EE3117 Digital IC Design course under the guidance of Dr. Linh Tran, with additional contributions from Doanh Bui, Tan-Khai Pham, and Phuc T. Nguyen-Phan.

Versions of this lab have been used in the following courses:

- EE3117 Digital IC Design (2023 – present) – the University of Technology – VNU, HCM.
- EE5154 Advanced Digital IC Design (2024 – present) – the University of Technology – VNU, HCM.
- EE3165 IC Design (2025 – present) – the University of Technology – VNU, HCM.
- EE3425 Introduction to VLSI System Design (2025 – present) – the University of Technology – VNU, HCM.
- EE5243 Advanced IC Design (2024 – present) – the University of Technology – VNU, HCM.