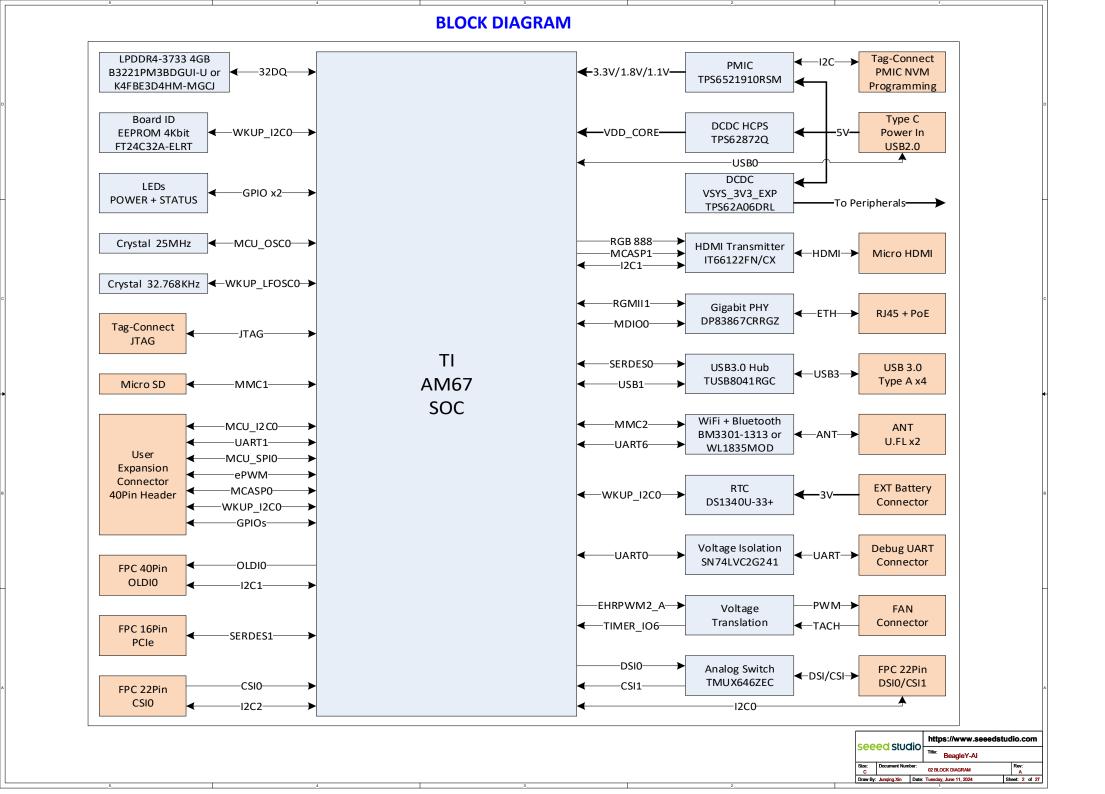
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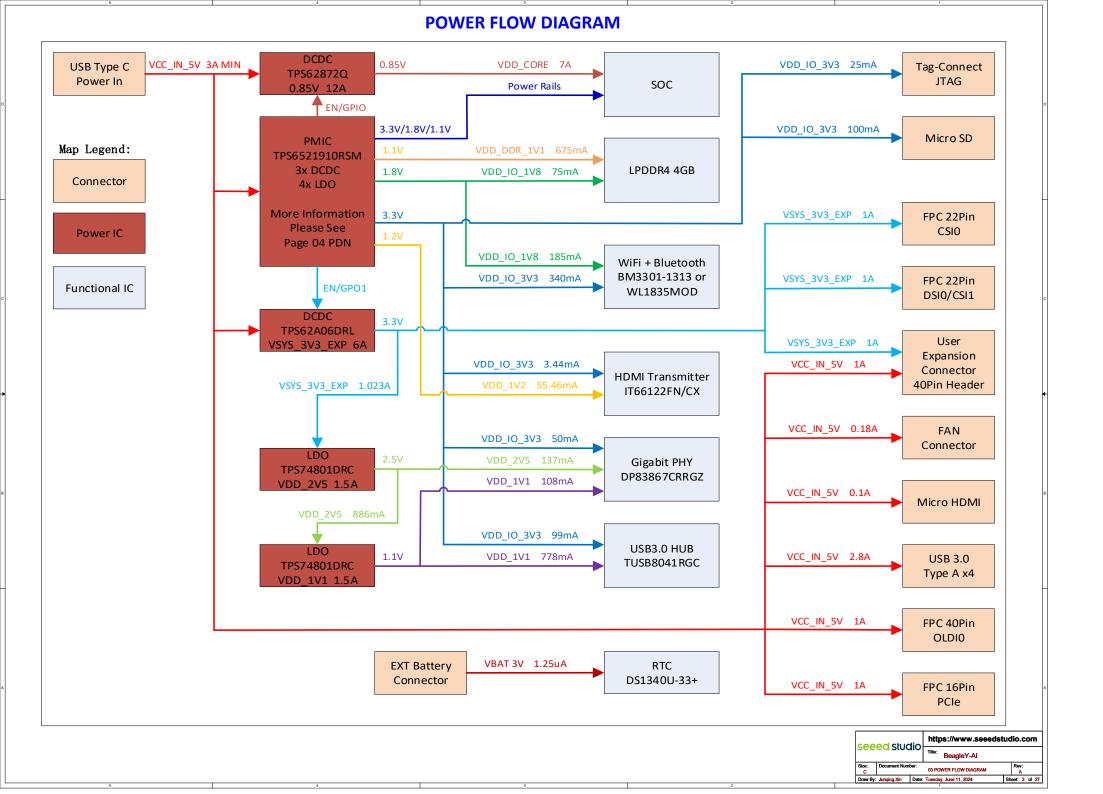
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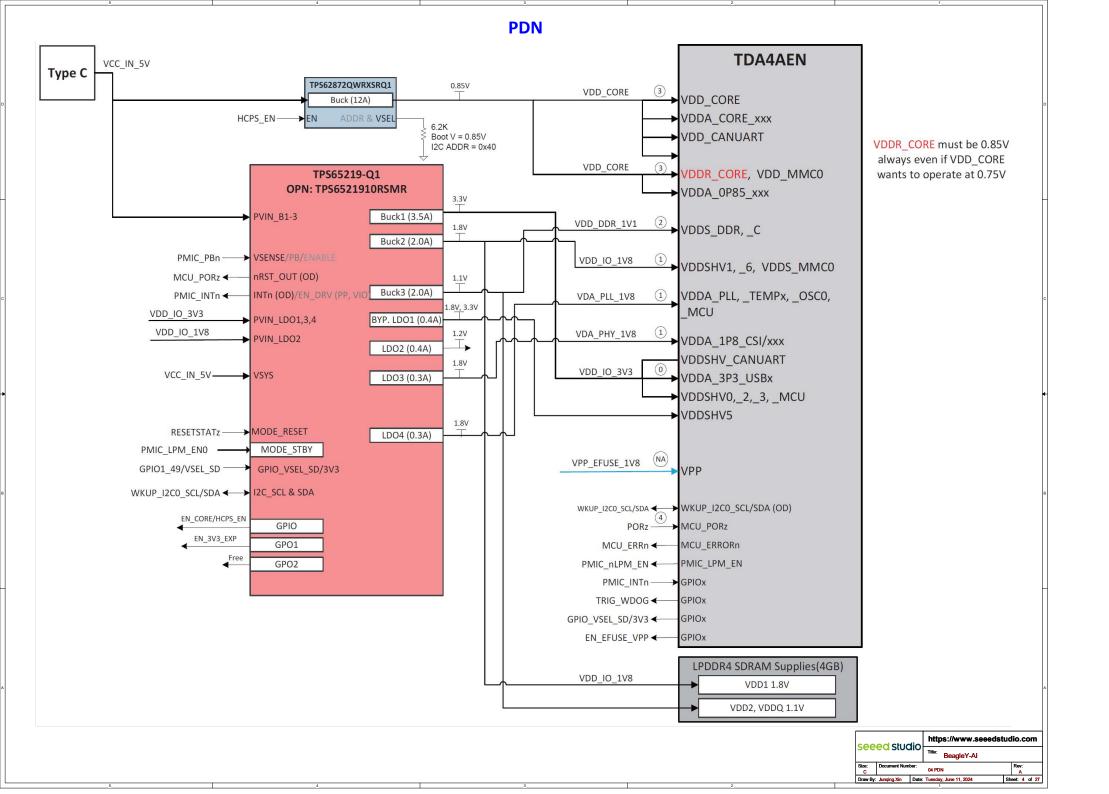
# **REVISION HISTORY**

VER#	DATE	REVISION	DESCRIPTION OF CHANGES	AUTHOR
Rev A	26 Apr 2024	BeagleY-AI_SCH_Rev A_240426	Initial Release	Junqing.Xin

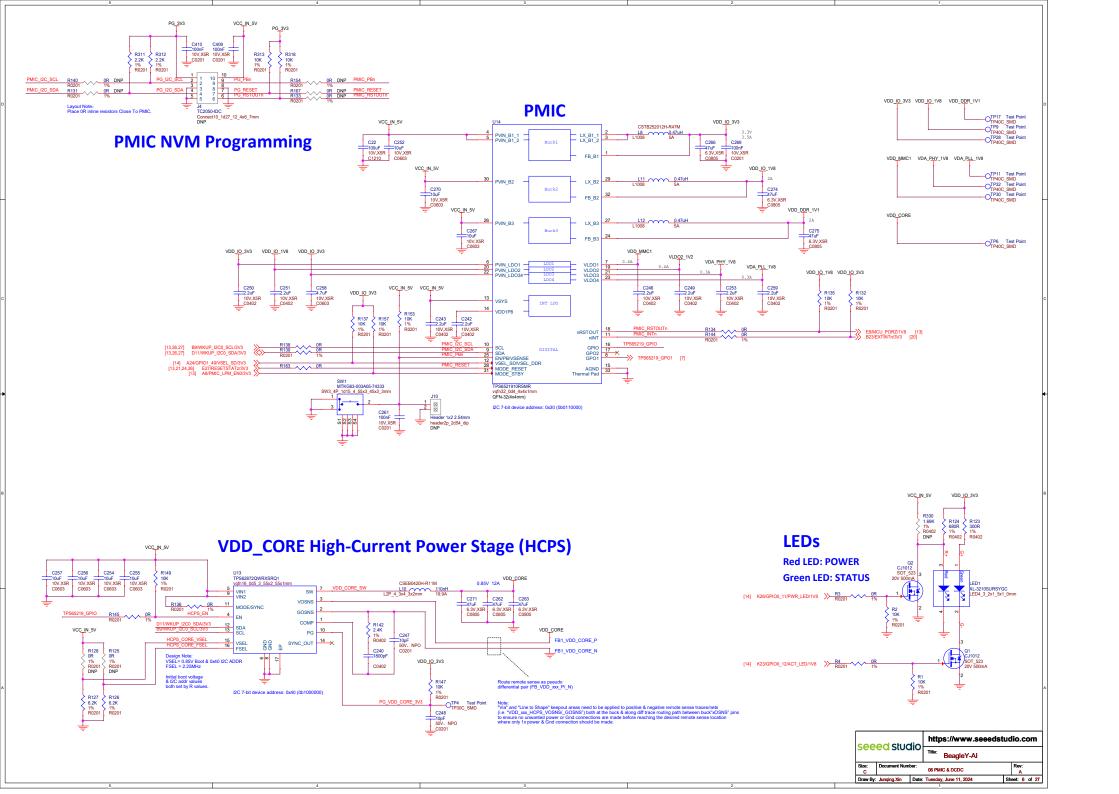




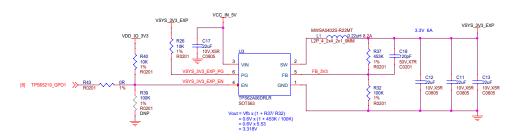


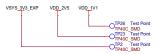


#### **IIC TREE** VDD\_IO\_3V3 2.2K WKUP\_I2CO\_SCL WKUP\_I2C0 WKUP\_I2CO\_SDA PMIC DCDC HCPS Board ID EEPROM EXT RTC **User Expansion** TPS6521910RSM DS1340U-33+ TPS62872Q FT24C32A-ELRT Connector (0x30)(0x40)(0x50)(0x68) 40Pin Header VDD\_IO\_3V3 Map Legend: 2.2K IC I2CO\_SCL FPC 22Pin 12C0 I2CO\_SDA Connector CSI1/DSI0 Connector VDD\_IO\_3V3 ΤI **HDMI Transmitter** AM67A IT66122FN/CX 2.2K 2.2K SOC (0x98) I2C1\_SCL 12C1\_SCL/1V8 Level Translator FPC 40Pin I2C1 I2C1\_SDA PCA9306DQE 12C1 SDA/1V8 Connector Or TCA9801DGK OLDI VDD\_IO\_3V3 2.2K 2.2K I2C2\_SCL FPC 22Pin I2C2 I2C2\_SDA Connector CSI0 VDD\_IO\_3V3 2.2K MCU\_I2CO\_SCL User Expansion MCU\_I2C0 MCU\_I2CO\_SDA Connector 40Pin Header https://www.seeedstudio.com seeed studio Title: BeagleY-Al Size: Document Number: 05 IIC TREE Draw By: Junqing Xin Date: Tuesday, June 11, 2024



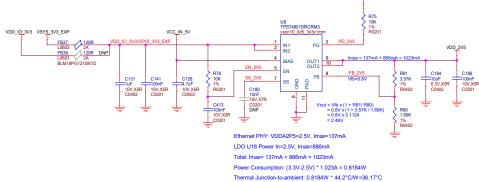
# VSYS\_3V3\_EXP For LDO & CSI & DSI & RPi 40Pin (Total: 4A)



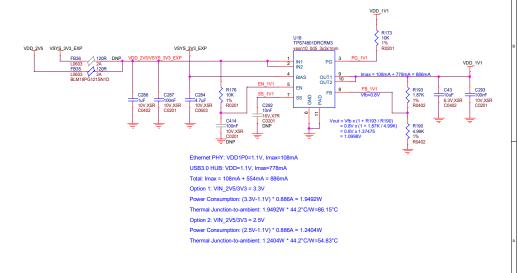


# **ETHERNET POWER**

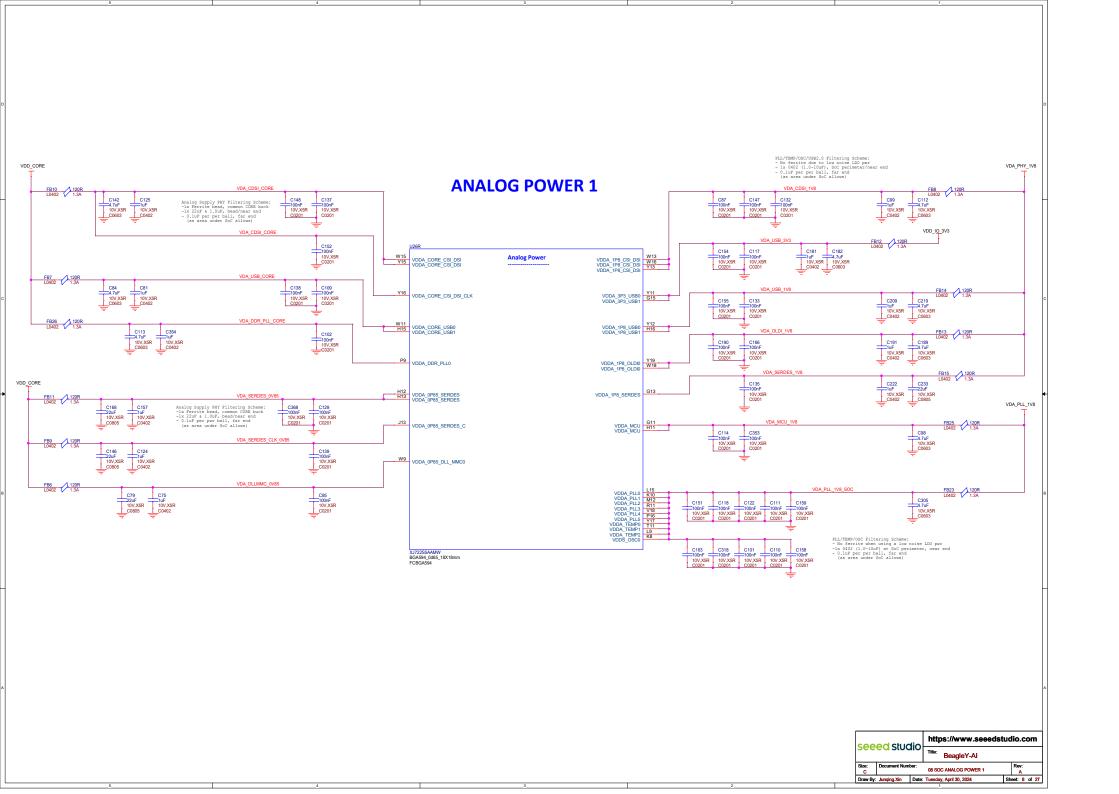
3.3V to 2.5V LDO

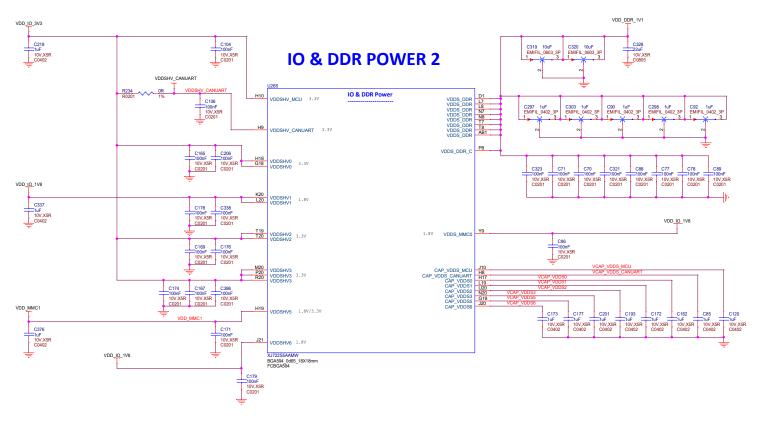


# USB3.0 HUB & ETHERNET POWER 3.3V/2.5V to 1.1V LDO



| https://www.seeedstudio.com | Title: BeagleY-Al | Size: | Document Number: or 793\_EXP DCDC, LDOs | Rev. | C | Draw By: Junying Xin | Date: Toreday, Juny 11, 2024 | Sheet: 7 of 27





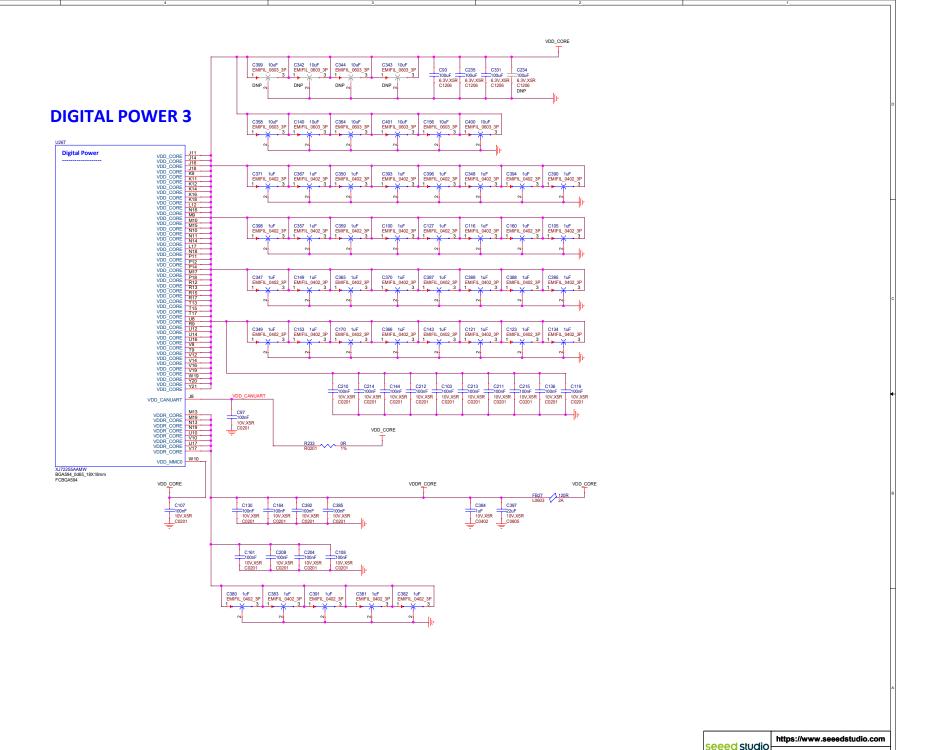
#### Note:

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A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Populate" (DNP) components if Power Integrity (PI) simulation results for a particular power rail on this PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (2t).

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see	eu sioc	JIO	Title: BeagleY-Al						
Size: C	Document Num	ber:	09 SOC IO & DDR POWER 2		Rev:				
Draw By:	Junqing.Xin	Date:	Tuesday, April 30, 2024	Sh	neet: 9	of 27			



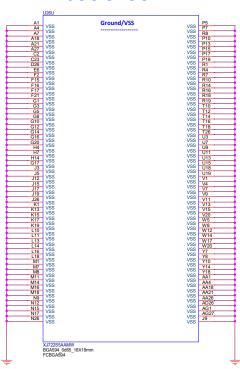
Title: BeagleY-AI

10 SOC DIGITAL POWER 3

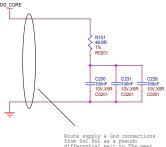
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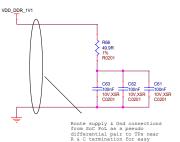
Draw By: Junqing.Xin Date: Tuesday, April 30, 2024

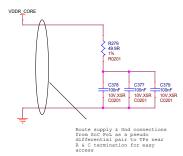
#### **SOC GROUND**



# **SoC Supply Noise Kelvin Sensing**

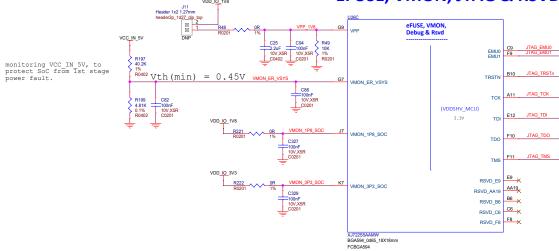




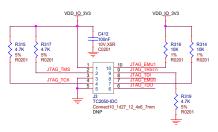




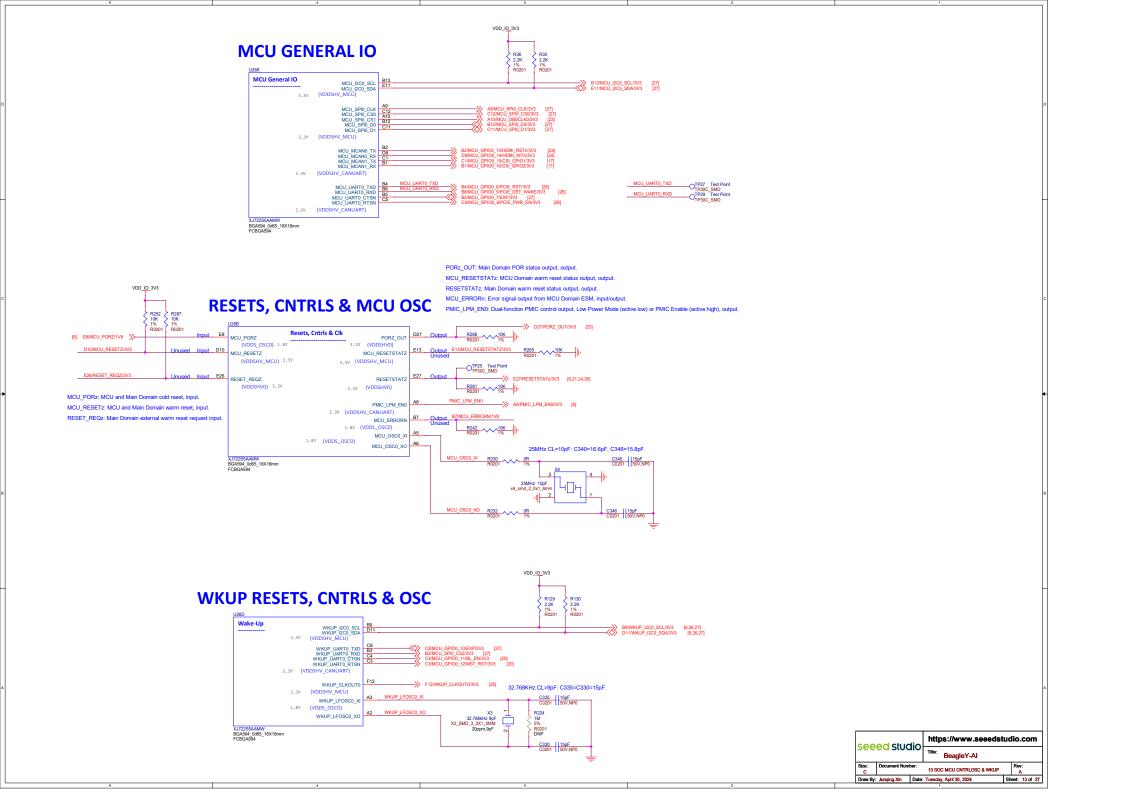
# **EFUSE, VMON, JTAG & RSVD**



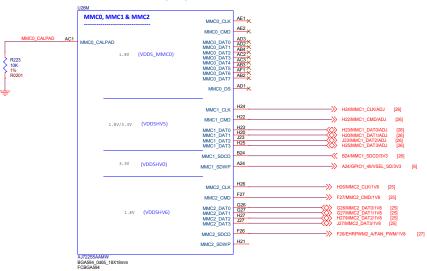
# **Tag-Connect**



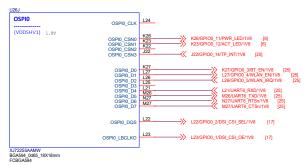


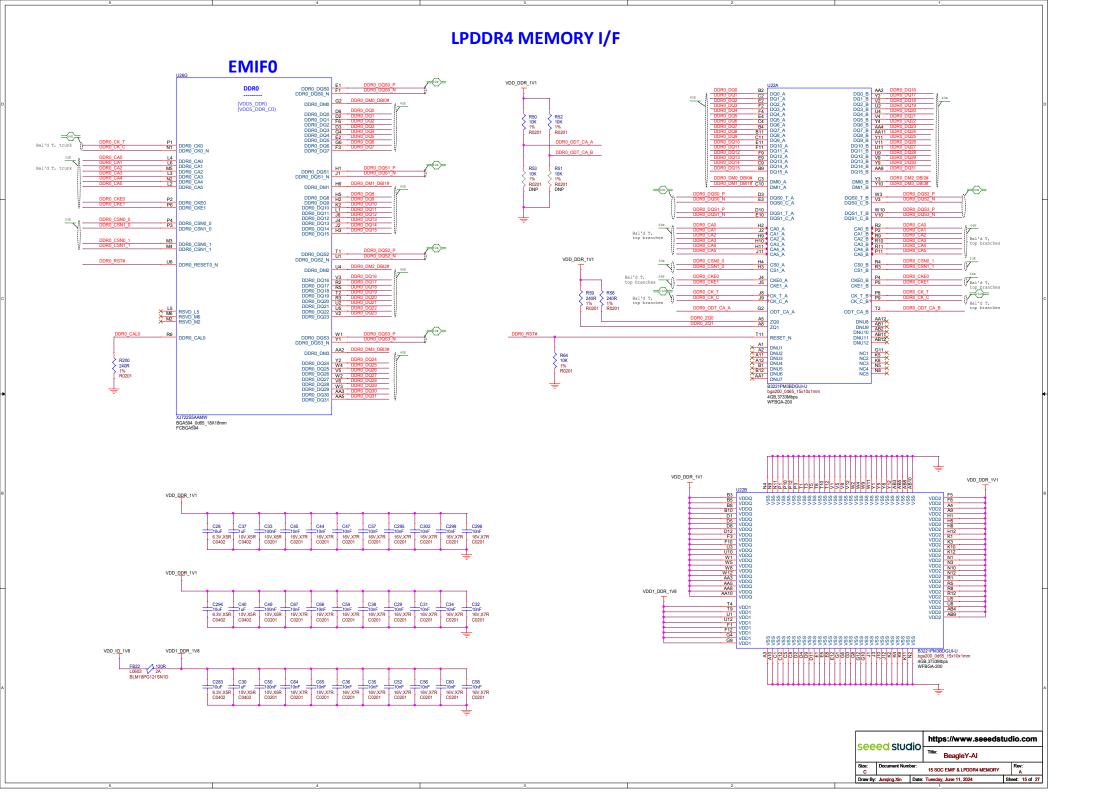


# MMC 0, 1, 2

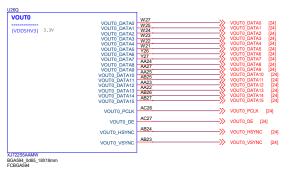


#### **OSPI**





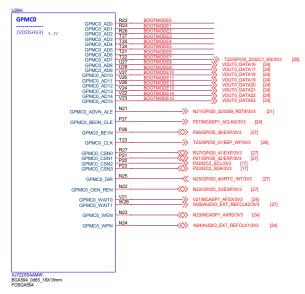






VDD\_IO\_3V3

#### **GPMC**

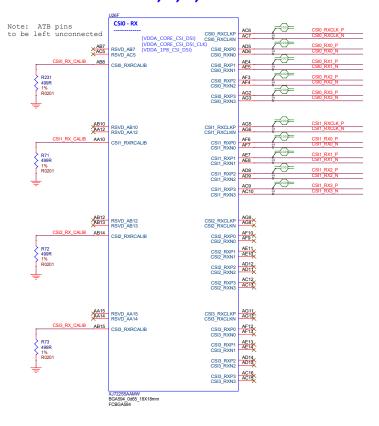


R84 10K 1% R0201	R89 10K > 1% > R0201	R304 > 10K > 1% > R0201 DNP	R91 > 10K > 1% > R0201 DNP	R97 > 10K > 1% > R0201 DNP	R98 10K > 1% > R0201 DNP	R308 10K 1% R0201	R309 > 10K > 1% > R0201	R85 10K 1% R0201 DNP	R88 10K 1% R0201	R92 10K > 1% > R0201 DNP	R94 10K 1% R0201 DNP	R90 10K > 1% > R0201	R95 > 10K > 1% > R0201 DNP	R96 10K 1% R0201 DNP	R8S 10K
															<u>BOOTMODE(1</u>   BOOTMODE(2:0]: PLL Config. set to '011' for 25MHz input frequency.
		•	,												BOOTMODES 0 BOOTMODES 0 BOOTMODES 1 BOOTMODES 1
						,									BOOTMODE? 0.  BOOTMODE8 0. MCU_BOOTMODE[9:7]: Primary Boot Mode Config, set to '100': B8=1: MMC Port 1 (4 bit width).  BOOTMODE9 1. BOOTMODE9:7]: Primary Boot Mode Config, set to '100': B8=1: MMC Port 1 (4 bit width).  BOOTMODE9 1.
															BOOTMODE(0 0   MCU_BOOTMODE[12:10]: Backup Boot Mode, set to '100' for Backup boot is Ethernet.
															BOOTMODE(18 0   MCU_BOOTMODE(13): Backup Boot Mode Config. set to '0' :RGMII with internal TX delay.    BOOTMODE(14 0   BOOTMODE(15:14): Reserved pins.
				R86	R87	R306	R307	R284	R303	R299	R297	R301	R296	R295	R298

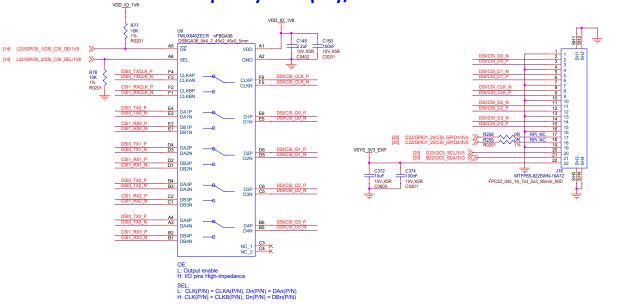
**Backup Boot: Ethernet.** 

# DSI U28E DSI0 - TX (VDDA\_CORE\_CSL\_DSI) DSI0\_TXCLKP BSID\_TXCLKP (NDDA\_CORE\_CSL\_DSI) DSI0\_TXCLKP DSI0\_TXCLKP AE16 DSI0\_TXCLKP AE17 DSI0\_TXCLKP AE16 DSI0\_TXCLKP AE17 DSI0\_TXCLKP AE17 DSI0\_TXCLKP AE17 DSI0\_TXCLX N AD18 DSI0\_TXCLX N AD19 DSI0\_TXCLX

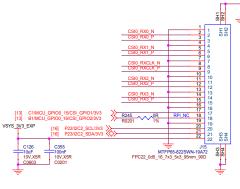
# CSI 0, 1, 2, 3



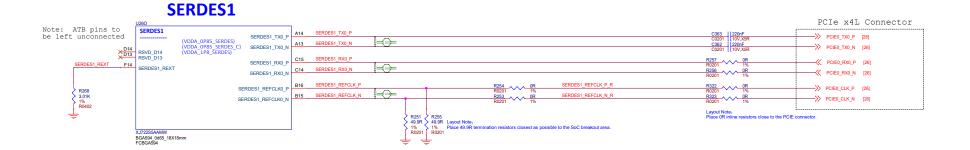
# Raspberry Pi Display/Camera Connector x4 Lane



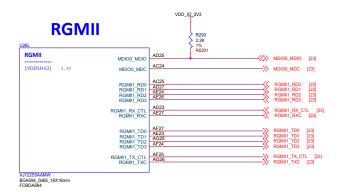
# Raspberry Pi Camera Connector x4 Lane





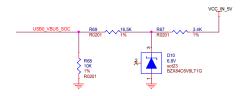


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Draw By	Junqing.Xin	Date:	Tuesda	y, April 30, 2024	Si	neet: 18 of 27		



#### **USB VBUS Resistor divider circuit**

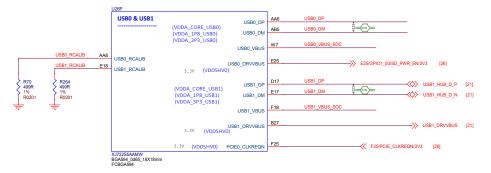
Note: Recommended VBUS circuit for USB connector. Supports 5V VBUS

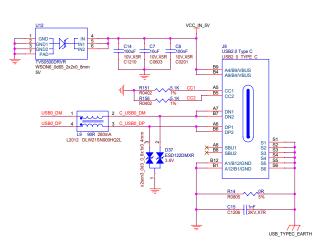


Note: Recommended VBUS circuit for embedded Hub

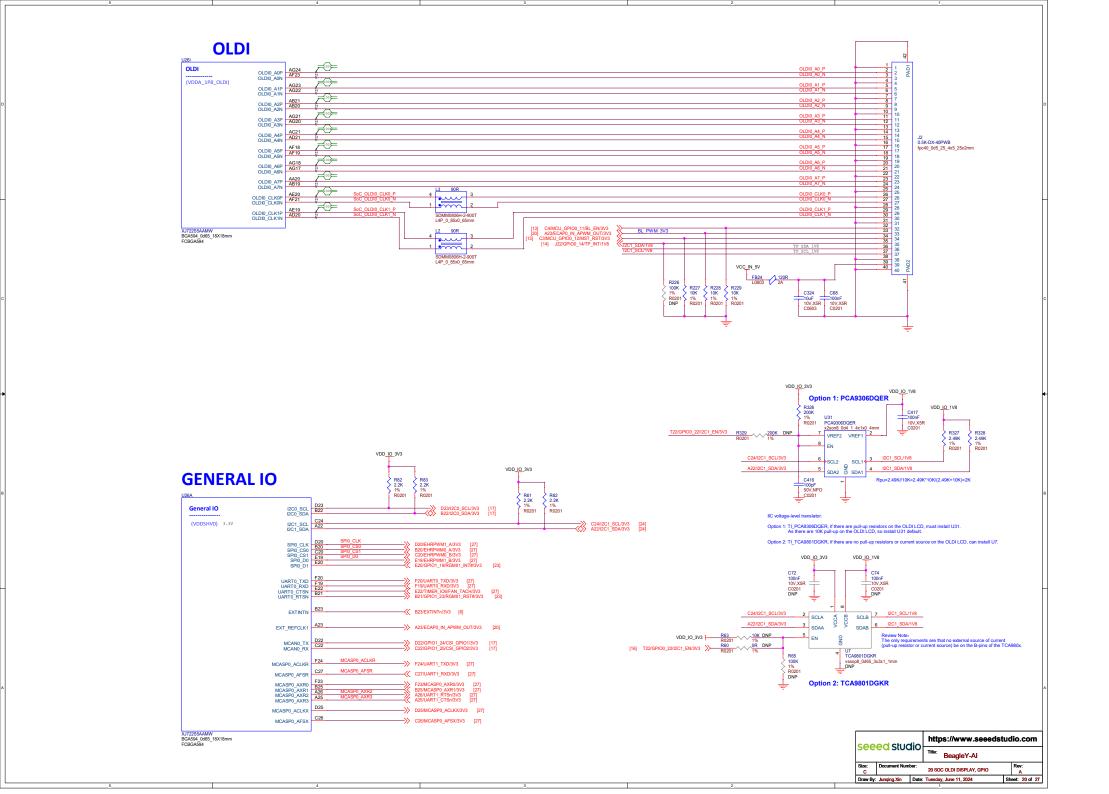


# **USB0 & USB1**

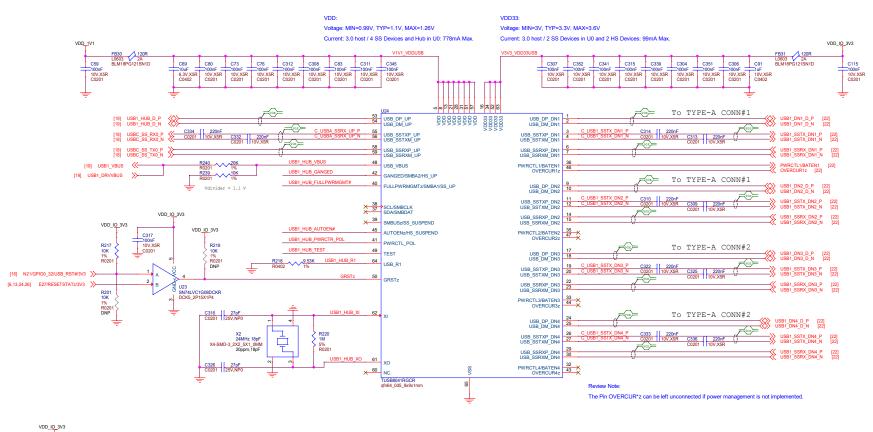


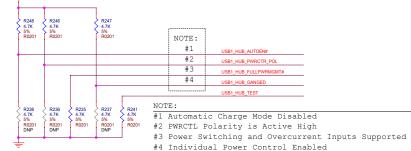


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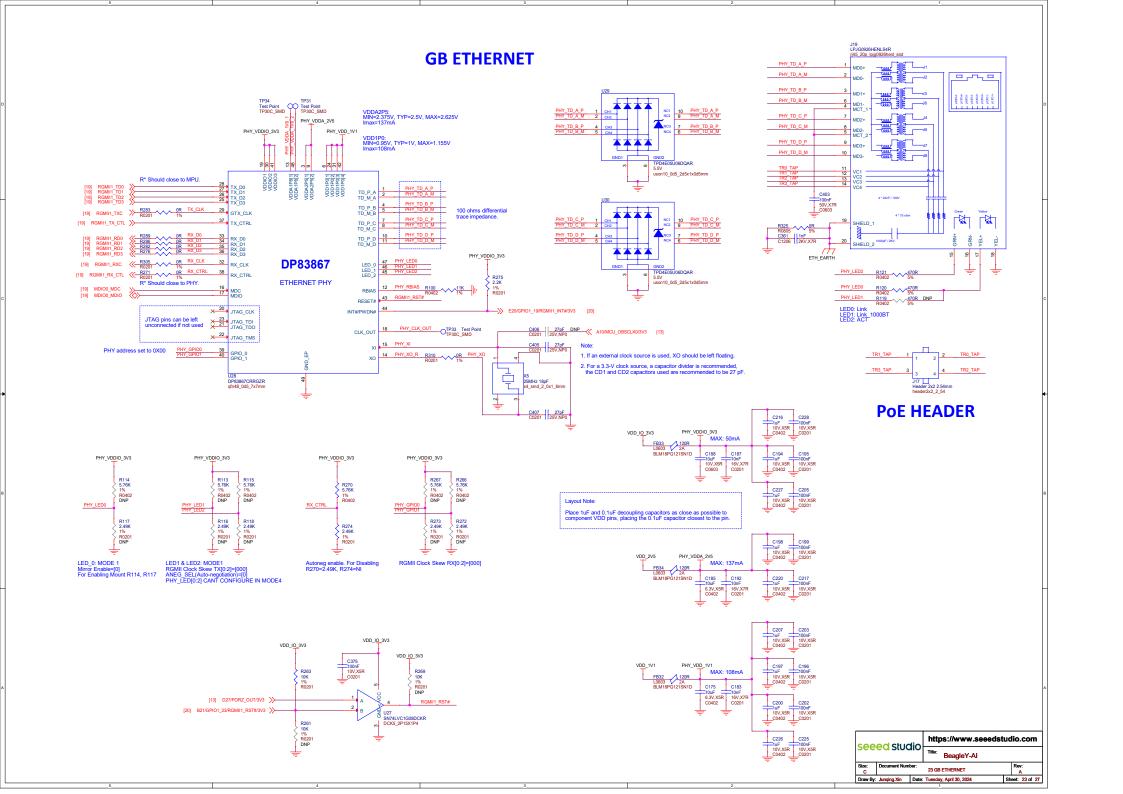


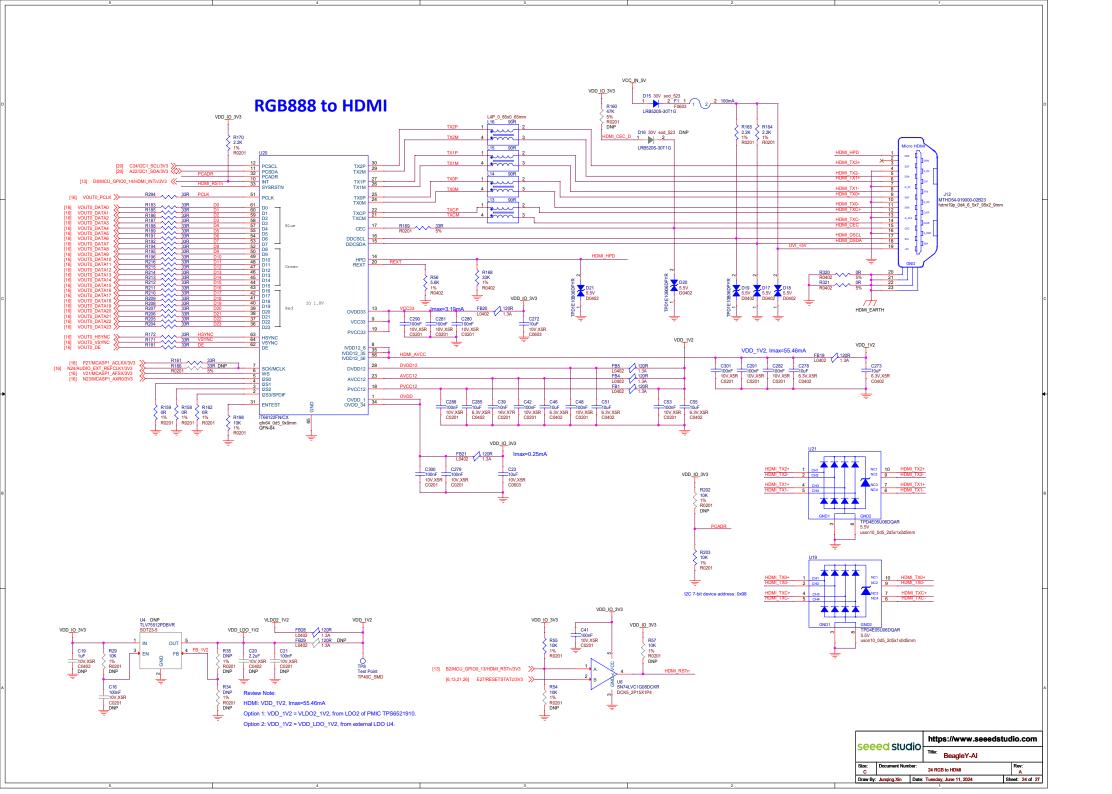
#### **USB 3.0 HUB**

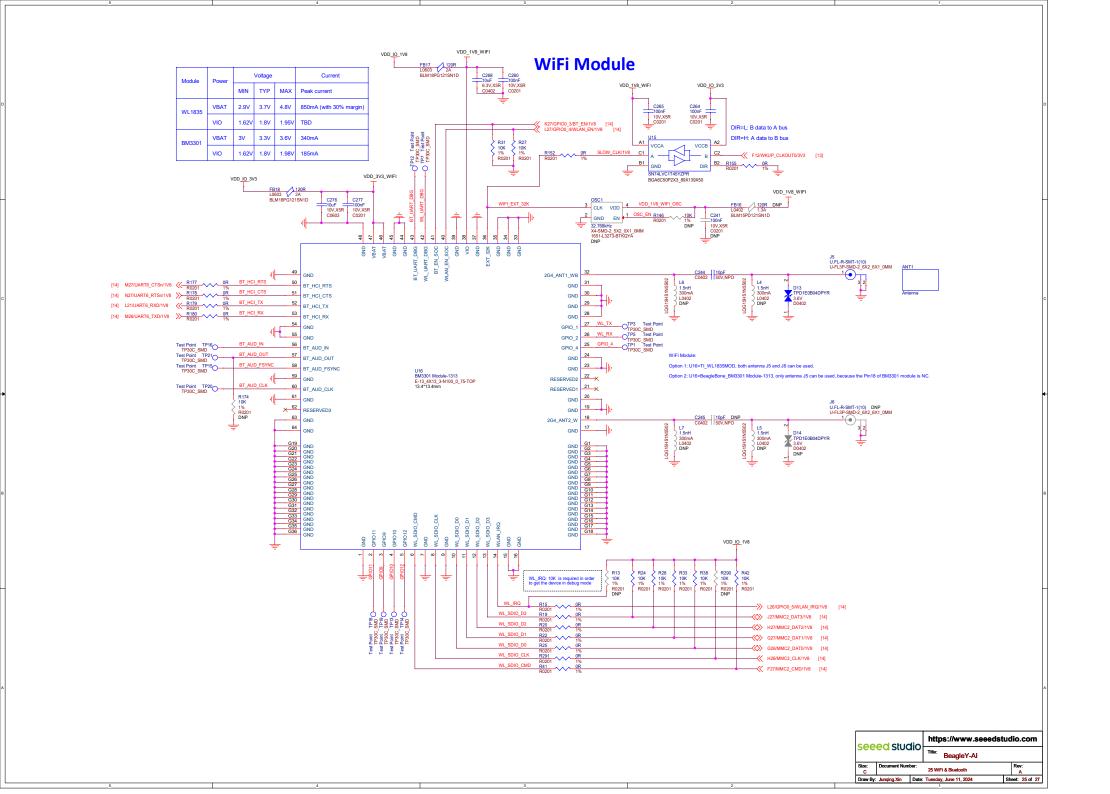




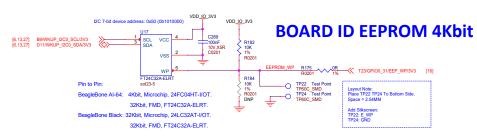
#### L17 90R 280mA 1 2 **USB 3.0 DUAL TYPE-A** L2012 DLW21SN900HQ2L L28 90R 280mA [21] USB1\_SSRX\_DN2\_N <<-TAB\_2 22 4 3 L2012 DLW21SN900HQ2L VCC\_IN\_5V L26 90R 280mA USB3\_TYPE\_A\_TOP VDD\_IO\_3V3 [21] USB1\_SSTX\_DN2\_N >>-[21] USB1 SSTX DN2 P >> VBUS 5V0 TYPEA U11 TPS2561DRCR L2012 DLW21SN900HQ2L R110 > 100K • 1% R0201 vson10\_0d5\_3x3x1mm OUT1 8 X 150uF 10V,Tantalum AVX\_C 10 FAULT1 FAULT2 [21] OVERCUR1z <<-C411 100nF 10V,X5R C0201 4 EN1 Q Q LIM 7 R99 10K 1% R0201 L27 90R 280mA USB3\_TYPE\_A\_BOTTOM 12012 DI W21SN900HO21 L18 90R 280mA TAB\_4 20 <del>, .....</del> [21] USB1 SSRX DN1 P ( L2012 DLW21SN900HQ2L L25 90R 280mA [21] USB1\_SSTX\_DN1\_N >> 4 3 [21] USB1\_SSTX\_DN1\_P >> C237 | 1nF C1206 | 2KV,X7R D33 ESD122DMXR L2012 DLW21SN900HQ2L USB\_TYPEA1\_EARTH VBUS\_5V0\_TYPEA J20 UBF30-D2112 L22 90R 280mA USB3\_0\_2d0\_17\_5x13\_78x15\_49mm\_slot [21] USB1\_DN4\_D\_P (>> L23 90R 280mA TAB 1 [21] USB1\_SSRX\_DN4\_N <<-2 TAB\_2 22 4 3 T\_USB1\_SSTX\_DN4\_N 1 2012 DI W21SN900HO21 USB3\_TYPE\_A\_TOP [21] USB1\_SSTX\_DN4\_N >> 4 3 [21] USB1 SSTX DN4 P SS-D29 ESD122DMXR L2012 DLW21SN900HQ2L L21 90R 280mA 4 .... USB3\_TYPE\_A\_BOTTOM VBUS\_0 DN\_0 DP\_0 GND 1 • ~ 2 [21] USB1\_DN3\_D\_P ( ) L2012 DLW21SN900HQ2L TAB\_3 L24 90R 280mA [21] USB1\_SSRX\_DN3\_N <<-TAB\_4 - www 4 3 [21] USB1\_SSRX\_DN3\_P <<-L2012 DLW21SN900HQ2L L19 90R 280mA [21] USB1 SSTX DN3 N >>-4 3 [21] USB1\_SSTX\_DN3\_P >> C360 | 1nF C1206 | 2KV,X7R L2012 DLW21SN900HQ2L USB\_TYPEA2\_EARTH https://www.seeedstudio.com seeed studio Title: BeagleY-Al 22 USB3.0 TYPE-A CONNECTORS Draw By: Junqing.Xin Date: Tuesday, April 30, 2024 Sheet: 22 of 27







# **Micro SD CARD INTERFACE** VDD IO 3V3 C9 100nF 10V,X5R C0201 C8 22uF 10V,X5R C0805 **Load Switch** R17 10K 1% R0201 [6,13,21,24] E27/RESETSTATz/3V3 >> [19] E25/GPIO1\_50/SD\_PWR\_EN/3V3 >>g QOD VDD\_MMC1 power is from PMIC VDD\_IO\_3V3 R8 47K 5% R0201 **uSD Card Connector** R6 > 47K > 5% R0201 R9 47K 5% R0201 Lavout Note: Place ESD near SD Card Connector **PCIe CONNECTOR** C238 100nF 10V,X5R C0201 VDD\_IO\_3V3 R143 2.2K 1% R0201 DNP J7 MTFP65-816SWN-19A72 FPC16\_0d5\_13\_7x3\_5x3\_95mm\_90D [13] C5/MCU\_GPIO0\_8/PCIE\_PWR\_EN/3V3 [13] B8/MCU\_GPIO0\_5/PCIE\_DET\_WAKE/3V3 [19] F25/PCIE\_CLKREQN/3V3 [13] B4/MCU\_GPIO0\_6/PCIE\_RST/3V3 R141 100K 1% R0201 DNP



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Draw By:	Junqing.Xin	Date: T	uesda	y, June 11, 2024	SI	heet: 26 of 27	

### **USER EXPANSION CONNECTOR** TXD0(GPIOTA RXD0(GPIOTA GPIO18 GND\_7 GEN4(GPIO23 GEN5(GPIO24 GND - 6 GEN6(GPIO25 CEGIGPIO8 CET/GPIO7 ID SC GND\_5 GPIO12 GND\_4 GPIO16 GPIO20 GPIO20 GPIO21 TI EVM: Used A25/UART1\_CTSn [13] [13] TI EVM: Used C5/MCU\_GPIO0\_8 [6,13,26] D11/WKUP\_I2C0\_SDA/3V3 [20] B20/EFRPWM0\_A3V3 [20] D20/EFRPWM1\_A3V3 [20] C20/EFRPWM1\_B3V3 [20] C26/MCASP0\_AFSW3V3 [16] P26/GPIO\_36/EXP/3V3 TI EVM: Used A10/MCU\_SPI0\_CS1 ⟨ C20/EHRPWM0\_B/3V3 [20] A25/UART1\_CTSn/3V3 [20] F23/MCASP0\_AXR0/3V3 [20] B25/MCASP0\_AXR1/3V3 [20] TI EVM: Used R27/GPIO0\_41 **FAN CONNECTOR** VDD\_IO\_3V3 VCC\_IN\_5V VDD\_IO\_1V8 OR DNP U10 SN74LVC1T45YZPR BGA6C50P2X3 89X139X50 BeagleY-Al PCB [14] F26/EHRPWM2 A/FAN PWM/1V8 >> GND B1 FAN\_TACH R107 10K 1% R0201 R104 10K 1% R0201 J18 MTWF63-104SRN-01163 JST4P\_1d0\_6\_2x3x4\_9mm D12 5.5V D0402 8 D0402 VDD IO 3V3 VDD\_IO\_3V3 VCC IN 5V R112 10K 1% R0201 [20] E22/TIMER\_IO6/FAN\_TACH/3V3 <<-VDD IO 3V3 **IIC EXT RTC Debug** Layout Note: Add Silkscreen J13: UART0 Pin1: RXD Pin2: GND Pin3: TXD VDD\_IO\_3V3 J13 MTWF63-103SRN-01163 UART0 is MPU Debug UART. MTWF63-102SRN-01163 JST2P\_1D0\_4\_2X3X4\_9MM I2C 7-bit device address: 0x68 (0b1101000) GND\_RTC LRB520S-30T1G https://www.seeedstudio.com seeed studio Title: BeagleY-Al 27 EXP 40PIN, FAN, RTC, DEBUG Draw By: Junqing.Xin Date: Tuesday, June 11, 2024 Sheet: 27 of 27