Integrated Circuit Design

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Chapter 1:

CMOS CIRCUIT AND TECHNOLOGY

Contents

- History and Trends of electronics.
- Evolution of Electronic Devices and ICs.
- VLSI procedure.
- Basic Components In VLSI Circuits

History and Trends of electronics

The first BJT

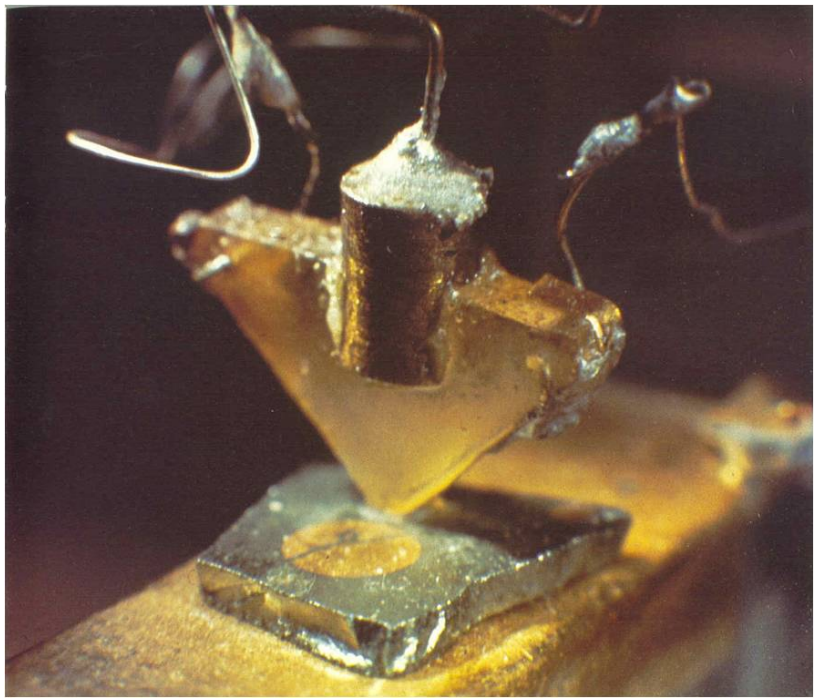


Figure 1: *Bardeen, Shockley, and Brattain at Bell Labs - Brattain and Bardeen invented the bipolar transistor in 1947 (left) , and The first germanium bipolar transistor (right)*

Evolution of Electronic Devices

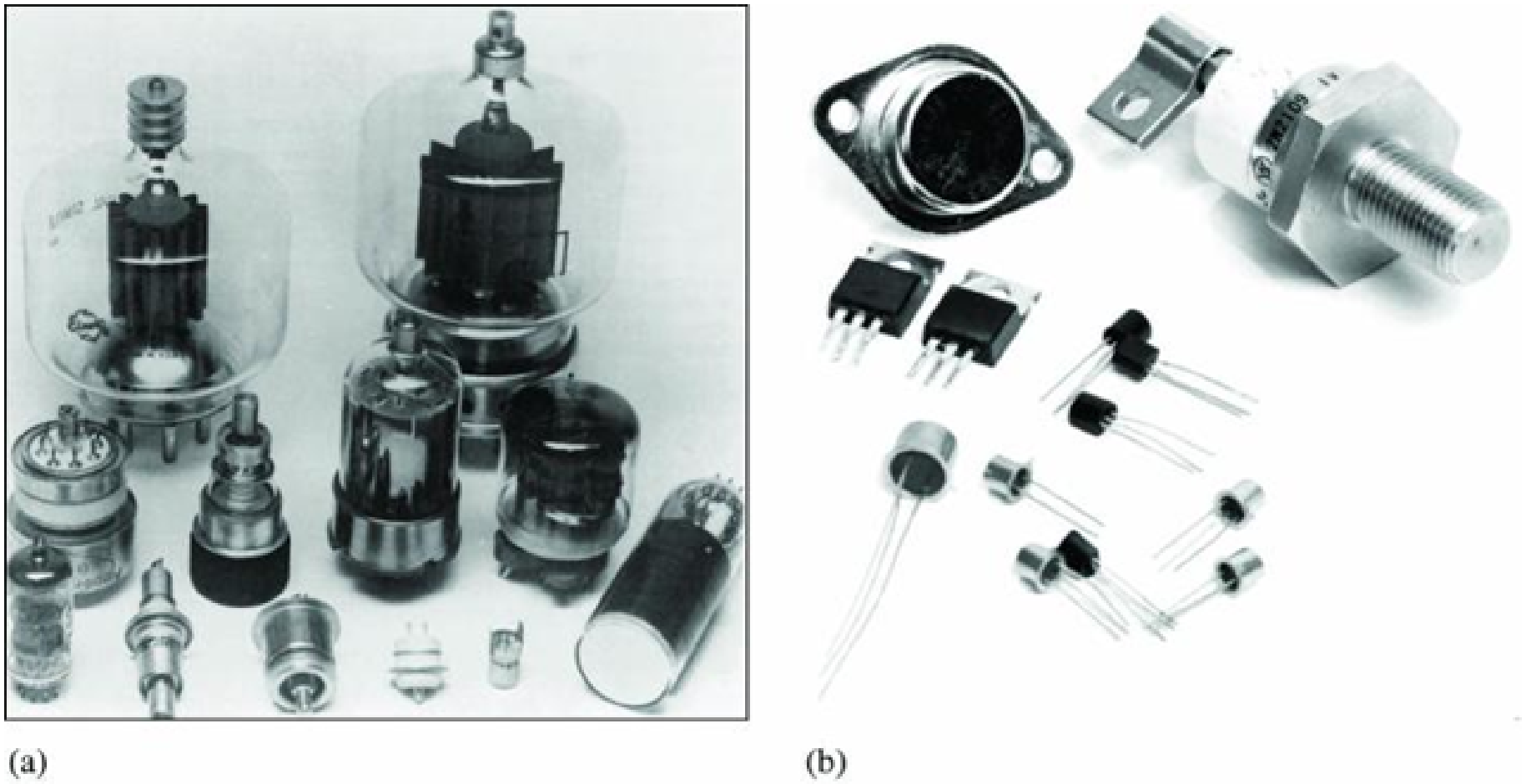


Figure 2: *a) Vacuum Tubes and b) Discrete Transistors*

The first Integrated circuit

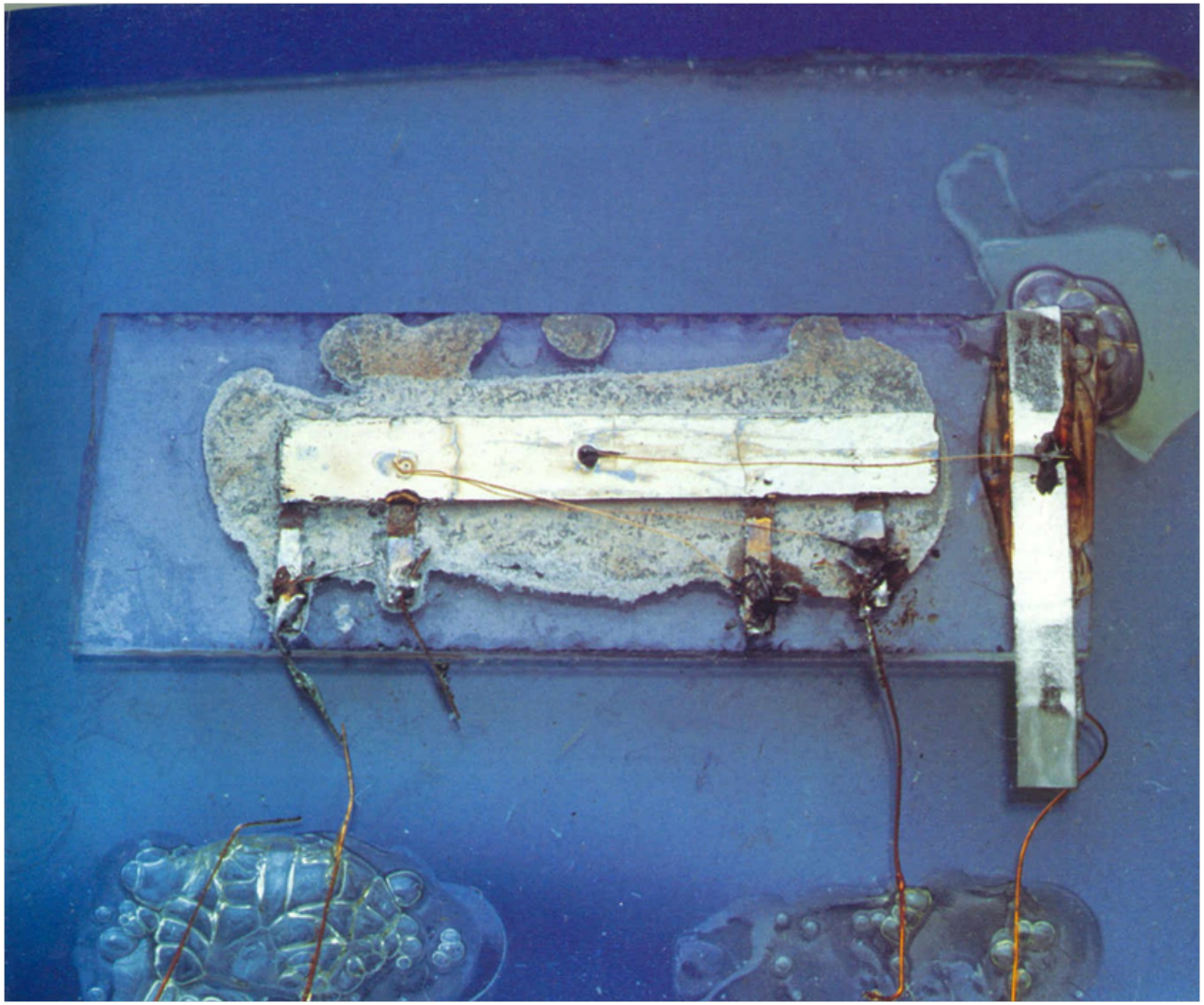


Figure 3: *The first IC Jack Kilby Texas Instruments 1958*

Evolution of Electronic Devices

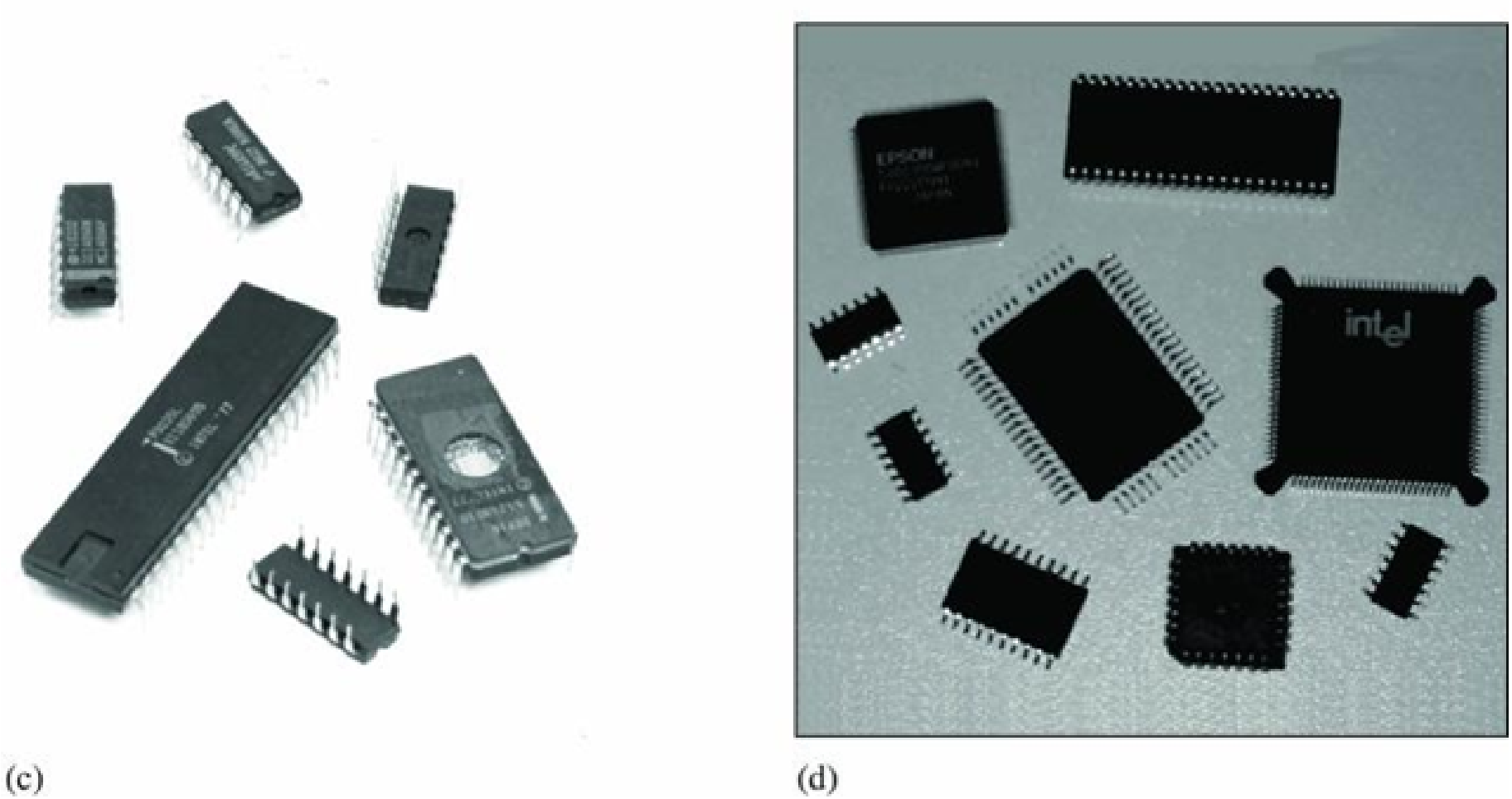
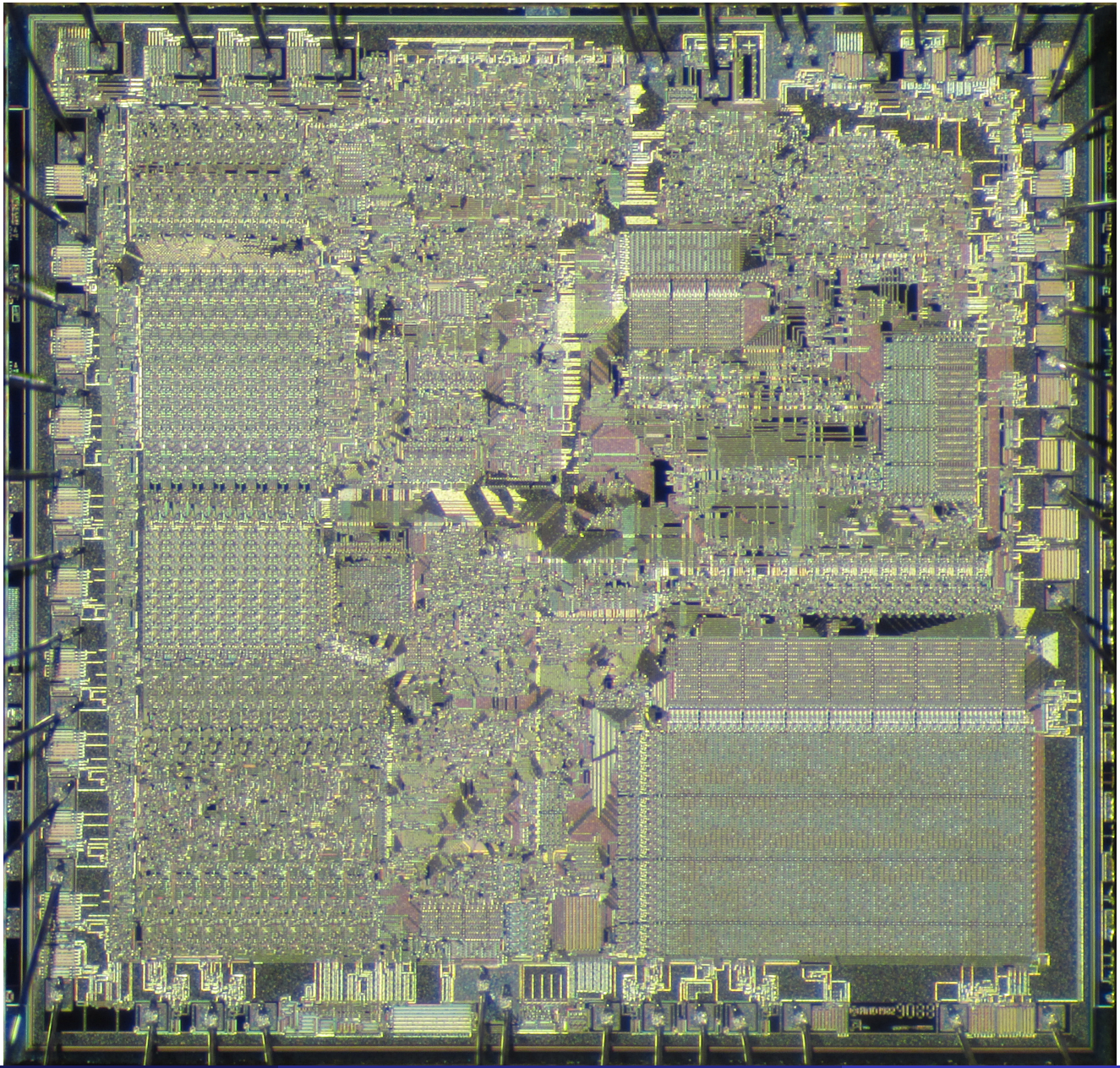


Figure 4: *c) SSI and MSI Integrated Circuits, and d) VLSI Surface-Mount Circuits*

AMD 8088 die



Pentium IV circuit mask diagram

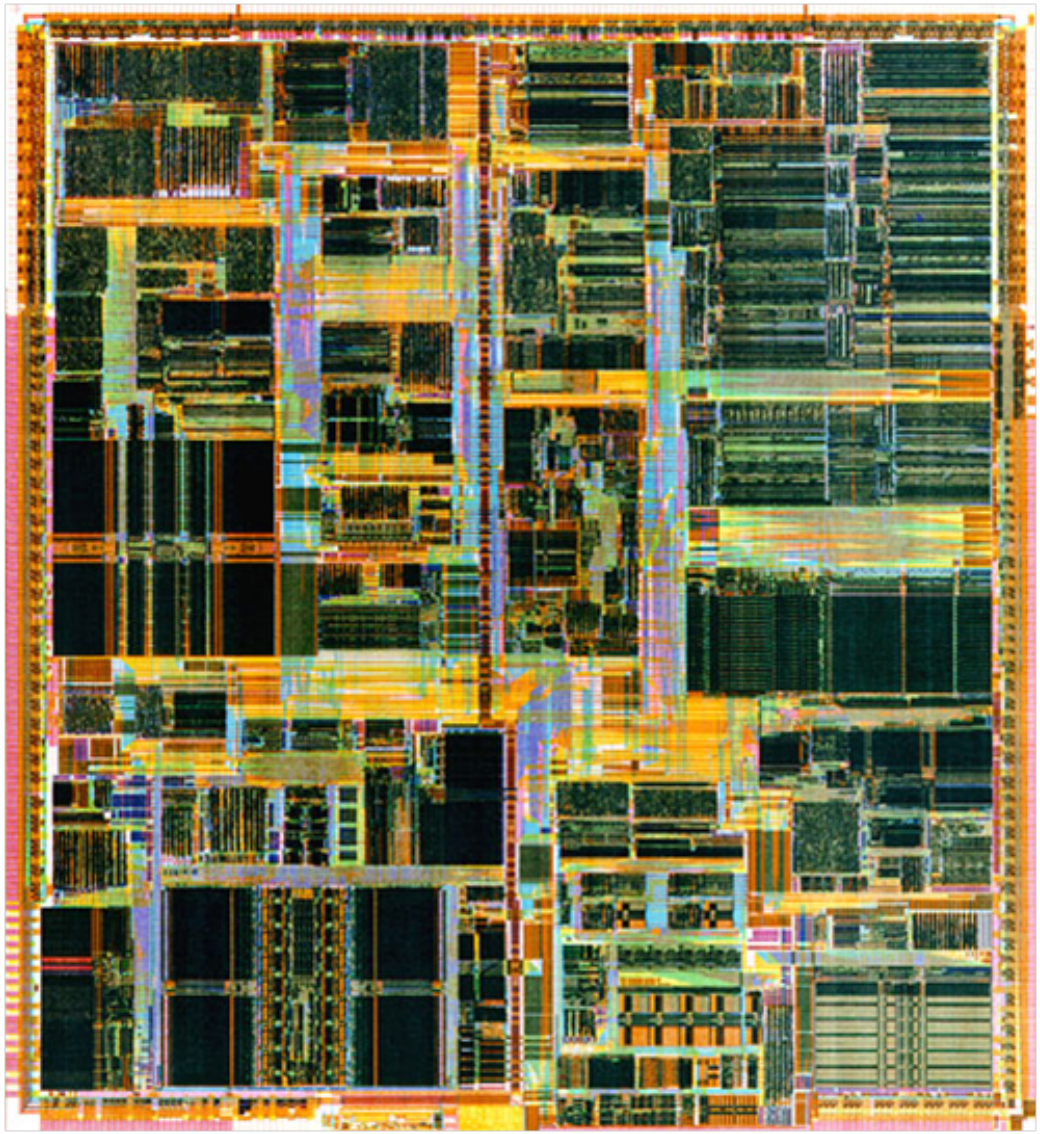


Figure 6: *2002 - 42 million transistors - 1.5 GHz, 130 nm tech.*

Core i7 circuit mask diagram

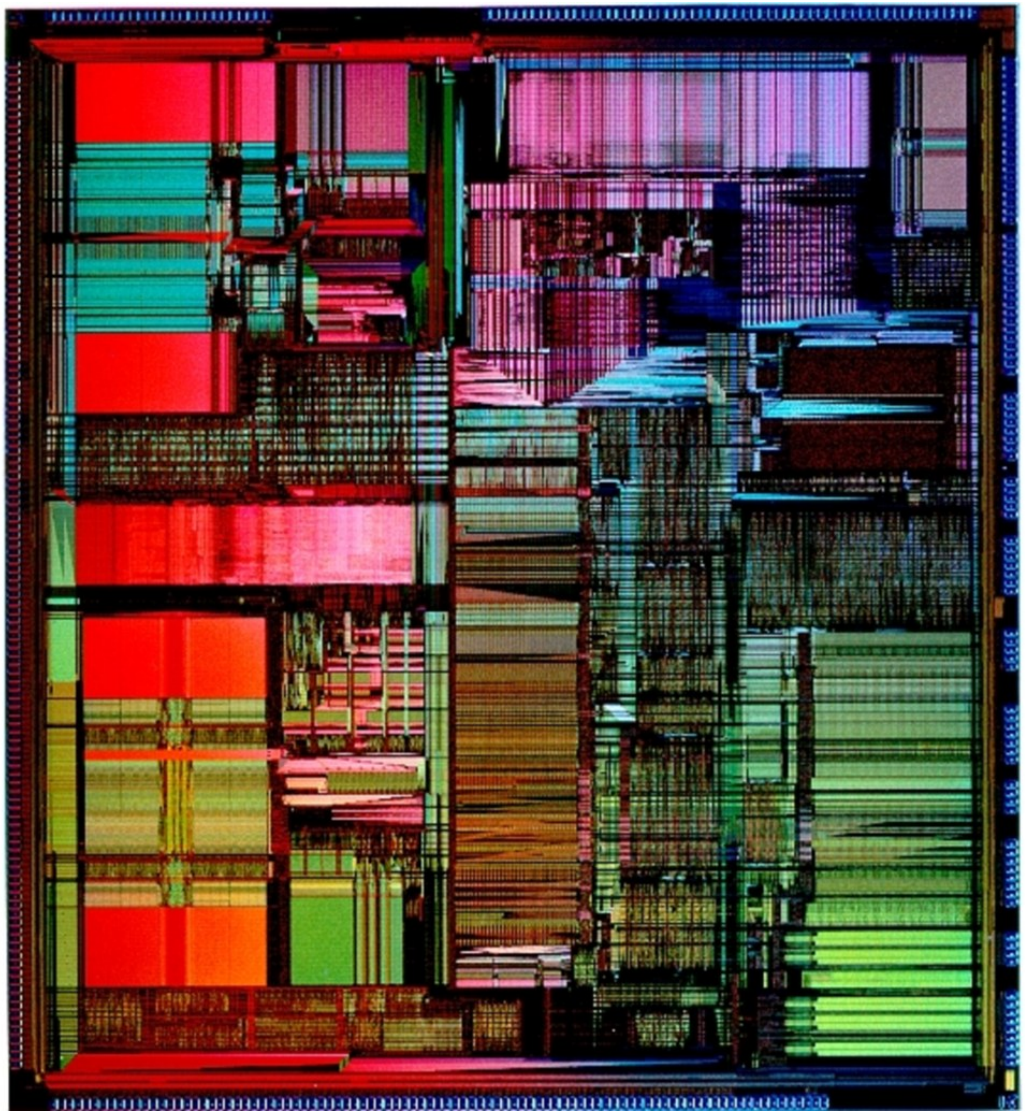


Figure 7: *Intel Core i7 processors based on Intel's Broadwell 14 nm technology*

Microprocessor trend

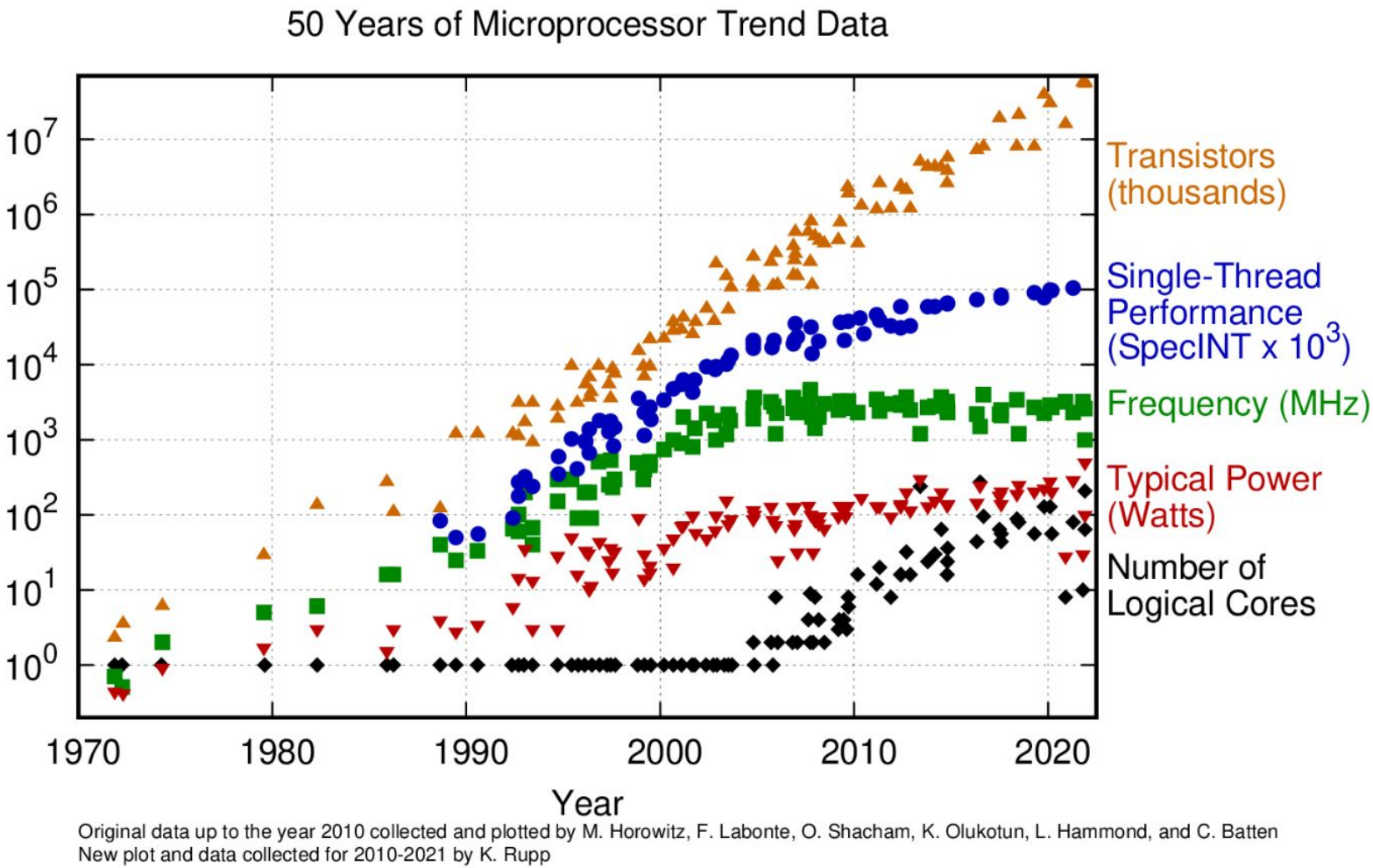


Figure 8

Other applications

Figure 9: *Many chips*

IC market

Military
2%

Industrial
8%

Computers
42%

Transportation
8%

Communications
24%

Consumer Electronics
16%

Technology nodes

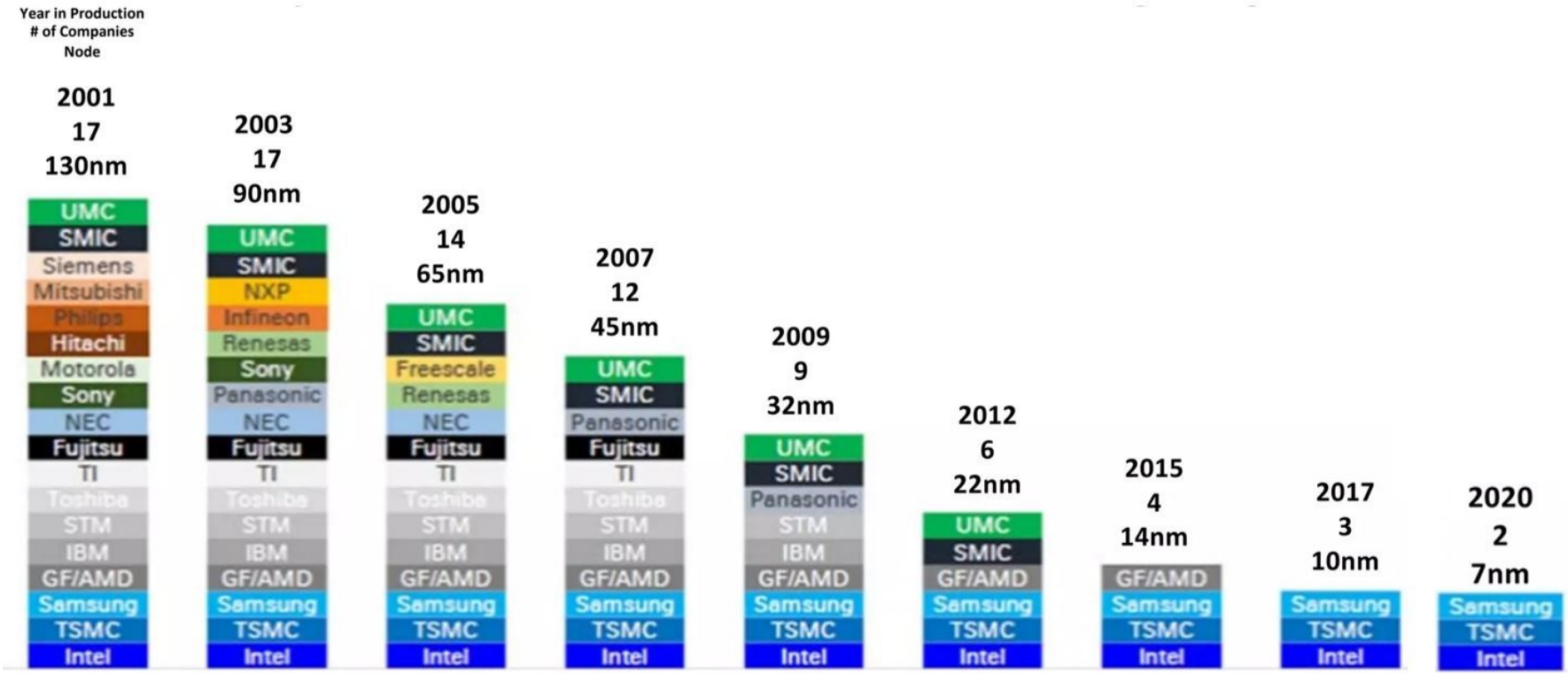


Figure 10

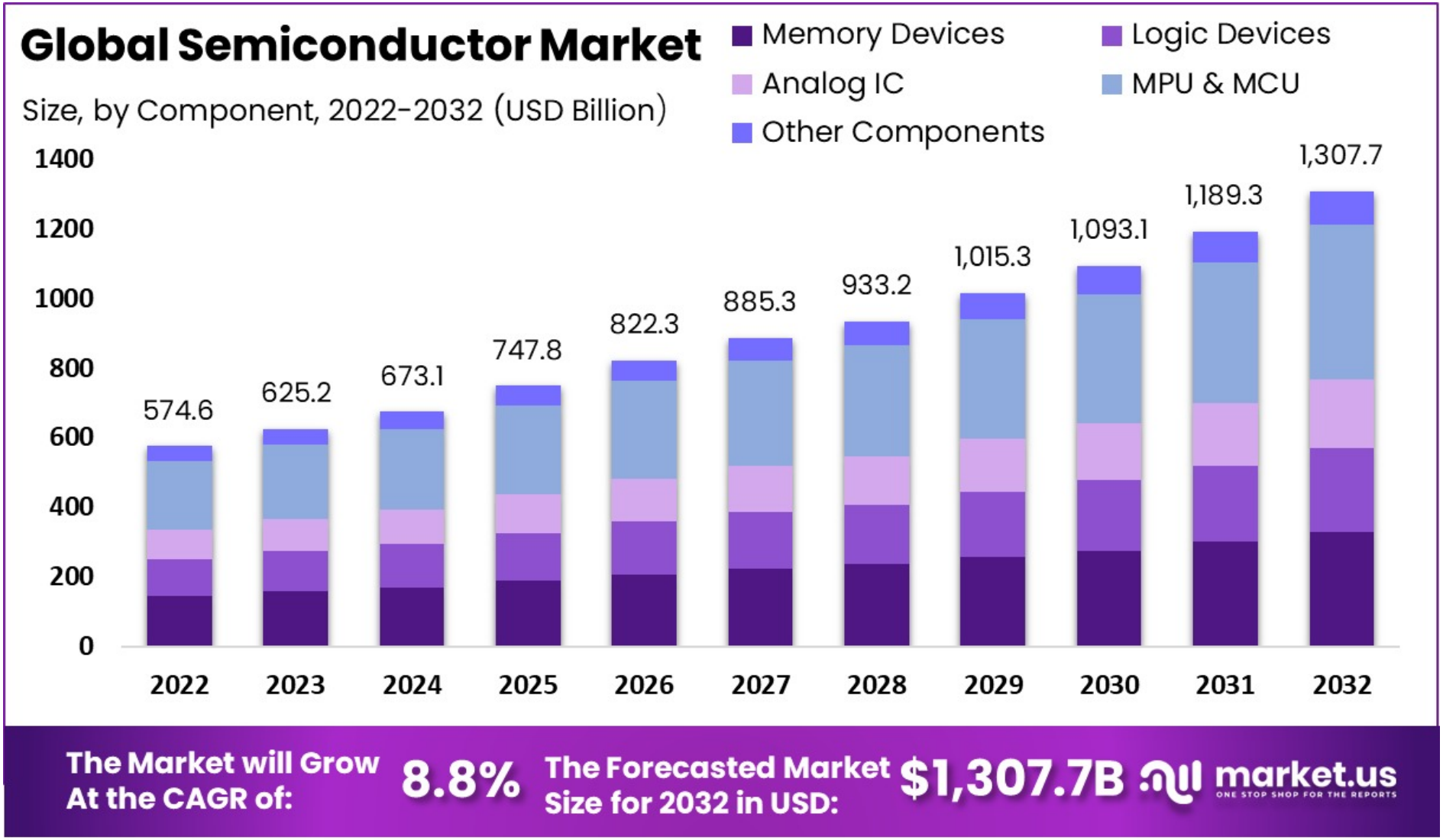
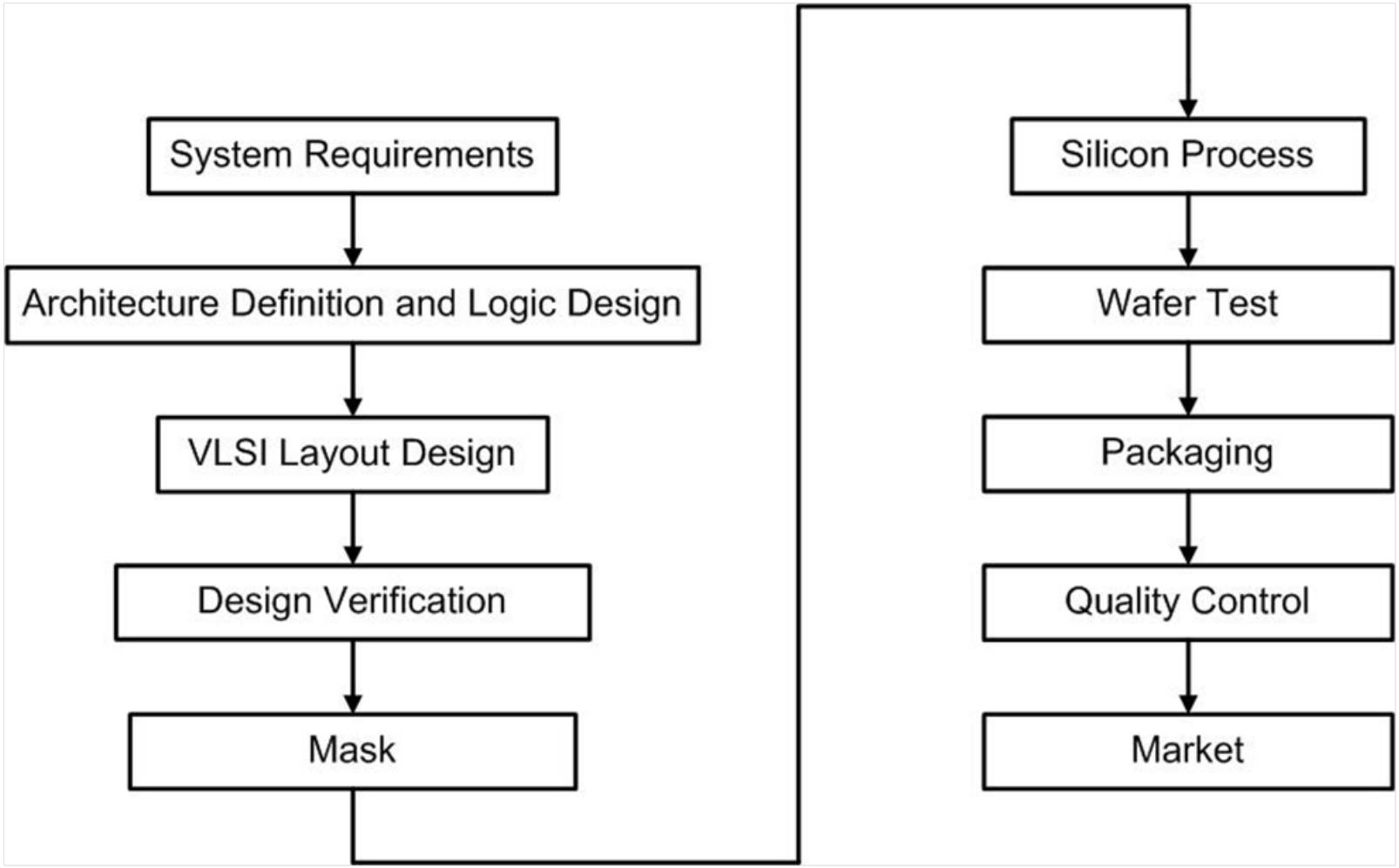

Global Semiconductor Market
Size, by Component, 2022-2032 (USD Billion)
Memory Devices
Logic Devices
Analog IC
MPU & MCU
Other Components
1400
1200
1000
800
600
400
200
0
574.6
625.2
673.1
747.8
822.3
885.3
933.2
1,015.3
1,093.1
1,189.3
1,307.7
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
The Market will Grow At the CAGR of:
8.8%
The Forecasted Market Size for 2032 in USD:
$1,307.7B
market.us
ONE STOP SHOP FOR THE REPORTS

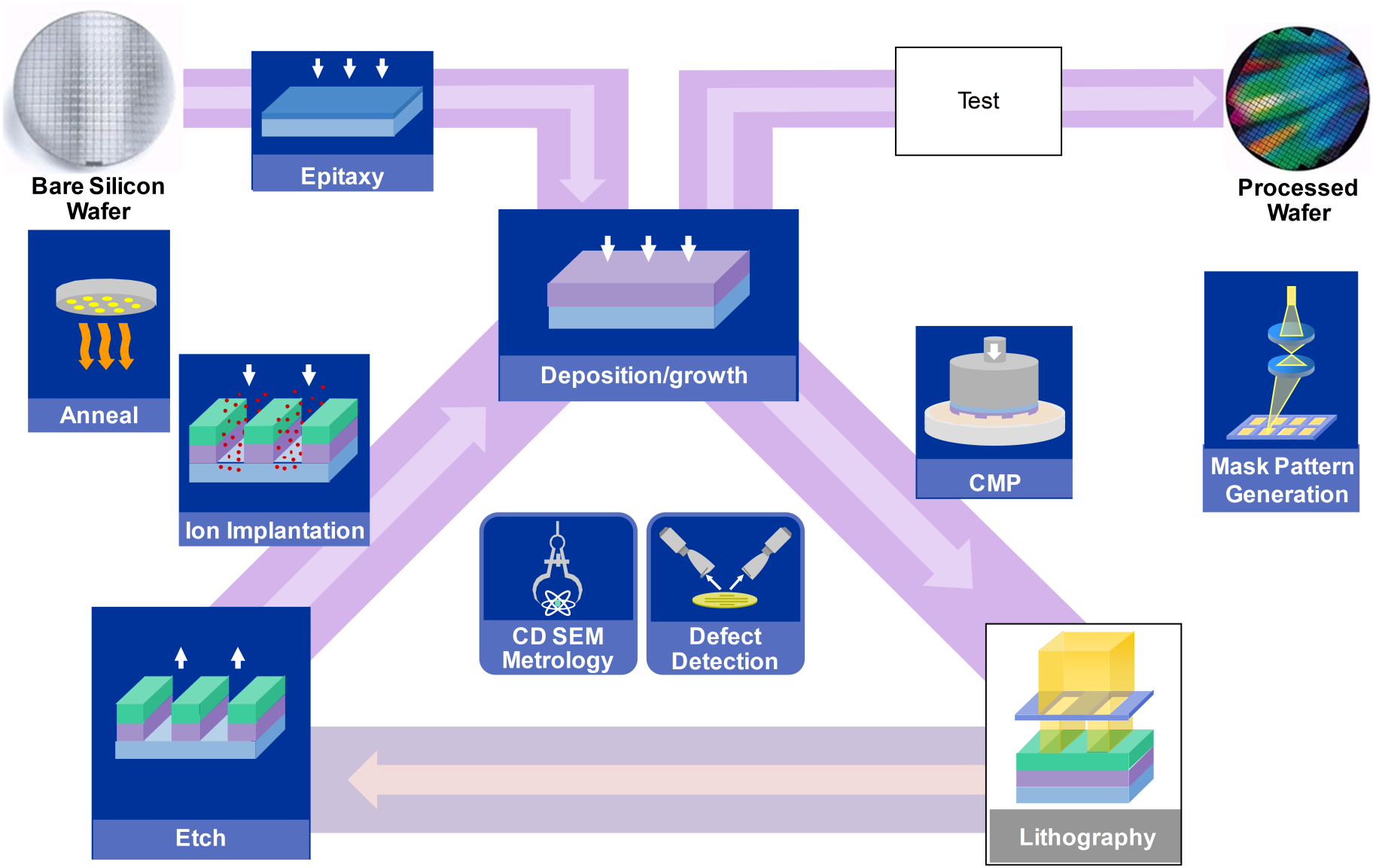
Figure 11

VLSI procedure

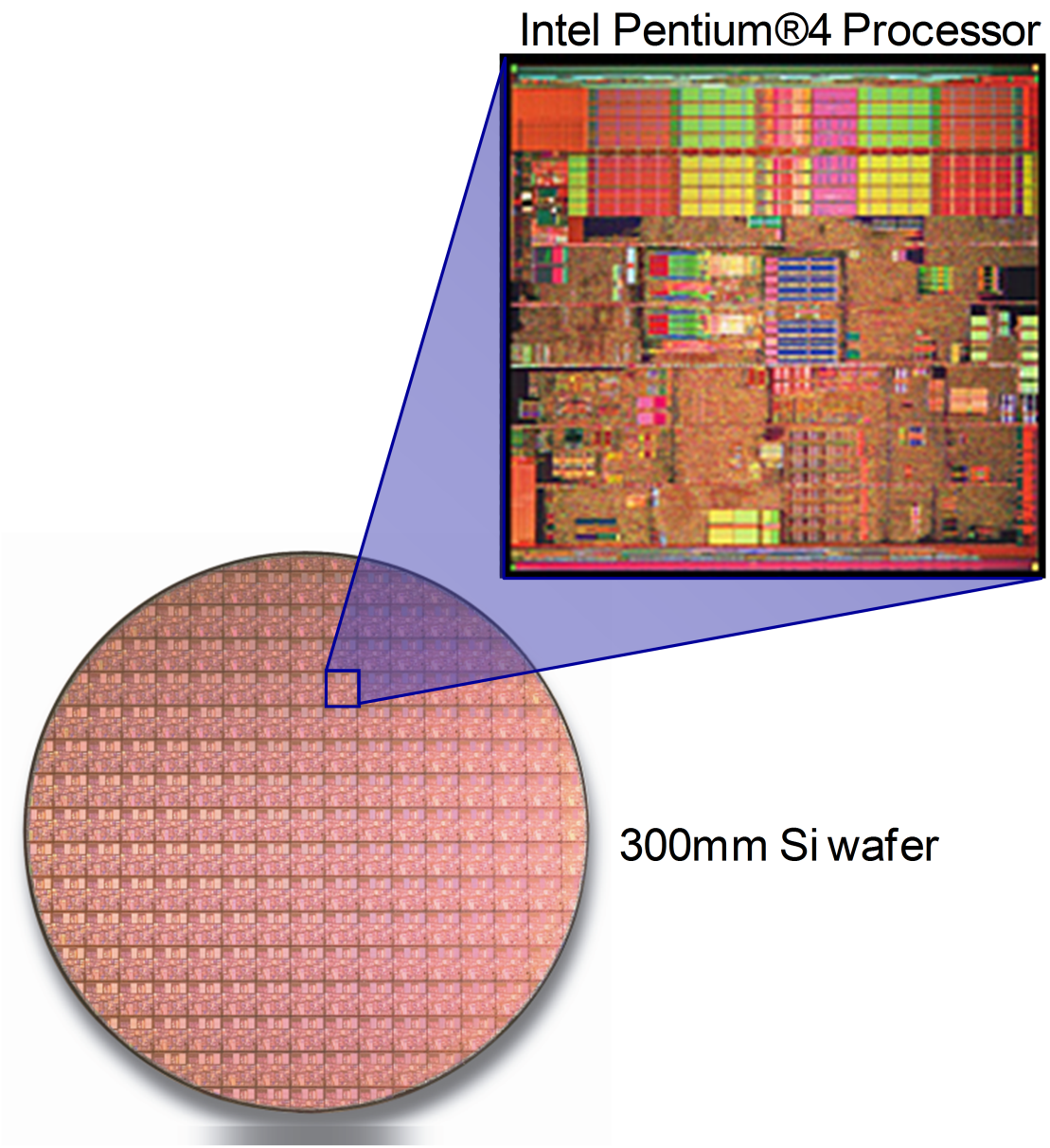


Design **Fabrication**

Overview of IC Process Steps (Lithography tech)



Example: Pentium IV



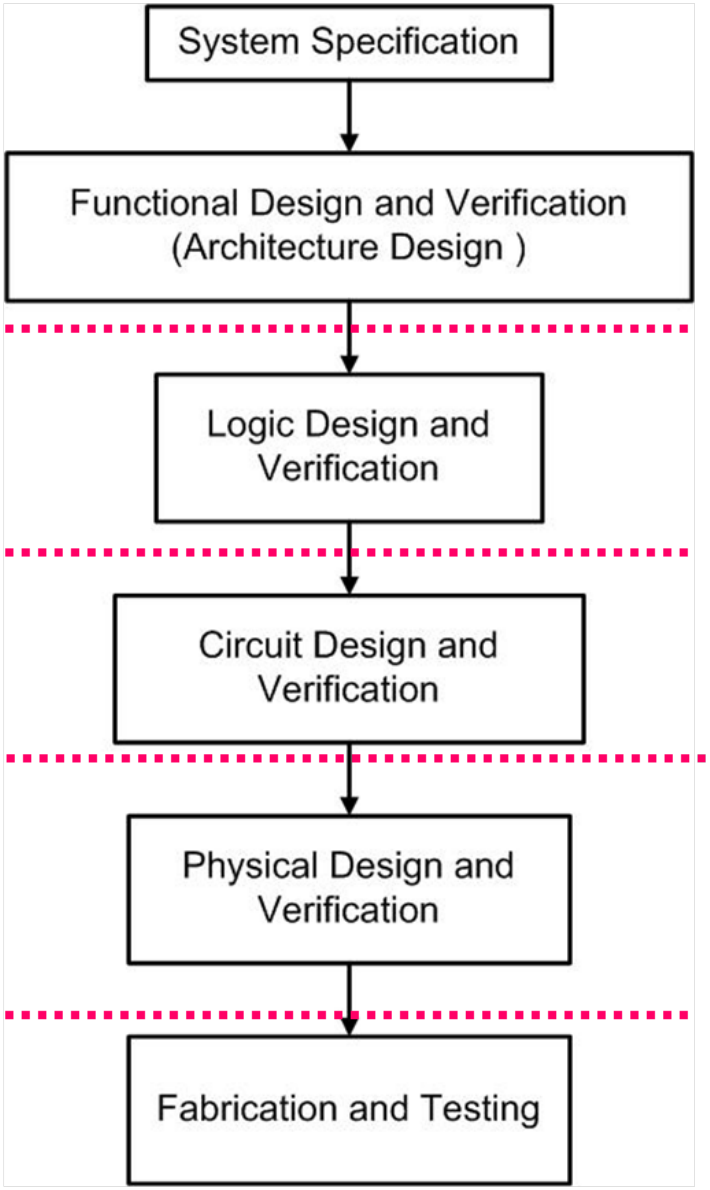
CAD tool

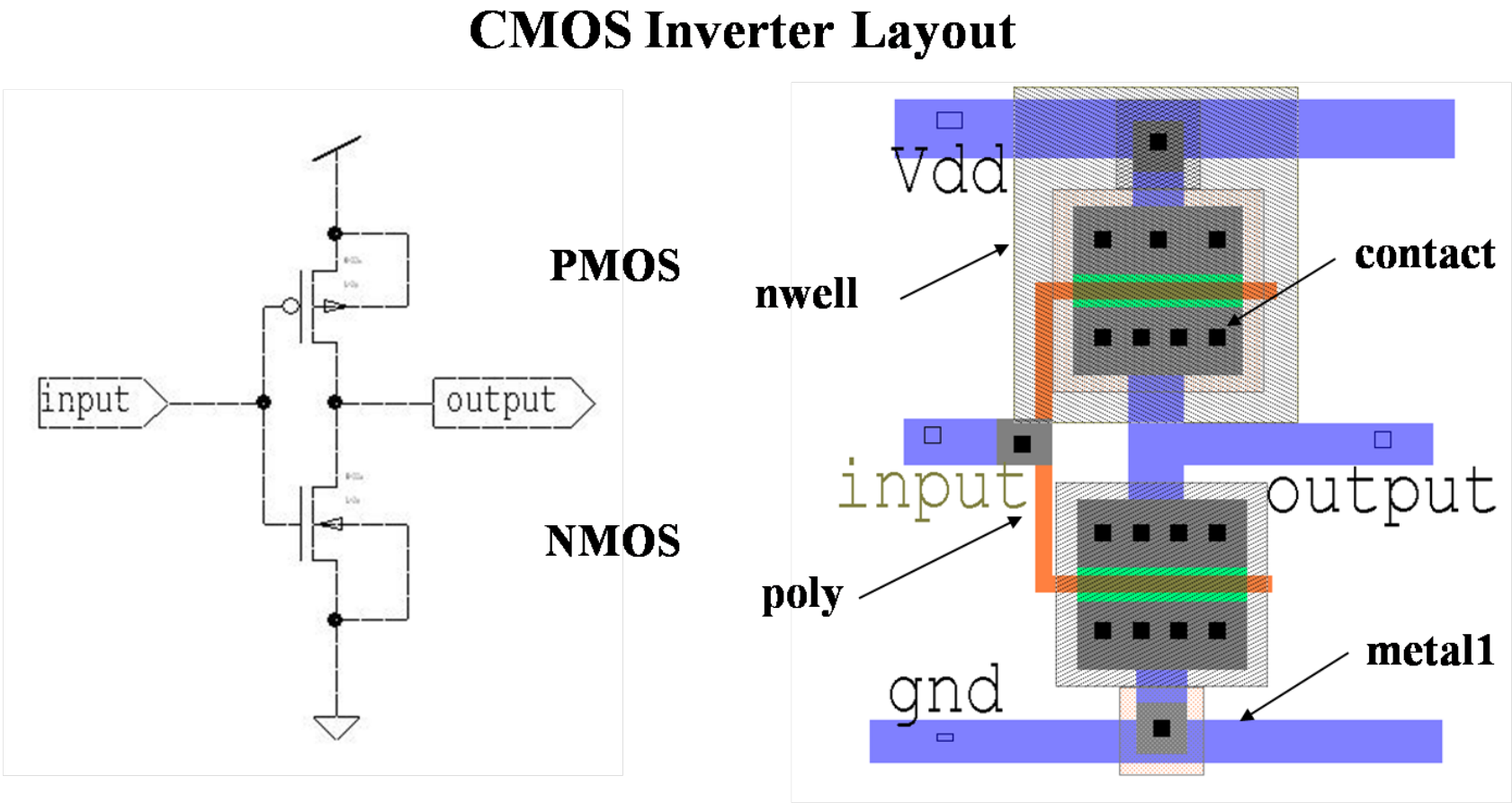
Behavioral Model
VHDL, Verilog

Gate Level
Sysnopsis, Leonardo, Microsim

Transistor Level
HSPICE, PSPICE, Cadence

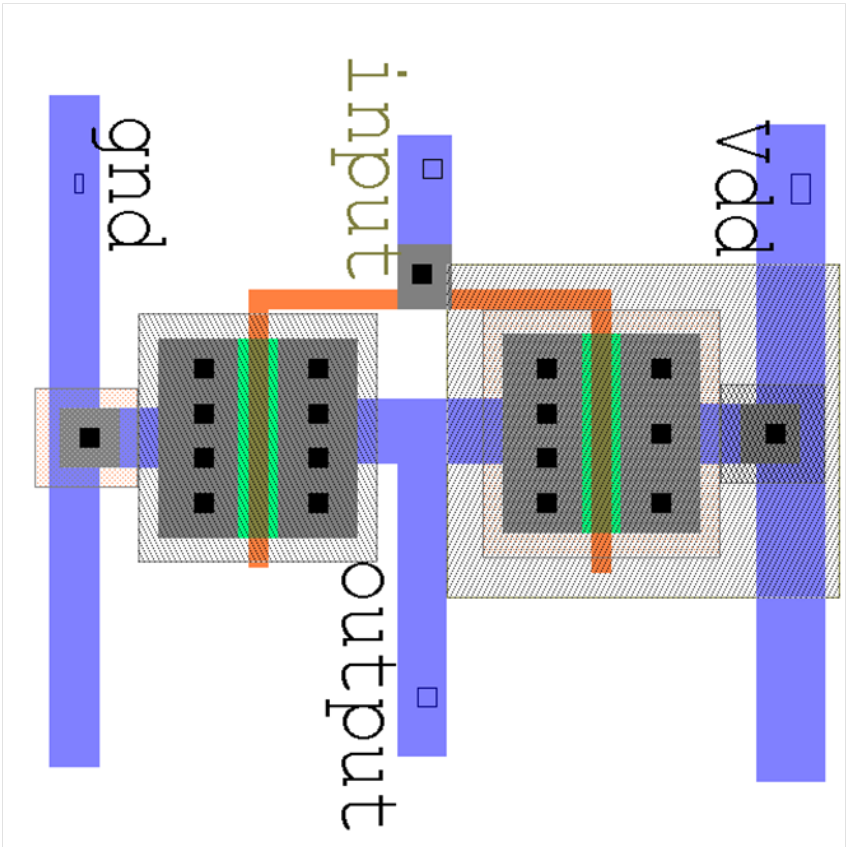
Physical Level (Layout Editor)
L-Edit, Magic, Mentor Graphic
Cadence



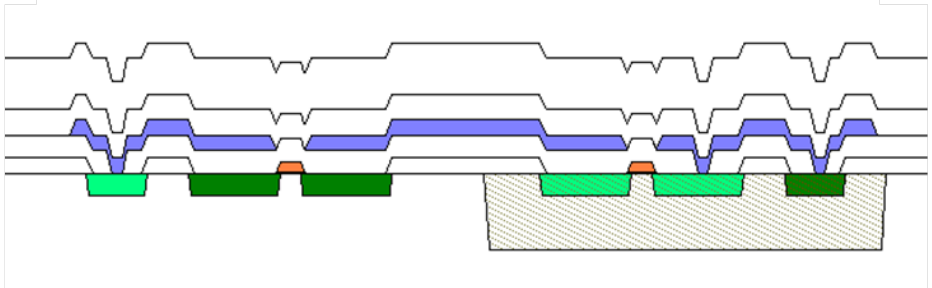

CMOS Inverter Layout
PMOS
NMOS
input
output
Vdd
nwell
contact
input
output
poly
metal1
gnd

Physical design

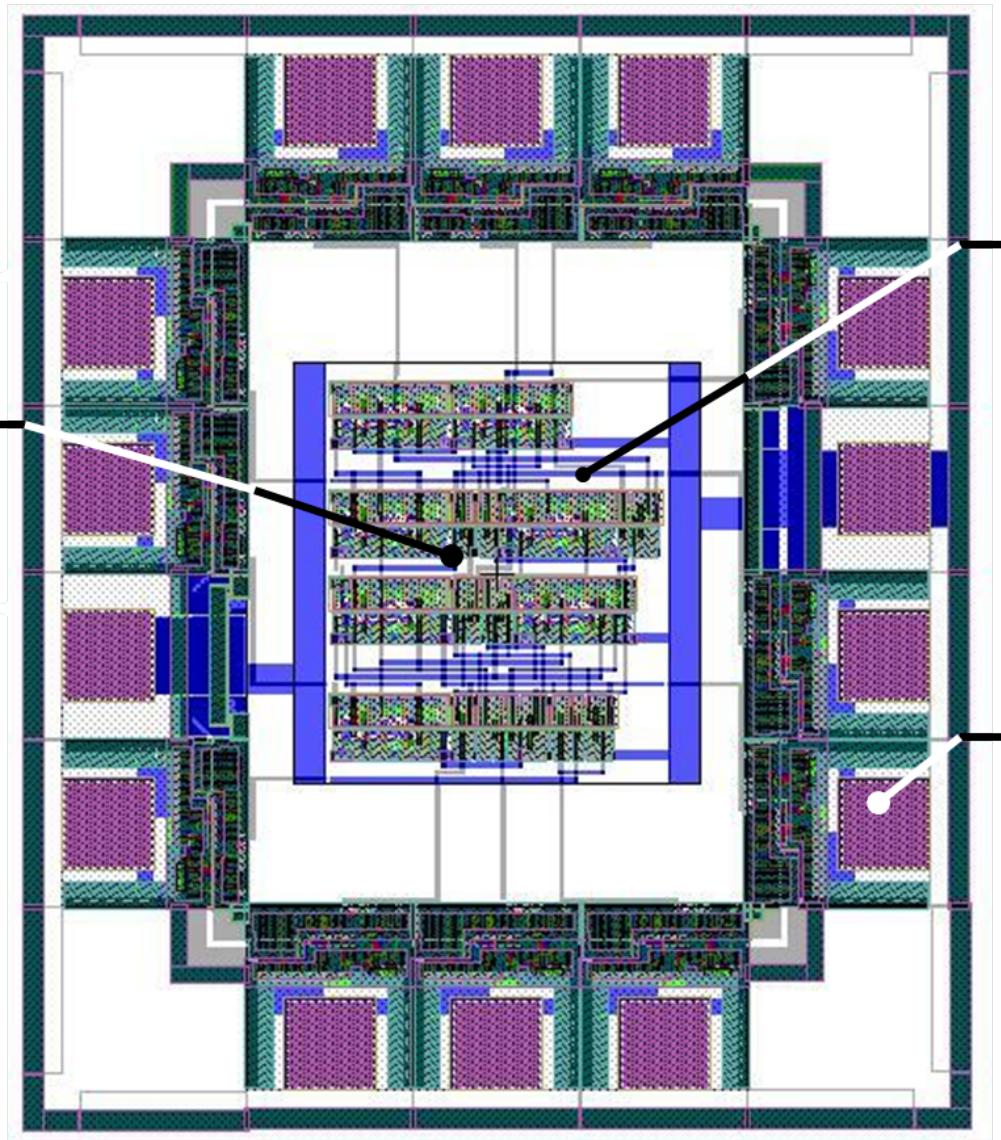
Top View (Layout)



Cross Sectional View

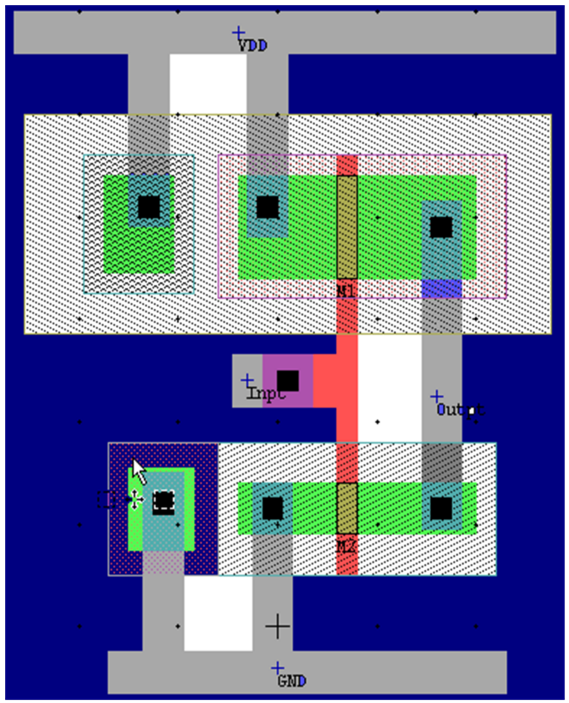


Chip layout

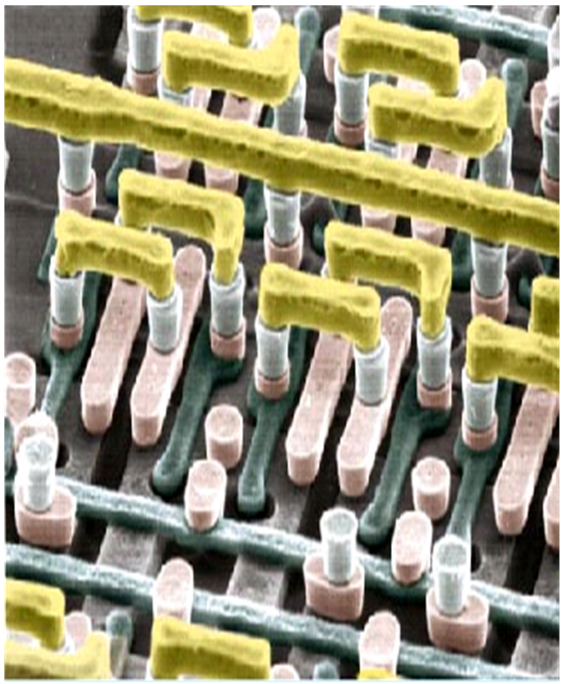


(Source: Tanner)

Layout to chip



Lithography Process



Designed Chip Layout

Fabricated Chip

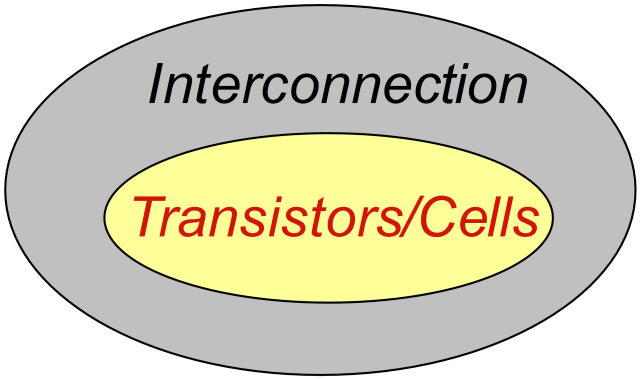
Figure 12

Basic Components In VLSI Circuits

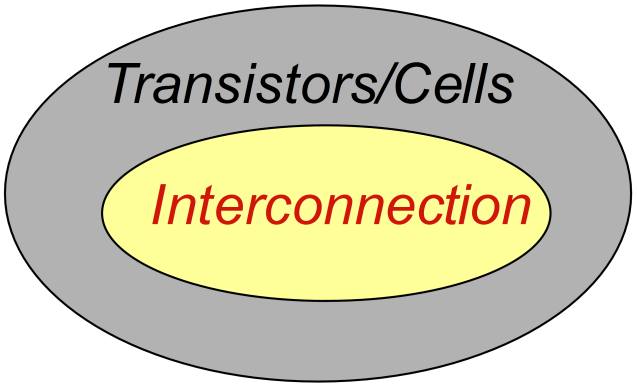
* **Devices**
  - Transistors - next .... ***Basic CMOS devices***
  - Logic gates and cells - next .... ***Logic gates***
  - Function blocks - next .... ***Analog and Digital circuits***

* **Interconnects**
  - Local interconnects
  - Global interconnects
  - Clock interconnects
  - Power/ground nets

New Paradigm for VLSI Design



Conventional Approach



New Approach

Interconnect-Driven Design

Interconnects

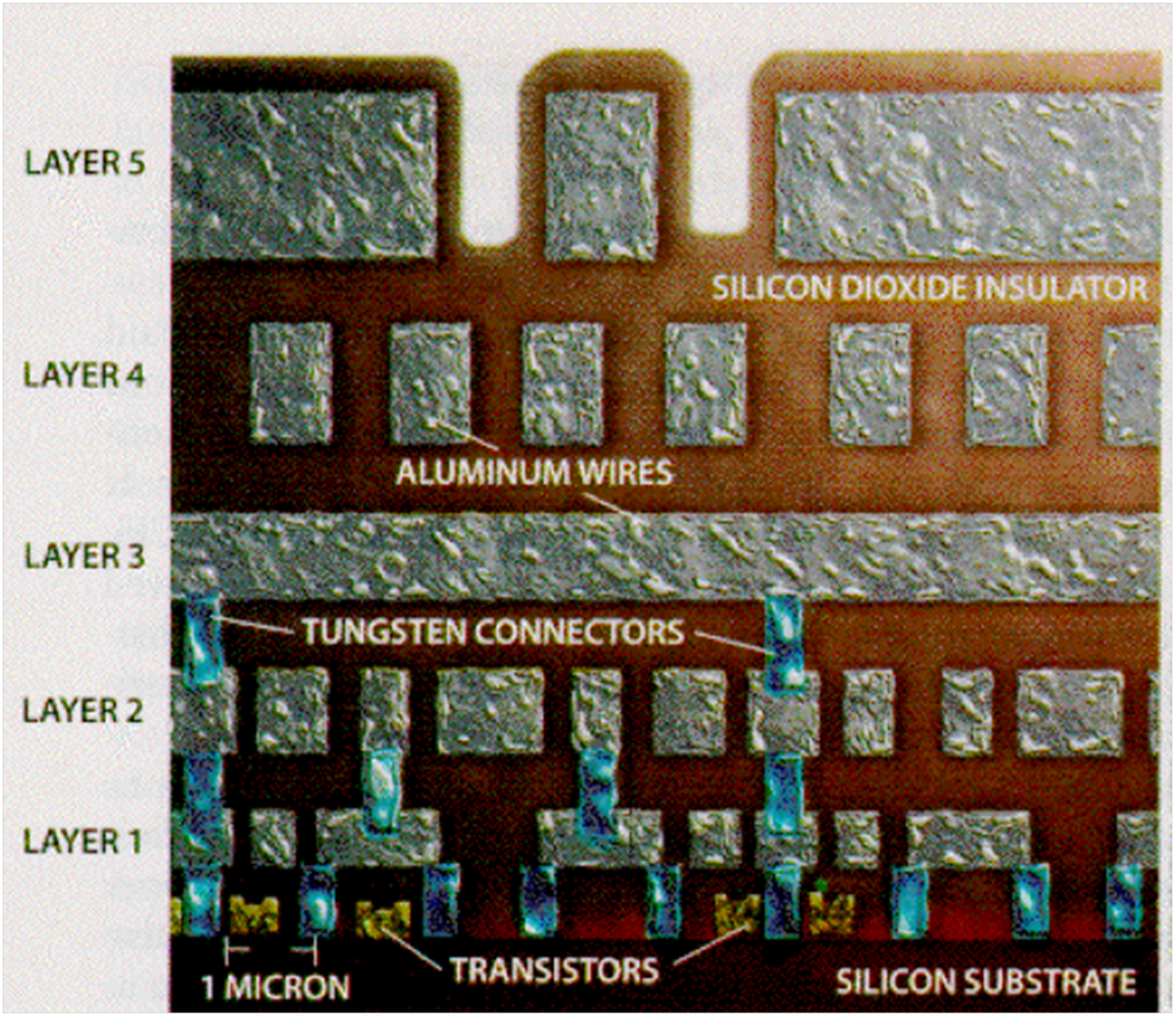
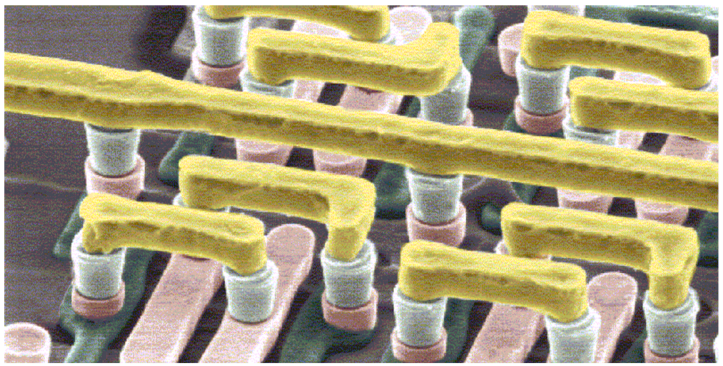
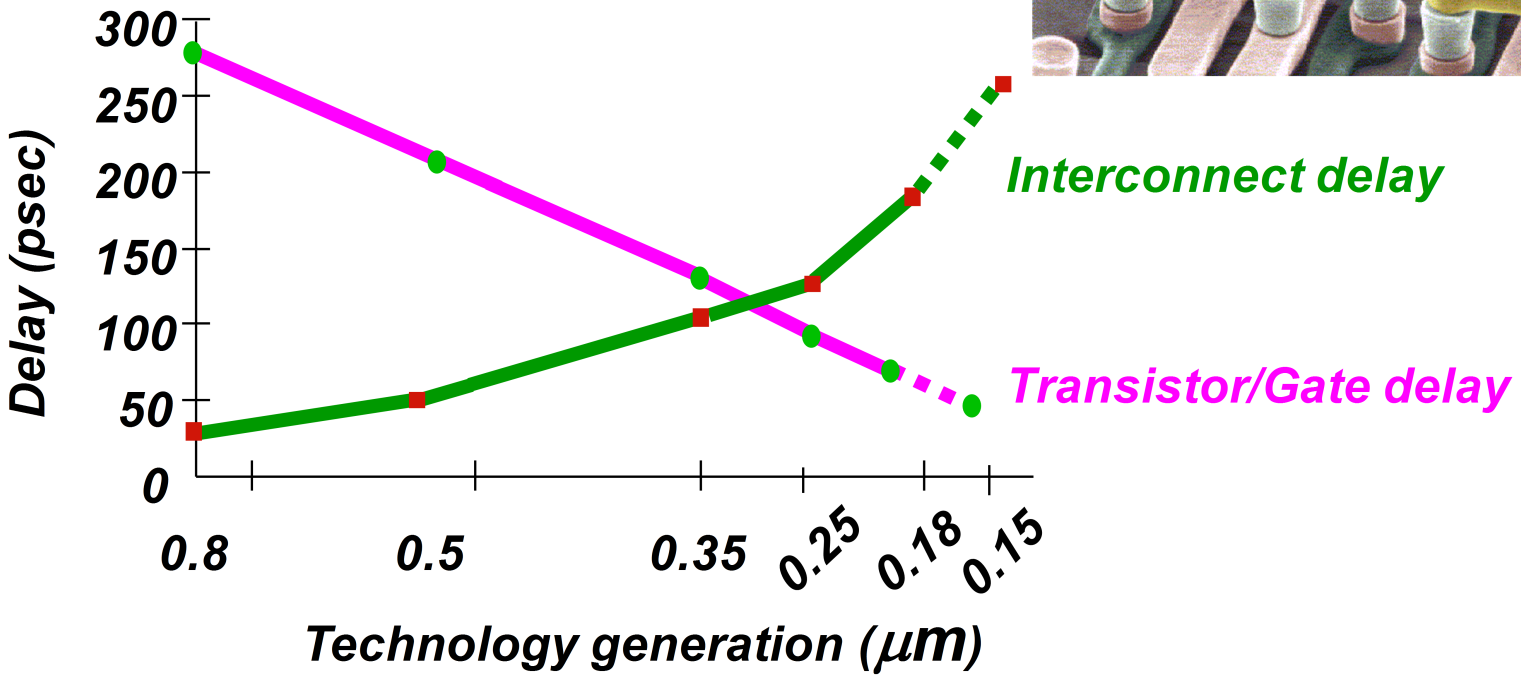


Figure 13: *Cross-Section of A Chip*

Interconnects Dominate





Source: ***Gordon Moore, Chairman Emeritus, Intel Corp.***

Figure 14: *Impact of scale technology to delay*

Why is MOS the dominant technology for VLSI ?

MOS = Metal Oxide Semiconductor

- Smaller size
- Higher degree of integration
- More transistor means more circuit functions
- Cheaper
- Less power consumption

CMOS:Complementary MOS

Means we are using both N-channel and P-channel type enhancement mode Field Effect Transistors (FETs).

PMOS - pull up

NMOS - pull down

Summary: Trend and Challenges

- Performance doubles every 2 years
- Technology scaling by 0.7 per generation
- Speed and Clock distribution
- Complexity: More functions per chip
- Signal Integrity
  + Crosstalk
  + Switching Noises
- Power
  + Distribution
  + Dissipation and IR drop

next .... **Chapter 2: Basic CMOS devices**