

Integrated Circuit Design

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Chapter 4: DIGITAL CMOS CIRCUITS

Outline

- Issues in digital design
- CMOS logic gates
- Flip-flop

Issues in digital design

Challenges and Efforts

Chip designers face a bewildering array of choices:

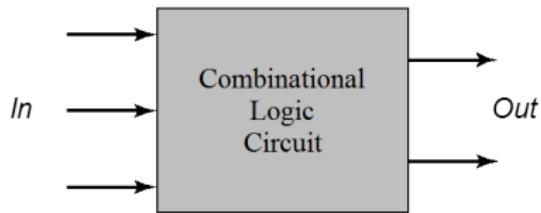
- What is the best **circuit topology** for a function?
- How many stages of logic give **least delay**?
- How wide should the transistors be?

Logical effort is a method to make these decisions

- Uses a simple model of delay
- Allows back-of-the-envelope calculations
- Helps make rapid comparisons between alternatives
- Emphasizes remarkable symmetries

Logic Circuit Classification

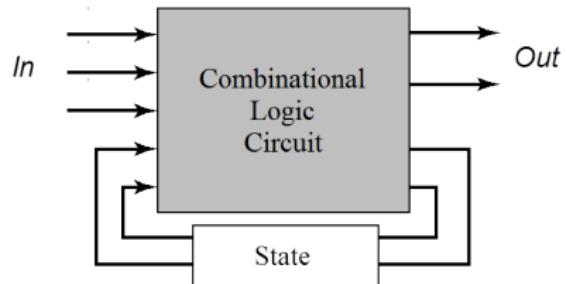
Combinational



$$\text{Output} = f(\text{In})$$

Ex: Logic gates, mux,
decoder, adder

Sequential



$$\text{Output} = f(\text{In}, \text{Previous In})$$

Ex: Registers, counters,
oscillators memory

Logic Styles: Static / Dynamic CMOS circuits.

Static CMOS: Properties

- Full rail-to-rail swing; high noise margins
- Number of Transistor = $2n$ where n is the number of input **least delay**?
- Logic levels not dependent upon the relative device sizes; ratioless
- Always a path to Vdd or Gnd in steady state; low output impedance
- Extremely high input resistance; nearly zero steady-state input current
- No direct path steady state between power and ground; no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors

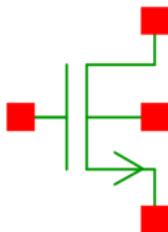
Optimize the design metrics

How to evaluate performance of a digital circuit ?

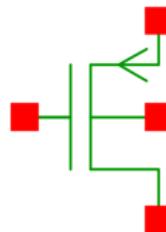
- Cost
- Reliability
- Scalability
- Speed (delay, operating frequency)
- Power dissipation
- Energy to perform a function

Models for Digital design

MOSFET is a simple logic-controlled switch. The PMOS device operates in a complementary way to the NMOS device.



NMOS



PMOS

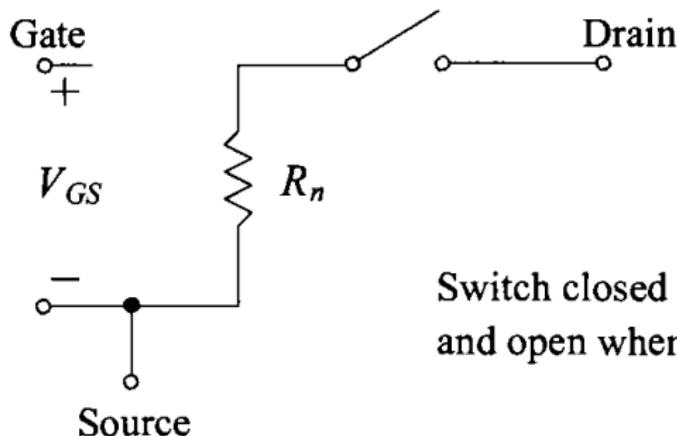
NMOS:

- Turns on when the gate is a logic 1.
- Turns off when the gate is a logic 0.

PMOS:

- Turns on when the gate is a logic 0.
- Turns off when the gate is a logic 1.

Digital MOSFET model

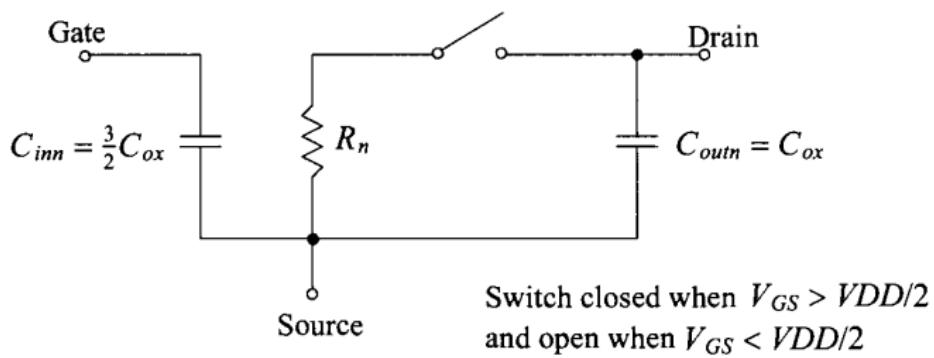
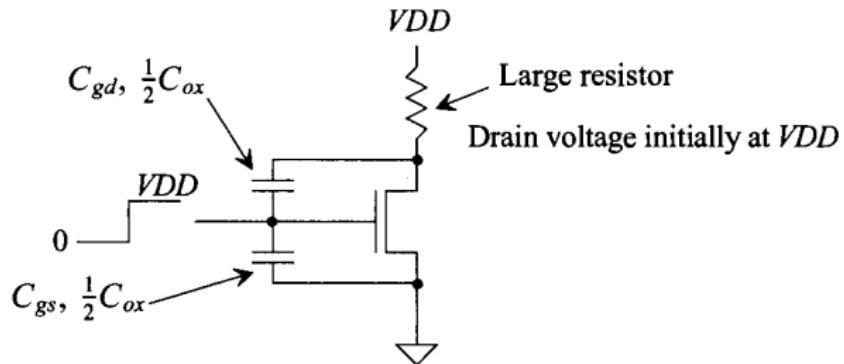


Switch closed when $V_{GS} > VDD/2$
and open when $V_{GS} < VDD/2$

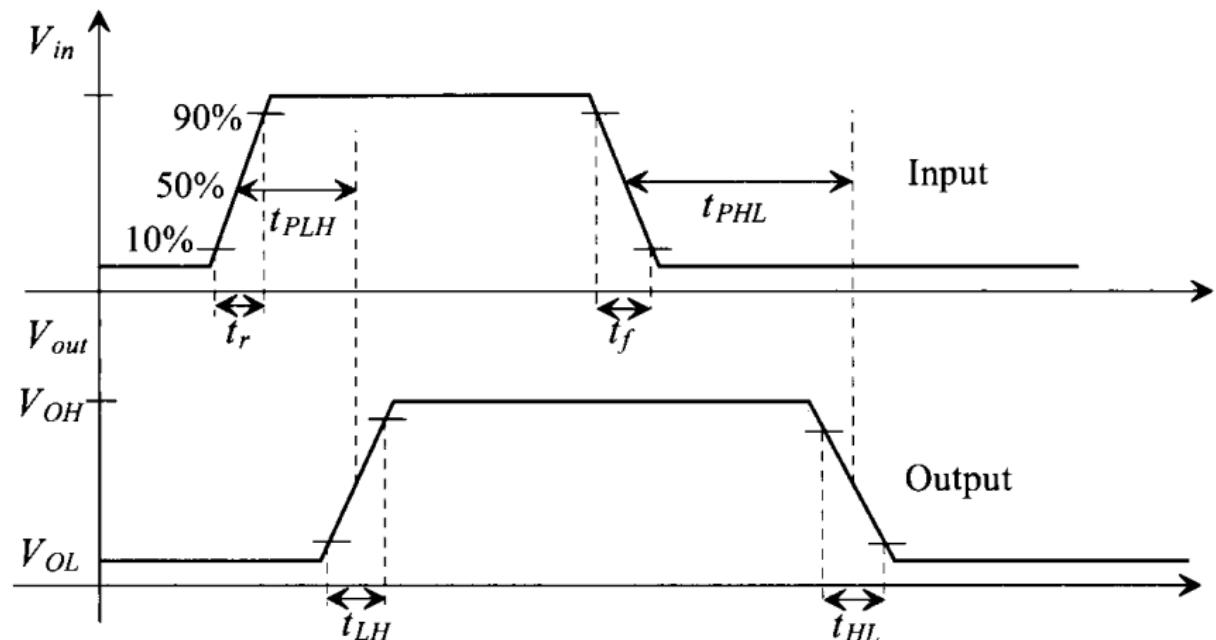
$$R_n = R'_n \times \frac{L}{W}$$

$$R'_n = \frac{V_{DD}}{I_{D,sat}}$$

Digital MOSFET model with capacitive effects

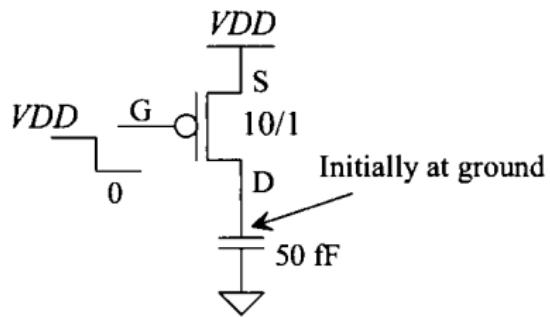
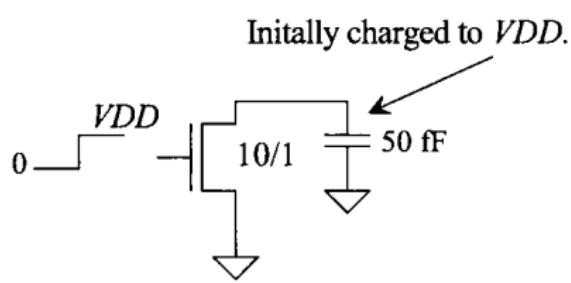


Definition of delays and transition times



Problem

Hand calculations, estimate the rise, fall and delay times of the following circuits. Compare to SPICE simulation.



CMOS logic gates

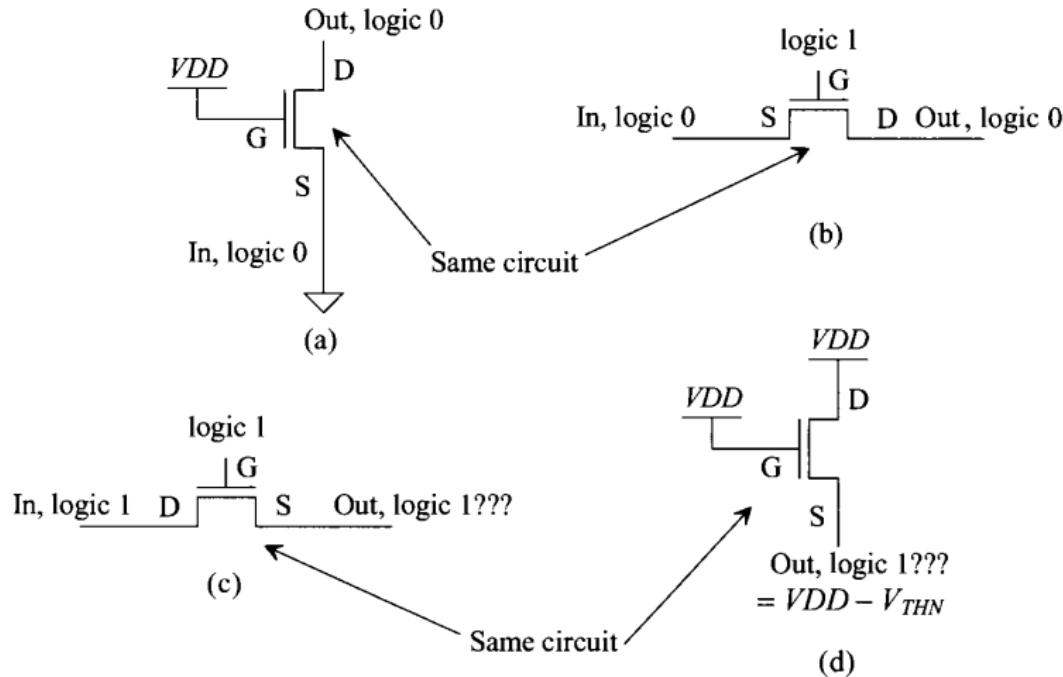
- Pass gate and transmission gate
- Inverter and Ring oscillator
- NOR
- NAND

MOSFET pass gate and transmission gate

MOSFET pass gate

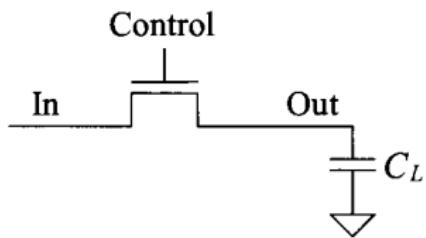
Logic flow through the PG can be bi-directional.

NMOS switch as a pass gate

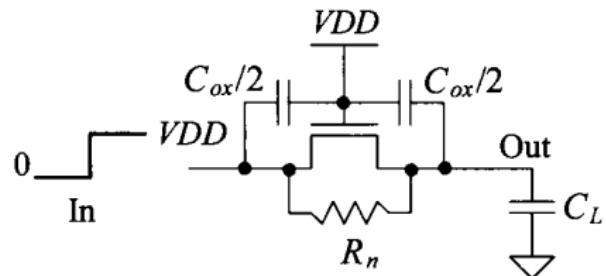


Delay through a pass gate

Estimate the delay through an NMOS pass gate.



(a) Delay from the input to the output through a pass gate.



(b) The capacitances and effective resistance when turning the MOSFET on with an input 1.

MOSFET pass gate

- * NMOS device is good at passing a "0".
- * PMOS device is good at passing a "1".

PG is used as a delay.

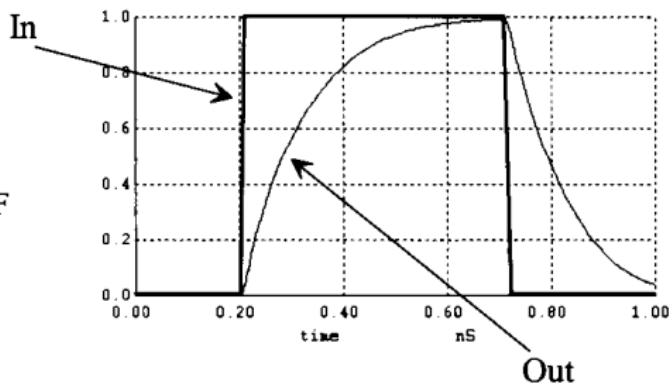
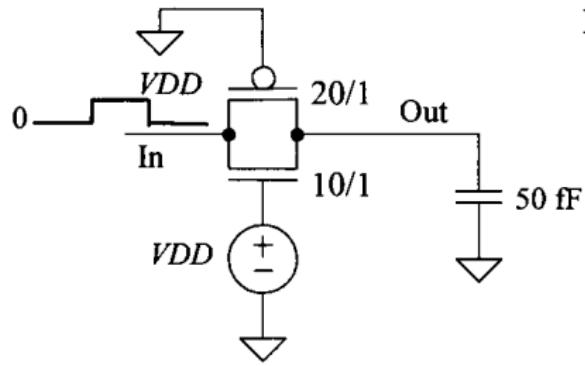
MOSFET transmission gate



The benefit of using the TG is its rail-to-rail output swing.

MOSFET transmission gate

TG circuit and simulation result.



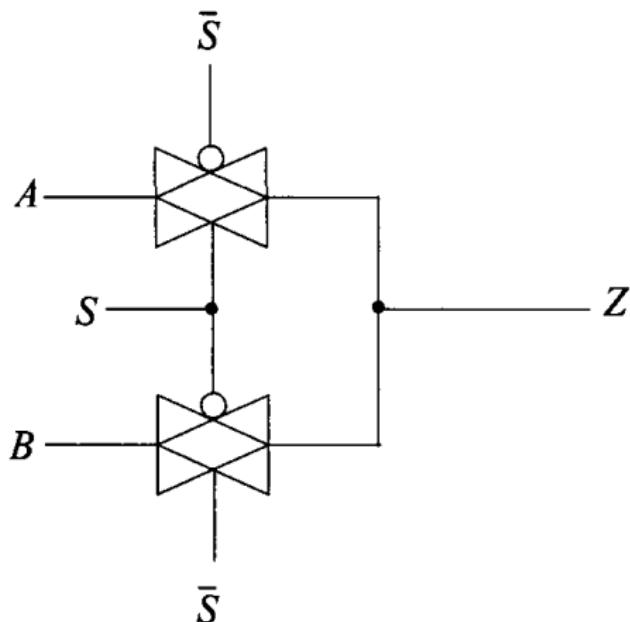
TG: applications

- Path selector
- MUX/DEMUX
- Static gates

Example: Path selector

The output of the path selector:

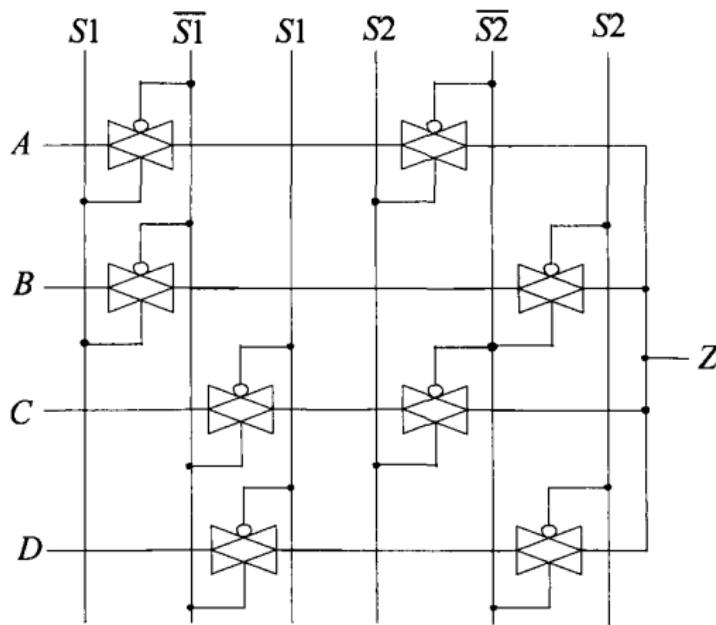
$$Z = AS + BS\bar{S}$$



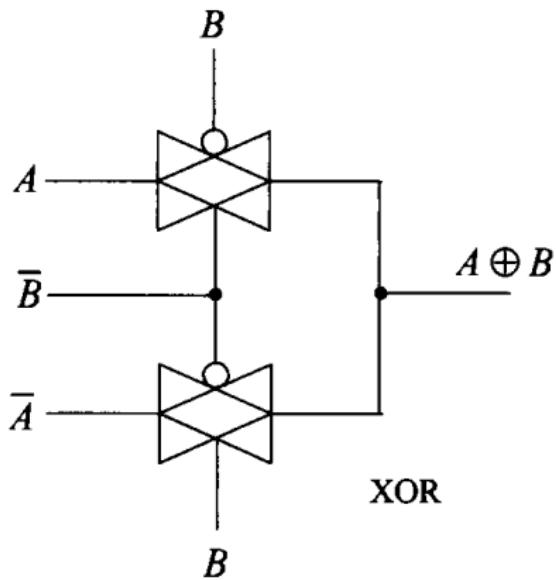
Example: MUX/DEMUX

The output of a 4-to-1 MUX:

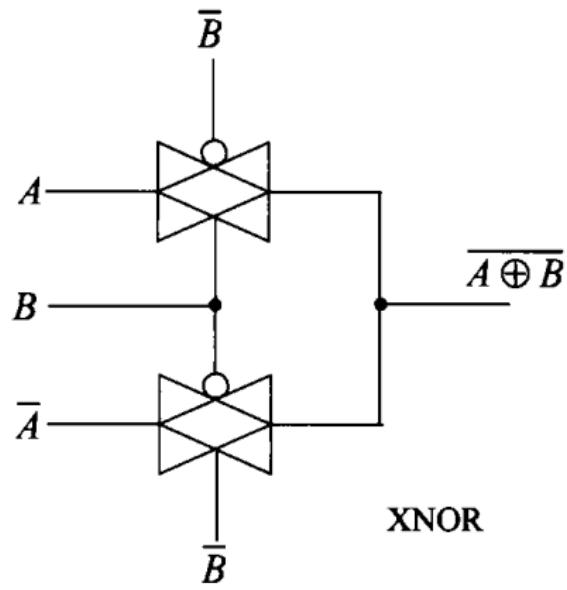
$$Z = A(S_1 \cdot S_2) + B(S_1 \cdot \overline{S_2}) + C(\overline{S_1} \cdot S_2) + D(\overline{S_1} \cdot \overline{S_2})$$



Example: XOR/XNOR gate



XOR

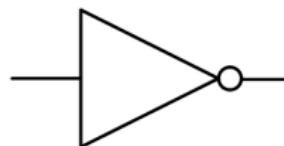
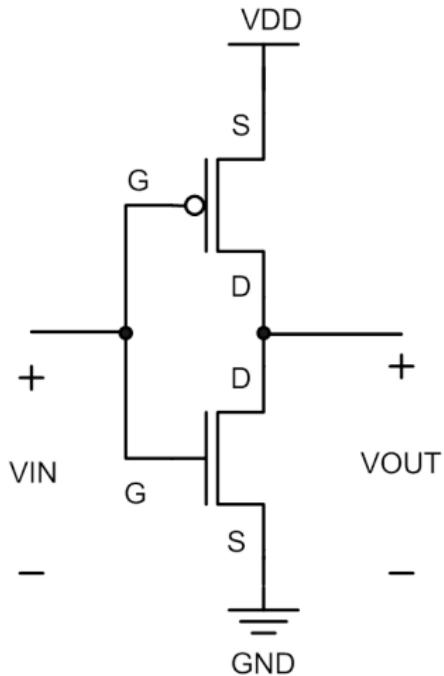


XNOR

CMOS Inverter

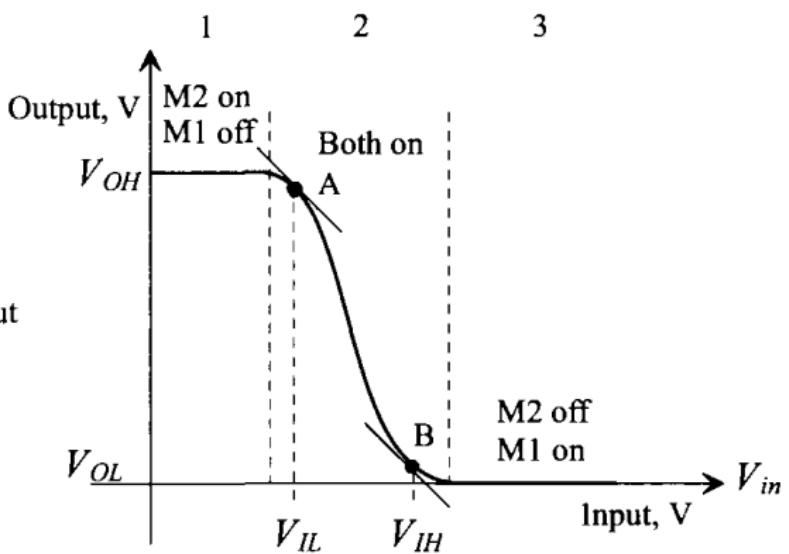
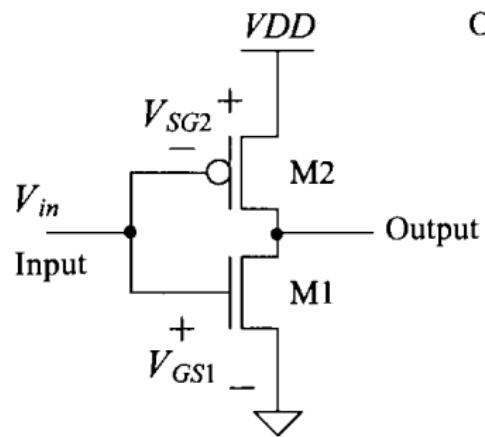
This is a basic block for digital circuit design. The inverter performs the logic operation of A to \bar{A}

CMOS Inverter: DC analysis



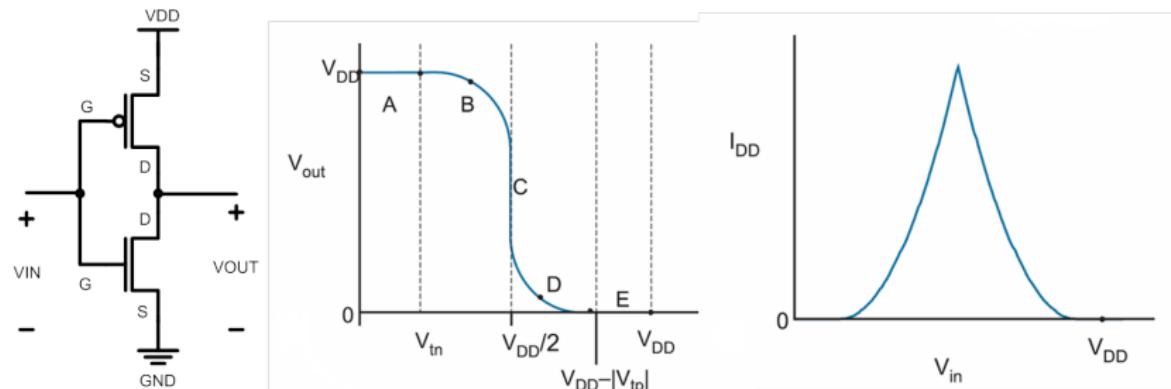
$$\begin{aligned}V_{GSN} &= V_{IN} \\V_{DSN} &= V_{OUT} \\|V_{GSP}| &= V_{DD} - V_{IN} \\|V_{DSP}| &= V_{DD} - V_{OUT} \\I_{DSP} &= I_{DSN}\end{aligned}$$

CMOS Inverter: Voltage Transfer Curve - VTC



CMOS Inverter Analysis

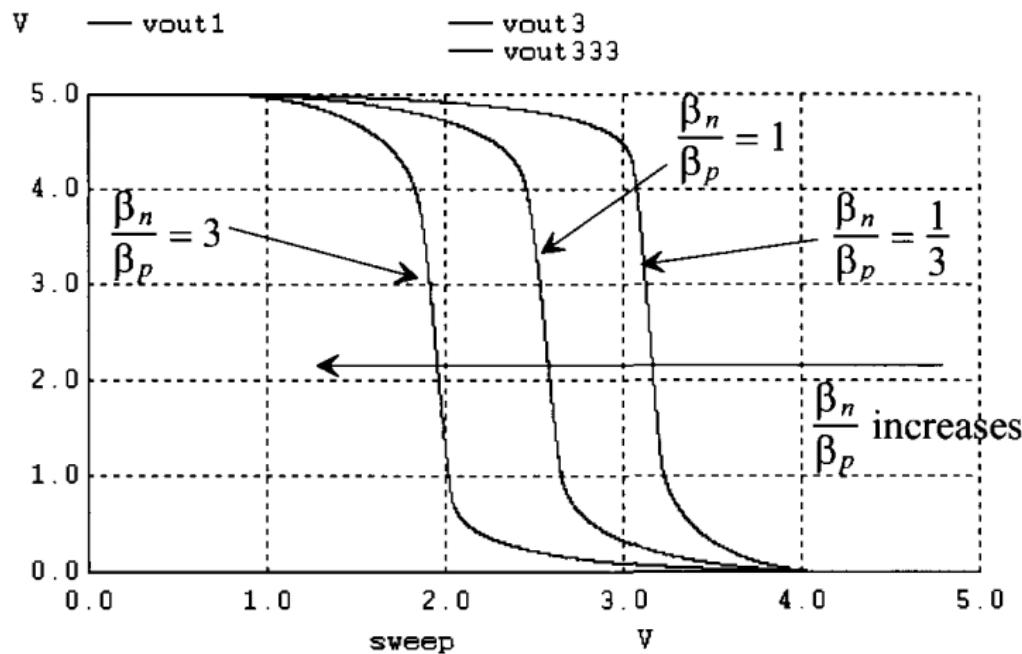
Graphical Method



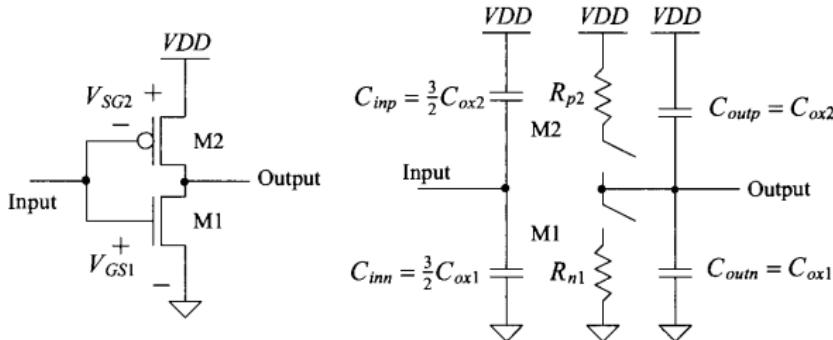
Region	Condition	p-device	n-device	Output
A	$0 \leq V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \leq V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \leq V_{DD} - V_{tp} $	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - V_{tp} $	cutoff	linear	$V_{out} = 0$

CMOS Inverter: Sizing

Sizing the inverter changes the switching point voltage



CMOS Inverter: switching characteristics



* The effective input capacitance of the inverter is:

$$C_{in} = C_{inn} + C_{inp} = \frac{3}{2}(C_{ox1} + C_{ox2})$$

* The effective output capacitance of the inverter is:

$$C_{out} = C_{outn} + C_{outp} = C_{ox1} + C_{ox2}$$

* The propagation delays:

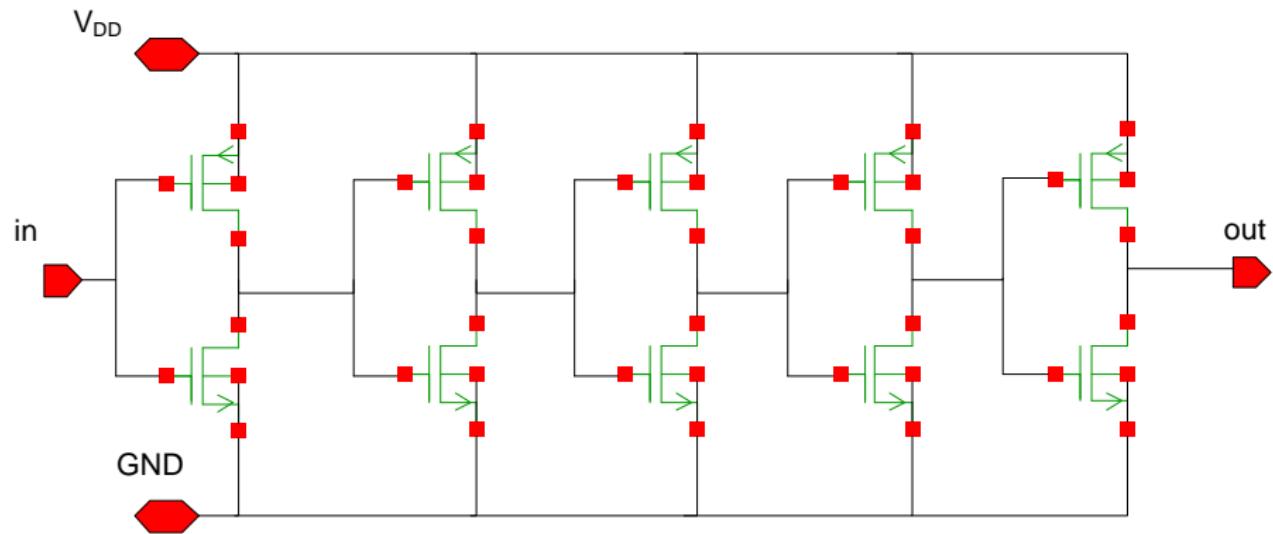
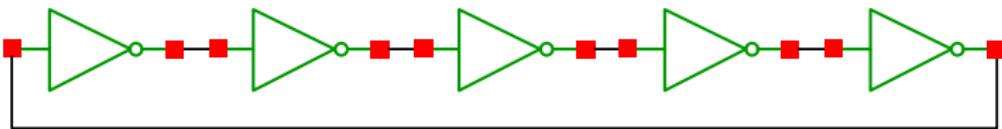
$$t_{PLH} = 0.7 \cdot R_{p2} \cdot C_{out} \quad \text{and} \quad t_{PHL} = 0.7 \cdot R_{n1} \cdot C_{out}$$

Ring oscillator

An odd number of inverters could form a closed loop with positive feedback. It is called a ring oscillator, whose frequency is given by:

$$f_{osc} = \frac{1}{n.(t_{PHL} + t_{PLH})}$$

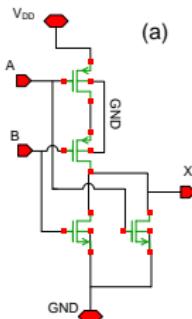
Example a five-stage ring oscillator



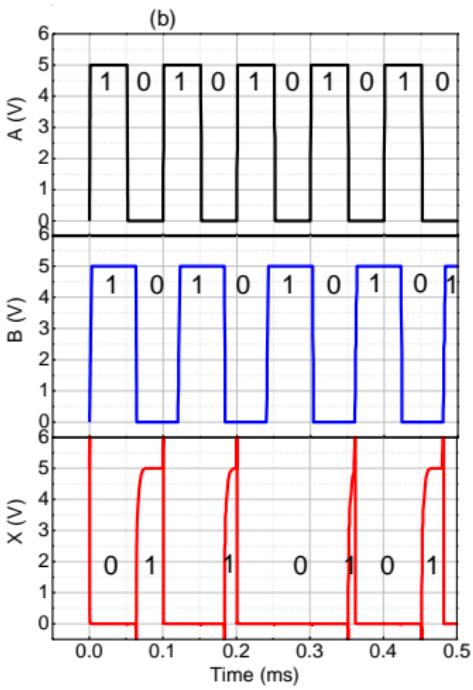
NOR and NAND gates

2-input NOR

$$X = \overline{A + B}$$

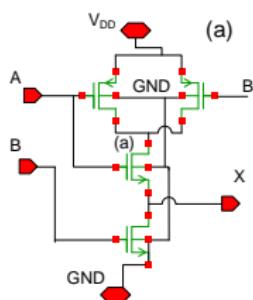


A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

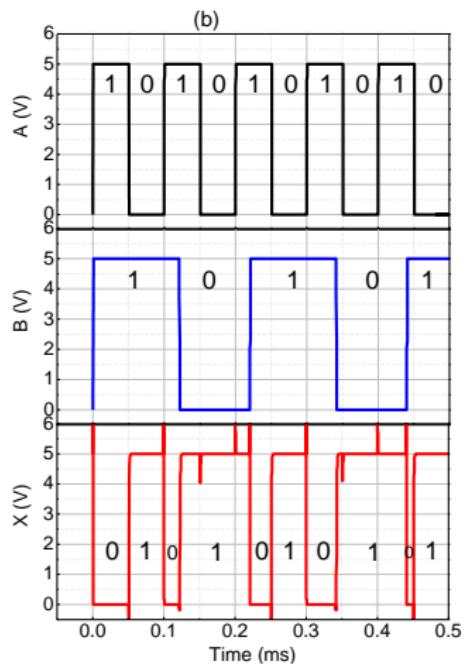


2-input NAND

$$X = \overline{A \cdot B}$$



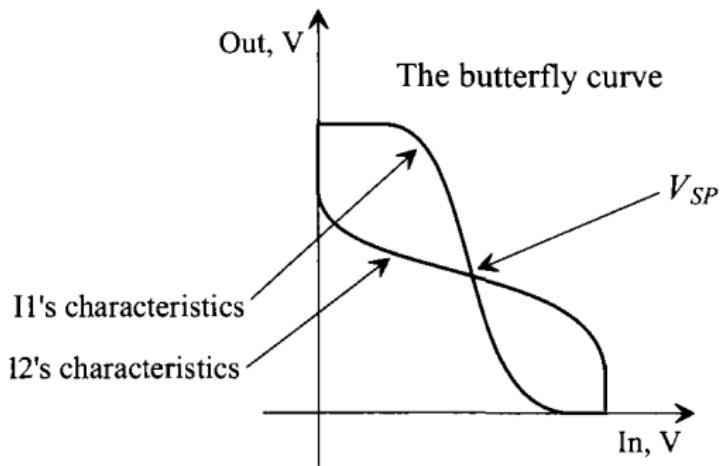
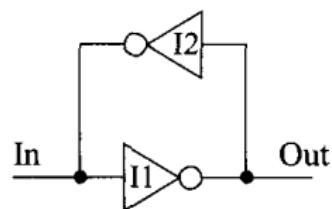
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0



Flip-flop

FF: introduction

A FF is a storage circuit that changes states on the rising or falling edge of a clock signal.
FFs are based on logic gates and clock.



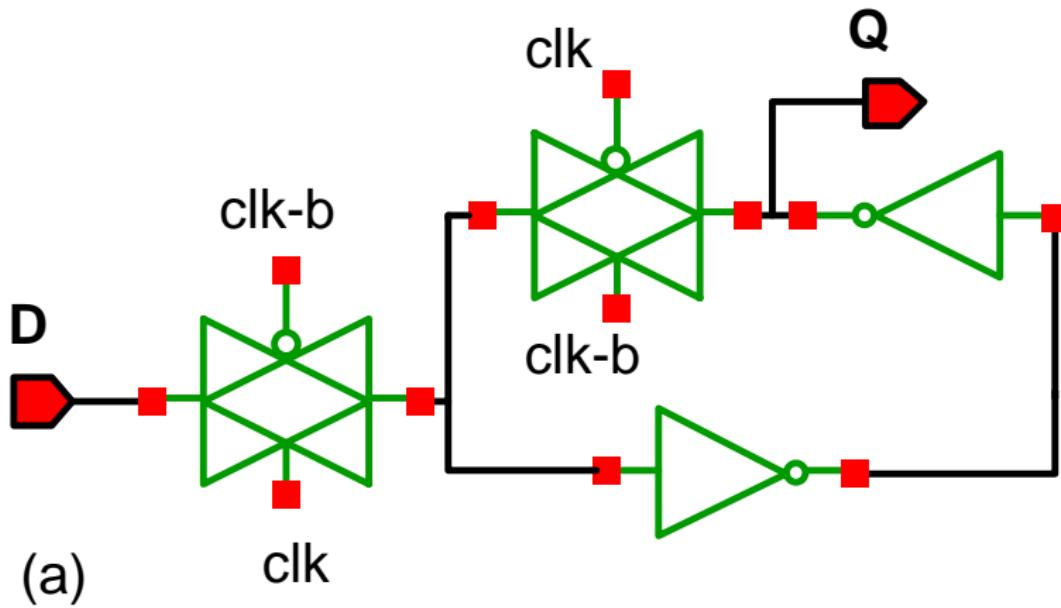
A latch and its characteristics

FF: applications

- Store one bit
- Register
- Memory

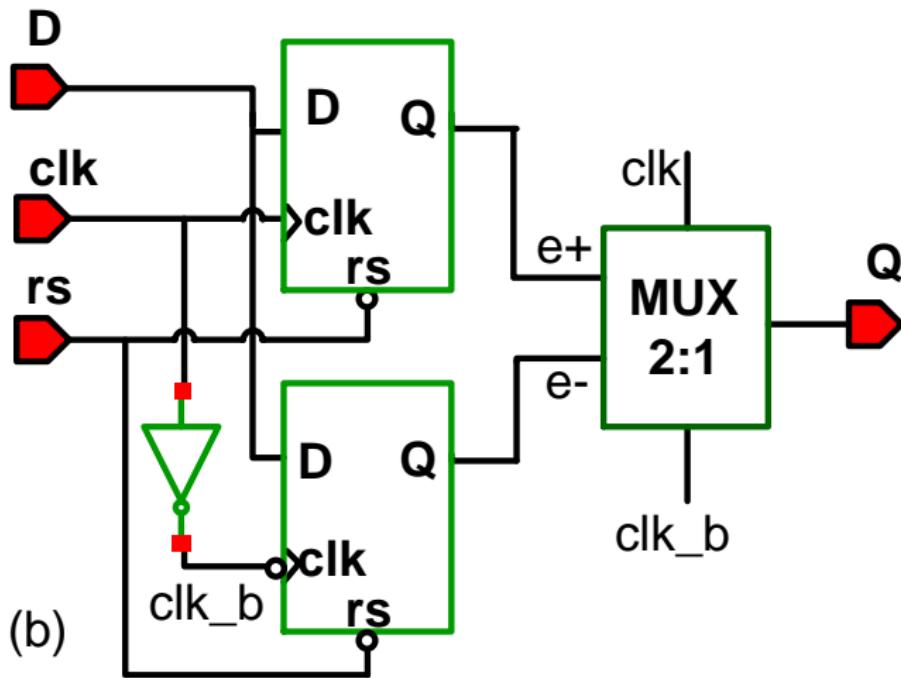
D flip-flop

Single-edge triggered D-FF



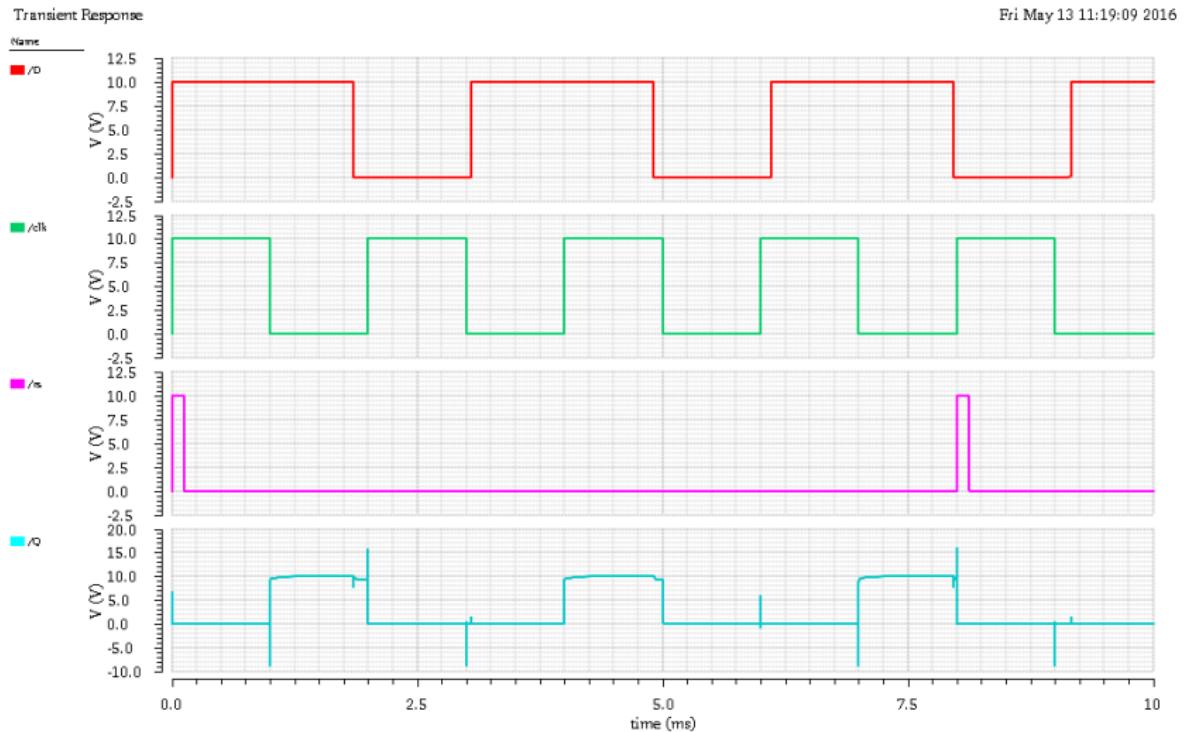
D flip-flop

Double-edge triggered D-FF



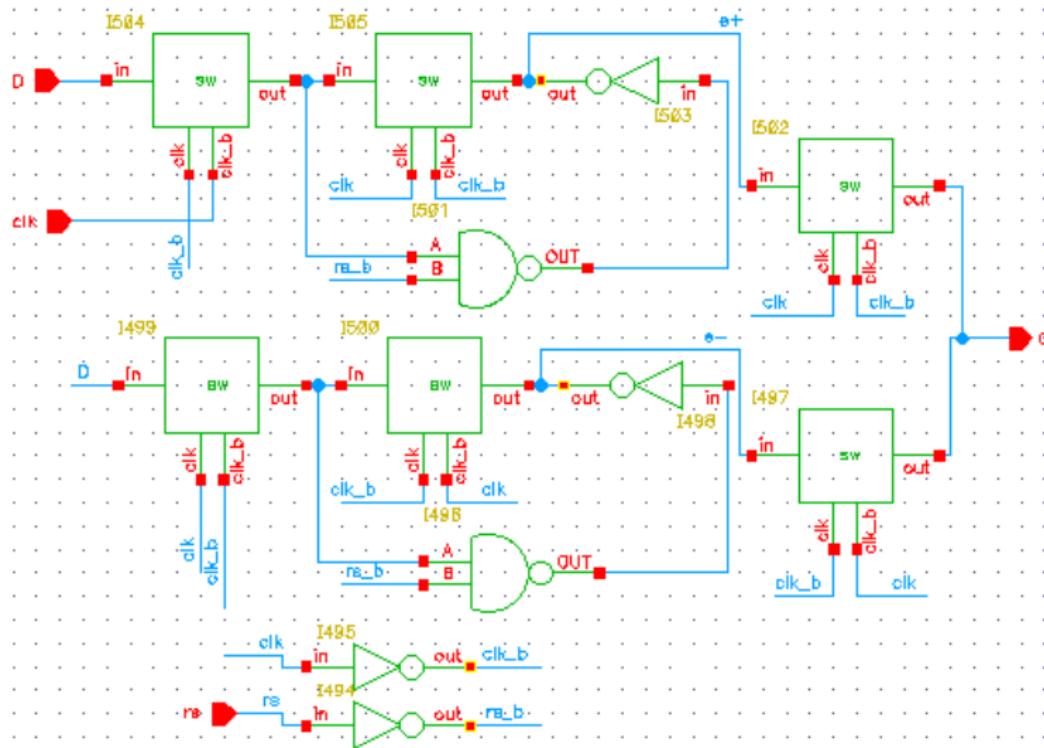
Example 1

Waveforms of single or double-edge D-FF ?



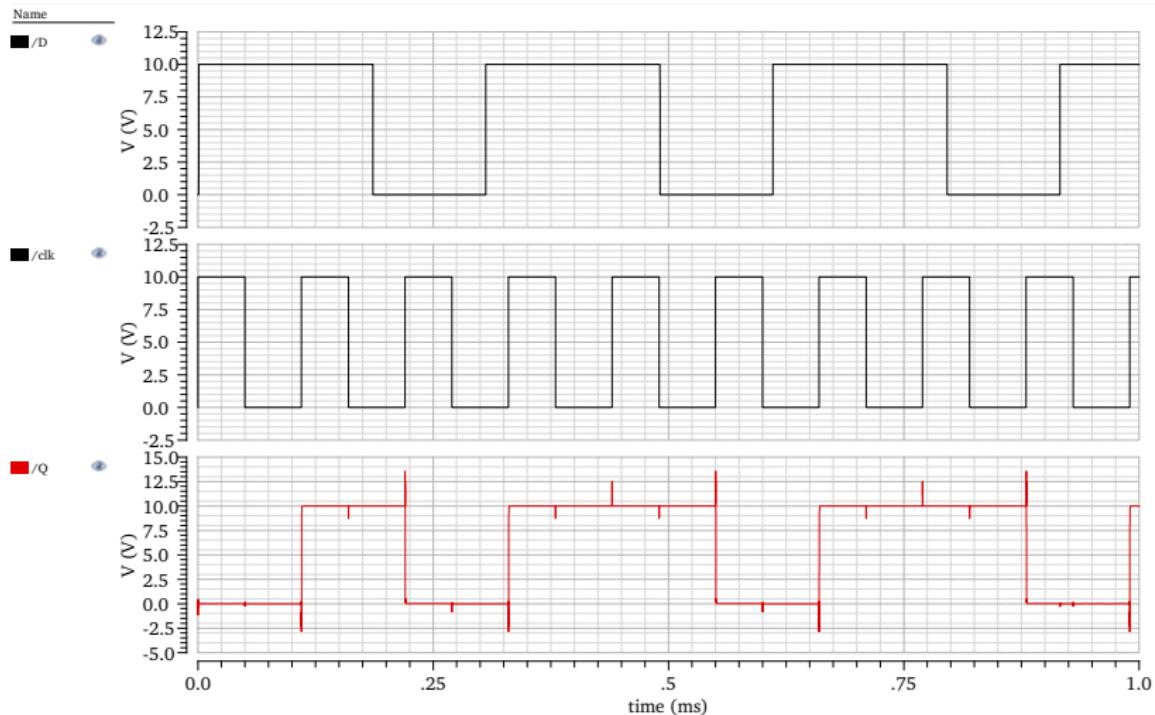
Example 1: circuit

Double-edge D-FF



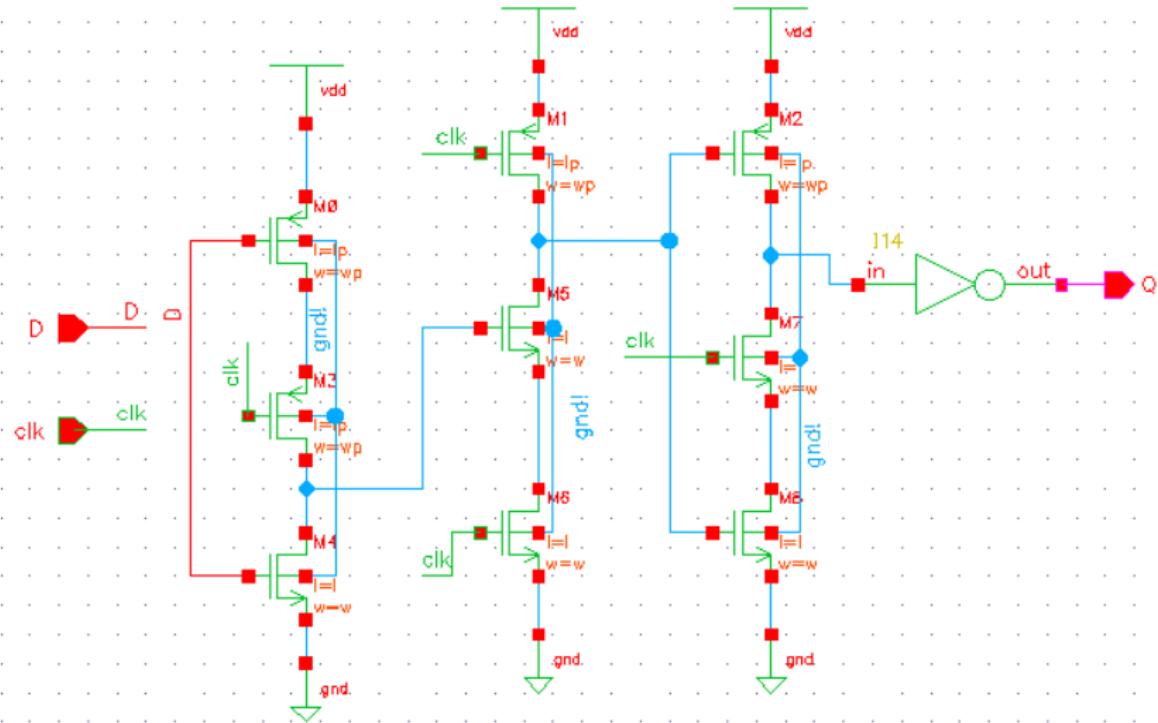
Example 2

Waveforms of single or double-edge D-FF ?



Example 2: circuit

Single-edge D-FF



THE END