



# Integrated Circuit Design

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## Chapter 2: **BASIC CMOS DEVICES**

# Warm up !!!!!

Why IC ?

# Warm up !!!!!

Why IC ?

IC technology nodes ?

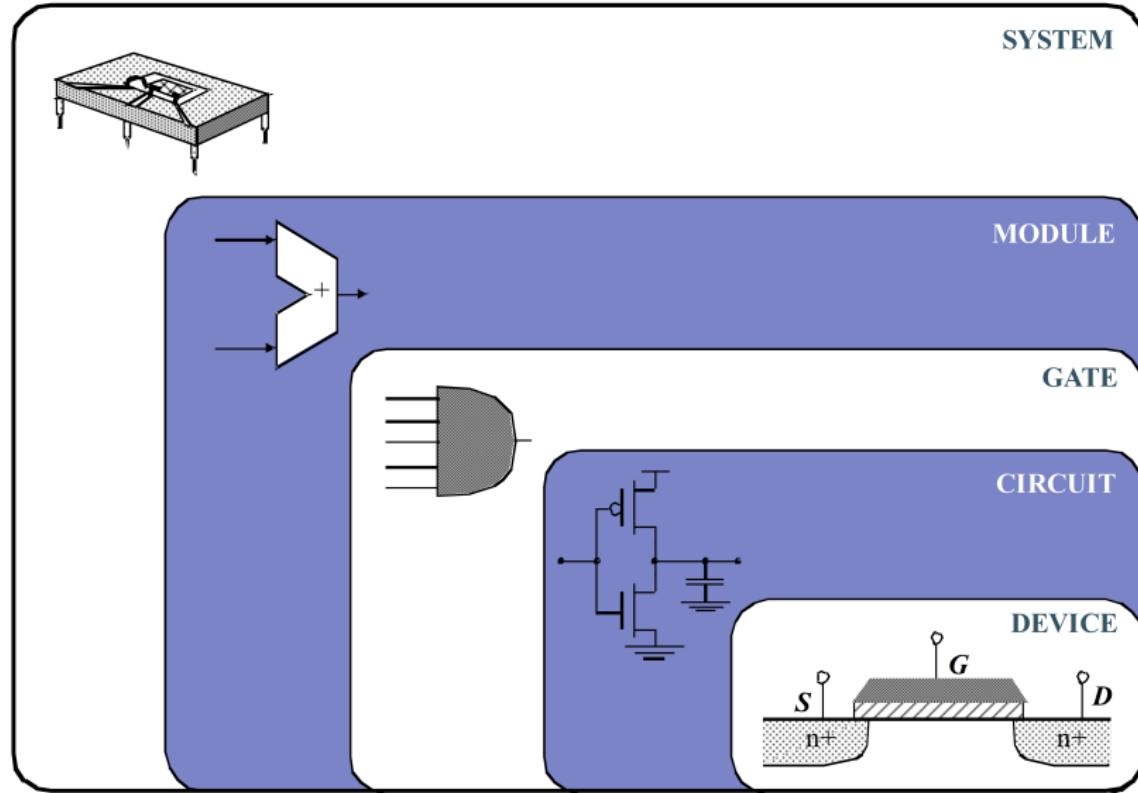
# Warm up !!!!

Why IC ?

IC technology nodes ?

Why CMOS ?

# Levels in circuit design



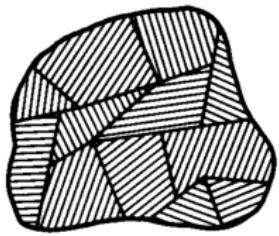
# Outline

- Basic CMOS device physic
- MOS theory.
- NMOS & PMOS
- Small-signal model for FET
- MOS Resistor and Capacitor

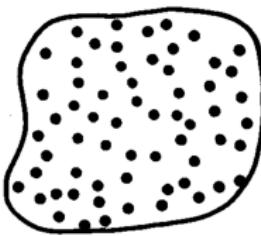
# Basic CMOS device physic

# What is a Semiconductor?

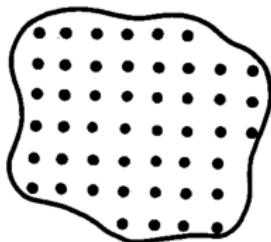
- Low resistivity => “conductor”
- High resistivity => “insulator”
- Intermediate resistivity => “semiconductor”  
conductivity lies between that of conductors and insulators  
generally crystalline in structure for IC devices



polycrystalline



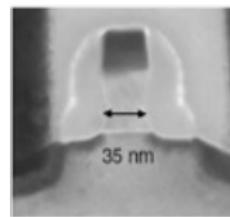
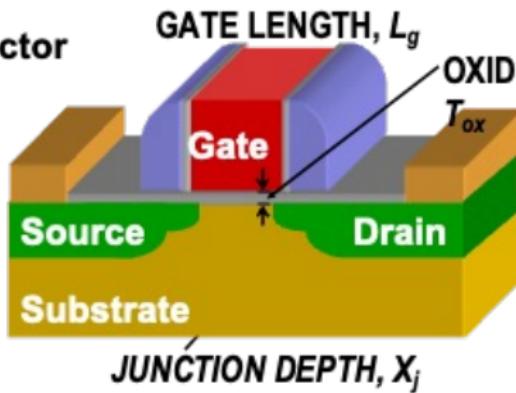
amorphous



crystalline

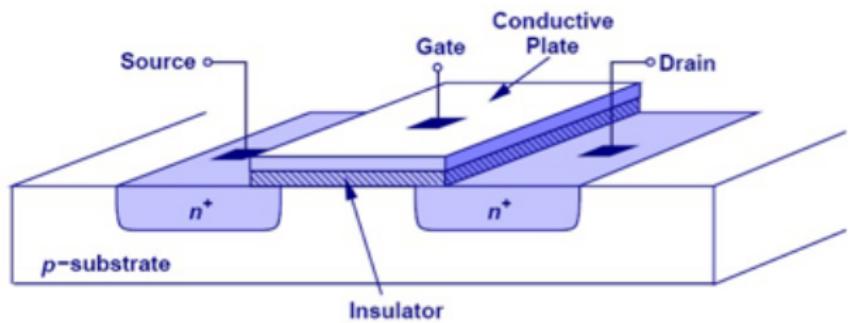
# MOS: Structure

**Metal-Oxide-Semiconductor  
Field-Effect Transistor:**

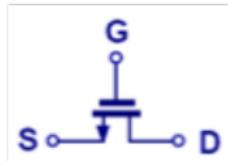


M. Bohr, Intel Developer Forum, September 2004

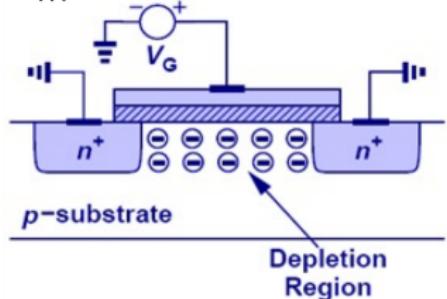
# MOS: Structure



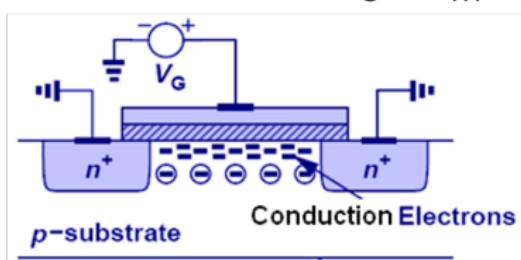
Circuit symbol



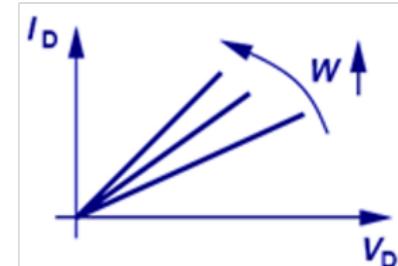
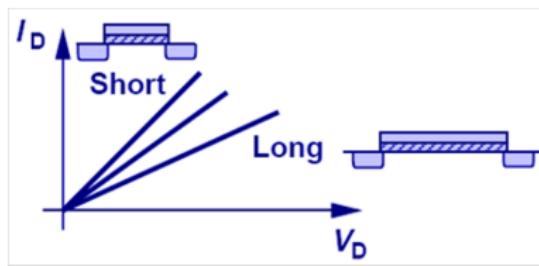
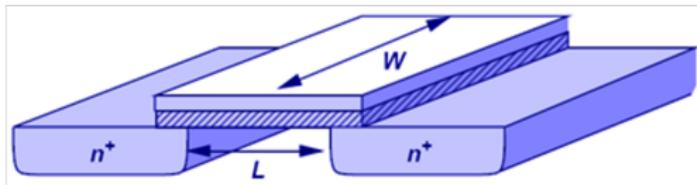
$$V_G < V_{TH}$$



$$V_G \geq V_{TH}$$



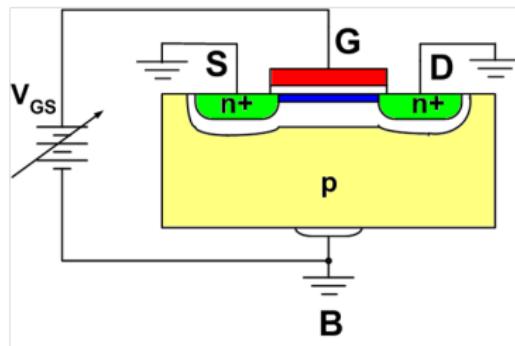
# Channel Length and Width Dependence



Shorter channel length and wider channel width each yield lower channel resistance, hence larger drain current.

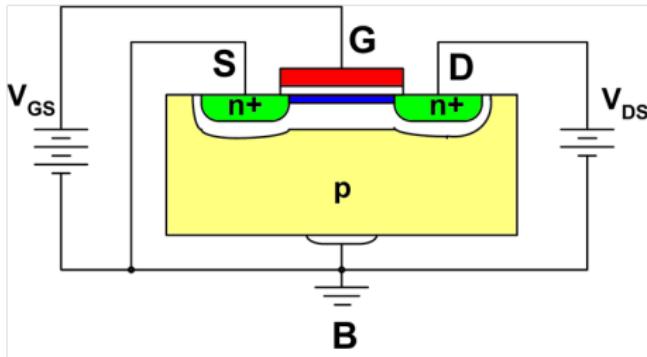
Increasing  $W$  also increases the gate capacitance, however, which limits circuit operating speed

# MOS: Operation



- $V_{GS} < 0$  accumulation : holes are attracted to area beneath gate. **MOS is OFF**
- $0 < V_{GS} < V_{TH}$  depletion: holes are repelled from layer beneath gate while electron are attracted. **MOS is OFF**
- $V_{GS} > V_{TH}$  inversion: conductive layer of electrons formed beneath the gate i.e. “n-channel” **MOS is ON**

# Operation: Linear Mode



- $V_{GS} > V_{TH}$  and  $V_{DS} > 0$  current  $I_{DS}$  flows from drain to source.
- For a small  $V_{DS}$  current  $I_{DS}$  is a linear function of both  $V_{GS}$  and  $V_{DS}$

# Operation: Linear Mode

For Long Channel devices: when  $V_{DS} < V_{GS} - V_{TH}$

$$I_{DS} = k_n' \frac{W}{L} \left[ (V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$k_n' = \mu_n C_{ox} = \frac{\mu_n \epsilon_{ox}}{t_{ox}}$$

$$V_{TH} = V_{TH0} + \gamma (\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|})$$

$k_n'$  :process transconductance parameter

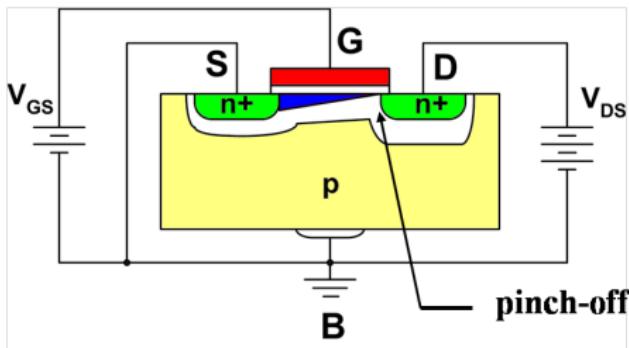
$\mu_n$  :electron mobility  
Độ linh động của điện tử

$\epsilon_{ox}$  :dielectric constant of SiO<sub>2</sub>  
hằng số điện môi

$t_{ox}$  :oxide thickness  
độ dày của lớp oxit

- For **small**  $V_{DS}$ , there is a **linear dependence** between  $V_{DS}$  and  $I_{DS}$  (ignore quadratic term), hence the name **resistive** or **linear** region

# Operation: Saturation Mode



- As  $V_{DS} > V_{GS} - V_{TH}$  the depletion region at drain grows resulting in effective channel length L decreases
- When charge in the inversion layer = 0, number of mobile electrons at drain reduces drastically. This is pinch-off
- Number of carriers arriving at pinch-off point from source remain the same. Thus current  $I_{DS}$  is constant.

# Operation: Saturation Mode

For Long Channel devices: when  $V_{DS} \geq V_{GS} - V_{TH}$

$$I_{DS} = \frac{k' W}{2 L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

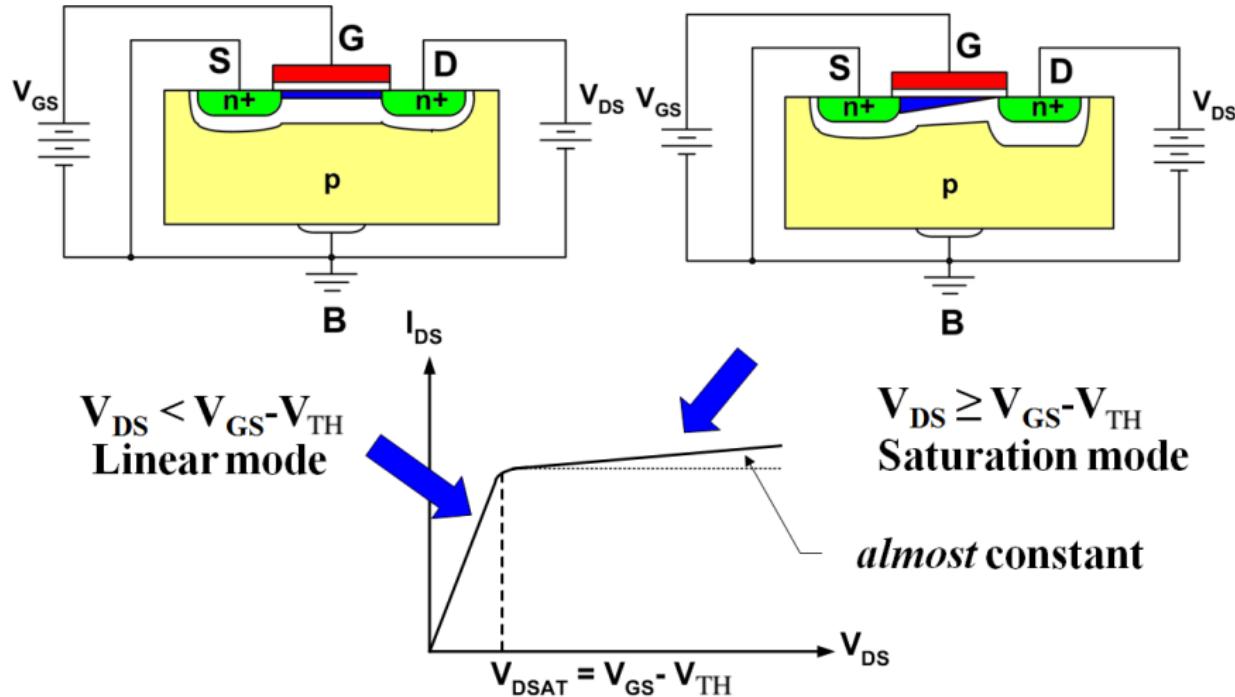
$\lambda$  :channel length modulation parameter

$(1 + \lambda V_{DS})$  accounts for the effective length of the conductive channel that reduces with further increases in  $V_{DS}$ ,

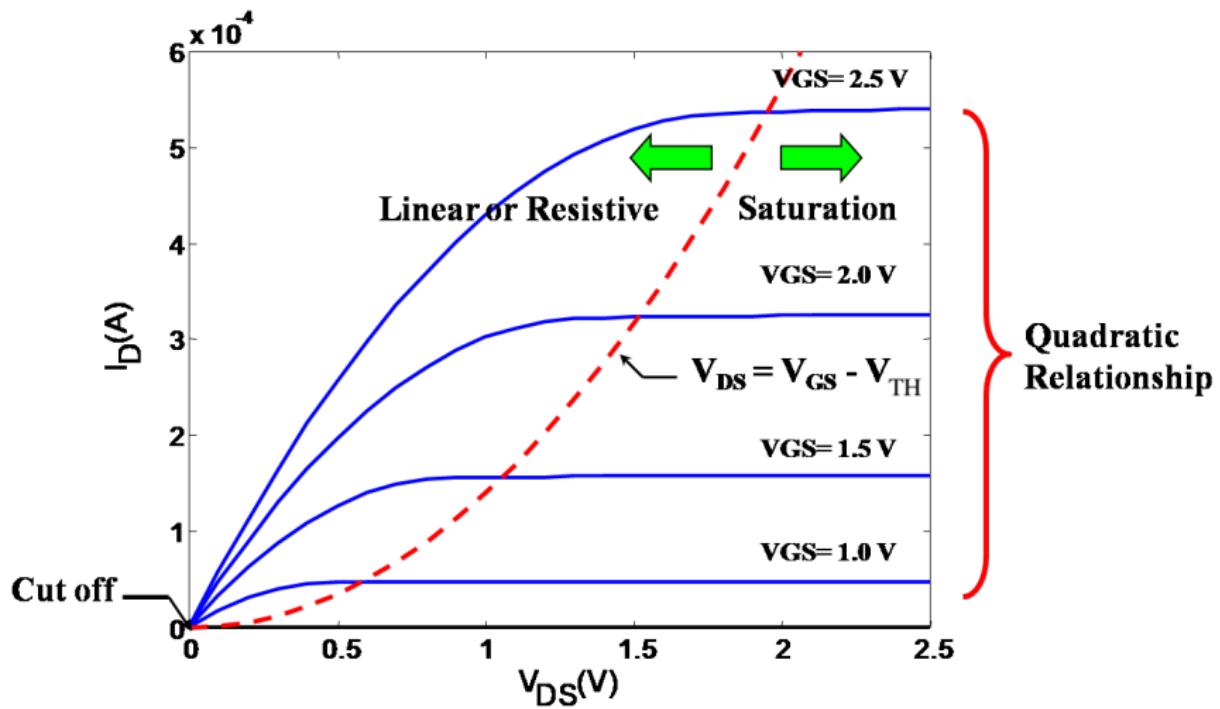
for digital design:

$$I_{DS} = \frac{k' W}{2 L} (V_{GS} - V_{TH})^2$$

# Long Channel I-V Plot



# Long Channel I-V Plot



NMOS transistor,  $0.25\text{ }\mu\text{m}$ ,  $L = 10\text{ }\mu\text{m}$ ,  $W/L = 1.5$ ,  $V_{DD} = 2.5\text{V}$ ,  $V_{TH} = 0.4\text{V}$

# Long-channel devices (NMOS)

$$V_{DSAT} = V_{GS} - V_{TH}$$

**Linear:**  $V_{DS} < V_{GS} - V_{TH}$

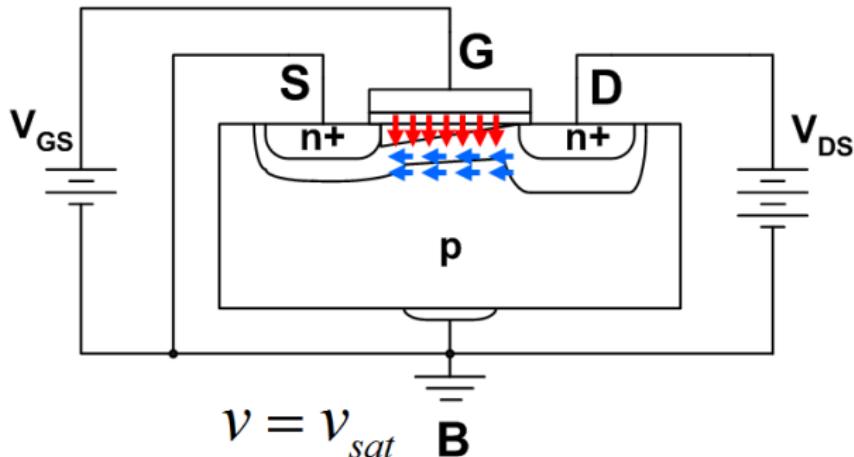
$$I_{DS} = k' \frac{W}{L} [(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2}]$$

**Saturation:**  $V_{DS} \geq V_{GS} - V_{TH}$

$$I_{DS} = \frac{k'}{2} \frac{W}{L} (V_{GS} - V_{TH})^2$$

# MOS Short Channel

$L \ll 1\mu\text{m}$



- Vertical Field:  $E_z = \frac{V_G}{t_{ox}}$  max@  $V_G = V_{DD}$
- Horizontal Field:  $E_y \cong \frac{V_{DS}}{L}$  max@  $V_{DS} = V_{DD}$

Both fields have effects on carrier mobility:  $\mu$

# Short-channel devices (NMOS)

$$V_{DSAT} = \frac{(V_{GS} - V_T)E_C L}{(V_{GS} - V_T) + E_C L}$$

**Linear:**  $V_{DS} < \frac{(V_{GS} - V_T)E_C L}{(V_{GS} - V_T) + E_C L}$

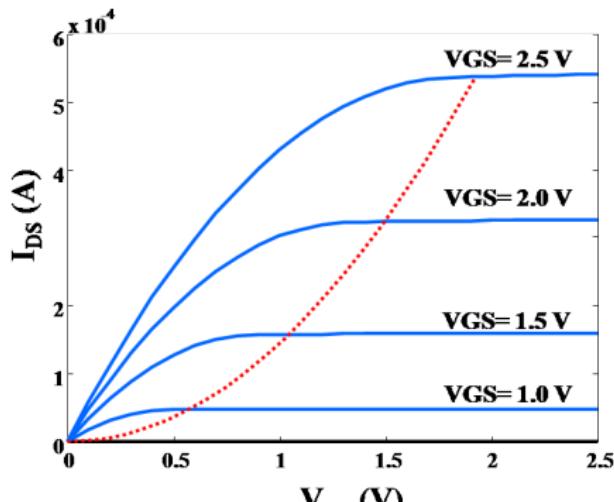
$$I_{DS} = \frac{W}{L} \cdot \frac{\mu_e C_{ox}}{1 + \frac{V_{DS}}{E_C L}} \cdot (V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$$

**Sat:**  $V_{DS} \geq \frac{(V_{GS} - V_T)E_C L}{(V_{GS} - V_T) + E_C L}$

$$I_{DS} = Wv_{sat}C_{ox} \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_C L} (1 + \lambda V_{DS})$$

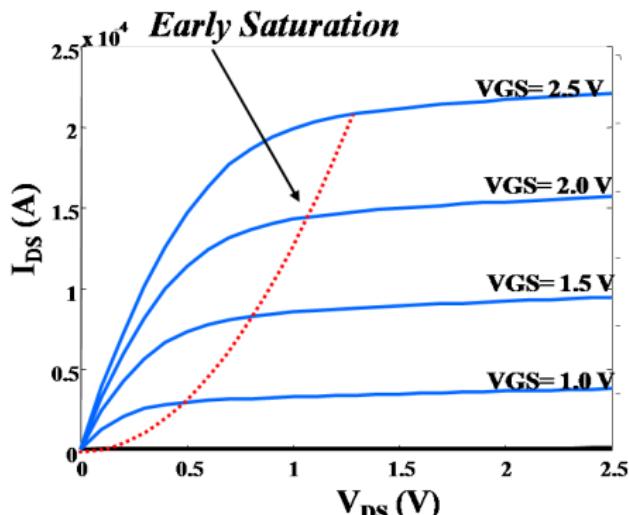
$$V_T \sim V_{TH}$$

# Long channel vs short channel



Long Channel ( $L = 10 \mu\text{m}$ )

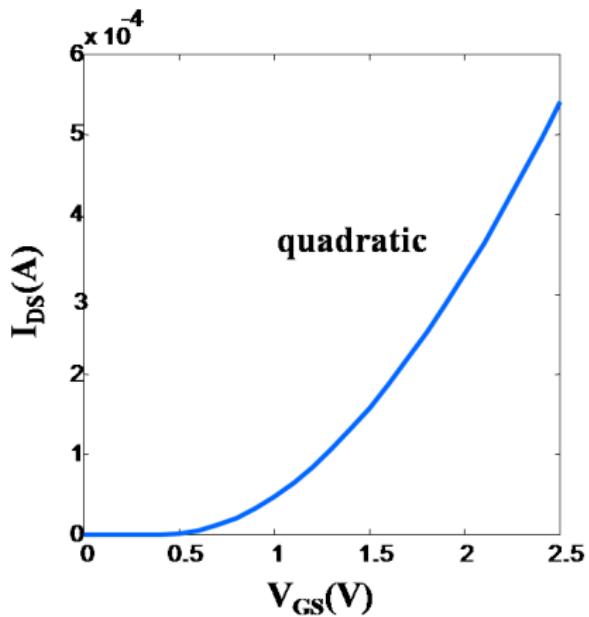
**Quadratic** dependent on  $V_{GS}$



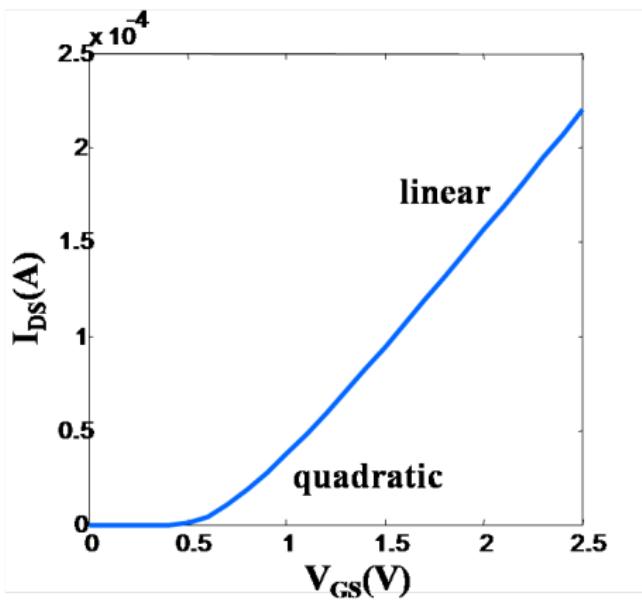
Short Channel ( $L = 0.25 \mu\text{m}$ )

**Linear** dependent on  $V_{GS}$

# Long channel vs short channel



Long Channel



Short Channel

## Example 1

**Compute the saturation current per micron width for 0.13  $\mu m$  technology.**

Given  $L = 100 \text{ nm}$ ,  $t_{ox} = 22^{-10}$ ,  $V_{TN} = 0.4 \text{ V}$ ,

$V_{TP} = -0.4 \text{ V}$ ,  $V_{DD} = 1.2 \text{ V}$

Use  $v_{sat} = 8 \times 10^6 \text{ cm/s}$ ,

$E_{CN} = 6 \times 10^4$ ,  $E_{CP} = 24 \times 10^4 \text{ V/cm}$ .

# Solution

Example compute the saturation *current per micron width* for 0.13 $\mu\text{m}$  technology. Given L = 100nm,  $t_{\text{ox}} = 22 \text{ \AA}$ ,  $V_{\text{TN}} = 0.4 \text{ V}$ ,  $V_{\text{TP}} = -0.4 \text{ V}$ ,  $V_{\text{DD}} = 1.2 \text{ V}$ , use  $v_{\text{sat}} = 8 \times 10^6 \text{ cm/s}$

Solution: Use  $E_{\text{CN}} = 6 \times 10^4$ ,  $E_{\text{CP}} = 24 \times 10^4 \text{ V/cm}$

from

$$I_{DS} = W v_{\text{sat}} C_{\text{ox}} \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_C L}$$

Current per width

$$\frac{I_{DS}}{W} = v_{\text{sat}} C_{\text{ox}} \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_C L}$$

For NMOS

$$\frac{I_{DS}}{W} = (8 \times 10^6)(1.6 \times 10^{-6}) \frac{(1.2 - 0.4)^2}{(1.2 - 0.4) + 0.6} = 585 \mu\text{A} / \mu\text{m}$$

For PMOS

$$\frac{I_{DS}}{W} = (8 \times 10^6)(1.6 \times 10^{-6}) \frac{(1.2 - 0.4)^2}{(1.2 - 0.4) + 2.4} = 256 \mu\text{A} / \mu\text{m}$$

## Example 2

**Compute  $V_{DSAT}$  and saturation current ratio between NMOS and PMOS that have the same width.**

Given  $L = 100 \text{ nm}$ ,  $t_{ox} = 22^{-10}$ ,  $V_{TN} = 0.4 \text{ V}$ ,  
 $V_{TP} = -0.4 \text{ V}$ ,  $V_{DD} = 1.2 \text{ V}$

Use  $v_{sat} = 8 \times 10^6 \text{ cm/s}$ ,

$E_{CN} = 6 \times 10^4$ ,  $E_{CP} = 24 \times 10^4 \text{ V/cm}$ .

# Solution

**Example** compute  $V_{DSAT}$  and saturation current ratio between NMOS and PMOS that have the same width. Given  $L = 100\text{nm}$ ,  $V_{TN} = 0.4 \text{ V}$ ,  $V_{TP} = -0.4 \text{ V}$ ,  $V_{DD} = 1.2 \text{ V}$ ,  $v_{sat} = 8 \times 10^6 \text{ cm/s}$ ,  $E_{CN} = 6 \times 10^4 \text{ V/cm}$ ,  $E_{CP} = 24 \times 10^4 \text{ V/cm}$

$$V_{DSat} = \frac{(V_{GS} - V_T)E_c L}{(V_{GS} - V_T) + E_c L}$$

for NMOS  $V_{DSatn} = \frac{(1.2 - 0.4)(0.6)}{(1.2 - 0.4 + 0.6)} = 0.34 \text{ V}$

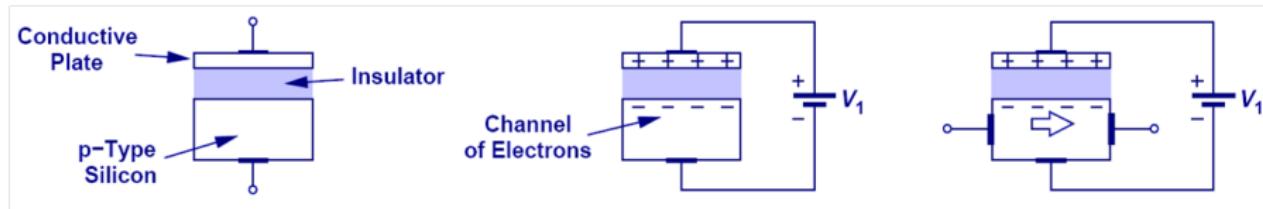
for PMOS  $V_{DSatp} = \frac{(1.2 - 0.4)(2.4)}{(1.2 - 0.4 + 2.4)} = 0.6 \text{ V}$

$$\frac{I_{DSatn}}{I_{DSatp}} = \frac{W_N v_{sat} C_{ox} (V_{GS} - V_{TN})^2 / (V_{GS} - V_{TN} + E_{CN} L_N)}{W_P v_{sat} C_{ox} (V_{GS} - V_{TP})^2 / (V_{GS} - V_{TP} + E_{CN} L_P)} = 2.3$$

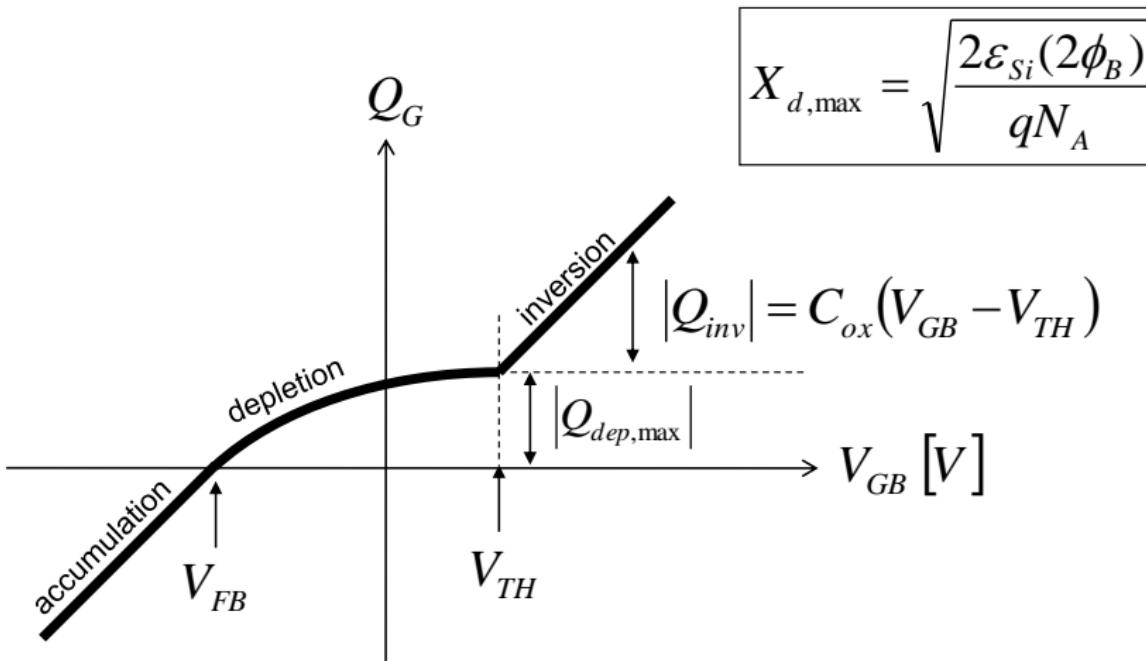
# CMOS capacitor and resistor

# MOS Capacitor

A metal-oxide-semiconductor structure can be considered as a parallel-plate capacitor, with the top plate being the positive plate, the gate insulator being the dielectric, and the p-type semiconductor substrate being the negative plate.



# Q-V Curve for NMOS Capacitor



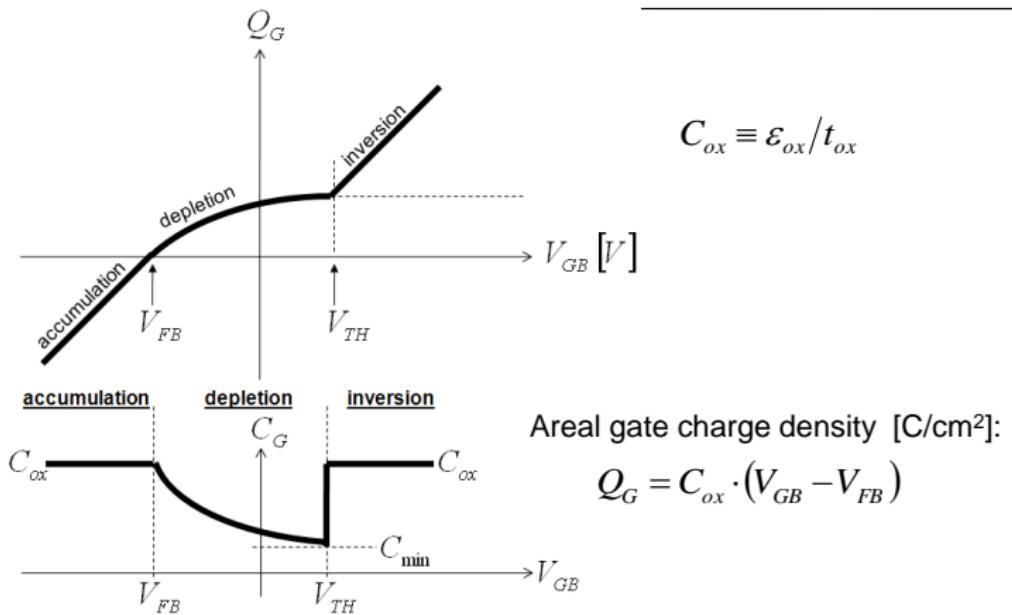
$$Q_{dep,max} = -qN_A X_{d,max} = -\sqrt{2qN_A \epsilon_{Si}(2\phi_B)}$$

# NMOS C-V Curve

The MOS C-V curve is obtained by taking the slope of the Q-V curve.

+  $C_G = C_{ox}$  in the accumulation and inversion regions of operation.

+  $C_G$  is smaller, and is a non-linear function of  $V_{GB}$  in the depletion region of operation.

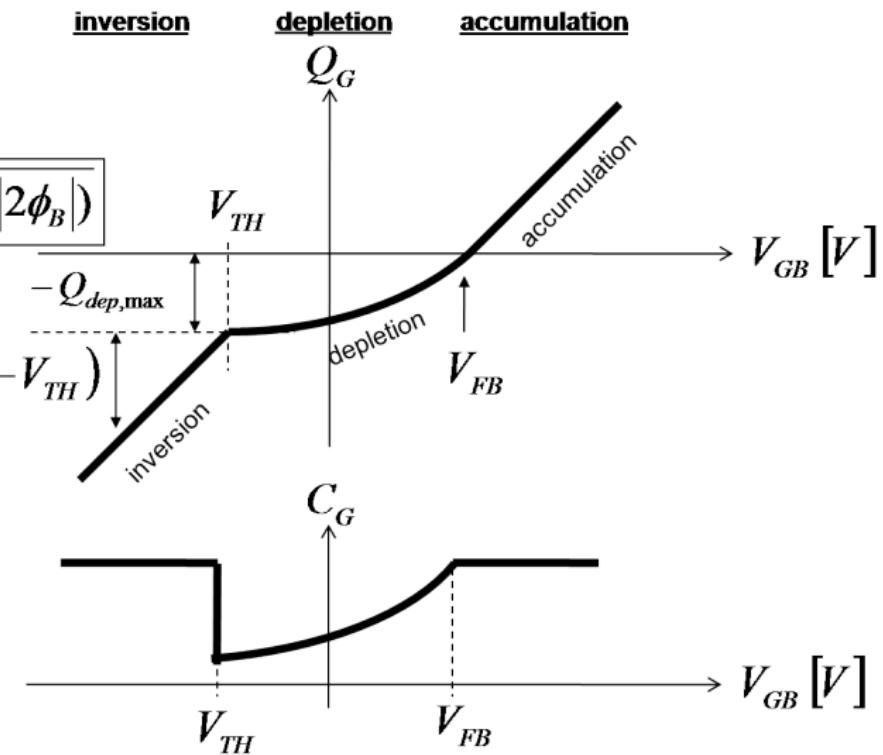


# PMOS Q-V , C-V

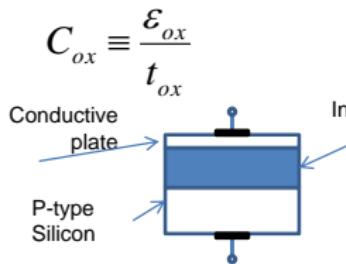
$$X_{d,\max} = \sqrt{\frac{2\epsilon_{Si}(|2\phi_B|)}{qN_D}}$$

$$Q_{dep,\max} = \sqrt{2qN_D\epsilon_{Si}(|2\phi_B|)}$$

$$-Q_{inv} = C_{ox}(V_{GB} - V_{TH})$$

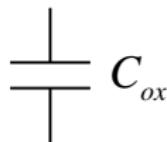


# MOS Small-Signal Capacitance Model



$$C_{ox} \equiv \frac{\epsilon_{ox}}{t_{ox}}$$

## Accumulation

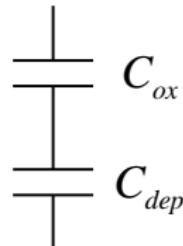


P-type  
Silicon

$$C_{dep} \equiv \frac{\epsilon_{Si}}{X_d}$$

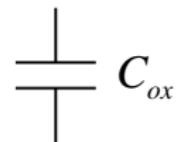
The incremental charge is located at the semiconductor surface

## Depletion



The incremental charge is located at the bottom edge of the depletion region

## Inversion

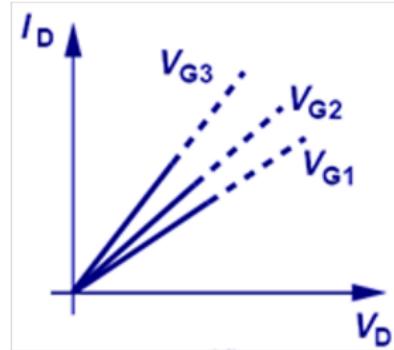
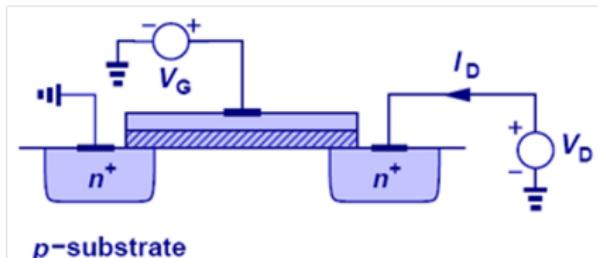
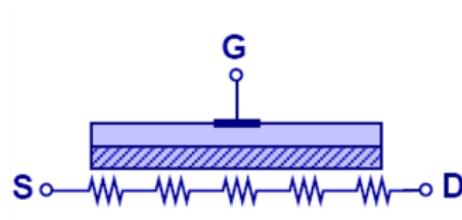


The incremental charge is located at the semiconductor surface

$$C_{\min} = \frac{C_{ox} C_{dep,\min}}{C_{ox} + C_{dep,\min}}$$

$$\text{where } C_{dep,\min} \equiv \frac{\epsilon_{Si}}{X_{d,\max}}$$

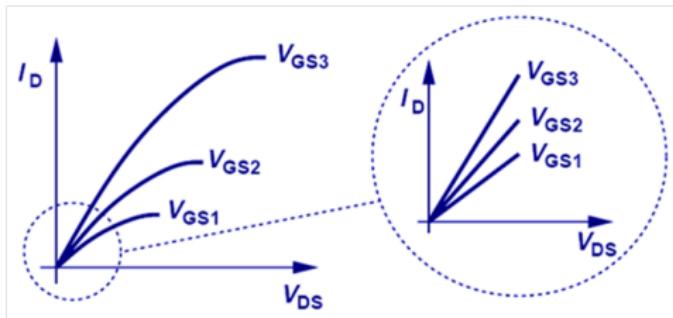
# MOSFET as Voltage-Controlled Resistor



In the ON state, the MOSFET channel can be viewed as a resistor. Since the mobile charge density within the channel depends on the gate voltage, the channel resistance is voltage-dependent.

# MOSFET as Voltage-Controlled Resistor

- For small  $V_{DS}$ , the MOSFET can be viewed as a resistor, with the channel resistance depending on the gate voltage.



$$R_{ON} = \text{resistivity} \cdot \frac{L}{t_{inv} \cdot W} = \frac{1}{q\mu_n n_{inv}} \cdot \frac{L}{t_{inv} \cdot W}$$

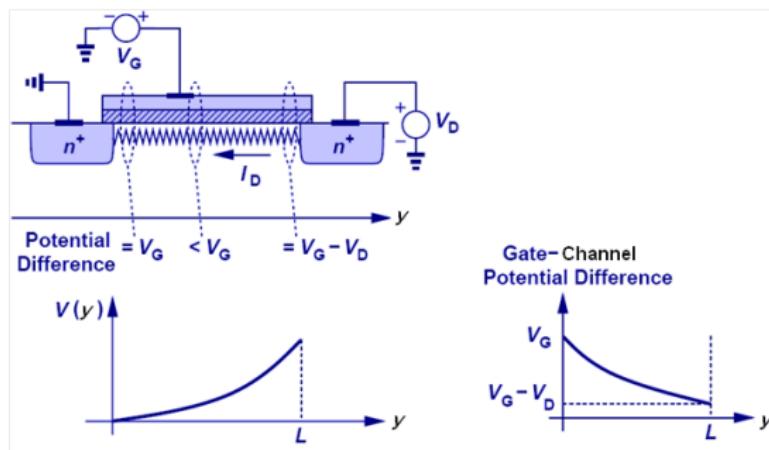
- Note that  $qn_{inv} \cdot t_{inv} = Q_{inv} = C_{ox}(V_{GS} - V_{TH})$

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

# MOSFET Channel Potential Variation

If the drain is biased at a higher potential than the source, the channel potential increases from the source to the drain.

The potential difference between the gate and channel decreases from the source to drain.



next ....

## Chapter 3: Analog circuit design