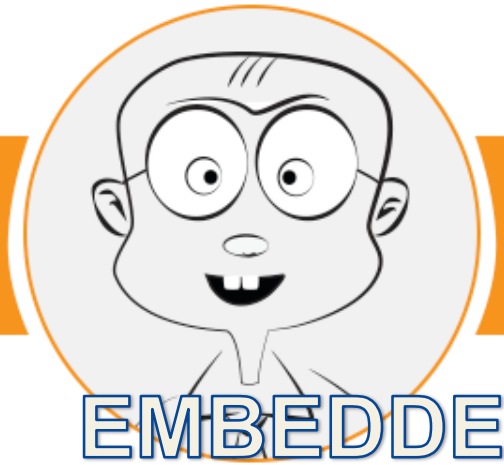

EMBEDDED SYSTEM COURSE

LECTURE 6: PERIPHERALS CLOCK DISTRIBUTION & MULTIPURPOSE CLOCK GENERATOR (MCG)

Learning Goals

- Understanding about how the clock signal has been distributed among KL46 SoC
- Understanding on how to configure an specific clock signal for given peripheral.,
- Understanding on how to configure the PLL and FLL on using internal clock or external clock.

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- Overview on KL46 Clock Modules
- Clock distribution
- System Oscillator (OSC)
- System Integration Module (SIM)
- Multipurpose Clock Generator (MCG)
  - Mode of Operations
  - MCG Loss Lock Detector
  - MCG Auto Trim – ATM
- Examples

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Overview on KL46 Clock Modules

- The KL46 contains the following modules on maintaining the MCU clock and its power mode:
  - **System Oscillator (OSC)**: The OSC module is a crystal oscillator. The module, in conjunction with an external crystal or resonator, generates a reference clock for the MCU. Refer chapter 25 in KL46 Reference Manual.
  - **System Integration Module (SIM)**: Configure the output clock and its divide factory for MCU system clock and other peripherals. Refer chapter 12 in KL46 Reference Manual.
  - **System Mode Controller (SMC):** is responsible for sequencing the system into and out of all low-power Stop and Run modes. Refer chapter 13 in KL46 Reference Manual.

Overview on KL46 Clock Modules

- The KL46 contains the following modules on maintaining the MCU clock and its power mode:
  - **Multipurpose Clock Generator (MCG)**: provides several clock source choices for the MCU. The module contains a frequency-locked loop (FLL) and a phase-locked loop (PLL)
  - **Clock distribution diagram**: depict all clock lines, PLL and FLL in the system. It also provides the relationship among the MCG, OSC and SIM in the MCU. Refer chapter 5 in KL46 Reference Manual.
- In this scope of the lecture, only the Clock distribution, SIM, OSC, MCG have been discussed. The SMC is an advance topic and target on self-studying.

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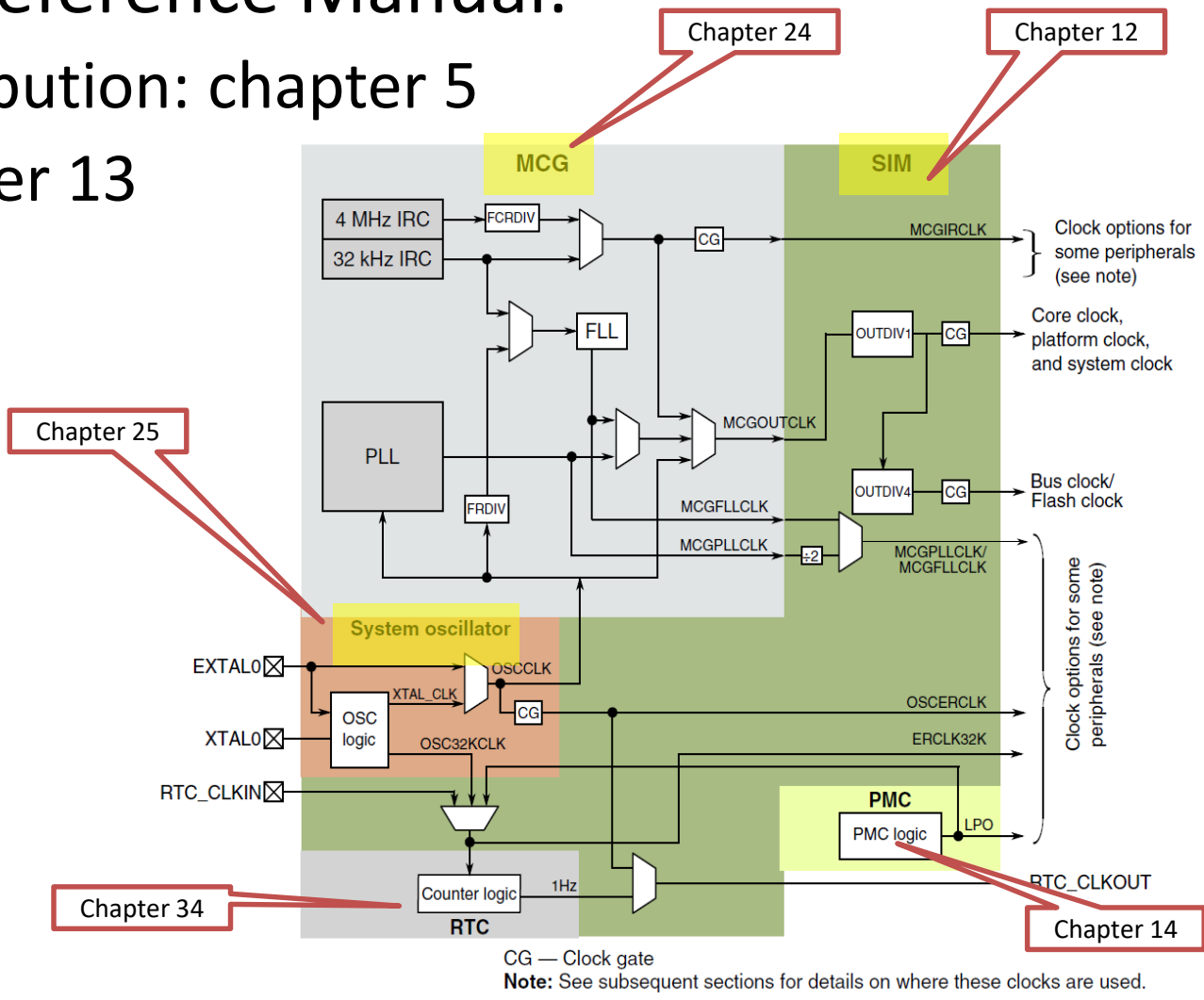
Clock Distribution

- Refer KL46 Reference Manual:
  - Clock Distribution: chapter 5
  - SMC: chapter 13



Clock Distribution

- Clock definitions

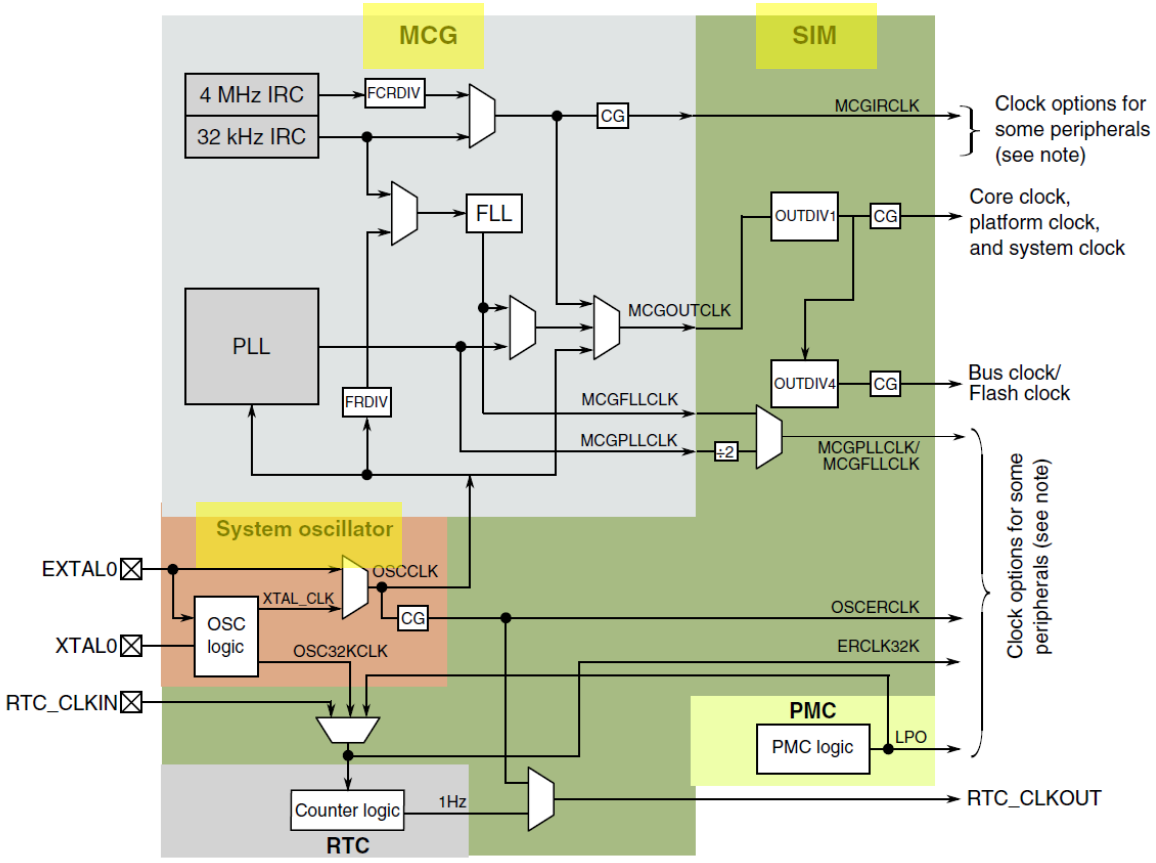
Clock name	Description
Core clock	MCGOUTCLK divided by OUTDIV1 Clocks the ARM Cortex-M0+ core.
Platform clock	MCGOUTCLK divided by OUTDIV1 Clocks the crossbar switch and NVIC.
System clock	MCGOUTCLK divided by OUTDIV1 Clocks the bus masters directly
Bus clock	System clock divided by OUTDIV4. Clocks the bus slaves and peripherals.
Flash clock	Flash memory clock On this device, it is the same as Bus clock

Clock Distribution

- Clock definitions

Clock name	Description
MCGIRCLK	MCG output of the slow or fast internal reference clock
MCGOUTCLK	MCG output of either IRC, MCGFLLCLK, MCGPLLCLK, or MCG's external reference clock that sources the core, system, bus, and flash clock.
MCGFLLCLK, MCGPLLCLK	MCG output of the FLL and PLL
OSCCLK	System oscillator output of the internal oscillator or sourced directly from EXTAL. Used as MCG external reference clock
OSCERCLK	System oscillator output sourced from OSCCLK that may clock some on-chip modules
OSC32KCLK	System oscillator 32kHz output

Clock Distribution



- Base on this diagram, to configure:
  - **External clock selection**: refer to System Oscillator module in chapter 25
  - **Internal clock source and PLL, FLL**: refer to MCG module in chapter 24
  - **Peripheral clock gate and its divide factor**: refer to SIM module in chapter 12.

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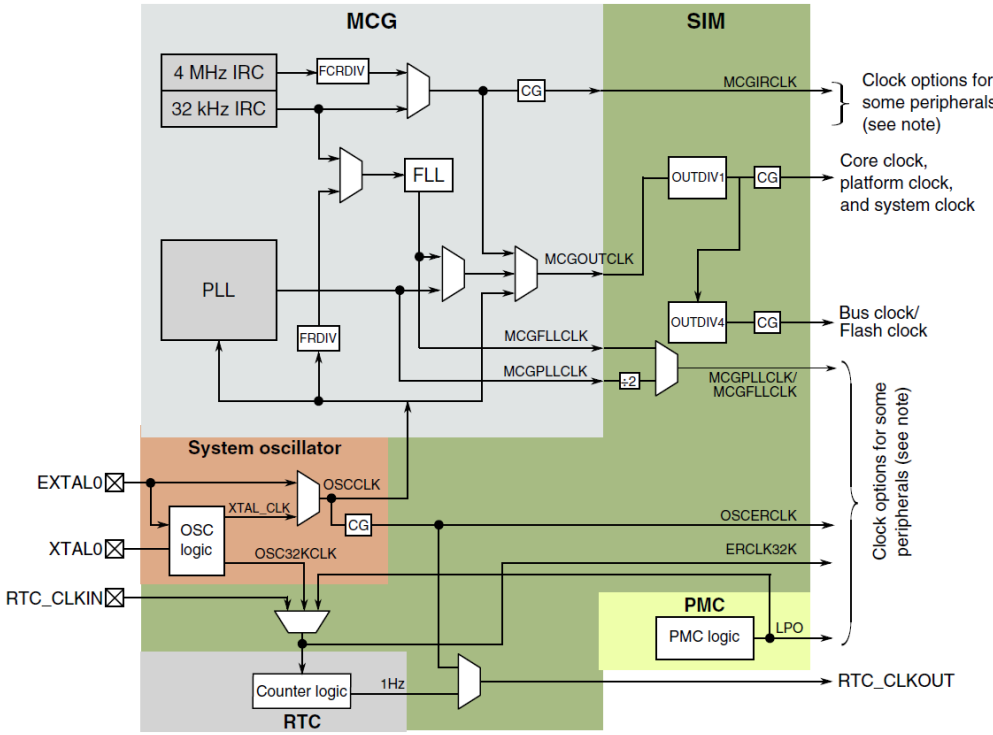
System Oscillator (OSC)

- **System Oscillator (OSC)**
  - The module, in conjunction with an external crystal or resonator, generates a reference clock for the MCU
  - Input:
    - External Crystal
    - Input RTC Clock
  - Output:
    - OSCCLK for MCU system
    - OSCERCLK for on-chip peripherals, and OSC32KCLK
    - OSC32KCLK for RTC



CG — Clock gate

Note: See subsequent sections for details on where these clocks are used.

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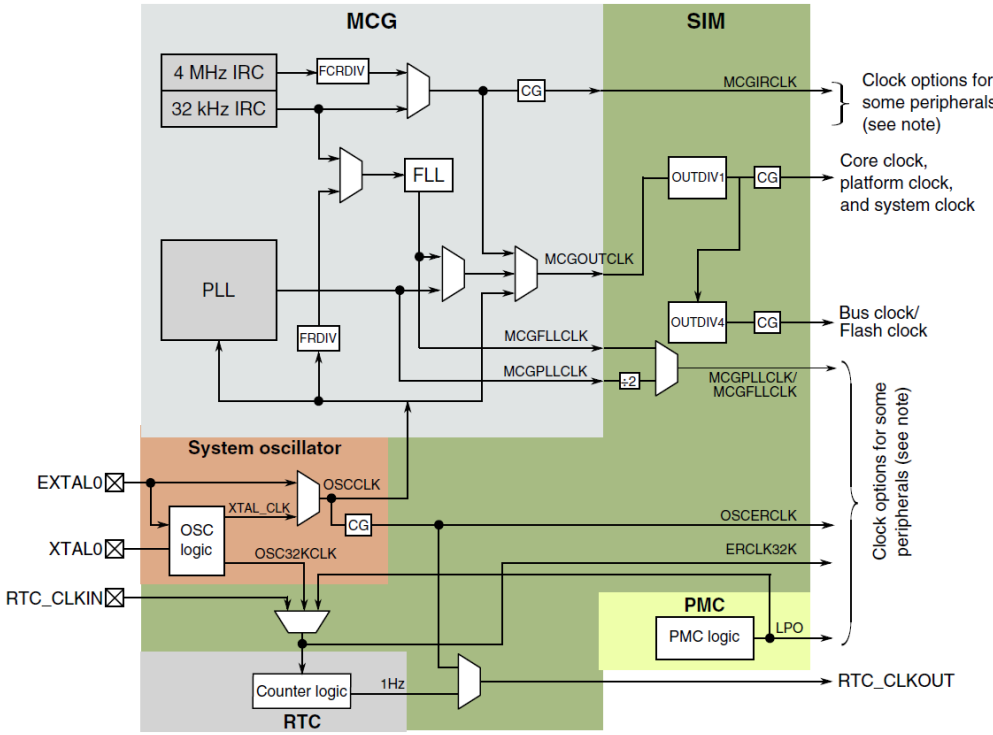
System Integration Module (SIM)

- **System Integration Module (SIM)**
  - System clock configuration
    - System Clock divide values
    - ERCLK32K clock selection
    - Peripheral clock gate and selection



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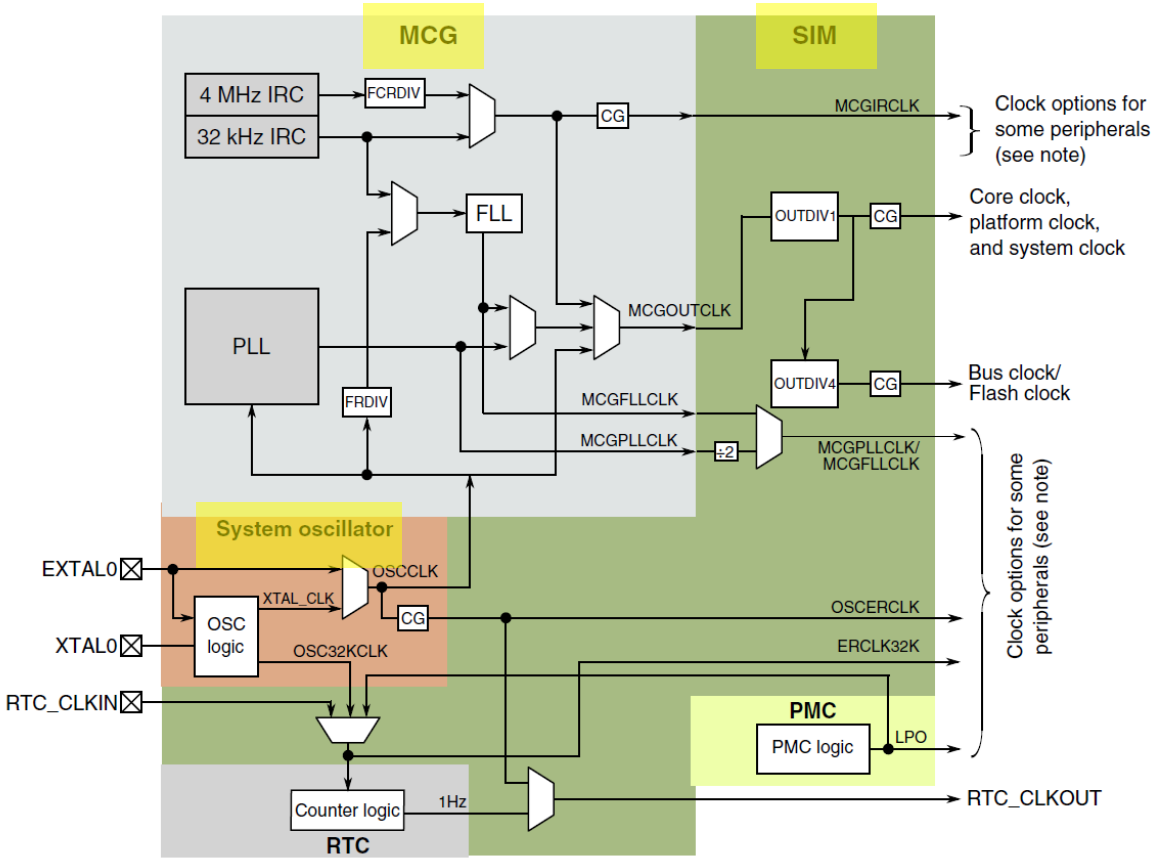
Multipurpose Clock Generator (MCG)

- **Multipurpose Clock Generator (MCG)**: provides several clock source choices for the MCU. The module contains a frequency-locked loop (FLL) and a phase-locked loop (PLL)

Multipurpose Clock Generator (MCG)



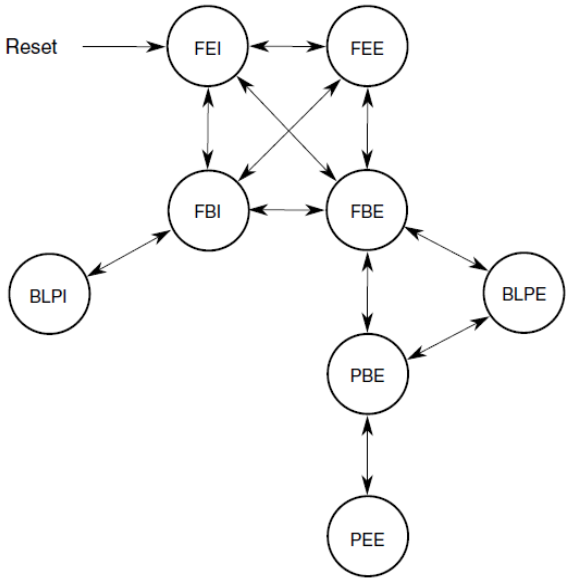
CG — Clock gate
Note: See subsequent sections for details on where these clocks are used.

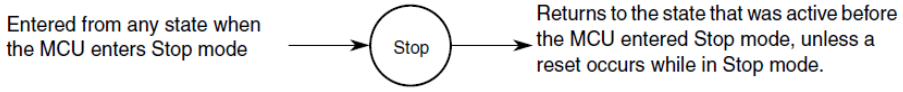
Key features:

- **01 Frequency-locked loop (FLL)**
  - Internal or external reference clock can be used as the FLL source
  - Can be used as a clock source for other on-chip peripherals
- **01 Phase-locked loop (PLL)**
  - External reference clock is used as the PLL source
  - Integrated loop filter
  - Can be used as a clock source for other on-chip peripherals
- **Internal reference clock generator**
  - Slow clock with nine trim bits for accuracy.
  - Fast clock with four trim bits
  - Can be used as source clock for the FLL
  - Either the slow or the fast clock can be selected as the clock source for the MCU
  - Can be used as a clock source for other on-chip peripherals
- **External clock from the Crystal Oscillator (OSC0)**: can be used as a source for FLL and/or PLL. Also can provide clock to MCU
- **External clock from the Crystal Oscillator (OSC1)**: can be used as a source for PLL. Also can provide clock to MCU
- **External clock from the Real Time Counter (RTC)**: clock source for FLL. Also can provide clock to MCU
- **External clock monitor** with reset and interrupt request
- **Internal Reference Clocks Auto Trim Machine (ATM)** capability using an external clock as a reference

Multipurpose Clock Generator (MCG)

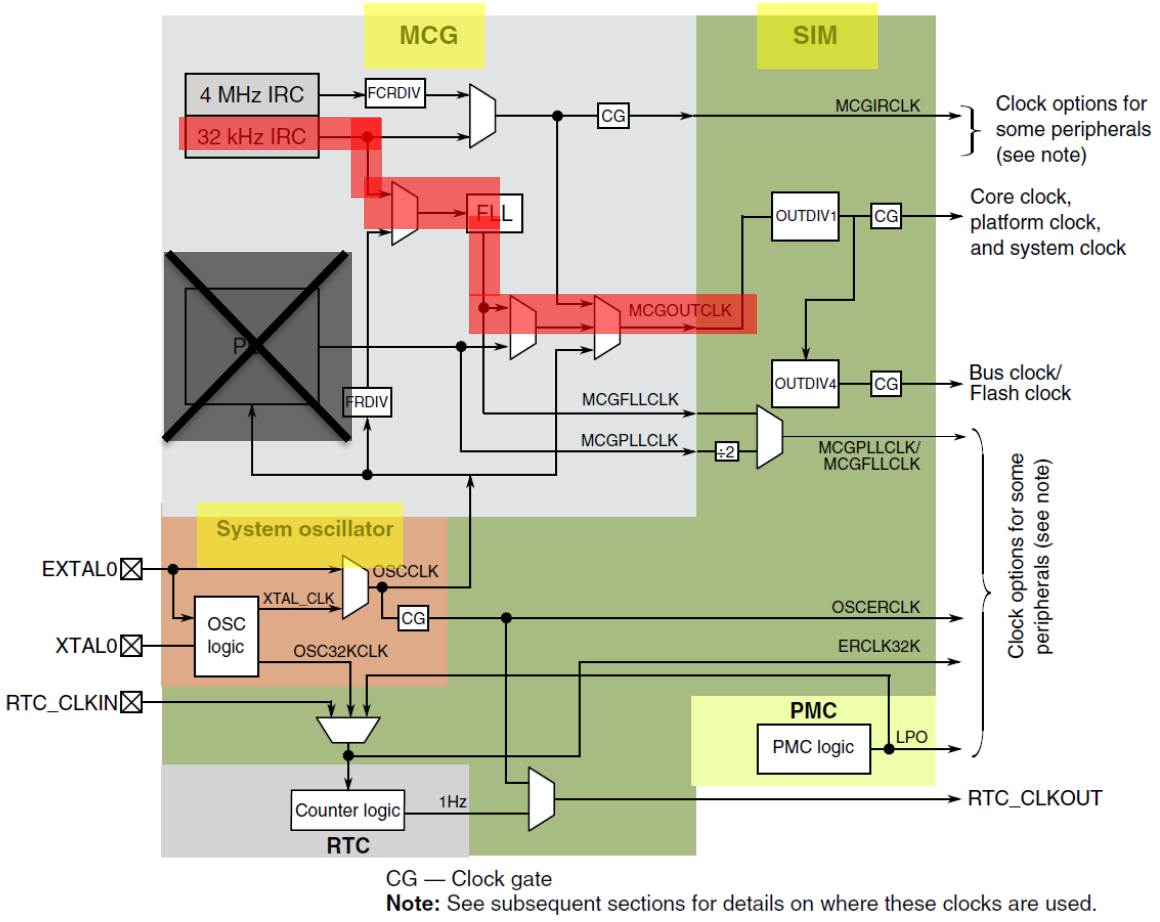
- **Mode of Operations**
  - **FEI :** FLL Engaged Internal
  - **FEE**: FLL Engaged External
  - **FBI**: FLL Bypassed Internal
  - **FBE**: FLL Bypassed External
  - **PEE:** PLL Engaged External
  - **PBE:** PLL Bypassed External
  - **BLPI**: Bypassed Low Power Internal
  - **BLPE:** Bypassed Low Power External
  - **STOP**





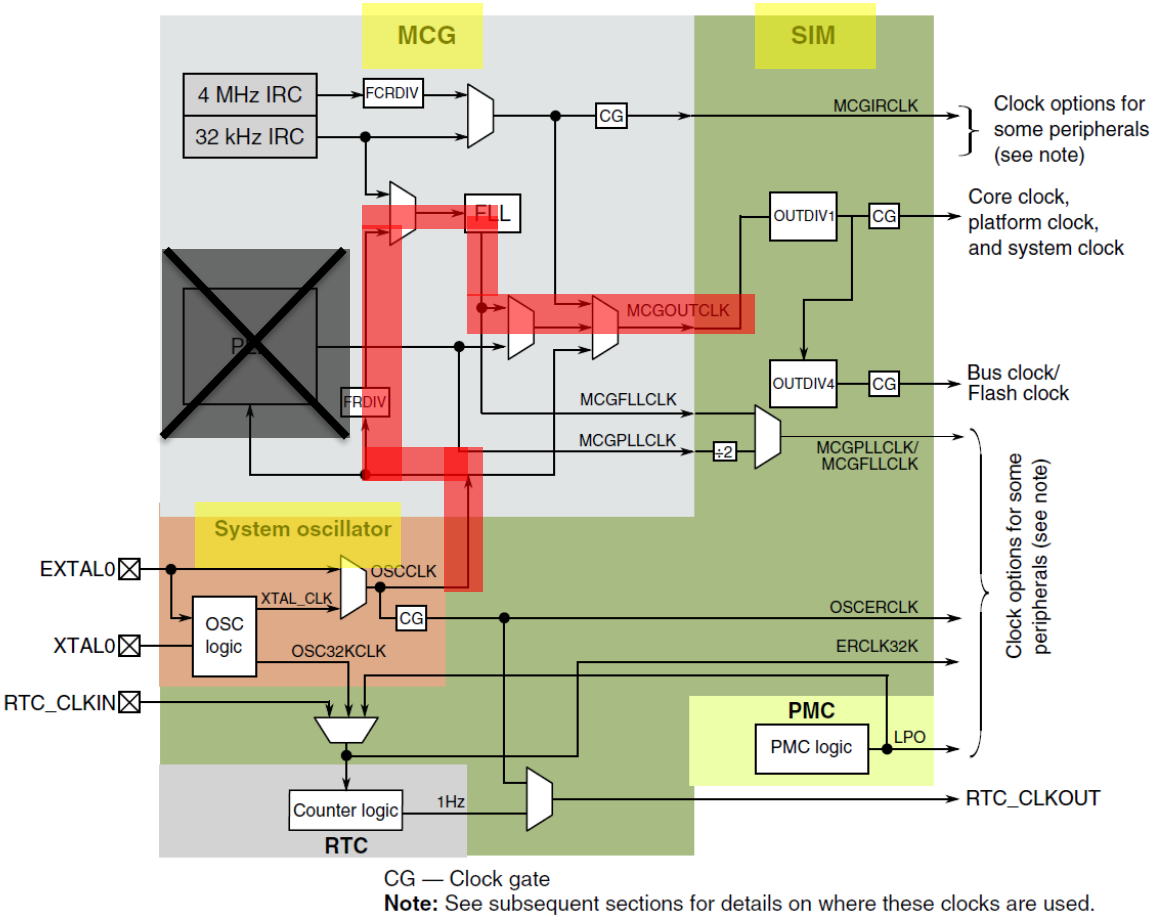
Multipurpose Clock Generator (MCG)

- **Mode of Operations**
  - **FEI :** FLL Engaged Internal
    - Default mode of operation
    - Selects the FLL output as the MCGOUT clock
    - Multiplies the Slow Internal Reference Clock
    - PLL is disabled in a low-power state unless C5[PLLCLKEN] is set
    - Setting: C1[CLKS]=0, C1[IREFS]=1, C6[PLLS]=0



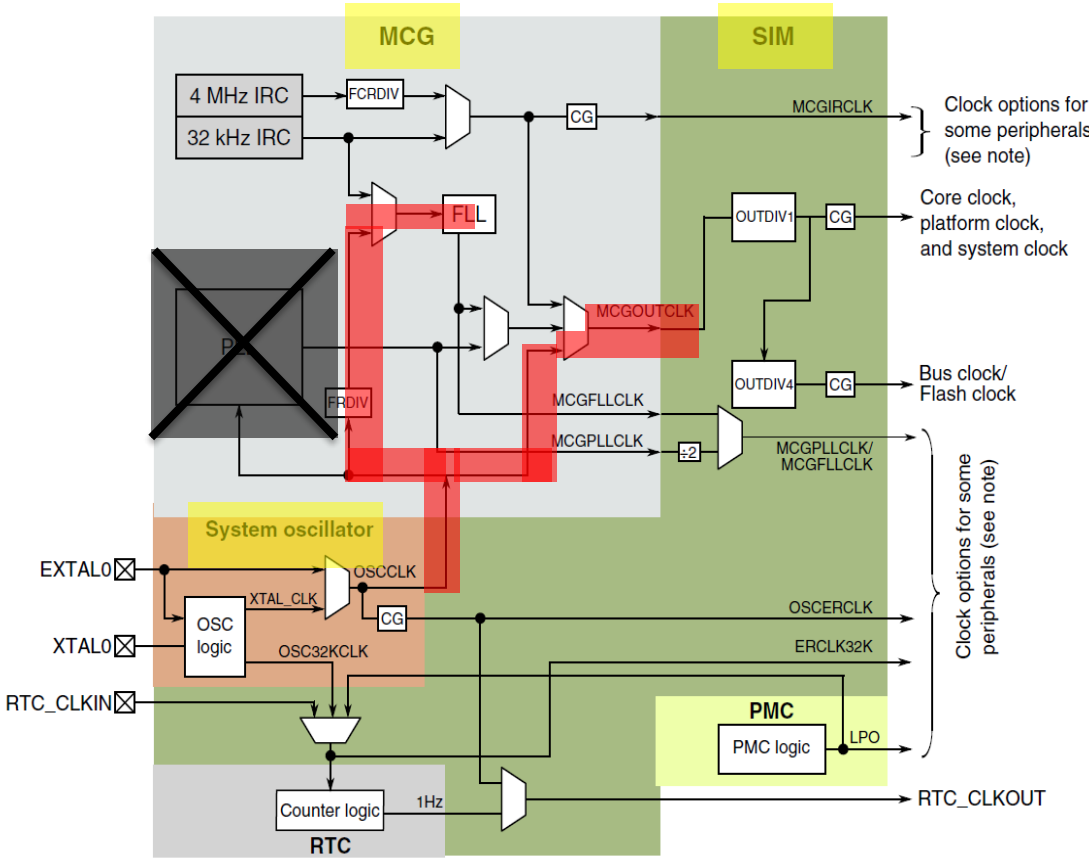
Multipurpose Clock Generator (MCG)

- **Mode of Operations**
  - **FEE :** FLL Engaged External
    - Selects the FLL output as the MCGOUT clock
    - Multiplies the External Reference Clock
    - PLL is disabled in a low-power state unless C5[PLLCLKEN] is set
    - Setting: C1[CLKS] = 00, C1[IREFS] = 0, C6[PLLS] = 0 and C1[FRDIV] set to provide an external ref clock in the range of 31.25 kHz to 39.0625 kHz



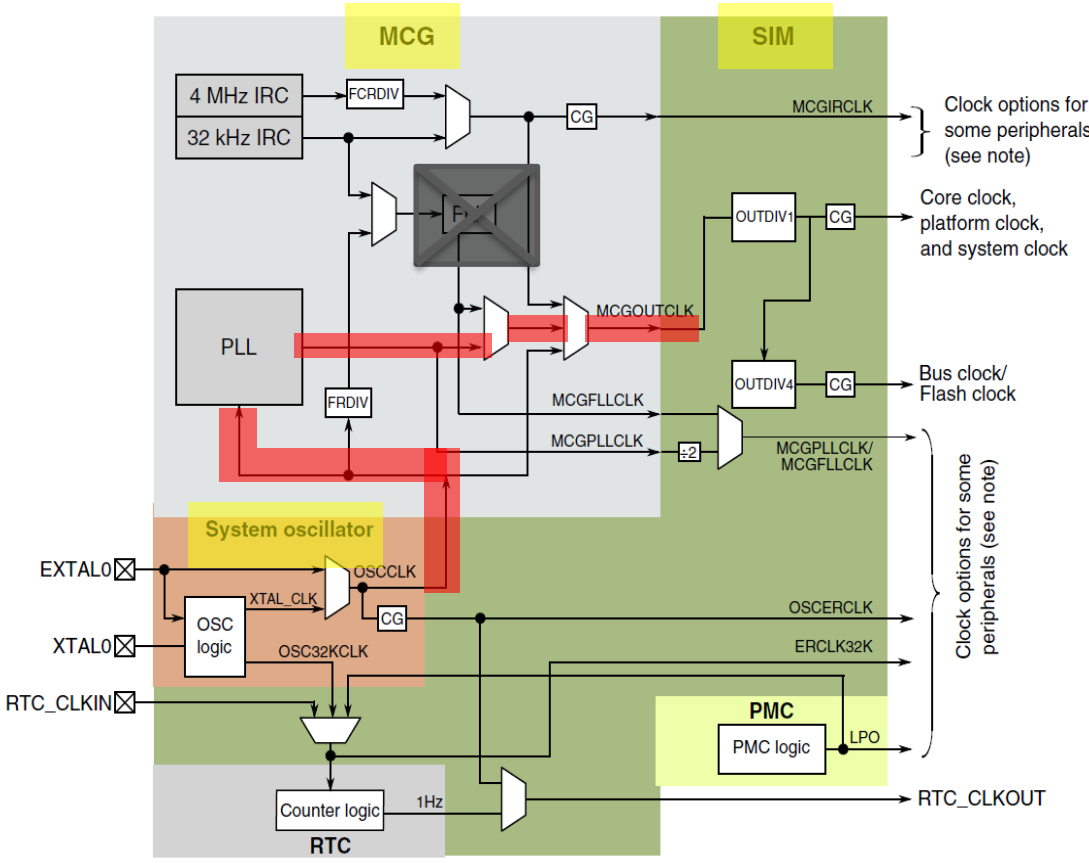
Multipurpose Clock Generator (MCG)

- **Mode of Operations**
  - **FBE:** FLL Bypassed External
    - Selects the External Reference Clock as the MCGOUT clock.
    - The FLL is operational but the output is not used (external reference clock is used as the input reference)
    - Can be provide a system clock by when FLL archived the target frequency.
    - PLL is disabled in a low-power state unless C5[PLLCLKEN] is set
    - Setting: C1[CLKS] = 10, C1[IREFS] = 0, C1[FRDIV] set to provide an external ref clock in the range of 31.25 kHz to 39.0625 kHz, C6[PLLS] = 0 and C2[LP] = 0



Multipurpose Clock Generator (MCG)

- **Mode of Operations**
  - **PEE:** PLL Engaged External
    - Selects the PLL output as the MCGOUT clock
    - The external reference clock provides the PLL reference clock
    - Setting: C1[CLKS] = 00, C1[IREFS] = 0, C5[PRDIV] set to provide an external ref clock in the range of 2 MHz to 4 MHz and C6[PLLS] = 1 and C2[LP] = 0
    - FLL is disabled in a lowpower state.

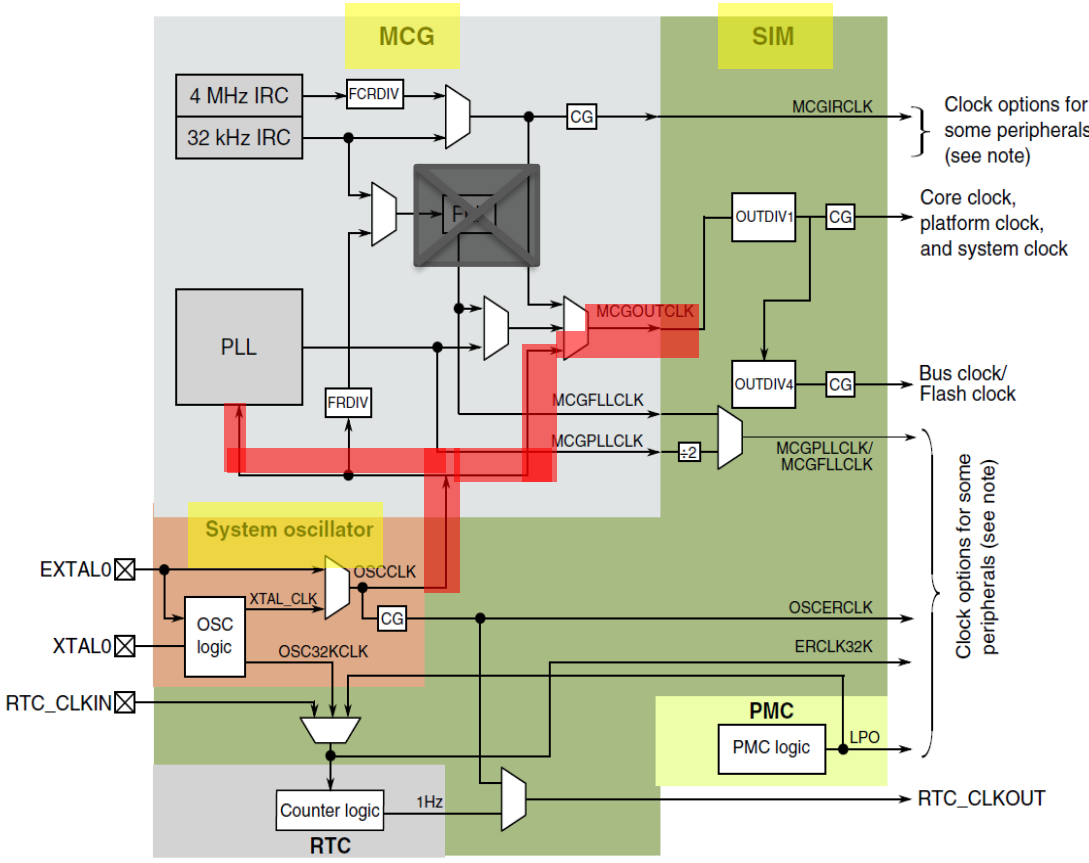


CG — Clock gate

Note: See subsequent sections for details on where these clocks are used.

Multipurpose Clock Generator (MCG)

- **Mode of Operations**
  - **PBE:** PLL Bypassed External
    - Selects the External Reference Clock as the MCGOUT clock.
    - The PLL is operational but the output is not used (external reference clock is used as the input reference)
    - This mode can be used to provide a system clock while the PLL achieves the target frequency
    - Setting: C1[CLKS] = 10, C1[IREFS] = 0, C5[PRDIV] set to provide an external ref clock in the range of 2 MHz to 4 MHz, C6[PLLS] = 1 and C2[LP] = 0
    - FLL is disabled in a lowpower state.

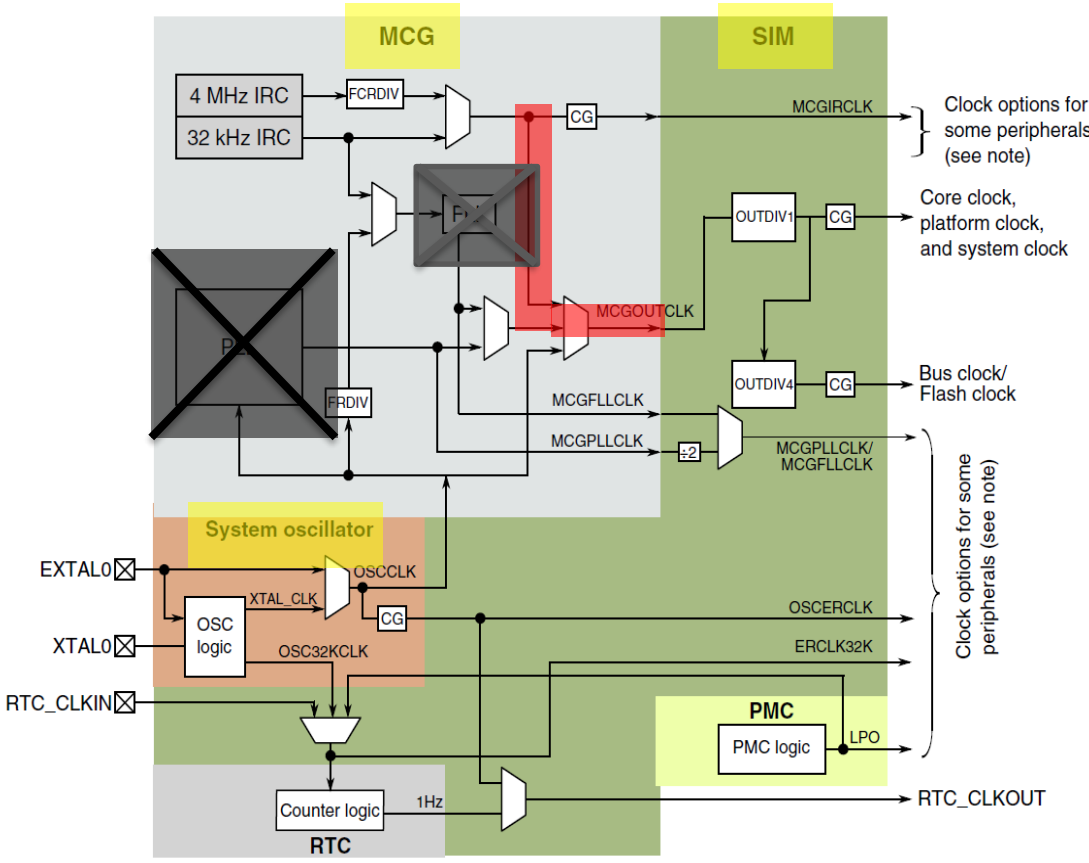


CG — Clock gate

Note: See subsequent sections for details on where these clocks are used.

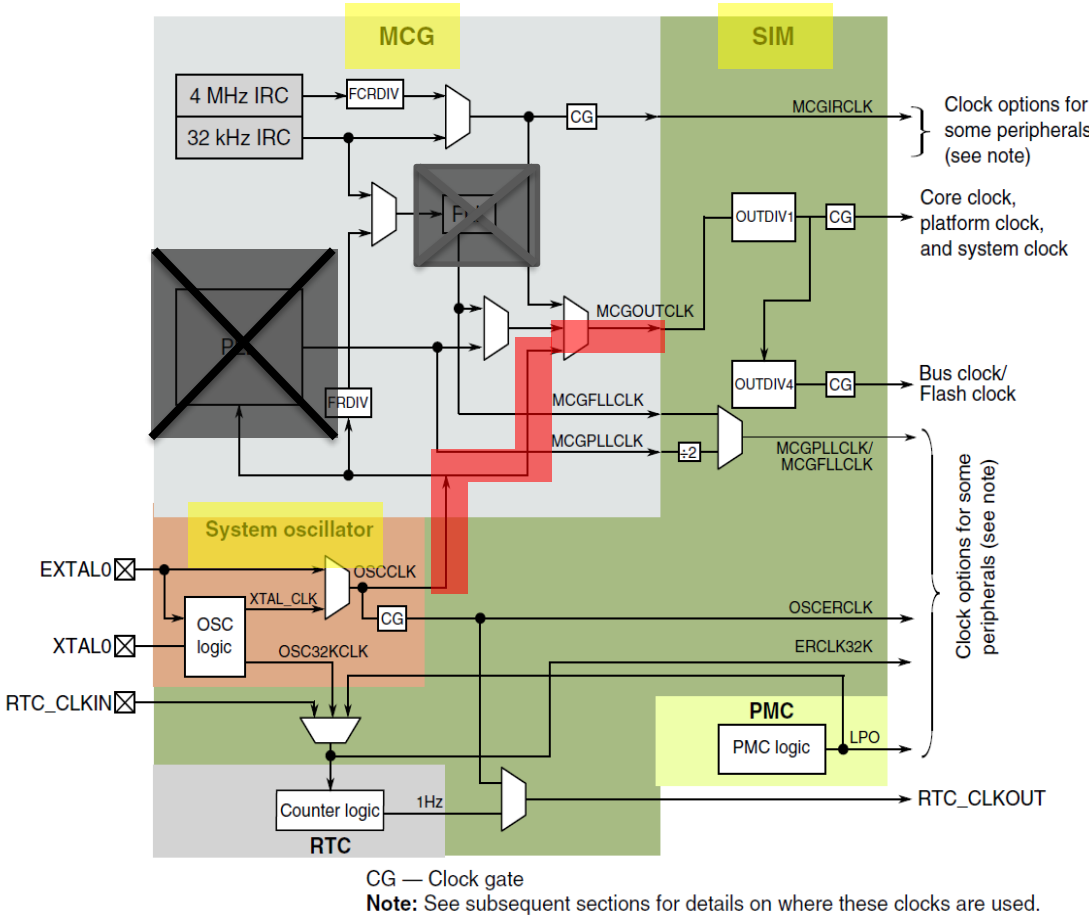
Multipurpose Clock Generator (MCG)

- **Mode of Operations**
  - **BLPI:** Bypassed Low Power Internal
    - Can select slow or fast Internal Reference Clock as the MCGOUT clock
    - The FLL and PLL are disabled (even if PLLCLKEN set)
    - Setting: C1[CLKS] = 01, C1[IREFS] = 1, C6[PLLS] = 0 and C2[LP] = 1



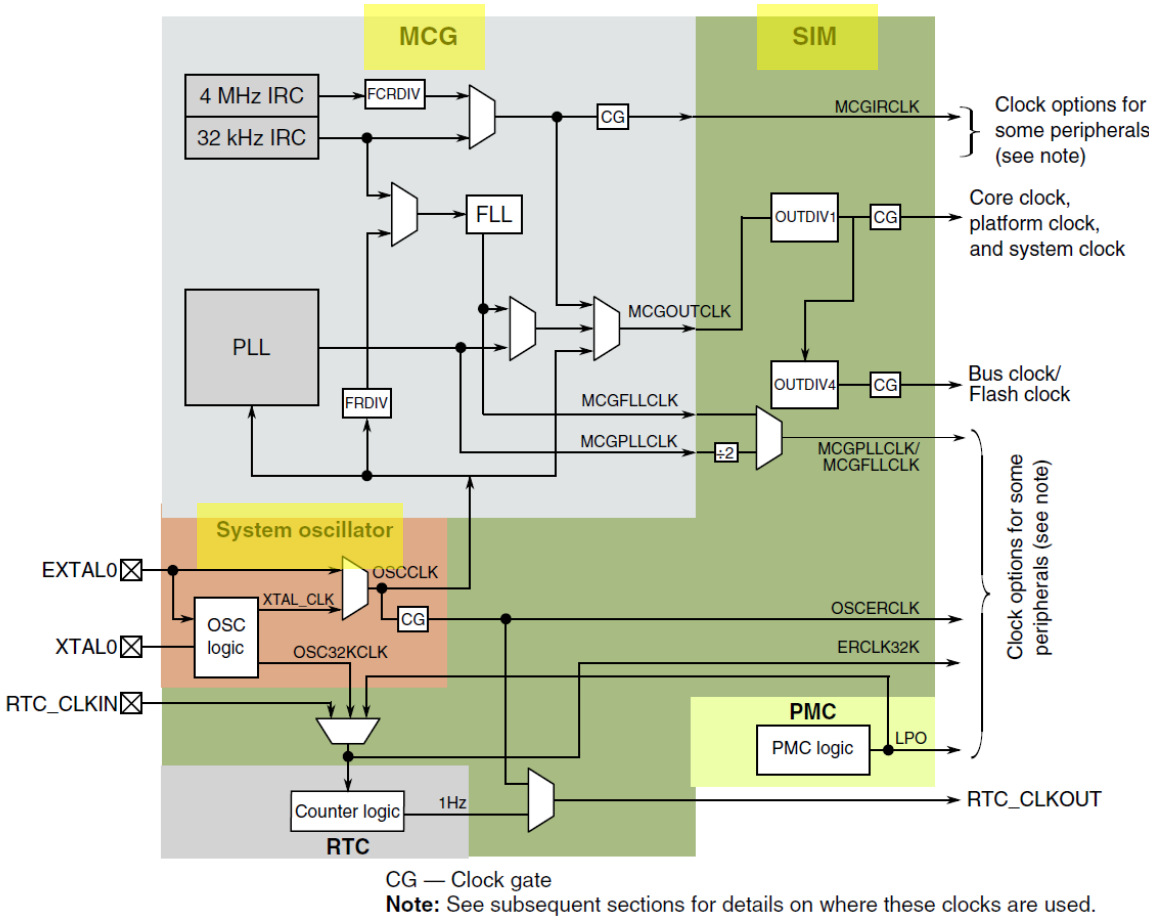
Multipurpose Clock Generator (MCG)

- **Mode of Operations**
  - **BLPE:** Bypassed Low Power External
    - External Reference Clock as the MCGOUT clock
    - The FLL and PLL are disabled (even if PLLCLKEN set)
    - Setting: C1[CLKS] = 10, C1[IREFS] = 0 and C2[LP] = 1



Multipurpose Clock Generator (MCG)

- **Mode of Operations**
  - **STOP**
    - MCGPLLCLK is active in Normal Stop mode when PLLSTEN=1
    - MCGPLL1CLK is active in Normal Stop mode when PLLSTEN1=1
    - MCGIRCLK is active in Normal Stop mode when all the following conditions become true:
      - C1[IRCLKEN] = 1
      - C1[IREFSTEN] = 1



Multipurpose Clock Generator (MCG)

- **MCG Loss Lock Detector**
  - The MCG includes a PLL loss-of-lock detector – the MCU has been reset if the phase lock gets lost.
  - The detector is enabled when configured for PEE and lock has been achieved.
  - If the MCG_C8[LOLRE] bit in the MCG module is set and the PLL lock status bit (MCG_S[LOLS0]) becomes set, the MCU resets. The RCM_SRS0[LOL] bit is set to indicate this reset source.

Multipurpose Clock Generator (MCG)

- **MCG Auto Trim – ATM**
  - An feature enable the MCG hardware to automatically trim the MCG Internal Reference Clocks using an external clock as a reference.
  - The selection between which MCG IRC clock gets tested and enabled is controlled by the ATC[ATMS] control bit
    - (ATC[ATMS]=0 selects the 32 kHz IRC and ATC[ATMS]=1 selects the 4 MHz IRC).
    - If 4 MHz IRC is selected for the ATM, a divide by 128 is enabled to divide down the 4 MHz IRC to a range of 31.250 kHz.

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- **Examples**

Multipurpose Clock Generator (MCG)

- **Examples:** FRD KL46 uses external crystal 8MHz, Switching from FEI -> FEE (MCGOUTCLK=Bus clock = 8MHz, FLL output = 20MHz)
  - Configure OSC0 to use external crystal
    - Enable clock for PortA: SIM[SCGC5]
    - Configure the PTA18 and PTA19 to MUX
  - Select FLL as a clock source
  - MCG[C2].RANGE0 = 10 – Very high frequency range selected for the crystal oscillator
  - MCG[C2]. EREFS0 = 1 – Oscillator requested
  - OSC0[CR]. ERCLKEN = 0 – since we use the crystal instead of external clock reference.
  - MCG[C1].CLKS = 0x02 - Selects the clock source for MCGOUTCLK to external reference clock
  - MCG[C1].FRDIV = 0x03 – set input clock to FLL = external ref clock /256 = 31.250KHz
  - MCG[C1].IREFS = 0x00 – Select input FLL clock is external ref clock
  - Set MCG[C4].DMX32= 0x00, MCG[C4].DRST_DRS = 0x00 – set FLL factor = 640 -> input FLL ref clock = 31.250Khz * 640 = 20Mhz

Multipurpose Clock Generator (MCG)

- **Examples**
  - Switching from FEE -> FBE

Multipurpose Clock Generator (MCG)

- **Examples**
  - Switching from FEE -> PEE

Multipurpose Clock Generator (MCG)

- **Enable clock for I2C0 module**
  - Configure the MCG to specific mode (i.e. PEE), configure the Bus clock properly (setting OUTDIV4) since the I2C0 is clocking from Bus clock.
  - Configure the I2C0_SCL and I2C0_SDA pin to I2C mode
    - Set PTC9 (I2C0_SDA) mode 2: PORTC[PCR9].MUX=0x2
    - Set PTC8 (I2C0_SCL) to mode 2: PORTC[PCR8].MUX=0x2
  - Enable the clock gate for I2C0 module
    - Set SIM_SCGC4[I2C0] = 1
  - Setting the I2C0_F register to configure its baudrate
  - Enable the I2C0 module
    - Set I2C0_C1[IICEN] = 1

Summary

- Understanding about the basic concepts regarding KL46 clock modules including clock distribution, how to configure MCG to archives the target clock speed.

Question & Answer

Thanks for your attention !

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