‘07/10/31

Asynchronous Design Guide

Versionv1.0

Renesas Technology Corp.

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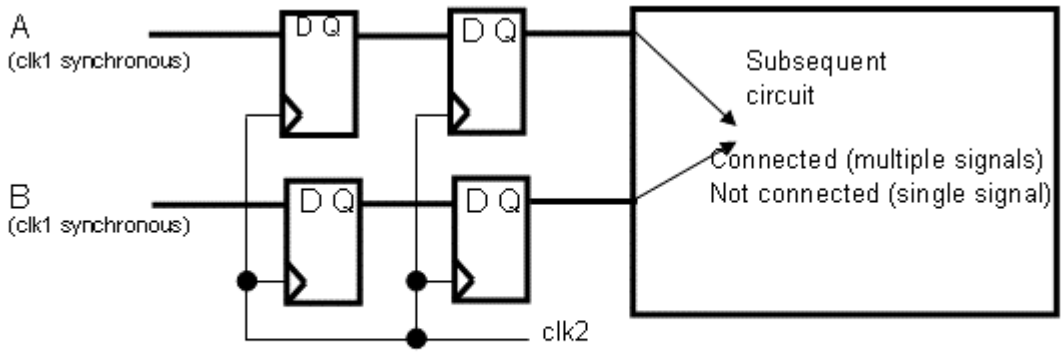
1. Introduction

1.1 Terms and Definitions

1.1.1 Single Signal, Mutiple Signal & Group Definitions

single signal ： After passing the circuit of "asynchronous signal transfer", timing dependencies with other signals are not generated.
multiple signals ： After passing the circuit of "asynchronous signal transfer", The timing dependencies must be maintained among the signals(A and B).



Example of single signal:
1 bit serial input in asynchronous communication that does not change dynamically is viewed as static signal.

Example of multiple signals:
Multiple bit data, data and control signal, control signal combined; for example if SHwyIF signal is synchronized with a diff clock, all signals convert to multiple signals.

As described later in the document, the configuration of synchronization circuit varies greatly in case of single signal and multiple signals.
In the improved version of STAcheck, check for circuit configuration of multiple signals is now possible, by clearly specifying group in check status file (like SDC).

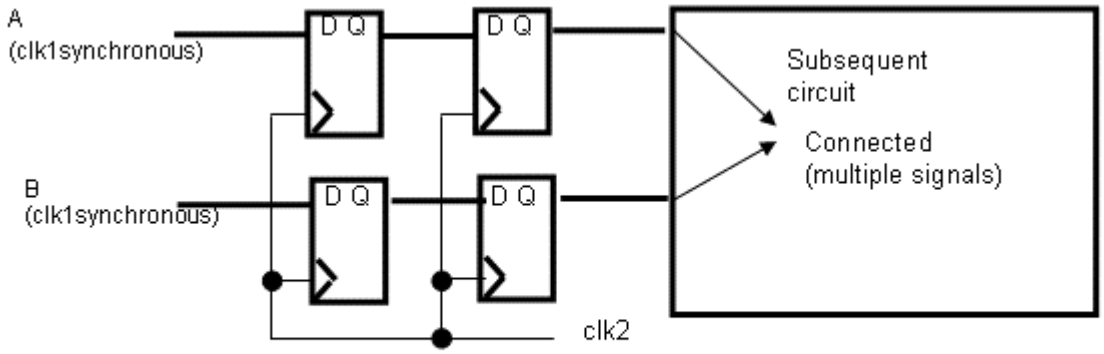
For details refer to STAcheck manual.

Context of Group signal definition introduction in STA check

As described later in the document, the circuit configuration of "asynchronous signal transfer" varies greatly in case of single signal and multiple signals. Especially, when multiple signals are incorrect, single signal is

interpreted, and “2 flopped” circuit is adopted. As a result, there were a lot of examples in the past that combined errors were generated in subsequent circuit of this circuit.
In STAcheck, by defining the bus control signals which you should treat as not only the bus signals but also synchronization signals as "multiple signals" in a check condition (SDC like) file,
Therefore, synchronization circuit and combined error can be checked as multiple signals

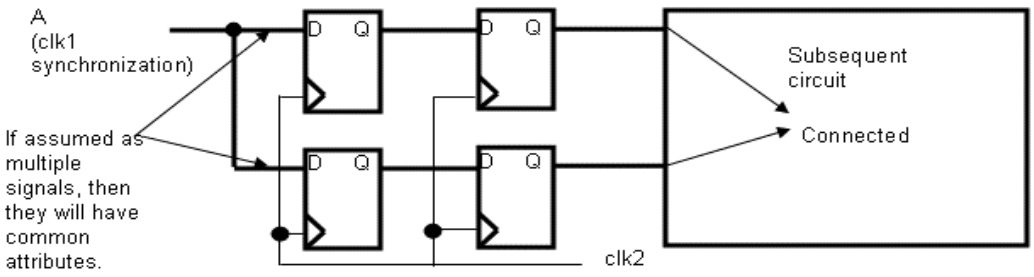
1.1.2 About combined error of multiple signals



In case of multiple signals (A and B), cycle slippage is generated in subsequent circuit of this circuit, and it becomes an **NG circuit.** Thus it is referred as combined error. This type of error is not detected easily, as the timing or operation status dependency is complex due to the layout. In other words, precise differentiation of single signal and multiple signals is important. Further, even if cycle slippage has occurred, and cycle slippage is not transferred to the subsequent circuits, it does not pose a problem. However, in order to ensure absence of any trouble, it is necessary to verify the timing as determining OK/NG. STAcheck cannot be done.

→ “Bad Circuit” is the root cause.

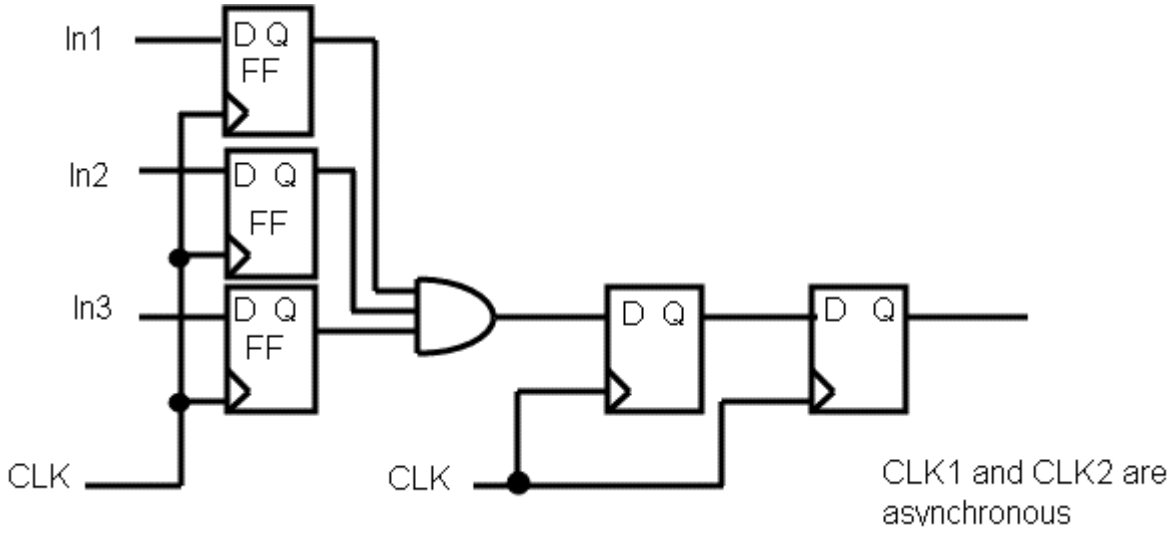
The current improvement in STAcheck is can detect combined error.



The fan-out circuit in an asynchronous signal transfer is a prohibited item in **single signal**. This circuit can be considered as **multiple signals** in case of combined circuit at the fan-out point in the latter circuits.
In this case, if A is changed, then cycle slippage may occur in the latter circuits.
Therefore this “Bad circuit” becomes NG circuit unless established that cycle slippage is not passed to the latter circuits.

1.1.3 DC signal

The circuit shown below becomes NG if In1, In2 and In3 change dynamically. (For root cause refer the reference data).
In STAcheck it is called as D005-01 type4 error. Also, simultaneously FF1, FF2 and FF3 are listed in log file as DC signal candidate.
When signals (In2 and In3) transfer asynchronously, In1 value is 0 or 1 has been fixed.
Whereas In1 is a DC signal, and is constant. Especially, in software flow (for ex. In1 is not changed simultaneously with In2 or In3) and mode signal, the signal is indicated.
As a result, among In1, In2 and In3, if 2 are DC signal, then above stated circuit becomes equivalent to 1 bit signal transfer and therefore is OK.
In the improved version of STAcheck, DC signal is specified in Check status (like SDC) file and function is created to eliminate any pseudo-error.



1.2 Usage Method for Design Guide

(1) New IP

Chapter 2 onwards has relevant details.

(2) Reuse IP

Chapter 4 onwards has relevant details.

Please refer to Chapter 2 & 3 for confirming design information of original diversions.

2. Architecture

Design Input	Standards, bus specifications, design basics etc.
Design Output	Determined by the clock ratio. Reasons for adopting the clock ratio (Including fixing and changing). Constraints due to standards and bus/IF and power consumption mode etc are stated in the document.

2.1 Clock Configuration Review

2.1.1 Detemining Clock Frequency, Clock Ratio

This, without exception, is determined by SoC specification and Module specification.
Ex) Video input: For CCIR656 support 27MHz, bus clock becomes the clock frequency of Shwy in case of Shwy adoption.

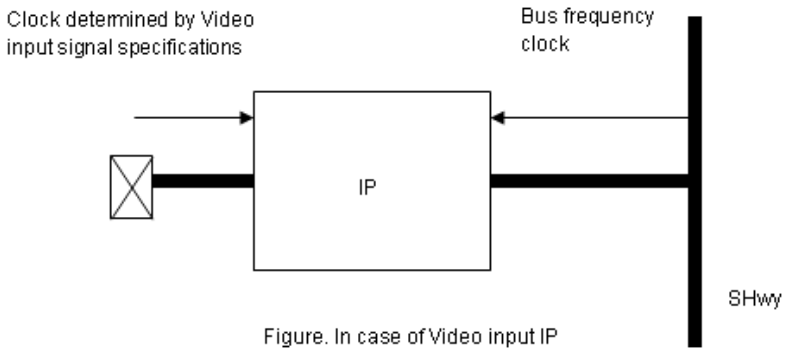


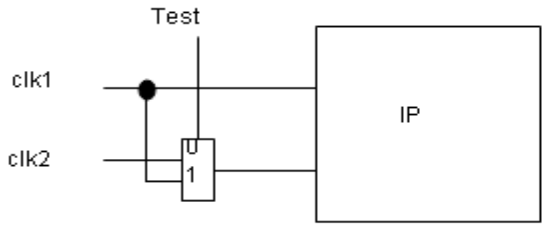
Figure. In case of Video input IP

2.1.2 Determining `Fixed` or `Changed` by Clock Ratio

Case that can be changed: If bus clock can be changed in another SoC, future scalability is considered while making regulation for scope of change in the clock. Meanwhile, if the IP (processor system) not having external IF, has asynchronous IF, then the bus frequency restrictions are released but 3 issues related to testing remain. However, the advantage in the above is that, frequency optimization can be done.

2.1.3 About Clock Integration during Testing.

First the necessity for specifying the clock type in the DFT and tester constraints is acknowledged. Following this, the tools and tester are confirmed and clock integration is reviewed.



Normal mode: There is asynchronous signal transfer between clk1 and clk2

Test mode: Synchronous circuit of entire clk1

2.1.4 Metastability Issues

In case of high frequency, it is necessary to review the stabilization duration of Metastability. Also, the normal transmission is more than 500MHz, but the standard transmission must be confirmed in ratio to gate delay. Especially so, since in the recent years the drive power and area of inverter of feedback of Flip/Flop in fine processors have reduced.

For details refer to Appendix Metastability.

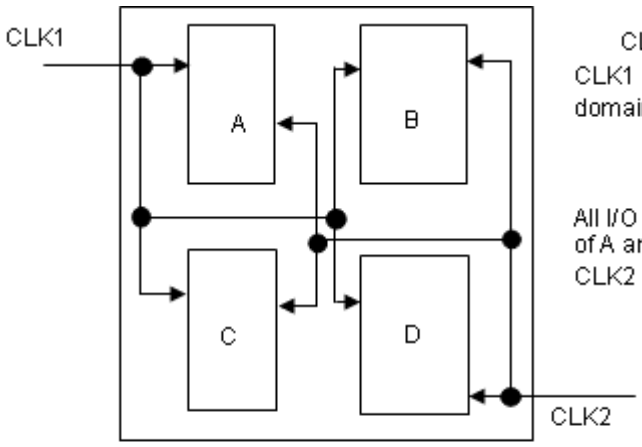
2.2 Clock/Block Division

Design Input	Clock configuration verification result, Module division plan
Design Output	1. The document contains information of process category and the corresponding domain for implementation, along with the reasons. (Performance evaluation, power consumption evaluation, and design verification facility evaluation etc.) 2. The document also contains asynchronous signal transfer circuit hid in sub-module of IP as sub-module configuration diagram.

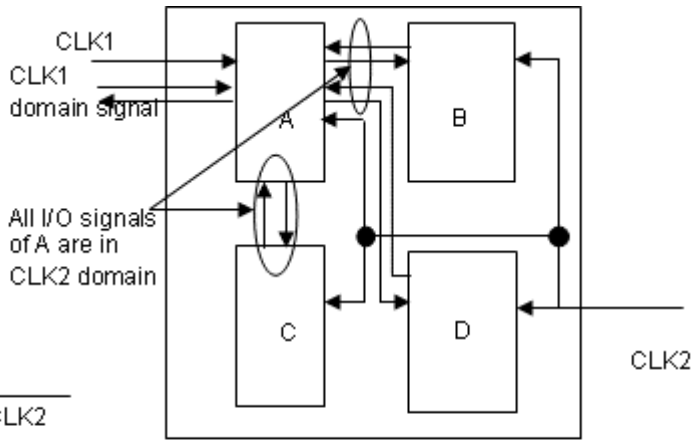
2.2.1 Most Important Features in Asynchronous Circuit Design

The most important feature in asynchronous circuit design is the hid circuit of asynchronous signal transfer in the sub-module of IP.

This leads to a sharp decrease in the number of errors, simplifies verification, clarity of operation status (clock ratio and enable timing etc), reliability up etc and numerous other benefits. As for the asynchronous design verification, architectural level review is exceedingly important as the downstream process requires substantial man-hours of effort.



Example of bad circuit
(Signals between modules are integrated with CLK1 and CLK2 domain signals.)



Example of good circuit
(Clock transfer is localized to sub module A)

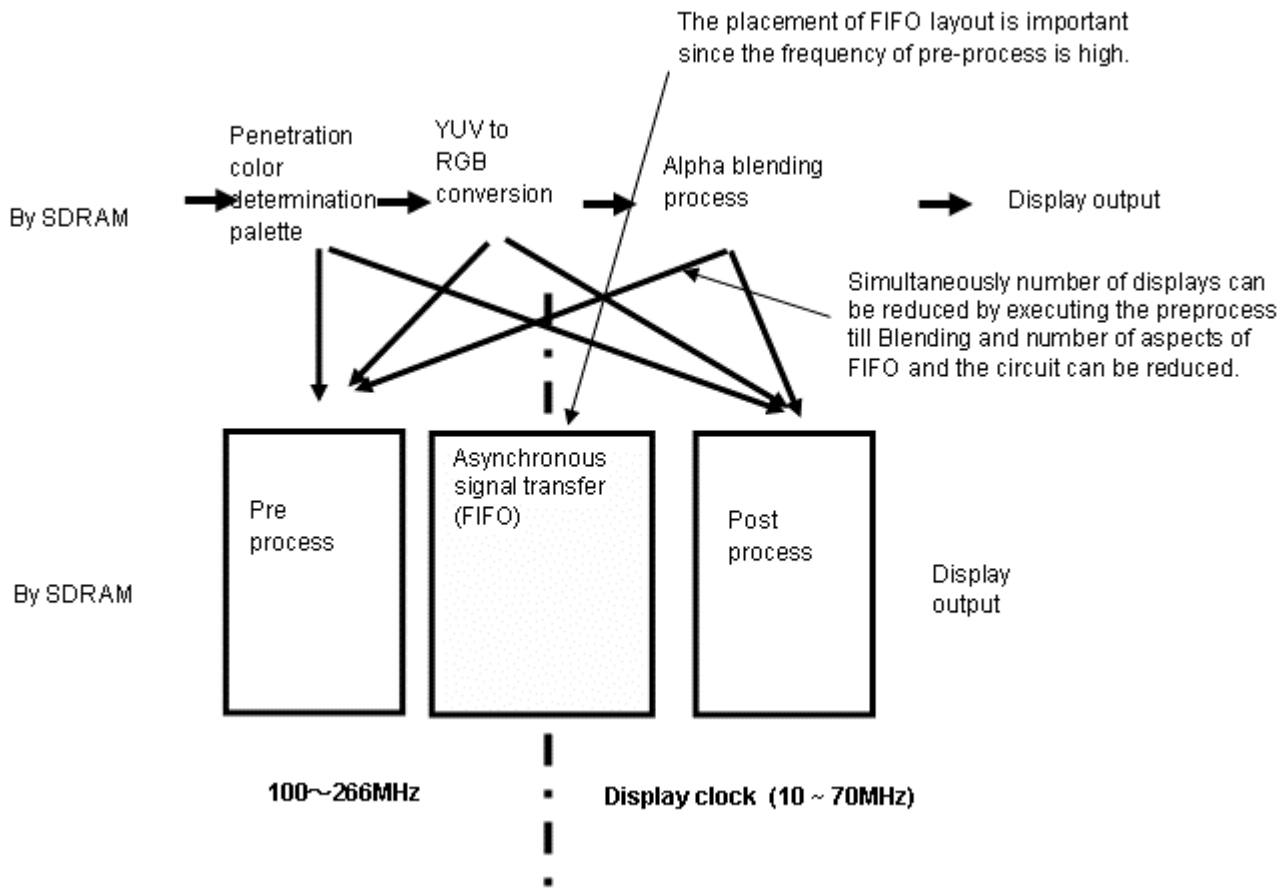
2.2.2 Example of Review Sequence

(1) Determines the process and the corresponding domain. The following standards must be selected and reviewed.

Significance of Power: Processing has increased while the clock domain is low-speed.
Significance of Latency: The total latency of the design is at minimum.
Significance of Design Simplicity: Least number of signals in asynchronous signal transfer. Minimum signals should be combined.
Simplification of Layout: long wires on the layout of high clock side should be short.
Simplification in Testing: Review of clock switch at the test.

Are there any problems in clock tree configuration on Layout?

Example of Block division: Display from SDRAM



Verify the process and the corresponding clock domain for implementation.

(2) Reason for induction is stated.

(Importance of Performance (significance of latency), significance of power, Design simplification, Layout simplification)

Example)

SCIF (asynchronous communication): Over sampling of input single signal and later; all designs are with synchronous circuit.

SSI (=I2S): Due to 3-wire communication of SCK, WS, Data, signal undergoes serial parallel conversion, and synchronization takes place. (See figure below)

VIN: Due to parallel bus signal (8 bit) and input clock, data is incorporated in input clock. Later, since throughput of digital filter is frequent, hence the synchronization with frequency of IF bus is carried out immediately.

DU: Based on performance or power consumption, the process contents of SHwy clock and Dotclk contain various alternatives. (Refer to the chart on the previous page)

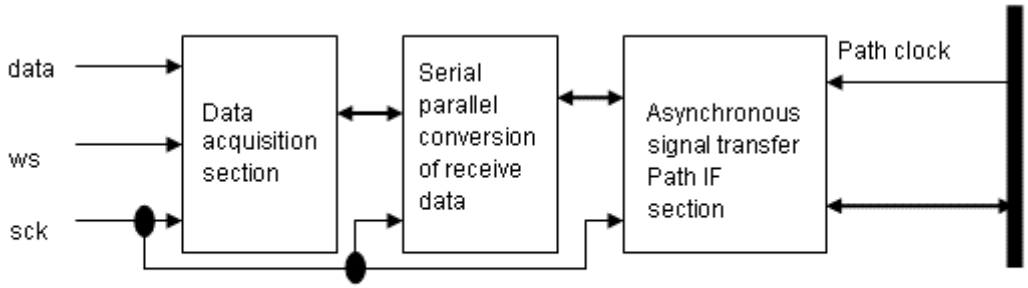


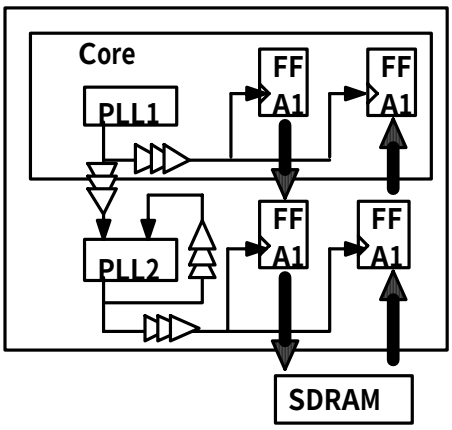
Figure. Example of SSI

2.3 Instructions for Clock Generation using PLL

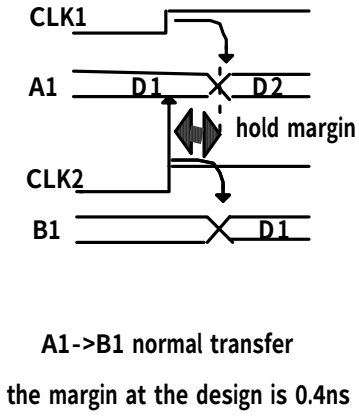
The reference clock of PLL and generated clock should be treated asynchronously.

Especially, if the data transfer is executed between the PLL clock systems with cascading connection, Asynchronous design needs.

The reason being, that since the timing design is created without considereing the clock jitter (fluctuation) and phase difference; hence the data transfer malfunction occurs due to insufficient holding margin etc.

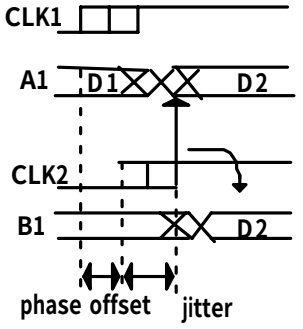


data transfer



A1->B1 normal transfer

the margin at the design is 0.4ns



A1->B1 abnormal transfer

the jitter is +1ns or -1ns

timing of transfer

Here, the clock phase is aligned by PLL and synchronous design is required due to emphasis on performance. Thus, special note should be taken of the points stated below.

(1) Appropriate attention should be given towards design, in order to achieve minimum output jitter for PLL1 & 2. Also, the power supply and core power supply distribution to PLL1 &2, hard-wiring for each module must be taken into consideration.

(2) Confirm there is sufficient setup and hold timing in clock transfer, by carrying out adjustment for reversed-phase + normal phase, and considering jitter value.

(3) Test the fluctuation for AC core power supply, check PLL1, 2 phase jitter and recurrence period jitter to confirm whether or not the timing margin of reversed phase of 2 is sufficient. Here, jitter is classified as Random jitter and Deterministic jitter. Random jitter utilizes n to achieve the system permissible error rate and evaluates it.

Further, the increase in monitoring points will result in increase in the jitter. The temperature (impact of low and high temperatures) also must be checked.

Tj(p-p value) = n × Rj (rms value) + Dj (p-p value)

Tj = Total jitter, Rj = Random jitter, Dj = Deterministic jitter

3. Function Logic Design

Design Input	Clock configuration of architecture, result of block division
Design Output	Classification of all the signals of asynchronous signal transfer in to single signals and multiple signals. The resons are also stated here. In case single signal, state the maximum frequency. In case of multiple signals specify the maximum frequency, burst specification (burst length) and enable (signal that indicates valid multiple signals.) specification in the document.

3.1 Category of Asynchronous Circuit

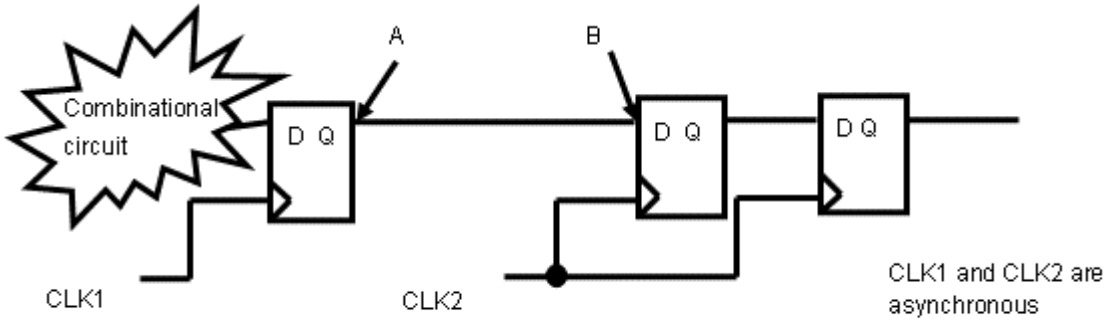
(1) Categorizes single signal and multiple signals. The circuit of single signal is vastly different from the circuit of multiple signals, hence the classification is important.
(2) Check and confirm the maximum frequency. This is necessary for identifying whether transmit side data can obtain the clock value of receive side. In case of multiple signals, in order to synchronize enable signal, the frequency becomes equivalent to the maximum frequency of valid duration of enable signal. Further, the selections of circuit configuration changes, if the transmit side: receive side clock ratio is other than 1:3(more).
(3) When the clock ratio is less than 1:3, it is necessary to adopt double buffer etc. The buffer depth is determined by signal burst specification. (For details refer Reference Data)

3.2 Asynchronous Circuit Classification and Circuit Adoption

The document must contain information regarding selection of circuit configuration and its reason. Includes the Timing Chart of the signal that passes through the circuit shown above.

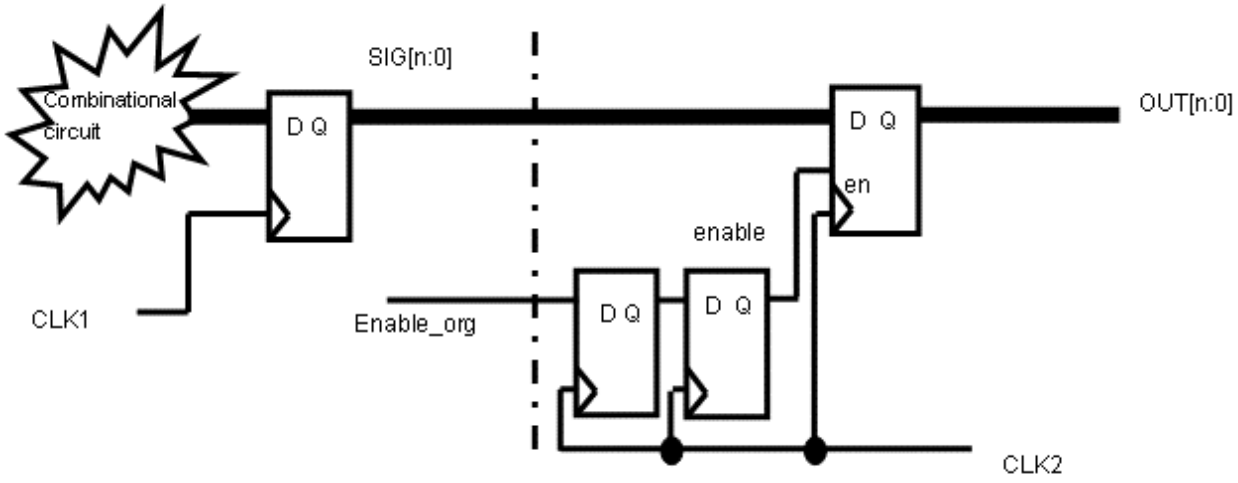
Signal	Detailed classification	Circuit
Single Signal		2flopped (metastability countermeasure) (Basic format 1)
Multiple Signals	Send signal: Clock ratio of receive side is more than 1:3.	Incorporated by FLIP/FLOP and enable signal (Basic format 2)
	Send signal: Clock ratio of receive side is less than 1:3.	FIFO or double buffer configuration and a control circuit (Basic format 3)
	Clock ratio Variable	Control circuit Request & acknowledge handshake (Basic format 4)

3.2.1 Basic Format 1: Synchronization of Single Signal



Asynchronous signal is 2 flopped in receive side clock, and corrected. (Metastability countermeasure)
Precaution 1: CLK1 and CLK 2 are different.
Precaution 2: Asynchronous signal transfer (A & B) to be connected directly. (Normal mode)
→Understanding of 2 reasons is necessary (1.Hazard prevention, 2. Combined error)
(For details refer Reference Data)
Precaution 3: Frequencies of CLK1 and CLK 2
When CLK1>CLK2, the pulse cannot be obtained.

3.2.2 Basic Format 2: Synchronization of Multiple Signals



(1) When using Basic Format 2, 3 & 4, the circuit is of **multiple signals** transfer, thus, **multiple signals** is specified as group in STAcheck. If group is not specified, circuit configuration cannot be checked. The Basic Format 2, 3 & 4 can be used for single signal also but, in order to check configuration in STAcheck, it is necessary to specify single signal in group.

(2) Whenever possible use the recommended circuit for multiple signals transfer, and also carry out Enable signal timing verification. The timing chart in the document should be treated as the design asset .

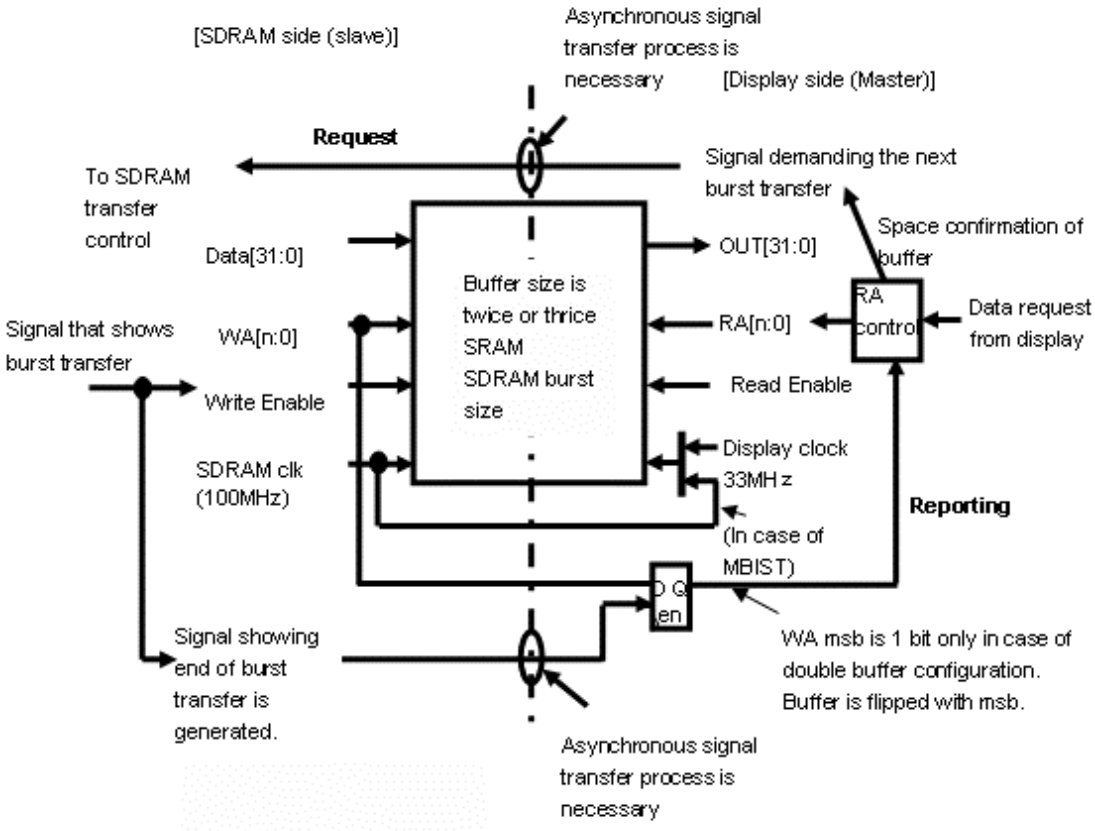
Timing relation cannot be checked in STAcheck.

3.2.3 Basic Format 3: Transfer using SRAM/FIFO

In this method, when clock on the synchronous side are three times or less than clock cycle at the transmission side, the synchronous signal frequency ratio is increased by 3 times, by using

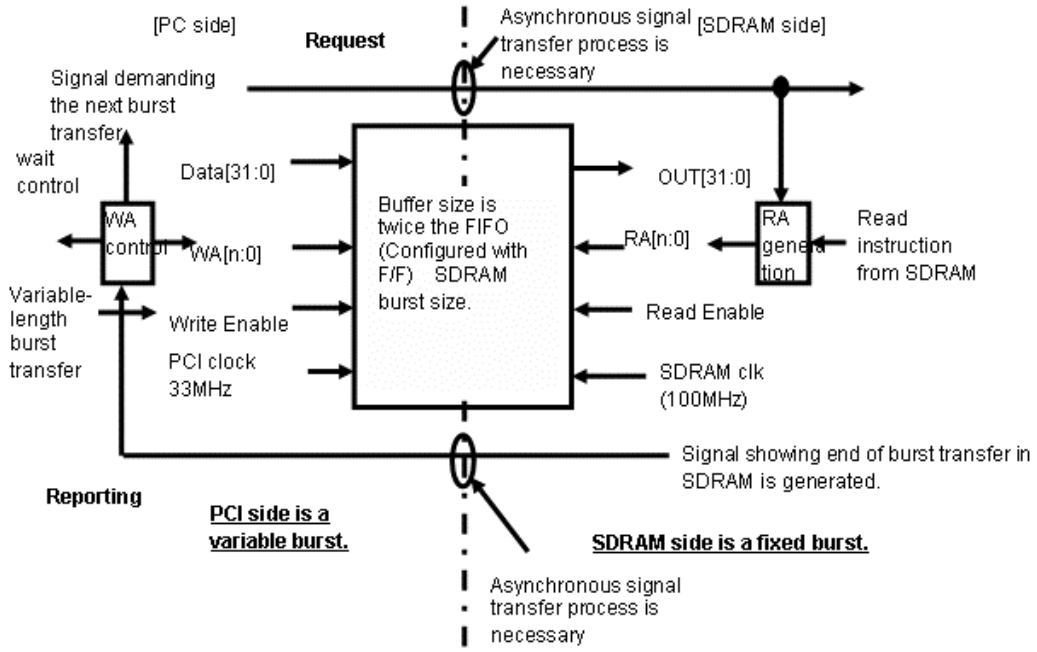
- FIFO for data buffering, and
- Corresponding flag (as following, equivalent to burst transfer request signals and burst transfer end signals.) in buffer full condition.

Example 1 Image signal display (Schematic diagram)



Timing diagram must be included in the document.

Example 2 PC target receive (Schematic diagram)

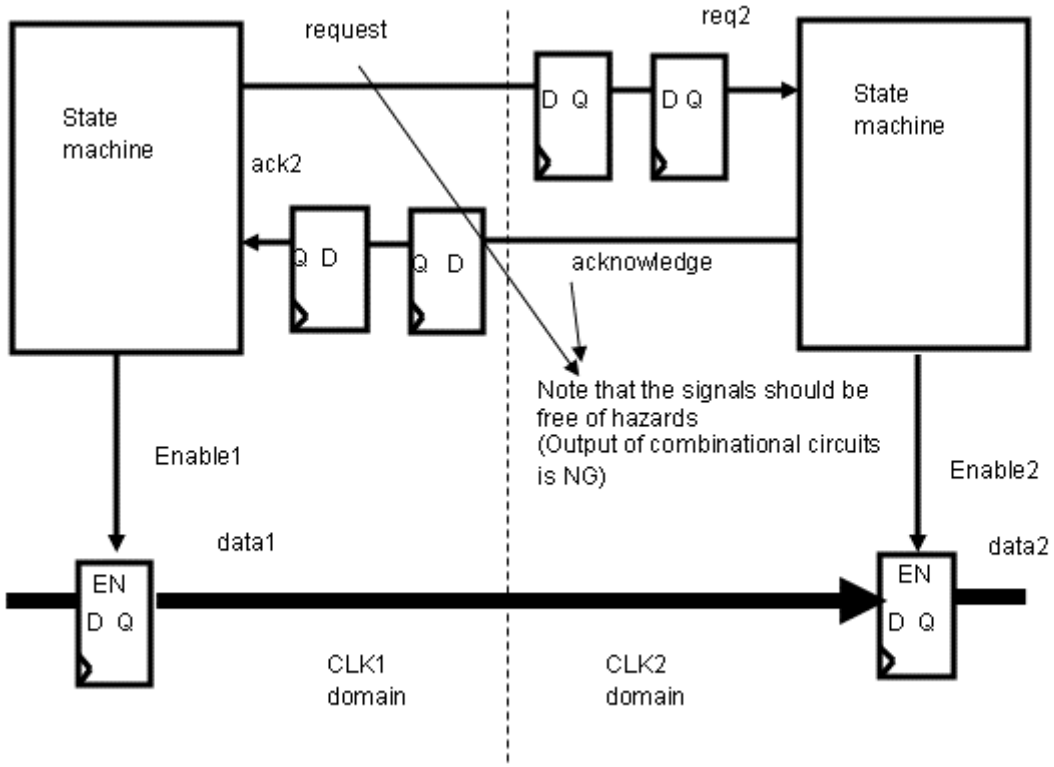


Timing diagram must be included in the document.

3.2.4 Basic Format 4: Development Pattern of Basic Format 2 (request-knowledge handshake)

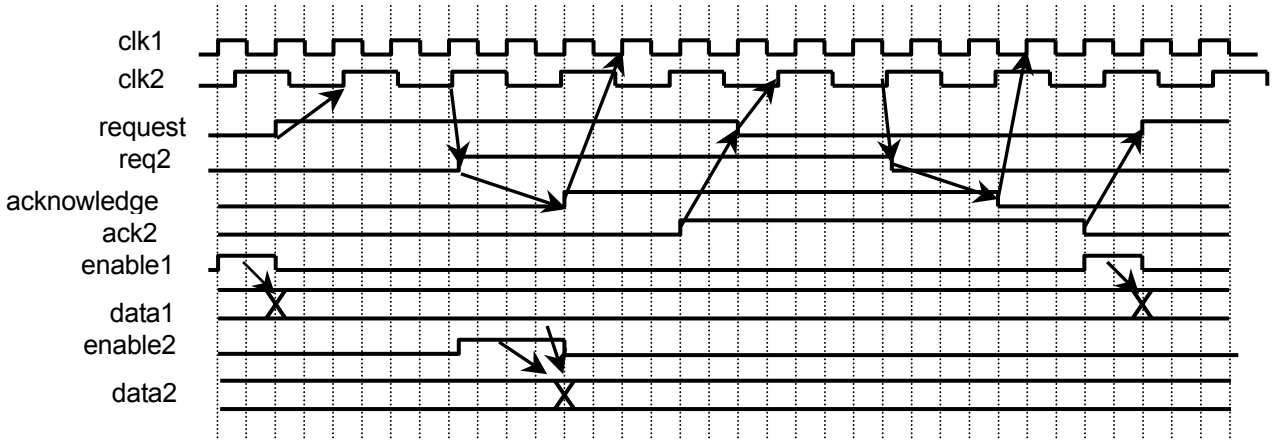
This is suitable when there is a change in the clock ratio of synchronization side and transmission side. However, there is an increase in latency and transfer pitch (interval).

Example for request-acknowledge



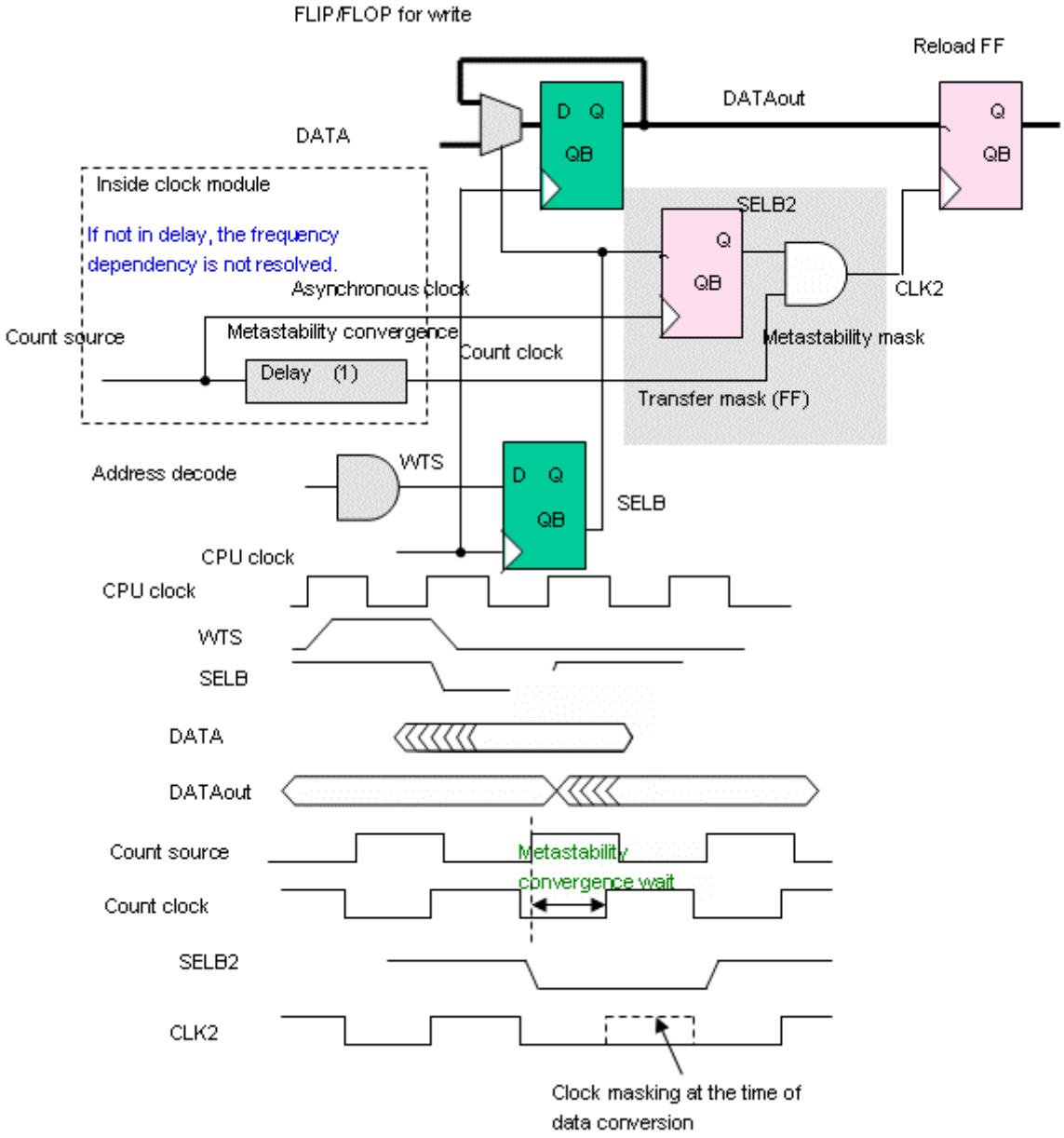
Flip/Flop enable is controlled using request and acknowledge handshake.

Timing chart is included in the design document.



3.2.5 Attentions for using Circuit for Application System

Besides the basic format explained here, there are asynchronous signal transfer circuits for specific reasons such as; decrease in power utilization and shortened latency.
When the circuit given below is adopted, there is a change in position of mask circuit due to re-synthesis which further causes trouble. Also, timing is assured by gate delay, the value of each processor must be confirmed.
When such a circuit is adopted, the circuit configuration and timing confirmation of the final gate layout are mandatory.



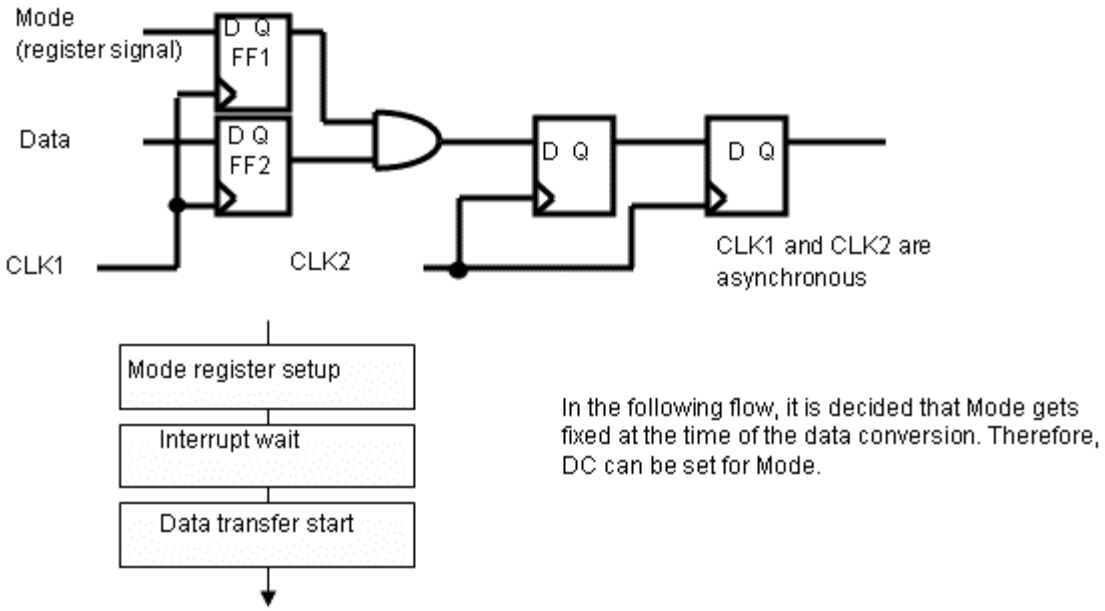
3.3 DC Signal in Asynchronous Signal Transfer

Design Input	Design of asynchronous signal transfer configuration
Design Output	DC signal elimination

The DC signal and its reasons are treated as part of proprietary design.
The pseudo-error can be reduced by registering DC signal in STAcheck of Check Status (like SDC) file.
Features for being considered as DC signal are:

(1) When the signals of asynchronous signal transfer change then the control signal of register is fixed to 0 or 1.
(2) When the signals of synchronous signal transfer change in software flow (Clear description in the manual is important.) then signal is fixed to 0 or 1. (Refer to the figure below).

Other items and reasons are also included in the document.
(Comments to be inserted in Check Status (like SDC) file is recommended.)



Asynchronous Signal Transfer Circuit and Software Procedure

4. RTL, Gate Verification

4.1 STAcheck Trial

Design Input	All design results of asynchronous signal transfer configuration and RTL
Design Output	The number of genuine errors is identified using DC signal and the workload of following process is estimated. STAcheck can input RTL or temporary combined gate netlist.

(1) For New Design
The process for verifying whether or not the results of architecture and function logic design was correct. Here, the input for verification of asynchronous signal transfer circuit diagram, timing chart and DC signal specification is collected in advance. Later, the process of confirming whether or not all the concepts were incorporated requires extra effort.

(2) Reuse Design
This process may require substantial time, if IP does not perform as asynchronous circuit.

In either of the case of (1), (2), firstly, confirm the error number and circuit position number pointed out in STAcheck. Based on this, the required work will be estimated.

While executing STAcheck, use DC signal for deleting pseudo errors. (For details refer to STAcheck manuals.). As a result, the number of errors may reduce greatly, and only error candidate needing the confirmation of signal and timing is extracted

According to the analogy of the test results obtained, the error number and circuit position number pointed out is 1:20 ~ 1:50(the reason being, in case of error in bus system signal, error is counted for all bits), hence if the number of errors is hundred or less, then the confirmation and correction are not difficult, and about 2000 cases can be handled. For a number above this, one requires considerable time, effort and a detailed workaround.

As for current faults, the root cause being that STAcheck is executed just before 1stSignOFlip/Flop, and for large number of errors, OK is indicated based on vague (unclear) results. The key to resolving this problem is to ensure appropriate support by STAcheck execution of IP unit in early design stage. Therefore it is recommended that person responsible for design should test STAcheck in the early design stage.

So far, authenticity of error of the reuse IP was not able to be judged and even the true error was not able to revise by oneself. There is no direct means to solve the problem other than a thorough circuit analysis. However, by applying STAcheck (DC signal application) in the early design stage, the genuine errors are detected. Also, by raising alarm early and gaining grace time till 1stSignOff, expert opinion can be obtained, which is necessary for setting up a line of action for resolving the problem.

The flow to reuse timing chart and documents (circuit diagram, clock definition, single signal, multiple signal definition) and STAcheck results (including check condition (like SDC) file) which are design output of the IP is recommended. The reason is because it can largely reduce the man-hour efforts.
Executed STAcheck result of each IP promotes reuse of IP.

4.2 Preparation for legacy IP verification

Design Input	All design results of asynchronous signal transfer configuration and RTL
Design Output	Case1: When design document of asynchronous signal transfer configuration is available; single/multiple signal classification, circuit configuration, timing chart, data related to DC signal specification is available or can be created. Case2: Follow the steps given below in case of absence of design document of asynchronous signal transfer configuration. 1. First, the asynchronous signal transfer circuit diagram is set up. Specify signal of asynchronous signal transfer. Create circuit configuration and classification of single/multiple signals. 2. Create clock ratio, block configuration diagram. Also verify metastability. 3. Create single/multiple signal classification, confirmation of circuit configuration and time chart with RTL simulation. 4. DC signal candidate is identified in IP specifications and manual.

4.2.1 Design document is available

Design document of Chapter 1.2 is available. It can be created when required.

4.2.2 Design document is not available

(1) First, the asynchronous signal transfer circuit diagram is set up. Specify signal of asynchronous signal transfer. Then create the under mentioned documents.

- Classification of single/multiple signal for all signals of asynchronous signal transfer, and its reasons.
- Selection of circuit configuration, and its reasons.
  ex1. Flip/Flop and enable
  ex2. FIFO and enable
  ex3. Double buffer etc and its enable
  ex4. If clock ratio is variable, the circuit for synchronization of handshake signal of req-ack is usually used.

(2) The clock ratio is treated as clock configuration. The document consists of information about whether or not the clock ratio can be fixed.
If the transfer circuit is concealed in the sub-module in IP, it must be stated in the document.

(3) Create the following documents as per RTL simulation.

a. When signal for asynchronous signal transfer is single signal:
   Mention the maximum frequency of that signal.
b. When signal for asynchronous signal transfer is multiple signal:
   Mention the maximum frequency, burst specifications (is there a burst length) and enable (signal that shows multiple signals are valid) specifications of that signal.

Also, describes those signals in timing chart, when multiple signals pass with enable and handshake generation circuit.

(4) Analyze error in STAcheck and extract DC signal.

4.3 STAcheck Verification

Design Input	All design results of asynchronous signal transfer configuration and RTL
Design Output	The change in DC signal specification, Group specification, and circuit will be executed till any of the below mentioned state is achieved. 1. Error 0 2. When the cycle slippage position is stated, the presence of the problem of cycle slippage is confirmed with the timing chart and Sim base and stated in the document. 3. When the location for occurrence of hazards is mentioned, it is not captured and that there is not influence is stated in the document. (Timing chart is necessary). Also, when metastability occurring location is stated, F/F frequency and metastability stabilization duration is confirmed.

Addition of DC signal is estimated from the DC signal candidate list of log of STAcheck. For details refer to STAcheck manual.

Regarding analog/digital mixed circuit; for example, for checking asynchronous signal transfer circuit of high-speed IF, DLL etc, it is necessary to check while the circuit is in digital and combined condition (only modules included in asynchronous signal transfer circuit) due to Verilog in analog behavior.

4.3.1 Check Flow

In STAcheck, asynchronous transfer is checked in code D005.
First, check is performed in D005-01 to determine if asynchronous circuit is added at the time of asynchronous transfer. Thereafter, check for the correct synchronization circuit is performed in D005-02 during single/multiple signals transfer. Lastly, D005-03 is used to check whether or not any cycle slippage hazard exists.

(1) Step1: D005-01 Synchronization circuit Check

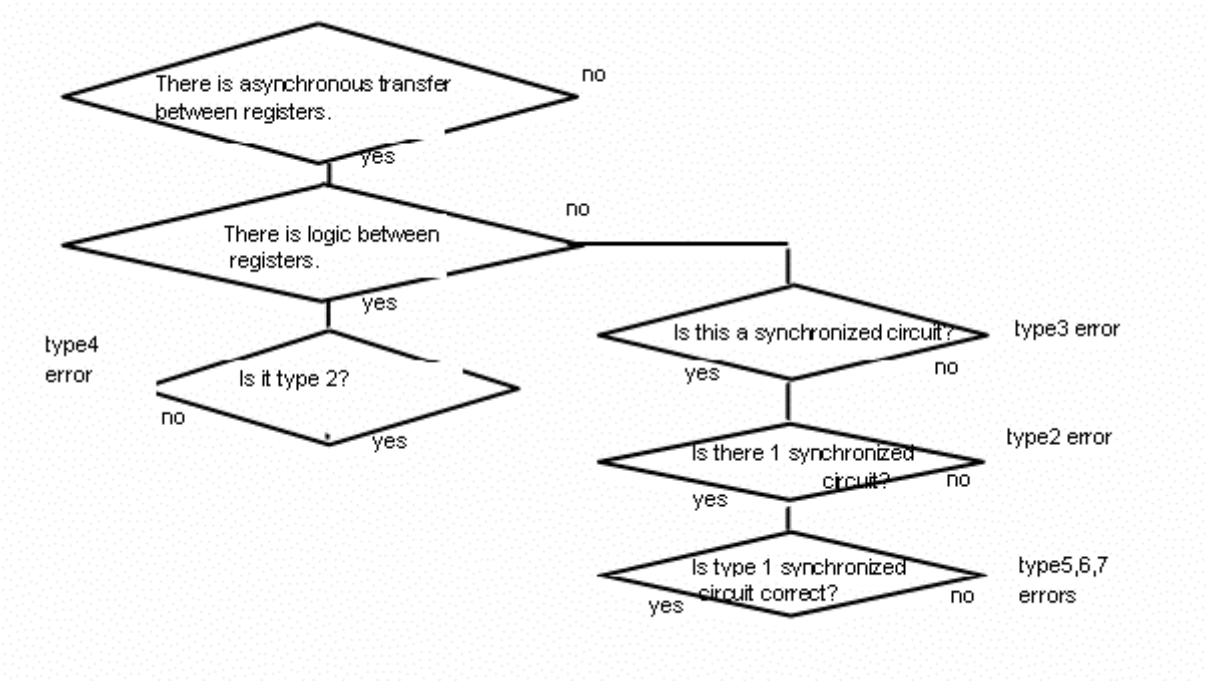
Check for confirming if synchronization circuit is added for signal with asynchronous transfer.
Also, when the error is output so that there is the logic in asynchronous transfer interval (type4), pseudo error can be deleted by DC signal specification or command option.

< Check contents of D005-01 >

- type2: 2 or more synchronization circuit exist for 1 signal.
- type3: Incomplete or no synchronization circuit.
  - type3-1: Receive side is latch and hard module.(first stage is not Flip/Flop)
  - type3-2: Other circuit uses output signal of stage 1 of the stage 2 Flip/Flop of synchronization midstream.
- type4: Logic exists in asynchronous transfer interval.
- type5: Synchronization with a different clock.
  - type5-1: reverse clock
  - type5-2: difference clock in synchronization
  - type5: asynchronization clock
- type6: The clock has not reached the clock terminal of 2nd stage Flip/Flop cell.
- type7: The output of 1st stage Flip/Flop cell connects it other than the data terminal of 2nd stage.

<Check sequence>

1. STAcheck extracts the asynchronous transfer between registers.
2. If there is a circuit in asynchronous transfer interval, check if it is in synchronous circuit basic format 2 of multiple signal transfer or in type4 error whitch there is logic in asynchronous transfer interval.
3. Check if stage 2 Flip/Flop synchronous circuit is correct.
4. Check whether there are type 2 synchronization circuits more than 2 in that signal, if no logic exists in asynchronous transfer interval.
5. Finally, check stage 2 Flip/Flop (type5, 6, 7) of synchronization circuit basic format 1 of single signal transfer.



(1-1) DC Signal specification

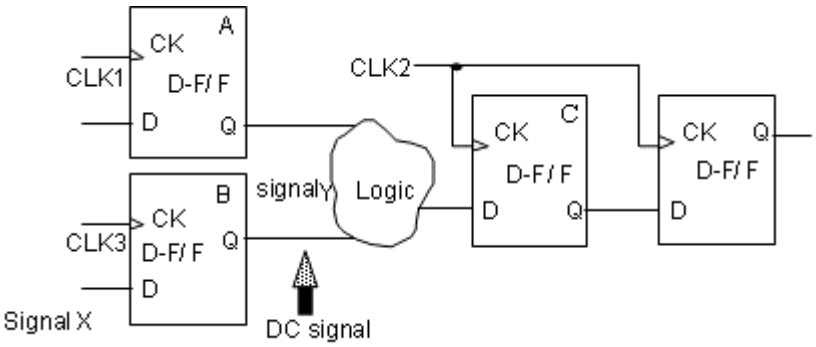
type4 D005-01: If there is logic in asynchronous transfer interval, pseudo errors are deleted by DC signal specification, and the genuine error is identified.

After the reset of the diagram given below is released, signal from B is fixed in either 1 or 0. Problem is not encountered in the following two conditions:

- When there is no change in the signal from transmission side B at the time of asynchronous transfer from transmission side A.
- When the value immediately after change of transmission side B is not used in receive side C by specification control (soft flow) etc.

In this case, the impact from transmission side B is removed by specifying DC signal in register B of transmission side.

In the figure below, set_strings DC_SIGNAL B.Q; is specified in the check status (Like SDC) file. However, X, Y, B.D used in place of B.Q can also obtain the same results.



<Merits of DC signal>

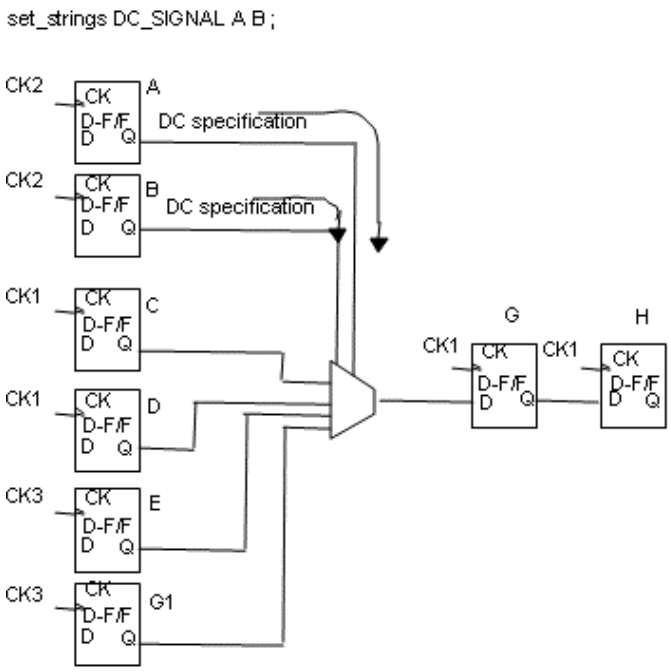
If DC signal etc is not specified, D005-01 type 4 (logic in asynchronous transfer midstream) error occurs. If A & B are specified in DC signal, DC signal is transmitted till selector terminal and it checks for asynchronous transfer in each case of 1 and 0. In the figure below if DC signal is set, the transfer from C-F to G is divided into 4 parts. The transfer from E to G and F to G is direct transfer, and is recognized as circuit of synchronization circuit basic format 1. The transfer from C and D to F is synchronous transfer; hence the circuit given below is recognized as circuit without errors.

set_strings Cancel_D005_01_from_reg_outnet A B;

When A & B are specified by method (Cancel_D005_01_from_reg_outnet) used for excluding the register that does not operate, the transfer from A & B is excluded from the check but, in transfer from E & F, D005-01 error which has the logic in asynchronous transfer interval is output.

Also, when DC signals of A & B are fixed in {0, 0}, only the transfer from F to G is checked. Because transfer from E to G is not checked it becomes a check leakage. In elementary signal fixing, check that set 4 following patterns in A & B is necessary.

{0, 0}, {0, 1}, {1, 0}, {1, 1}

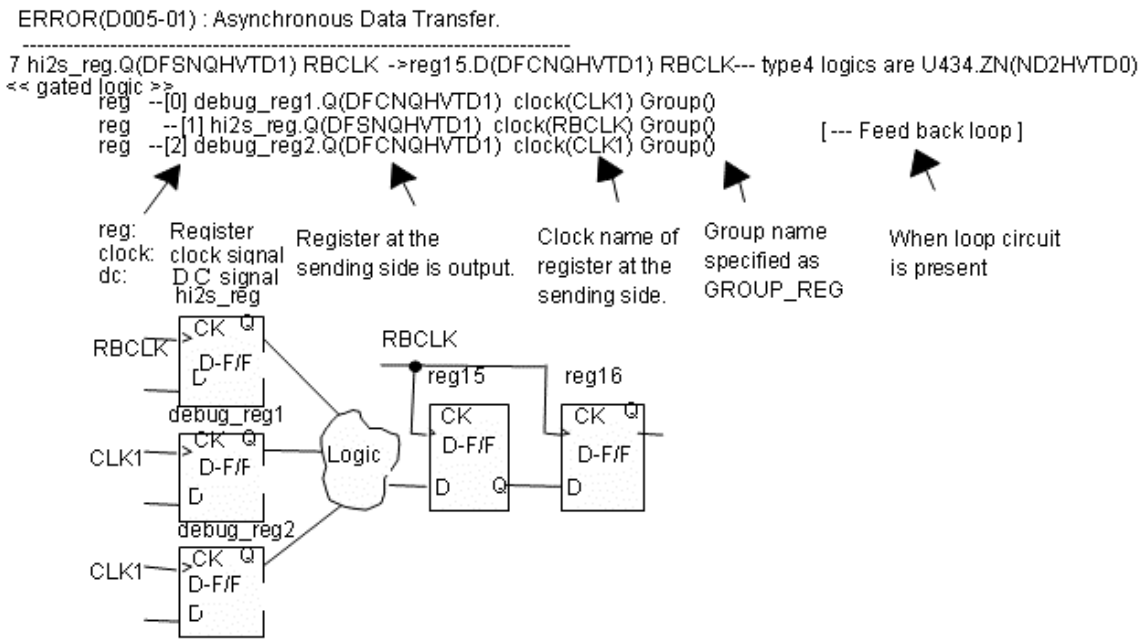


<DC signal candidate find method >

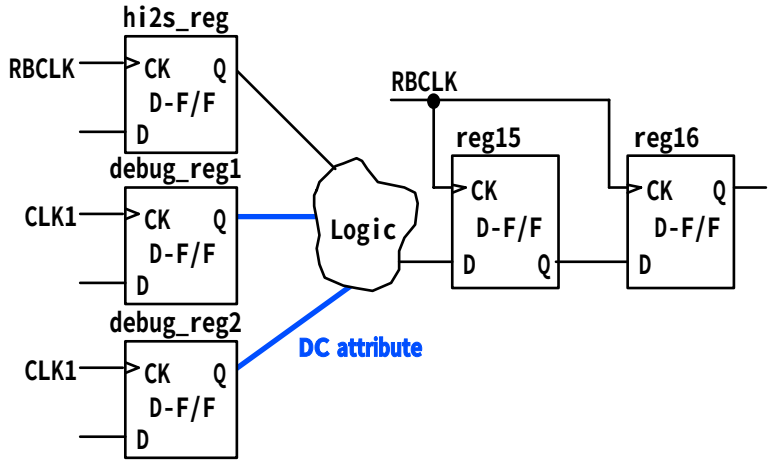
Confirm whether or not it is pseudo error due of DC signal from the error message (log.stacheck) regarding transmission side register.

In the figure below, transmission side register list and its information is output for receive side register of reg15.D.

Check whether or not there is DC signal inside that register.



In case of DC signal, if debug_reg*, specifies the following in the check status (like SDC) file.
set_strings DC_SIGNAL debug_reg*.Q ;
The impact of debug_reg* is ignored and only transfer from hi2s_reg.Q to reg15.D is checked. If DC signal candidate is not output, specify -NOT_PRT_D005_01_LOGIC_CONE in the command.



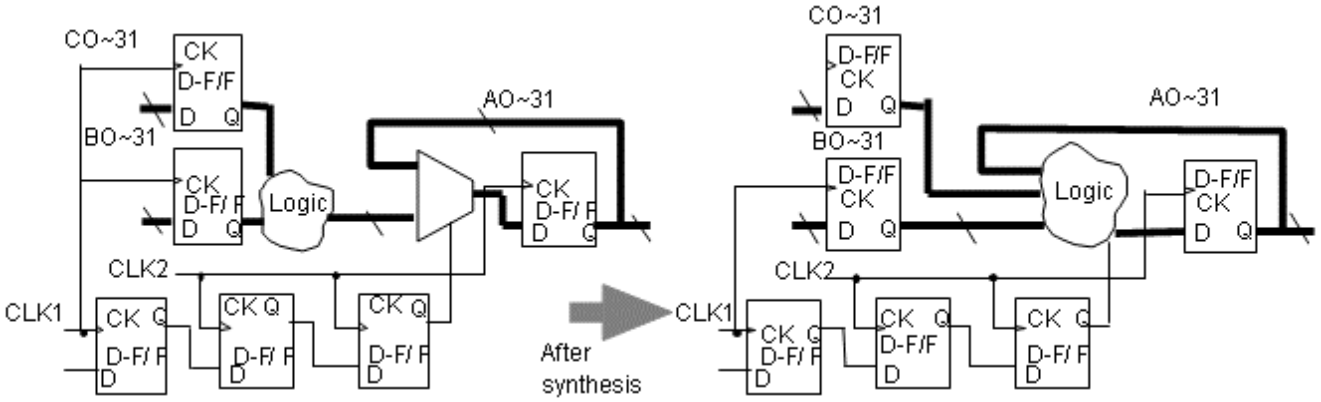
(1-2) Specification for excluding transformation circuit

By the following command options, The transformation type of synchronization circuit is recognized and pseudo error is eliminated and genuine error is found.

-D005_01_AND_OR_SYNCRO
In the synchronization logic of multiple signals, there are cases where selector analyses AND or OR gate with logic synthesis. Here, using this option is necessary, as the original selector cannot recognize STAcheck when gates are optimized during synthesis.

<Error exclusion status when this option is specified>
- On the receive side register A0-13 (see figure below), the output is the feedback to its own data terminal.
- GROUP_REG of control file contains information regarding multiple transfer. Also, B0-31 and C0-31 are identical groups.

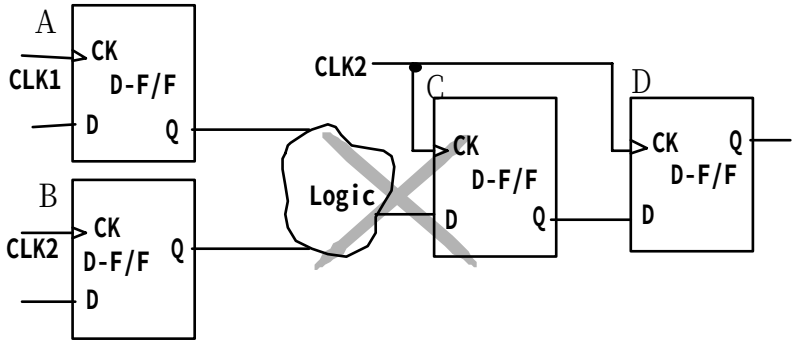
Specification method of GROUP_REG (control file)
First the transmission side register name, secondly group name of multiple transfer is specified.
Example)
set_strings GROUP_REG B* ASYNC1 ;
set_strings GROUP_REG C* ASYNC1 ;



-D005_01_SYNC_CONE

As shown in the figure below, if the signal from B is synchronous signal, the hazard is not captured, then no problem occurs in asynchronous transfer. (Only when CLK1 output is 1 FF, and when signal from CLK2 output operates as mask logic). However, because the signal of A which is masked by asynchronous signal B is not suitable, incorporating mask logic of B is necessary, for output signal of D after synchronization.

However, when the net is not modified and this circuit is treated as synchronous circuit, this option is specified.



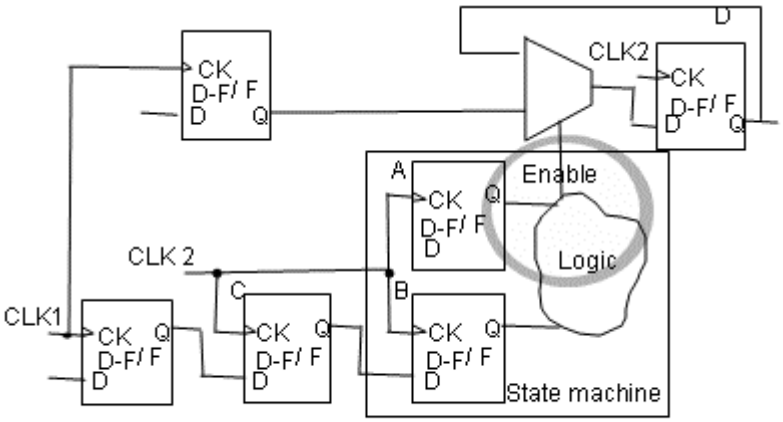
-D005_01_EN_ASYNC_CIRCUIT_TYPE

In the synchronization circuit format using enable of multiple signals, there is the case that combinational logic exist in the signal of selector, as showing in following figure.

In STAcheck, enable of asynchronous transfer circuit of multiple signals assumes absence of combinational logic as the main criteria. Thus, please specify

-D005_01_EN_ASYNC_CIRCUIT_TYPE 3

when hand shake circuit format as given in the figure below is used.

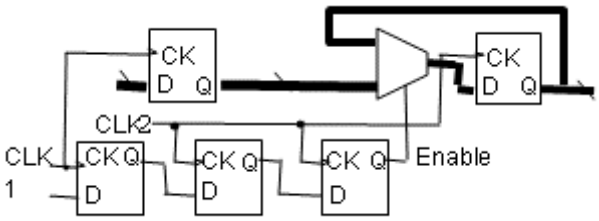


Case of -D005_01_EN_ASYNC_CIRCUIT_TYPE 3

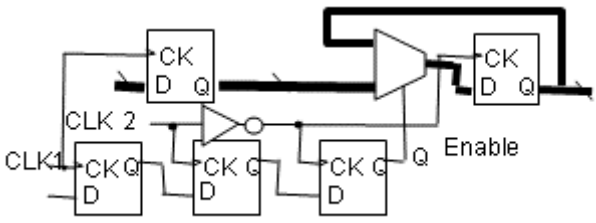
-D005_01_EN_ASYNC_CIRCUIT_TYPE

Check option of Enable logic

1(default): Only stage 2 F/F synchronization circuit. And the clock is identical to the clock of two F/F.



2: Only stage 2 Flip/Flop synchronization circuit. And two Flip/Flop clocks are synchronous clocks including reverse clock.



3: (Refer to TYPE3 figure on earlier page) Backtracking from enable signal, same as A and B, the clock of stage 1 Flip/Flop is synchronous with the clock of Flip/Flop D of **推奨** the receive side. Moreover, same as C and B, there is stage 2 FLIP/FLOP synchronization circuit and two Flip/Flop clocks are synchronous clocks including reverse clock.

4: Enable logic is not checked.

(2) Step2:D005-02 Synchronization of multiple signal transfer

Check whether synchronization circuit transfer is correct. Check whether synchronous circuit identified in D005-01 is single input signal or multiple input signals as per the group specification of the check status (Like SDC) file.

Though the cycle slippage of signal convergence in D005-03 is checked but, the cycle slippage problem will exist even if bus signals etc are not converged. After the bus signal was synchronized in 2 step of flip-flops circuit, it is the circuit which is output from the corresponding block. In this case, the synchronization circuit is checked for confirming that it is in accordance with the specifications. Hence it is necessary to specify single signal and multiple signals in GROUP_REG. In D005-02, check is performed to confirm whether GROUP_REG specification and enable signal interact directly and whether 2 step of flip-flops circuits are applicable for multiple signals as group. In case of error in D005-01, the check target is not present in D005-02.

GROUP_REG specification is used for the following.

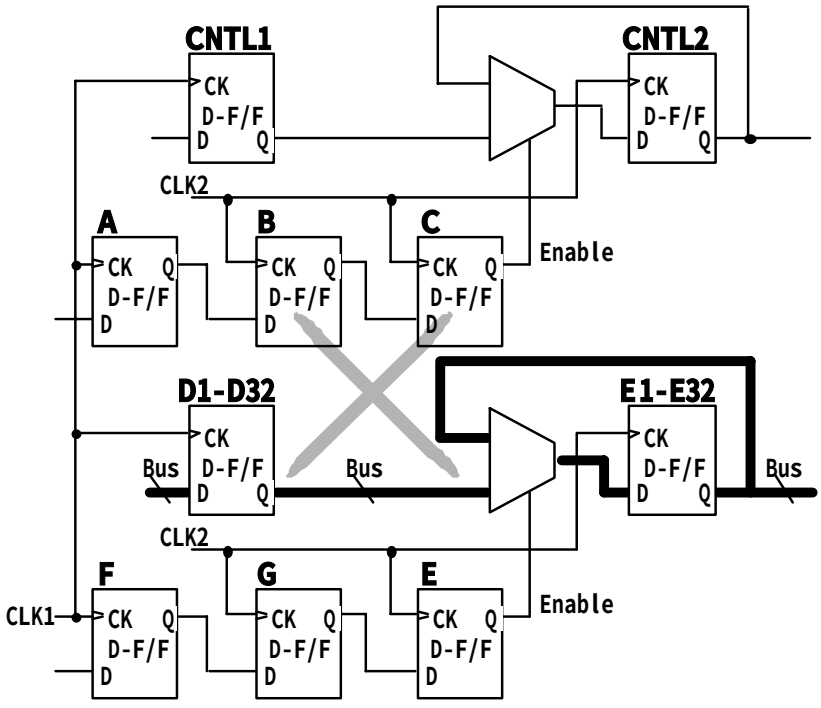
1. D005-02 check
2. When basic format 2 selector in D005-01 analyses AND-OR, circuit identification

On the second check, -D005_01_AND_OR_SYNCRO command option is specified.

Also, when GROUP_REG is not specified, the default group name that it was supposed that all synchronous circuits are the same groups is used.

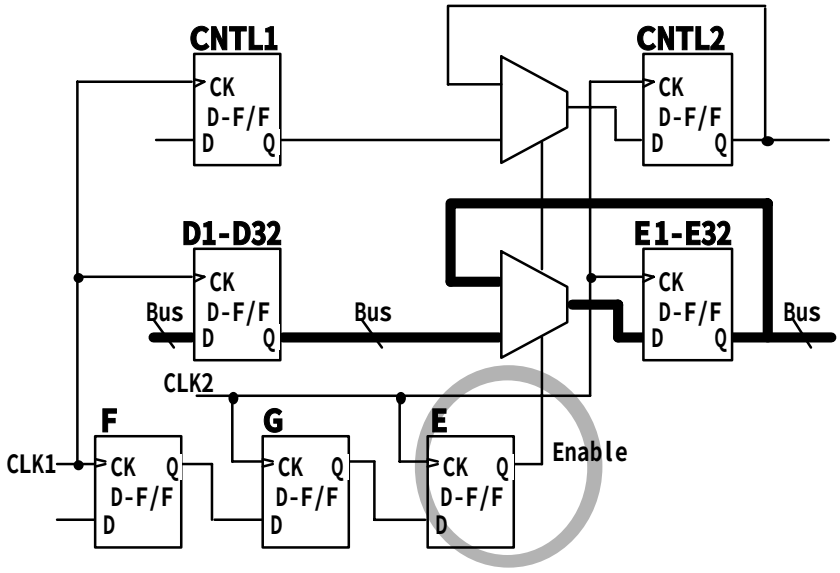
Example)

```
set_strings GROUP_REG CNTL1 ASYNC1   ;
set_strings GROUP_REG   D*    ASYNC1   ;
```



Circuit where trouble has occurred

In the above figure, even though CNTL1 and D1-D32 are in the same group (ASYNC1 is multiple signals), enable signal is generated separately, hence cycle slippage occurs, and results in NG.

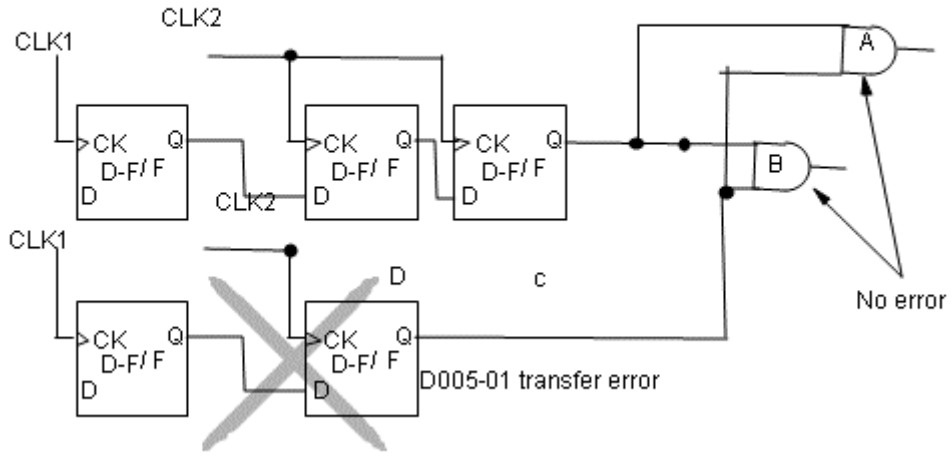


Good Circuit

(3) Step3:D005-03 Cycle slippage in signal convergence by different synchronization circuit

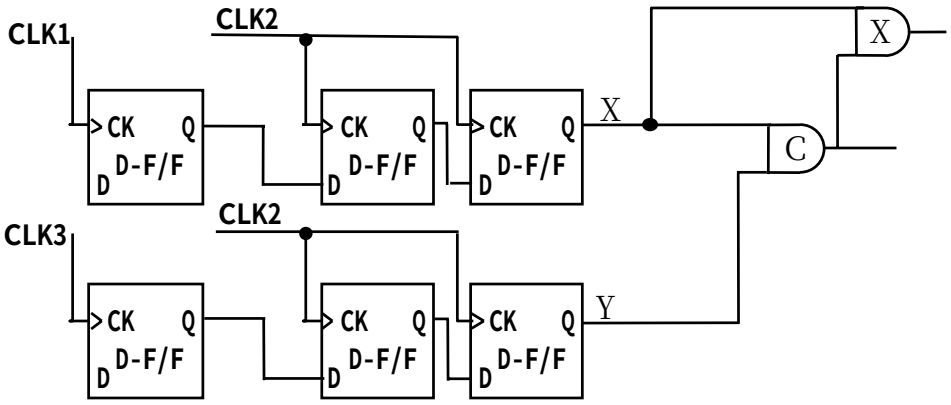
According to the specifications in D005-02, synchronization of multiple signal transfer is checked, but there is error in D005-03, if there is mistake in the group specification of the check status (like SDC) file or if there is an unplanned convergence as shown in the figure below.

In the figure below, when single input signal is specified in group specification of the check status (Like SDC) file, there is no error in D005-02. However, there is a risk of cycle slippage and if operational problems are led, then change to synchronization circuit for multiple signal transfer is necessary.



Further, in the circuit shown above, if there is not synchronization circuit (D005-01 error), the signal from D is out of scope for D005-03 check. Accordingly, the convergence of signal from D is out of scope for D005-03 check. It is Default.
For making it check the target, add
-D005_03_D005_01ERR
in the command.

As in the figure below, if clock of the transmission side or the reception side is different, it is not the check target for D005-03. If there is register in the stage behind X and C, it is detected as the error in asynchronous transfer of D005-01.



4.3.2 Execution Method

<Example for execution command>

```
%   STAcheck -WORK work_directory ¥
        -TOP   alu ¥
        -PTSHELL check_condition.txt ¥   -----①
#       -INIT   ¥
#       -LANG VERILOG  ¥                 ---②
        -NWCELL NetWalker_ib   ¥         ---③
        -RENEW ¥
#       -RECONVERGENCE_MAXFF   number(default:20)        ¥
#       -D005_01_LIMIT_DC_EXEC   number(default:20)            ¥
#       -D005_01_EN_ASYNC_CIRCUIT_TYPE 1/2/3/4[default:1] ¥
#       -D005_01_AND_OR_SYNCRO      ¥
#       -D005_01_SYNC_CONE          ¥
#       -D005_03_CHECK_D005_01ERR ¥
#       -PRT_ASYNC      file_name   ¥
#       -ADD_TOP_MODULE             ¥
#       -NOT_PRT_D005_01_LOGIC_CONE   ¥
#       -TCL            tcl_file    ¥
#       -TCLD                       ¥
         alu.v
```

① Check status (like SDC) file check_condition.txt

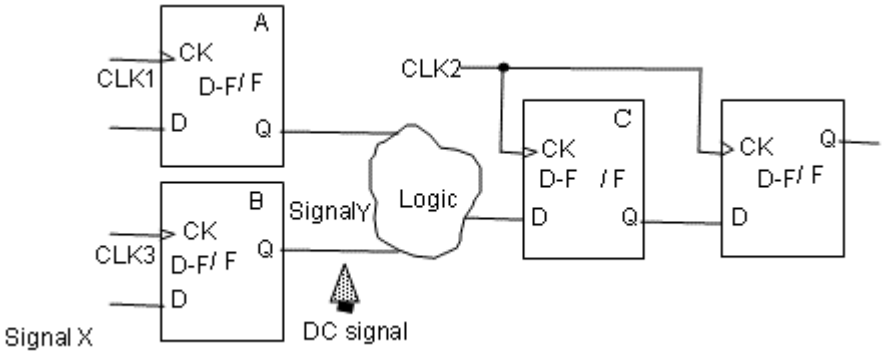
Clock signals and fixed value signal are specified by the format that looks like the PT shell of PrimeTime.
Five commands can be specified, namely; create_clock, create_generated_clock,
set_case_analysis, set_input_delay, set_faluse_path.
If the clocks are individually specified with create_clock, those clocks become asynchronous to each other.
If all the clocks are defined with create_clock by mistake, then correct result cannot be obtained by executing a check for asynchronous system. Hence the synchronous clock generated internally in frequency divider must be specified in create_generated_clock.
set_input_delay defines clock attribute of input signal and uses it in asynchronous transfer check of input signal.
The check can be omitted in set_false_path. However, if PT shell used in static timing verification is used, asynchronous transfer specifies set_false_path. If used in the same condition, the asynchronous transfer is not checked. Hence the STAcheck restrictions must be reviewed. This should be treated as an important instruction.

Example)

```
create_clock -period 8 -name VCLK -waveform { 2 6 } CK1
create_clock -period 8 -name UCLK -waveform { 2 6 } CK2
create_generated_clock -name MCLK -source CKW1 -edges{1   3   5} CK3
```

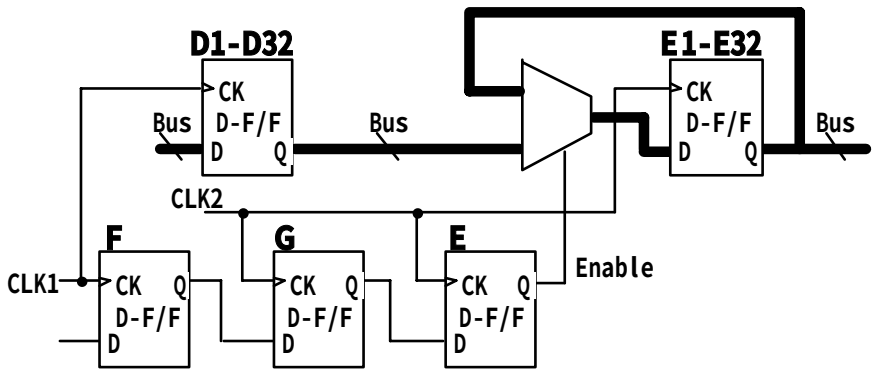
set_input_delay 4.4 -clock CLK1 { IN1 INX* }
set_case_analysis 1 S

<DC signal specification: function for omitting D005-01 (type4) error>
The DC signal is specified by net name or gate instance name + pin name.
In case of the under mention,
set_strings DC_SIGNAL B.Q ;
is specified but, X, Y, B.Q also have the same result and can be used in place of ”B.Q”.



<GROUP_REG specification: for D005-02 check>
The classification of single signal transfer and multiple signal transfer is specified in GROUP_REG by the register name and group name of transmission side.
(Transmission side register name can be specified in wildcard.)

In the figure shown below, transmission side registers D1 ~D32 is specified. ASYNC1 group checks that it is same synchronization circuit (G, E) of stage 2 Flip/Flop for enable signal of the selector connected to the register of D1 ~ D32.
(Description example)
set_strings GROUP_REG D* ASYNC1 ;

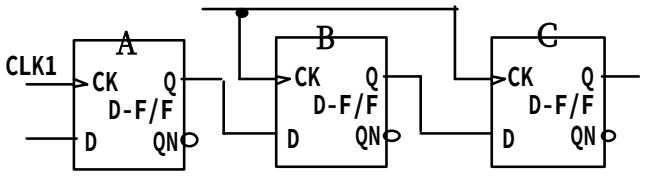


Even in the single signal, specification is necessary. The purpose is the sake of following checks.

- the signal is single signal transfer
- the specification has not been omitted(forgotten).

The tool considers the signal group which does not specify GROUP_REG belongs to the same group by default. In that case for example, when that signal is registered twice, error occurs in D005-02. And in case of convergence, then error occurs in D005-03. In the following case, register A at transmission side and group name specify NULL({}).

set_strings GROUP_REG A {};



In order to check that specification is not omitted (forgotten), both single signal transfer and multiple signal transfer need GROUP_REG specification.
Moreover, when the selector analyzes AND-OR, and enable cannot be identified, check is omitted.

② Language specification- LANG

<VERILOG/VERIRTL/VHDL>
The description language of netlist is specified. VERILOG is default language. If the execution is in VERILOG RTL, then –LANG VERIRTL should be specified. RTL description is synthesized temporarily inside, and it is checked.

VERILOG: Verilog gate description only
VERIRTL: Verilog gate, RTL that can be synthesized, integrated gate/RTL, integrated Verilog/VHDL
VHDL: VHDL gate, RTL that can be synthesized, integrated gate/RTL

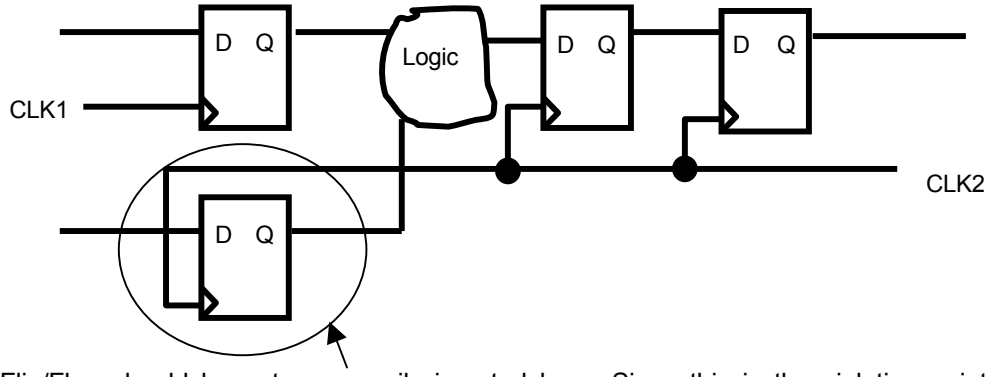
③ -NWCELL NetWalker library

NetWalker library is specified. In case of RTL description, the library specifications of general characteristics are not necessary. But it is required only when using hard module of RAM etc.

4.4 Circuits to be avoided

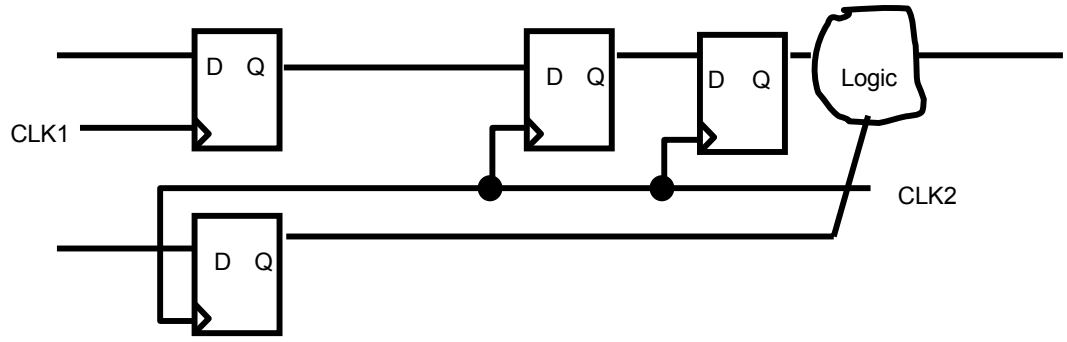
4.4.1 Circuits to be avoided Example1: From trial results in STAcheck

The signals of heterogeneous clock domains exist together in combinational circuit input of asynchronous signal transfer of single signal.



This Flip/Flop should be not necessarily inserted here. Since this is the violation point of timing, it must be corrected.
In this case, indicated in type4 of STAcheck D005-01.

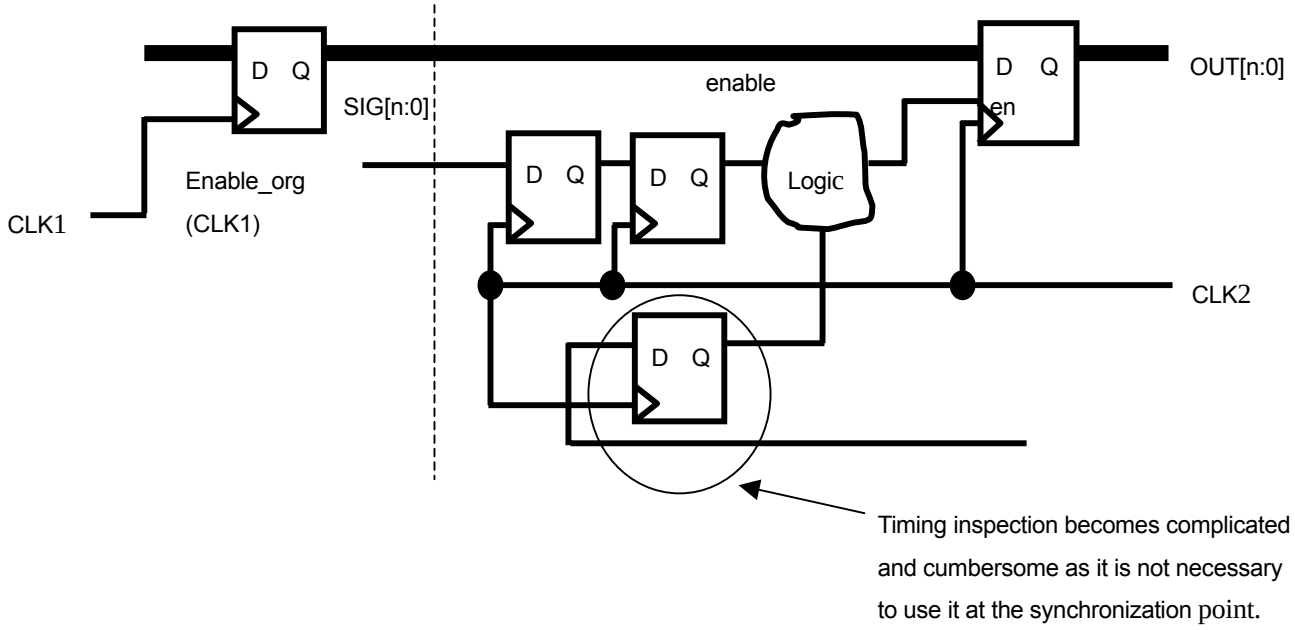
Measure1: Correction is done as shown in the figure below.



Measure2: In STAcheck, when net is not modified and this circuit is recognized as the synchronization circuit, please specify -D005_01_SYNC_CONE in execution command.
Refer 4.3.1 (1-2) Specification for excluding transformation circuit

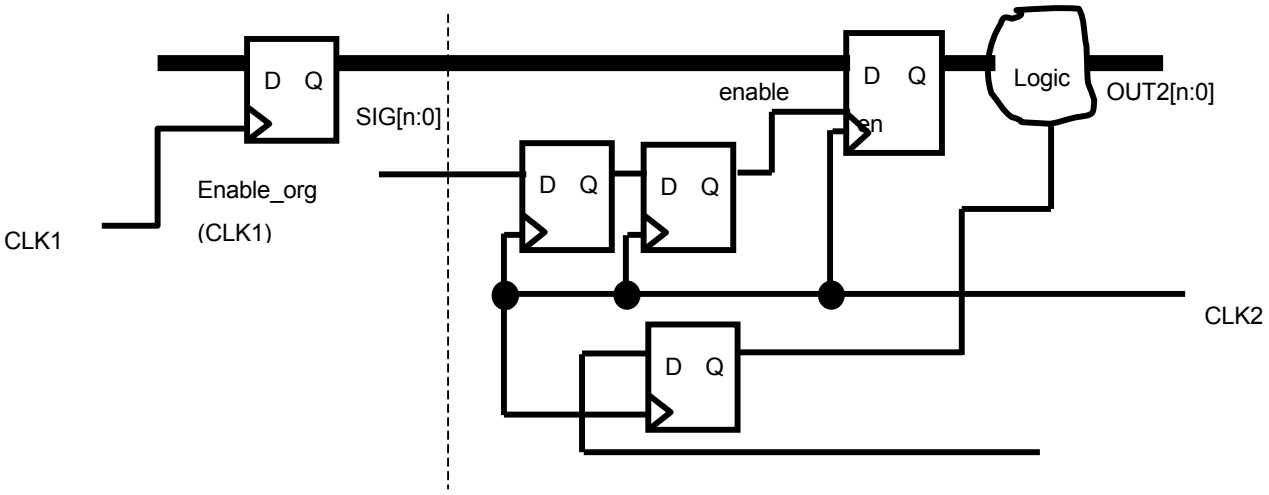
4.4.2 Circuit to be avoided Example 2 : From trial results in STAcheck

The combinational circuit of the homogeneous clock domain is used in enable of multiple signals transfer.
One side is case without signal transfer. In other words, at this point there is not the necessity to use. Since timing verification becomes complex, rectification is necessary.



Detected at STAcheck D005-01 type4

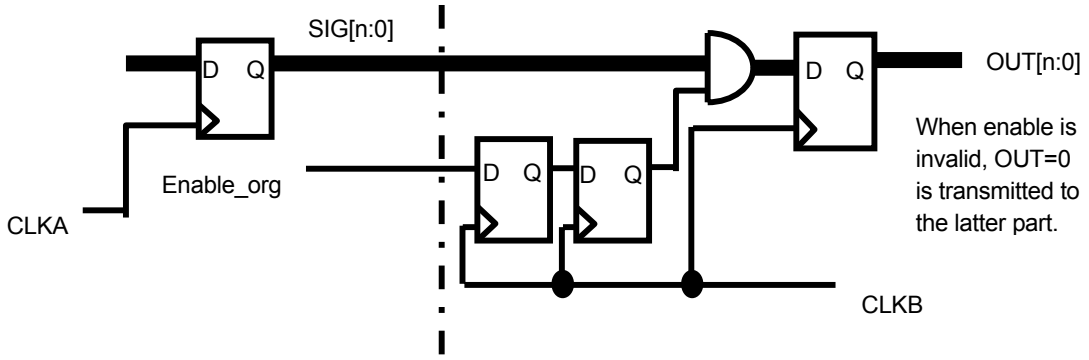
Measure1: -D005_01_EN_ASYNC_CIRCUIT_TYPE command specification
(Refer 4.3.1 (1-2) Specification for excluding transformation circuit)
Measure2: Used after the 1st stage. (See figure below)



4.4.3 Circuit to be avoided Example 3 : From trial results in STAcheck

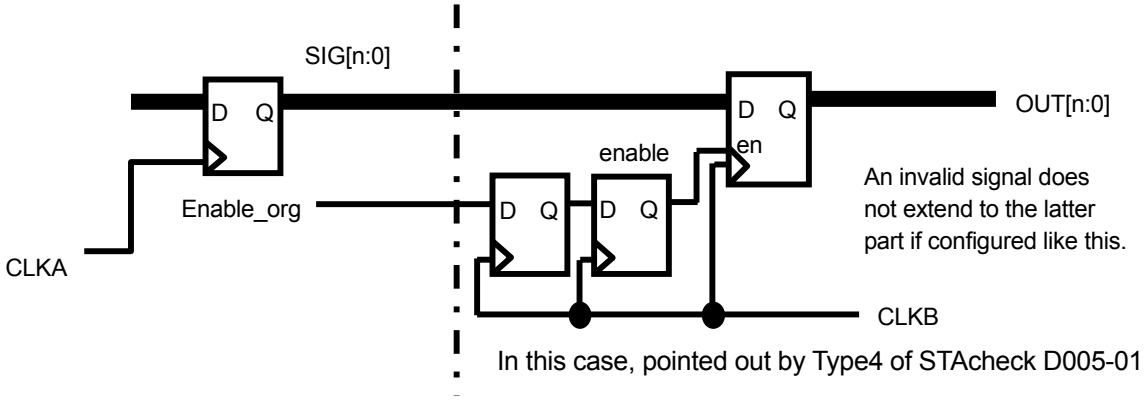
Absence of feedback signal in the enable logic.

→ Invalid signal is transmitted to the next stage, hence logic has become complex, and as a result verification is difficult.



Defective Circuit

Counter measure:

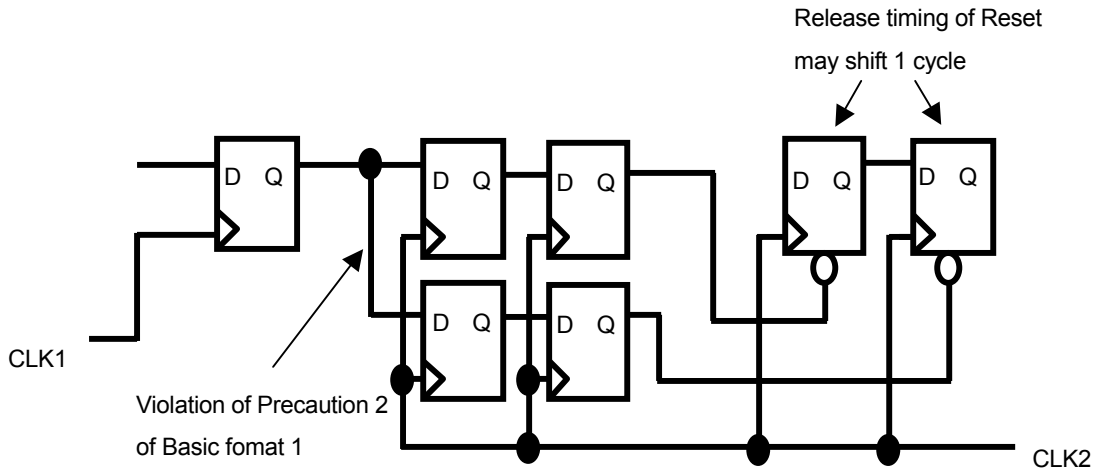


In this case, pointed out by Type4 of STAcheck D005-01

Modified Circuit

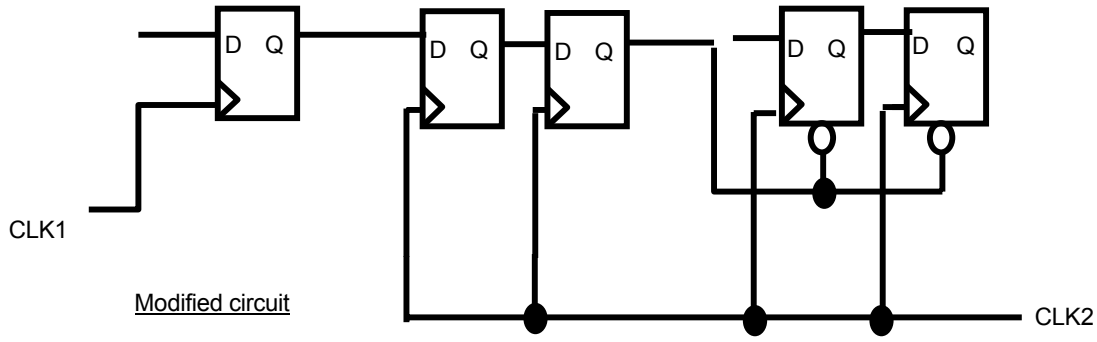
4.4.4 Circuit to be avoided Example 4 : From trial results in STAcheck

Violation of fan-out process of signal of synchronization part



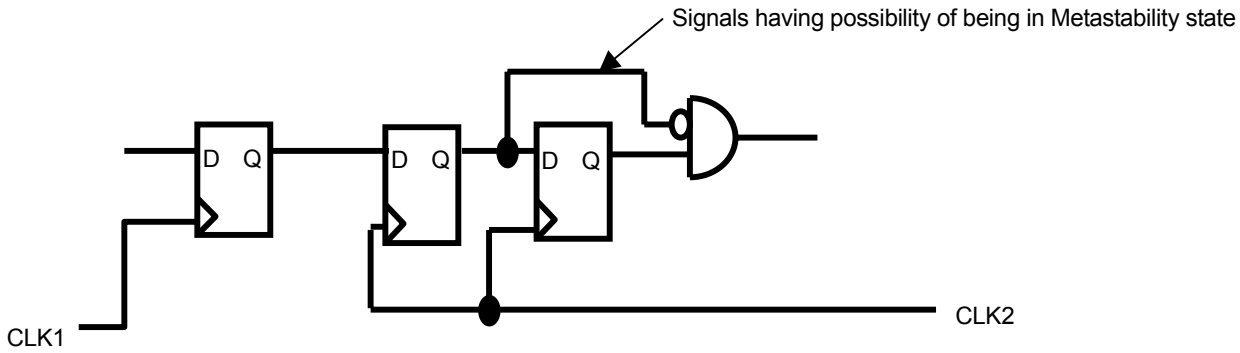
Detective circuit Detected at STAcheck D005-01 type2, D005-03

Counter Measures:



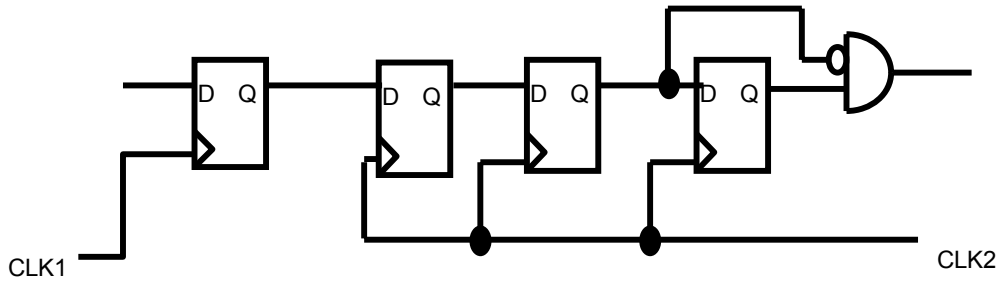
4.4.5 Circuit to be avoided Example 5 : From trial results in STAcheck

When synchronization process is incomplete



Defective circuit Detected at STA check D005-01 type3

Counter measures:



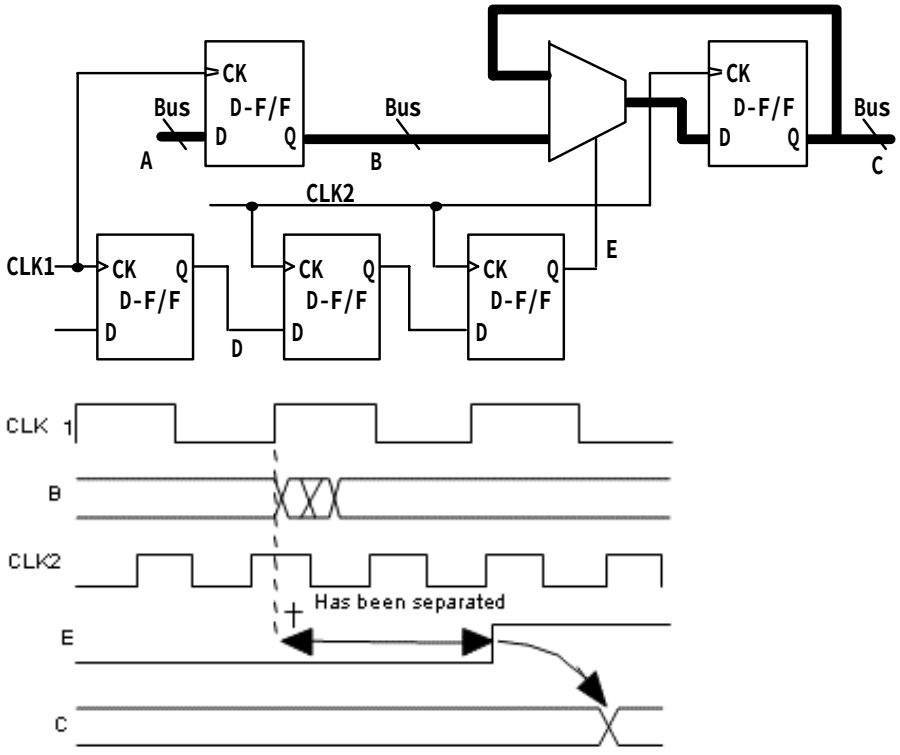
Modified circuit

4.5 RTL/Gate simulation

Design Input	All design results of asynchronous signal transfer configuration and RTL
Design Output	1. Compare asynchronous signal transfer timing with timing chart and confirm. Especially, confirm that multiple signal enable or handshake signal is sufficiently separated from transition timing of bus signal. This must be given special attention as timing check cannot be carried out in STAcheck. 2. In STAcheck verification, if there was the cycle slippage hazard location (D005-03) of convergence error, then simulation and timing chart should be verified. 3. In STAcheck verification, if there is hazard prone location, (D005-01 type4, D005-03) does not incorporate it even though hazard occurs. Else, confirms with simulation based on the documents which prove that there is no impact. (timing chart is necessary.).

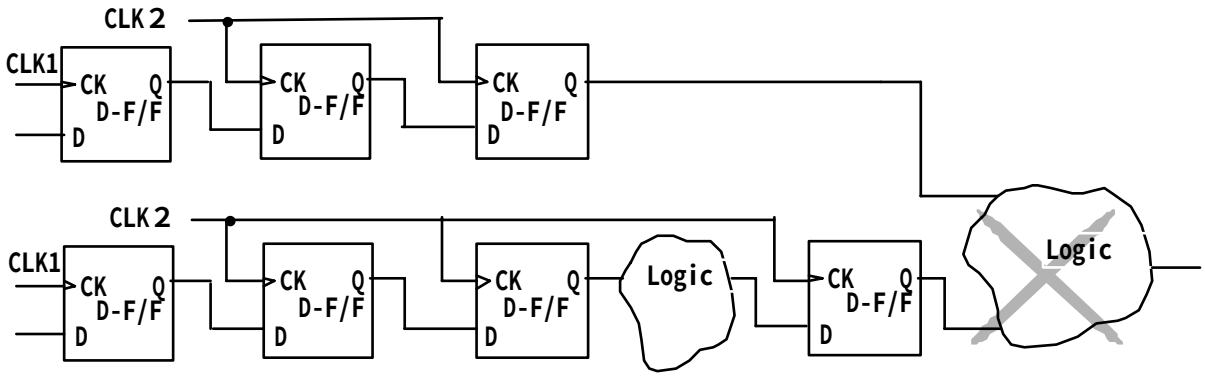
In most case, the proof of having convergence error or hazard requires considerable man-hour effort than circuit modification. Hence circuit modification in early design stages is recommended.

(1) Compare synchronous signal transfer timing with timing chart and confirm.
Especially, confirm that multiple signal enable or handshake signal is sufficiently separated from transition timing of bus signal. (Refer figure below)



(2) When there is risk prone location (D005-03) of cycle slippage of convergence error

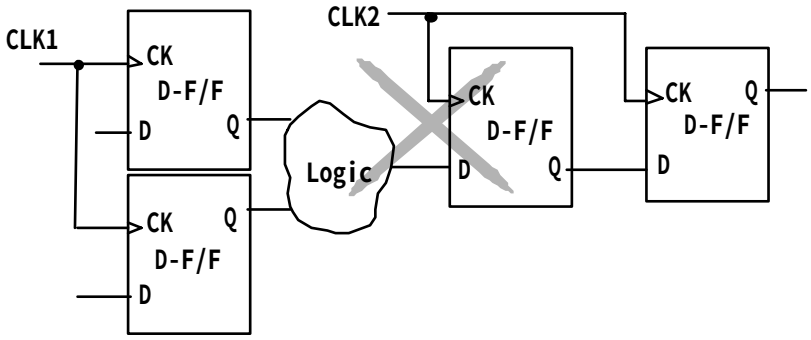
When there is risk prone location of cycle slippage or hazard, confirmation with timing chart is necessary.



Example of Circuit with Cycle Slippage

(3) When there is hazard prone location

Compare asynchronous signal transfer timing with timing chart and confirm. Especially, confirm that multiple signal enable or handshake signal is sufficiently separated from transition timing of bus signal.



Hazard prone location

5. SoC Chip Level Verification

Design Input	All design results of asynchronous signal transfer configuration.
Design Output	Confirms that there is not an unplanned asynchronous signal transfer between the IP modules. As a result, when Chapter 2-4 is not followed, logic correction or the analysis of the practice result of STAcheck which checked the inside of IP at LSI is necessary.

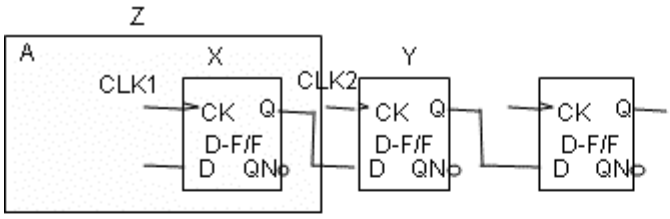
If all measures are taken appropriately in early design stages, the verification at SoC chip level is a process only to reconfirm those results.

The verification is necessary about connection with the other modules when asynchronous signal circuit is not hid in module. As a result, verification at SoC chip level is necessary.
However, if the stage number of convergence error verification in STAcheck increases, then the process in circuit size of SoC level may not end. As a result, the circuit might have to be divided into smaller circuits in order to achieve connection verification with the other module. Thus, there is an increase in the man-hours effort for verification when transmission scope of asynchronous circuit is wide.

The error without the problem in module verification or the error that is closed in a module can be excluded with **set_strings Cancel_D005_module module name;**
The target rule is D005-01/02/03.

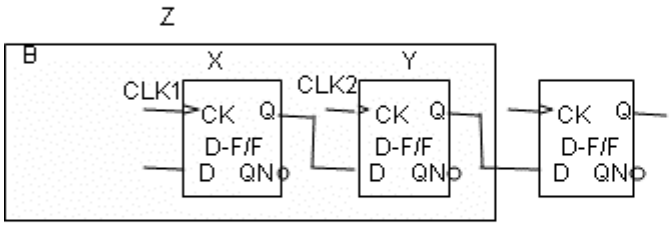
In case of D005-01

The error is excluded when specified module between asynchronous transfers is closed.
Note: If there is multiple routes from transmission side register to receive side register, then it is determined based on the route that is searched first.



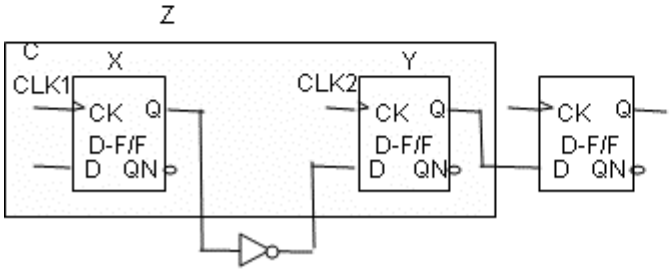
set_strings Cancel_D005_module A ;

outputs error



set_strings Cancel_D005_module B ;

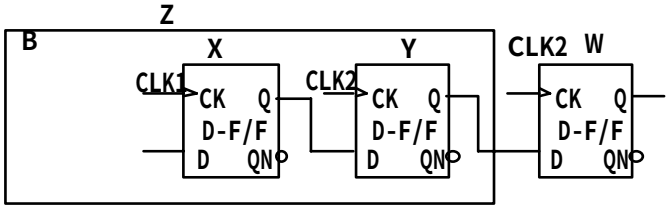
Does not output error



set_strings Cancel_D005_module C ;

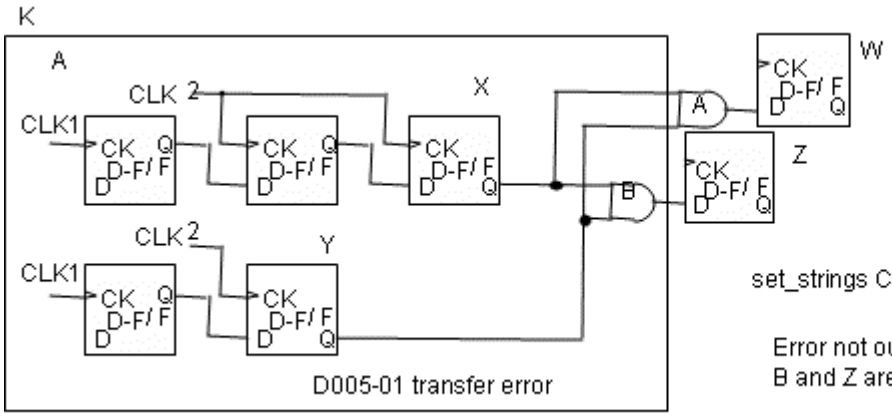
outputs error

In case of D005-02



set_strings Cancel_D005_module B ;

In case of D005-03



set_strings Cancel_D005_module A ;

Error not output for A and W
B and Z are excluded and hence, not output.

6. Layout, Timing Verification

Design Input	All design results of asynchronous signal transfer configuration
Design Output	1. Confirms asynchronous signal transfer timing. (When constraints in clock intervals are not implemented, a big detour is possible in layout and the timing chart is not complete) 2. Confirms the timing of cycle slippage/oscillation location, identified with STAcheck.

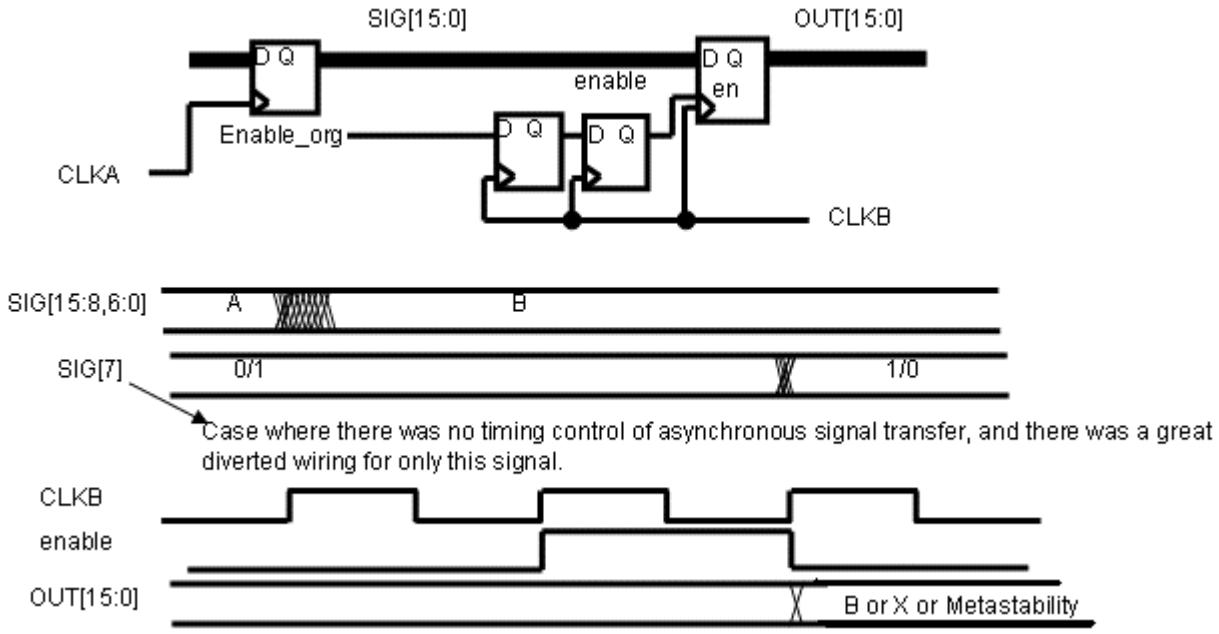
(1) Confirm asynchronous signal transfer timing.

In the layout, timing verification, confirm whether the restriction is such that CLK1→CLK2 transfer of the signal for which Group is specified becomes homogeneous at timing in synchronization circuit of multiple signals. Hypothetically, the synchronous circuit does not operate correctly when signal group for which Group is specified has Skew longer than one cycle of CLK2 and is transmitted. When a false path is set by set_false_path from CLK1 to CLK2, the skew may increase according to the layout tool. (Refer the diagram below). In order to avoid this, for example

(1-1) The timing restriction is provided in path of synchronization in the layout.

(1-2) During testing if the CLK2 clock is switched with another clock that is CLK1 and synchronous clock, the layout is done with the timing restrictions of test mode (in other words timing is controlled as synchronous path.)

As a specific example, refer “Example for Confirmation of Transfer Delay between STA and asynchronous path 070904.ppt”



(2) Confirm the timing of point where cycle slippage is specified in STA check.
This is a confirmation of layout for a case where circuit modification is difficult correction etc, even though the cycle slippage/oscillation is due to convergence error.

For example, regarding the timing analysis result of convergence error of signal A & B, if the change of A, takes place earlier than that of B and is established that the error does not occur in the later stage, then the wiring delay of A & B in the layout is controlled.

Although it becomes a repeated repetition, since it is proved that bug is not generated by such measures., but the verification man-hour is large, it is necessary to avoid it as much as possible. This, however, also decreases the recycling IP greatly.

7. Reference Material

Refer the following document for asynchronous circuit illustrations.

About Asynchronous Signal Transfer Design
STAcheck User Guide
STAcheck V4.0 Design Rules
Example for Confirmation of Transfer Delay between STA and Asynchronous Path 070904

8. Appendix

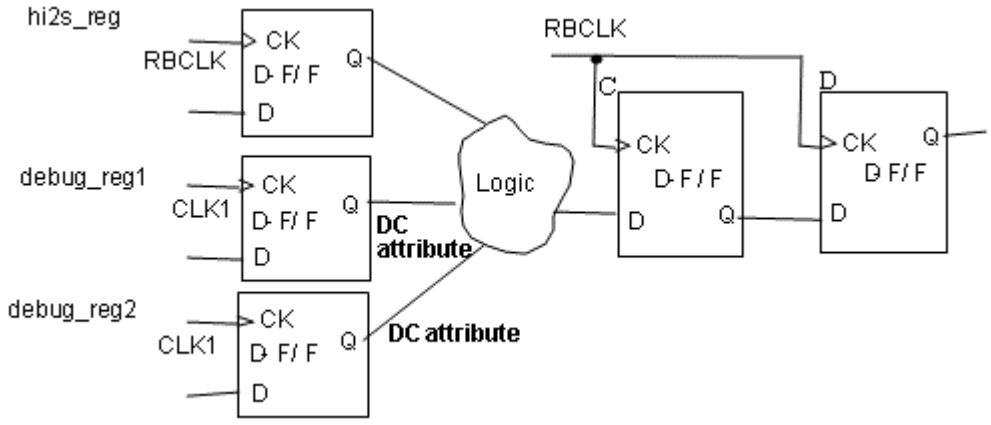
8.1 SpyGlass

Asynchronous transfer check in RTL stage can be checked with SpyGlass.
SpyGlass can simultaneously check the problems posed by RTL description in synthesis etc and asynchronous signal transfer. There are functions that cannot be checked in SpyGlass, hence it should be used for simple checks.

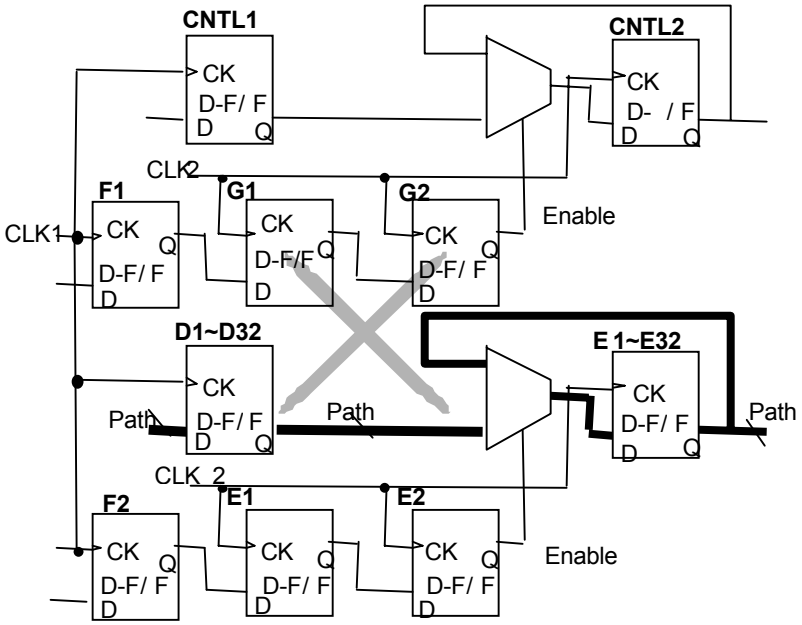
(1) Merits of using SpyGlass (effective in initial stages of RTL description)
- GUI function is enhanced, debug is easy
- RTL description is checked using simple check.

(2) Present in STAcheck, main function in SpyGlass
(2-1) Exclusion function by DC signal candidate output & DC signal specification
Function to exclude and to check impact by DC signal by specifying DC signal.

<DC signal definition>
In transmission side register,
when there no change of signal after reset is released and
the value immediately after change in transmission side register is not used in receive side then it is assumed as DC signal.



(2-2) Synchronization check of multiple signal transfer
In the CNTL1 and D1-D32 register (see figure below), if the transfer should carried out at identical time, the cycle slippage occurs if the synchronization circuit of G1/G2 enable signals and synchronization circuit of E1/E2 reside separately. This case is not checked in SpyGlass.
Cycle slippage occurs when the circuit of making to synchronization of G1/G2 enable signal and the circuit of making to synchronization of E1/E2 exist separately. If bus signal (signal specified in "[]") is not in synchronization signal (synchronous transfer signal of multiple signals) of enable type, is assumed as error by SpyGlass.



8.1.1 SpyGlass execution method

Confirm [No black box] [The clock attainment rate to Flip/Flop and latch must be 100%.] and check asynchronous transfer. When Flip/Flop and latch do not reach the Black Box and clock, correct result cannot be obtained.
Black box confirmation method (Macros such as ROM, RAM are excluded.)
SpyGlass easily synthesizes and checks RTL. If combined errors exist, the combinations that are out of scope are, handled and processed by black box. Black box detects the pseudo error in connection attribute check of block input, since all the terminal attributes are handled as bidirectional (INOUT). Also, since black box becomes out of scope of signal transmission process, correct result cannot be obtained. The presence of black box is detected by "DetectBlackBoxes", "ReportUnsynthesizedDU". The detailed error content is detected in "STX_", "SYNTH_", hence, modify the description of the corresponding location, and confirm that there is no black box.

② Confirming the clock attainment rate to Flip/Flop and latch to be 100%.
If the clock attainment to Flip/Flop and latch of logical circuit is not 100%, the logic part and its peripheral logic cannot be checked. If the clock in Flip/Flop and latch is not attained, "Clock_info03a" is detected; confirmation for no specification leakage of clock signal and description modification is carried out. Thereafter, it is confirmed that clock attainment rate to Flip/Flop and latch is 100%.

<Example for normal mode execution command>

```
% spyglass ¥
–verilog ¥
–top alu ¥
–policies=renesas ¥
–sgdc clock_reset.txt ¥          ___①
```

–allow_half_sync=no ¥ ___②
–v ram.v ¥ ___③
–stopfile ram.v ¥
–sgdc ram.txt ¥
alu.v

Clock/reset/normal mode signal, and input port clock specification information format is as shown in the structure below. This control file is specified.

–sgdc <clock, reset control file>

Example) current_design alu
clock –name clk1 –domain clkA
reset –async –name rst1
set_case_analysis –name nomal_mode –value 0
input –name in1 –domain clk1

Clock reversing prohibition specification for Flip/Flop 2 stage synchronization circuit

Clock reversing prohibition for Flip/Flop 2 stage synchronization circuit is specified.

–allow_half_sync=no

Example) The following case is detected as NG.

③ -ramv, –stopfile ram.v, –sgdc ram.txt specification

Specifications for checking the correctness of transfer to RAM etc and transfer from RAM etc.

Verilog description is specified in -v ram.v and the description in –stopfile is excluded from check. However, dual port RAM that inputs two or more clocks cannot be recognized.

In the cell in which 2 or more clocks are inserted, the terminal depends on the clock specified by reset control file.

–sgdc ram.txt (clock, reset control file) description method

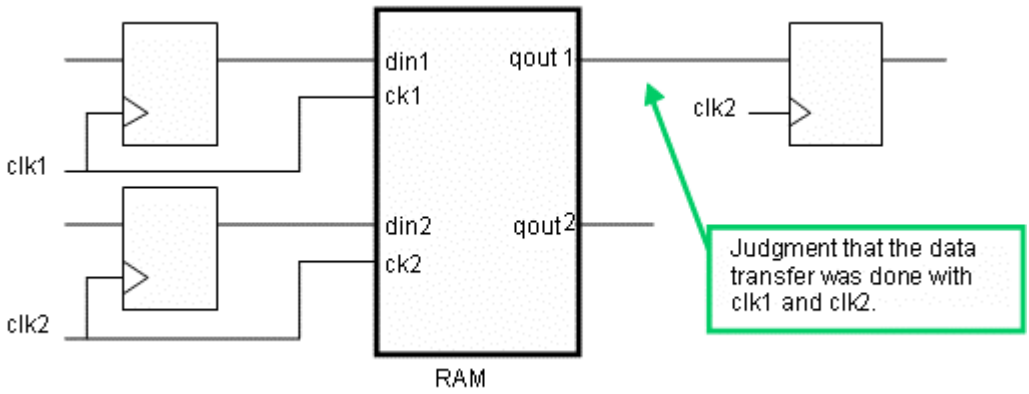
Set using signal_in_domain information.

current_design <du-name>
signal_in_domain
–name <bbdu-name>
–signal <sig-name-list>
–domain <input-pin-name>

<du-name>: top module name
<bbdu-name>: black box module name
<sig-name-list>:synchronization dependant terminal name list
<input-pin-name>: clock input terminal name

Example)

signal_in_domain –name RAM –signal din1 qout1 –domain ck1
signal_in_domain –name RAM –signal din2 qout2 –domain ck2



For details refer SpyGlass User Guide.

8.2 Metastability

8.2.1 Who should be reading this chapter?

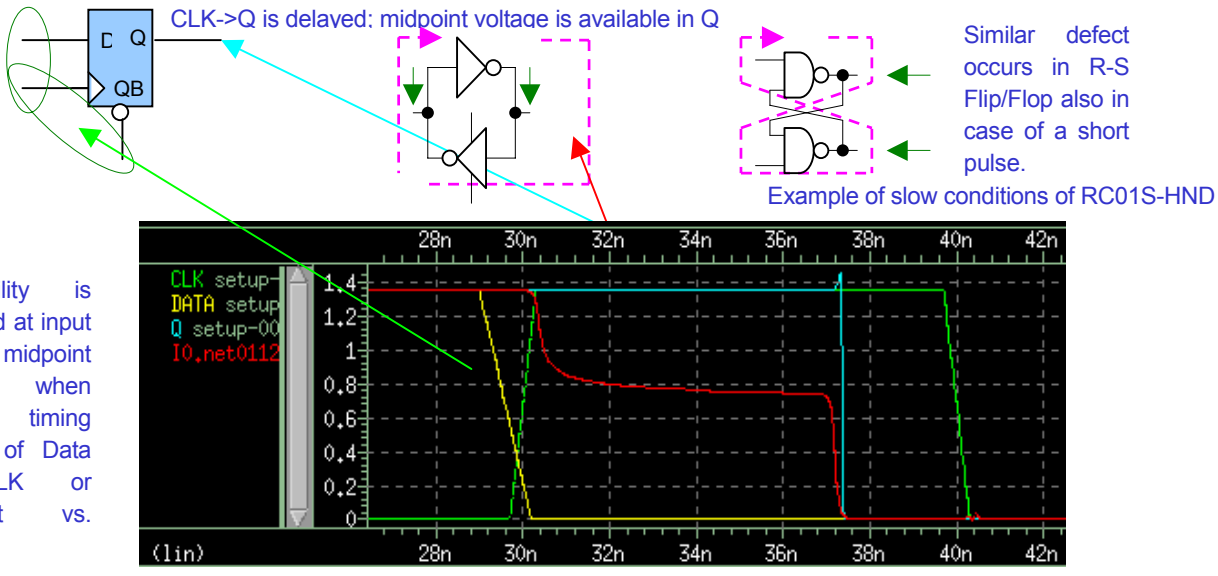
(1) Person using high speed asynchronous signal transfer (It is usually 100MHz in low-speed process of 500MHz RC01S) circuit and circuit for execution delay sampling of above-mentioned equivalence.
(2) Person requiring very high reliability (Lengthy MTBF)
(3) Person requiring evidence of error ratio of asynchronous signal transfer.

Verification of stabilizing (convergence/termination) time of Metastability is necessary in case of high frequencies. As per the standards, the gate delays should be compared for obtaining confirmation. Normally, the asynchronous transfer is at 500MHz and above (below 2ns), and in case of low-speed processes such as RC01S, the transfer is at 100MHz and above (below 10ns). Metastability being a probability event, there is no timing threshold for its generation. Therefore, when very high reliability (lengthy MTBF) is requested, verification is done for lower frequencies, and the records etc are saved for reference. Especially in the recent development of fine processes, the loop gain is getting smaller due to reduction in dimensions. This is achieved by reducing the inverter drive power of Flip/Flop feedback. This in turn leads to increase in the convergence time, thus due attention is required

8.2.2 What is metastability

Whenever there is setup and hold time violations in any flip/flop, and the data hold latch and storage node in Flip/Flop do not reach the VDD/VSS level it enters a state where its output is unpredictable: this state is known as Metastable state. At the end of Metastable state the flip/flop settles down to either `0` or `1`. This whole process is known as Metastability. When the input change in the timing that does not meet the setup time (tS) and the hold time(tH) and midpoint voltage inserted in the input Metastability occurs. (In the circuit with asynchronous terminal like set/reset, the timing violation in asynchronous terminal and clock occurs.)
(In asynchronous terminal like set/reset, timing violation of asynchronous terminal and clock occurs.)
Input timing violation (or midpoint voltage input)

→ Internal node stays in midpoint voltage for long time
→ CLK->Q is delayed, midpoint voltage is available

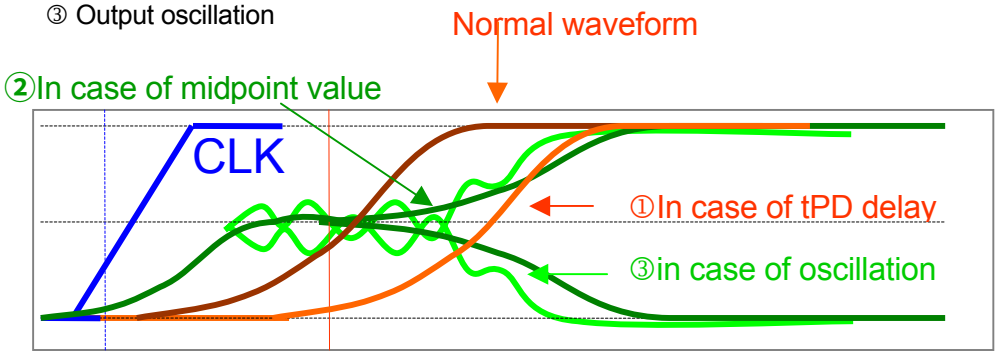


When internal node becomes the midpoint voltage, one (in multiples) of the following 3 phenomenon does occur.

① CLK->Q is delayed more than the standard value.

② Midpoint voltage is available in Q

③ Output oscillation

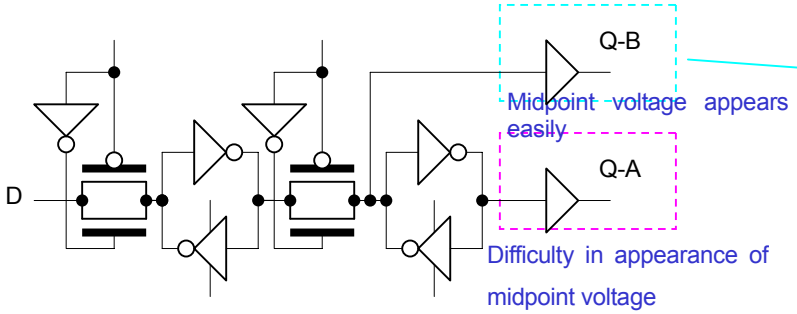


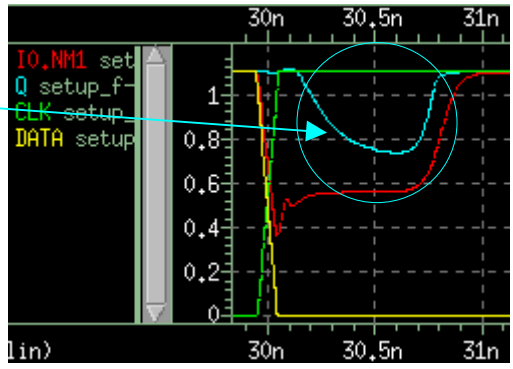
In this, the delay more than the standard value of CLK -> Q refers to the increase in the number of stages from storage node to Q, when

- The Vth of MOS has high threshold, as in low stand by library, in (Q-A).
- The appearance of midpoint voltage in ②Q in (Q-B) refers to the decrease in number of steps as output taken from storage node. Besides, the Vth of MOS is low as in the high-speed library.

Though, the oscillation in ③ output is very rare in the current model, a. increase in noise in the vicinity of the gate that has high gain at midpoint voltage is observed. Also, when the feedback loop is long, same as the RS type phase comparator having delay gate in the loop, there may be oscillation of narrow sense as per the phase shift.

Though, the oscillation in ③ output is very rare in the current model, a. increase in noise in the vicinity of the gate that has high gain at midpoint voltage is observed. Also, when the feedback loop is long, similar to the RS type phase comparator with delay gate in the loop, there may be oscillation of narrow sense as per the phase shift is observed.

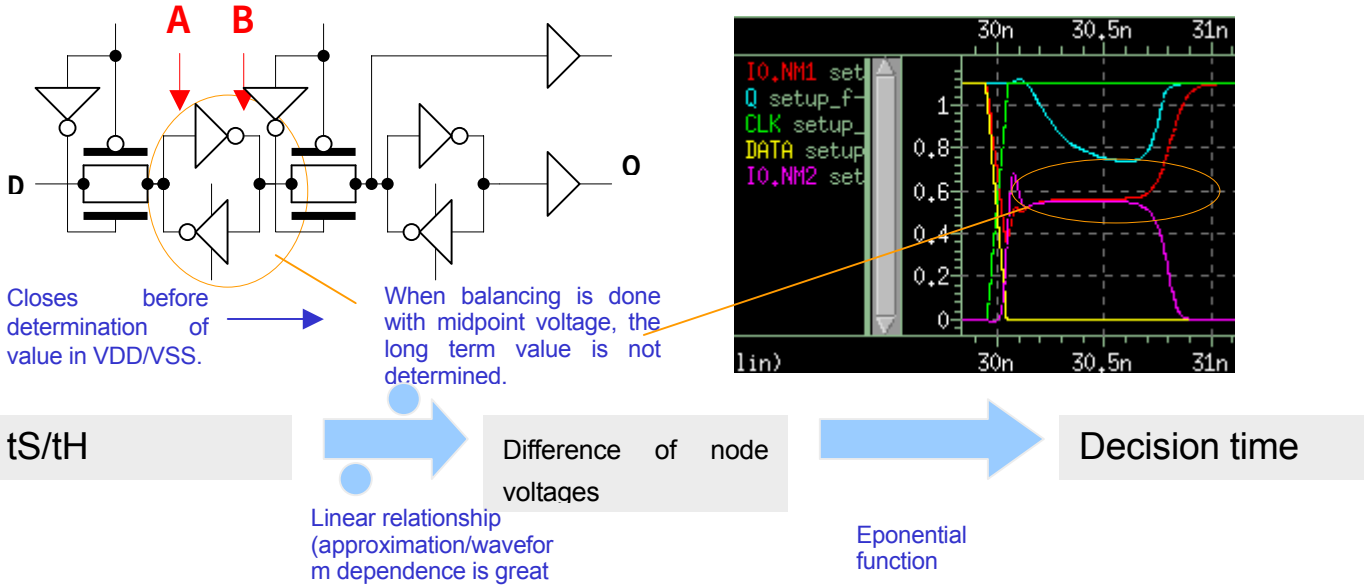




Example of midpoint voltage appearing in slow conditions of RC04

8.2.3 Metastability Mechanism

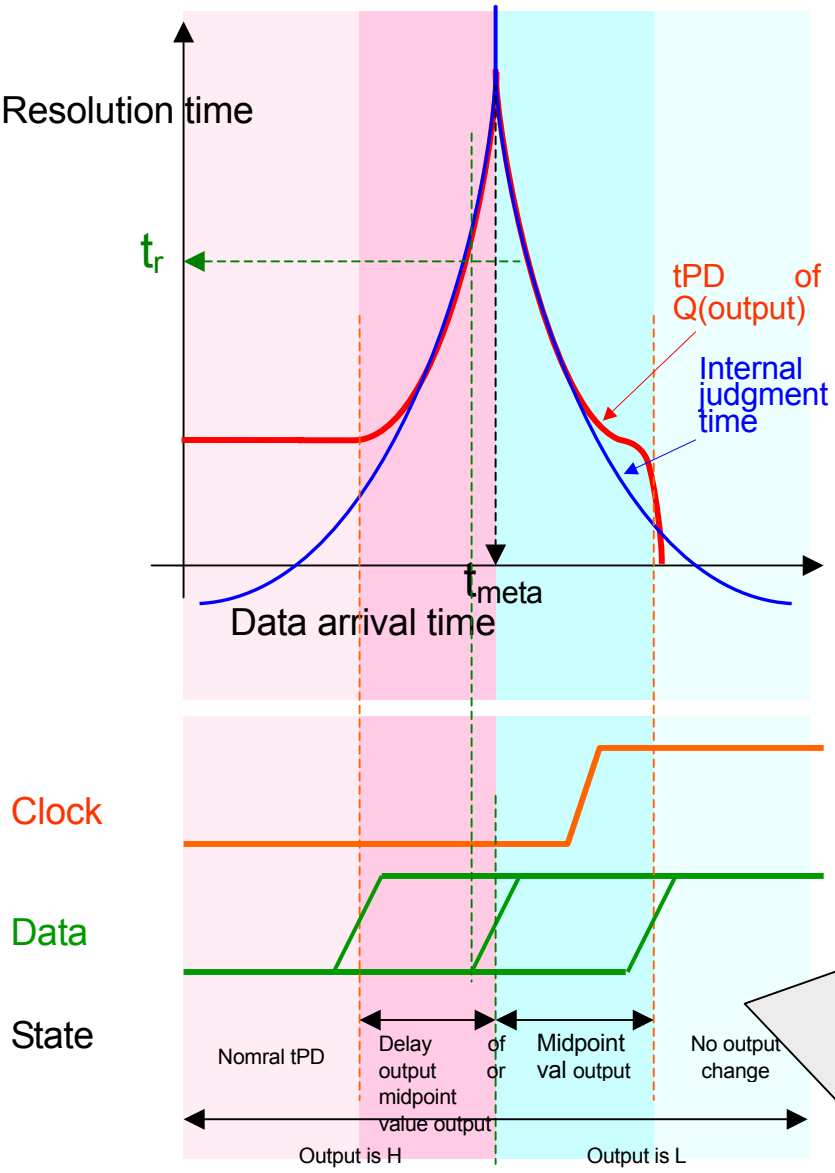
Metastability refers to the phenomenon wherein there is input change in setup time (tS) and hold time (tH) violations and if midpoint voltage is inserted, the data hold node does not change to VDD/VSS status. This occurs in order to balance the midpoint voltages by cutting off the input drive entering into data hold state.



Definition of T0 and τ by **Sca** C. L. Portmann and T. H. Y. Meng, "**Metastability in CMOS Library Elements in Reduced Supply and technology led Applications**", IEEE J. Solid-State Circuits, vol. 30, no. 1, pp. 39- 46, Jan. 1995.

There is an exponential function in the time duration (decision time) between the storage node of previously mentioned Flip/Flop, voltage difference in both ends node (A, B) and the value determination. Therefore in case of exact balance of voltage, the decision time becomes a theoretical infinity. (It actually converges in limited time due to noise etc.)

Also in many cases, it is assumed that the tS/tH duration is between the difference of voltages and linear function; hence tS/tH duration and decision time consists of the approximation for exponential function completion. For reproducing the Metastability state by adjusting tS/tH duration. This is difficult as it requires quadrillion more of accuracy, and there are no automated tools available. Even though automated tools/methods are available, care should be taken to ensure that waveform obtained by simulation are not (may become lengthy theoretically due to exponential response) of worst-case value. (Described later)

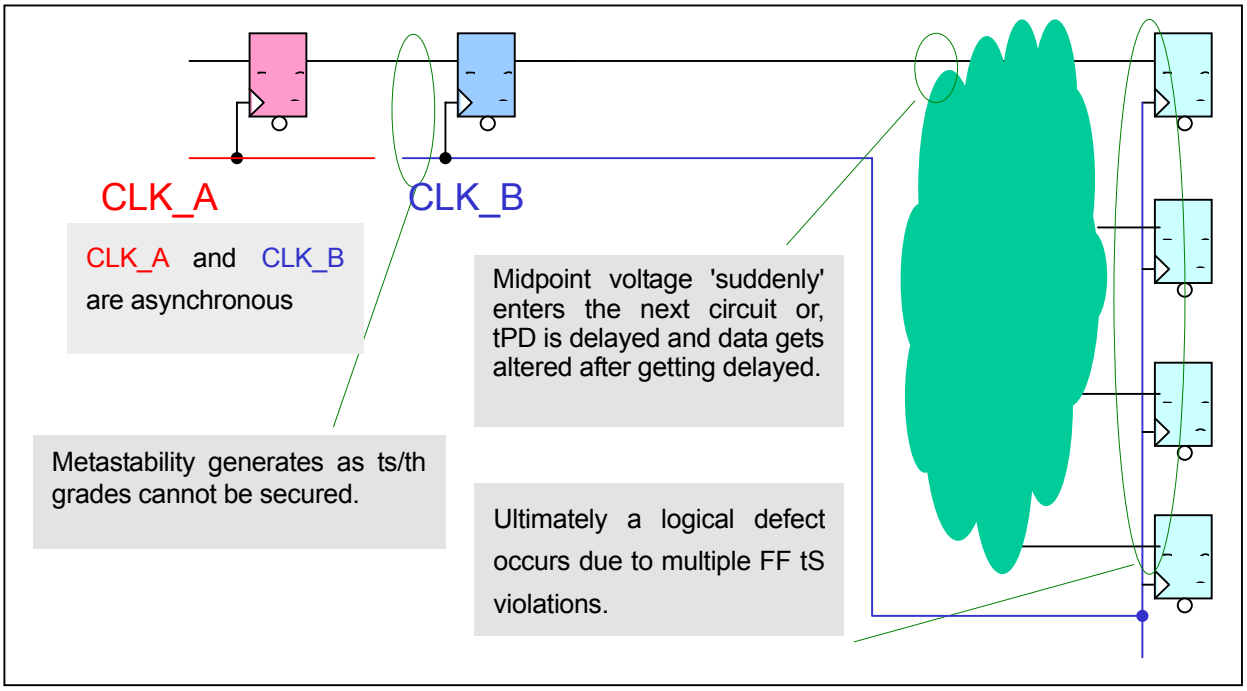


As for midpoint voltage, decision time is the basic criteria, hence should not be avoided. Even if mid point voltage that emerges with the gate that has shifted from logic Vt can be prevented with Schmitt Trigger, the transition time delay cannot be avoided. Moreover, the balance prevention circuit of various feedback loops often result in generating (balance is shifted) another balance point.

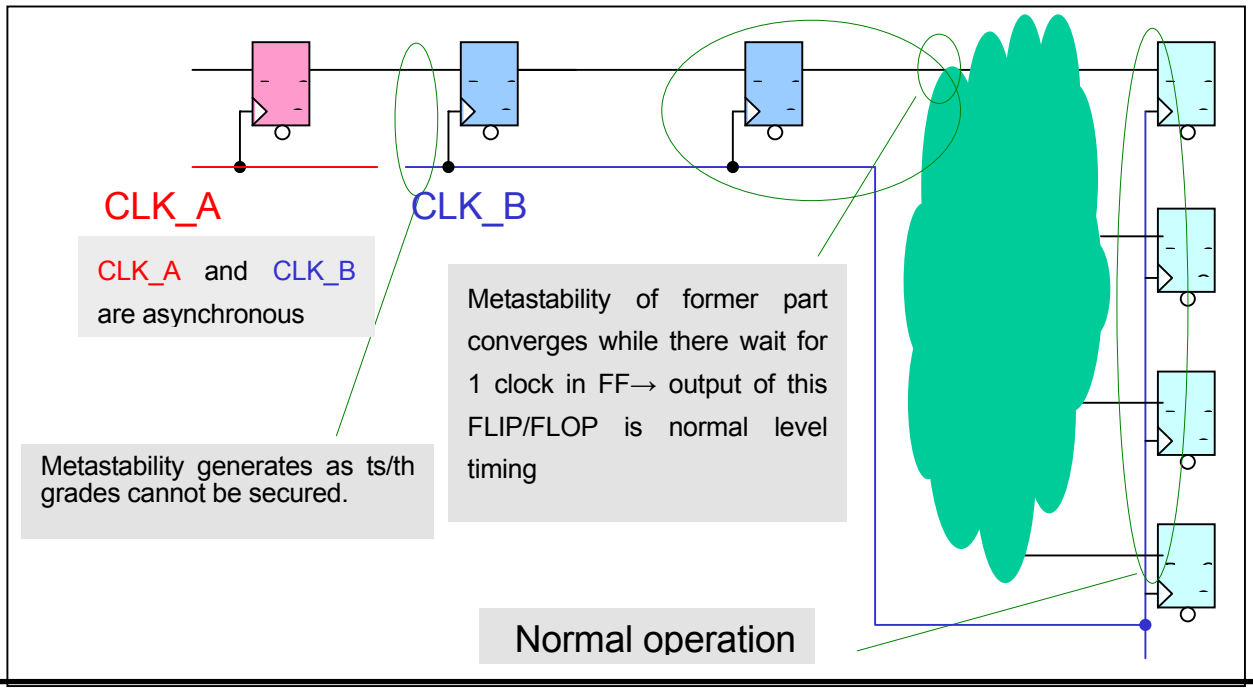
L is explained in the example where H is input in the hold FF.
The output becomes H if ↑ transition of Data is before Tmeta.
The output is L if ↑ transition of Data is after Tmeta.
The output temporarily becomes midpoint voltage or tPD is delayed in the period before and after Tmeta.
For the decision time that is the starting point of MTBF calculation, point 0(T0 both ends) cannot be externally observed for output buffered FLIP/FLOP.
(Attention: The Metastability window used in MTBF calculation is not the 'window where Metastability is actually observed'.)

8.2.4 Faults Originating in Metatability

The faults originating in Metastability ultimately appear as 1:N transfer inconsistency. When Metastability is developed in the present Flip/Flop, either the output is delayed or midpoint voltage is output. Therefore, there is a danger that the Flip/Flop connected to this output also develops Metastability in the same way due to tS/tH violation. Moreover, if there are multiple Flip/Flop connected to the output, there may be a difference in the logic values between them. Therefore, as a countermeasure for Metastability, wait for sufficient time (described later) before conversion to 1:N. When signals with multiple routes are combined, since the common timing is indefinite (there may be a gap of 1~several clocks) either the gap must be allowed or a synchronized design must be created.



Countermeasure is to wait for 1 clock (especially for 1 bit transfer)



8.2.5 Countermeasures for Metastability Faults and MTBF Calculation

There is no other valid countermeasure for Metastability faults but to wait till the termination of Metastability. However, since the decision time is an exponential response, the worst value is infinity, and cannot be decided uniquely. The waiting time necessary as countermeasure for Metastability faults is requested by reverse operation from the MTBF required in use conditions.

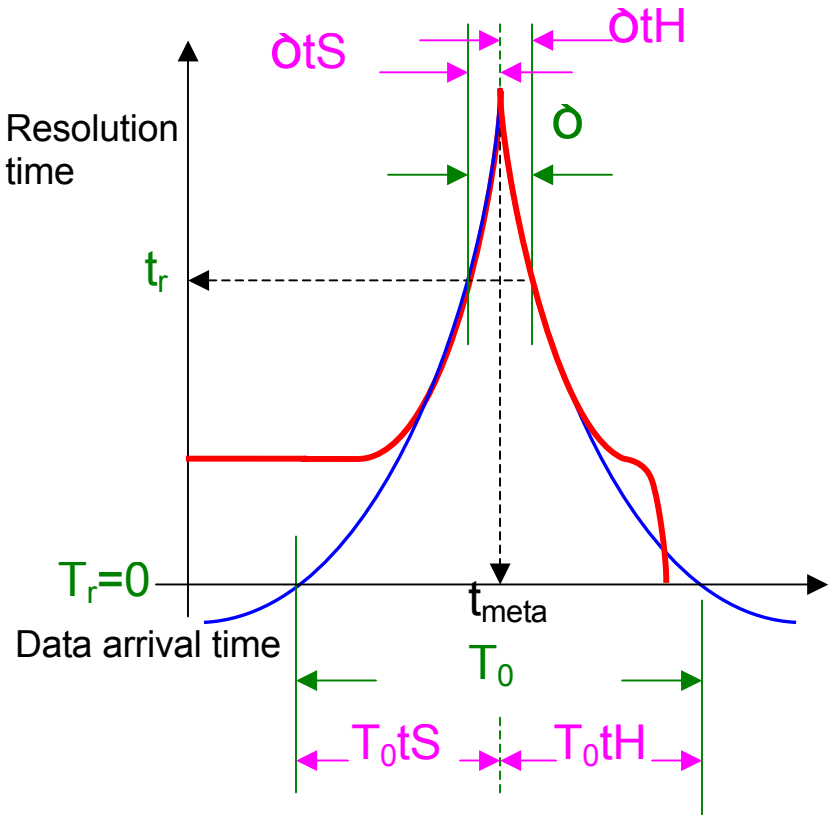
Worst value of Metastability end time (decision time) is infinity

→ **probabilistically requested from necessary MTBF**

The order of algorithm is; ① the Metastability attributes of applied devices are requested by simulation or measurement. ② The MTBF curve is requested from these attributes and use conditions. ① has to be essentially provided as a library parameter. However, currently since the maintenance has not been done, it should be prepared with the design as per the needs. As for②, the design has to be evaluated (part of the design) in any case.

For MTBF required in this procedure, it is assumed that the phases of 2 clocks are totally random. 'When there is a specific phase connection' in the delay etc of PLL/DLL/clock tree, the data transition always takes place next to the worst point (tmeta given below), and the fault ratio becomes much worse than MTBF obtained by calculation where random phase is required. In that case, with measures such as reversing the clock, the data transition is considered to be outside the T0 window.

Calculation of Metastability attribute of a single cell



t_r :Given convergence time

δ :Metastability window of that time

T_0: Asymptotically obtained window t=0

$$\delta = T_0 e^{-tr/\tau}$$

$$MTBF = 1 / f_B f_A T_0 e^{-tr/\tau}$$

The probability of Metastability of any convergence time can be calculated by T_0 and τ.

In case of $f_A > f_B$, since f_B edge is uniformly distributed in $1/f_A$ cycle, it enters the Metastability area in probability of $T_0 f_A$..

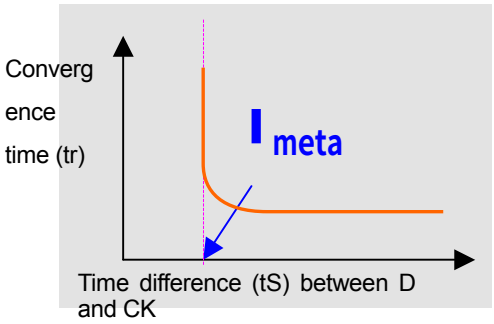
Since f_B edge within this area is uniformly distributed, due to exponential distribution of convergence time, the probability of convergence time exceeding tr is $T_0 f_A e^{-tr/\tau}$.

Therefore, the probability of the malfunction becomes $f_B T_0 f_A e^{-tr/\tau}$ by multiplying frequency f_B of the event by this probability.

In both, the figure and formula, δ and T_0 are bilateral values, but in reality since the values of tS side and tH side are different, they are considered in halves.

Summary of Dally/Poulton/Kuroda Tadahiro supervisor of translation "Digital System Engineering (application version)" (Maruzen) p.582-583

8.2.6 Concrete Procedure

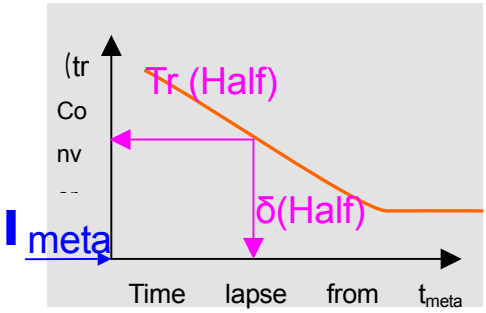


①Tmeta is obtained as accurately as possible.

Note that the simulation of point 2 is not linear if Tmeta is not obtained accurately and leads to generation of error.
Auto search is necessary → SpectoreMDL (example given below) etc is used

```
search V3:delay from binary(start=-5n, stop=5n, tol=1a) {
   run setup
} until ( setup -> DataQ < vol_VDD/2)
```

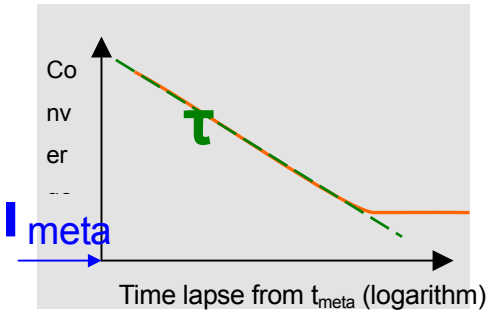
Note: Since an exponential distribution (= probability of Metastability is Poisson distribution) is considered for the decision time, the tPD delay value obtained by Sim is not a 'worst-case value'. Extrapolation is always to be done as per the following procedure



②The relation between tS/tH (difference from Tmeta) and Tr is requested.

If the convergence time is requested while logarithmically changing the offset from Tmeta, the convergence time becomes linear in the single logarithmic plot.
Auto Loop is useful → SpectoreMDL (example given below) etc is used

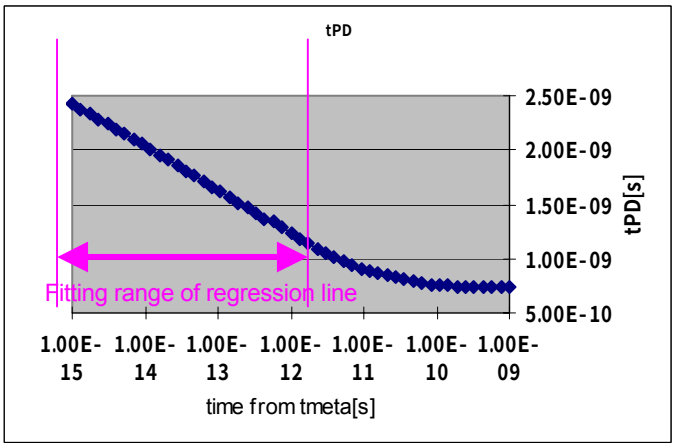
```
foreach delta from swp(start=1f, stop=1n, log=50) {
        V3:delay=tmeta-delta
        run td1
```



③Fitting, τ and T_0 are requested
tr=ln (time from t_{meta}) slant is τ
tr='time from t_{meta} ' resolved at 0 is T_0

The Sim results are obtained in Excel and "Analytical tool" is used.

Example of graph validation



$\delta = T_0 e^{-tr/\tau}$

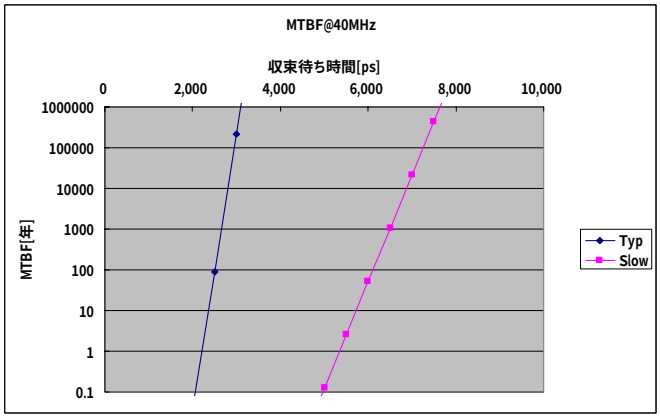
T0 obtained here is a one-side value.

Example of regression analysis of regression tools

	Coefficient		
Segment	1240.578818		
X value 1	-171.3864		Tau
y =	-171.386	* ln(x) +	1240.578818
7.238507335	= ln(x)		
x =	1392.0146		T0

MTBF is requested

Note: The following values are used for reference only and not for designing

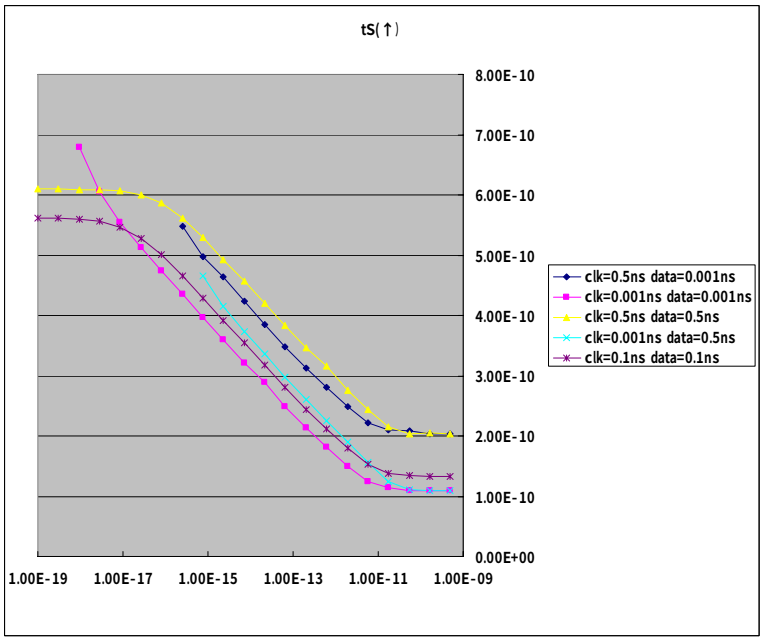


MTBF＝1／fBfAT0e-tr/τ

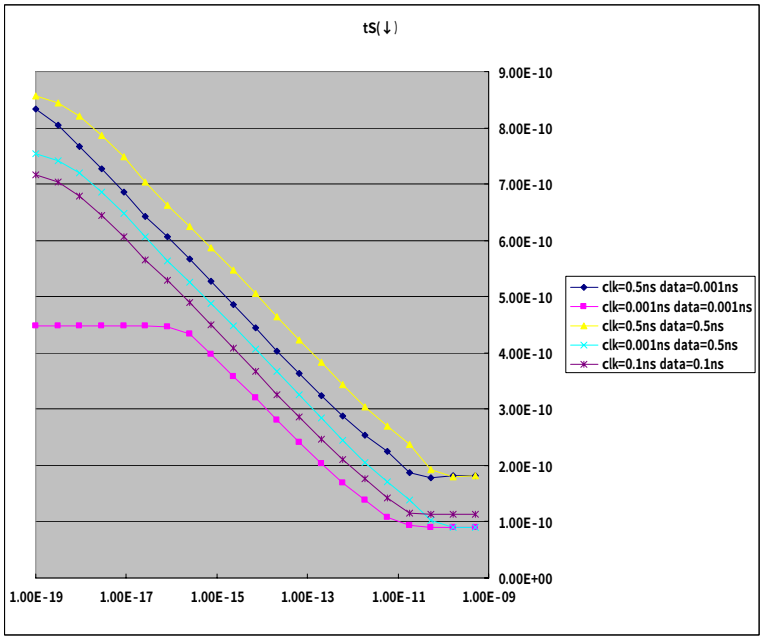
8.2.7 Example of Waveform Dependence (RC04) - Delay Amount

Note: Since the measurement is automatic, the midpoint voltages may not be measured correctly.

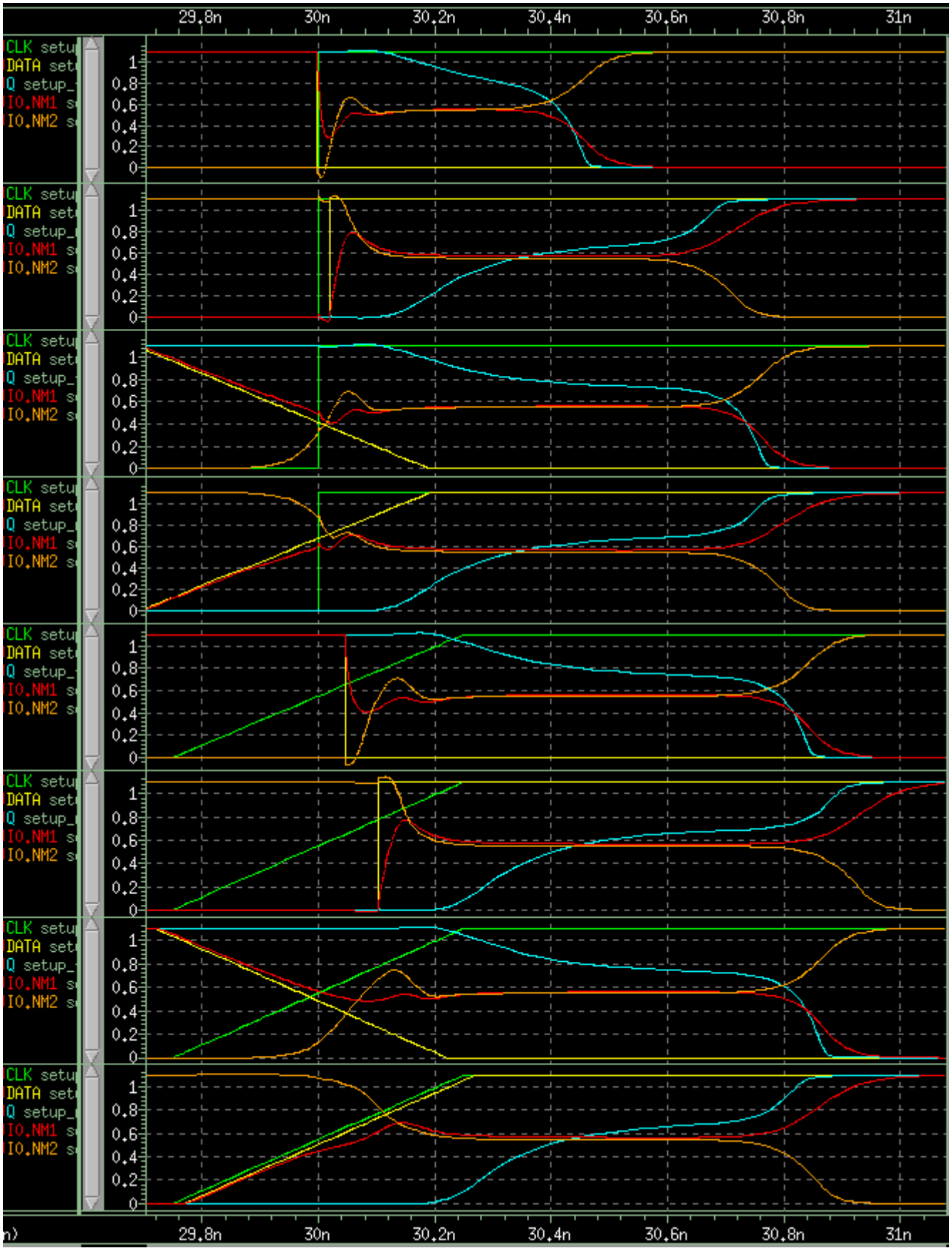
a. tS side attributes (0 to 1 transition)



b. tS side attributes (1 to 0 transition)

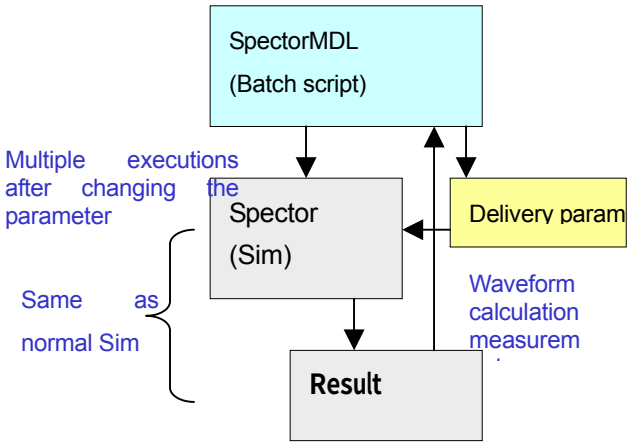


8.2.8 Example of Waveform Dependence (RC04) -- Waveform



(Reference) SpectreMDL

SpectreMDL is a script language to automate analog simulator Spectre of Cadence Co. For details on syntax, refer http://www.hoku.renesas.com/EDA/tools/cgi-bin-view/to_sel_menuframe.pl or contact 設技括／ＡＥＦ開.



Features:

- Performs loop and binary search
- Since the arithmetic operations and waveform calculations can be executed, based on their results Sim can be automatically executed by different parameters
- The measurement results are saved in a text file

• Shortcomings:

- License is different from Spectre‥
- There is no technique of passing values between multiple batches (Although it can be done through a file‥it may not be successful in case of a continuous action as the file does not have flash).

Example of current setup search

↓Execution command　↓ Digits of report files

```
bs -source /common/appl/dotfiles/mmsim.CSHRC_6.0_isr29 spectremdl -prec '%.35g' -design meta.scs -batch
meta_s.mdl
```

File for normal Sim ↑

↑Batch file (MDL description)

meta.scs

```
// For T0 & tau
// (C)2007 Renesas Technology Corp. Y. Takahahsi
simulator      lang=spectre
global         0 VDD! VSS!
parameters     tdd=-1e-15 vol_VDD=1.1 tdH=318.8n tdL=288.8n tdC=408.8n
include        "param_r.scs"
I0 (CLK  DATA  Q  VDD!  VSS!) TB1DFFJQXC
          :
V3 (DATA 0) vsource type=pwl wave=[0n 0 (30n-t2) 0 (30n+t2) vol_VDD] delay=0n
          :
tranMeta tran stop=60n errpreset=conservative autostop=no ¥
     errpreset=conservative annotate=status maxiters=5
          .
```

File is included for passing the parameters to the batch of Loop (First, the dummy is required).

meta_s.mdl

```
// search fot tmeta
// by Y.Takahashi MC-Setugi (C)2007 RENESAS
// tS/tH search #0-------------------------------------------------------------
Calling the transition analysis
alias measurement setup_r {
  export  real TV, Th, Clk_r, Data_r, Out, DataQ, aT
  run tranMeta
  Clk_r =cross(sig=V(CLK),  thresh=vol_VDD/2, dir='rise, n=2)
  Data_r=cross(sig=V(DATA), thresh=vol_VDD/2, dir='rise, n=1)
  Out   =cross(V(Q),        thresh=vol_VDD/2              )
  DataQ =V(Q)@50n
  TV    =vol_VDD
  Th    =vol_VDD/2
  aT    =V3:delay
}
// search rise tS
search V3:delay from binary(start=5n, stop=-5n, tol=0.00000001a) {
  run setup_r
  print fmt ("%-15s%.37g¥n¥n", "parameters tmeta_r=", V3:delay) to="param_r.scs"
} until ( setup_r -> DataQ > vol_VDD/2)
```

Definition of measurement alias

Calling the measurement alias

Param writing

param_r.scs

```
parameters tmeta_r=2.77595507473284946207731511241925985 1e-11
```

Loop also written in the same

meta_loop.mdl

```
foreach delta from swp(start=0.5n, stop=0.1a, log=20) {
       V3:delay=tmeta_r-delta+0.1a
        run td1_r_tS
```

Execution script of logarithm sweep

8.2.9 Measurement of Metastability Attributes

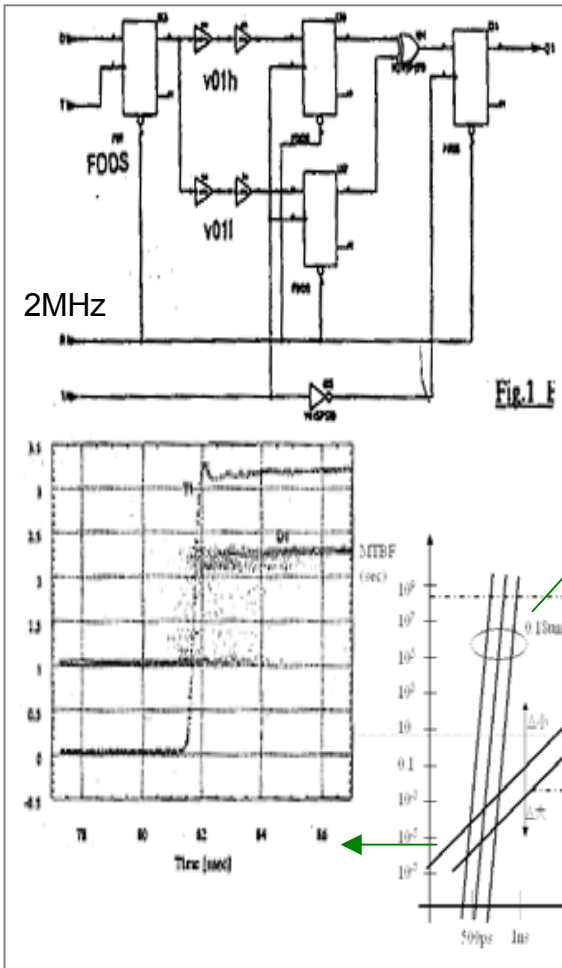
A common method of measuring the Metastability attributes is the method of counting errors by giving inputs that actually cause Metastability. Therefore, structure such as those given in the instructional text shown in the figure below is used frequently. However,

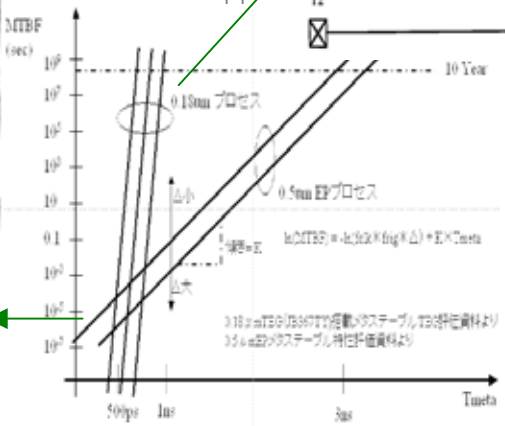
①Only mid-point voltage is not in bad status

②Error status in (statistically homogeneous) occurs in [resolutions less than quadrillion seconds] , hence is difficult. Thus it is not successful. (In reality, the features are not as good as shown here) The actual value must be used after correct understanding of rules/fundamentals and important points regarding these measurements. It is essential that the incorrect measurements are not ignored and defects are not left hidden.

Heisei 6 Mitsubishi Electric

'0.5μmEP Metastability attributes evaluation'





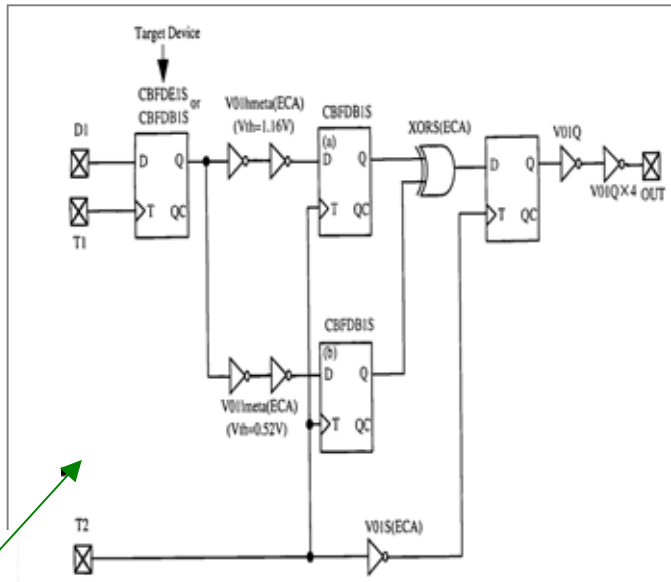
Jitter added to data

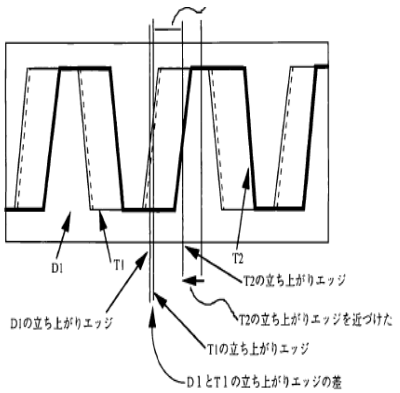
(What is the structural distribution of jitters?)

Although the measurement is theoretically correct, but it may not hit the sweet spot due to a statistically homogenous problem in the jitter. (Due to oversight, the attributes may appear better than actual).

1999 Mitsubishi Electric

'0.18μmTEG-mounted Metastability TEG evaluation'





TS is fixed to a suitable (standard

Data format only as per RZ 1

Measurement of which theory is difficult to understand in the explanation given in the report? (vdiff dependence of tmata is not considered) MTBF of asynchronous signal transfer cannot be assumed in the measurement "distribution of tmeta of special Metastability conditions" if there is no change in the report. Moreover, in the result analysis, discontinuation of partial data and "straight line section only"

Note: The observation method is not comprehensive, hence observation should be done thouroughly

Measurement Request

1. Defects in both, 'CLK->Q delay' and 'midpoint voltage' should be captured
2. It can be verified that the error distribution is "statistically uniform".
3. Time resolution of error inputs should be adequately small. (About quadrillion of 10 is necessary)

(Reference) How to create input signal, and example of measurement system

Considering the uniformity of distribution and time resolution, it is impossible to randomly distribute the data edge, therefore it is considered to scan the complete timing in 2 extremely close frequencies. Since the range of frequency resolution of high-grade PG is 8 digits, and the source oscillation of multiple devices can be bilaterally locked (apart from absolute value and instant fluctuation) the frequency ratio can be configured at 8-digit precision as an average of the measurement period. (Confirm with the manufacturer).

Distribution in random number is discontinued and is done in round robin

→ Two oscillators of nearly identical frequencies are used and it is observed for a very long time (For instance, if the frequencies are 20MH and 20,000,001Hz, the round robin of distribution will be 2.5fs+fluctuation in 50ns and 49.9999975ns)

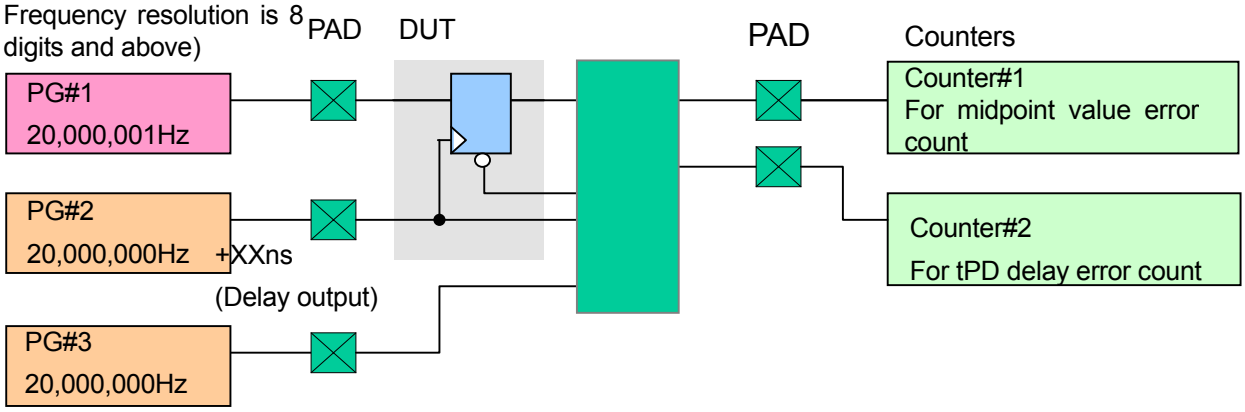
Combination of DTG5078+DTGM21 and AFG3251 (approx 5 million yen)

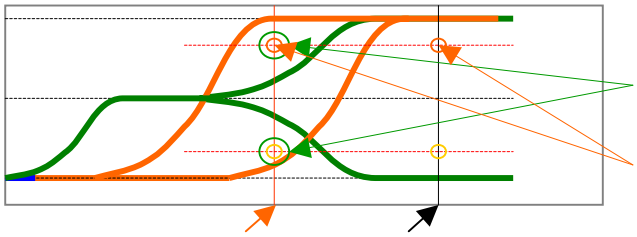
Textronix DTG5078 format/DTG5274 format/DTG5334 format etc.

Extracted from http://www.tektronix.co.jp/cgi-bin/frame.cgi?body=/products/signal_sources/dtg5000d.html

Example of measurement system

- In order to guarantee input Error distribution, the measurement is executed by round-robin as per the cycle difference.
- tPD delay measurement is used at the same time since it is difficult to output midpoint values in buffered
- Since the tPD delay measurement is inefficient in successive identical expected values, each clock is





Midpoint value determination using 2

TPD delay determination using time difference
(The threshold value is at 2 places, tPD appears abnormal in either one of them in case of midpoint voltage.)

DUT is obtained here

Determined by taking this as the

The measurement of single cell of RC01S-HND is in the planning stage
Actual survey example will be added to this document in autumn 2007