MOS Device: Basics

- MOSFET & Modeling -

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Lecture 3

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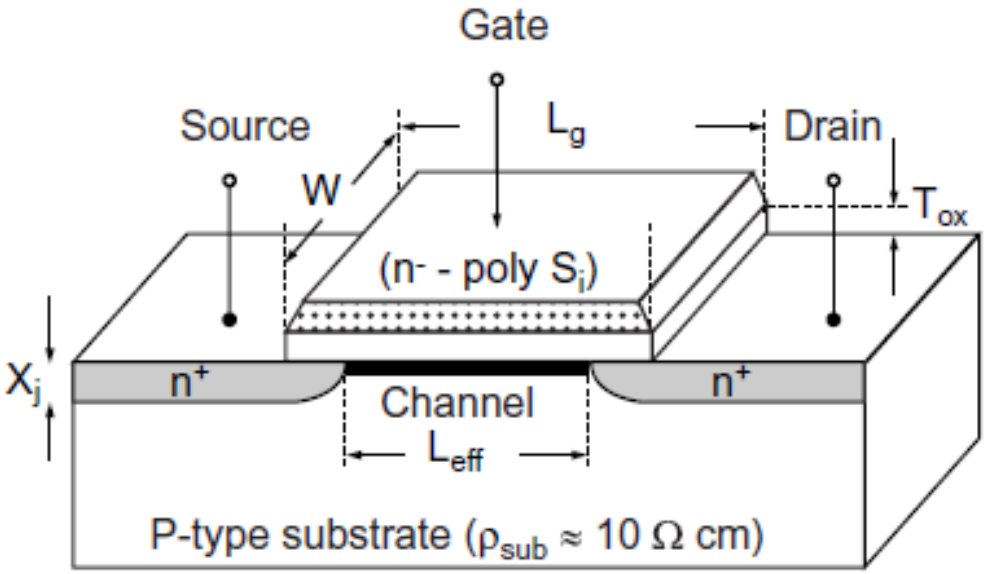
(5) MOSFET: Basic structure



Electrodes:

Source: Source of Electrons
(pin from which electron flows out)
Drain: Drain the Electron
(pin to which electron flows in)
Gate: Control gate for electron flow
Substrate: Fixed silicon substrate bias

Structural parameters:

Planar dimensions = Lg, Leff, and W
Longitudinal dimensions = Tox, Xj, and ρ sub

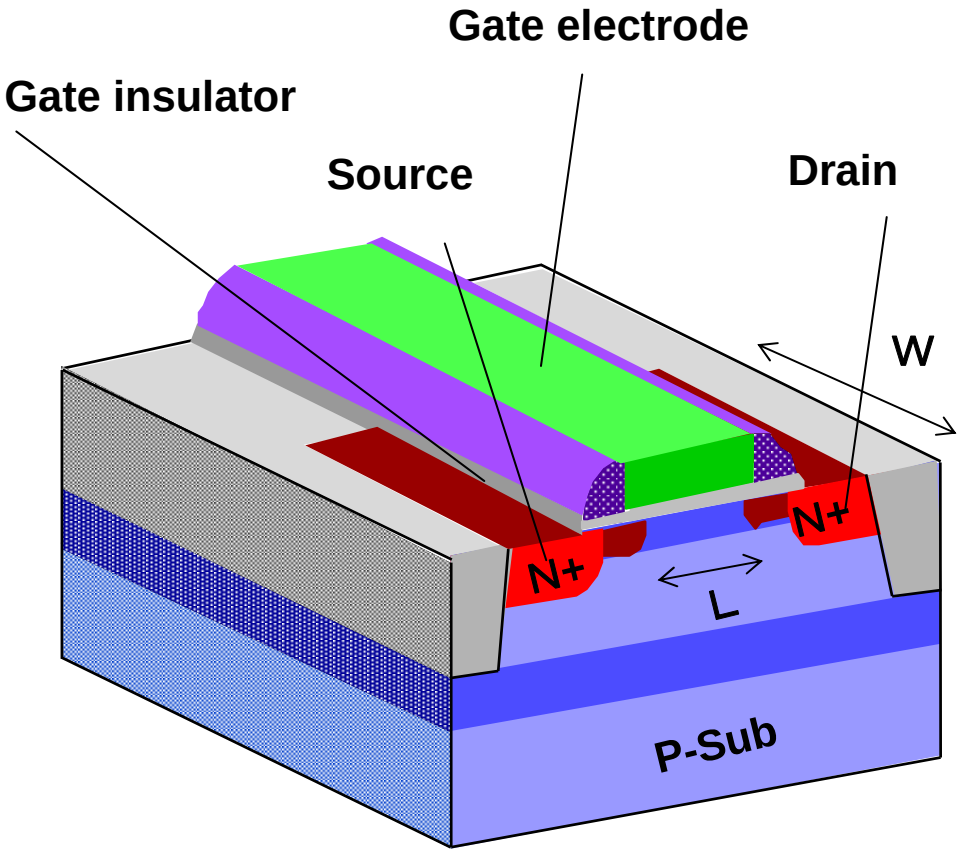
Operation:

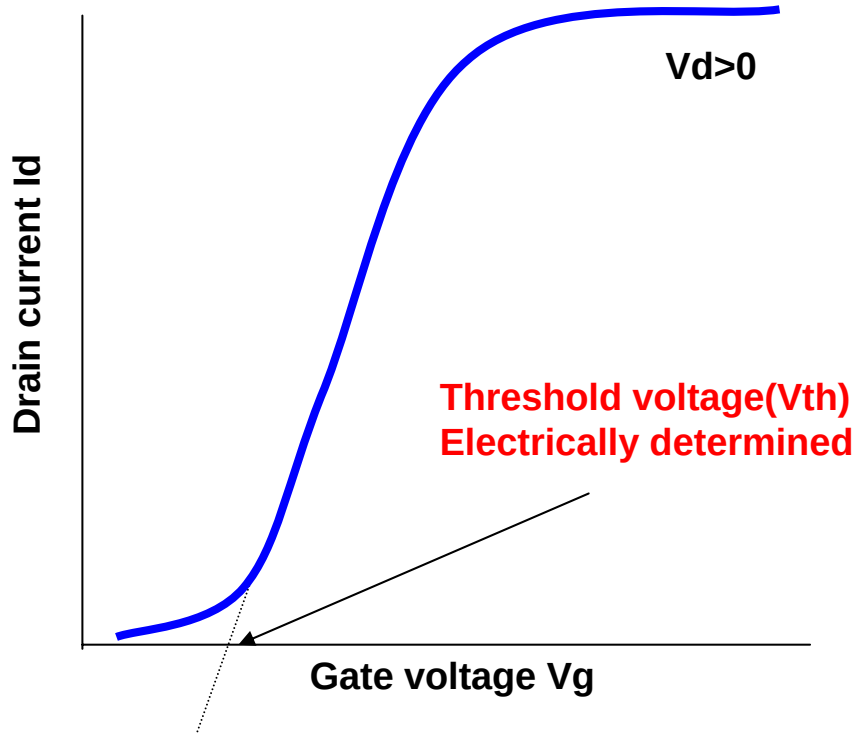
The conductance between source and drain is controlled by the gate voltage.

Features

1) Input impedance = completely capacitive. It allows direct circuit connection.
2) Utilization of silicon surface (channel) conduction. It gives easy to isolate devices, which is ideal as highly integrated LSI device.

MOSFET 3D-Image and Typical I-V Curve





L:Channel length
W:Channel width

$$V_{th} = \left(\phi_{MS} + \frac{Q_{ss}}{C_o}\right) + 2\phi_F + \frac{Q_B}{C_o}$$

How to Fabricate MOSFET; Photo-Lithography

Photolithography is the most important LSI process step.

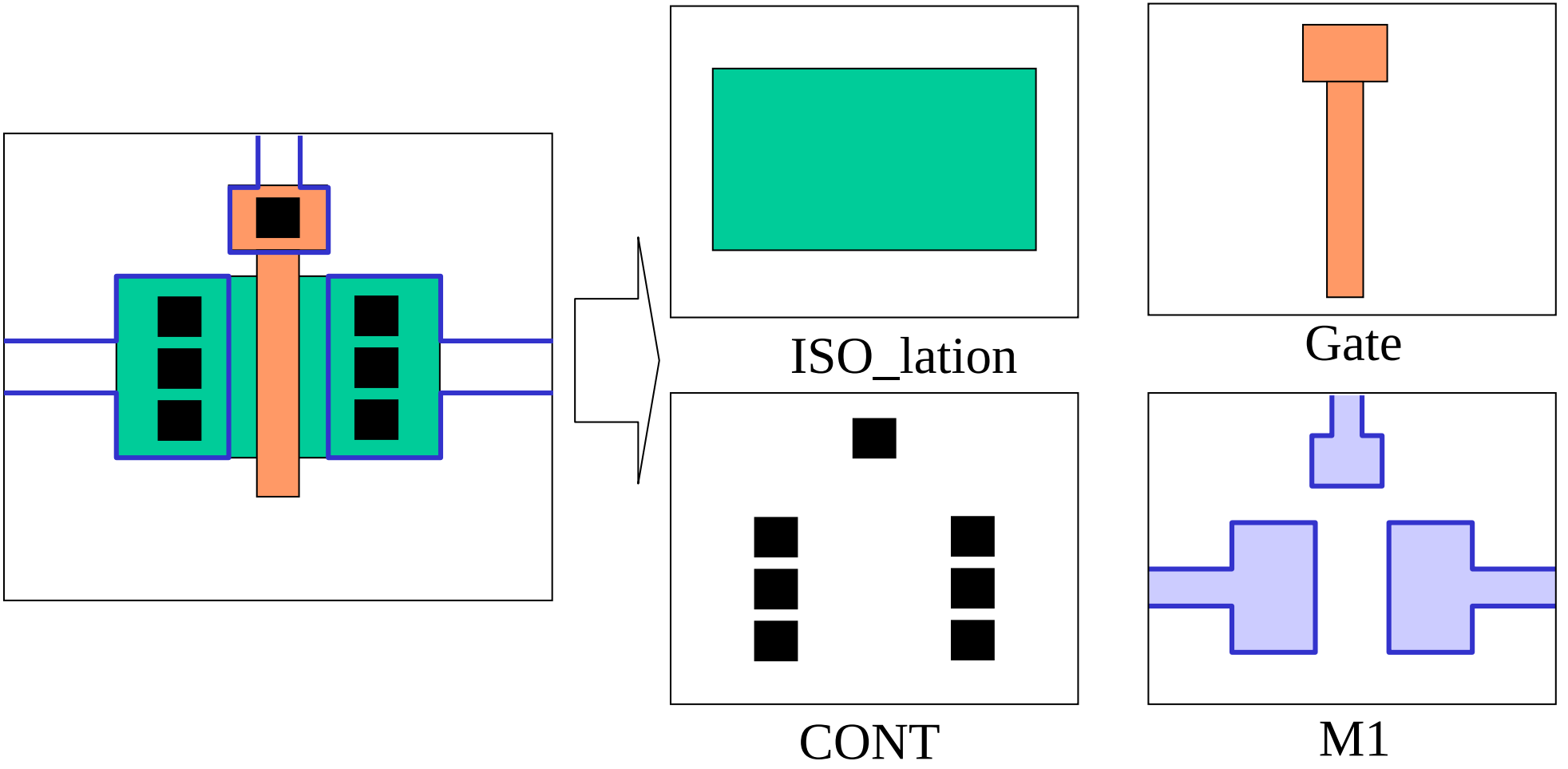
It is the same as photo printing process with Nega-film in optical photography.

In LSI process, we use Photo-mask instead of Nega-film.

Photolithography allows selective etching of layers or selective implant of impurities.

Example: Mask layout of NMOS

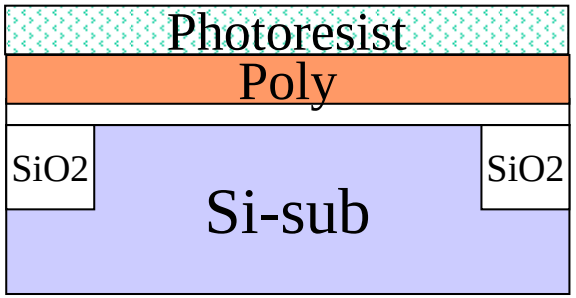
Four photo-masks for simplest NMOS design



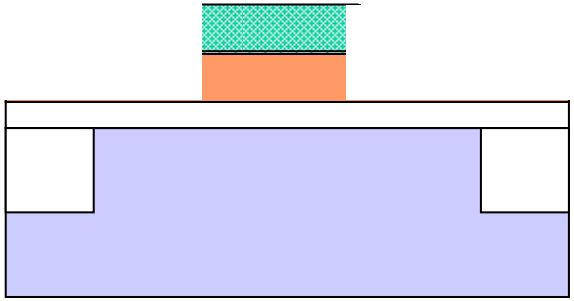
Key Process Flow; Changes in Sectional Structure

Gate Oxide & Poly deposition

Photoresist coating

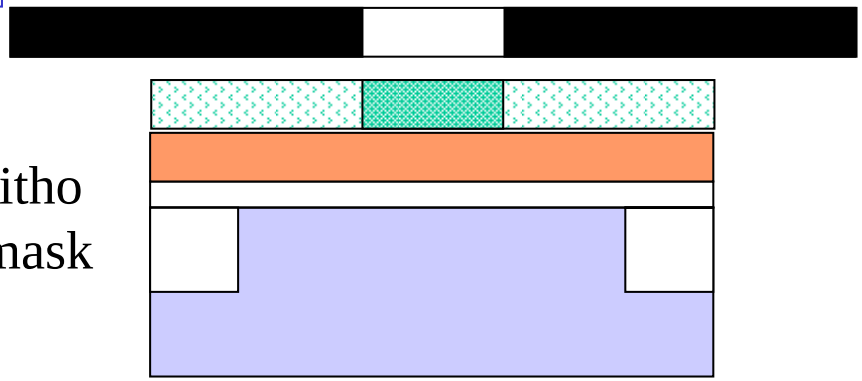


Development & baking & etch Poly



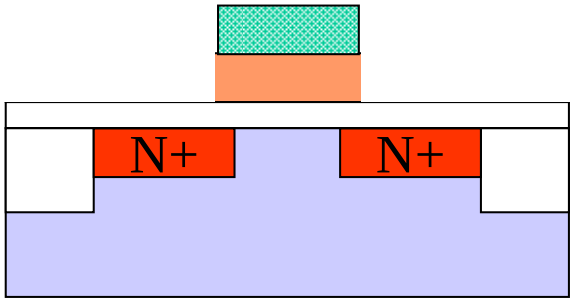
Mask

Ultraviolet light



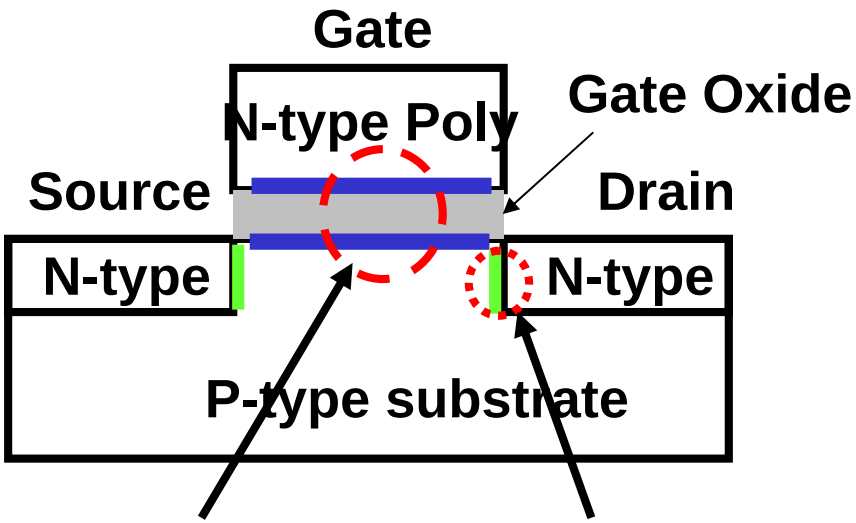
Photolitho With mask

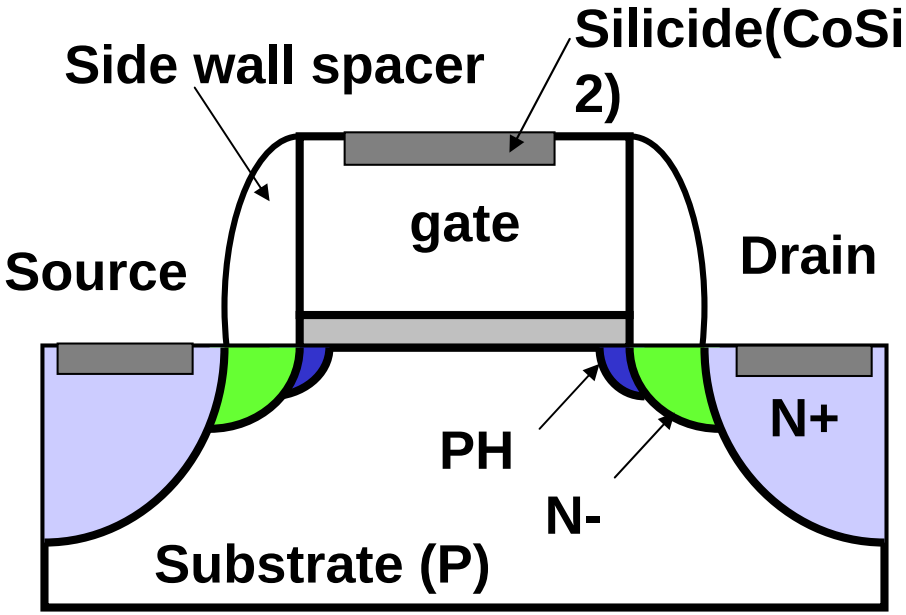
As (N-Type Impurity) ion



As Implant to form Source and Drain

Basic and Updated MOSFET structure





NMOS (Basic structure)

By applying voltage to gate, charges are induced at the capacitor.
The charges are pull out by Drain.

NMOS (Advanced structure)

N+: Diffusion layer(Highly doped N-type)

N-: Lower doped diffusion layer to relax the electric field at PN junction edge

PH: p-type diffusion layer to suppress short channel effect

MOSFET operation: I-V characteristics

There are three operational states:

Cut-off

Characteristic parameter = Threshold voltage Vth

Non-saturation (also called Linear)

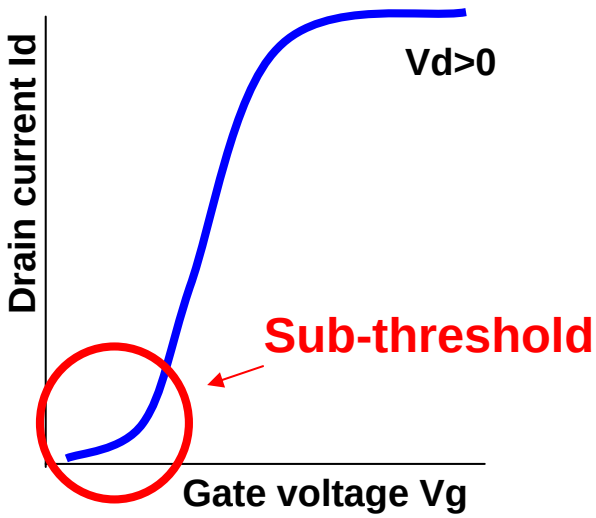
Characteristic parameter = Pinch-off voltage Vds'

Saturation

If you close look at the "Cut-off bias condition":

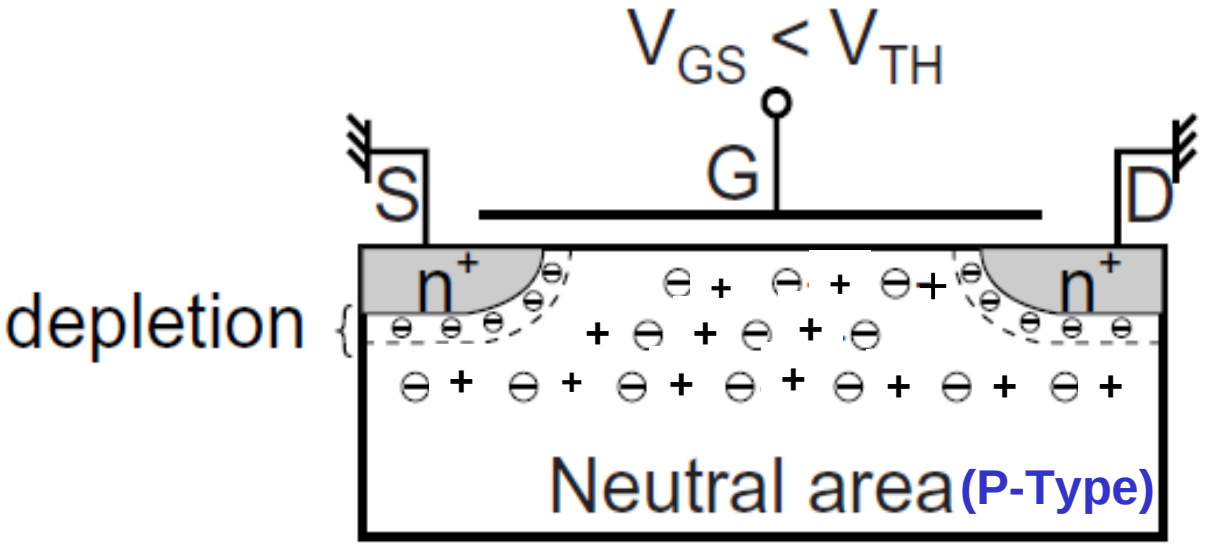
the small Ids leak-current can be characterized in Sub-threshold bias condition.

... **this leak-current is important. Since it determines CMOS leakage current! ... Limit low Pw operation.**



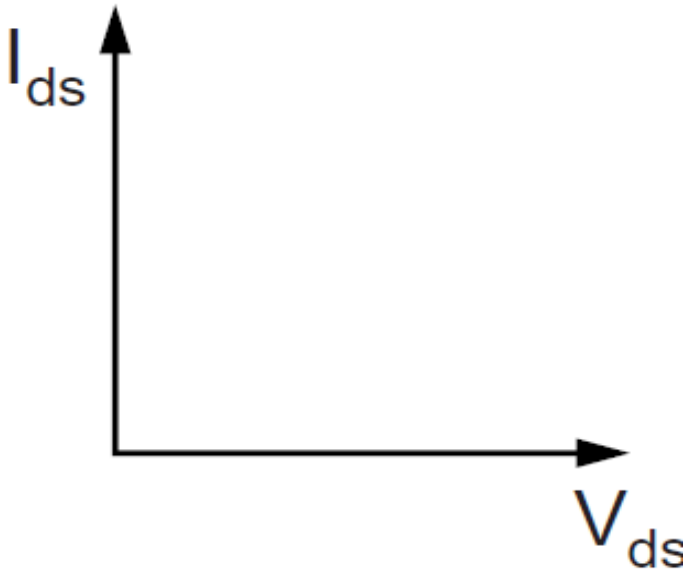
MOS Operation: Cut-off state

When Vg<Vth, no inversions at the surface, therefore no drain current Ids flows between source and drain.



⊖; Fixed Bulk Charge, + ; Hole

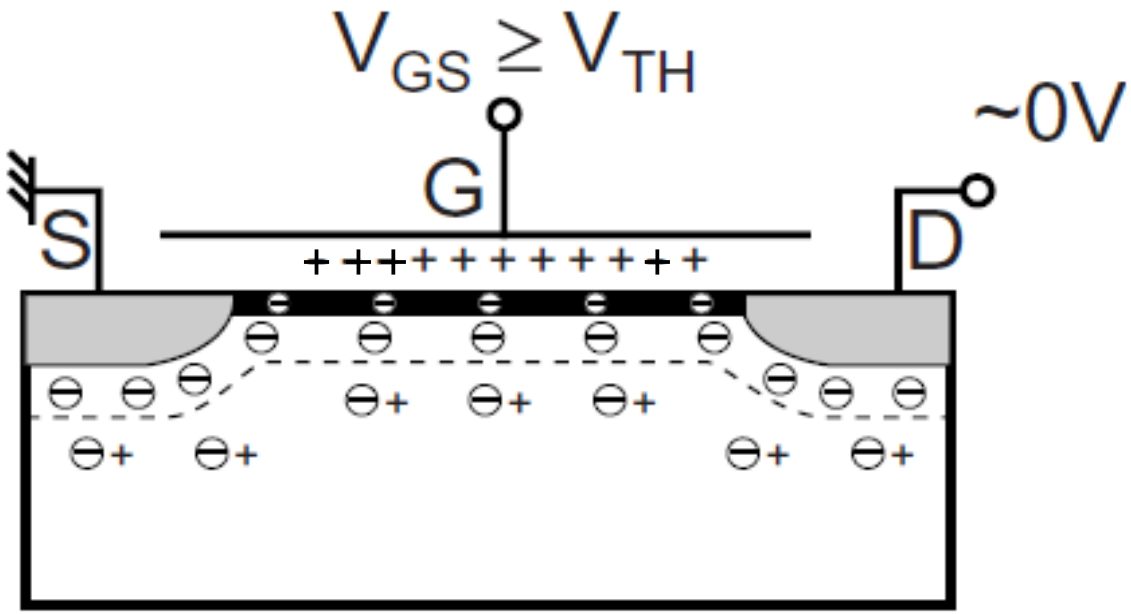
Charges and Channel



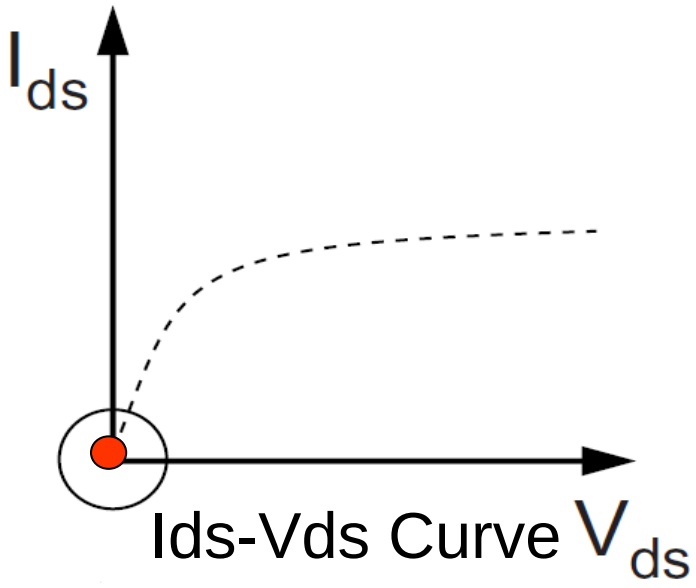
Ids-Vds Curve

MOS Operation: On state @ Vds=0V

When Vg>Vth, positive charges at Gate induce electrons at Si surface, which form a conductive "channel" between source and drain.



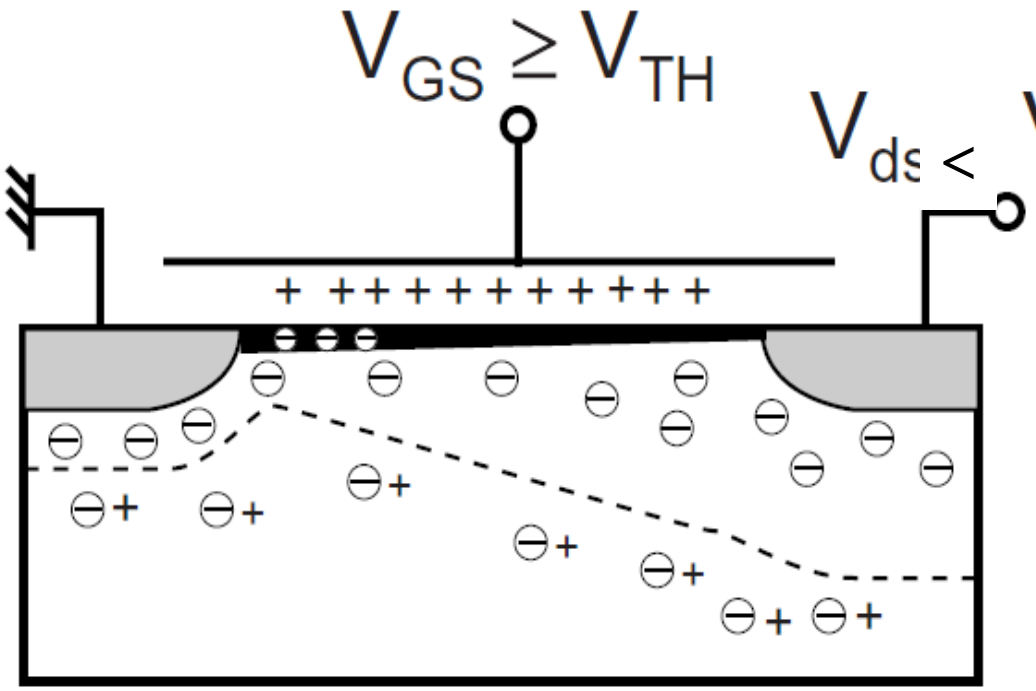
Charges and Channel



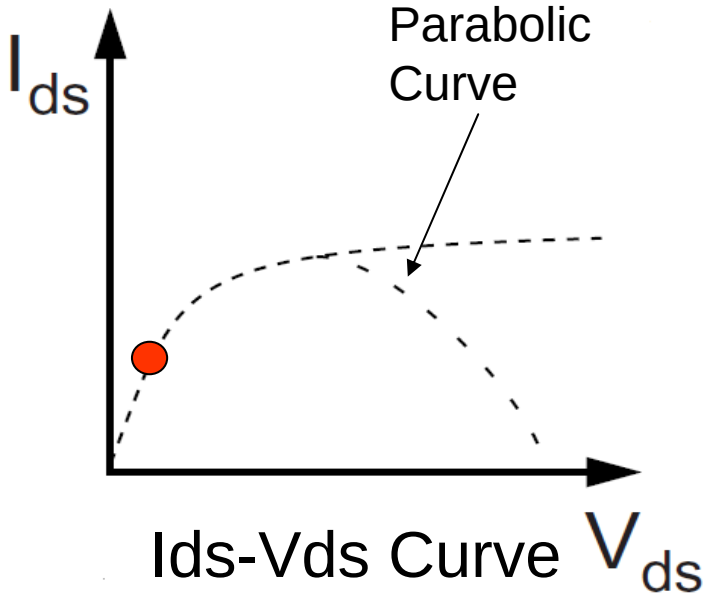
Ids-Vds Curve

MOS Operation: non-saturation state

When Vg>Vth and Vds>0V, Ids start flowing through the channel. Channel depth near the drain becomes thin compared with that at source, because Qnd=Cox(Vgs-Vds) < Qns=Cox(Vgs-Vs)



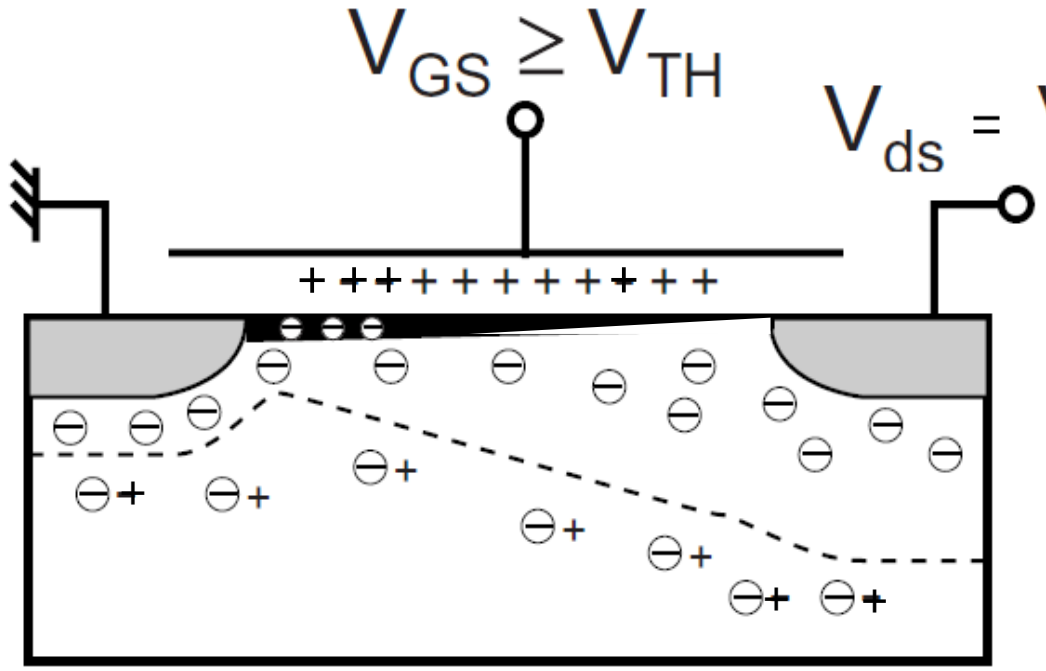
Charges and Channel



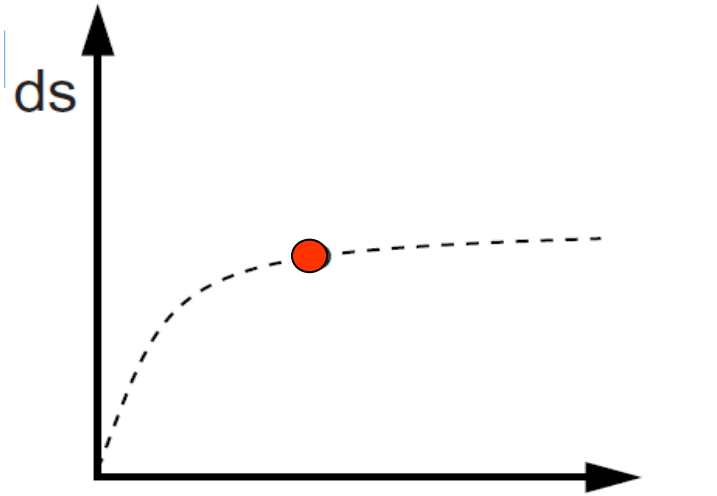
Ids-Vds Curve

MOS Operation: pinch-off state

When Vg>Vth and Vds=Vds’ (pinch-off voltage), channel depth at drain-end is pinched-off (disappeared) because Qn=Cox(Vgs-Vds’) =0 !



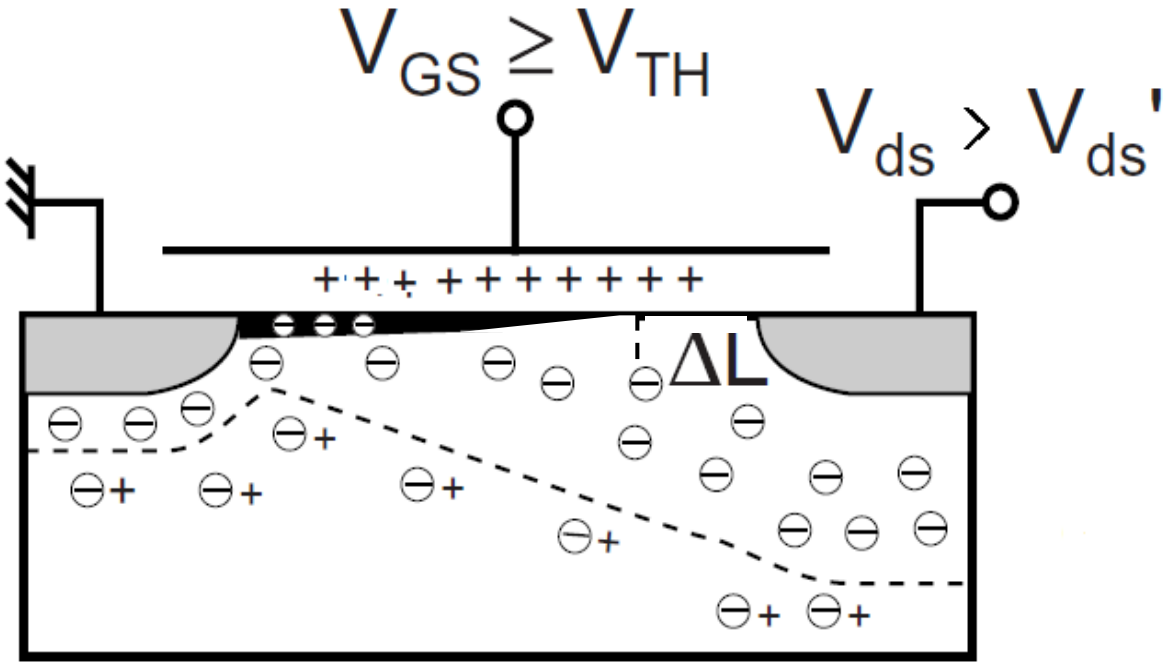
Charges and Channel



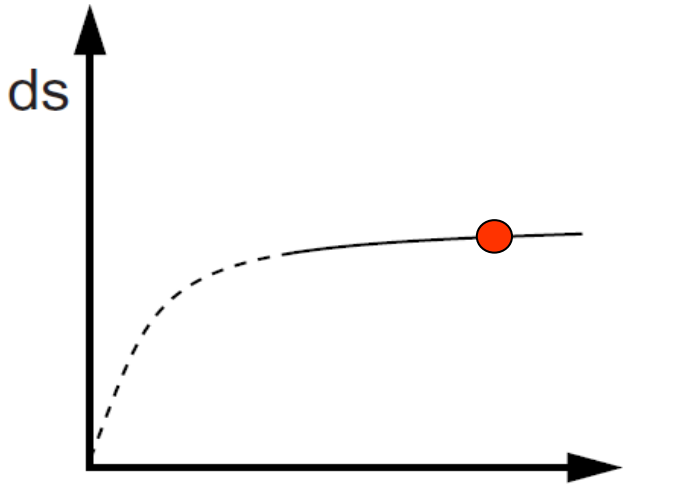
Ids-Vds Curve

MOS Operation: saturation state

When Vg>Vth and Vds are biased above the Vds' (pinch-off voltage), drain current are saturated with slightly increase due to channel shortening ΔL by high drain field effect.



Charges and Channel



Ids-Vds Curve

Summary of MOSFET Operation

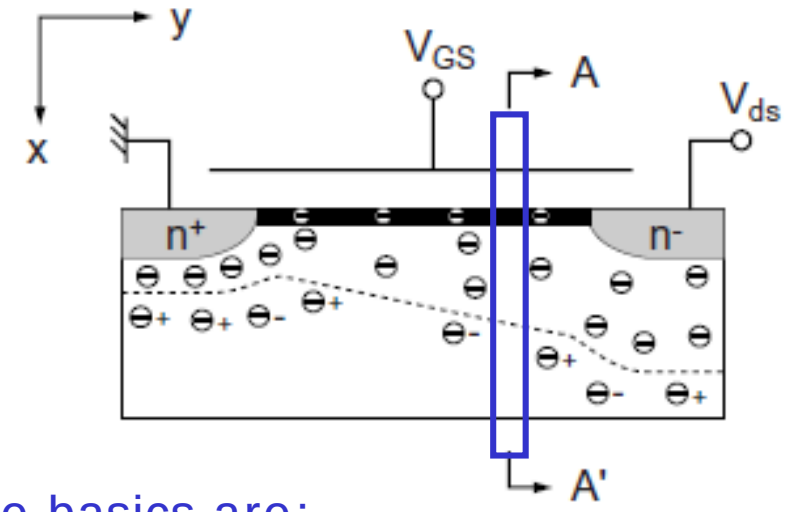
1) Voltage controlled device.

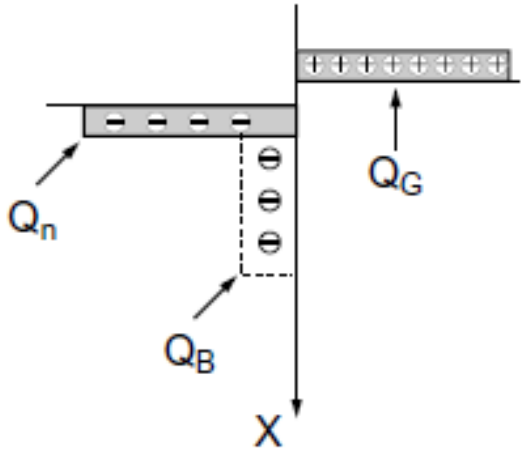
2) Can be used as a switching element.
   Ids = 0 (@ Vgs' < Vth), Ids > 0 (@ Vgs‘ > Vth)

3) Ids is characterized based on parabolic-curves, $Ids \propto Vgs^2$ at Saturation operation.

4) Bi-directional
   Symmetry even if source and drain are reversed.
   → Can be used as transfer gate (ideal switch)

Try! Physical I-V model Formulation: Gradual channel approximation





$Q_G = Q_n + Q_B$

$Q_G >> Q_B$

The basics are:

- Capacitor equation (How many free electrons ?): $Q_n = CV$
- Lateral drift current (How fast they move ?): $I = Q_{n*} v = Q_n \mu E$

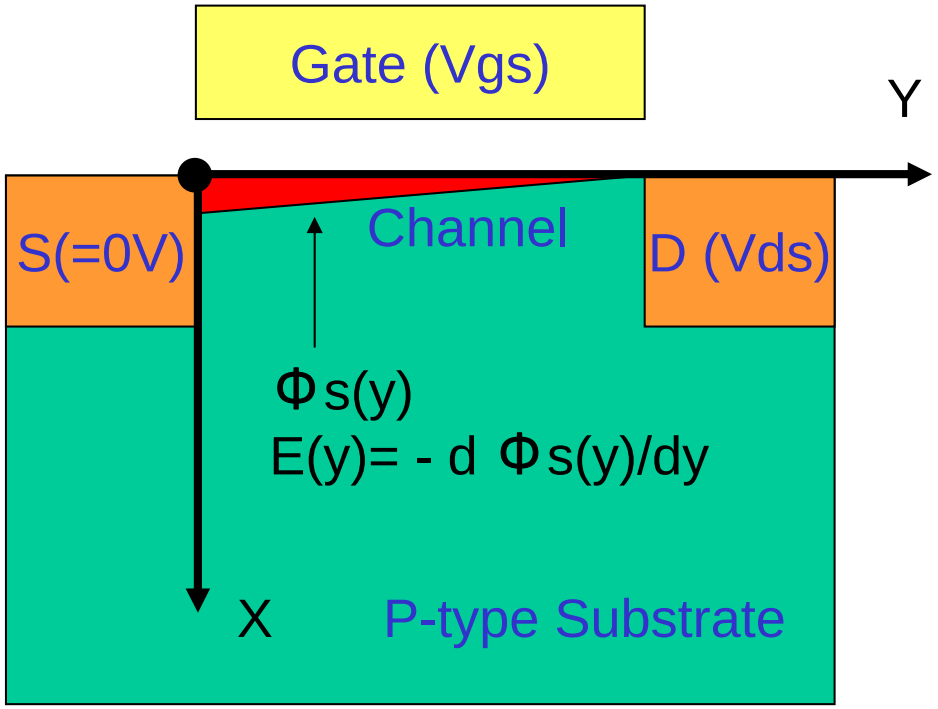
1) Capacitance Equation

$Q_n = Q_G - Q_B \fallingdotseq -Cox (V_{GS}' - \phi_S)$,

2) Drift current

$Ids = Q_n \mu W E(y)$, Here W is channel width

Some mathematics ..... (Important!)



$$I_{ds} = Q_n \mu_n W E_y$$

$$Q_n = -C_{ox} (V_{GS}' - \phi_s)$$

$V_{GS}' = V_{GS} - V_{th}$

ϕ_s (y) : Channel surface potential at y

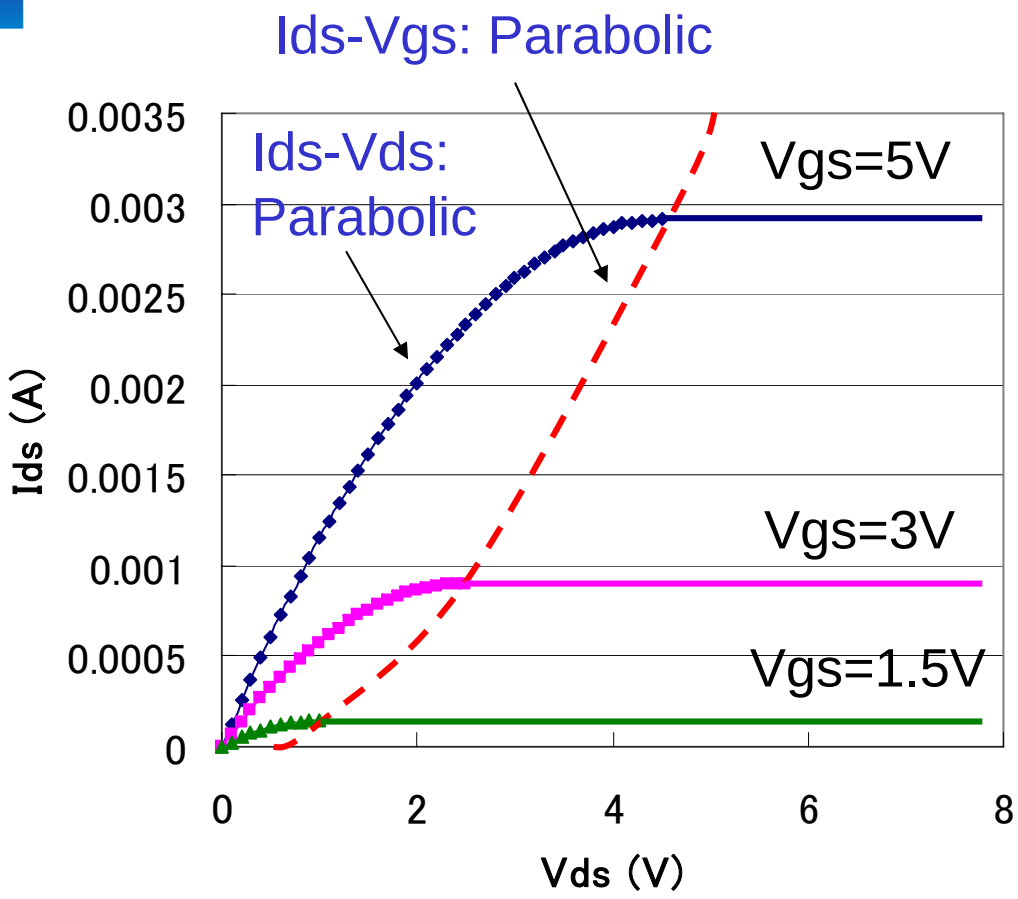
$$I_{ds} = C_{ox} \mu W (V_{GS}' - \phi_s) \frac{d\phi_s}{dy}$$

$$I_{ds} dy = C_{ox} \mu W (V_{GS}' - \phi_s) d\phi_s$$

$$\int_0^L I_{ds} dy = C_{ox} \mu W \int_0^{V_{ds}} (V_{GS}' - \phi_s) d\phi_s$$

Φs(y): Channel potential @ Y=y
E(y): Electric field in the channel

Continued …



@ 1um NMOS technology
L=1um, W=5um, Tox=30nm,
μ_{eff}=500cm^2/V.sec, Vgs=1.5, 3, 5V, Vth=0.5V

The integration results in:

$$L\, I_{ds} = C_{ox}\, \mu\, W\, (V_{GS}' V_{ds} - \frac{V_{ds}^2}{2})$$

$$I_{ds} = \frac{W}{L}\, C_{ox}\, \mu\, (V_{GS}' V_{ds} - \frac{V_{ds}^2}{2})$$

This is the basic MOSFET I-V Equation.

Schematic view of the I-V characteristics shows a parabolic based curve (see left Figure).

MOSFET characteristics are Parabolic Form!

We know;

- Ids-Vds curves
- Ids-Vgs curves
- they are all parabolic!

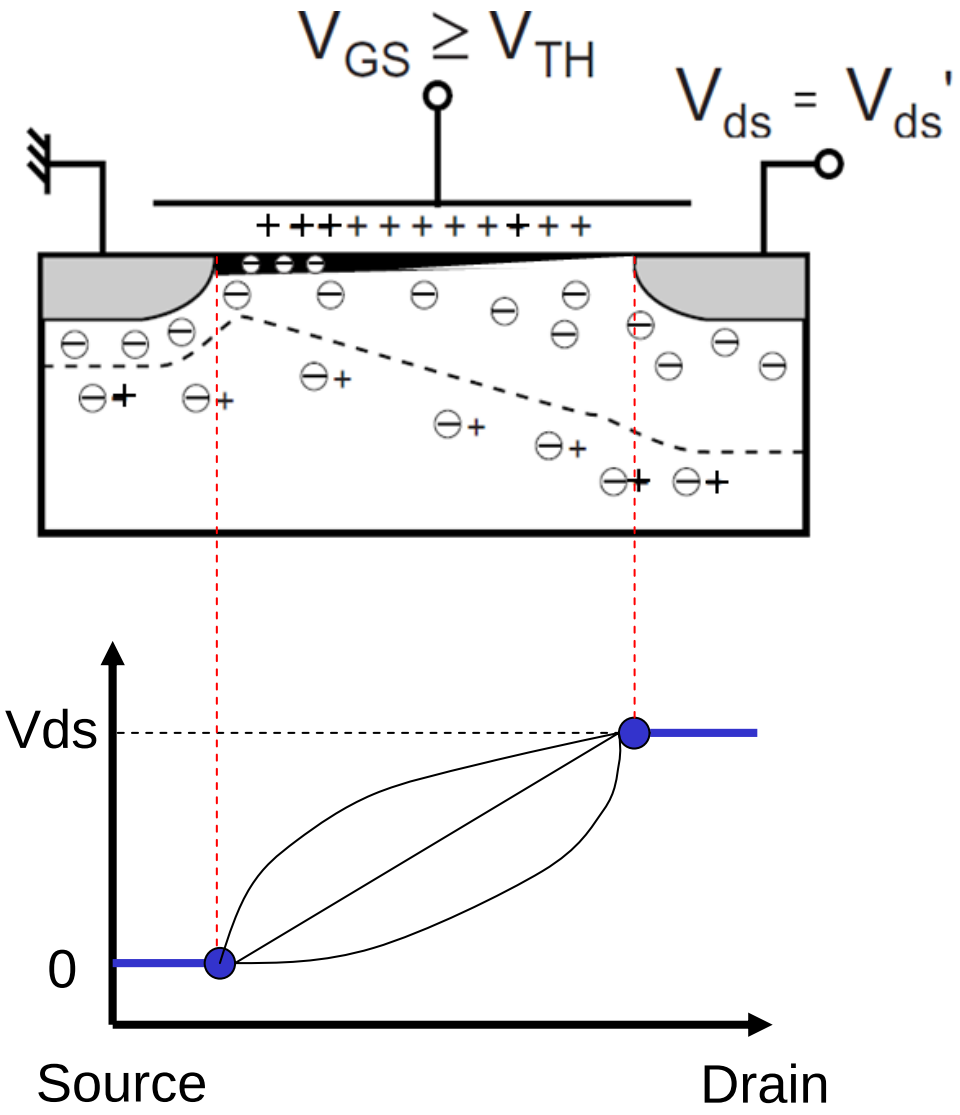
Quiz:

How about channel potential distribution between source and drain? How it looks like?

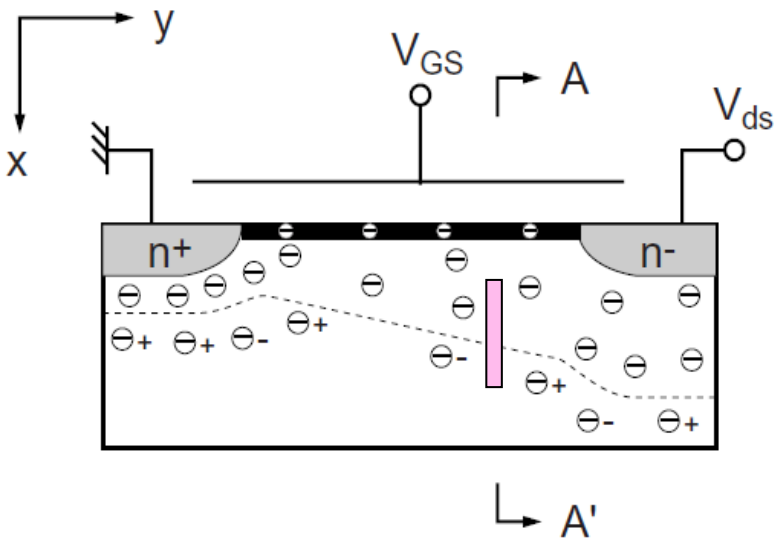
(@ saturation condition)

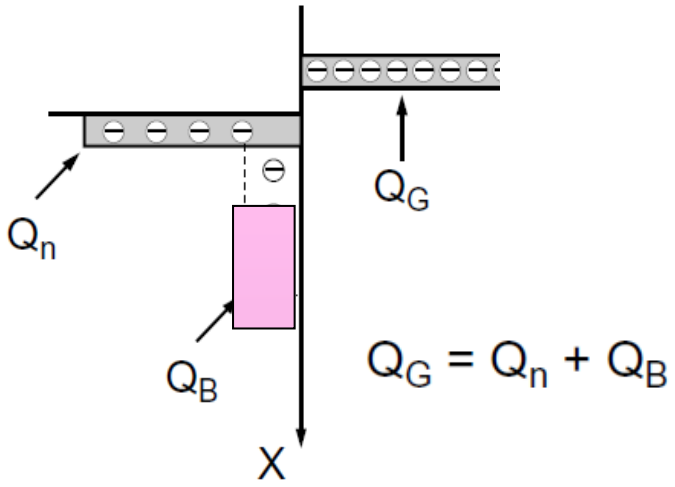
Answer:

It is also Parabolic!



physical I-V Model with bulk charge effect:
(Hofstein model)





A-A' charge diagram

In the Simple model, we neglect bulk charge (Q_B).
More accurate approach is to consider the bulk charge.
It brigs a new charge equation as follow:

$$Q_n = Q_G - Q_B = \underbrace{-C_{ox}(V_G' - \phi_s)}_{Q_G} + \underbrace{\qquad}_{Q_B \text{ (Depletion layer charge)}}$$

MOSFET I-V characteristics

By using similar derivation process, we can get the I-V equation, as follow:

$$I_{ds} = -Q_n \mu_n W E_y$$

$$= \mu W \left[C_{ox} (V_G' - \phi_s) - \sqrt{2\varepsilon_s q N_A} \sqrt{\phi_s + 2\phi_F} \right] \frac{d\phi_s}{dy}$$

$$\int_0^L I_{ds} dy = \mu W C_{ox} \int_0^{V_d} \left[(V_G' - \phi_s) - K_b \sqrt{\phi_s + 2\phi_F} \right] d\phi_s$$

$$\therefore$$

$$I_{ds} = C_{ox} \mu \frac{W}{L} \left\{ (V_{GS}' - \frac{V_d}{2}) V_d - \frac{2}{3} K_b \left[(V_d + 2\phi_F)^{\frac{3}{2}} - (2\phi_F)^{\frac{3}{2}} \right] \right\}$$

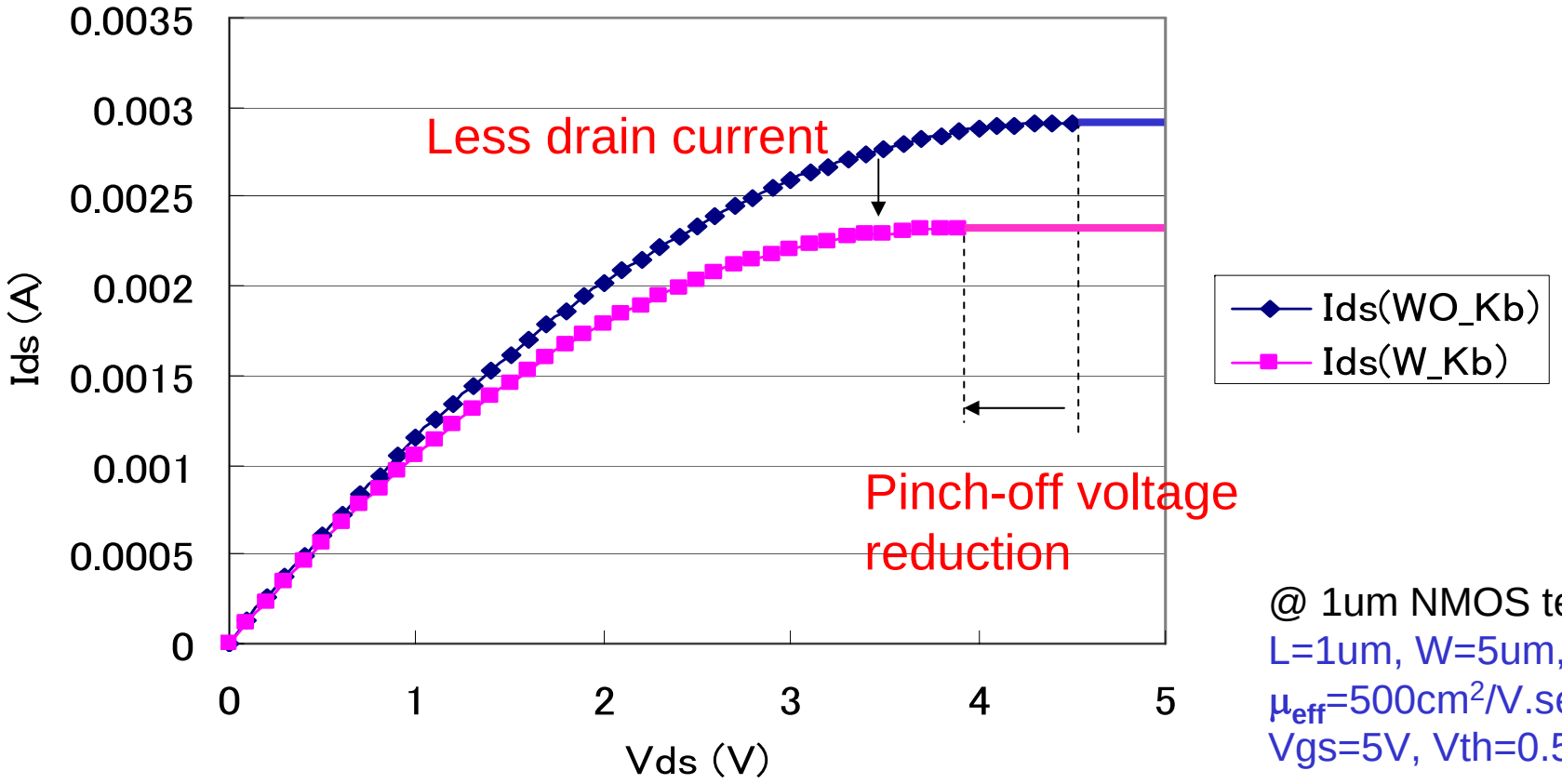
Bulk charge effect

$$K_b \equiv \frac{\sqrt{2\varepsilon_s q N_A}}{C_{ox}}$$

:Substrate bias effect coefficient

How different ?
with taking into account “bulk charge”

“With bulk charge” model is more accurate physically:
It results in an early pinch-off voltage and less drain current



@ 1um NMOS technology
L=1um, W=5um, Tox=30nm
μ_{eff}=500cm^2/V.sec, Kb=0.5
Vgs=5V, Vth=0.5V

Show Time on I-V Characteristics!

MOSFET Operation

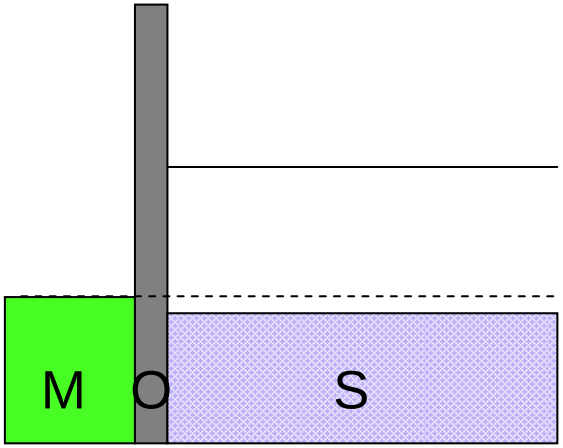
- Electrons
- Band Structure
- I-V Characteristics

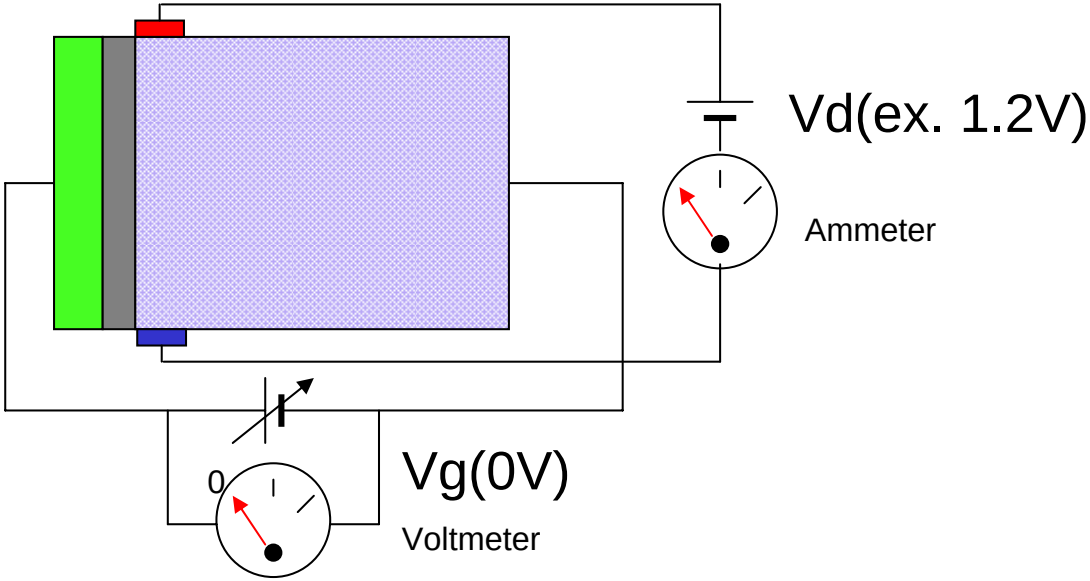
The above physical quantities are changed by:

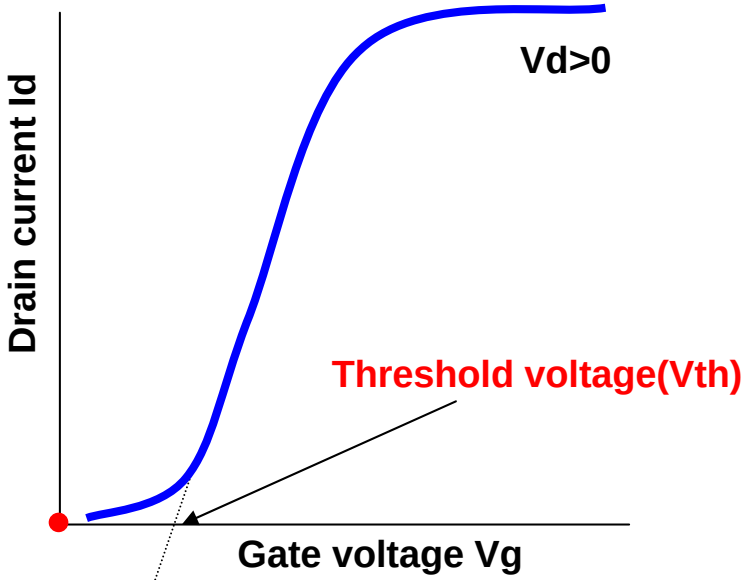
- Gate Bias Voltage = Vg
- Drain Bias Voltage = Vd

Operation of N-channel MOS(NMOS)FET

- Gate characteristics: Id-Vg characteristics



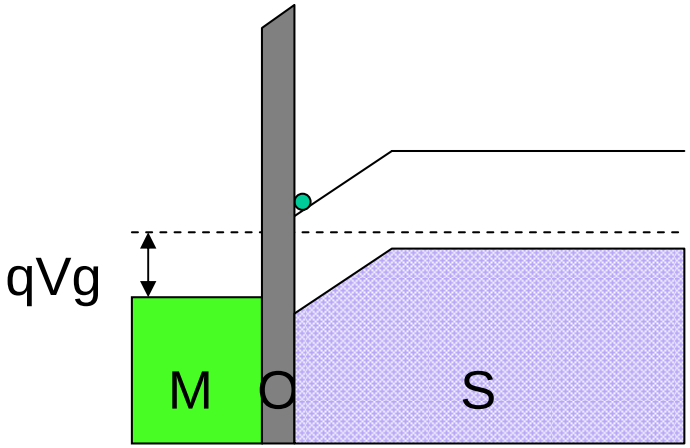


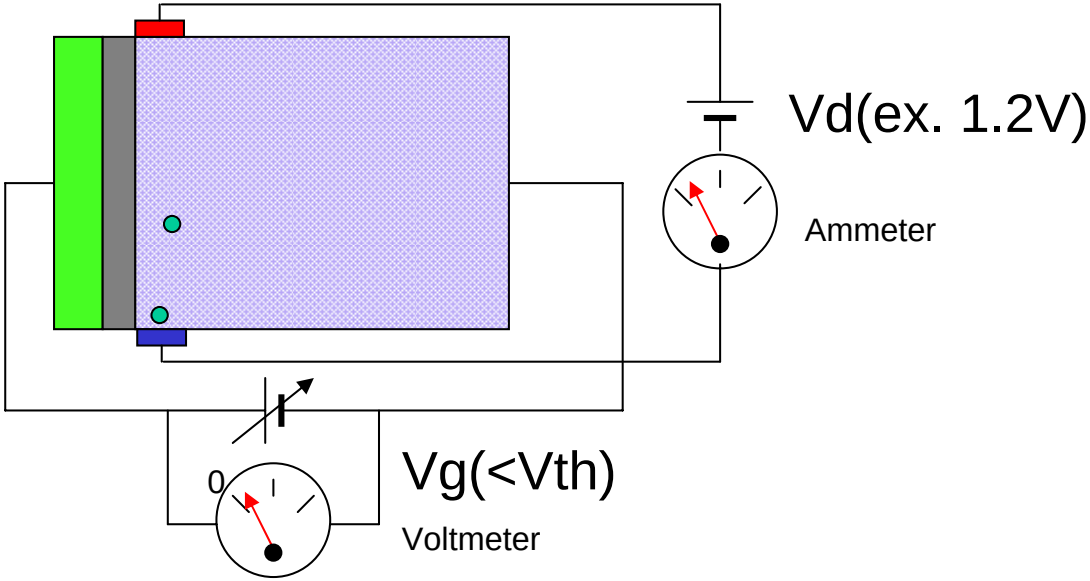


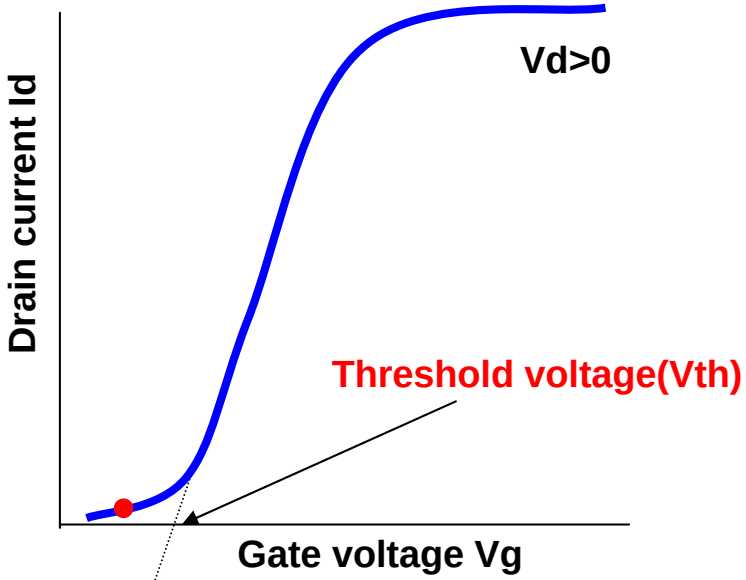
OK, we will see what happen when gate voltage is increased @ Vds=1.2V.

Operation of N-channel MOS(NMOS)FET

- Gate characteristics (Vgs<Vth)



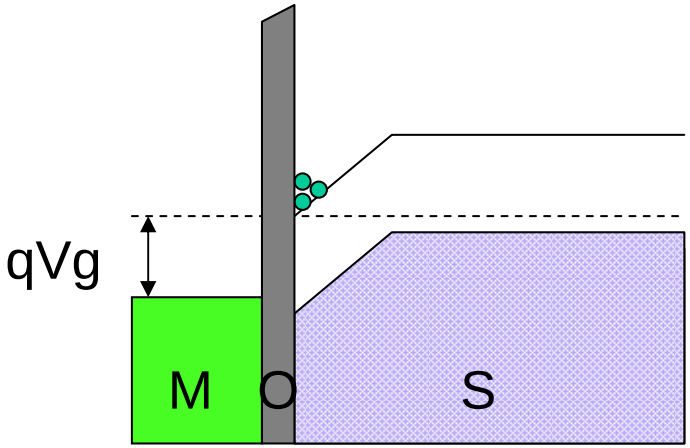


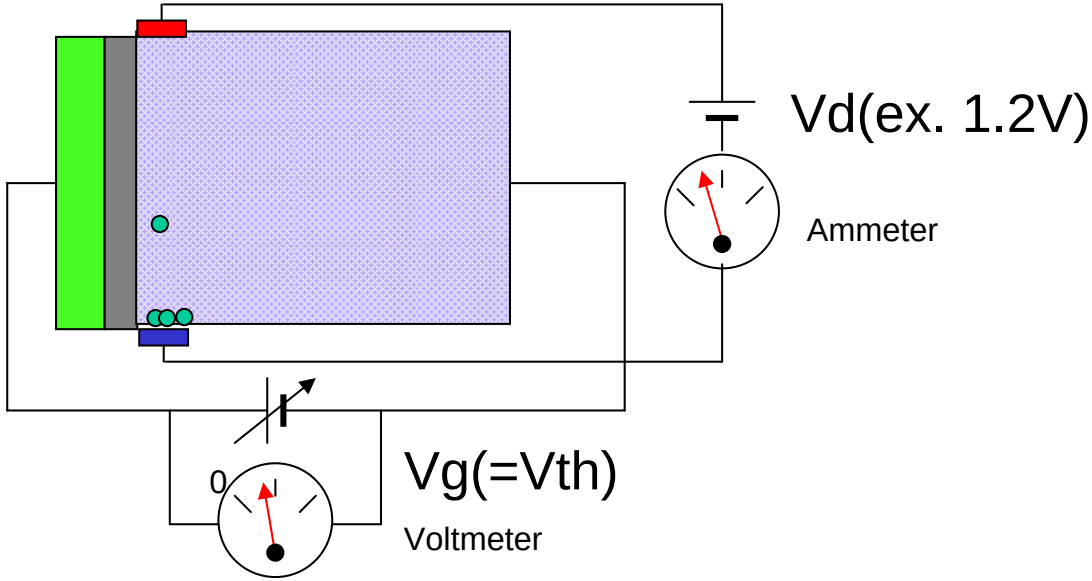


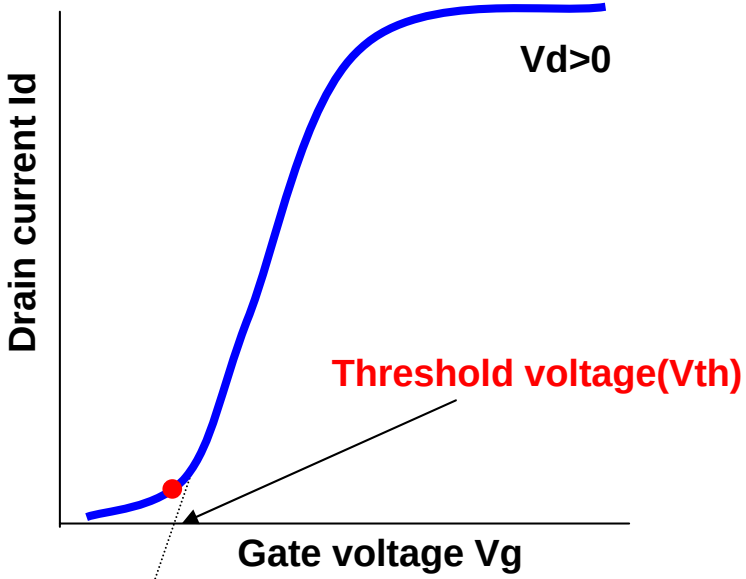
The current under Vgs<Vth is called sub-threshold current.
This is one of leakage currents.

Operation of N-channel MOS(NMOS)FET

- Gate characteristics (Vgs=Vth)



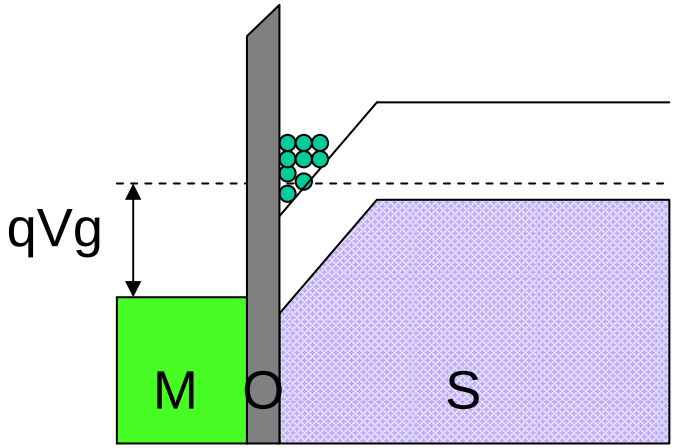


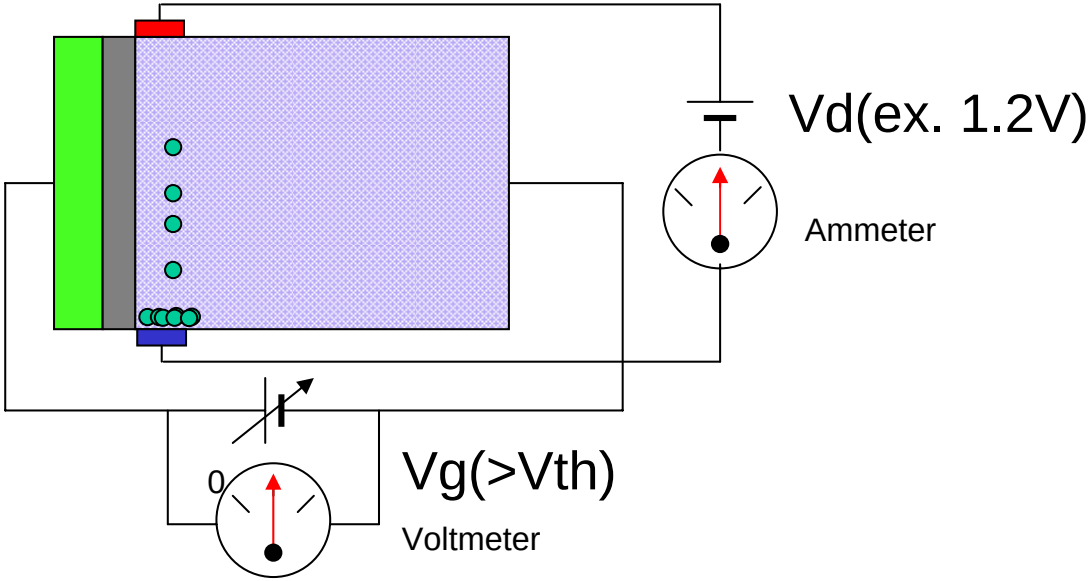


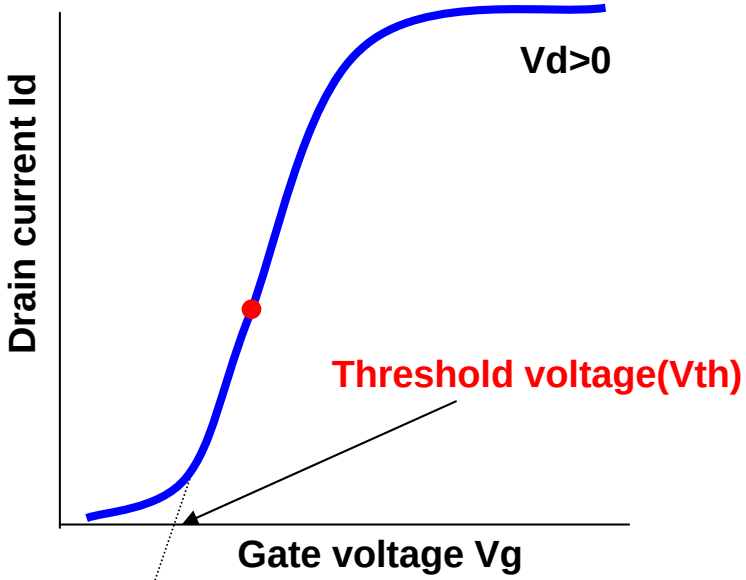
When gate is biased at Vth, leak-current of 0.1μA-order does flow between source and drain. (for L=W square NMOS)

Operation of N-channel MOS(NMOS)FET

- Gate characteristics (Vgs>Vth)



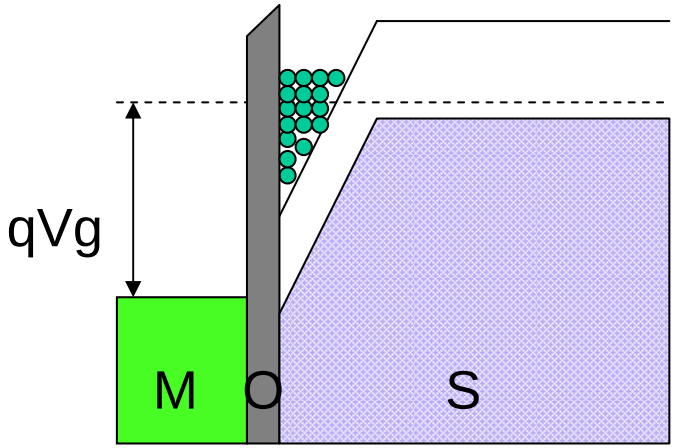


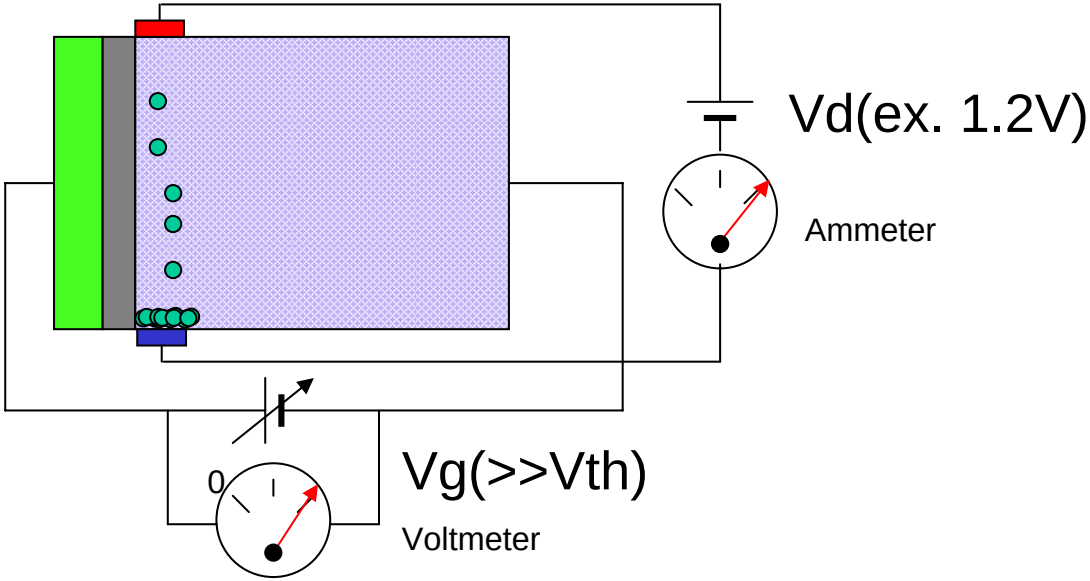


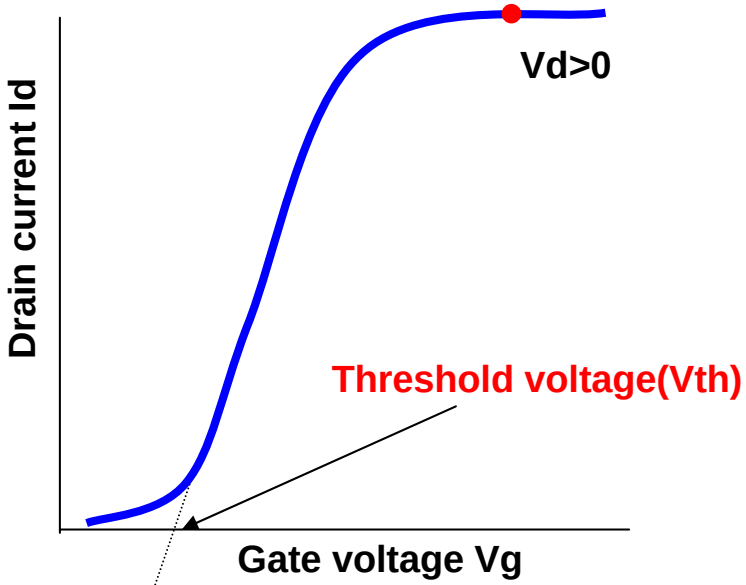
When gate is biased above th Vth, drain current increase sharply in proportion to $(Vgs-Vth)^2$.

Operation of N-channel MOS(NMOS)FET

- Gate characteristics (Vgs>>Vth)



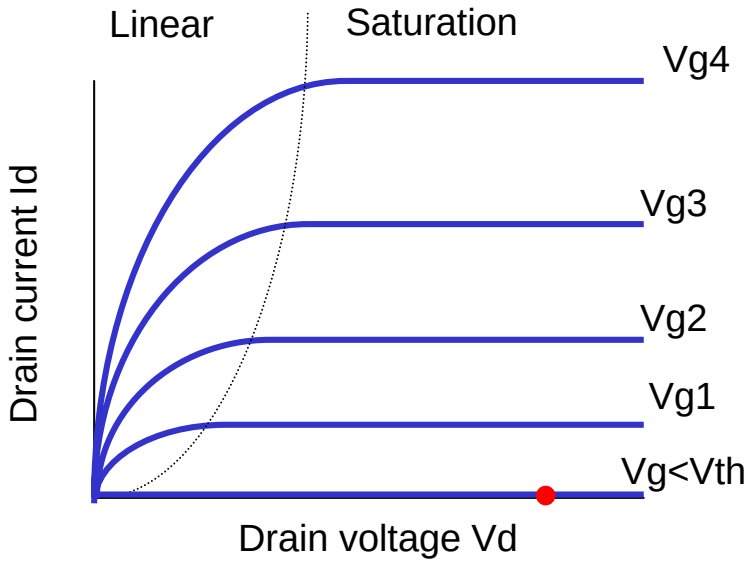


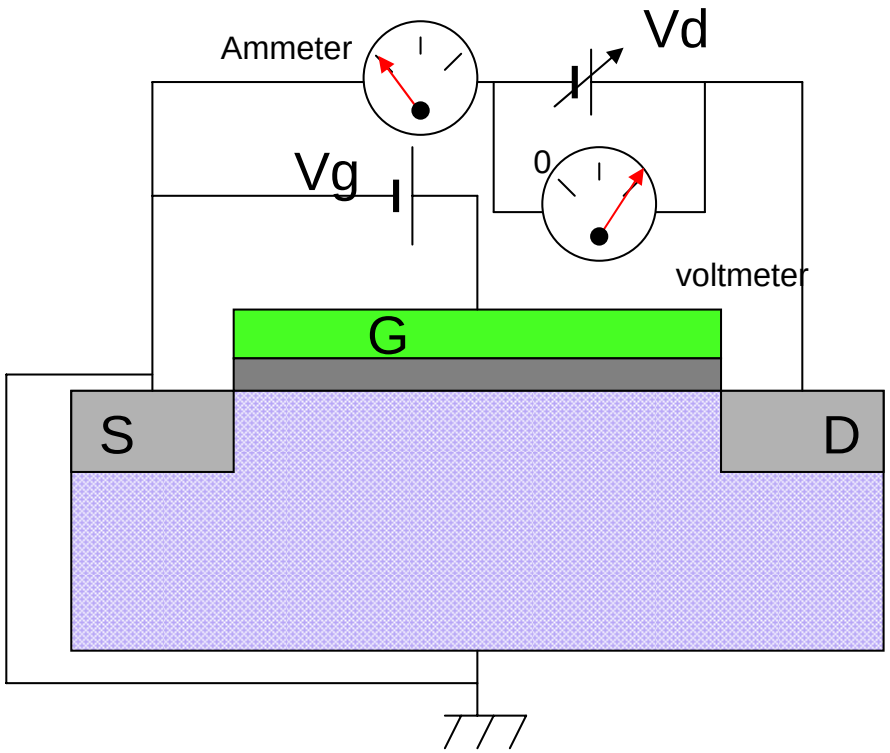


However the gate is biased high enough, carrier velocity saturates due to high drain field effect. It limits increase of drain current.

Operation of N-channel MOS(NMOS)FET

- Drain characteristics : Id-Vd characteristics

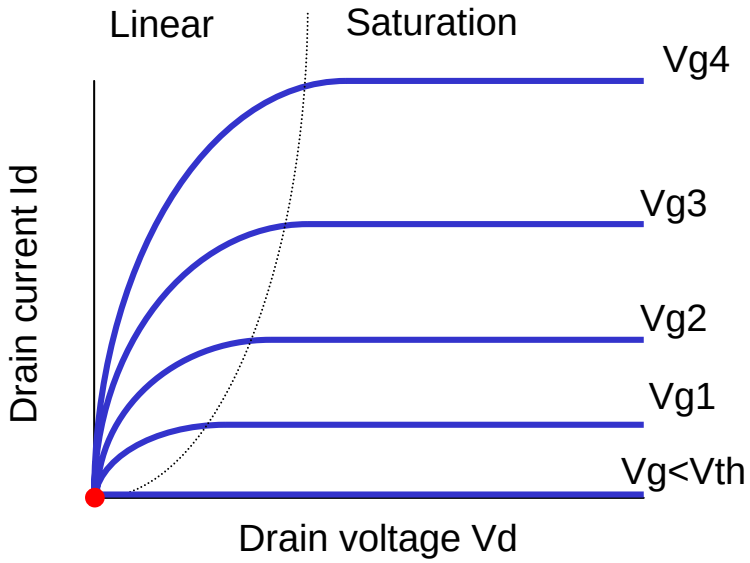


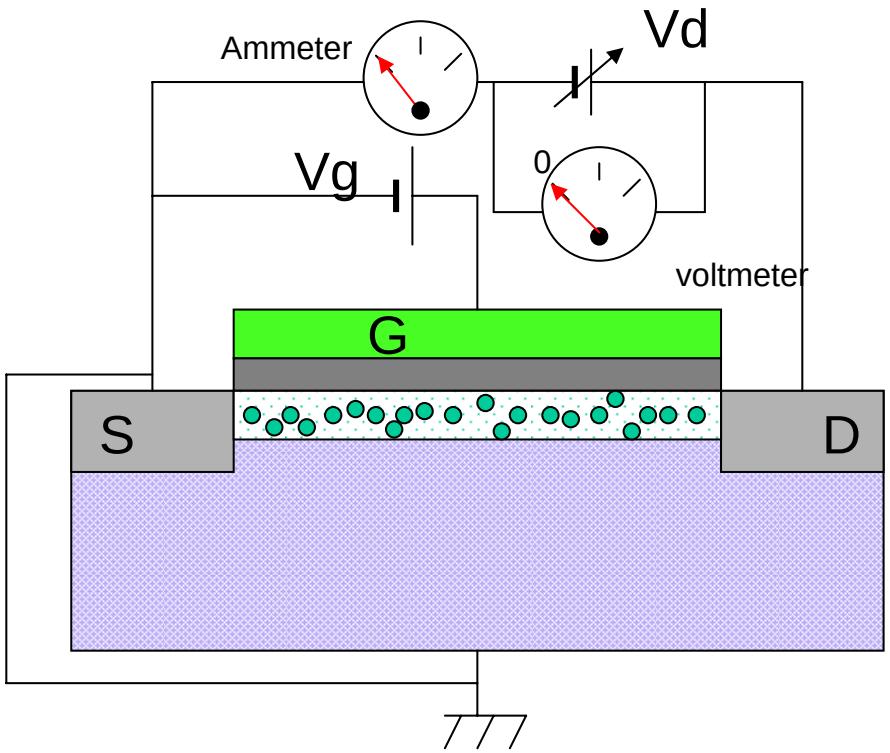


When Vgs=0<Vth, even if Vds>0, there is no current flows (except leakage).

Operation of N-channel MOS(NMOS)FET

- Drain characteristics: Vgs=Vg3, Vds=0

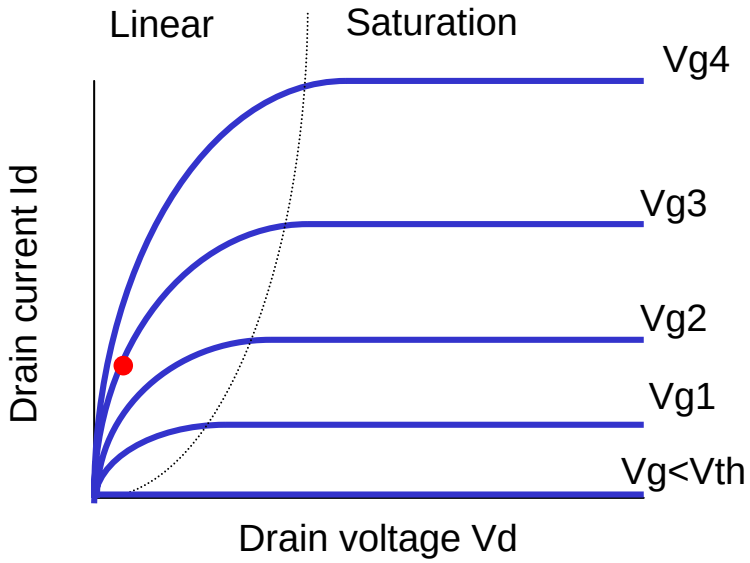


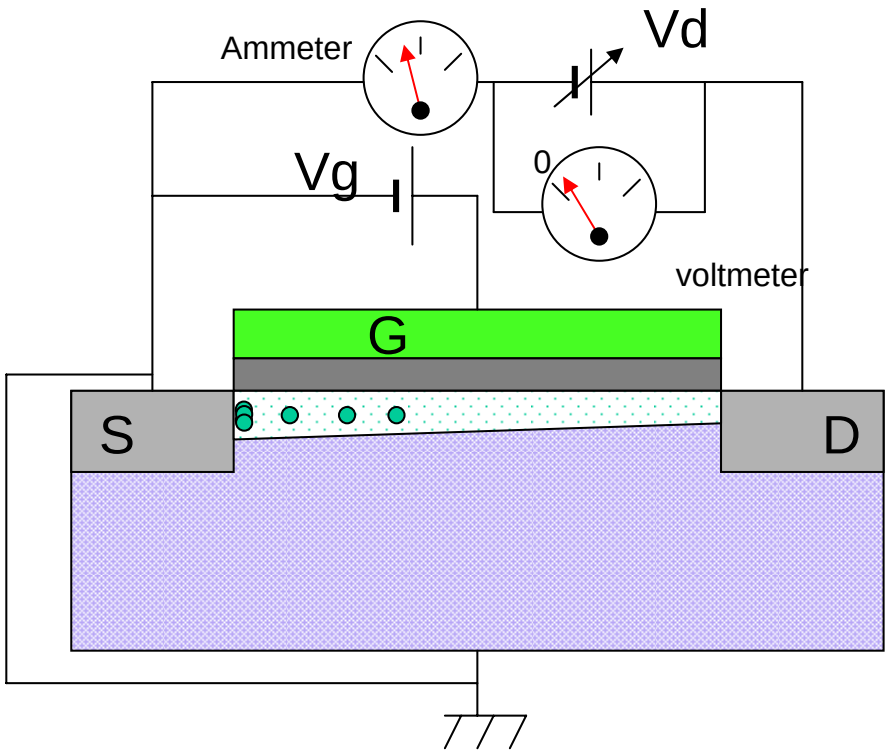


Apply Vg=Vg3 and see what happens, when you increase Vds.
Now, Vds=0V

Operation of N-channel MOS(NMOS)FET

- Drain characteristics: Vgs=Vg3, Vds≧0

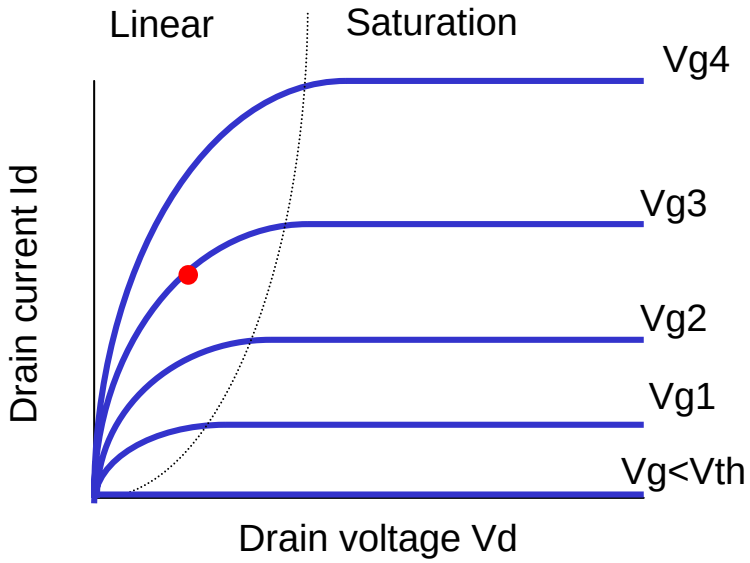


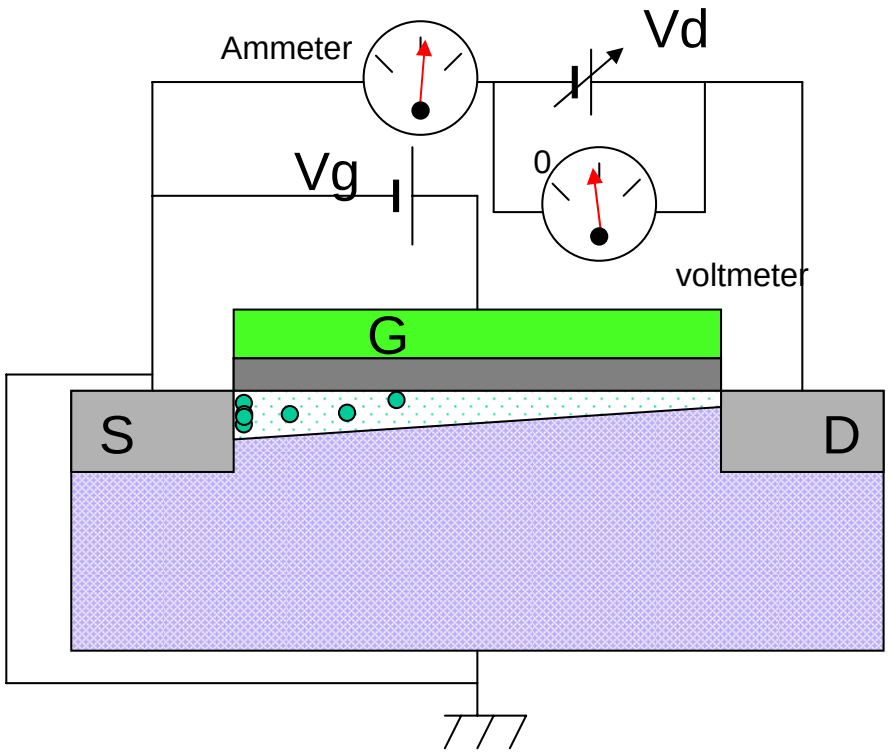


Apply small drain bias Vds!
You can get quick rise in drain current.
Thickness of channel looks same along source and drain

Operation of N-channel MOS(NMOS)FET

- Drain characteristics : Vgs=Vg3, Vds>>0

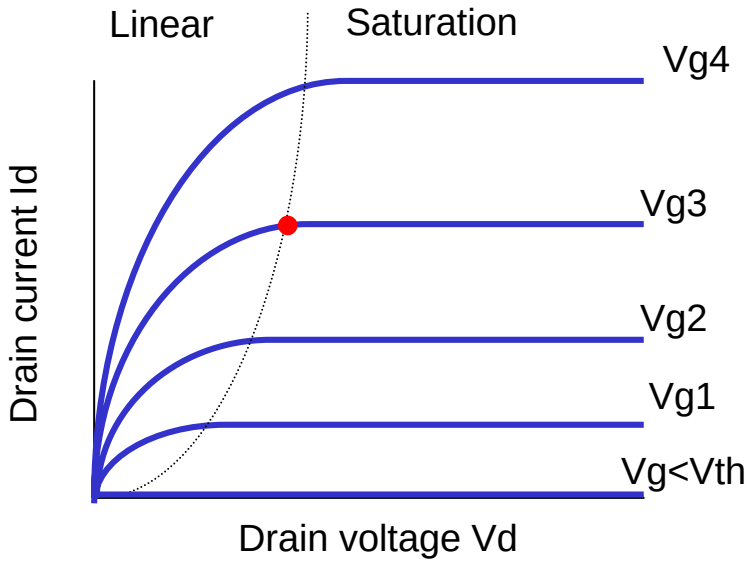


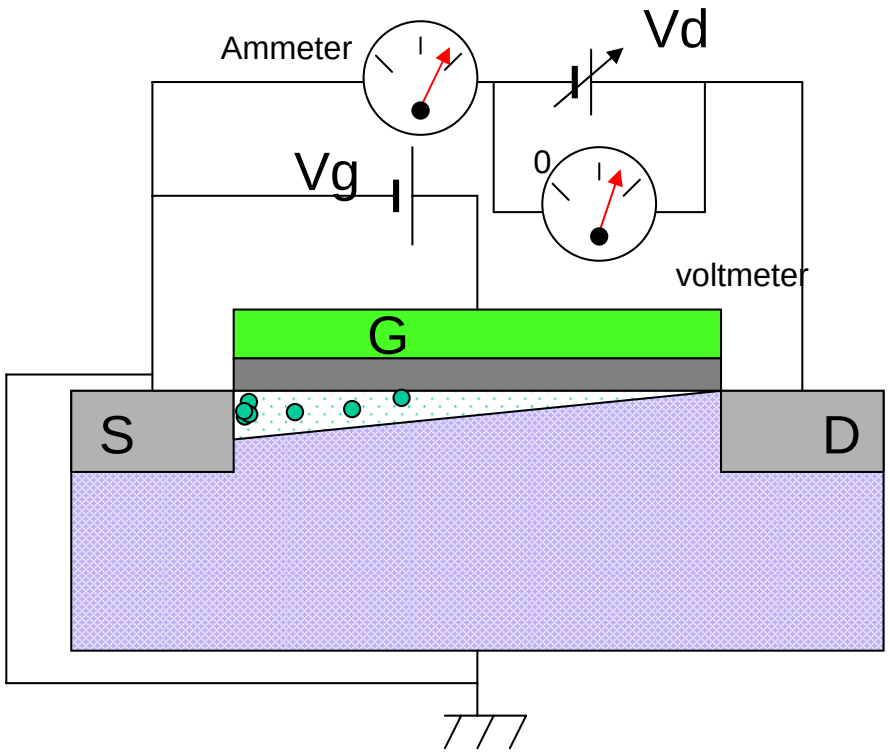


Furter increase of Vds! What happen in current and channel thickness?
Drain current has started to leveled-off!
Thickness of channel; channel thickness at drain edge become thinner!

Operation of N-channel MOS(NMOS)FET

- Drain characteristics : Vgs=Vg3, Vds=Vgs-Vth

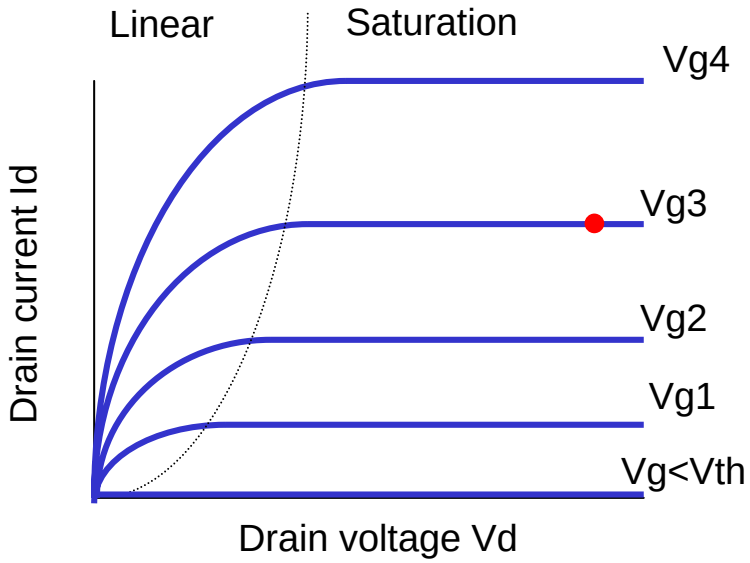


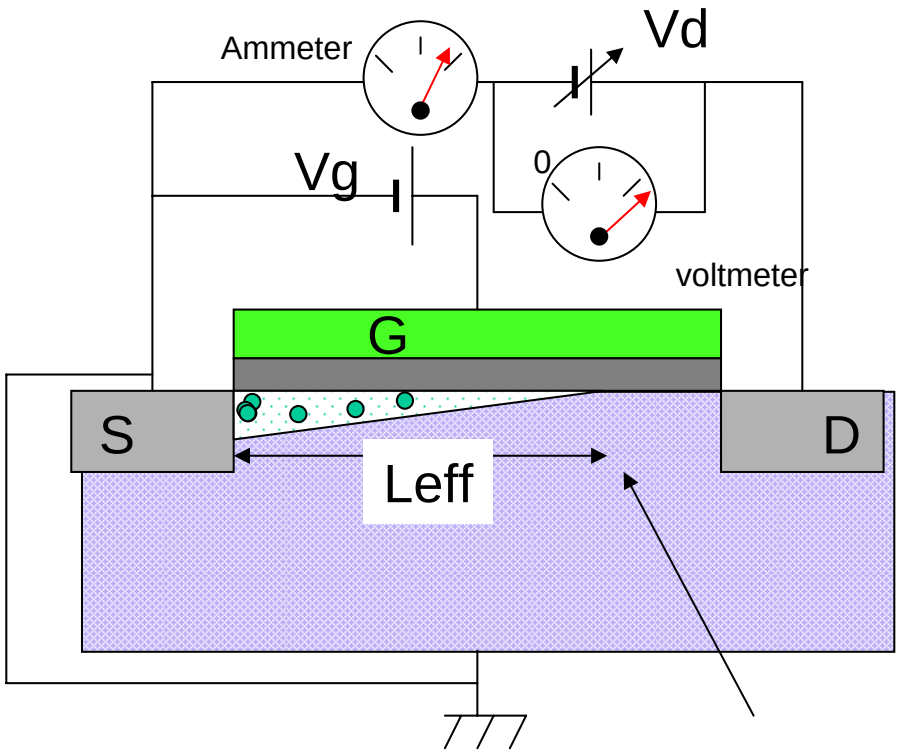


When Vds=Vgs-Vth, this situation is called “Pinch-off condition”!
Because drain current was saturated (drain conductance = 0), and the channel at drain-end has disappeared (its thickness = 0)!

Operation of N-channel MOS(NMOS)FET

- Drain characteristics : Vgs=Vg3, Vds>Vgs-Vth





After the pinch-off, the drain current becomes constant.
Electrons are swept-out from the pinched channel to Drain, and flow through the depletion region.

Summary of basic MOSFET & I-V Characters

MOSFET is ideal device for LSI:

- Small size
- Easy to isolate each others in highly integrated MOSFETs
- Capacitive input allows direct circuit connections
- Others:
  - Low power (CMOS)
  - Easy to shrink sizes (Scaling)
  - ….. Will be discussed later

MOSFET I-V Characteristics:

- Parabolic voltage dependency of Ids (to Vgs and Vds)
- Switching can be determined by “Vth”
- Current drivability is in proportion to “W/L” (geometry parameters)

Quiz

(1) What is the charged carrier in NMOS?

It flows from ( ) to ( ). Current flows from ( ) to ( ).

(2) What is the charged carrier in PMOS?

It flows from ( ) to ( ). Current flows from ( ) to ( ).

(3) When you design MOS Layout (determine L, W), How you can do to get double of drain current Ids?

(4) How you can control Vth of NMOS? If you want increase Vth by 0.1V, what is the best way to do in processing?

(5) How you can measure Vth?