

# INSTRUCTIONS FOR SSGEN ENHANCEMENT

MAR. 30, 2018  
DESIGN METHODOLOGY DEPARTMENT  
RENESAS ELECTRONICS CORPORATION

# INSTRUCTIONS

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- The followings should be done.
  - To improve feature of verification environments generation
  - To update SSGEN user guide
- Points to keep in mind
  - When you cannot handle the request or problem from HLD designers, please ask REL for support
  - When you ask REL for help, please explain what you have considered, and distinct the points you have resolved and that you could not resolve

# CONTENTS OF THIS ACTIVITY

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1. Improve feature of verification environments generation
2. Other enhancements
3. SSGEN implement
4. SSGEN test
5. Update SSGEN user guide

# CONTENTS OF THIS ACTIVITY

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## 1. Improve feature of verification environments generation

- Prepare a new command to change main\_\*.cpp generation way
  - Purpose: to keep user modification of sc\_main function
- Support “#include” and “cthread” in `ifdef TESTBENCH
  - Purpose: to make user modify TB easily
- Build cocotb-SystemC environment
  - Purpose: to introduce cocotb (HDL verification framework) for Unit Test quality improvement

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## 1. Improve feature of verification environments generation

- Prepare a new command to change main\_\*.cpp generation way (1/3)
  - Add new command **separate\_scmain\_file {on|off}**
    - **off** : default
      - ✓ Output main\_\*.cpp only as before
    - **on** : Output sc\_main descriptions into two files (main\_\*.hpp and main\_\*.cpp)
      - ✓ main\_\*.hpp
        - ✓ Output only following descriptions
          - Instantiations of DUT, TB and memory model
          - sc\_signal declarations
          - Signal connections
      - ✓ File overwrite rule is same as \*.h file (rename existed main\_\*.hpp to main\_\*.hpp.N)

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## 1. Improve feature of verification environments generation

- Prepare a new command to change main\_\*.cpp generation way (2/3)
  - Add new command **separate\_scmain\_file {on|off}**
    - **on** : Output sc\_main descriptions to two files (main\_\*.hpp and main\_\*.cpp) (Cont.)
      - ✓ main\_\*.cpp
      - ✓ Output other descriptions
      - ✓ Output #include main\_\*.hpp
      - ✓ File overwrite rule is same as \*.cpp file (Generate main\_\*.cpp\_tmp if main\_\*.cpp already exists)

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## 1. Improve feature of verification environments generation

- Prepare a new command to change main\_\*.cpp generation way (3/E)

### test.in

**separate\_scmain\_file on**

```
module test
clock clk
sreset rst pos
...
```

SSGEN

### main\_test.cpp

```
// main_test.cpp
#include "test.h"
#include "tb_test.h"

int sc_main(int argc, char *argv[]) {
    ...
    printf("clk: %d ns ...");

    #include "main_test.hpp"

    ssgen_trace_file *tf = NULL;
    ...
    return 0;
}
```

### main\_test.hpp

```
// main_test.hpp

test test0("test0");
tb_test tb_test0("tb_test0");

sc_signal < bool > rst;
sc_signal < bool > in0;
sc_signal < bool > out0;

test0.clk(clk);
...
test0.out0(out0);

tb_test0.clk(clk);
...
tb_test0.out0(out0);
```

Instantiations

sc\_signal  
declarations

Signal  
connections

# CONTENTS OF THIS ACTIVITY

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## 1. Improve feature of verification environments generation

- Support “#include” and “cthread” in `ifdef TESTBENCH (1/2)
  - **#include**
    - When “#include” is specified inside of `ifdef TESTBENCH, the “#include” description is generated in TB only.
  - **cthread**
    - When “cthread” is specified inside of `ifdef TESTBENCH, SC\_CTHREAD descriptions are generated in TB in addition to “thread\_main”



# CONTENTS OF THIS ACTIVITY

## 1. Improve feature of verification environments generation

- Support “#include” and “cthread” in `ifdef TESTBENCH (2/E)

### test.in

```
module test
clock clk
sreset rst pos

...

`ifdef TESTBENCH

#include “tb_lib.h”

cthread thread_sub

`endif
```

SSGEN

### tb\_test.h

```
#include <systemc.h>
#include "ssgenlib.h"
#include “tb_lib.h”

SC_MODULE(tb_test) {
    ...
    SC_CTOR(tb_test)
    {
        SC_CTHREAD(thread_main, clk.pos());

        SC_CTHREAD(thread_sub, clk.pos());
        reset_signal_is(rst, true);
    }
    ...
};
```

Generate in only TB

Output as before

Descriptions of additional  
cthread from user  
specification

### tb\_test.cpp

```
#include "tb_test.h"

void tb_test::thread_main() {
    ...
}

void tb_test::thread_sub() {
    wait();
    while(1) {
        // please write here!
        wait();
    }
}
```

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## 1. Improve feature of verification environments generation

- Build cocotb-SystemC environment (1/6)

- cocotb: Coroutine Co-simulation Test Bench

- <https://github.com/potentialventures/cocotb>

- <http://cocotb.readthedocs.io/en/latest/introduction.html#what-is-cocotb>

- ✓ Cocotb is a COroutine based COsimulation TestBench environment for verifying VHDL/Verilog RTL using Python.
    - ✓ Cocotb is completely free, open source (under the BSD License) and hosted on GitHub.
    - ✓ Cocotb requires a simulator to simulate the RTL.

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## 1. Improve feature of verification environments generation

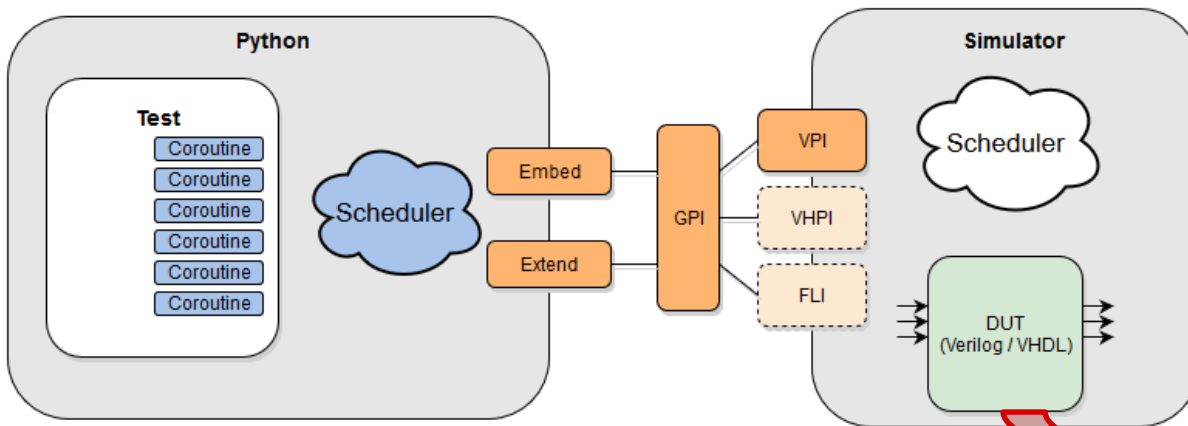
- Build cocotb-SystemC environment (2/6)
  - Motivation of cocotb introduction
    - Encourage to do Unit Test in smaller unit, and improve efficiency and quality of Unit Test
      - Run test concurrently with SystemC coding
    - Conventional checklist-based Unit Test and TOP verification remain even if cocotb is introduced

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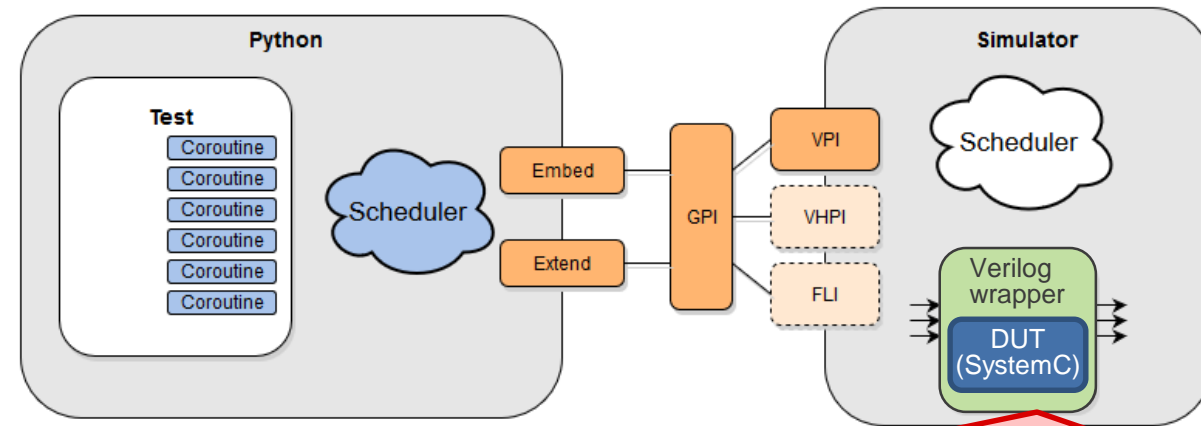
## 1. Improve feature of verification environments generation

- Build cocotb-SystemC environment (3/6)
  - cocotb-SystemC environment

### HDL



### SystemC



- Prepare Verilog wrapper module for top module of SystemC DUT
- Compile Verilog wrapper file and SystemC files by VCS/IES Co-simulation feature

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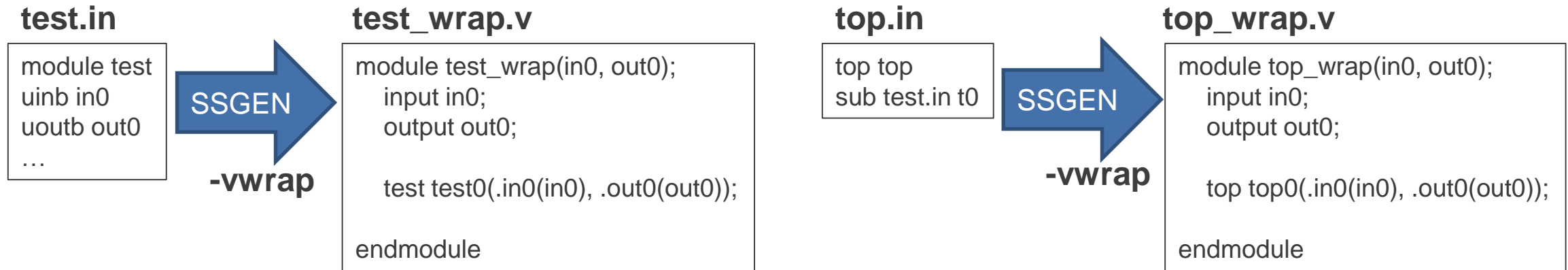
## 1. Improve feature of verification environments generation

- Build cocotb-SystemC environment (4/6)
  - Add new command line option **-vwrap**
  - When **-vwrap** is specified, SSGEN outputs Verilog wrapper module file.
    - File name: xxx\_wrap.v (“module test”->test\_wrap.v, “top top”->top\_wrap.v)
    - Module name: xxx\_wrap (“module test”->test\_wrap, “top top”->top\_wrap)
    - Verilog wrapper module has same input and output ports with SystemC module
    - Verilog wrapper module instantiates SystemC module

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## 1. Improve feature of verification environments generation

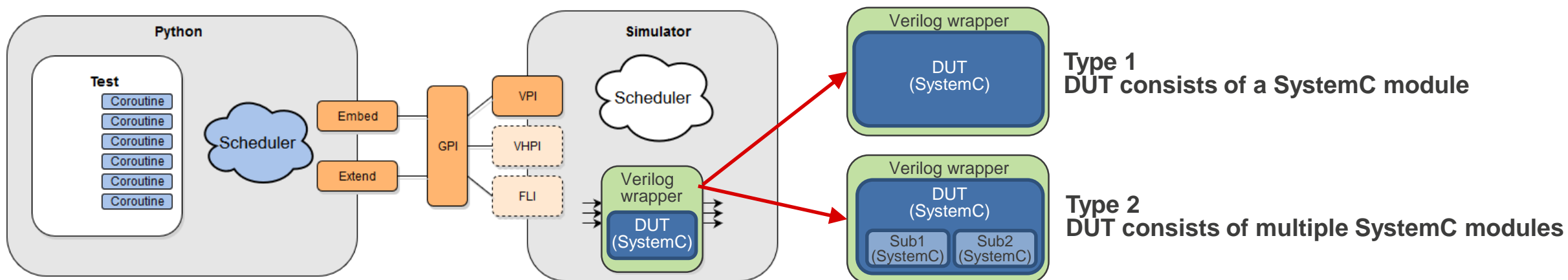
- Build cocotb-SystemC environment (5/6)
  - Add new command line option **-vwrap** (Cont.)



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## 1. Improve feature of verification environments generation

- Build cocotb-SystemC environment (6/E)
  - Modify Makefile of cocotb to compile Verilog wrapper module file and SystemC files
  - VCS: cocotb-master/makefiles/simulators/Makefile.vcs
  - IES: cocotb-master/makefiles/simulators/Makefile.ius
  - With two types of SystemC DUT, confirm compile and simulation on cocotb with your Makefile.



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## 2. Other enhancements

- Delete W003 message
  - It became unnecessary message in according with current CtoS usage.
- Prepare command-line option to not stop SSGEN due to ERROR.
  - One user wants SSGEN to report all of ERROR for .in file at a time as much as possible.
  - In default, SSGEN stops immediately due to ERROR.
  - When new command-line option is specified, SSGEN does not stop due to ERROR.



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## 3. SSGEN implement

- Implement SSGEN in according with Step1.

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## 4. SSGEN test

- Make checklist about verification environments generation improvements
- Make test data
- Import test data that you created in 2018Q1 to regression environment
- Test SSGEN

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## 5. Update SSGEN user guide

- Update “ssgen\_user\_manual\_En.doc”
  - Add enhancement information of this term.

# DELIVERABLE

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- Specification document, SSGEN script, SSGEN checklist and SSGEN user guide
  - **specification document:** specification for enhancements (Step1)
  - **SSGEN:** Perl script (Step3)
  - **SSGEN checklist:** checklist for enhancements (Step4)
  - **SSGEN user guide:** SSGEN user guide (Step5)

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