Document No.: D-SLD-CMN-00XX-01

# User manual

# Erakis enhancement

(V1.1)


Summary:

This document describes the User Manual of Erakis enhancement phase 1


Relative Document

| Reference Manuals | | | | |
|---|---|---|---|---|
| **No.** | **Title name** | **Document number** | **Description** | **Path** |
| 1 | REQ-SLD-14015_Erakis-Enhancement.pptx | REQ-SLD-14015 (Rev 1.1) | Requirement specifications of Erakis enhancement phase 1 | Documents/010_ENG/140_FrontEnd/Project/01_SLD/2_SLD_Project/Model_Documents/01_Project_Document_Management/REQ/2014 |

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# 1.Introduction

## 1.1.Overview

(1) Erakis is a verification environment generator tool for equivalence verification between Analog circuit and functional model. Figure 1.1 below describes input/output files of the Erakis tool.

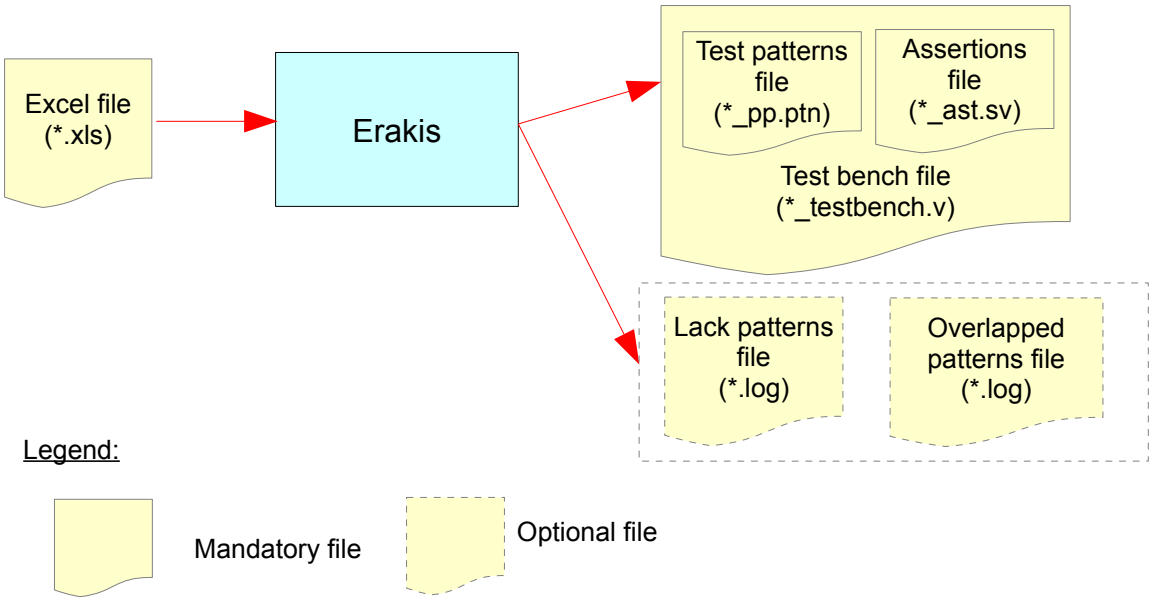


*Figure 1.1: Input/output file of Erakis tool*

(2) Input of the Erakis tool is an Excel file. This file includes the information about

(2.1) The general information about Analog circuit: cell name, delay time, output directory, name of test bench file, assertion file, test vector file *(the word phrase "test pattern" is same meaning with "test vector")*, lack log file *(if any)*, …

Refer to chapter Erakis info sheet for more information.

(2.2) The information of ports using in users design.

Refer to chapter Port info sheet for how to create input information for port.

(2.3) The truth table and sub-tables

Refer to chapter Table0 sheet, referent table sheet for how to create input information for truth table.

(2.4) The FSM *(Finite State Machine)* table and its related tables *(in case Analog design contains an internal FSM)*.

Refer to chapter FSM0 sheet, State definition sheet, Event definition sheet, State transition sheet, Output definition sheet for how to create input information for FSM table.

(3) Outputs of the Erakis are below. The outputs of the Erakis tool depends on the input options. These options are passed to the Erakis tool by users. Refer to chapter Options of Erakis for more detail.

(3.1) The test bench file instantiates the DUV, provides inputs and checks outputs . This file includes the test vector file of truth table, the assertion file of truth table, the test vector file of FSM, and the assertion of FSM.

(3.2) The test vector file of truth table and the test vector file of FSM.

(3.3) The assertion file of truth table and the assertion file of FSM.

(3.4) Lack log file if the truth table lacks test patterns.

(3.5) Overlapped pattern file if there are overlapped patterns in the truth table.

(3.6) Execution file to run.

## 1.2.Supported features

(1) Table 1.1 lists all features which has been already supported.

*Table 1.1: List of supported functions of the Erakis tool*

| Feature | | Description | Supported in Version |
|---|---|---|---|
| GENERAL | Make test bench | Make test bench for both truth table and FSM | v1.5 |
| | Make script of execution simulation | Make scripts of execution simulation (VCS/irun) | v1.5 |
| | Support inout port | Support inout ports | v2.0 |
| | Select output wave format | Execution VCS/irun: nowave (default)/VPD/FSDB. Execution irun(circuit): nowave/PSF(default). | v1.5 |
| | Save simulation log | As for the file name, users are impossible of designation (vcslog.erks/irunlog.erks). | v1.5 |
| | Input Excel (*.xls) file | Erakis reads input file as Excel format. | v1.5 |
| TRUTH TABLE | Overlap check truth table | Check the truth table has no overlap item. | v1.5 |
| | Lack check truth table | Check the truth table has no lack item. | v1.5 |
| | Make test vector | Make test vector to check truth table | v1.5 |
| | Make assertion | Make assertion for truth table | v1.5 |
| | Support using variable in truth table | Support using variable in truth table | v2.0 |
| | Support using referent table in truth table | Support using referent table in truth table output definition table | v1.5 |
| | Control completeness checking | If there is any lack pattern in truth table, Erakis considers value of output ports of this pattern is "X" | v2.0 |
| | Allow "*" (don't care) in output log file | Erakis mergers the lack patterns. | v2.0 |
| FSM | Check validity | Check validity of FSM tables. Refer to table 3.13 Summary constraints in FSM. | v2.0 |
| | Make test vector | Make test vector to check FSM | v2.0 |
| | Make assertion | Make assertion to verify FSM | v2.0 |

# 2.Getting Started

## 2.1.Erakis File

(1) Table 2.1 lists all files of Erakis design version v2.0.

*Table 2.1: All files of the Erakis design*

| No. | File name | Description |
|---|---|---|
| 1 | erks | Main script file to run Erakis. This file invokes the top.pl file to execute functions of Erakis. |
| 2 | top.pl | Main Perl file. This file includes ErksFunc.pl, Ex2Tbl.pl, MakeOutFile.pl file. It invokes functions of other Perl file to process input option, input Excel file, and generate the output files. |
| 3 | ErksFunc.pl | This file defines functions to check the input options. |
| 4 | Ex2Tbl.pl | This file defines functions to make table of data from the input Excel file. |
| 5 | MakeOutFile.pl | This file defines functions to create output files. |
| 6 | L2F.vams | This file is included in test bench if DUV has oscillation ports. The module in this file changes from oscillation to frequency. And, this is used in simulation. |
| 7 | solveBCP | Execution file to check the lack patterns in a truth table. |
| 8 | solveSTP | Execution file to generate the combination path which cover all state in State Transition Table. |
| 9 | run_fsm | This script invokes solveSTP to generate the combination path. |

(2) Figure 2.1 below shows the files structure.

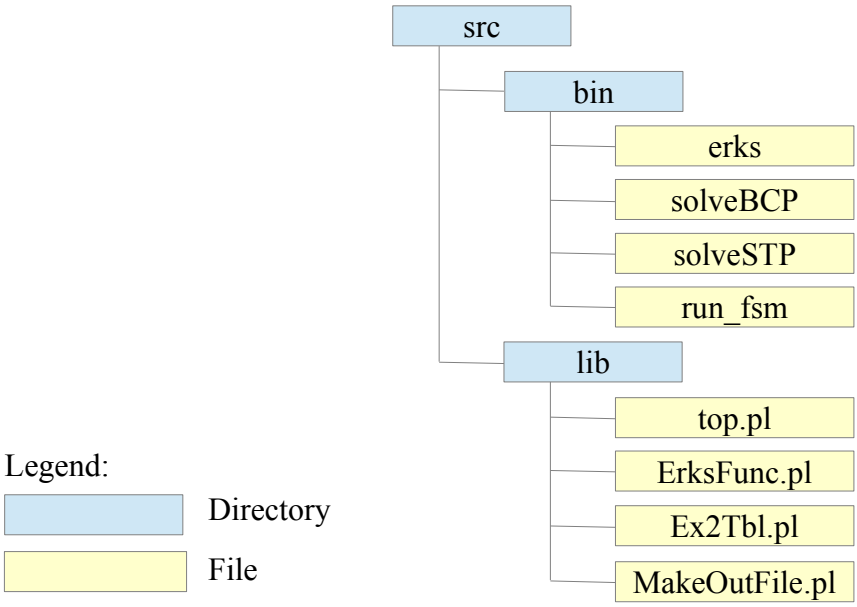


*Figure 2.1: Files structure of the Erakis tool*

### 2.2.System requirement

(1) Table 2.2 lists the required tools/softwares needed to run Erakis. They are required to install before starting the Erakis.

*Table 2.2: Necessary tools/softwares for running Erakis*

| Software/Module | Version |
|---|---|
| OS | Linux Red Hat 5.0 |
| Perl | 5.8.8 |
| CPAN (Spreadsheet::ParseExcel) | 0.65 |
| Sugar | 2.1.3 |
| Minisat | 2.0 |

### 2.3.Setting environment variable

(1) Following environment variables are required to set. They are described in table table 2.3.

*Table 2.3: Necessary tools/sofwares for running Erakis*

| No. | Variable name | Description | Example |
|---|---|---|---|
| 1 | ERAKIS_PATH | Stored Erakis directory | `pwd` |
| 2 | ERAKIS_LIB | Earkis's library directory | ${ERAKIS_LIB}/lib |
| 3 | ERAKIS | Erakis's execution file directory | ${ERAKIS_LIB}/bin |
| 4 | ERAKIS_VER | Erakis version | Erakis V02.00.00 20150317 |

(2) Note: The “ERAKIS_VER” variable is used in generating output file. Detail, the header of each output file includes information about Erakis version. Do not change the ERAKIS_VER many times. Its value is required to keep as same as the released version.

## 3.How to create input Excel file

(1) The table 3.1 below lists all sheets in an input Excel file. This table also describes the attribute of each sheet.

*Table 3.1: List all sheets in input Excel file*

| Sheet name | Description | Mandatory/Optional |
|---|---|---|
| Erakis info | Describe general information about the cell name, output file name, delay time, …for Erakis generating output. | Mandatory |
| Port info | Describe all information of port: the port name, port width, clock period, care range, digital or analog. | Mandatory |
| Table0 | The truth table is described here | Optional (*) |
| Exclude | Indicate the input prohibition | Optional |
| Variable | Declare all variable and its expression. | Optional |
| Reference | The referent table for truth table or output definition table | Optional |
| FSM0 | Describe the FSM name. Indicate the sheet name of state transition table, output definition, state definition, event definition. | Optional (*) |

(2) **Note:** (*) The input Excel file is required to contain at least Table0 sheet or FSM0 sheet. If not, the Erakis dumps an error message.

### 3.1.“Erakis info” sheet

(1) The name of sheet is required to be “Erakis info” correctly. This is a mandatory sheet in an input Excel file.

(2) This sheet contains the general information for generating output file such as file name, the path to some tools, library,...

(3) Each information is defined in a tag. The order of tags in this sheet is optional.

(4) Table 3.2 lists all supported tags in Erakis info sheet. Based on the demands, users define necessary tasks, and ignore others.

*Table 3.2: List tag name in “Erakis info” sheet*

| Tag name | Description | Default value |
| --- | --- | --- |
| cell | The cell name. This name is used in naming output files. | name of input Excel file |
| max_delay | The delay is used in test vector file of truth table. This is the delay time to change input's value. | 20 |
| out_dir | Indicate a relative path to the output directory. The Erakis will make a directory. Its name is specified in out_dir tag by users. | “out_dir” directory. (Erakis make directory named “out_dir” in running location) |
| ptn_file | Indicate the name of test vector file of truth table | ptn_<cell_name>.ptn |
| tb_file | Indicate the name of test bench file. | testbench_<cell_name>.v |
| ast_file | Indicate the name of assertion file of truth table | ast_<cell_name>.sv |
| overlap_log | Indicate the name of overlapped log file | overlap_<cell_name>.log |
| lack_log | Indicate the name of lack log file | lack_<cell_name>.log |
| pref_unit | Indicate the unit of clock frequency used in generating test bench. | MHz |
| exclude_in | Indicate the name of assertion file checking input prohibition. | ex_ast_<cell_name>.sv |
| lib_name | Indicate the library name used in generating script for irun with circuit. | None |
| virtuoso | Indicate the path to virtuoso used in generating script for irun with circuit. | None |
| ConnectRule | Indicate the AMS connect rule used in generating script for irun with circuit. | None |
| view_name | Indicate the cell's name which users want to view net list. This tag's value is used in generating script for irun with circuit. | None |
| cds.lib | Indicate the path to library of CDS used in generating script for irun with circuit. | None |
| Incisive | Indicate the path to irun used in generating script for irun with circuit, and generating shell script for Incisive | None |
| VCS | Indicate the path to VCS used in generating shell script for VCS | None |

| | | |
|---|---|---|
| Verdi | Indicate the path to Verdi used in generating shell script for VCS | None |
| verilog | Indicate the verilog module used in generating shell script for Incisive, and generating shell script for VCS | None |

(5) Table 3.3 shows an example of Erakis info sheet.

*Table 3.3: An example about "Erakis info" sheet*

| tag | default | const |
|---|---|---|
| cell | - | test |
| max_delay | 20 | 100 |
| out_dir | out_dir | test |
| ptn_file | ptn_test.ptn | aaa |
| tb_file | testbench_test.v | 4_1_8_testbench.v |
| ast_file | ast_test.sv | 4_1_8_ast.sv |
| overlap_log | overlap_test.log | 4_1_8_ov.log |
| lack_log | lack_test.log | 4_1_8_lk.log |
| pref_unit | MHz | Hz |
| exclude_in | ex_ast_test.sv | |
| lib_name | - | lib |
| virtuoso | - | /aaa/bbb/ccc/virtuoso |
| ConnectRule | - | rule |
| view_name | - | top |
| cds.lib | - | /aaa/bbb/ccc/cds.lib |
| Incisive | - | / common/appl/dotfiles/cadence.CSHRC_ius13.20s007 |
| VCS | - | /common/appl/Env/Synopsys/vcs-mx_vD-2009.12-4 |
| Verdi | - | /common/appl/dotfiles/verdi3.CSHRC_2014.03-sp1 |
| verilog | - | /aa/bb/cc/verilog_top.v |
| | | /aa/bb/cc/verilog_top2.v |

(5.1) "default" column: the value in this column is got if the tag is one in followings: lib_name, virtuoso, ConnectRule, view_name, cds.lib, Incisive, VCS, Verdi, verilog. With the remain tags, if the "const" column is empty, the value in "default" column is not got. Its default value is described in table 3.2.

(5.2) Users can indicate many verilog files by writing them into many cells in "const" column, from the first line of verilog. Refer to table 3.3 above for an example.

(6) Users can use option to drive output of Erakis. However, with some options, the Erakis tool need information defined in tags to generating output file. If lack these information, the Erakis dumps an error message and exit.

Table 3.4 below shows the constraints between options and tags.

*Table 3.4: Harmonization between options and tags in “Erakis info” sheet*

| Option | Mandatory tags |
|---|---|
| -vcs | VCS, verilog |
| -vcs -fsdb | VCS, verilog, Verdi |
| -irun \| -incisive | Incisive, verilog |
| -ams -irun | view_name, lib_name, cds.lib, Incisive, virtuoso, ConnectRule |

### 3.2.“Port info” sheet

(1) The name of sheet is required to be “Port info” correctly. This is a mandatory sheet in an input Excel file to declare ports of DUV *(Design Under Verify)*.

(2) Table 3.5 lists all kind of information related to a port.

*Table 3.5: An example about “Erakis info” sheet*

| Column name | Description | Mandatory/Optional |
|---|---|---|
| port | The port name.<br>“pin”, “name” are alternative. No case sensitive. | Mandatory |
| I/O | Indicate the kind of port. Its value can be: “input”, “output”, “inout”, “IO”, “I/O”, “Power”, “Supply”, “Ground”.<br>“input”, “output”, “inout” are not case sensitive. | Mandatory |
| D/A | Indicate the port is digital port or analog port. Its value can be: “A”, “D”, “Analog”, “Digital”.<br>Default is none *(Error if undefined)*. | Optional |
| SA | Indicate the signal amplitude. | Mandatory |
| bit | Indicate the bit width of port. Default is 1. | Optional |
| care range | Indicate the care range of port. This information is used in generating test vector.<br>Default follows D/A column (A: “z”, D: “x”).<br>“-” means that port cares 0/1.<br>“x” means that port cares 0/1/x.<br>“z” means that port cares 0/1/x/z.<br><br>Oscillation's care range:<br>Valid format: +- {val0}% or +{val1}% - {val2}% or {val3}%<br>Example:<br>+-10%, +13%-5%, 10% | Optional |
| clk period | Indicate the period of clock. This information is used in generating clock source in test bench.<br>Recommend to specify value of this column in case clock port.<br>Default is 100. | Optional |

(3) Table 3.6 shows an example about Port info sheet.

*Table 3.6: An example about “Port info” sheet*

| Pin name | I/O | SA | care range | D/A | clk period |
|---|---|---|---|---|---|
| VDD | power | 1.8 | - | D | |
| VSS | power | 0V | - | D | |
| INA | input | AVDD | - | A | |

| | | | | | |
|---|---|---|---|---|---|
| INB | input | VDD | - | D | |
| OUT | output | VDD | +-5% | D | |
| EN | input | VDD | - | | |
| AAA | power | AVDD | - | A | |
| AVDD | power | 5V | - | A | |
| AVSS | supply | 0 | - | A | |
| clk | input | VDD | - | D | 200 |

### 3.3.“Table0” sheet

(1) The name of sheet is required to be “Table0” correctly. This is an optional sheet in an input Excel file. But if any one of following options: *-tc | -check*, *-ta | -assertion*, *-tv | -ptn* is used, this sheet is required in the input Excel file. If not, the Erakis tool dumps an error message and exits.

(2) This sheet contains the information of truth table, the power supply, and some additional information related to checking. The test vector file, the assertion file are generated from information of this sheet if the corresponding options *(-tv, -ta)* are specified.

(3) Table 3.7 below is an example of “Table0” sheet.

*Table 3.7: An example about “Table0” sheet*

| pcheck | supply | | input | | | output | |
|---|---|---|---|---|---|---|---|
| | VDD | VSS | INA | INB | EN | OUT | AAA |
| | 0 | * | * | * | * | x | x |
| | x | * | 1 | * | * | x | x |
| | z | * | 1 | * | * | x | x |
| 1 | 1 | 1 | 1 | * | * | x | x |
| | 1 | x | 1 | * | * | x | x |
| | 1 | z | 1 | * | * | x | x |
| 1 | 1 | 0 | * | * | 0 | [var1] | vdd |
| 1 | 1 | 0 | 1 | 1 | 1 | <full> | 0 |
| | 1 | 0 | * | * | x | [varE] | vdd |

(4) Explanation:

(4.1) **pcheck:** this column indicates which test vector is generated in test vector file if “-pcheck” option is used.

(4.2) **[var1]:** In this example, the *[var1]* is a variable. To indicate cell's content is a variable, the cell's content is required to be in [] character. Expression of a variable is defined in “Variable” sheet. Its expression will be replaced to this cell, and be calculated to a certain value.

(4.3) **<full>:** In this example, the *<full>* is a referent table. To indicate cell's content is a referent table, a cell's content is required to be covered in <> character. The line contains a referent table will be replaced by another lines which defined in referent

sheet. In detail, come back this example, the line 2nd from the bottom will be replaced by lines in “full” sheet.

(4.4) **Other notes**: For a 2 bit width port, if users write value “x”, the Erakis understands it as “2'b0x”. So, if users want to specify value “x” for both 2 bits, “xx” value is recommended.

### 3.4.“Exclude” sheet

(1) The name of sheet is required to be “Exclude” correctly. This is an optional sheet in an input Excel file. But if the *-ex_ast* option is used, the input Excel file is required to contain this sheet. If not, the Erakis tool dumps an error message and exits.

(2) This sheet contains the information of prohibited input vector. The assertion file to check the input prohibition is generated if -ex_ast option is specified.

(3) Table 3.8 below is an example about “Exclude” sheet.

*Table 3.8: An example about “Exclude” sheet*

| supply | supply | Input | | |
|---|---|---|---|---|
| VDD | GND | EN | DATA_A | DATA_B |
| vdd | vss | 0 | 1 | * |
| vdd | vss | 0 | * | * |

(4) The “Exclude” sheet is same with “Table0” sheet, except below:

(4.1) “pcheck” column is for Table0 only. Because “Exclude” sheet is not used to generate test vector.

(4.2) The value of “output” port is no meaning. Its value can be empty if it is the last column in “Exclude” sheet.

### 3.5.“Variable” sheet

(1) The name of sheet is required to be “Variable” correctly. This is an optional sheet in an input Excel file. But if there is any variable is used in “Table0” sheet, the input Excel fileis required to contain “Variable” sheet. If not, the Erakis tool dumps an error message and exits.

(2) This sheet contains the information of variable and its expression.

In truth table *(Table0 sheet or referent sheet)*, the variable is replaced by its expression. Table 3.9 below shows an example about variable “var1” for truth table (table 3.7 above).

*Table 3.9: An example about “Variable” sheet*

| variable | Expression |
|---|---|
| var1 | (INA==1)?0:1 |
| var2 | (INA>EN)?0:1 |
| var3 | (EN>=1)?0:1 |
| var4 | (BBB<=1)?0:1 |
| var5 | (INA<1)?0:1 |
| var6 | ~EN |

| | |
|---|---|
| var7 | INA&EN |
| var8 | EN\|1 |
| var9 | INA^EN |
| var10 | INA+1 |
| var11 | INA-1 |
| var12 | INA*EN |
| var13 | INA/EN |
| var14 | (BBB<1)?0:1 |
| var15 | INA+2 |

(3) Notes:

(3.1) The name of variable column may be “variable” or “var” *(case in-sensitive)*.

(3.1.1) The variable declared in variable column might not referred at any place in Table0 sheet or referent sheet.

Example: In table 3.9, “var2”, “var3”, … are declared in variable column but might not be referred in any place.

(3.1.2) The variable used in Table0 sheet or referent sheet is required to be included in this variable column. If not, the Erakis dumps an error message and exits.

Example: In table 3.7, “varE” variable is not declared in variable column. An error message will be dumped for this case.

(3.2) The name of expression column may be “expression” or “expr” *(case in-sensitive)*. The expression is required to be valid. If users put an invalid expression, the Erakis will not dump warning message. Users care this issue by themselves.

(3.3) If expression refers to a “x” or “z” value. The value of expression will be assign to “x”.

(3.4) The variable column is required to be placed before expression column.

(3.5) No duplicated variable column or expression column.

(3.6) If “#” (comment character) appears at any position in a row, that row is ignored.

### 3.6.Referent sheet

(1) The name of sheet is required to be same with one was used in other sheet. Example, with table 3.7 above, name of referent sheet is required to be “full”, correctly.

(2) Referent sheet is a sheet used as a referent for a cell or a row in input Excel file. It is used in a truth table, an output definition table of FSM or in another referent table of truth table.

(3) This sheet might not be referred by any other sheet. But if there is any sheet being referred in other sheet(s), the input Excel file is required to contain corresponding referent sheet. If not, the Erakis tool dumps an error message and exits.

(4) Notes:

(4.1) In truth table, the referent sheet can nest many times.

(4.2) In output definition table of FSM, not nest in referent sheet is required.

(5) Table 3.10 shows an example about referent sheet of truth table (table 3.7 above).

*Table 3.10: An example about referent sheet of truth table*

| pcheck | input | | output |
|---|---|---|---|
| | INA | INB | OUT |
| 1 | 0 | 0 | 1 |
| | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| | 1 | 1 | 1 |
| | x | * | x |
| 1 | 0 | x | 0 |
| | 1 | x | 0 |

### 3.7.“FSM0” sheet

(1) The name of sheet is required to be “FSM0” correctly. This is an optional sheet in an input Excel file. But if any one of following options: *-fsmc*, *-fsmast*, *-fsmtv* is used, the input Excel file is required to contain this sheet. If not, the Erakis tool dumps an error message and exits.

(2) This sheet contains the information of the FSM names included in DUV, the sheet names of state definition tables, the sheet names of event definition tables, the sheet names of state transition tables, the sheet names of output definition tables, clock source of each FSM, the reset signal of each FSM.

(3) If a “#” is added at the beginning of a row, the row is ignored. See table 3.12 for an example.

(4) There are 7 mandatory columns which is required to exist in FSM0 sheet. Their attributes are described in table 3.11 below.

*Table 3.11: List of columns in FSM0 sheet*

| No. | Column name | Description |
|---|---|---|
| 1 | FSM | The FSM name. This name is used as name of FSM module in DUV.<br>Filling FSM's name in this column the name as same as one used in DUV is required, so that compilation on VCS has not error. |
| 2 | EVENT | The sheet name of event definition table.<br>If the value of this column is “-”, default name is “<cell_name>_EVENT”. |
| 3 | STAT_TRAN | The sheet name of state transition table.<br>If the value of this column is “-”, default name is “<cell_name>_TRAN”. |
| 4 | STAT_DEF | The sheet name of state definition table.<br>If the value of this column is “-”, default name is “<cell_name>_STAT”. |
| 5 | OUT | The sheet name of output definition table.<br>If the value of this column is “-”, default name is “<cell_name>_OUT”. |
| 6 | CLK | The name of clock source used in FSM. Declare this clock's period in Port info sheet is recommended. |
| 7 | RESET | The name of reset port used in FSM. Declare this reset port in Port info sheet is recommended.<br>The Erakis tool always considers that reset signal is active LOW. |

*Table 3.12: Example about FSM0 sheet*

| | No | FSM | EVENT | STAT_TRAN | STAT_DEF | OUT | CLK | RESET |
|---|---|---|---|---|---|---|---|---|
| | 1 | test_FSM | - | - | - | - | clk | rst_n |
| # | 2 | dummy | tmp_EVENT | tmp_TRAN | tmp_DEF | tmp_OUT | clk | rst_n |
| | 3 | FSM2 | subFSM_EVT | subFSM_STT | subFSM_DEF | subFSM_OUT | clk | rst_n |

(5) Table 3.13 summarizes the constraints in sheets related to FSM. The details are described in each chapter: state transition, event definition, state definition, output definition.

*Table 3.13: Summary constraints in FSM*

| No. | Item | Severity | State transition | Event definition | State definition | Output definition |
|---|---|---|---|---|---|---|
| 1 | Blank cell | Error | v | v | v | v |
| 2 | State not transition from other | Warning | v | - | - | - |
| 3 | State not transition to other | Warning | v | - | - | - |
| 4 | Transition state not defined in state definition | Error | v | - | - | - |
| 5 | Transition to source state | Warning | v | - | - | - |
| 6 | No initial state | Error | v | - | - | - |
| 7 | Duplicated event name | Error | - | v | - | - |
| 8 | Duplicated combination of event signal | Error | - | v | - | - |
| 9 | Duplicated state name | Error | - | - | v | - |
| 10 | Duplicated combination of state signal | Error | - | - | v | - |
| 11 | Table of reference | Error | - | - | - | v |
| 12 | Event name matching between state transition and event definition | Error | v | v | - | - |
| 13 | Event name matching between state transition and state definition | Error | v | - | v | - |
| 14 | Event name matching between state transition and output definition | Error | v | - | - | v |

## 3.8.Event definition sheet

(1) The name of sheet is required to be same with one was declared in FSM0 sheet. The sheet name is specified by the column “EVENT” in FSM0 sheet. If the content of “EVENT” column is blank or “-”, the sheet name is recommended to be <FSM_name>_EVENT. Note: <FSM_name> is content of “FSM” column in FSM0 sheet.

(2) This is an optional sheet in an input Excel file. But if FSM0 sheet exists, this sheet is required. If not, the Erakis dumps an error message and exits.

(3) Event definition sheet is a sheet used to declare events and their corresponding signals' values. Refer to table 3.14 for an example.

*Table 3.14: Example about event definition sheet*

| event_sig | ctrl | [Event] |
|---|---|---|
| 3'b111 | 1 | Event1 |
| 3'b000 | 0 | Event2 |
| 3'b001 | 0 | Event3 |
| 3'b010 | 0 | Event4 |
| 3'b011 | 0 | Event5 |
| 3'b100 | 0 | Event6 |
| 3'b101 | 0 | Event7 |
| 3'b110 | 0 | Event8 |
| 3'b111 | 0 | Event9 |
| 3'b101 | 1 | Event10 |
| 3'b010 | 1 | Event11 |
| 3'b000 | 1 | Event12 |

(4) Constraints:

(4.1) No blank cell. Example: in table 3.15, line Event3 has 1 blank cell.

(4.2) No duplicated event name. Example, in table 3.15, there are 2 Event1.

(4.3) No duplicated combination of event signals. Example, in table 3.15, Event4 and Event5 have same combination of event signals.

(4.4) Event name is required to be matched between state transition table and event definition table.

(5) Additional information:

(5.1) If an event signal is not defined in Port info sheet. Its port width can be got by the format of value. Example, in table 3.14, the “event_sig” has value “3'b111”. So, its port width is 3 bits.

*Table 3.15: Example about WRONG event definition sheet*

| event_sig | ctrl | [Event] |
|---|---|---|
| 3'b111 | 1 | Event1 |
| 3'b000 | 0 | Event1 |
| 3'b001 | | Event3 |
| 3'b011 | 0 | Event4 |
| 3'b011 | 0 | Event5 |
| 3'b100 | 0 | Event6 |

### 3.9.State transition table sheet

(1) The name of sheet is required to be same with one was declared in FSM0 sheet. The sheet name is specified by the column “STAT_TRAN” in FSM0 sheet. If the content of “STAT_TRAN” column is blank or “-”, the sheet name is recommended to be <FSM_name>_TRAN. Note: <FSM_name> is content of “FSM” column in FSM0 sheet.

(2) This is an optional sheet in an input Excel file. But if FSM0 sheet exists, this sheet is

required. If not, the Erakis dumps an error message and exits.

(3) State transition table sheet is a sheet used to declare the transition from state to state based on the changes of events. Refer to table 3.16 for an example.

*Table 3.16: Example about state transition table sheet*

| [Event] | *State0 | State1 | State2 | State3 | State4 | State5 | State6 | State7 | State8 | State9 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Event1 | State1 | / | / | / | / | / | / | / | / | State0 |
| Event2 | / | State2 | / | X | X | X | x | X | X | X |
| Event3 | / | X | State3 | / | x | X | X | X | X | X |
| Event4 | / | / | / | State4 | / | / | / | / | / | X |
| Event5 | / | / | / | State5 | State5 | / | / | / | / | X |
| Event6 | / | / | / | / | / | State6 | State5 | / | / | X |
| Event7 | / | / | / | / | / | State7 | x | / | / | X |
| Event8 | / | / | / | / | / | State9 | X | State9 | / | / |
| Event9 | / | / | / | / | / | / | State7 | / | / | X |
| Event10 | / | / | / | / | / | / | State9 | / | / | / |
| Event11 | / | / | / | / | / | / | / | State8 | State7 | X |
| Event12 | / | / | / | / | / | / | X | X | State9 | / |

(4) Legend:

(4.1) The initial state is required to be start with “*”. Example, In table 3.16, initial state is “State0”.

Only one initial state in a state transition table is required.

(4.2) If a state ignore a certain event, the “/” character is required in this cell.

(4.3) If an event never occurs in a certain state, the “x” character is required in this cell.

(5) Some constraints in this sheet:

(5.1) No blank cell.

(5.2) State is required to be transmitted from other.

(5.3) State is required to transmit to other.

(5.4) All states in this sheet are required to be defined in state definition sheet.

(5.5) A state must not transit to itself.

(5.6) Event name is required to be matched between state transition table and event definition table.

(5.7) State name is required to be matched between state transition table sheet and state definition sheet.

(5.8) State name is required to be matched between state transition table sheet and output definition sheet.

### 3.10.State definition sheet

(1) The name of sheet is required to be same with one was declared in FSM0 sheet. The

sheet name is specified by the column “STAT_DEF” in FSM0 sheet. If the content of “STAT_DEF” column is blank or “-”, the sheet name is recommended to be <FSM_name>_DEF. Note: <FSM_name> is content of “FSM” column in FSM0 sheet.

(2) This is an optional sheet in an input Excel file. But if FSM0 sheet exists, this sheet is required. If not, the Erakis dumps an error message and exits.

(3) State definition sheet is a sheet used to declare the state and their corresponding state signals. Refer to table 3.17 for an example.

*Table 3.17: Example about state definition sheet*

| STn | ST2 | ST1 | ST0 | [State] |
| --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | State0 |
| 0 | 0 | 0 | 1 | State1 |
| 0 | 0 | 1 | 0 | State2 |
| 0 | 0 | 1 | 1 | State3 |
| 0 | 1 | 0 | 0 | State4 |
| 0 | 1 | 0 | 1 | State5 |
| 0 | 1 | 1 | 0 | State6 |
| 0 | 1 | 1 | 1 | State7 |
| 1 | 0 | 1 | 0 | State8 |
| 1 | 1 | 1 | 1 | State9 |

(4) Some constraints in this sheet:

(4.1) No blank cell.

(4.2) No duplicated state name.

(4.3) No duplicated combination of state signal.

(4.4) State name is required to be matched between state transition table sheet and state definition sheet.

### 3.11. Output definition sheet

(1) The name of sheet is required to be same with one was declared in FSM0 sheet. The sheet name is specified by the column “OUT” in FSM0 sheet. If the content of “OUT” column is blank or “-”, the sheet name is recommended to be <FSM_name>_OUT. Note: <FSM_name> is content of “FSM” column in FSM0 sheet.

(2) This is an optional sheet in an input Excel file. But if FSM0 sheet exists, this sheet is required. If not, the Erakis dumps an error message and exits.

(3) State definition sheet is a sheet used to declare the state and their corresponding state signals. Refer to table 3.18 for an example.

*Table 3.18: Example about output definition sheet*

| [state] | out |
| --- | --- |
| State0 | 2'b00 |

| | |
|---|---|
| State1 | 2'b00 |
| State2 | 2'b00 |
| State3 | 2'b00 |
| State4 | 2'b00 |
| State5 | 2'b00 |
| State6 | 2'b01 |
| State7 | 2'b10 |
| State8 | 2'b10 |
| State9 | 2'b11 |

(4) Some constraints in this sheet:

(4.1) No blank cell.

(4.2) Referent table used in this sheet is required to exist in input Excel file.

(4.3) State name is required to be matched between state transition table sheet and this sheet.

(5) Additional information:

(5.1) If an output signal is not defined in Port info sheet. Its port width can be got by the format of value. Example, in table 3.18, the “out” has value “2'b00”. So, its port width is 2 bits.

# 4.Output description

## 4.1.Lack log file

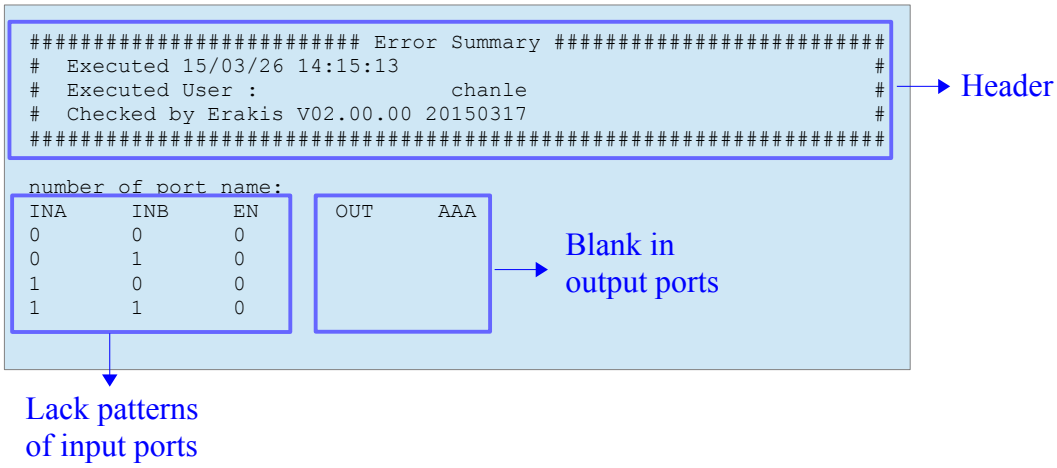


*Figure 4.1: Example of lack log file*

## 4.2.Overlap log file

```
########################## Error Summary ##########################
#  Executed 15/03/31 09:13:54                                      #
#  Executed User :               chanle                            #
#  Checked by Erakis V02.00.00 20150317                            #
###################################################################

number of port name:
=======================

Sheet    line     input    input    input    output
-        -        INA      INB      EN       BBB
***ERROR : Exist Data two or more
Table0   20       *        0        0        1
Table0   28       *        0        0        1
***ERROR : Exist Data two or more
Table0   23       X        1        X        0
Table0   26       X        1        X        X

 ### END ###
```

A pair of overlapped patterns

A pair of overlapped patterns

*Figure 4.2: Example of overlap log file*

## 4.3.Test bench file

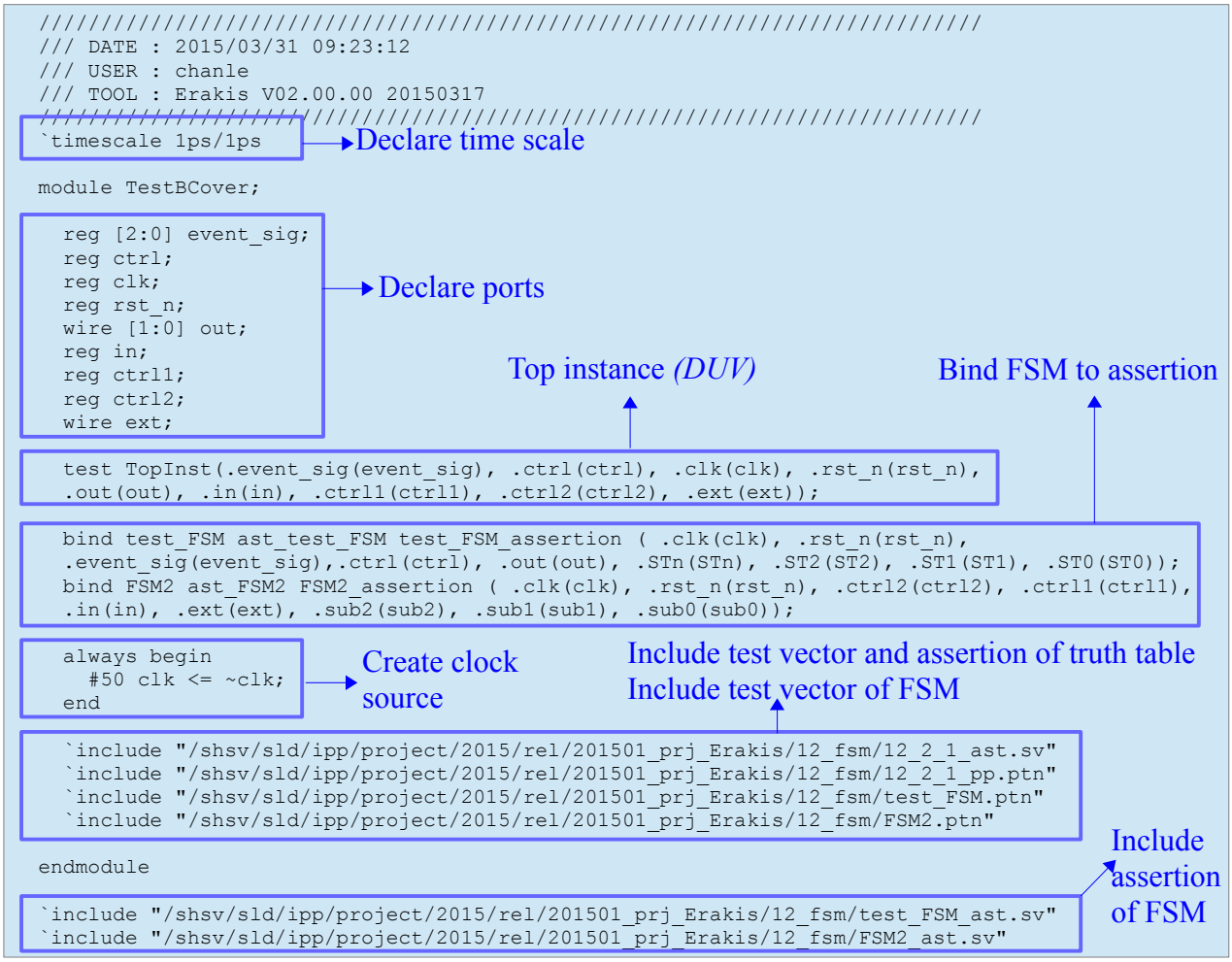


*Figure 4.3: Example of test bench file*

### 4.4.Test vector file of truth table

```
////////////////////////////////////////////////////////////////////////////////
/// DATE : 2015/03/31 09:23:12
/// USER : chanle
/// TOOL : Erakis V02.00.00 20150317
////////////////////////////////////////////////////////////////////////////////

parameter DELAY=99;

reg b_it[3:0];
  integer  i1, i2, i3;

initial begin

  b_it[3]=1'bz;
  b_it[2]=1'bx;
  b_it[1]=1'b1;
  b_it[0]=1'b0;


//------------next truth table-------//
  for(i1=0;i1<3;i1=i1+1) begin
    clk = b_it[i1];
    for(i2=0;i2<3;i2=i2+1) begin
      rst_n = b_it[i2];
      for(i3=0;i3<8;i3=i3+1) begin
        event_sig = i3;
        #DELAY  i0=i0+1;
        #1;
      end
    end
  end

  #DELAY  i0=i0+1;

end
```

Declare variable

Create test patterns

i0 is used to trigger assertion

*Figure 4.4: Example of test vector file of truth table*

## 4.5.Assertion file of truth table

```
////////////////////////////////////////////////////////////////////////////////
/// DATE : 2015/03/31 09:57:03
/// USER : chanle
/// TOOL : Erakis V02.00.00 20150317
////////////////////////////////////////////////////////////////////////////////

// SVA check

  integer i0=0;
//------------next truth table-------//
  check0 : assert property (
    @(i0) disable iff(i0==0)
    ((INA===1'b0)&&(INB===1'b0)) |-> ((OUT===1'b0))
  );

  check1 : assert property (
    @(i0) disable iff(i0==0)
    ((INA===1'b0)&&(INB===1'b1)) |-> ((OUT===1'b1))
  );

//=============================================//
//============Completeness lack patterns=======//
//=============================================//

//------------next truth table-------//
  completeness0 : assert property (
    @(i0) disable iff(i0==0)
    ((INA===1'b0)&&(INB===1'bX)) |-> ((OUT===1'bX))
  );

  completeness1 : assert property (
    @(i0) disable iff(i0==0)
    ((INA===1'b0)&&(INB===1'bZ)) |-> ((OUT===1'bX))
  );

  completeness2 : assert property (
    @(i0) disable iff(i0==0)
    ((INA===1'b1)) |-> ((OUT===1'bX))
  );

  completeness3 : assert property (
    @(i0) disable iff(i0==0)
    ((INA===1'bX)) |-> ((OUT===1'bX))
  );
```

Assertions of test patterns in the truth table

Assertions of lack patterns *(in case using -cpl option)*

*Figure 4.5: Example of assertion file of truth table*

### 4.6.Test vector file of FSM

```
////////////////////////////////////////////////////////////////////////////////
/// DATE : 2015/03/31 09:24:11
/// USER : chanle
/// TOOL : Erakis V02.00.00 20150317
////////////////////////////////////////////////////////////////////////////////

parameter DELAY_FSM2=100;

initial begin

  #(79700+100)

  //Correct the clock
  clk=1;
  #1 //Make signal stable at rising edge
  //===== Create PTN check state path=====
  rst_n = 1'b0;
  #DELAY_FSM2
  #DELAY_FSM2
  rst_n = 1'b1;
  //----- Come from initial to state "StateA" -----
  #DELAY_FSM2

  force TopInst.ctrl2=1'bx;
  force TopInst.ctrl1=1;
  #DELAY_FSM2
  force TopInst.ctrl2=0;
  force TopInst.ctrl1=1;
  #DELAY_FSM2
  force TopInst.ctrl2=1;
  force TopInst.ctrl1=0;
  force TopInst.in=0;
  #DELAY_FSM2
  force TopInst.ctrl2=1;
  force TopInst.ctrl1=0;
  force TopInst.in=1;
  #DELAY_FSM2
  force TopInst.ctrl2=1;
  force TopInst.ctrl1=1;
  force TopInst.in=0;
  #DELAY_FSM2
  force TopInst.ctrl2=1;
  force TopInst.ctrl1=1;
  force TopInst.in=1;
  #DELAY_FSM2

  rst_n = 1'b0;
  #DELAY_FSM2
  #DELAY_FSM2
  rst_n = 1'b1;

  //----- Come from initial to state "StateB" -----
  …
  …


  #DELAY_FSM2
  $finish;

end
```

Clock period

Reset to go to initial state

Change event signal to go to “StateA”

Reset to go to initial state *(before go to “StateB”)*

Change event signal to go to remain states

*Figure 4.6: Example of test vector of FSM*

## 4.7.Assertion file of FSM

```
//=========================================//
//============Check FSM name: FSM2
//=========================================//
module ast_FSM2(clk, rst_n, ctrl2, ctrl1, in, ext, sub2, sub1, sub0);

input clk;
input rst_n;
input ctrl2;
input ctrl1;
input in;
input ext;
input sub2;
input sub1;
input sub0;
```

Declare input of "assertion" mudule

Check initial state after de-asserting reset.
Check ignored event, prohibited event of any state.

```
check_initial_state_FSM2: assert property (
    @(posedge rst_n) ((sub2===1)&&(sub1===0)&&(sub0===1))
);
ignored_FSM2_0: assert property (
    @(posedge clk) disable iff(rst_n===1'b0)((sub2===0)&&(sub1===0)&&(sub0===0)
    && (ctrl2===1'bx)&&(ctrl1===0)) |=> (sub2===0)&&(sub1===0)&&(sub0===0)
);
ignored_FSM2_1: assert property (
    @(posedge clk) disable iff(rst_n===1'b0) ((sub2===0)&&(sub1===0)&&(sub0===0)
    && (ctrl2===1'bx)&&(ctrl1===1)) |=> (sub2===0)&&(sub1===0)&&(sub0===0)
);
covered_FSM2_0: assert property (
    @(posedge clk) disable iff(rst_n===1'b0) ((sub2===0)&&(sub1===0)&&(sub0===0)
    && (ctrl2===0)&&(ctrl1===0)) |=> (sub2===1)&&(sub1===0)&&(sub0===0)
);
ignored_FSM2_2: assert property (
    @(posedge clk) disable iff(rst_n===1'b0) ((sub2===0)&&(sub1===0)&&(sub0===0)
    && (ctrl2===0)&&(ctrl1===1)) |=> (sub2===0)&&(sub1===0)&&(sub0===0)
);
ignored_FSM2_3: assert property (
    @(posedge clk) disable iff(rst_n===1'b0) ((sub2===0)&&(sub1===0)&&(sub0===0)
    && (ctrl2===1)&&(ctrl1===0)&&(in===0)) |=> (sub2===0)&&(sub1===0)&&(sub0===0)
);
ignored_FSM2_4: assert property (
    @(posedge clk) disable iff(rst_n===1'b0) ((sub2===0)&&(sub1===0)&&(sub0===0)
    && (ctrl2===1)&&(ctrl1===0)&&(in===1)) |=> (sub2===0)&&(sub1===0)&&(sub0===0)
);
prohibited_FSM2_0: assert property (
    @(posedge clk) disable iff(rst_n===1'b0)
    ((sub2===0)&&(sub1===0)&&(sub0===0)) |-> !((ctrl2===1)&&(ctrl1===1)&&(in===0))
);
…
…
```

```
output_of_states_FSM2_0: assert property (
    @(posedge clk) ((sub2===0)&&(sub1===0)&&(sub0===0)) |-> ((ext===1'bz))
);
output_of_states_FSM2_1: assert property (
    @(posedge clk) ((sub2===0)&&(sub1===0)&&(sub0===1)) |-> ((ext===0))
);
output_of_states_FSM2_2: assert property (
    @(posedge clk) ((sub2===0)&&(sub1===1)&&(sub0===0)) |-> ((ext===0))
);
output_of_states_FSM2_3: assert property (
    @(posedge clk) ((sub2===0)&&(sub1===1)&&(sub0===1)) |-> ((ext===1))
);
output_of_states_FSM2_4: assert property (
    @(posedge clk) ((sub2===1)&&(sub1===0)&&(sub0===0)) |-> ((ext===1))
);
output_of_states_FSM2_5: assert property (
    @(posedge clk) ((sub2===1)&&(sub1===0)&&(sub0===1)) |-> ((ext===1'bz))
);
endmodule
```

Check output of each state

*Figure 4.7: Example of assertion file of FSM*

# 5.Tool options

(1) Table 5.1 summarizes, and categorizes all options of Erakis. The details are describes in the followings chapters *(in "Referent chapter" column).*

*Table 5.1: Summary options of Erakis*

| Option | | Description | Supported in Version |
|---|---|---|---|
| GENERAL | -tb \| -testbench | Execute to make test bench | v1.5 |
| | -vcs | Execute to make scripts of execution VCS | v1.5 |
| | -irun \| -incisive | Execute to make scripts of execution irun | v1.5 |
| | -ams | Set this option when users execute irun command with circuit | v1.5 |
| | -ts \| -timescale | Set timescale in test bench | v1.5 |
| | -nowave | No wave output | v1.5 |
| | -vpd | Set VPD for output wave file format | v1.5 |
| | -fsdb | Set FSDB for output wave file format | v1.5 |
| | -h \| -help | Show help | v1.5 |
| TRUTH TABLE | -tc \| -check | Execute to check truth table | v1.5 |
| | -tv \| -ptn | Execute to make test pattern (test vector) for truth table | v1.5 |
| | -ta \| -assertion | Execute to make assertion for truth table | v1.5 |
| | -err | Max error number will be dumped in output log file when users check truth table | v1.5 |
| | -ex_ast | Execute to make assertion of input prohibition | v1.5 |
| | -pg | Set this option when users use model with power-ground (PG) | v1.5 |
| | -cr \| -compression | Set port name which allows "*" (don't care) in output log file | v1.5 |
| | -cpl | Control completeness checking | v2.0 |
| | -p \| -pcheck | Output only pattern that appointed in truth table as pattern | v1.5 |
| FSM | -fsmc | Execute to check tables related to FSM | v2.0 |
| | -fsmtv | Execute to make test pattern (test vector) for FSM | v2.0 |
| | -fsmast | Execute to make assertion for FSM | v2.0 |

(2) Some notes below about options:

**(2.1) Note 1: the default options.**

(2.1.1) The options: -tb, -tc, -tv, -ta, -fsmc, -fsmtv, -fsmast are defined as default.

Example: >> erks input.xls.

Equivalent to: >> erks input.xls -tb -tc -tv - ta - fsmc -fsmtv -fsmast

(2.1.2) If users define any option belong to list above, Erakis executes with the defined option only.

Example: >> erks input.xls -tb -tc

Erakis checks the truth table (-tc option), and makes the test bench (-tb option).

**(2.2) Note 2: using -tc, -tv, -ta option**

Do not define any of options above (-tc, -tv, -ta) when there is no truth table *(Table0 sheet)*.

If users define any option of -tc, -tv, -ta when there is no truth table, an error message will be dumped and Erakis exits.

**(2.3) Note 3: using -fsmc, -fsmtv, -fsmast option**

These options above are used to check the FSM tables, make test vectors, make assertions for FSM.

Do not define any of options above (-fsmc, -fsmtv, -fsmast) when there is no FSM table *(FSM0 sheet)*.

If users do define any option of -fsmc, -fsmtv, -fsmast when there is no FSM table, an error message will be dumped and Erakis exits.

**(2.4) Note 4: Do not define a option more than one time.**

### 5.1.-tb | -testbench option

(1) Set this option to generate a test bench file. The file name of this test bench is defined in “tb_file” tag of Erakis info sheet.

(2) Usage:

>> erks input.xls -tb

or

>> erks input.xls -testbench.

(3) Depending on the other used options, a generated test bench file may include test vector file of truth table, test vector file of FSM, the assertion file of truth table, and assertion file of FSM.

### 5.2.-tc | -check option

(1) Set this option to check the validity of truth table. There are 2 kinds of checking:

(1.1) Check whether truth table lacks test pattern or not. If lack pattern, the Erakis dumps an error message and exits. A “lack output” file containing the lack patterns is generated to inform users. The name of lack output file is defined in “lack_log” tag of Erakis info sheet.

This option can be combined with other options such as:

(1.1.1) -err option to limit the maximum lack test pattens dumped in lack output file.

(1.1.2) -cr | -compression option to compress the lack patterns based on the value of input.

(1.2) Check whether truth table has overlapped test pattern or not. If overlapped, the Erakis dumps an error message and exits. An “overlapped output” file containing the overlapped test patterns is generated to inform users. The name of overlapped output file is defined in “overlap_log” tag of Erakis info sheet.

(2) Usage:

>> erks input.xls -tc

or

>> erks input.xls -check

(3) Some notes about this option:

(3.1) Do not set this option with -cpl option, because they are exclusive each other.

(3.2) The lack patterns is the patterns to which users did not care in input Excel file. So, the reported lack patterns are the lack ones in both truth table and exclude table.

### 5.3.-tv | -ptn option

(1) Set this option to generate a test vector file for truth table. The file name of test vector is defined in “ptn_file” tag of Erakis info sheet.

(2) Usage:

>> erks input.xls -tv

or

>> erks input.xls -ptn

(3) In the test vector file, an “i0” variable is used to trigger checking assertion for truth table.

### 5.4.-ta | -assertion option

(1) Set this option to generate a assertion file for truth table. The file name of assertion is defined in “ast_file” tag of Erakis info sheet.

(2) Usage:

>> erks input.xls -ta

or

>> erks input.xls -assertion

(3) In the assertion file, assertions are checked at the change of “i0” variable. This variable is change after changing input ports *(in the test vector file)*.

### 5.5.-fsmc option

(1) Set this option to check the validity of FSM tables. They are FSM0 table, state definition table, event definition table, state transition table, output definition table.

(2) If the FSM tables above do not satisfy rules in table 3.13 “Summary constraints in FSM“, the Erakis dumps message and exits in case of error.

(3) Usage:

>> erks input.xls -fsmc

### 5.6.-fsmtv option

(1) Set this option to generate test vector file(s) for FSM. The number of test vector file is the number FSM in DUV. Each FSM is defined in one row in FSM0 sheet. The file name of each test vector file is defined by the FSM name in FSM0 sheet with format:

<FSM_name>.ptn

(2) Usage:

>> erks input.xls -fsmtv

(3) In test vector, the followings are created.

(3.1) Change event signals to move all states in state transition table.

(3.2) In each state, change event signals to create the ignored event of this state.

(3.3) Assert reset, then, de-assert reset at every state.

### 5.7.-fsmast option

(1) Set this option to generate assertion file(s) for FSM. The number of assertion file is the number FSM in DUV. Each FSM is defined in one row in FSM0 sheet. The file name of each assertion file is defined by FSM name in FSM0 sheet with format: <FSM_name>_ast.sv

(2) Usage:

>> erks input.xls -fsmast

(3) In the assertion file, the followings are checked.

(3.1) The output of each state.

(3.2) The moving from previous state to next state according with an event.

(3.3) A state is kept or not when its ignored event is triggered.

(3.4) Prohibited event of a state never occurs.

(3.5) After the reset signal is de-asserted, the state moves to “initial” state.

### 5.8.-vcs option

(1) Set this option to generate a script to run VCS. The following files are generated:

(1.1) “infile.f” contains file and option list.

(1.2) “uclirc” contains the UCLI executive command.

(1.3) “run_vcs” contains the shell script to run VCS.

(2) Usage:

>> erks input.xls -vcs

(3) Some notes when using this option:

(3.1) Do not set this option with -irun | -incisive option because they are exclusive each other.

(3.2) Define “VCS” tag and “verilog” in Erakis info to satisfy the table 3.4 “Harmonization between options and tags in “Erakis info” sheet“.

### 5.9.-irun | -incisive option

(1) Set this option to generate a shell script for “Incisive”. The following files are generated:

(1.1) “infile.f” contains input file.

(1.2) “irun.tcl” contains the executive TCL script.

(1.3) “run_irun” contains the shell script to run Incisive.

(2) Usage:

>> erks input.xls -irun

or

>> erks input.xls -incisive

(3) Some notes when using this option:

(3.1) Do not set this option with -vcs option because they are exclusive each other.

(3.2) Define “Incisive” tag and “verilog” tag in Erakis info to satisfy the table 3.4 “Harmonization between options and tags in “Erakis info” sheet“.

### 5.10.-ams option

(1) Set this option to generate a shell script for “irun” with circuit. The following files are generated:

(1.1) “probe.tcl”: TCL script.

(1.2) “amsControlSpectre.scs” to control spectre.

(1.3) “<cell_name>.ocn”: ocean script.

(1.4) “run_irun”: shell script to run irun.

(2) Usage**:**

>> erks input.xls -ams

(3) The “view_name” tag, “lib_name” tag, “cds.lib” tag, “Incisive” tag, “virtuoso” tag, and “ConnectRule” tag are required in Erakis info. Refer to table 3.4 “Harmonization between options and tags in “Erakis info” sheet“.

### 5.11.-err option

(1) Set this option to limit the number of error dumped in lack output file. This option often is used with -tc | -check option.

(2) Usage**:**

>> erks input.xls -err <number>

In this: <number> is an positive integer number indicating maximum error number.

(3) Some notes when using this option:

(3.1) If this option is not defined, The maximum error number is 100.

(3.2) Unlimited error number if <number> is -1.

### 5.12.-ex_ast option

(1) Set this option to generate the assertion file for prohibited inputs. The prohibited inputs are the patterns defined in Exclude sheet.

(2) This assertion file for prohibited inputs and the assertion file of truth table (when using -ta | -assertion option) are essentially separate. The file name of assertion file for prohibited inputs is defined in “exclude_in” tag of Erakis info sheet.

(3) Usage:

>> erks input.xls -ex_ast

### 5.13.-pg option

(1) Set this option to get all information of power port into test vector.

(2) Usage:

>> erks input.xls -pg

(3) Some notes related to this option.

(3.1) When this option is not used, the validity of power/supply ports is checked.

(3.1.1) The value of VDD/VCC port is required to be “1” or “*” *(don't care)*.

(3.1.2) The value of VSS/GND port is required to be “0” or “*” *(don't care)*.

A pattern is omitted if failing any of 2 conditions above.

(3.2) When this option is used, the Erakis does not checks values of power/supply ports.

### 5.14.-ts | -timescale option

(1) Set this option to specify the time scale.

(2) Usage:

>> erks input.xls -ts <time_scale>

or

>> erks input.xls -timescale <time_scale>

In this: <time_scale> is time scale. Example: 1ns/1ps

(3) When this option is not used, default time scale is 1ps/1ps

### 5.15.-nowave option

(1) Set this option to not generate any waveform.

(2) Usage:

>> erks input.xls -nowave

(3) Do not set this option with -vpd option or -fsdb option because they are exclusive each other.

### 5.16.-vpd option

(1) Set this option to generate waveform as VPD format.

(2) Usage:

>> erks input.xls -vpd

(3) Do not set this option with -fsdb option because they are exclusive each other.

### 5.17.-fsdb option

(1) Set this option to generate waveform as FSDB format.

(2) Usage:

>> erks input.xls -fsdb

(3) Do not set this option with -vpd option because they are exclusive each other.

### 5.18.-cr | -compression option

(1) Set this option to compress the lack pattern dumped in lack log file to be smaller.

(2) Usage:

>> erks input.xls -cr <port_list>

or

>> erks input.xls -compression <port_list>

In this, <port_list> is the port list. Example: INA INB

(3) Some notes related to this option.

(3.1) If list of port is empty, all input ports are compressed.

(3.2) If any port in list is not declared in Port info sheet. The Erakis dumps error message and exits.

### 5.19.-cpl option

(1) Set this option to control completeness checking.

(2) When using this option, based on input options (-tv, -ta), the Erakis generates output files: test vector file, assertion file without checking truth table. Below is processing steps:

(2.1) Dump warning message: “The truth table's lack patterns output X. And total assertions is N. Is it really all right?”

Note: N is an estimation number of lack patterns needed to generate assertion.

(2.2) Users press the decision that “yes” | ”y” or “no”.

(2.2.1) If “yes”, the Erakis generates test vectors and assertions for the patterns in truth table and the lack ones.

(2.2.2) If “no”, the Erakis just generate test vector and assertion for truth table only.

(3) Usage:

>> erks input.xls -cpl

(4) Some notes related to this option.

(4.1) The lack patterns is the patterns in both truth table and exclude table.

(4.2) Do not set this option with -tc | -check option, because they are exclusive each other.

(4.3) In assertion file, all lack patterns has values of outputs port are “X”.

### 5.20.-p | -pcheck option

(1) Set this option to generate test vectors and assertions for some appointed patterns only.

(2) Usage:

>> erks input.xls -p

or

>> erks input.xls -pcheck

(3) Some notes related to this option.

(3.1) When not use this option, the column “pcheck” in truth table *(maybe Table0 or referent tables of Table0)* is no meaning. This column is ignored.

(3.2) When this option is used, only patterns having value “1” in “pcheck” column is used to generate test vector and assertion.

Refer to table 5.2 for an example. The Erakis generates test vectors and assertions for “white” rows only; and omits the “gray” rows.

*Table 5.2: Example about omitting patterns when using -p | -pcheck option.*

| pcheck | input | | output |
| --- | --- | --- | --- |
| | INA | INB | OUT |
| 1 | 0 | 0 | 1 |
| | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| | 1 | 1 | 1 |
| | x | * | x |
| 1 | 0 | x | 0 |
| | 1 | x | 0 |

### 5.21.-h | -help option

(1) Set this option to know about Erakis' options.

(2) Usage:

>> erks input.xls -h

or

>> erks input.xls -help

(3) When users run command **erks** only *(without any option or input parameter)*.

Example: erks

The help message is also dumped for instructing users.

## 6.Message

(1) This chapter lists all messages in Erakis tool, and describes when a message is dumped. Refer to table below:

*Table 6.1: List of all messages in the Erakis tool*

| No. | Severity | Message | Description |
|---|---|---|---|
| 1 | Error | ERROR ::: Cannot define "<option_name>" option more than twice | This message is dumped when an option is defined 2 times or more.<br><br><option_name>: -err option or -ts \| -timescale option, |
| 2 | Error | ERROR ::: Don't set <option_name> option with -irun or -incisive option. | This message is dumped when -vcs option is defined with -irun \| -incisive option.<br><br><option_name>: -vcs option. |
| 3 | Error | ERROR ::: Don't set <option_name> option with -vcs option. | This message is dumped when -irun \| -incisive option is defined with -vcs option.<br><br><option_name>: -irun \| -incisive option. |
| 4 | Error | ERROR ::: Don't set <option_name> option with -vpd option. | This message is dumped when -fsdb option is defined with -vpd option.<br><br><option_name>: -fsdb option. |
| 5 | Error | ERROR ::: Don't set <option_name> option with -fsdb option. | This message is dumped when -vpd option is defined with -fsdb option.<br><br><option_name>: -vpd option. |
| 6 | Error | ERROR ::: Don't set <option_name> option with -fsdb or -vpd option. | This message is dumped when -nowave option is defined with -vpd option or -fsdb option.<br><br><option_name>: -nowave option. |
| 7 | Error | ERROR ::: Not duplicate -cpl option. | This message is dumped when -cpl option is defined 2 times, or more. |
| 8 | Error | ERROR ::: Unknown option <option_name> | This message is dumped when users specify an invalid option which is not included in supported option of Erakis.<br><br><option_name>: invalid option |
| 9 | Error | ERROR ::: Cannot define Excel file more than twice. | This message is dumped when users specify the input Excel file 2 times or more. |
| 10 | Error | ERROR ::: Please include Excel file. | This message is dumped when users do not specify the input Excel file. |
| 11 | Error | ERROR ::: Do not set both checking truth table and completeness lack pattern. | This message is dumped when users define both -cpl option and -tc \| -check option. |
| 12 | Error | ERROR ::: Set max err number after -err option. | This message is dumped when users use -err option but not specify the maximum number of error for this option. |
| 13 | Error | ERROR ::: Please defined timescale after -ts or -timescale option. | This message is dumped when users use -ts \| -timescale option but not specify the time scale or the specified value is invalid. |
| 14 | Error | ERROR ::: Set Port name after -cr or -compression option. | This message is dumped when users use -cr \| -compression option but not specify the port name after or specify wrong port name. |
| 15 | Error | ERROR ::: [Port info] <cell> is invalid | This message is dumped when users specify: |

| No. | Severity | Message | Description |
|---|---|---|---|
| | | value. | - an invalid value in “care range” column of Port info sheet.<br>- or blank cell in Port info sheet.<br><br><cell>: the invalid cell in Excel file. |
| 16 | Error | Error ::: <column_name> info is not in <excel> - port info. | This message is dumped when Port info sheet has not <column_name> column.<br><br><column_name>: can be “port” or “I/O” or “D/A”.<br><excel>: the name of input Excel file. |
| 17 | Error | ERROR ::: Port info and truth table's port name differ: <port_name> | This message is dumped when users use a port in truth table. But this port is not declared in Port info sheet.<br><br><port_name>: the name of wrong port. |
| 18 | Error | ERROR ::: No <column_name> column in <excel> - <sheet>. | This message is dumped when Table0 sheet has not <column_name> column.<br><br><column_name> Can be “supply” or “input” or “output”.<br><excel>: the name of input Excel file.<br><sheet>: the Table0 sheet. |
| 19 | Error | ERROR ::: When you use OPTION -p, truth table needs "pcheck" column. file : <excel> - <sheet>. | This message is dumped when a truth table *(Table0 sheet or referent sheet related to truth table)* has not “pcheck” column, in case the -p \| -pcheck option is used.<br><br><excel>: the name of input Excel file.<br><sheet>: the Table0 sheet. |
| 20 | Error | ERROR ::: <cell_content> must be covered in <> in case of referent table or be covered in [] in case of variable. | This message is dumped when content of a cell in truth table *(Table0 sheet or referent sheet related to truth table)* is invalid. Invalid value means that it is not a digit.<br><br><cell_content>: the content of a cell. |
| 21 | Error | ERROR ::: [Variable] Duplicated variable column in. | This message is dumped when “Variable” sheet has 2 “variable” column. |
| 22 | Error | ERROR ::: [Variable] Duplicated expression column. | This message is dumped when “Variable” sheet has 2 “expression” column. |
| 23 | Error | ERROR ::: [Variable] "variable" column must be before "expression" column. | This message is dumped when the “expression” column is placed before “variable” column. |
| 24 | Error | ERROR ::: [Variable] Invalid input. The title of variable column must be "var" or "variable".The title of expression column must be "expr" or "expression". | This message is dumped when:<br>- wrong title name of “variable” column<br>- or wrong title name of “expression” column. |
| 25 | Error | ERROR ::: "Variable" is not found in <excel>. | This message is dumped when a variable is used in truth table but “Variable” sheet does not exist in the input Excel file.<br><br><excel>: the input Excel file. |

| No. | Severity | Message | Description |
|---|---|---|---|
| 26 | Error | "ERROR ::: [Variable] <variable> does not exist. | This message is dumped when a variable is used in truth table but it is not found in the “Variable” sheet.<br><br><variable>: the not found variable |
| 27 | Error | ERROR ::: [Variable] There are more than one <variable> exist. | This message is dumped when a variable is used in truth table but is is found in the “Variable” sheet more than one time.<br><br><variable>: the duplicated variable |
| 28 | Error | ERROR ::: Cannot calculate value of <variable> because of invalid expression. | This message is dumped when a variable is used in truth table but its expression is invalid.<br><br><variable>: variable |
| 29 | Error | ERROR ::: <tag_name> is defined two or more. | This message is dumped when users define a tag in Erakis info sheet more than one time.<br><br><tag_name>: the tag name. It may be: cell, out_dir, tb_file, ptn_file, ast_file, lack_log, overlap_log, lib_name, view_name, max_delay, cds.lib, Incisive, VCS, Verdi, virtuoso, ConnectRule, exclude_in, pref_unit. |
| 30 | Error | ERROR ::: [Erakis info] Please define the "<tag_name>" tag. | This message is dumped when users:<br>- defined -vcs option, but not defined “VCS” tag or “verilog” tag in Erakis info sheet.<br>- defined -vcs option, and -fsdb option, but not defined “VCS” tag or “verilog” tag or “Verdi” tag in Erakis info sheet.<br>- defined -irun \| -incisive option, but not defined “Incisive” tag or “verilog” tag in Erakis info sheet.<br>- defined -ams option, but not defined “view_name” tag, “lib_name” tag, “cds.lib” tag, “Incisive” tag, “virtuoso” tag, or “ConnectRule” tag in Erakis info sheet.<br><br><tag_name>: the not defined tag. |
| 31 | Error | ERROR ::: [FSM0] Duplicated "<column_name>" column. | This message is dumped when FSM0 sheet has duplicated column name.<br><br><column_name>: the duplicated column name. It may be FSM, EVENT, STAT_TRAN, STAT_DEF, OUT, CLK, RESET. |
| 32 | Error | ERROR ::: [FSM0] FSM name info is not defined. | This message is dumped when the FSM name info is not defined in the FSM column of FSM0 sheet. |
| 33 | Error | ERROR ::: [FSM0] Event definition info is not defined. | This message is dumped when the Event definition info is not defined in the EVENT column of FSM0 sheet. |
| 34 | Error | ERROR ::: [FSM0] State transition info is not defined. | This message is dumped when the State transition info is not defined in the STAT_TRAN column of FSM0 sheet. |
| 35 | Error | ERROR ::: [FSM0] State definition info is not defined. | This message is dumped when the State definition info is not defined in the STAT_DEF column of FSM0 sheet. |

| No. | Severity | Message | Description |
| --- | --- | --- | --- |
| 36 | Error | ERROR ::: [FSM0] Output definition info is not defined. | This message is dumped when the Output definition info is not defined in the OUT column of FSM0 sheet. |
| 37 | Error | ERROR ::: [<event_sheet>] Duplicated \"event\" column. | This message is dumped when the Event definition sheet has duplicated “event” column.<br><br><event_sheet>: the sheet name of Event definition sheet. |
| 38 | Error | ERROR ::: [<event_sheet>] Invalid at <cell>. | This message is dumped when in Event definition sheet, there is a cell that out of valid range of Event definition table area.<br><br><event_sheet>: the sheet name of Event definition sheet.<br><cell>: the invalid cell. |
| 39 | Error | ERROR ::: [<event_sheet>] Blank cell at <cell>. | This message is dumped when in Event definition sheet, there is blank cell in Event definition table area.<br><br><event_sheet>: the sheet name of Event definition sheet.<br><cell>: the invalid cell. |
| 40 | Error | ERROR ::: [<state_sheet>] Duplicated "state" column. | This message is dumped when the State definition sheet has duplicated “state” column.<br><br><state_sheet>: the sheet name of State definition sheet. |
| 41 | Error | ERROR ::: [<state_sheet>] Invalid at <cell>. | This message is dumped when in State definition sheet, there is a cell that out of valid range of State definition table area.<br><br><state_sheet>: the sheet name of State definition sheet.<br><cell>: the invalid cell. |
| 42 | Error | ERROR ::: [<state_sheet>] Blank cell at <cell>. | This message is dumped when in State definition sheet, there is blank cell in State definition table area.<br><br><state_sheet>: the sheet name of State definition sheet.<br><cell>: the invalid cell. |
| 43 | Error | ERROR ::: [<trans_sheet>] Duplicated "event" column. | This message is dumped when the State transition sheet has duplicated “event” column.<br><br><trans_sheet>: the sheet name of State transition sheet. |
| 44 | Error | ERROR ::: [<trans_sheet>] Invalid at <cell>. | This message is dumped when in State transition sheet, there is a cell that out of valid range of State transition table area.<br><br><trans_sheet>: the sheet name of State transition sheet.<br><cell>: the invalid cell. |

| No. | Severity | Message | Description |
| --- | --- | --- | --- |
| 45 | Error | ERROR ::: [<trans_sheet>] Blank cell at <cell>. | This message is dumped when in State transition sheet, there is blank cell in State transition table area.<br><br><trans_sheet>: the sheet name of State transition sheet.<br><cell>: the invalid cell. |
| 46 | Error | ERROR ::: [<out_sheet>] Duplicated "state" column. | This message is dumped when the Output definition sheet has duplicated “state” column.<br><br><out_sheet>: the sheet name of Output definition sheet. |
| 47 | Error | ERROR ::: [<out_sheet>] Invalid at <cell>. | This message is dumped when in Output definition sheet, there is a cell that out of valid range of Output definition table area.<br><br><out_sheet>: the sheet name of Output definition sheet.<br><cell>: the invalid cell. |
| 48 | Error | ERROR ::: [<out_sheet>] Blank cell at <cell>. | This message is dumped when in Output definition sheet, there is blank cell in Output definition table area.<br><br><out_sheet>: the sheet name of Output definition sheet.<br><cell>: the invalid cell. |
| 49 | Error | ERROR ::: [<out_sheet>] Reference table <ref_sheet> is not existed in $excel. | This message is dumped when a referent table in Output definition sheet is not found in input Excel file.<br><br><out_sheet>: the sheet name of Output definition sheet.<br><ref_sheet>: the referent sheet. |
| 50 | Error | ERROR ::: State "<state>" is NOT existed in state table. | This message is dumped when a state used in State transition table, but was not defined in State definition table.<br><br><state>: the state name. |
| 51 | Error | ERROR ::: [<stt_sheet>] None of initial state is found. | This message is dumped when there is no initial state in the State transition table.<br><br><stt_sheet>: the sheet name containing State transition table. |
| 52 | Error | ERROR ::: [<stt_sheet>] More than one initial states is found. | This message is dumped when there is more than one initial state in the State transition table.<br><br><stt_sheet>: the sheet name containing State transition table. |
| 53 | Error | ERROR ::: Duplicate <category> '<name>' in <table_name> table. | This message is dumped when there are duplicated state/event name in State/Event definition table.<br><br><category>: “state” or “event”.<br><name>: the name which is duplicated. |

| No. | Severity | Message | Description |
|---|---|---|---|
| | | | <table_name>: the State/Event definition table. |
| 54 | Error | ERROR ::: Duplicate combination of signals of '<name>' in <category> table. | This message is dumped when there are duplicated combination of signals of state/event in State/Event definition table.<br><br><name>: the name which is duplicated combination.<br><category>: “state” or “event”. |
| 55 | Error | ERROR ::: [<sheet_name>] <category> "<name>" is not defined in <table_kind> table "<table_name>". | This message is dumped when a state/event is used in a sheet, but was not declared in State/Event definition table yet.<br><br><sheet_name>: the name of sheet containing undeclared state/event.<br><category>: “state” or “event”.<br><table_kind>: the State/Event definition table.<br><table_name>: the name of State/Event definition sheet. |
| 56 | Error | ERROR ::: [-cr \|-compression] "<port_name>" is not a port in truth table. | This message is dumped when users define -cr \| -compression option with a port which was not declared in port table<br><br><port_name>: the port name. |
| 57 | Error | ERROR ::: Cannot open file <file>. | This message is dumped when cannot open a file.<br><br><file>: the name of file which cannot open. |
| 58 | Error | ERROR ::: [FSM] None optimal combination path of states.<br>So, Erakis stops generating test vector and assertion file for FSM. | This message is dumped when there is error in running Haskell script generating optimal combination path of states. |
| 59 | Error | ERROR ::: "Table0" sheet and "FSM0" sheet do not exist in <excel> | This message is dumped when the “Table0” sheet and “FSM0” sheet do not exist in the input Excel file.<br><br><excel>: the input Excel file. |
| 60 | Error | ERROR ::: Cannot run options above while "Table0" does not exist. | This message is dumped when users define “-tc \| -check” option or “-tv \| -ptn” option or “-ta \| assertion” option, but the “Table0” sheet does not exist in the input Excel file |
| 61 | Error | ERROR ::: Cannot run options above while "FSM0" does not exist. | This message is dumped when users define “-fsmc” option or “-fsmtv” option or “-fsmast” option, but the “FSM0” sheet does not exist in the input Excel file |
| 62 | Error | ERROR ::: Cannot run options above while "FSM0" has no data. | This message is dumped when users define “-fsmc” option or “-fsmtv” option or “-fsmast” option, but the “FSM0” sheet does not contain any data. |
| 63 | Error | ERROR ::: Please set Exclude sheet in <excel>. | This message is dumped when users define “-ex_ast” option, but the “Exclude” sheet does not exist in the input Excel file.<br><br><excel>: the input Excel file. |
| 64 | Error | ERROR ::: Checking the truth | This message is dumped when the Erakis cannot |

| No. | Severity | Message | Description |
|---|---|---|---|
| | | table(Lack) is missed. | check the truth table lacks or not, because there is an error related to open/create output lack log file. |
| 65 | Error | ERROR ::: Checking the truth table(Overlap) is missed. | This message is dumped when the Erakis cannot check the truth table has overlapped pattern or not, because of error related to open/create output overlap log file. |
| 66 | Error | ERROR ::: Making testbench is missed. | This message is dumped when the Erakis cannot generate test bench file because of error related to open/create file. |
| 67 | Error | ERROR ::: Making test vector is missed. | This message is dumped when the Erakis cannot generate test vector file because of error related to open/create file. |
| 68 | Error | ERROR ::: Making assertion for exclude input is missed. | This message is dumped when the Erakis cannot generate assertion file for prohibited input because of error related to open/create file. |
| 69 | Error | ERROR ::: Making execution shell script for <script_name> is missed. | This message is dumped when the Erakis cannot generate shell script file because of error related to open/create file.<br><br><script_name>: “VCS” or “incisive” |
| 70 | Error | ERROR ::: <excel> is not found. | This message is dumped when the input Excel file can not be found.<br><br><excel>: the input Excel file. |
| 71 | Error | ERROR ::: "<sheet_name>" is not found in "<excel>” | This message is dumped when a sheet is not found in the input Excel file.<br><br><sheet_name>: the not found sheet.<br><excel>: the input Excel file. |
| 72 | Error | ERROR ::: Cannot open temporary table.log file. | This message is dumped when Erakis cannot open the temporary file. This temporary file is an input of Haskell script to check lack pattern. |
| 73 | Warning | WARNING ::: <tag_name> will be ignored. | This message is dumped when users define a tag which is not included in supported tags.<br><br><tag_name>: the invalid tag |
| 74 | Warning | "WARNING ::: State "<state>" is not transited from others. | This message is dumped when a state is not transited from other in the State transition table.<br><br><state>: the state name. |
| 75 | Warning | "WARNING ::: State "<state>" transits to itself. | This message is dumped when a state transits to itseft *(source state)* in the State transition table.<br><br><state>: the state name. |
| 76 | Warning | WARNING ::: State "<state>" does NOT transit to other state. | This message is dumped when a state does not transit to other state in the State transition table.<br><br><state>: the state name. |
| 77 | Warning | WARNING ::: Directory "<out_dir>" already exist. If output file's name is same, the files will be overwritten. | This message is dumped when the output directory has already existed. |

| No. | Severity | Message | Description |
|---|---|---|---|
| | | | <out_dir>: the output directory. |
| 78 | Warning | WARNING ::: The truth table's lack patterns output X.<br>And total assertions is <estimated_lack_ast>.<br>Is it really all right? | This message is dumped when users define “-cpl” option.<br><br><estimated_lack_ast>: the estimated assertions need to add. |
| 79 | Warning | WARNING ::: Making testbench is stopped because the truth table <miss>. | This message is dumped when users define “-tb \| -testbench” option, but the truth table has overlapped or lack pattern.<br><br><miss>: “is lacked” or “has overlap”. |
| 80 | Warning | WARNING ::: Making test vector is stopped because the truth table <miss>. | This message is dumped when users define “-tv \| -ptn” option, but the truth table has overlapped or lack pattern.<br><br><miss>: “is lacked” or “has overlap”. |
| 81 | Warning | WARNING ::: Making assertion for exclude input is stopped because the truth table <miss>. | This message is dumped when users define “-ex_ast” option, but the truth table has overlapped or lack pattern.<br><br><miss>: “is lacked” or “has overlap”. |
| 82 | Warning | WARNING ::: Making execution shell script is stopped because the truth table <miss>. | This message is dumped when users define “-vcs” option or “-irun \| -incisive” option or “-ams” option, but the truth table has overlapped or lack pattern.<br><br><miss>: “is lacked” or “has overlap”. |
| 83 | Info | *** Fix all ERROR above before generating test patterns and assertions for FSM. | This message is dumped when there is error in FSM tables. |
| 84 | Info | # Check the Truth Table # | This message is dumped when users define “-tc \| -check” to check truth table. |
| 85 | Info | ***Complete to check the truth table - Truth table no overlap! | This message is dumped when the Erakis checks that there is no overlapped in truth table. |
| 86 | Info | *** Now checking for lack. Please wait a few minutes. | This message is dumped when the Erakis starts checking whether truth table lacks pattern or not. |
| 87 | Info | "***Complete to check the truth table - Truth table no lack! | This message is dumped when the Erakis checks that there is no lack pattern in truth table. |
| 88 | Info | ***Complete to check the truth table - Truth table has lack:<br>- <out_dir>/<lack_log>. | This message is dumped when the Erakis checks that there is lack pattern in truth table.<br><br><out_dir>: the output directory.<br><lack_log>: the lack log file name. |
| 89 | Info | ***Complete to check the truth table - Truth table has overlap:<br>- <out_dir>/<overlap_log>. | This message is dumped when the Erakis checks that there is overlapped pattern in truth table.<br><br><out_dir>: the output directory.<br><overlap_log>: the overlap log file name. |
| 90 | Info | # Making Testbench # | This message is dumped when users define “-tb \| -testbench” option to generate test bench file. |
| 91 | Info | ***Complete to make testbench file :<br>- <out_dir>/<tb_file>. | This message is dumped when the Erakis finishes generating test bench file. |

| No. | Severity | Message | Description |
| --- | --- | --- | --- |
| | | - <out_dir>/AmsTop.vams | <out_dir>: the output directory.<br><tb_file>: the file name of test bench. |
| 92 | Info | # Making Test Vector # | This message is dumped when users define “-tv \| -ptn” option to generate test vector file. |
| 93 | Info | ***Complete to make test vector file :<br>- <out_dir>/<ptn_file>. | This message is dumped when the Erakis finishes generating test vector file.<br><br><out_dir>: the output directory.<br><ptn_file>: the file name of test vector. |
| 94 | Info | # Making Assertion for exclude input # | This message is dumped when users define “-ex_ast” option to generate assertion file for prohibited input. |
| 95 | Info | ***Complete to make assertion file for exclude input :<br>- <out_dir>/<exclude_in>. | This message is dumped when the Erakis finishes generating assertion file for prohibited input.<br><br><out_dir>: the output directory.<br><exclude_in>: the file name of assertion file for prohibited input. |
| 96 | Info | ***Complete to make FSM test vectors file :<br>- <out_dir>/<FSM_tv> | This message is dumped when the Erakis finishes generating test vector file for FSM.<br><br><out_dir>: the output directory.<br><FSM_tv>: the name of test vector file for FSM. |
| 97 | Info | ***Complete to make FSM assertions file :<br>- <out_dir>/<FSM_ast> | This message is dumped when the Erakis finishes generating assertion file for FSM.<br><br><out_dir>: the output directory.<br><FSM_ast>: the name of assertion file for FSM. |
| 98 | Info | # Making Execution shell script for <script_name> # | This message is dumped when users define “-vcs” option or “-irun \| -incisive” option or “-ams” option.<br><br><script_name>: “VCS” or “incisive”. |
| 99 | Info | ***Complete to make execution shell script file for <script_name> : | This message is dumped when the Erakis finishes generating script.<br><br><script_name>: “VCS” or “incisive”. |

(2) Help message:

*Table 6.2: help message of the Erakis tool*

| **Condition** | This message is dumped when users define “-h \| -help” option. |
|---|---|

```
info :  $ENV{'ERAKIS_VER'}
  Usage:  erks [Excel File] [OPTION]...
  OPTION details
    -err               : Set max error number which checked.(-1:Output all error)
    -ex_ast            : Make assertion file with \"Exclude\" sheet.(check input)
    -h | -help         : Reference help.
    -p | -pcheck       : Make test vector a part of truth table.
    -pg                : Use when verilog model with pg.
    -tc | -check       : Execute to check truth table.
    -tv | -ptn         : Execute to make test vector.
    -tb | -testbench   : Execute to make testbench.
    -ta | -assert      : Execute to make assertion file.
    -ts | -timescale   : Set timescale number. ex) 1ps/1ps.
    -vcs               : Make shell file which execute VCS.
    -irun | -insicive  : Make shell file which execute Insicive.
    -fsdb              : FSDB for output wave file format.
    -ams               : Excution irun command with circuit.(wave type : psf)
    -vpd               : VPD for output wave file format.
    -nowave            : No wave output(default is nowave).
    -compression | -cr : Port allows \"*\".(unrecommend option)
    -cpl               : Control generating assertions for all lack patterns (not use
  with -tc| -check option)
    -fsmc              : Execute to check tables related to FSM.)
    -fsmtv             : Execute to make test vectors for FSM.
    -fsmast            : Execute to make assertions for FSM.

  Exit states:
  0 : OK,
  1 : ERROR(Detail is check to standard output).
```

# 7.Limitation

This section list limitations of the current version of the Erakis tool. Not only the current limitations but also the suggestions/solutions are described.

These information can be used for improvement in next phase. Details are below.

**(1) Limitation about check duplicated option for -err option and -ts | -timescale option.**

(1.1) Current:

Checking duplicated define option applied only in -err option and -ts | -timescale option. However the message “ERROR ::: Cannot define \"$opt\" option more than twice” is not correct.

(1.2) Suggestion:

In next phase of Erakis, this message is recommended to be revised to “ERROR ::: Cannot define option “<option_name>” more than one time.”.

And check duplicated for all options.

**(2) Limitation about unifying message when check duplicated option.**

(2.1) Current:

When checking duplicated option, the message for -err option and -ts | -timescale option is “ERROR ::: Cannot define \"$opt\" option more than twice”. But the message for -cpl option is “ERROR ::: Not duplicate -cpl option.”. They are different.

(2.2) Suggestion:

In next phase of Erakis, unify these message to “ERROR ::: Cannot define \"$opt\" option more than one time.”.

**(3) Limitation about dumping oscillation port in assertion file.**

(3.1) Current:

The oscillation port is dumped in assertion file of truth table.

(3.2) Suggestion:

In next phase of Erakis, when generating assertion file for truth table or FSM, Erakis check whether a port is an oscillation port or not. The Erakis does not dumps code to check oscillation port in assertion file.

**(4) Limitation about warning message may be dumped to screen by Perl compiler.**

(4.1) Current:

Some message as format: “Use of uninitialized value in string ne at FILE line N.”

In this, FILE is the Perl file; N is the line number in file.

(4.2) Solution:

Users checking whether blank cells in the input Excel file is recommended.

| Revision History | | | | | |
|---|---|---|---|---|---|
| **Rev.** | **Modified Contents** | **Agreed by Customer** | **Approved by RVC** | **Checked** | **Created** |
| 1.0 | - Create new. | | Vu Pham 03/31/2015 | Duc Duong 03/31/2015 | Chan Le 03/31/2015 |
| 1.1 | - Table 3.2, change default value of tag “lib_name” to “verilog” to none.<br>- Table 3.3:<br>+ tag “cell” and "lib_name" to "view_name" 's default column is "-"<br>+ tag "pref_unit"'s default column is "MHz"<br>+ tag "exclude_in"'s default column is "ex_ast_test.sv".<br>- Table 3.4, option "-ams" is correct "-ams -irun".<br>- Table 3.5:<br>+about D/A, default is none;<br>+about SA, revise from “voltage” to “signal amplitude”.<br>+about care range, add describe about meaning of “-”, “x”, “z”, and valid format of oscillation port's care range.<br>- Table 3.8:<br>+ revise the caption name from “Table0” to “Exclude”.<br>+ remove pcheck column, output column.<br>- Revise the note of pcheck column in Exclude sheet to “pcheck column is for Table0 only”. | N.Konishi 04/02/2015 | Vu Pham 04/02/2015 | Hong Lam 04/02/2015 | Chan Le 04/02/2015 |
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