MOS Device: Basics

- MOSFET & Modeling -

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Lecture 2

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(4) How many types of Devices on LSI ?

So far, we learned "Semiconductor Physics", it's a basic knowledge to understand Devices.

- How many free electrons in semiconductor material
- How fast the electron moves in the semiconductor material

Now we start learning "Semiconductor Devices".

Typical device used in LSI is categorized with:

- Two terminal Devices: Diode
- Three terminal Devices: Transistor

Diode: we have "PN-Diode" and "MOS-Diode".

Transistor: we have:

"MOSFET; Metal Oxide Semiconductor Field Effect Transistor"

"BJT; Bipolar Junction Transistor"

We will learn the operation of "PN-Diode", "MOS-Diode" and "MOSFET".

Note on LSI:
words of IC and SSI-ULSI, the integration level

IC: Integrated Circuit is general term to express chips in which many circuits are integrated on a single die

SSI ~ ULSI can be used to distinguish integration level of the chip, however it is troublesome for engineers

Therefore, many people simply use term "LSI" for all the relatively large integrated chips (say >1K components)

In my case, I use the term of "IC", if I want to describe the small integrated chips intentionally such as RF-IC

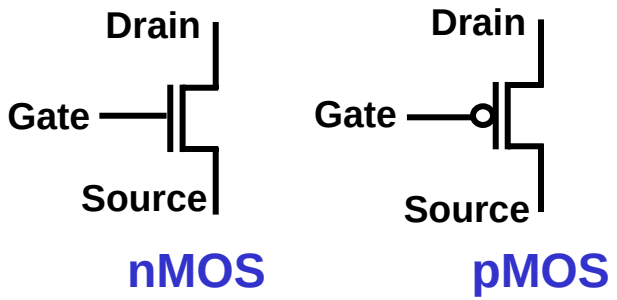
Continued:
General definition on the Integration level and notation

SSI,	Small Scale IC,	# of component=2-100
MSI,	Middle Scale IC,	# of component=100-1000
LSI,	Large Scale IC,	# of component=1000-100K
VLSI,	Very Large Scale IC,	# of component=100K-10M
ULSI,	Ultra Large Scale IC,	# of component= >10M

Symbols of Devices Used in LSI

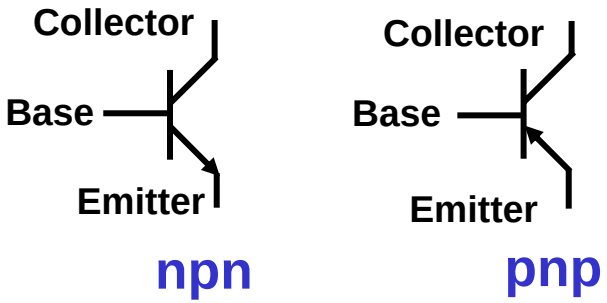
○ MOS Transistor (MOSFET)

Broadly used owing to the properties of high-speed, low-voltage, and high-integration.



○ Bipolar Transistor (BJT)

Used in RF and analog applications owing to its high-driveability.

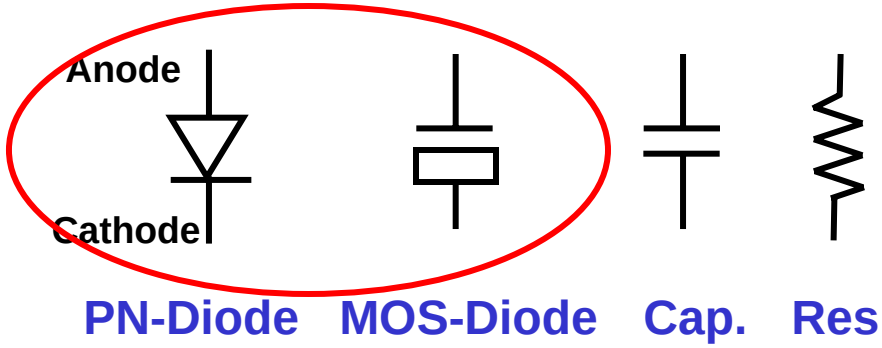


○ Diode & Other devices

PN-Diode, MOS-Diode

capacitors, resistors etc.

MOS: Metal Oxide Semiconductor



(4-1) PN-diode or PN-junction

Firstly, the **most important Device** is PN-diode, within many sophisticated semiconductor devices.

It gives Electrical Rectifier element by itself.

Also it is the basic element of BJT (Bipolar Junction Transistor) and IC, invented by Schockley and Noyce, respectively.

In MOSFET, it works as Device Isolation element in CMOS, which achieves updated Highly integrated LSI.

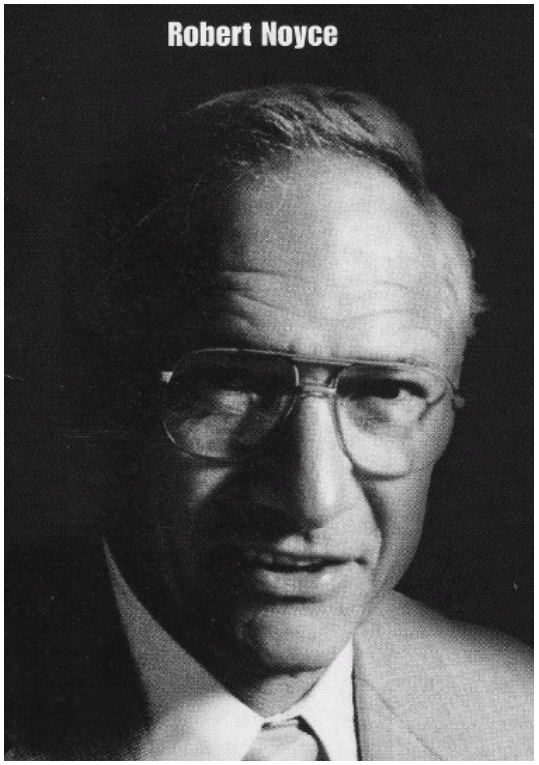
Again! …. IC: Integrated Circuit, LSI: Large Scale Integration

Historical BJT Integrated Circuit invention

Reprint of U.S. Patent 2,981,877 (Issued April 25, 1961. Filed July 30, 1959)

PN-diode, BJT and Resistors are integrated on a same material (chip).

This is done by using various PN-junctions on chip!



Fairchild Co.

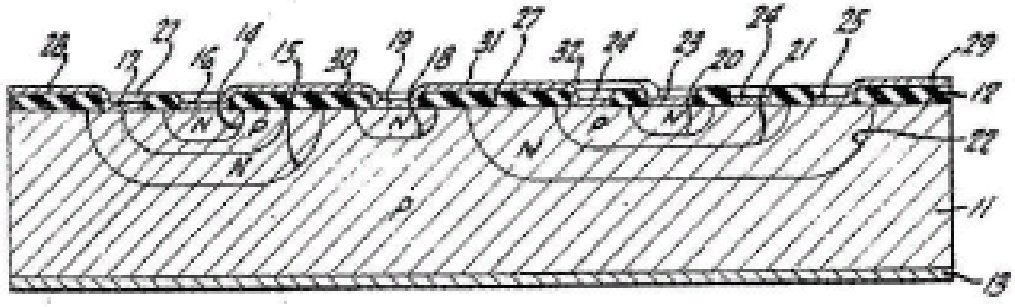


FIG-4

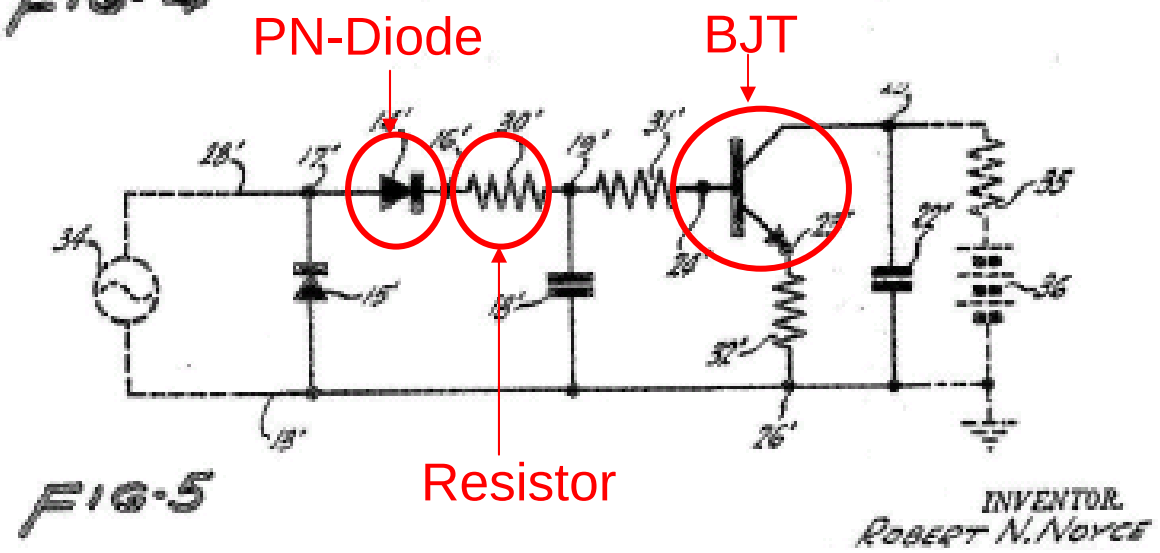
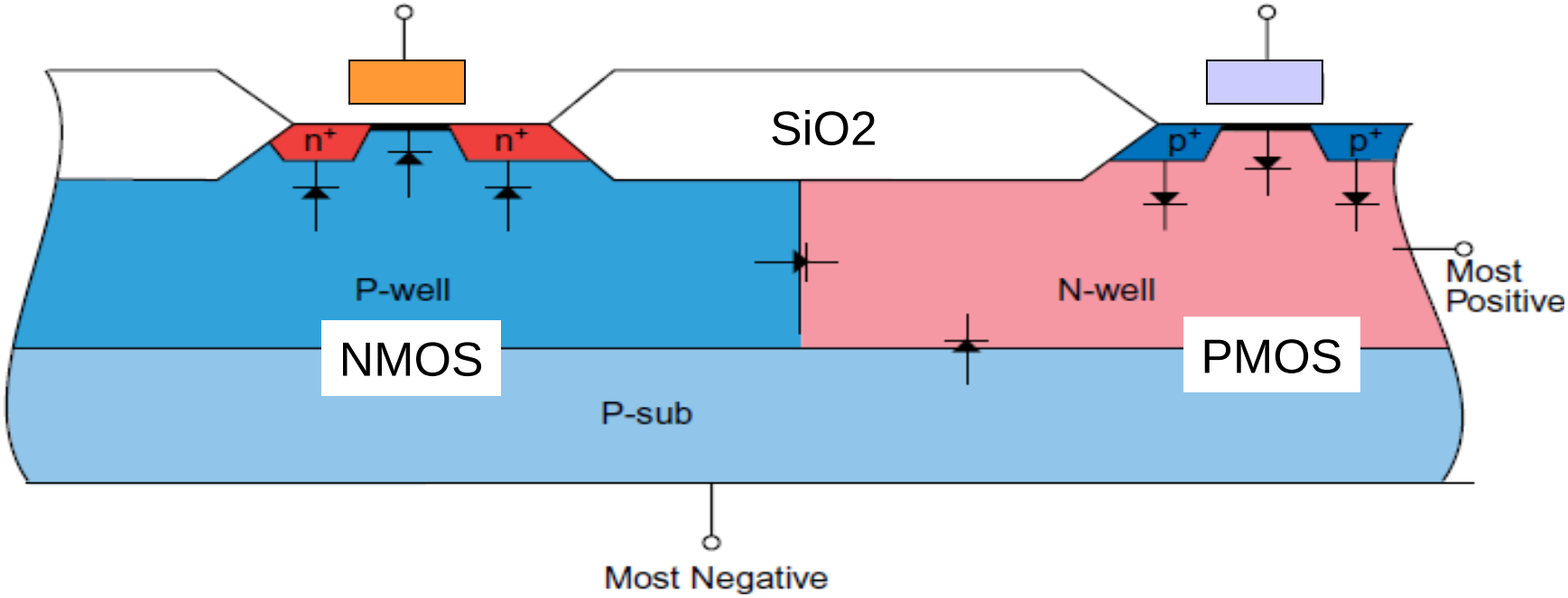


FIG-5

INVENTOR
ROBERT N. NOYCE

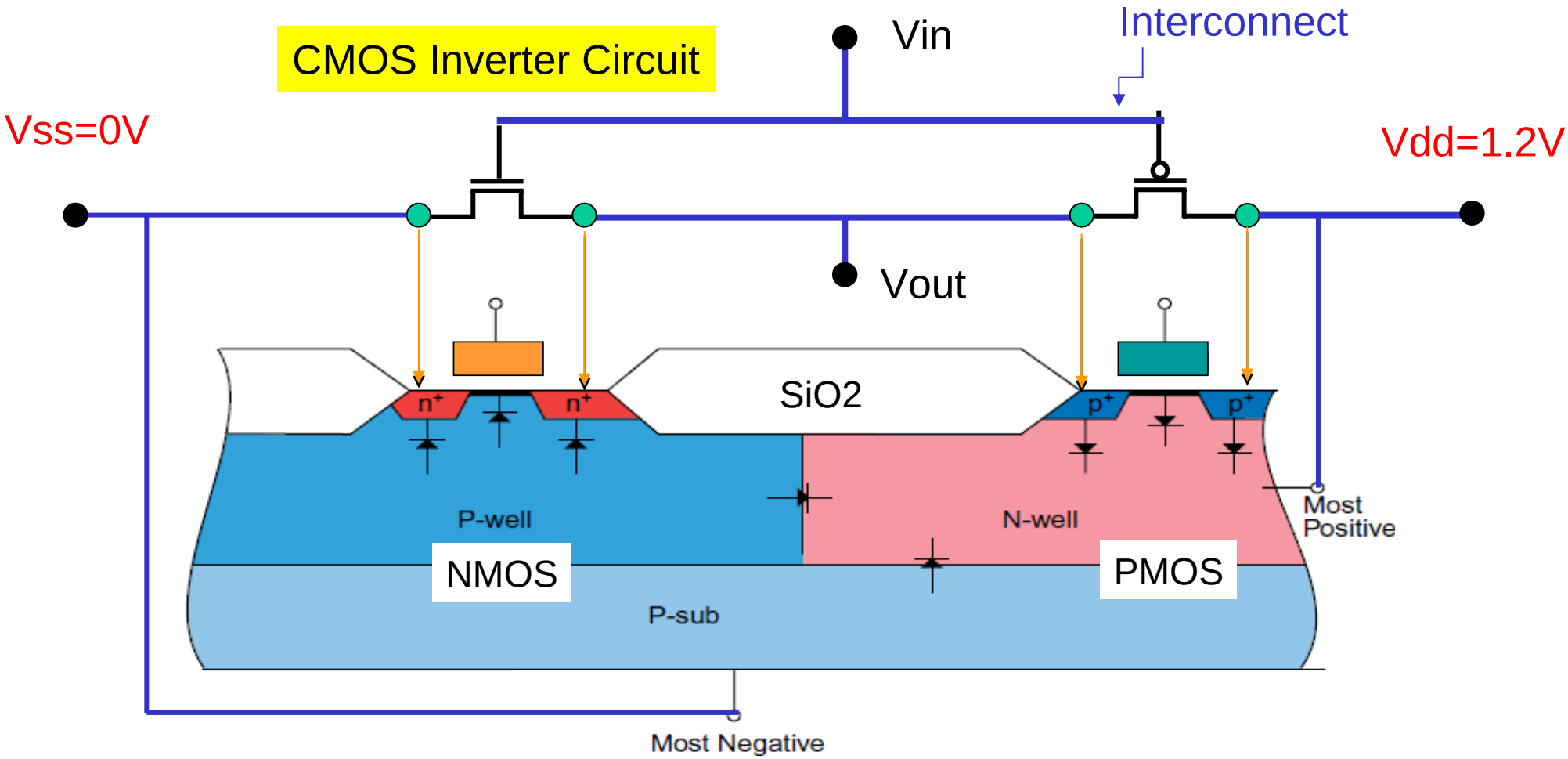
PN-diode is used for Electrical Isolation in CMOS Devices

PN-Diode works as Device Isolation structure in CMOS-LSI
It also used as Capacitor element.
Many PN-Diodes are un-intentionally formed in CMOS as shown below.



Quiz: Confirm all the PN-diodes are reverse biased ($V_P \leqq V_N$) in CMOS LSI!

Interconnects form a CMOS inverter circuit using NMOS and PMOS.



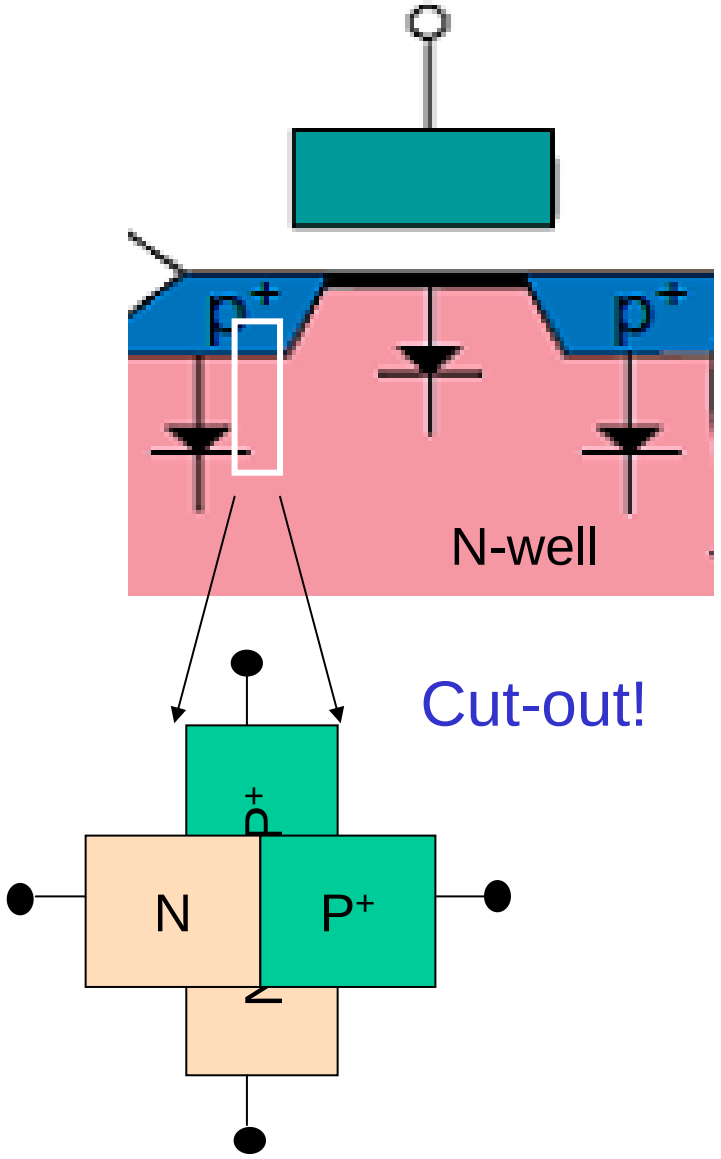
Electrostatics of PN-diode in equilibrium

Focus on intrinsic p+ and n- regions located in PMOS source diffusion.

Let's cut out a piece of P^+N junction

Then rotate it 90 degree to the right!

OK! How the PN-diode works?

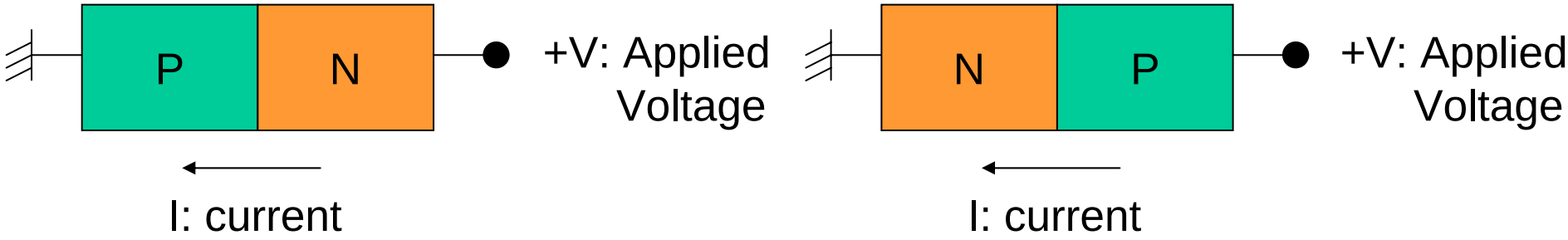


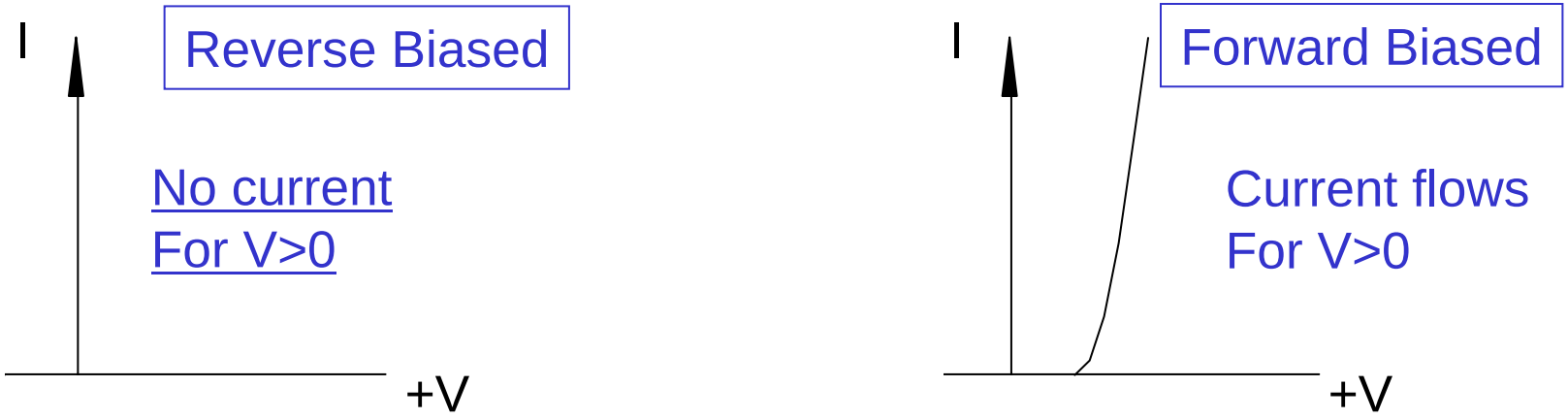
Current Flow through PN-Diode

PN-Diode allows the current flow only one direction, from P to N.

It forms electrical rectifier.

Note: In MOS-LSI, PN-Diodes are always “Reverse Biased” to electrically isolate NMOS and PMOS.





Characteristic Parameters in PN-Diode (In MOS-LSI, always Reverse Biased!)

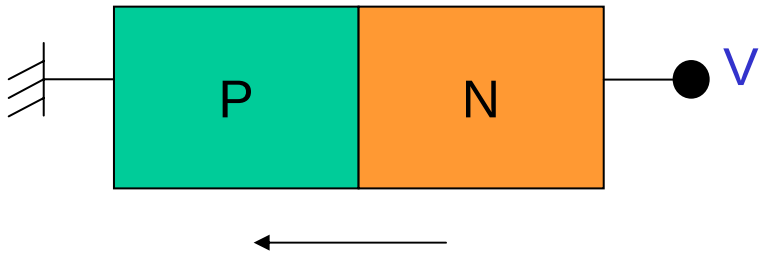
Important Parameters:

(1) Electrical
V: Applied Bias Voltage
I: Diode Leak Current
C: Capacitance

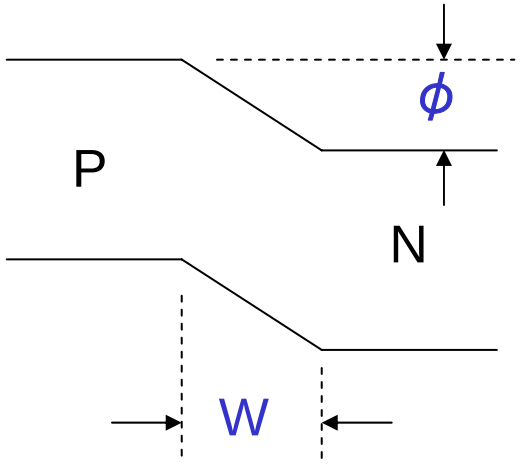
(2) Physical
ϕ : Potential Difference Between N & P
W: Depletion Width

$$C = \frac{\varepsilon_{Si}}{W} \qquad \varepsilon_{Si} : Permittivity\ of\ Silicon$$

Capacitance is a function of W;



(a) Physical Structure



(b) Band Structure

Bias dependency:
Equilibrium, Reverse bias, Forward bias

1) Equilibrium condition

$$\phi_{Bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Built-in voltage

$$W_{dep} = \sqrt{\frac{2\varepsilon_S}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}\ \sqrt{\phi_{Bi}}$$

$$\approx \sqrt{\frac{2\varepsilon_S}{qN_A}\phi_{Bi}}$$: In case of N^+P junction ($N_D >> N_A$)

2) Reverse bias condition

$$\phi = \phi_{Bi} + V_{(n)} > \phi_{Bi}$$: $V_{(n)} > 0$

In CMOS, always Reverse Biased

$$W_{dep} \approx \sqrt{\frac{2\varepsilon_S}{qN_A}(V_{(n)} + \phi_{Bi})}$$

$$I \approx \frac{qAni}{2\tau_o} W_{dep} \approx 0$$: Generation/Recombination Current

3) Forward bias condition

$$\phi = \phi_{Bi} + V_{(n)} < \phi_{Bi}$$: $V_{(n)} < 0$

$$W_{dep} \approx \sqrt{\frac{2\varepsilon_S}{qN_A}(V_{(n)} + \phi_{Bi})}$$

$$I_{diode} \approx I_o\left(e^{\frac{q}{kT}V} - 1\right)$$

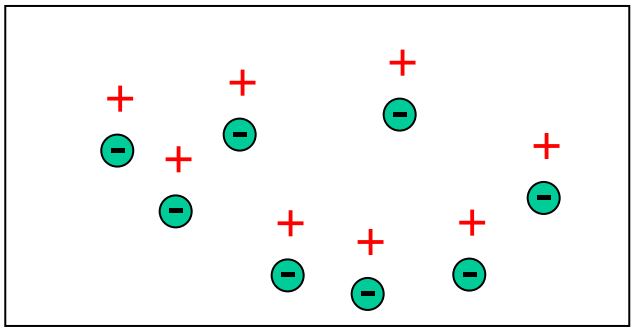
Show Time !

PN-Diode or PN-Junction :

Electrons and Holes in PN-diode
Movement of Electrons and Holes
Related Current Flow
Change of Depletion Layer Width

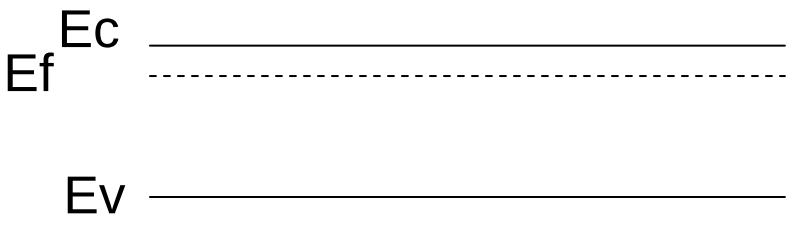
N-type silicon and P-type silicon

When donor ions are added to silicon, free electrons appear whose number is same as ionized donors (N-type Silicon). Then…
Fermi-level (Ef) is formed close to conduction band, as you know.



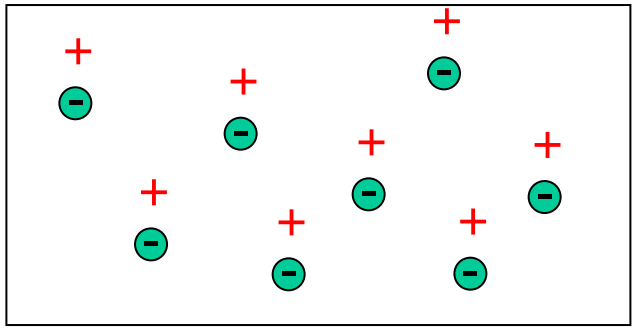
\+ Ionized Donor ion

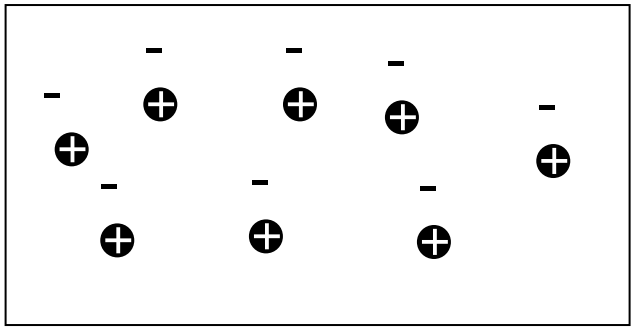
⊖ Free electron



N-type silicon and P-type silicon

When acceptor ions are added to different piece of silicon, holes are generated whose number is same as ionized acceptors (P-Type Silicon). Then Fermi level of P-type silicon is formed close to valence band.



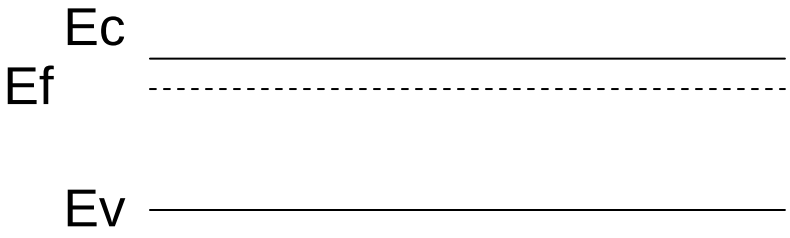


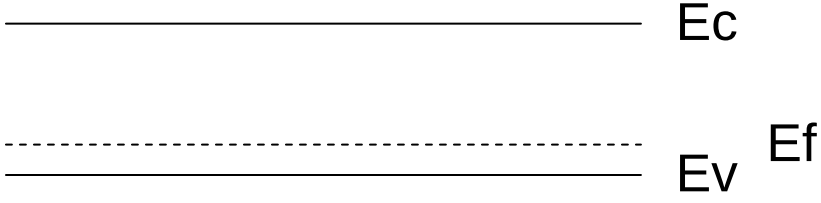
\+ Ionized Donor ion

⊖ Free Electron

\- Ionized Acceptor ion

⊕ Free Hole

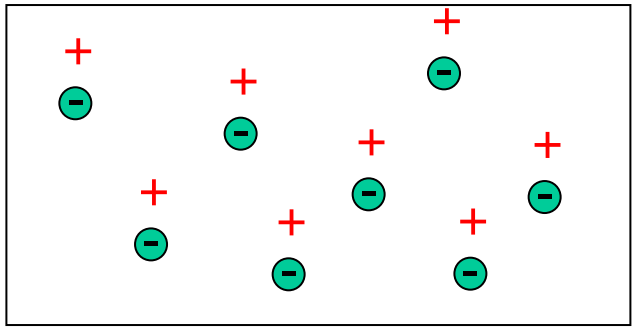




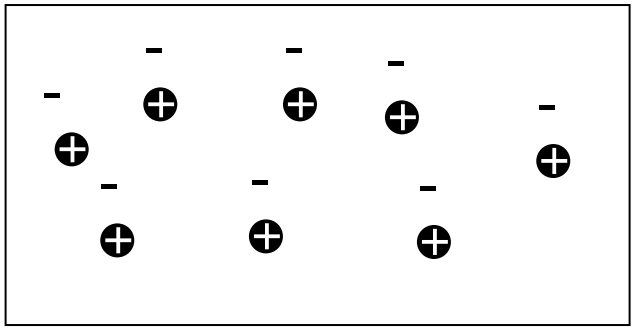
N-type silicon and P-type silicon

A lot of electrons in N-region.
A lot of holes at P-region.
Fermi-levels different! They needs to become equal @ equilibrium.

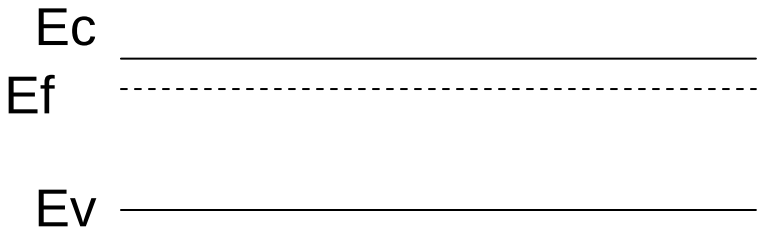
Let's combine these two semiconductors.

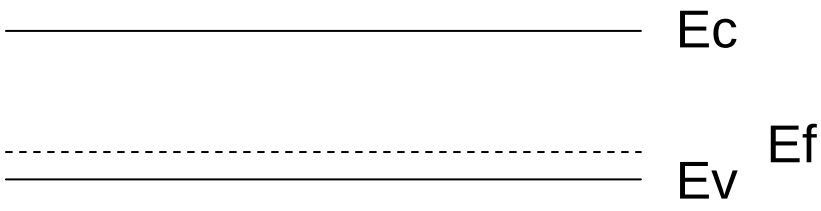


\+ Ionized Donor ion
⊖ Free Electron



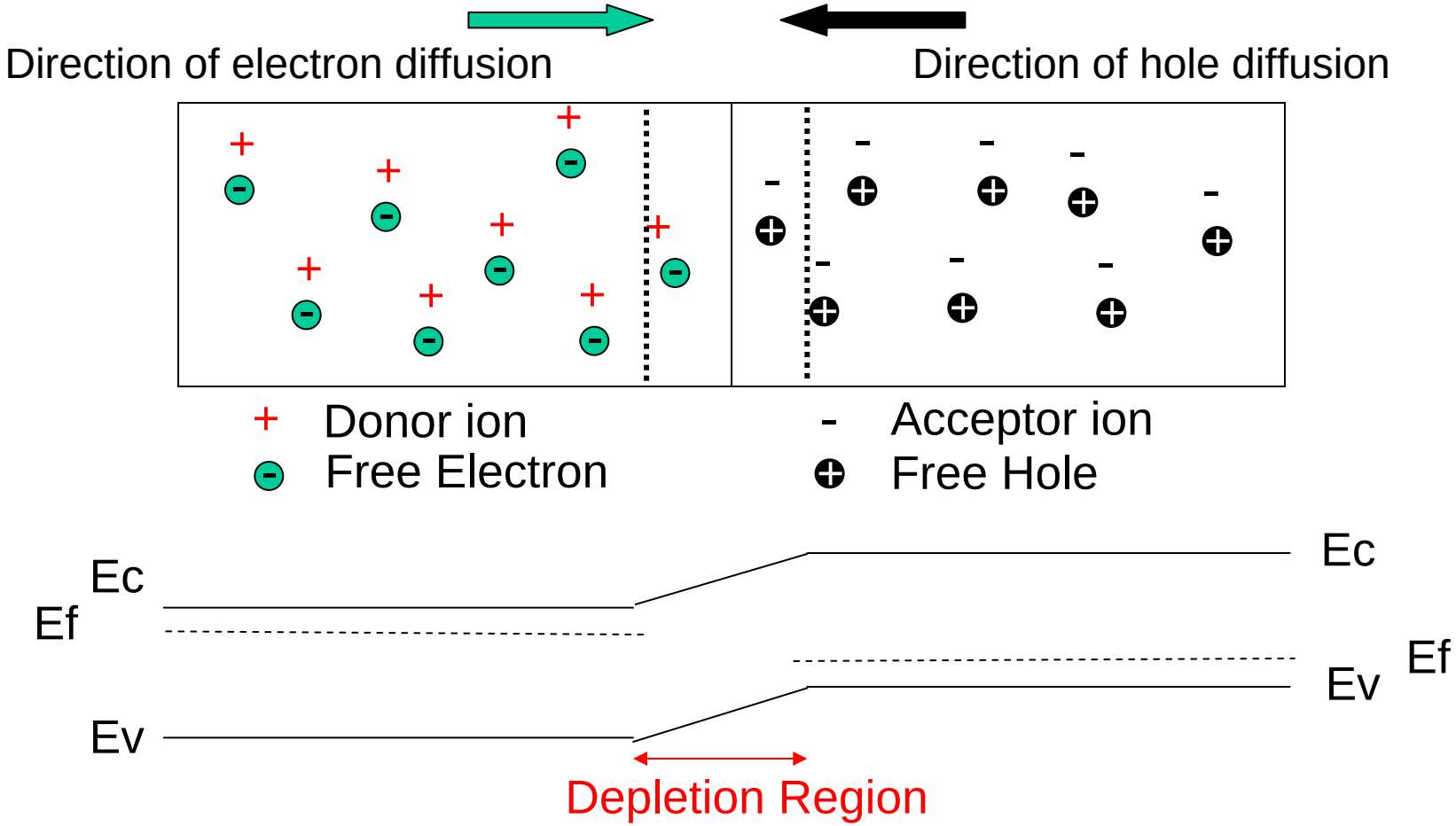
\- Ionized Acceptor ion
⊕ Free Hole





Depletion layer generation:

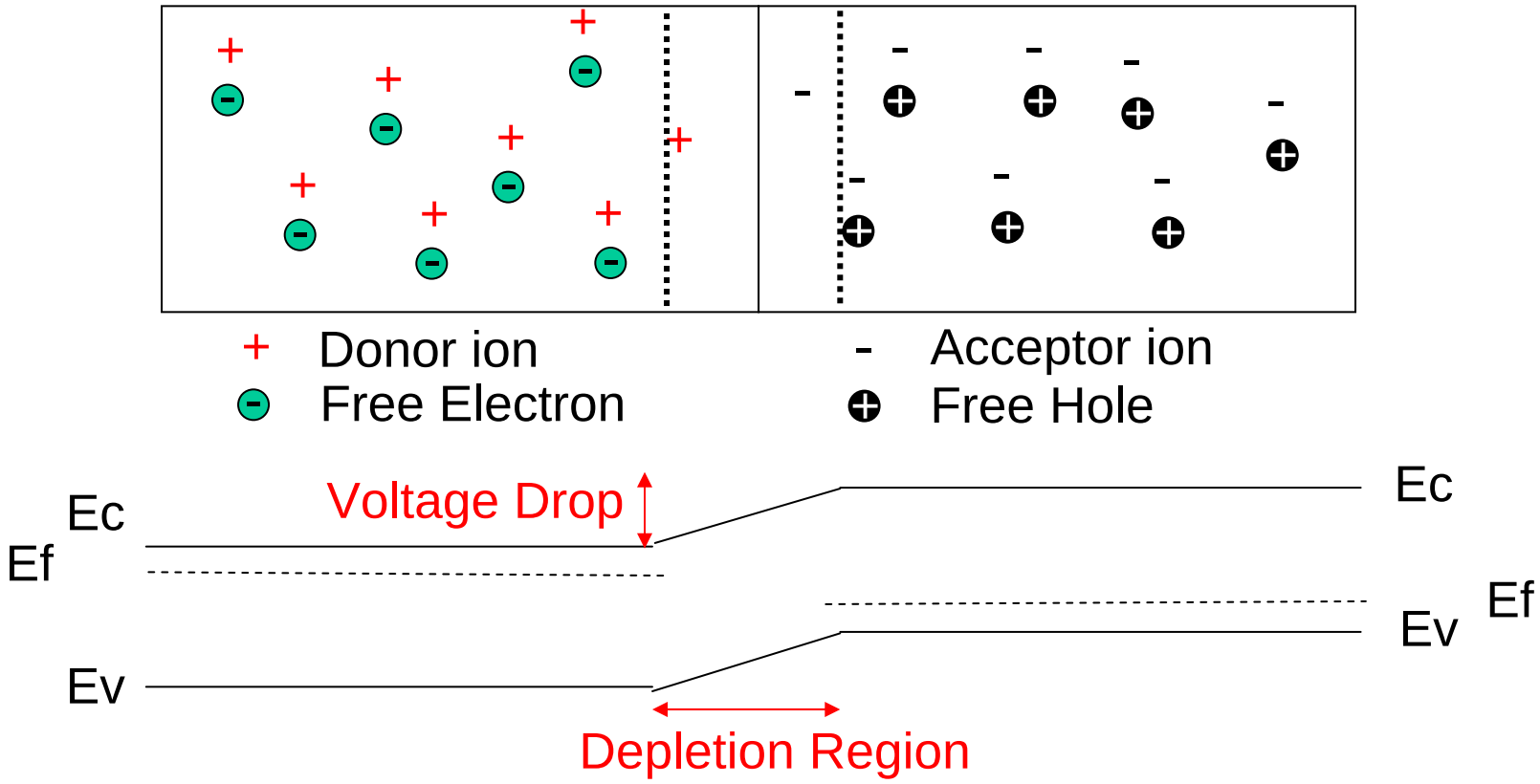
Excess electrons and holes cause self-diffusion to opposite region.
The two diffused carriers disappear when they meet together (recombination).
It generate a layer, where no carriers exist (depletion region).



Voltage drop is also generated:

In the depletion layer, fixed acceptor and donner ions are left behind.

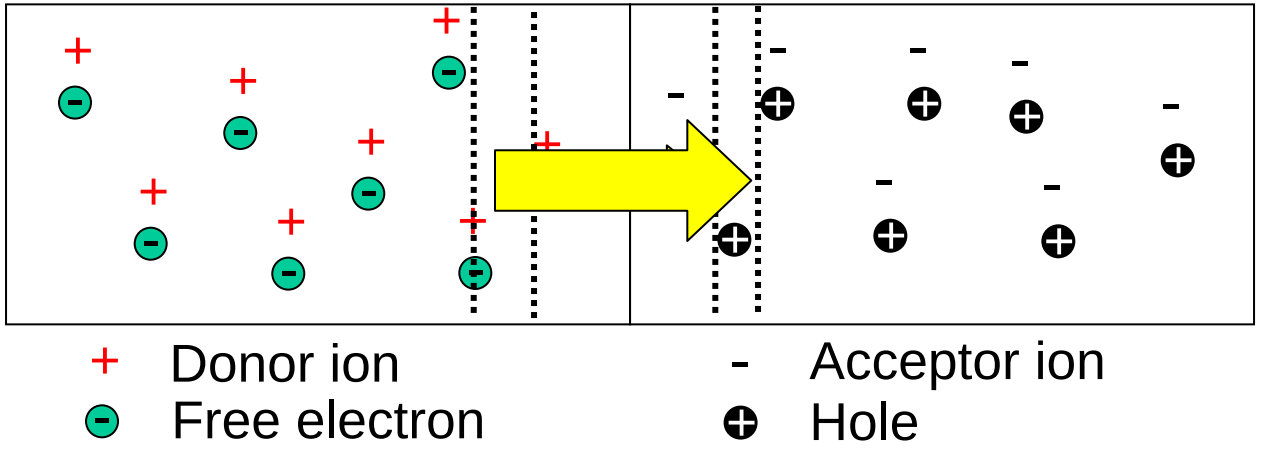
It create voltage drop between N- & P-type regions.

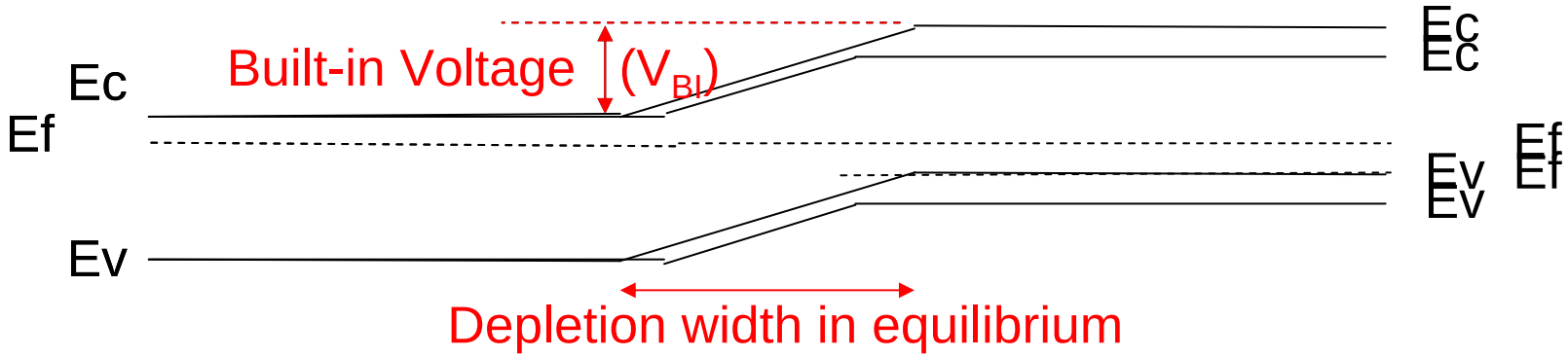


Further carrier diffusion until Equilibrium:

Electrons & holes continue to flow by diffusion, until the electric field becomes strong enough to prevent further diffusion.

It results in the increases of “depletion width” and “electric-field strength”.

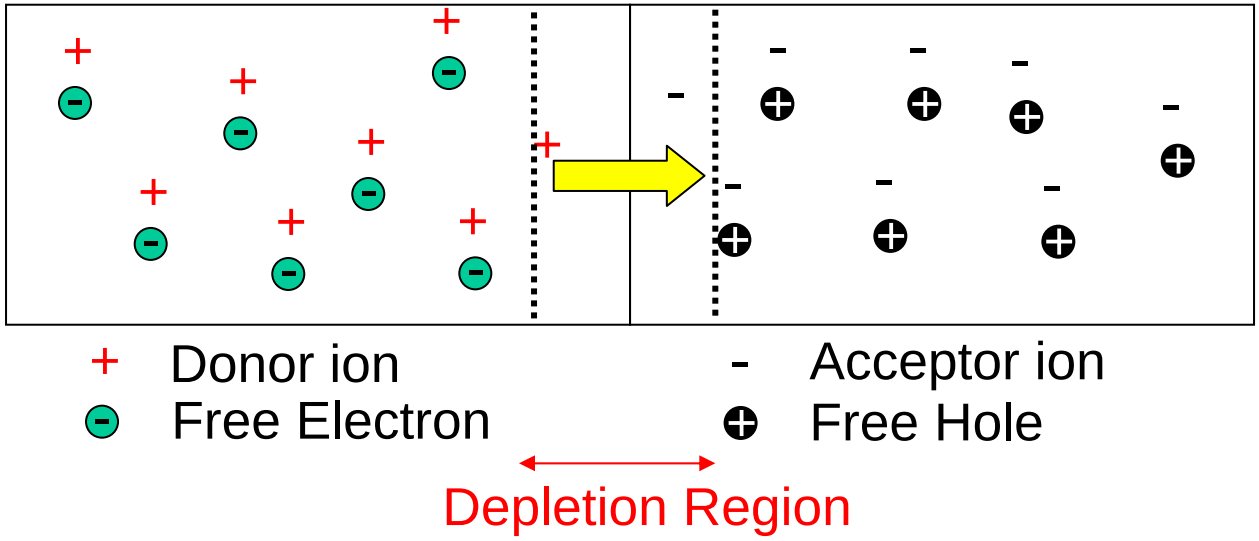




Quiz 1:

The voltage-drop across the depletion region, it generate “Electric-Field” inside of depletion layer, naturally.

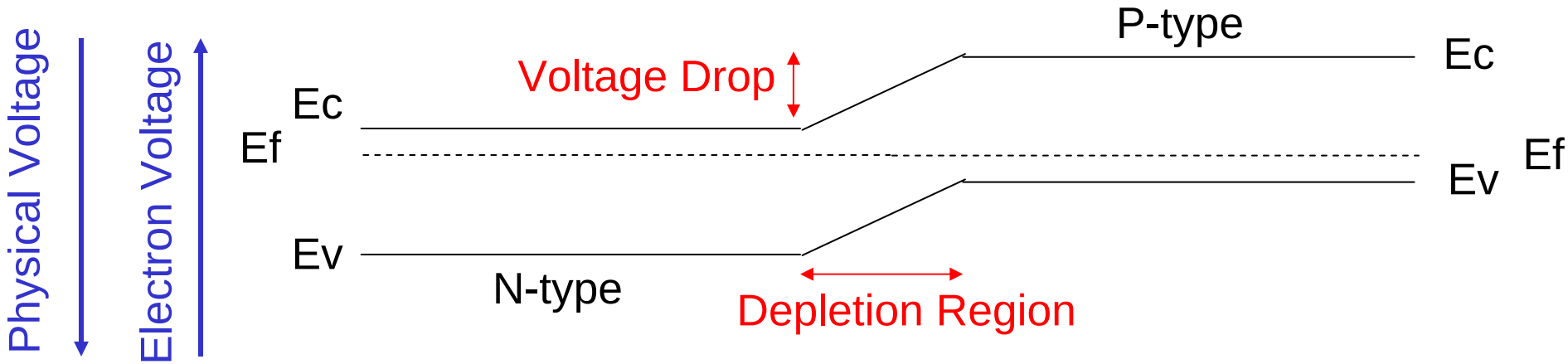
Question: Why no electric field exist in n-type and p-type silicon?



Answer: outside the depletion region, the number of impurity and carrier (ex. donors and electrons) are the same in number, therefore the total charge is zero. So there exists no electric field (neutral regions).

Quiz 2:

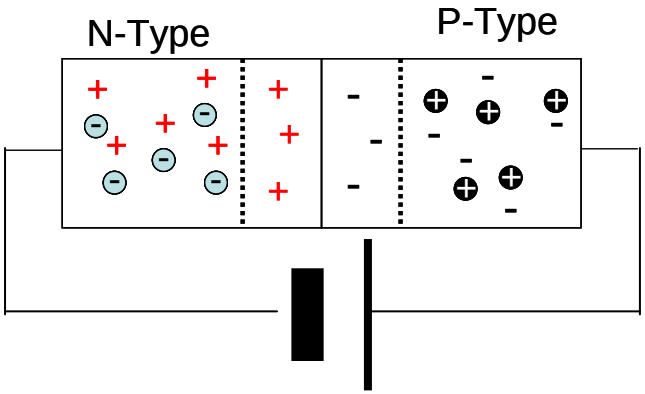
1. Silicon with Boron: n-type or p-type?
2. Silicon with Phospholous: n-type or p-type?
3. Silicon with Arsenic: n-type or p-type?
4. N-type impurity is called: Acceptor or Donner?
5. P-type impurity is called: Acceptor or Donner?
6. What is the name of voltage built between n- & p-type silicon?
7. Which is higher potential (voltage): n-type or p-type?



What happen when we put bias across the PN-diode?

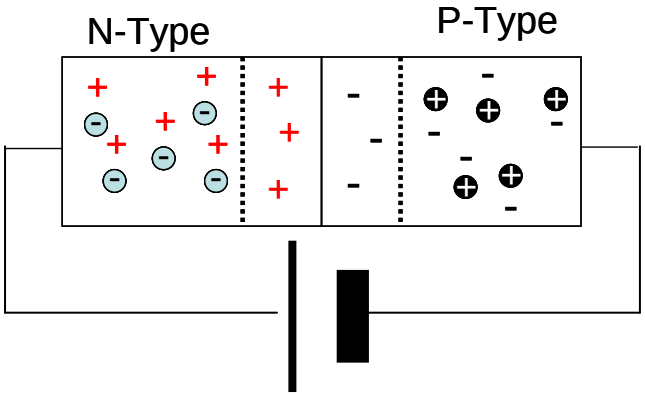
(1) Forward biasing:

Positive bias on P-type region on PN-diode

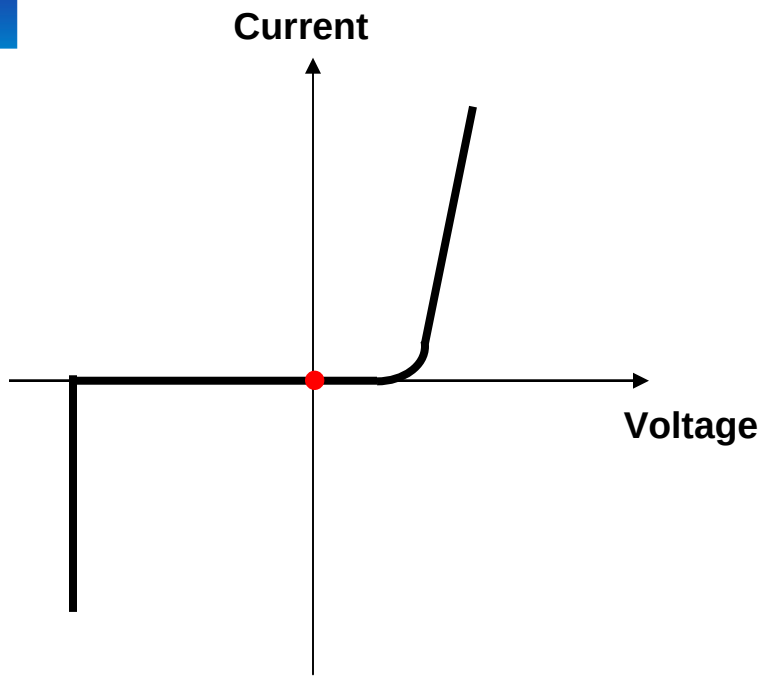


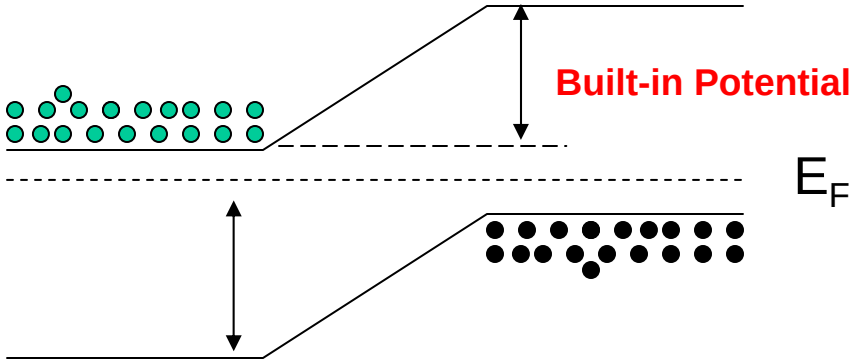
(2) Reverse biasing: ··· Important in CMOS LSI

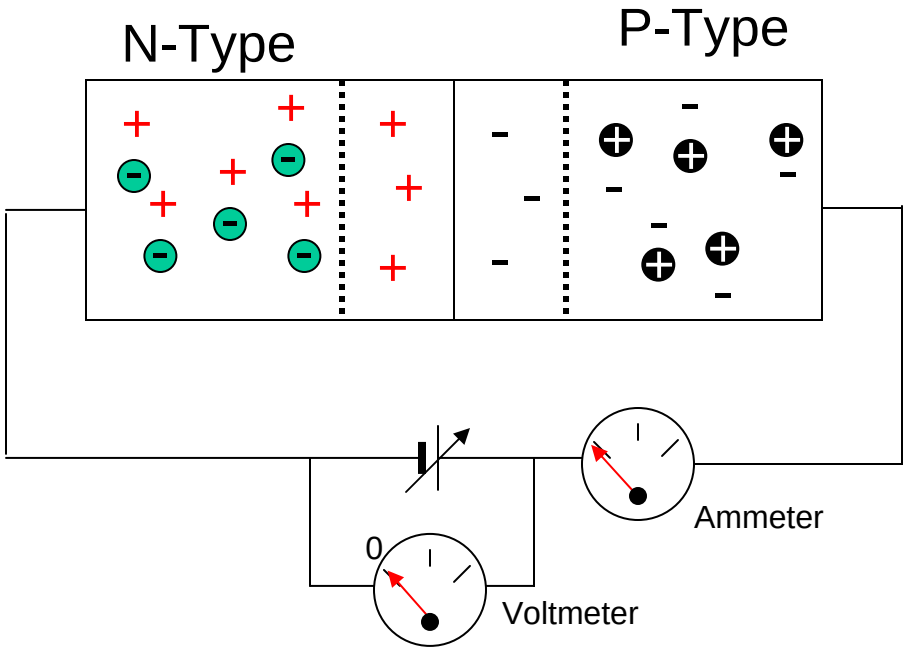
Negative bias on P-type region on PN-diode



PN-Diode at no-bias (V=0V)



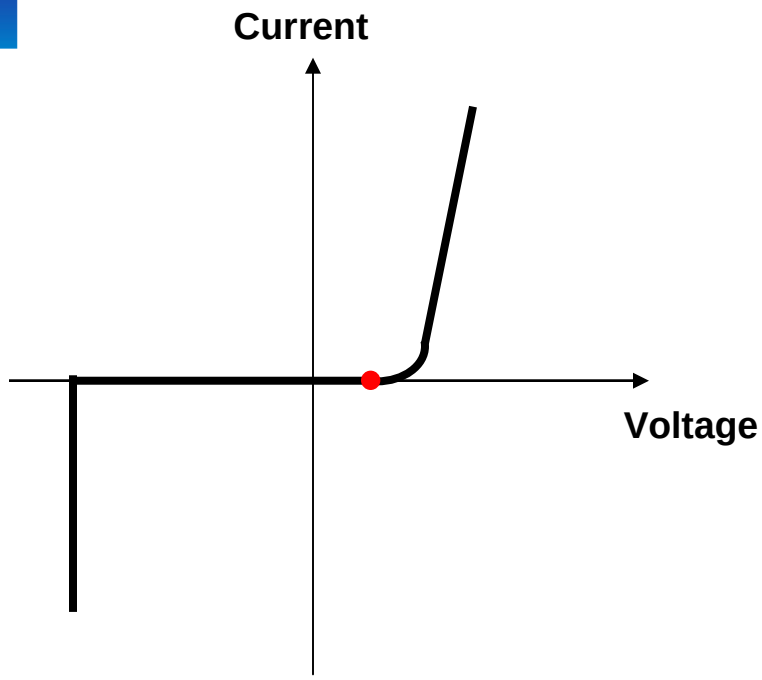


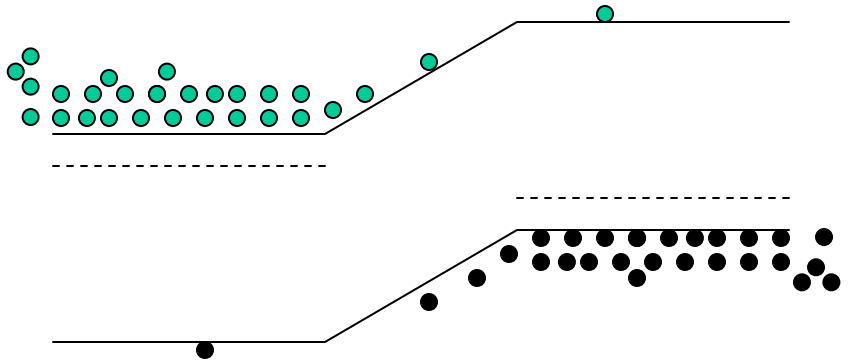


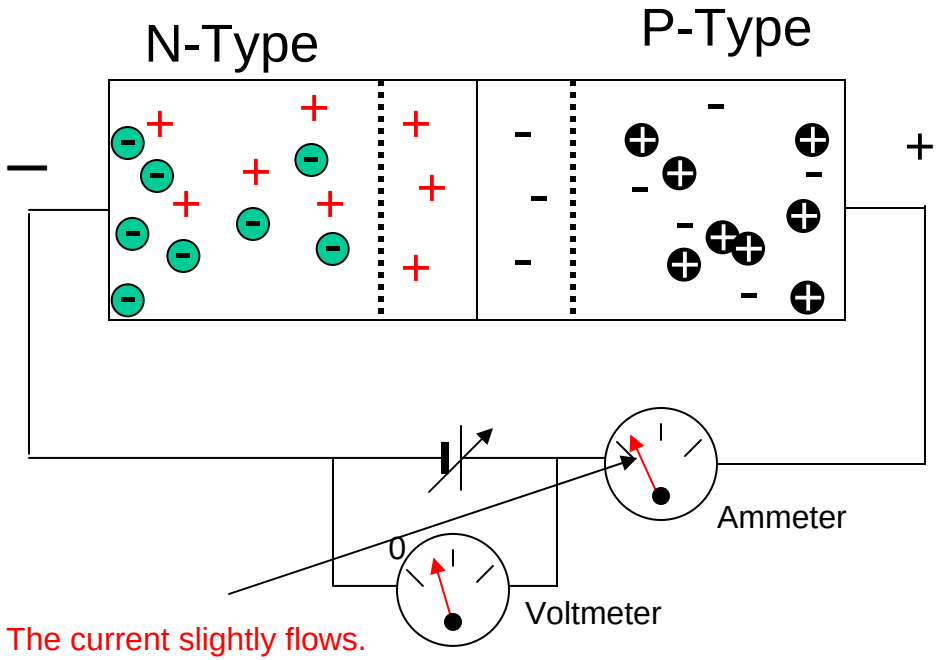
Now, in no-bias (V=0V); it is in thermal equilibrium condition

- Fermi energy level (E_F) is flat across PN-diode
- No current flows

PN Diode forward biasing ($0<V<V_{BI}$)



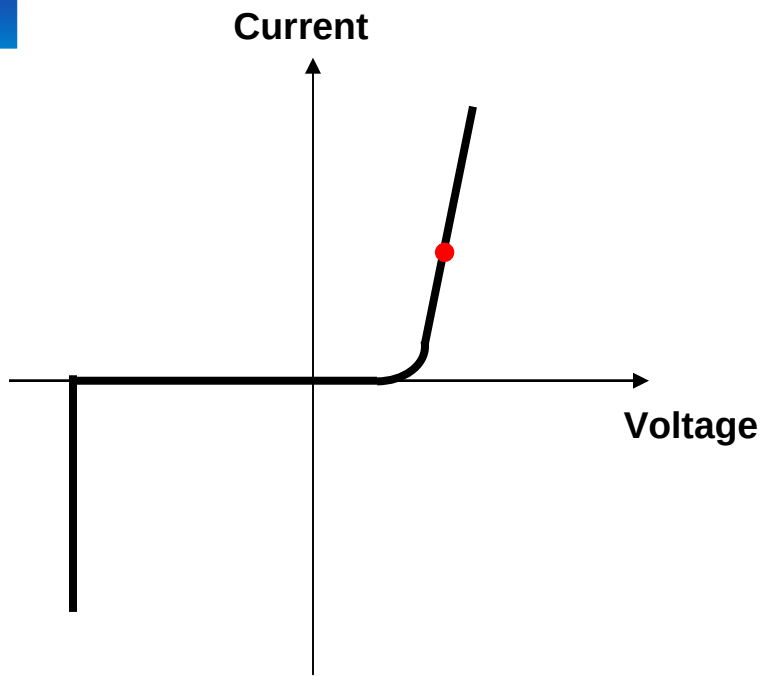


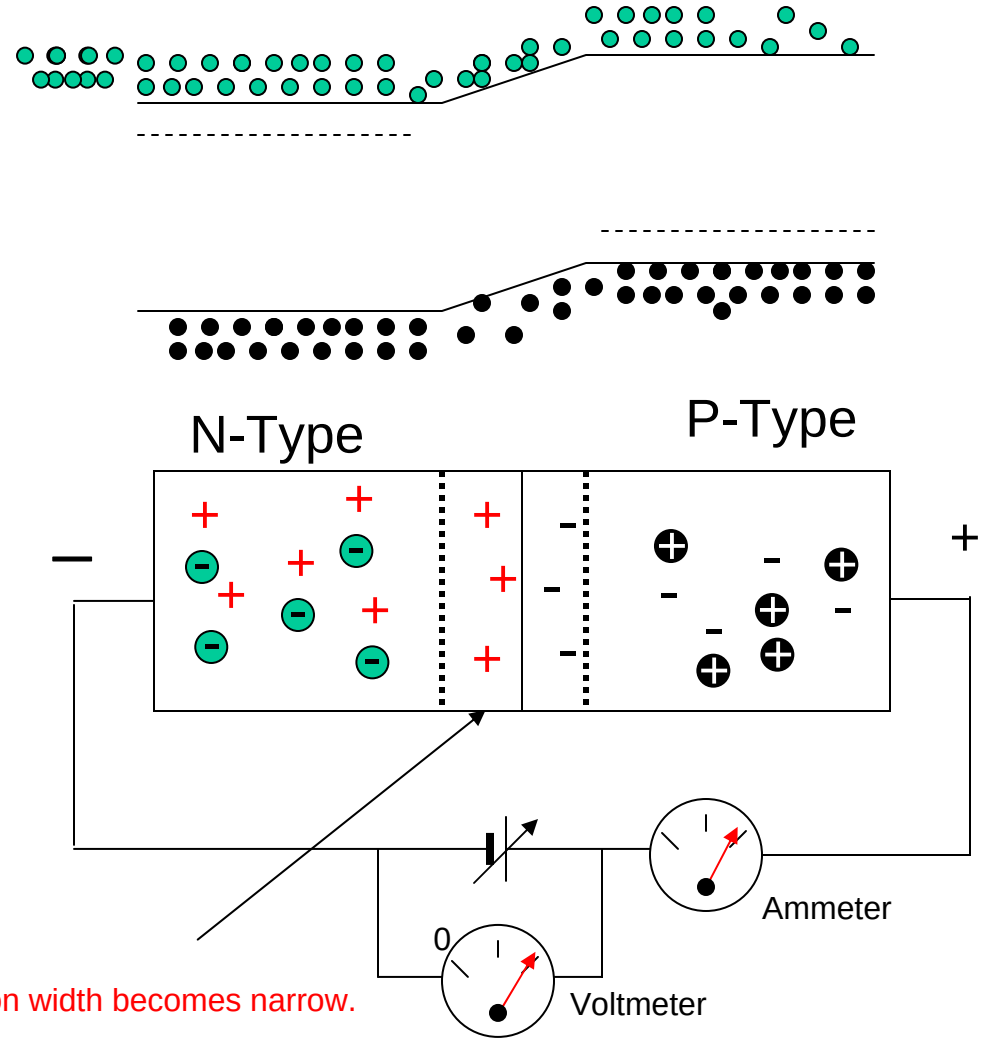


When forward biased, voltage barrier is reduced. So electron and hole start diffuse.

It results in small current flow across the PN-diode.

PN Diode forward biasing ($V_{BI} \leqq V$)



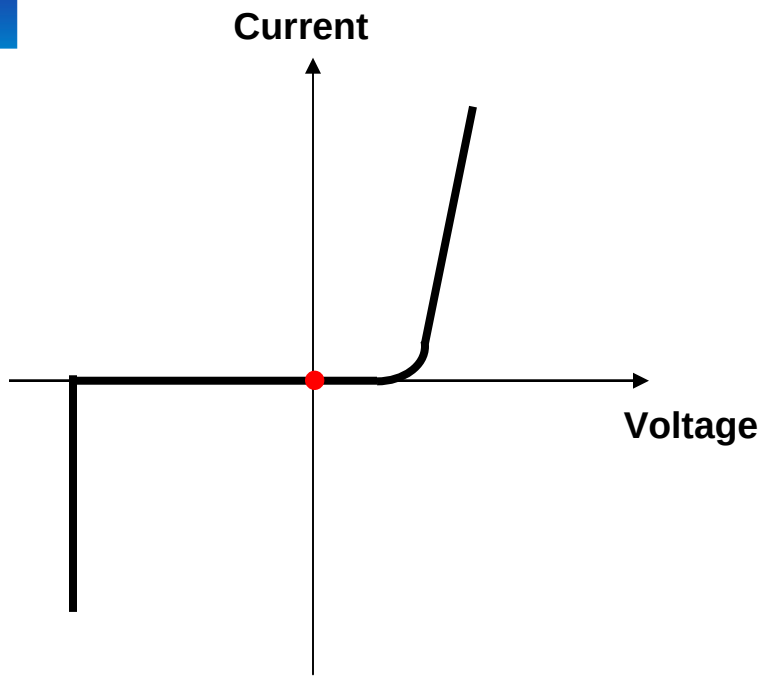


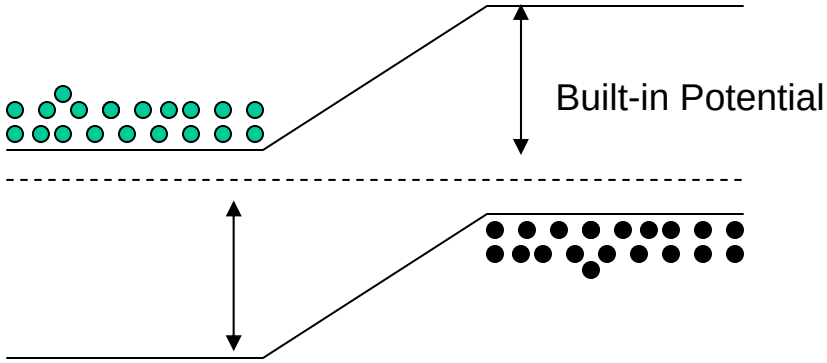
Further increase of bias close to Built-in voltage (V_{BI}), exponential rise of current is obtained.

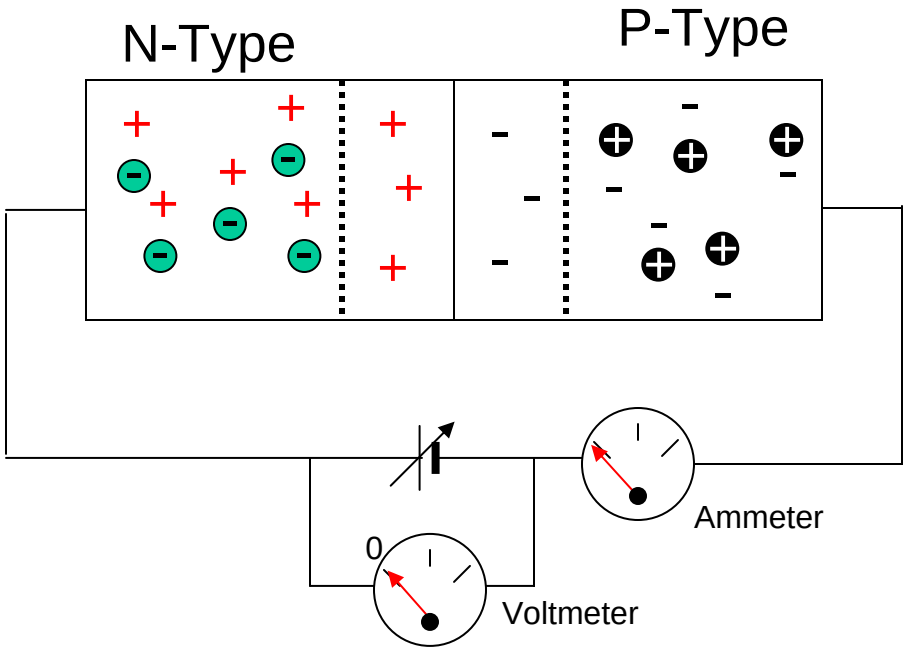
It is on state of PN-diode operation.

Depletion width becomes narrow.

What happen PN-Diode is Reverse Biased ?



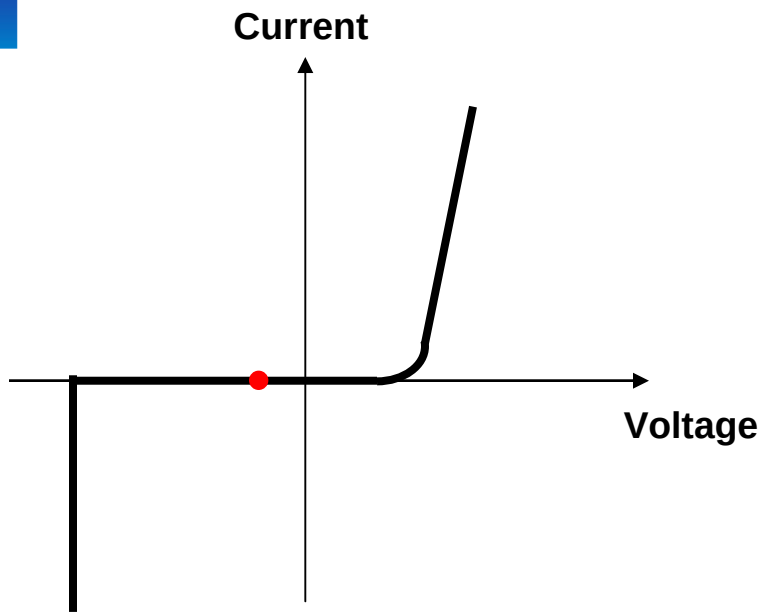


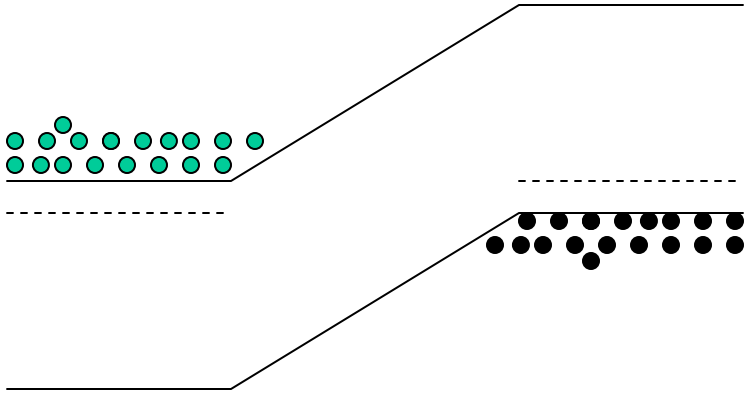


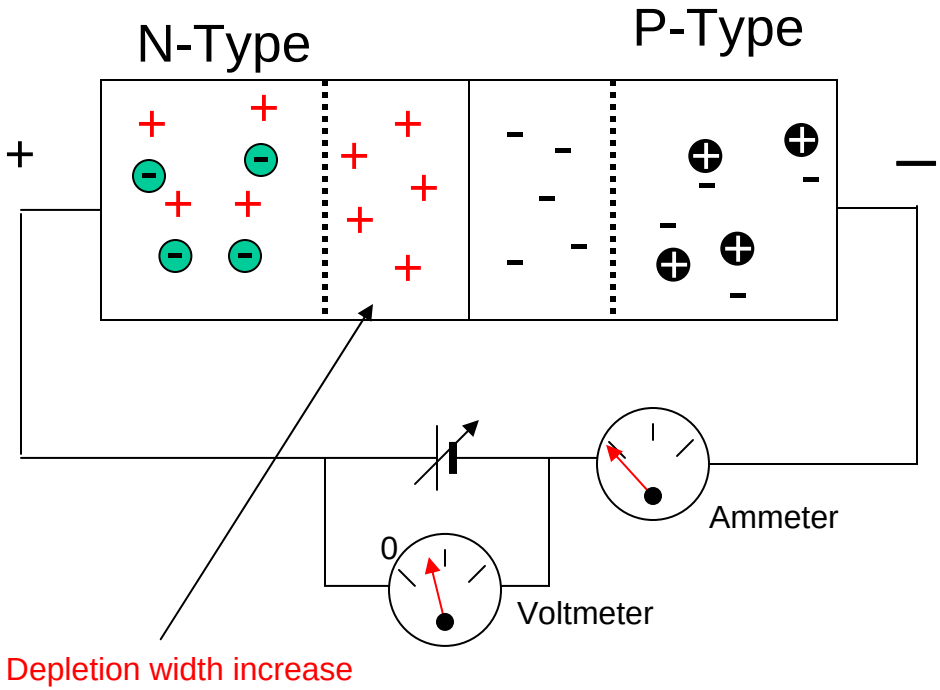
Again the thermal equilibrium condition.

No current flows.

PN-Diode **Reverse Biased (V<0)**





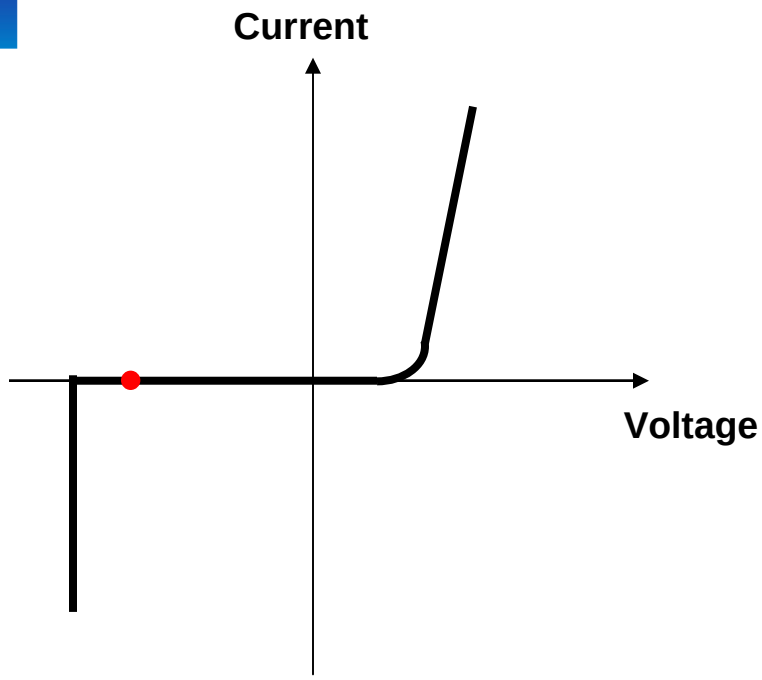


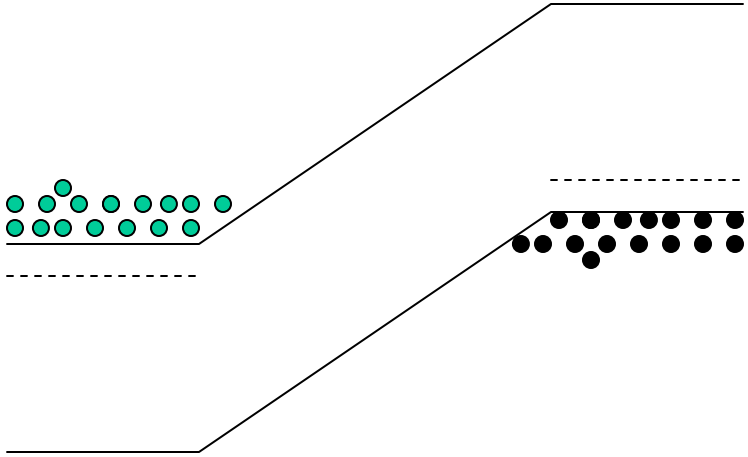
The potential barrier is increased by negative bias across PN-diode.

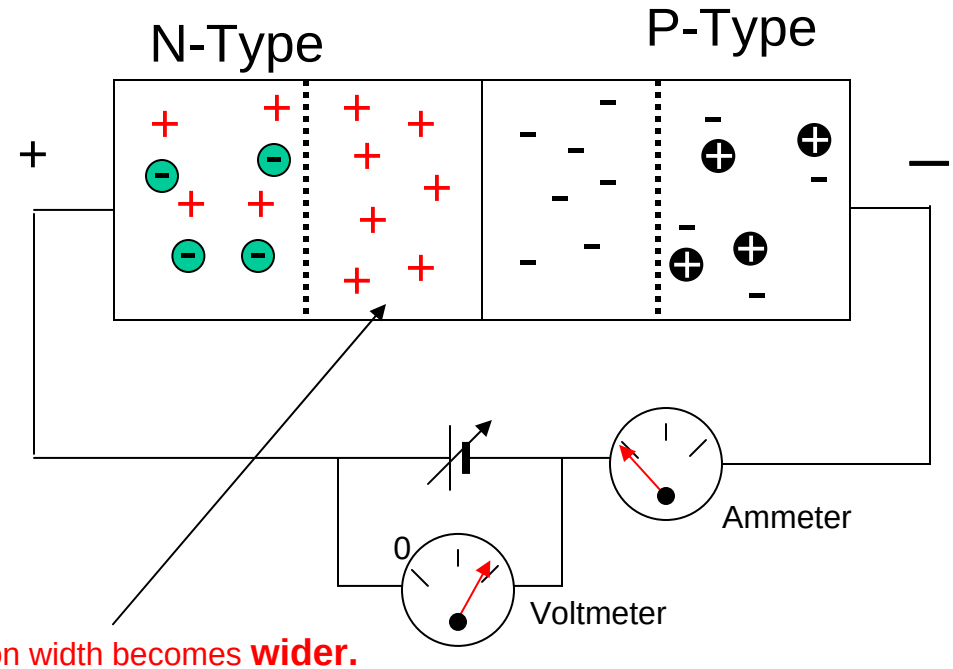
Therefore, carrier diffusion current stays in small value.

Widened depletion width decrease parasitic capacitance between P and N regions.

PN-Diode **Reverse Biased (V<<0)**







Further increase of negative bias does not change current, until junction breakdown.

However capacitance is decreased, which is preferable in CMOS circuit speed.

Depletion width becomes **wider.**

What are key parameters of PN-diode?

Device structure:

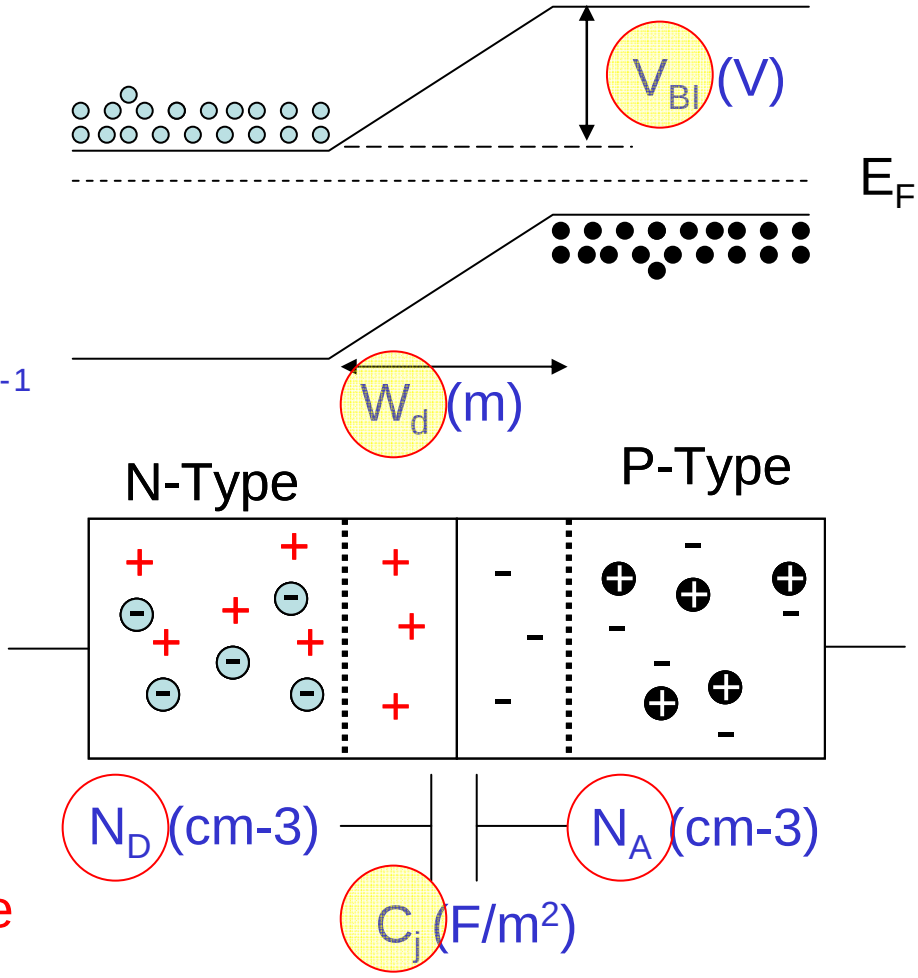
- Acceptor doping level: N_A (cm^{-3})
- Donner doping level: N_D (cm^{-3})

Current equations:

- Reverse: $I_R = 0$
- Forward: $I_F \propto \{\exp[\beta(V)] - 1\}$; $\beta = (kT/q)^{-1}$

Device performance:

- Build-in voltage: V_{BI} (V)
- Depletion width: W_d (m)
- Junction Capacitance: C_j (F/m^2)



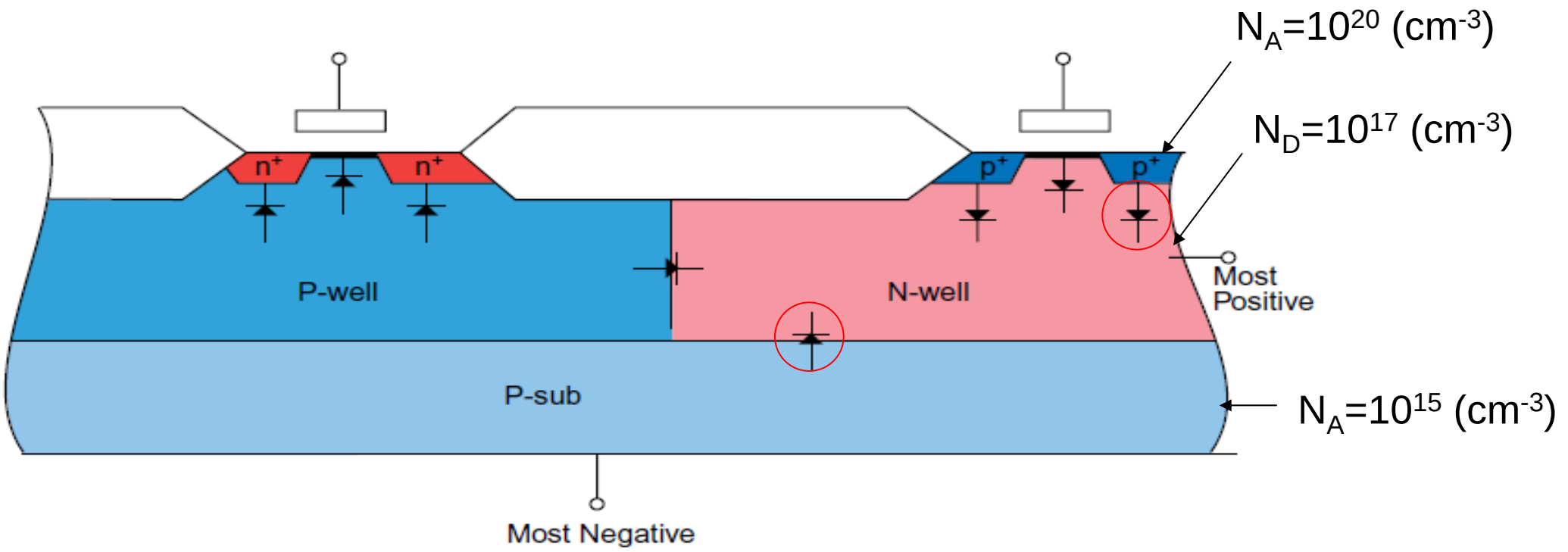
How can we calculate PN-diode performance from device parameters?

Look at real PN-diodes in CMOS ! It is one-sided abrupt junction

PN-diode (P^+/N_{well}): $N_A >> N_D$ ···N_D determine performances (Wd, Cj)

PN-diode (N_{well}/P_{sub}): $N_D >> N_A$ ···N_A determine performances (Wd, Cj)

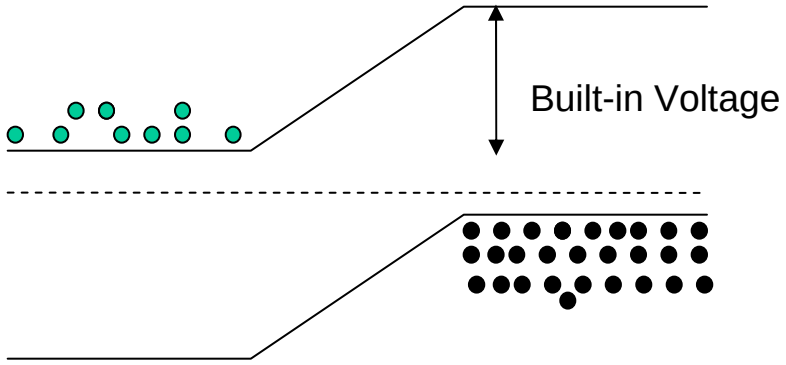
Therefore, performance of PN-diode is determined by lightly doping region, since …….



P⁺N-diode (reverse biased) performance: how the parameters are formulated?

Built-in voltage at equilibrium (V_{BI}):

$$V_{BI} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

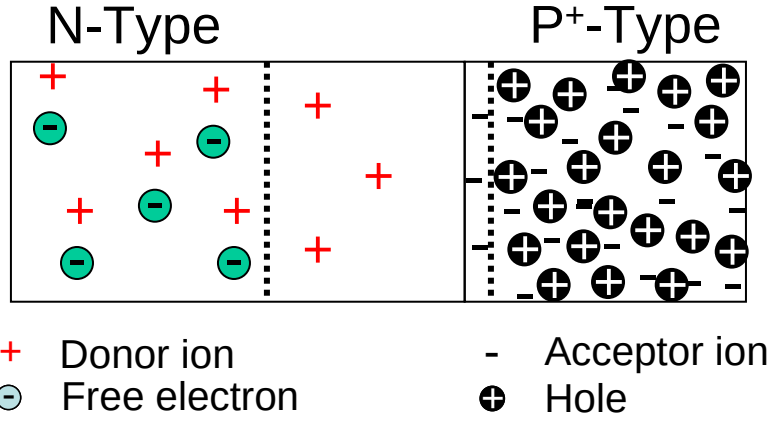


Depletion width (W_d):

$$W_d = \sqrt{\frac{2\varepsilon_S V_{BI}(N_A + N_D)}{qN_A N_D}} \approx \sqrt{\frac{2\varepsilon_S V_{BI}}{qN_D}} \quad @\, N_A >> N_D$$

PN-diode junction capacitance (C_j):

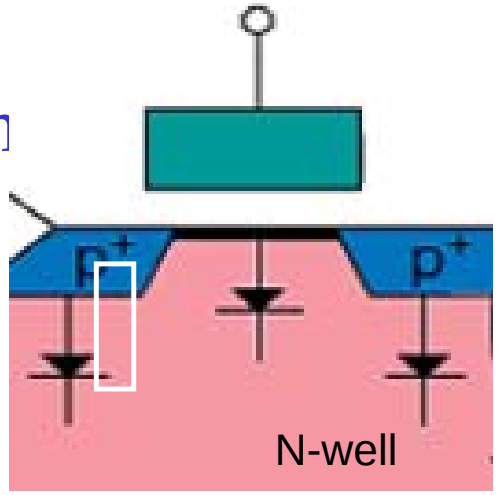
$$C_j = \frac{\varepsilon_S}{W_d} \approx \sqrt{\frac{\varepsilon_S q N_D}{2V_{BI}}} \quad @\, N_A >> N_D$$



Typical value of V_{BI}, W_d and C_j at equilibrium:

- Let's assume $N_A=10^{20}$ (cm^{-3}) and $N_D=10^{17}$ (cm

$$V_{BI}=\frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)=0.026(eV)\ln\left[\frac{10^{20}*10^{17}}{\left(1.5*10^{10}\right)^2}\right]=0.997(V)$$



$$W_d=\sqrt{\frac{2\varepsilon_S V_{BI}}{qN_D}}=\sqrt{\frac{2*11.7*8.85*10^{-14}(F/cm)*0.996(V)}{1.6*10^{-19}(Q)*10^{17}(cm^{-3})}}=0.1135(\mu m)$$

$$C_j=\frac{\varepsilon_S}{W_d}=\frac{11.7*8.85*10^{-14}(F/cm)}{1.135*10^{-5}(cm)}=9.11*10^{-20}(F/cm^2)=9.11(fF/\mu m^2)$$

PN-diode biasing:

In MOS LSI, PN-diode are used as isolation devices. It is sufficient to consider only the negative biased PN-diode, which works as “parasitic C-elements”.

Quiz:

When a PN-diode is negatively biased by “-V”, how change the V_{BI}, W_d and C_j ?

$$V_{BI} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \longrightarrow$$

$$W_d = \sqrt{\frac{2\varepsilon_S V_{BI}}{qN_D}} \longrightarrow$$

$$C_j = \sqrt{\frac{2\varepsilon_S qN_D}{V_{BI}}} \longrightarrow$$

Quiz

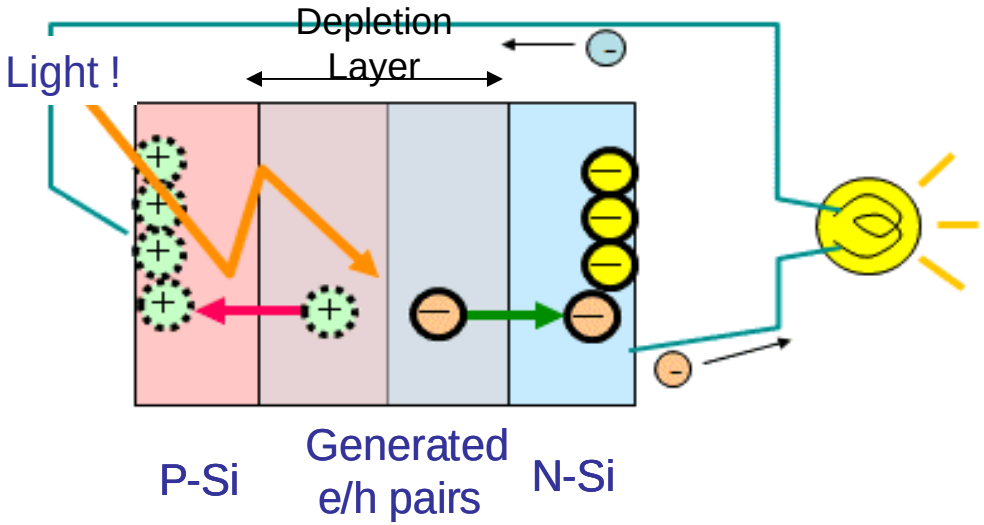
(1) Why PN diode is useful in CMOS Integrated Circuit?

(2) How the built-in voltage V_{BI} is formed?

(3) Calculate ϕ_{Bi} and Wdep & Cj/unit-area in equilibrium condition,
@ $N_A = 10^{15}$ cm^{-3}, $N_D = 10^{20}$ cm^{-3}; Note: ni= 1.5x10^{10} cm^{-3} at Room Temp. (27^{o}C)

Quiz (Continued)

(4) Solar Cell is one of the clean energy as you know. How the Solar Cell generates electricity?



Solar Cell is large PN-Diode

Solar Project in UK: 390kW, 7k panel

Summary of PN-diode:

(1) PN-diode or PN-junction is the most important basic device in CMOS LSI, since it provides electrical isolation between NMOS's and PMOS's.

(2) In CMOS LSI, all the PN-diodes operate in reverse-biased condition (I_R=0). Therefore only the parasitic junction capacitance is major device parameter in circuit design.

(3) Key PN-diode properties:

・Built-in voltage;

$V_{BI} \fallingdotseq 0.7 \sim 1.0$ (V)

・Junction capacitance;

$C_j \fallingdotseq 1.0 \sim 10$ (fF/um^2),

Reverse-bias (-V) dependency, $C_j \propto (V_{BI}\text{-}V)^{-1/2}$

Break !

(4-2) MOS-diode or MOS-capacitor

Why MOS-structure is “Diode”?

Since it is two terminal bias dependent devices.

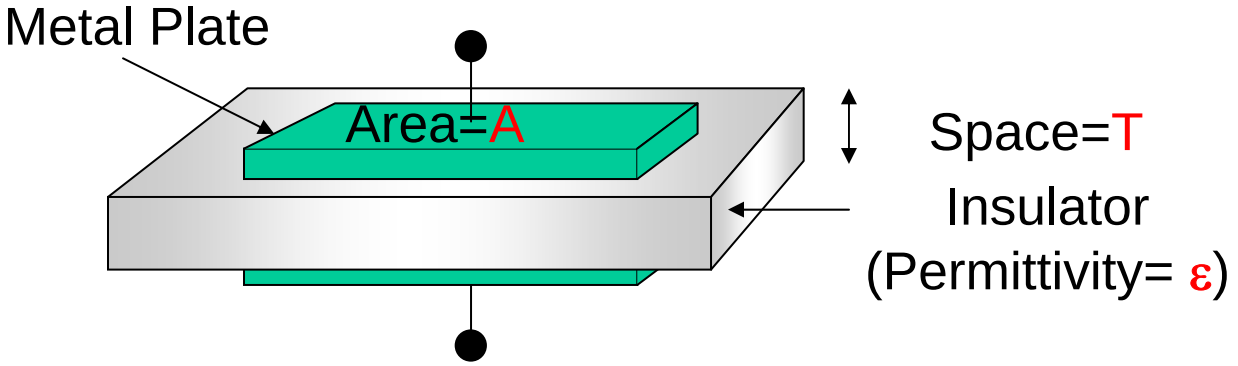
Why MOS-structure is “Capacitor”?

Since no DC-current flows between terminals.

What is difference compared with Simple Capacitor?

MOS-capacitor shows bias dependency.

<Simple Capacitor Structure and its Capacitance Equation>

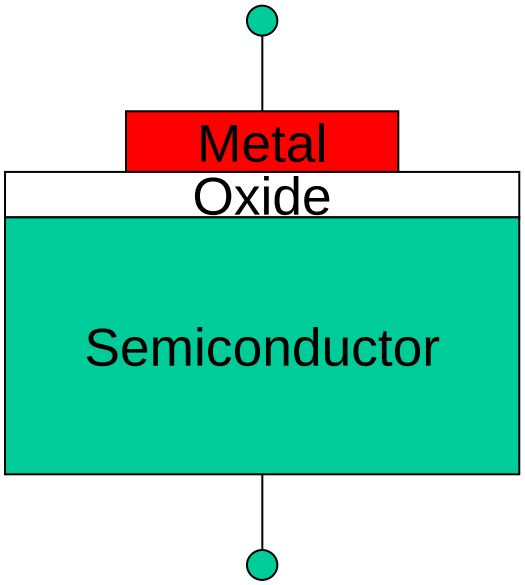


$$Capacitance:\ C = \frac{\varepsilon A}{T}$$

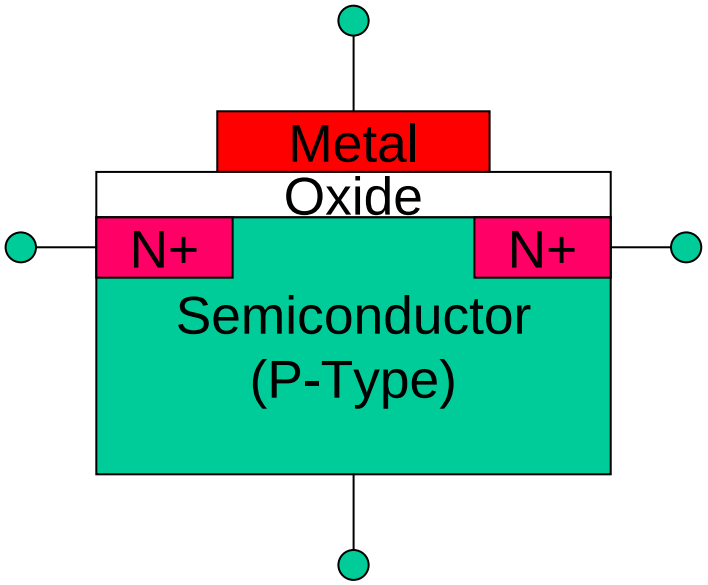
(4-2) MOS-diode or MOS-capacitor

Before you study MOSFET electrical operation, MOS-diode is another key device to learn, as well as PN-diode.

MOS: which stands for Metal-Oxide-Semiconductor, a two terminal device (therefore Diode). A bit difference compared with MOSFET.



MOS-Diode

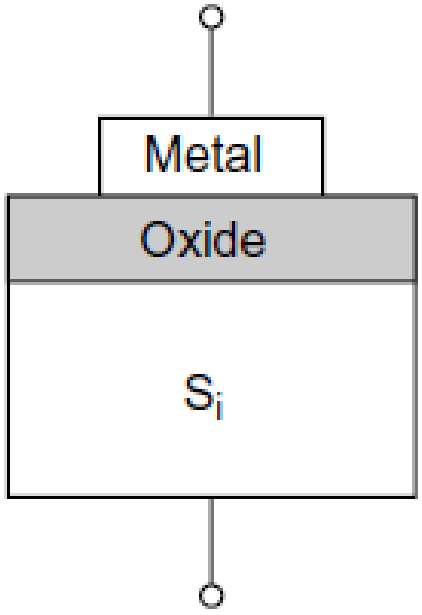


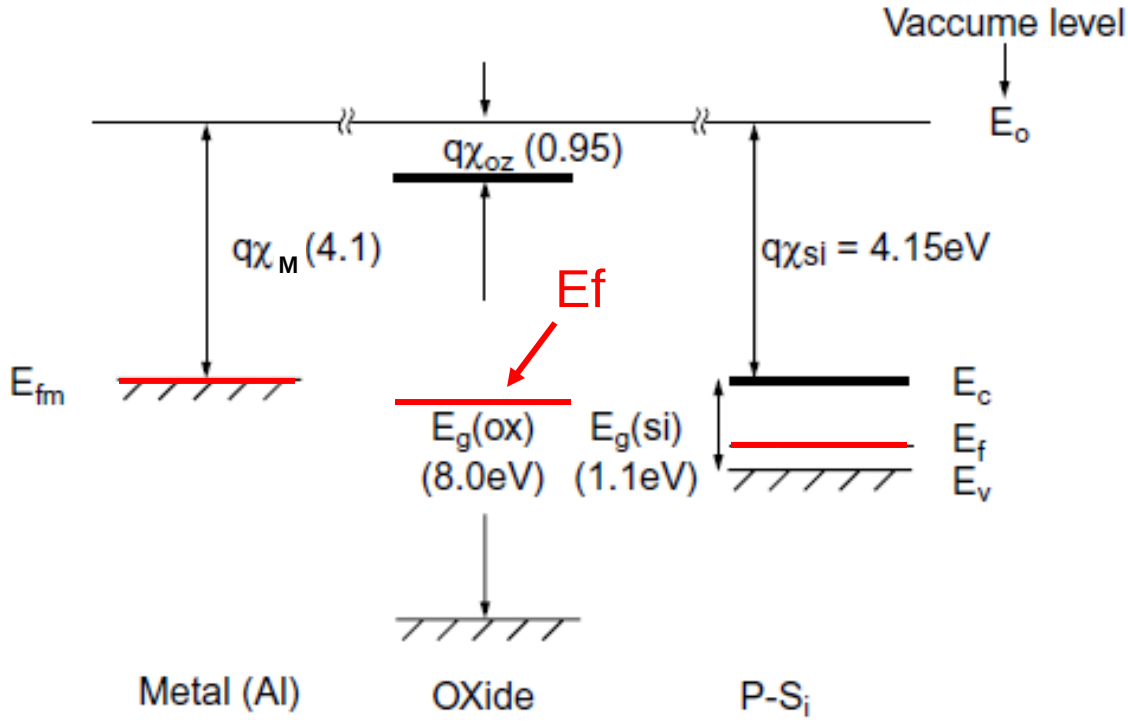
MOSFET

MOS-Diode Basics

What happens when Metal, Oxide, and Semiconductor are joined together?

- Joining three materials makes Ef (Fermi-Energy) at the same level
- Therefore, the S/C band can be bent at the silicon surface due to the work function difference (Efm - Ef) between the metal and the substrate silicon.

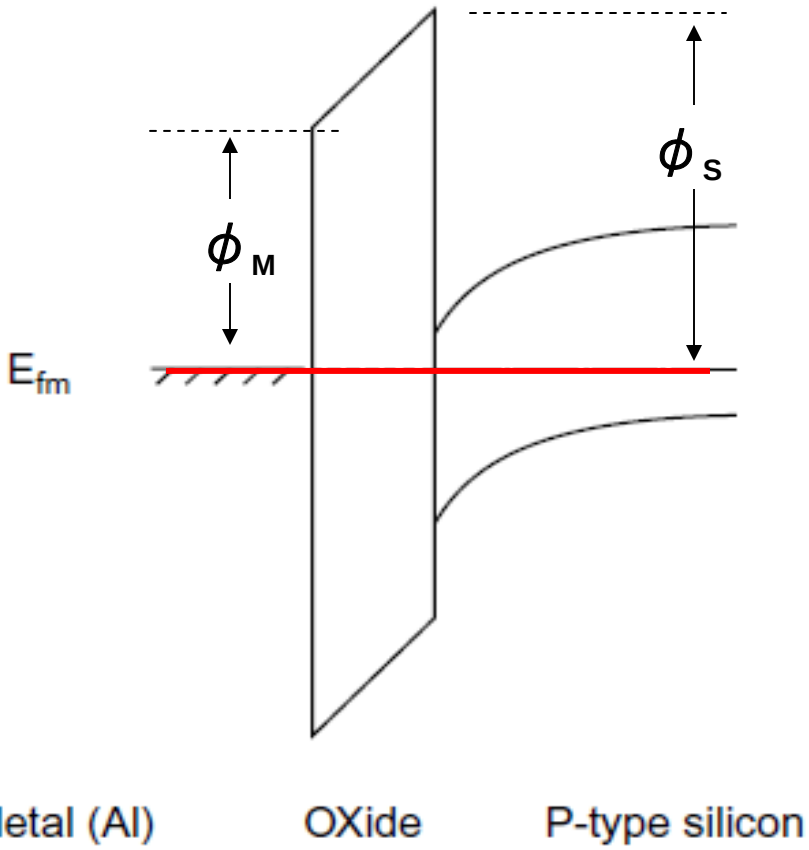




Band diagram at Equilibrium

Note: In MOS structure, Electrical field is generated in the oxide, at which the voltage applied across the oxide is "qϕ_{MS}" the work-function difference.

Band diagram (band structure)



$$\phi_{MS} = \phi_M - \phi_s$$
$$= \chi_M - (\chi si + E_g(si) - E_F)$$
$$= \chi_M - (\chi si + E_g(si) - \frac{kT}{q} \ln(\frac{N_C}{N_A}))$$
$$= 4.1 - (4.15 + 1.1 - 0.025 \ln(\frac{2.8 \times 10^{19}\ cm^{-3}}{10^{16}\ cm^{-3}}))$$
$$= -0.95\ (eV)$$

The ϕ_{MS} in MOS-Diode looks very much alike with Built-in Voltage **ϕ_{Bi}** in PN-Diode!

What happen if we apply Gate Bias ?

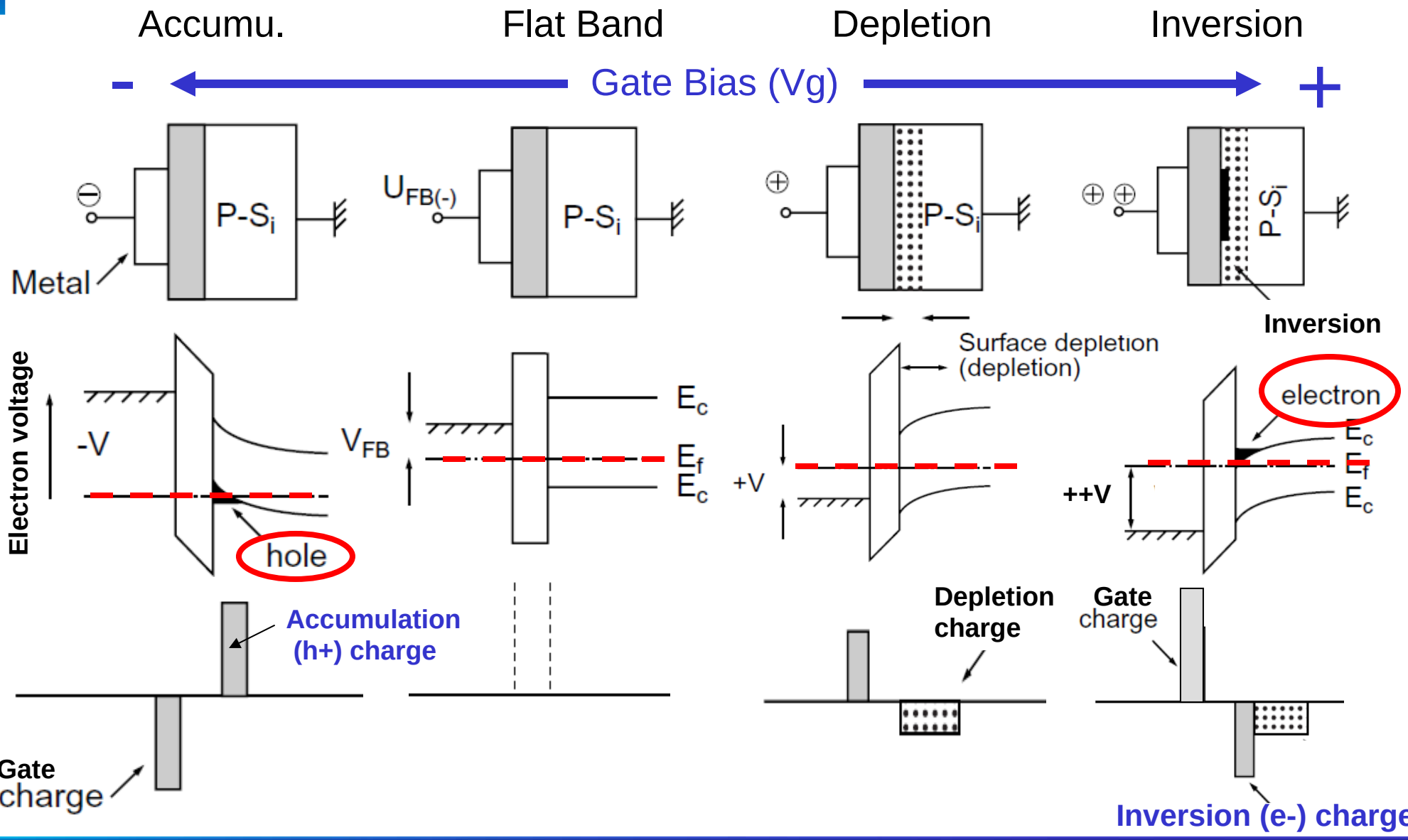
In MOS(P-type Si) Diode:

(1) Apply “–” Voltage to the Gate:
Positive charge (holes) are induced at Si/SiO2 interface

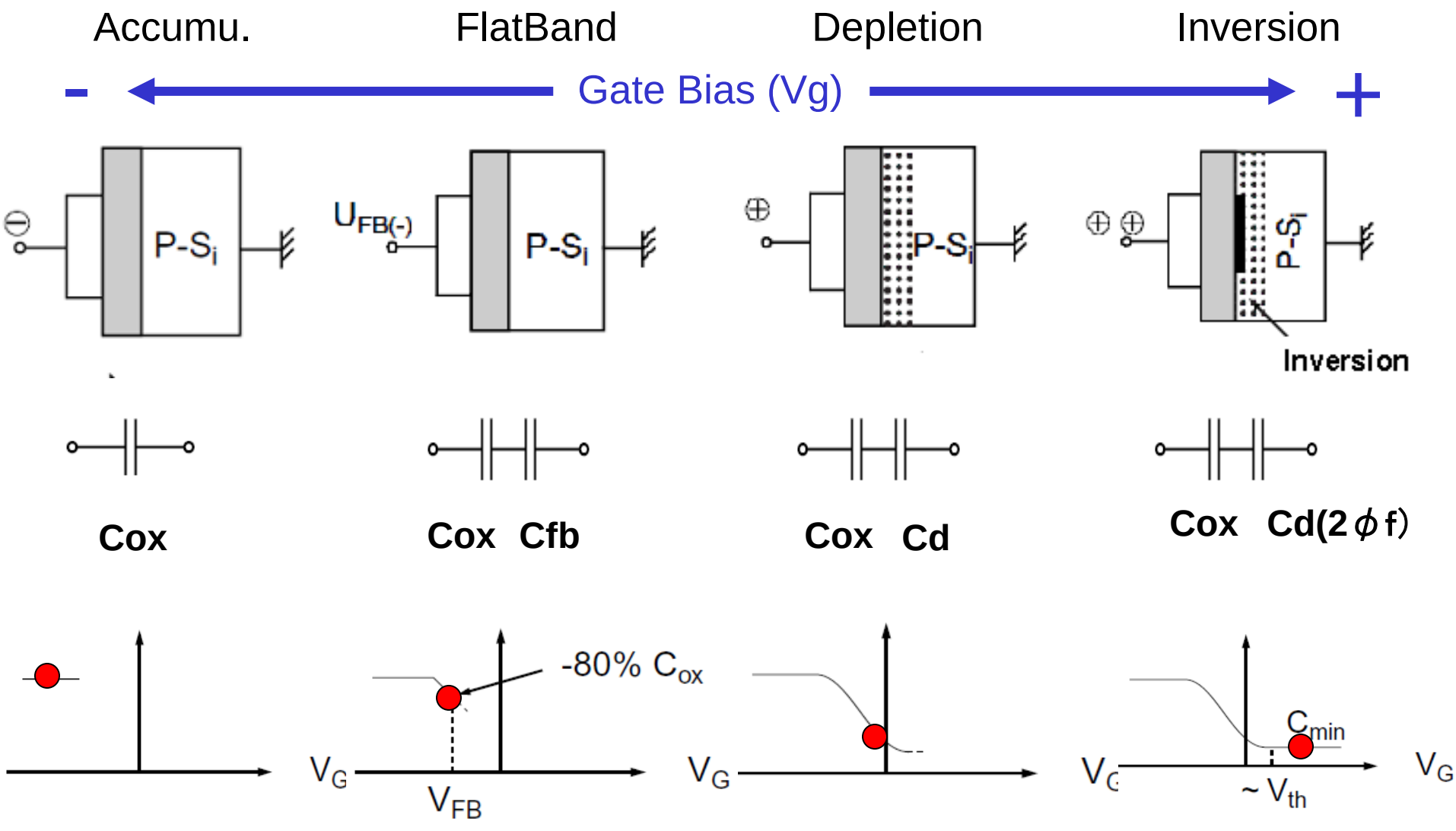
(2) Apply “+” Voltage to the Gate:
Negative charge (electrons) are induced at Si/SiO2 interface

How change in band diagram during Gate Bias from “-” to “+” ?
Interesting change is happen!

Biasing: Accumulation, Flat-band, Inversion



How change in C-V characteristics: (Ideal MOS-Diode C-V curve)



Key Physical Features

In the MOS diode, ϕ_f (the Fermi level) matches in the equilibrium condition.

MOS-Diode has three operational region
(Accumulation, Depletion, and Inversion)

Important characteristic values in the MOS-diode:

Flat-band voltage

$$V_{FB} = \phi_{MS} + \frac{Q_{ss}}{C_o}$$

This is an important Parameter of MOSFET

Threshold voltage

$$V_{th} = \left(\phi_{MS} + \frac{Q_{ss}}{C_o}\right) + 2\phi_F + \frac{Q_B}{C_o}$$

where,

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \qquad Q_B = \sqrt{2\varepsilon_s q N_A}\ \sqrt{2\phi_F}$$

Note: MOS Diode determines “Vth” the important MOSFET parameter !

Show Time !

MOS-Diode or MOS-Capacitor

- Electrons at Surface (Silicon/SiO2 interface)
- Depletion Layer at Silicon Surface
- C-V Characteristics of MOS-Diode

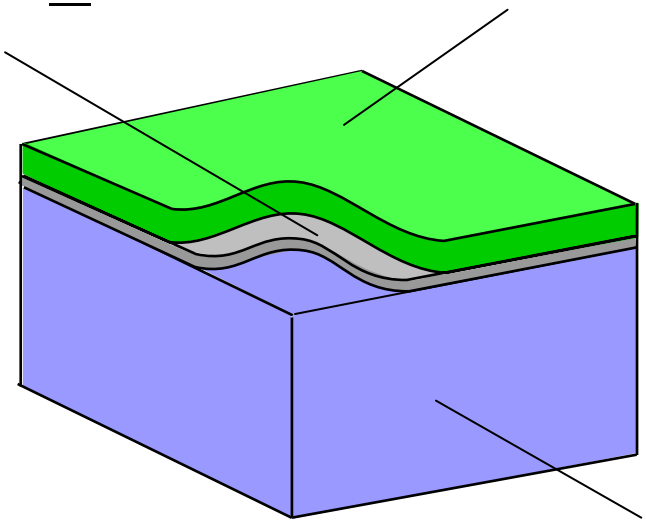
How changes the above quantities as Gate bias?

- Accumulation condition
- Depletion condition
- Inversion condition

MOS (Metal Oxide Semiconductor)Capacitor

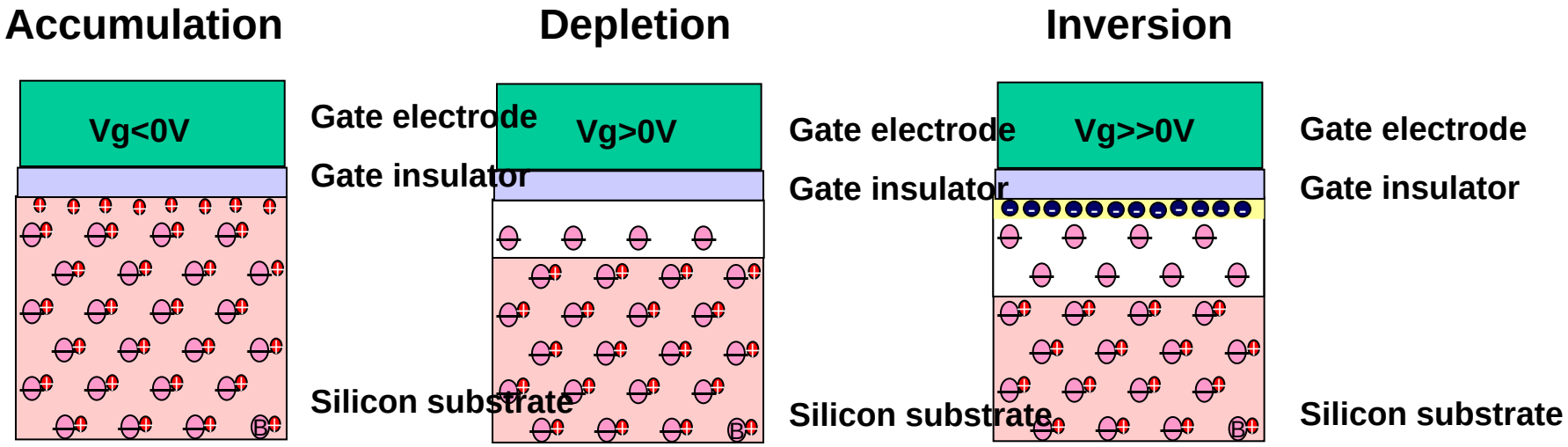
Insulator : Oxide

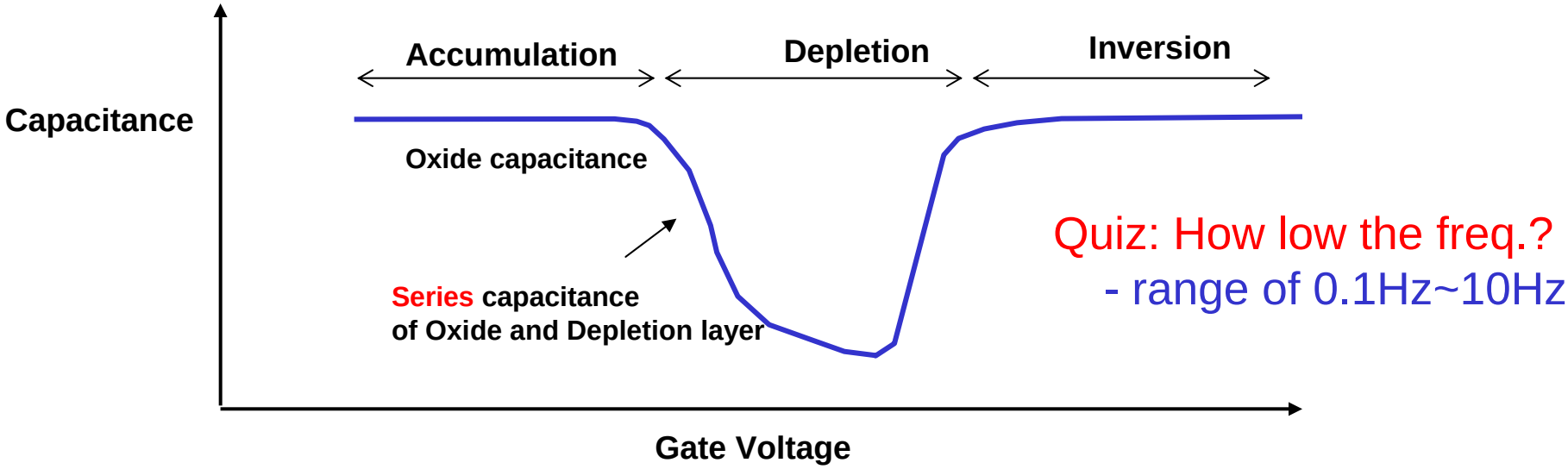
Metal electrode : Metal (Gate electrode)



Semiconductor substrate

Operation of MOS Capacitor (In case of very low frequency)

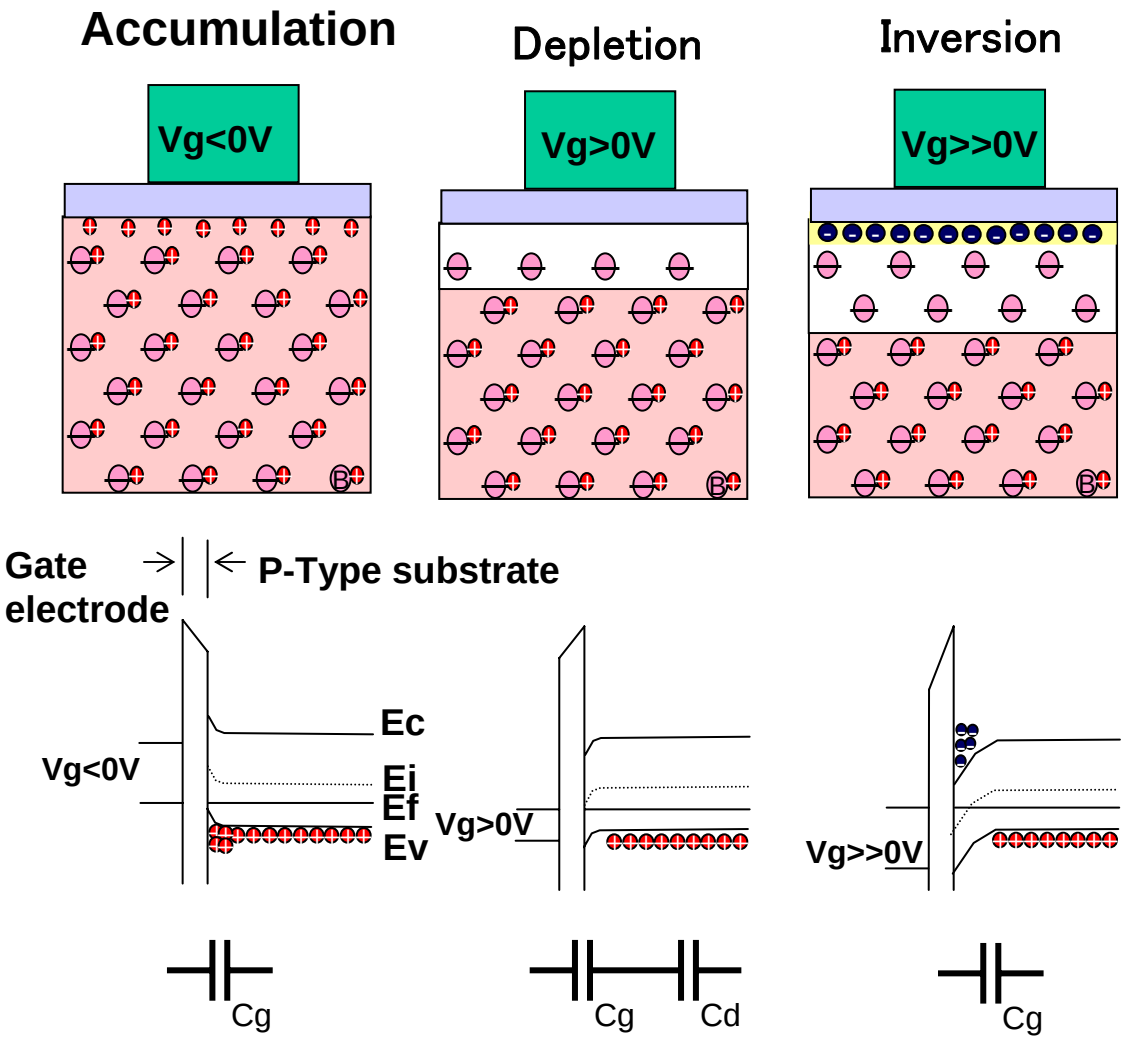


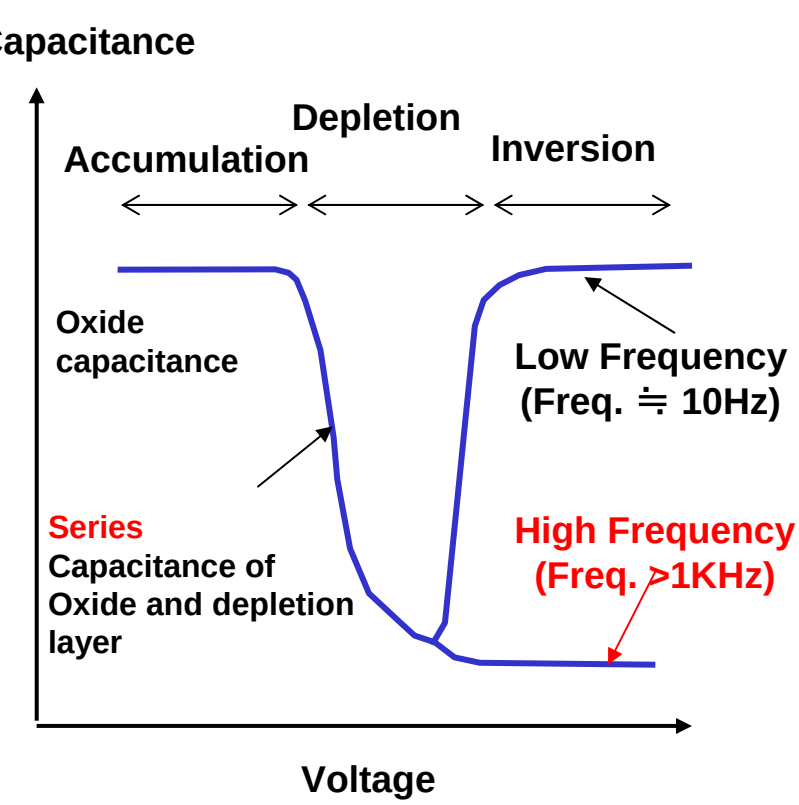


Quiz: How low the freq.?
- range of 0.1Hz~10Hz

MOS Capacitor: what happen in high frequency?

C-V curve shows quite different frequency characteristics in Inversion condition!





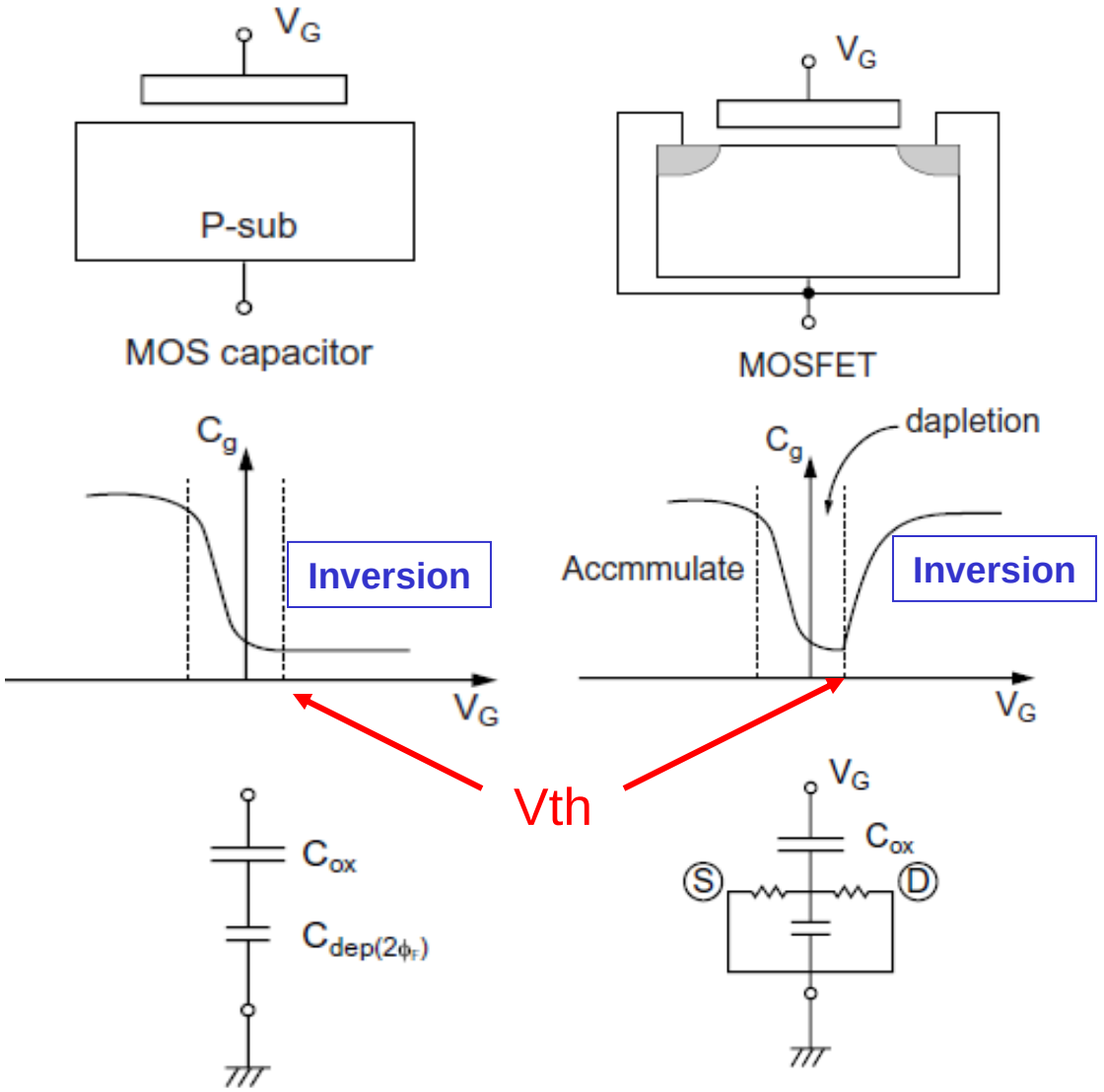
Q. Why the differences?

Difference in C-V Curves (@ high frequency): Between MOS-Diode and MOSFET

Digital LSI speed=MHz~GHz:
MOS-diode and MOSFET operate in high frequency condition・・・:

MOS-Diode:
In inversion region, Ctot is determined with series-connection of Cox & Cdep

MOSFET:
In inversion region, Ctot is determined with Cox only. Cdep is short-circuited by Source/Drain connected with body substrate.



Summary of MOS-diode

- MOS structure is very simple structure.
- It can induce N+ Inversion Layer at Si surface below the Metal-Gate, when you apply the gate bias above threshold voltage.
- Gate bias voltage at which the Inversion Layer appears at Si surface is one of the important parameters related switching voltage in MOSFET ……(Threshold voltage).

$$V_{th} = \phi_{MS} + \frac{Q_{SS}}{C_O} + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_A}}{C_O}\left(2\phi_F\right)^{1/2}$$

- MOS capacitance shows bias-dependent, which can be used as MOS Varactor (Variable Capacitor) in RF circuits.

Quiz

(1) Depict band structure of: accumulation, flat band, depletion and inversion conditions.

(2) Draw charge diagram at inversion condition. When gate bias is increased further, what happens in charge diagram?

(3) Why we can assume Fermi level is in identical value (Metal and semiconductor) at thermal equilibrium?

(4) Explain the difference between C-V curves of MOS diode and MOSFET, in digital circuit operation condition.

(5) How the inversion charge is generated under the gate; in the case of MOS diode and MOSFET?