Quality Assurance Basic Educational Course

Based on Reliability Handbook

Section 4 Failure Mechanisms.

Renesas Design Vietnam Co., Ltd.
Design Engineering Division

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Section 4 Failure Mechanisms.

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Table 4.1 Failure Factors, Mechanisms, and Modes

Failure Factors		Failure Mechanisms	Failure Modes	Example
Diffusion	Substrate	Crystal defect	Decreased breakdown voltage	
Junction	Diffused junction	Impurity precipitation	Short circuit	
	Isolation	Photoresist mask misalignment	Increased leakage current	
		Surface contamination		
Oxide film	Gate oxide film	Mobile ion	Decreased breakdown voltage	Figure 4.1
	Field oxide film	Pinhole	Short circuit	
		Interface state	Increased leakage current	
		TDDB	h_{FE} and/or Vth drift	
		Hot carrier		
Metallization	Interconnection	Scratch or void damage	Open circuit	Figure 4.2
	Contact hole	Mechanical damage	Short circuit	
	Via hole	Non-ohmic contact	Increased resistance	
		Step coverage		
		Weak adhesion strength		
		Improper thickness		
		Corrosion		
		Electromigration		
		Stress migration		
Passivation	Surface protection film	Pinhole or crack	Decreased breakdown voltage	
	Interlayer dielectric film	Thickness variation	Short circuit	
		Contamination	Increased leakage current	
		Surface inversion	h_{FE} and/or Vth drift	
			Noise deterioration	

Failure Factors		Failure Mechanisms	Failure Modes	Example
Die bonding	Chip-frame connection	Die detachment Die crack	Open circuit Short circuit Unstable/intermittent operation Increased thermal resistance	Figure 4.3
Wire bonding	Wire bonding connection Wire lead	Wire bonding deviation Off-center wire bonding Damage under wire bonding contact Disconnection Loose wire Contact between wires	Open circuit Short circuit Increased resistance	Figure 4.4 Figure 4.5
Sealing	Resin Sealing gas	Void No sealing Water penetration Peeling Surface contamination Insufficient airtightness Impure sealing gas Particles	Open circuit Short circuit Increased leakage current	Figures 4.6 and 4.7, Figure 4.8
Input/output pin	Static electricity Surge Over voltage Over current	Diffusion junction breakdown Oxide film damage Metallization defect/destruction	Open circuit Short circuit Increased leakage current	Figure 4.9
Others	Alpha particles High electric-field Noise	Electron-hole pair generation Surface inversion	Soft error Increased leakage current	

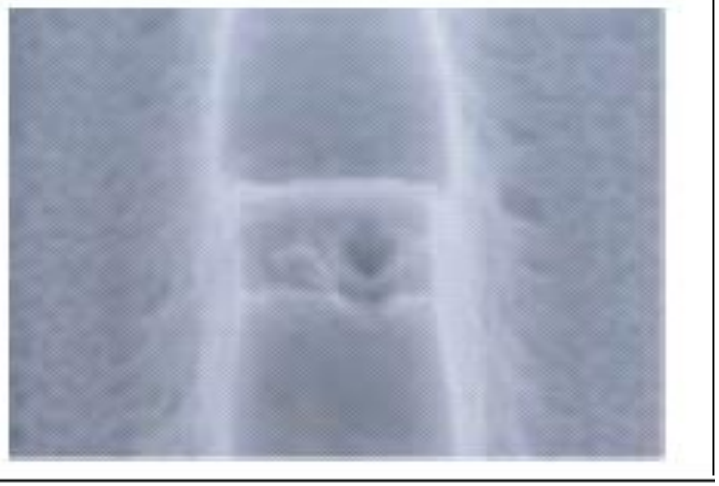


Figure 4.1 Gate Pinhole

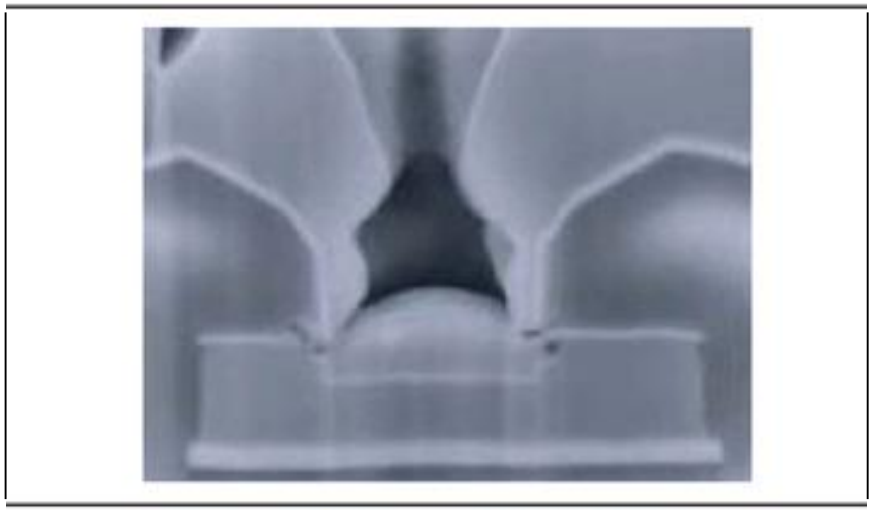


Figure 4.2 Al Wiring Coverage Disconnection

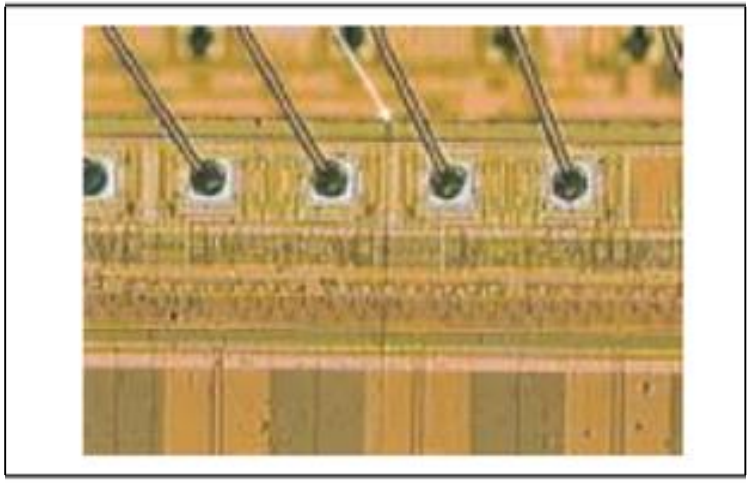


Figure 4.3 Crack

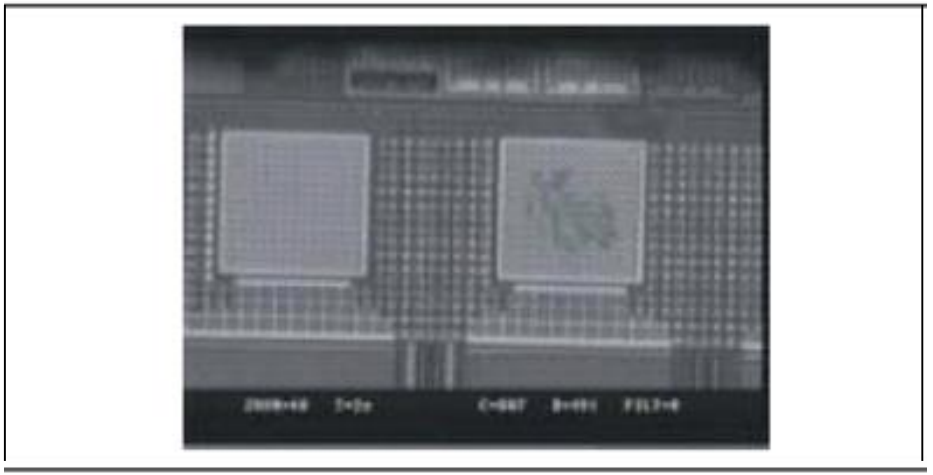


Figure 4.4 Damage under Bonding (Bottom View)

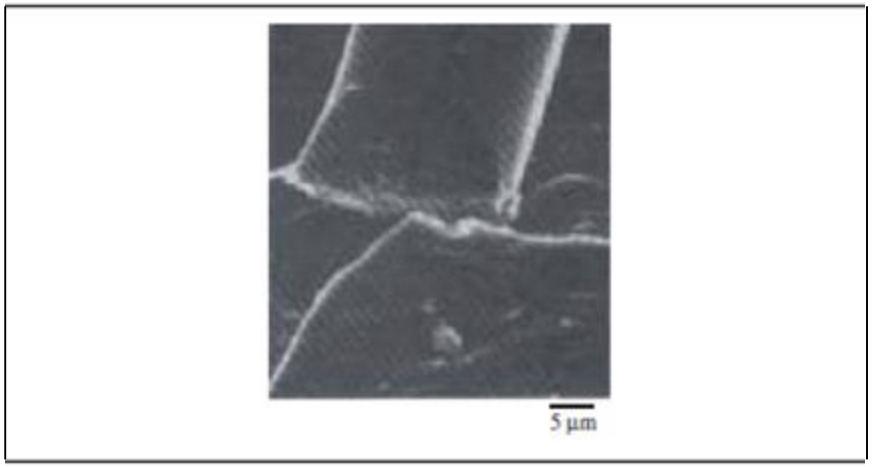


Figure 4.5 Damage on Wire Due to Ultrasonic Fatigue

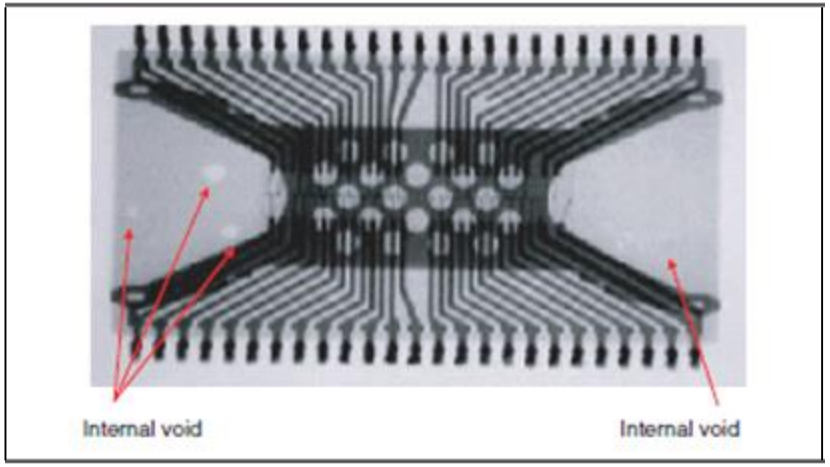


Figure 4.6 Internal Voids in Package

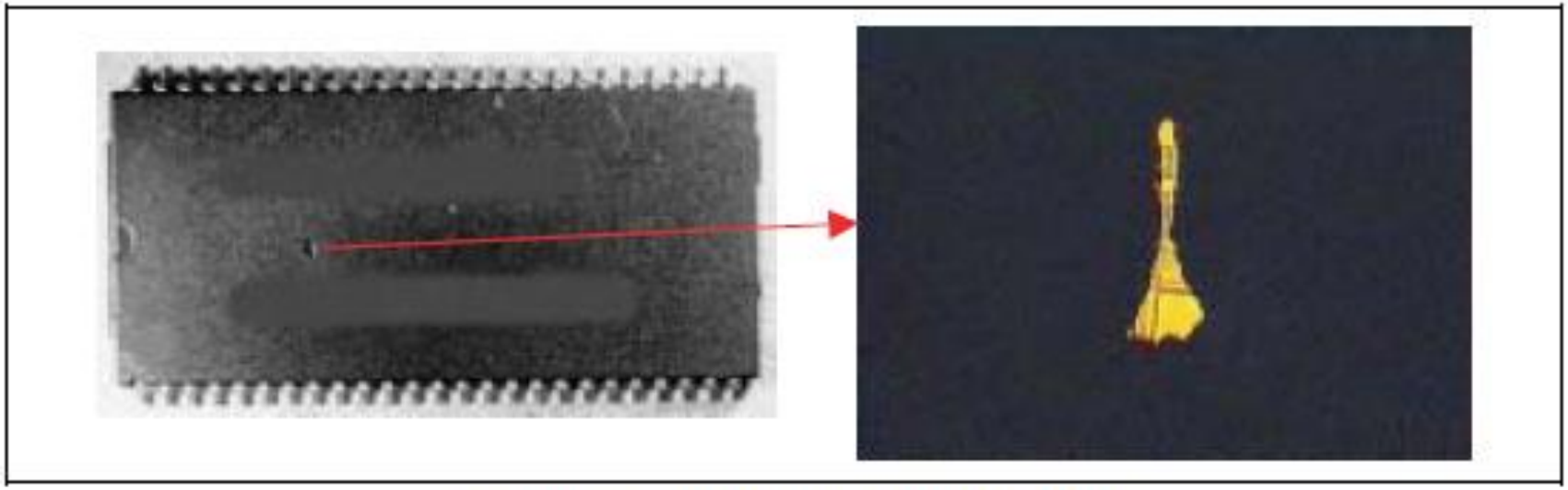


Figure 4.7 No Molding Resin Injected

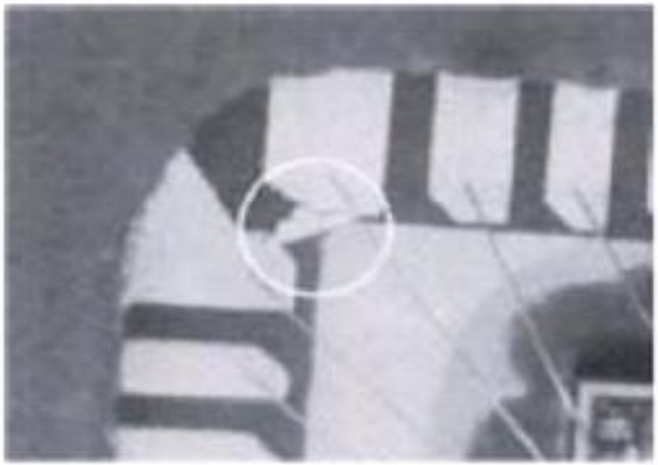


Figure 4.8 Short Circuit Due to Conductive Particles in Package

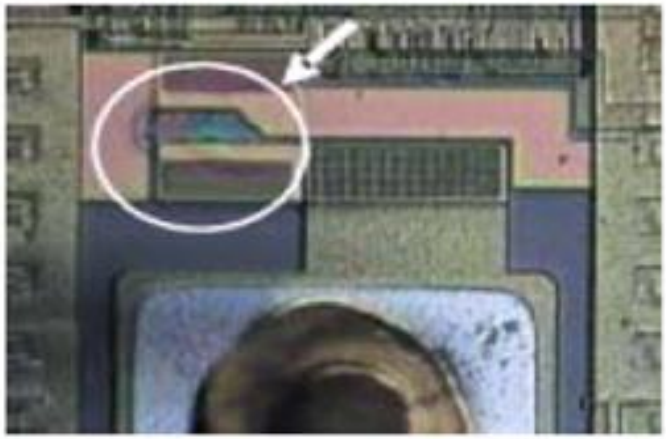


Figure 4.9 Terminal Breakdown Due to Overvoltage

Important failure mechanisms that chip designers should know

Failure mechanism	The items should be careful on chip design	Remark
-TDDB	Voltage specification	Must obey the contents specified in design manual of each wafer process.
-HC	Voltage specification and the rate of transient signal wave etc.	
-NBTI	Voltage specification	
-EM	Maximum allowable current specification of metal wire	
-SM	Depend on wafer process specification.	

Table 4.2 Scaling Rule [1]

Parameter	Constant Electric Field Scaling Factor
Gate oxide film thickness	1/k
Gate length	1/k
Gate width	1/k
Junction depth	1/k
Impurity concentration	k
Voltage	1/k
Electric field	1
Current	1/k

Rule for maintaining characteristics and reliability when shrinking die to 1/k time.

Table 4.3 Typical Failure Mechanisms related to the Wafer Process

Failure Mechanism	Activation Energy (eV)
Time-dependent dielectric breakdown (TDDB)	0.5 to 0.8
Hot carrier	—
NBTI	About 1
Al electromigration	0.6 to 1.0
Al stress migration	About 1
Soft error	—
Volatile failure of Nonvolatile memory	1 or more

Next

TDDB (Time Dependent Dielectric Breakdown)

TDDB is a phenomenon that insulated films such as gate oxide of MOS type semiconductors are degraded and broken with time, when receiving voltage stress.

Explanation of a mechanism

1) Impression of voltage to oxide film

→ Holes are injected by the electric field into oxide film at the positive electrode side.

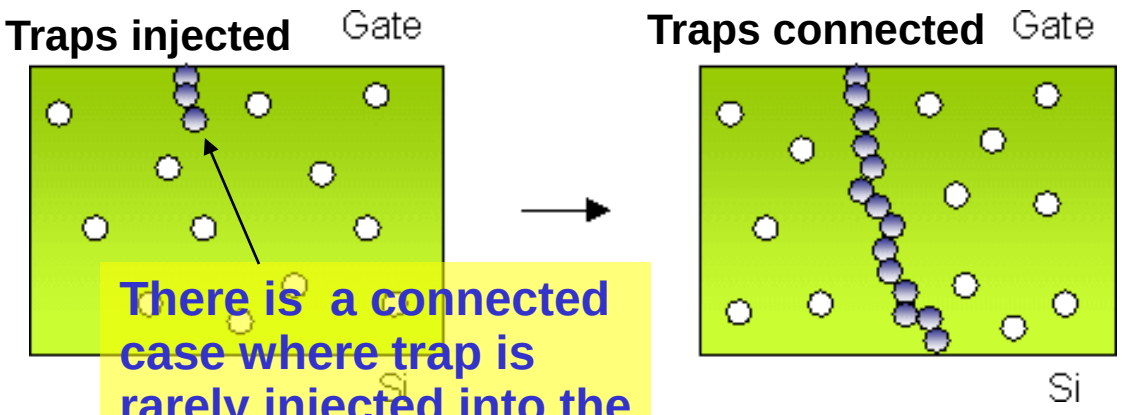
→Defects (traps) are generated in oxide film.

2) Voltage impression continues.

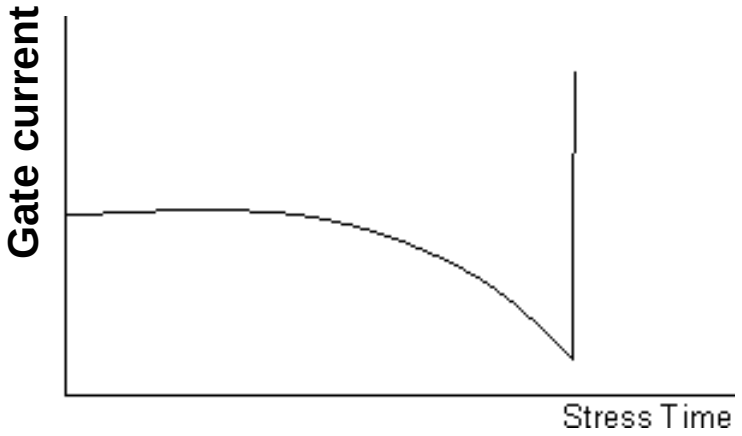
→ Traps increase and they are connected from gate electrode to substrate.

→ Large current flows.

→ Oxide film is broken.



There is a connected case where trap is rarely injected into the same place.



Change of the gate current by voltage stress

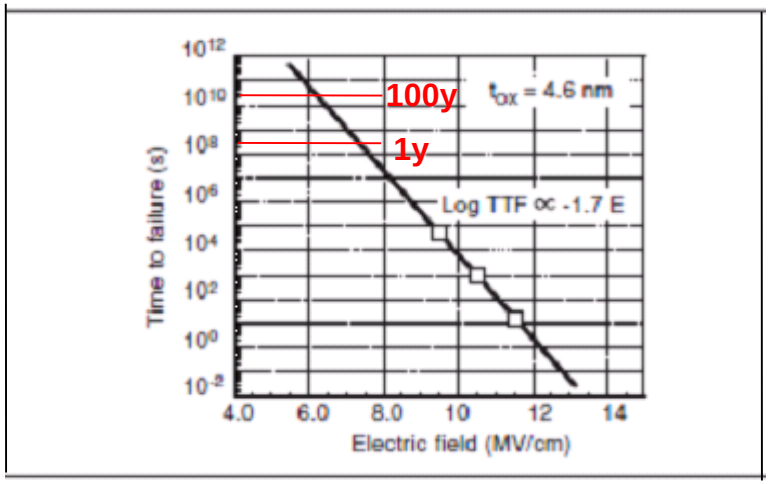


Figure 4.10 Electric Field Dependency of TDDB

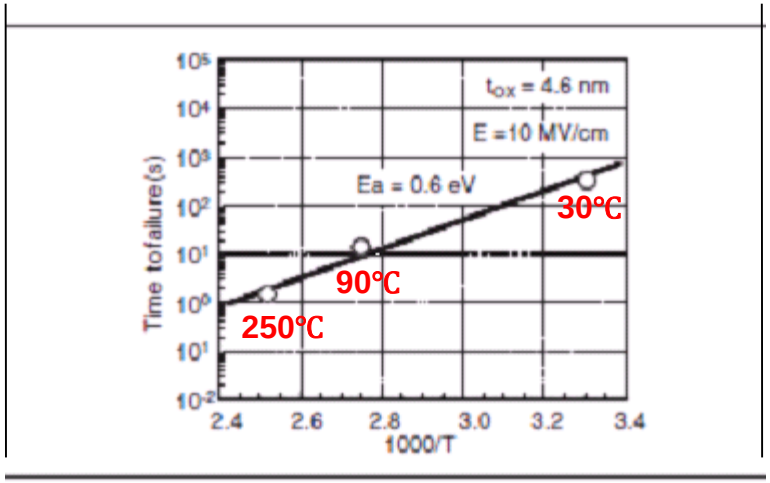


Figure 4.11 Temperature Dependency of TDDB

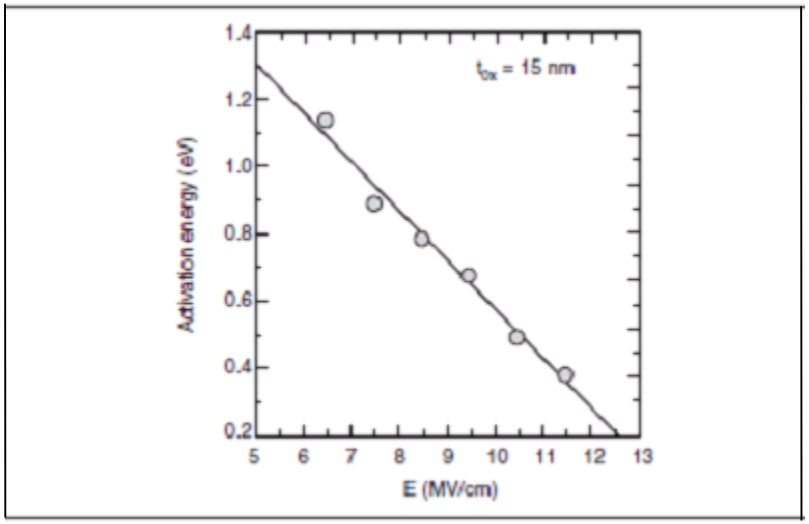


Figure 4.12 Electric-Field Dependency of Activation Energy[5]

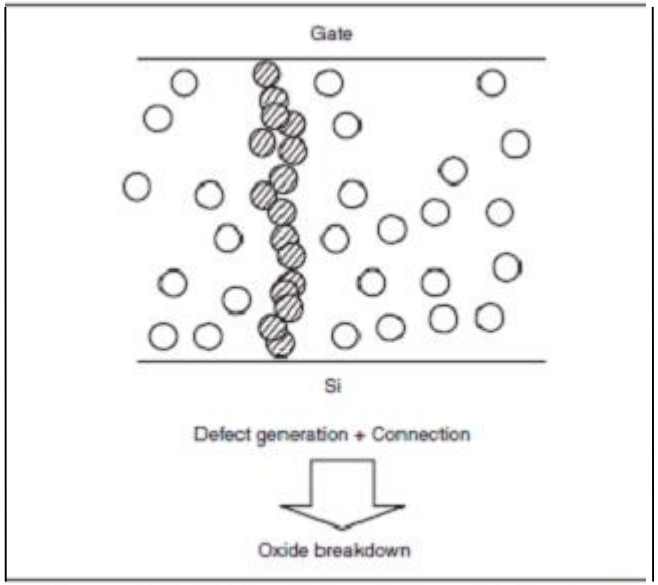


Figure 4.13 Dielectric Breakdown Mechanism[6]

HC (Hot Carrier)

HC is one of the failure mechanisms with the tendency generated with progress of transistor fine structure.

In the area of high electric field in channel, the carriers which flow from source got high energy by electric field, it collides with the atom in the area of channel, and the pairs of electron and hole are generated.

Although almost of holes flow into substrate, the electrons got high energy inject into gate oxide.

By affection of the electrons in gate oxide, the threshold value (Vth) of transistor is changed, the characteristics of transistor shift, and fault of device is caused.

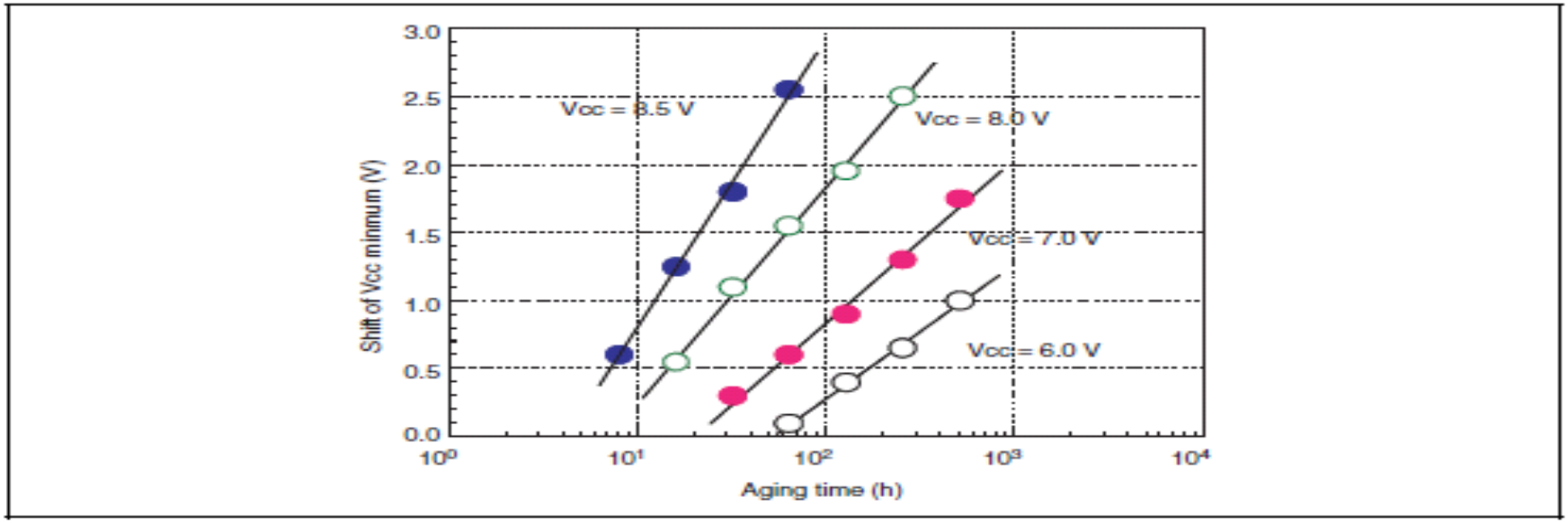


Figure 4.15 Supply Voltage (Drain Voltage) Dependency of Degradation

High speed electron collide with atom of silicon

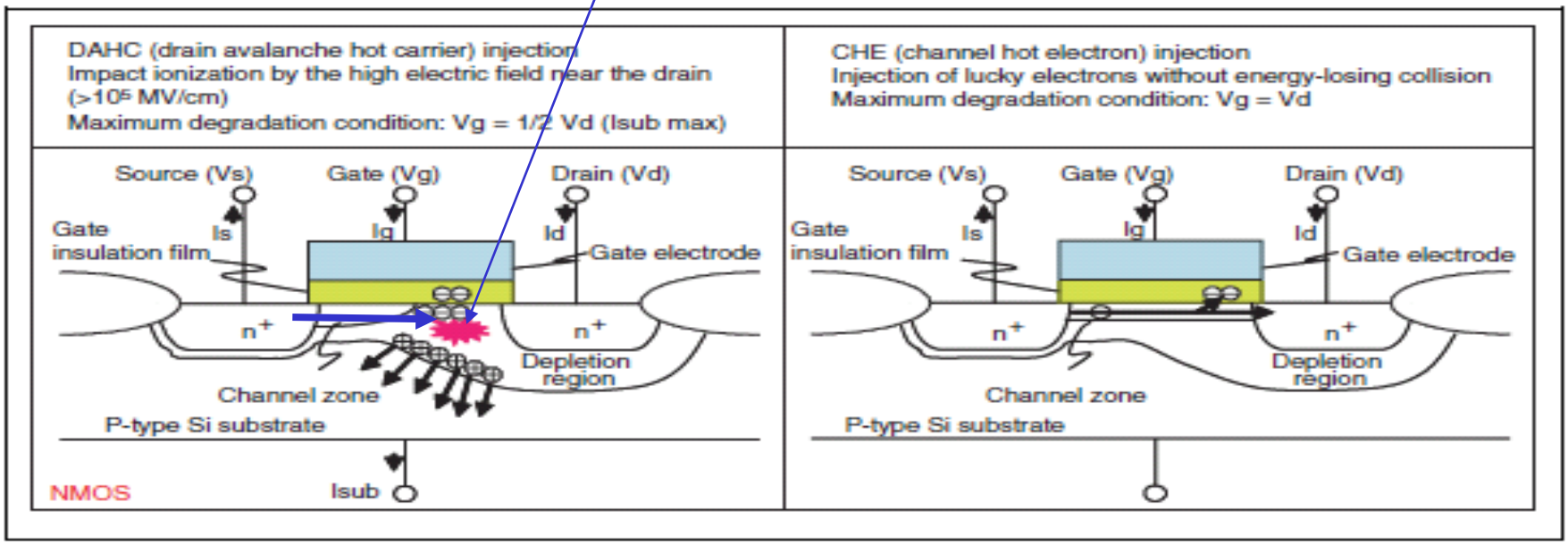


Figure 4.14 Major Mechanisms of Hot Carrier Generation

Two types of HC degradation

DAHC: **It happens, when transistor change from ON to OFF, and OFF to ON.**

CHE: **In the state of ON of transistor, when the potential of drain does not descend, it happens. (When capacitance load is at the drain etc.)**

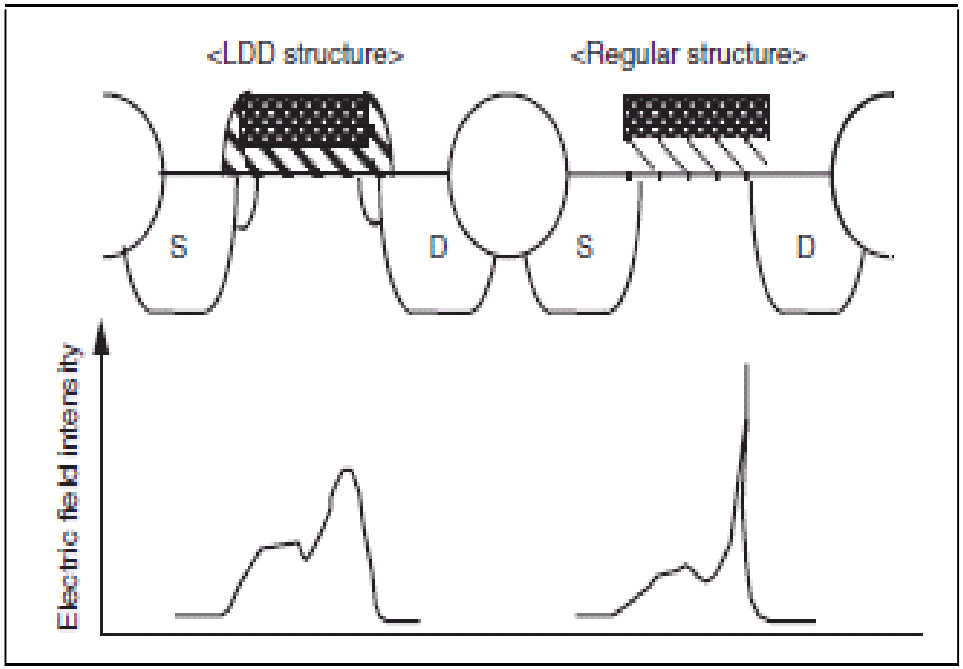
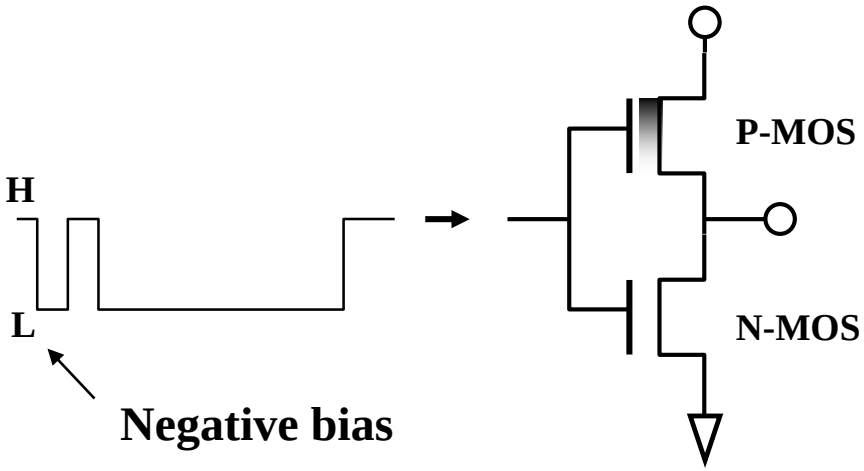


Figure 4.16 LDD Structure

Lightly Doped Drain (LDD) structure as a way to improve HC degradation.

NBTI (Negative Bias Temperature Instability)

While negative bias is impressed to the gate of PMOS transistor, ~~electrons~~ holes are injected into gate oxide with time from the substrate side, and the characteristics of a transistor degrade.



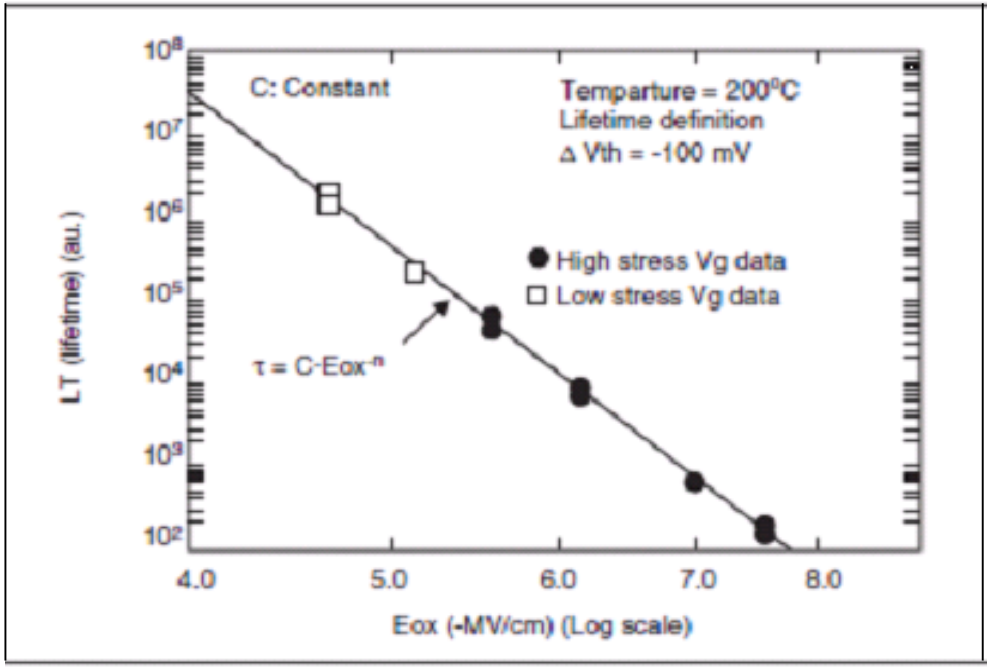


Figure 4.17 Electric field Dependency of Device Life[14]

EM(Electromigration)

EM is a phenomenon which the atom of metal wiring moves by current.
By this movement of atom, resistance increase and disconnection of wiring occur and the fault of device occurs.

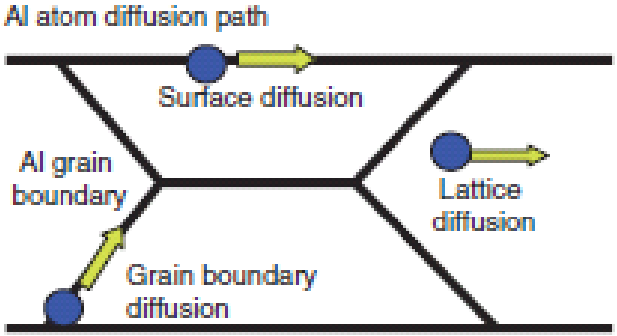


Figure 4.20 Lattice Diffusion, Grain Boundary Diffusion, and Surface Diffusion of Polycrystalline Al

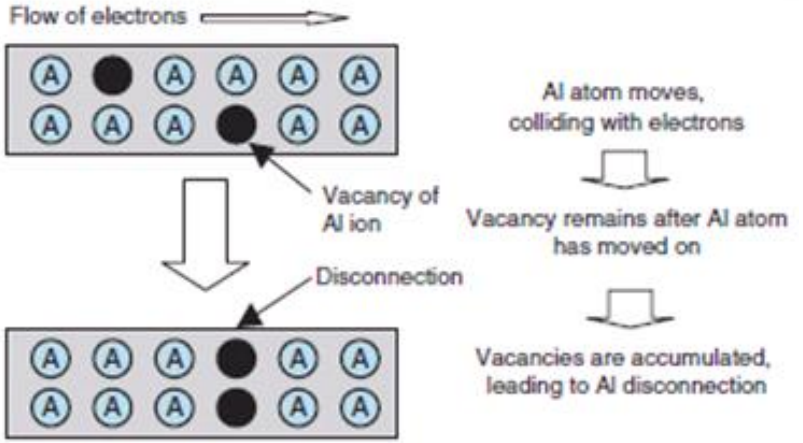


Figure 4.18 Failure Mechanism

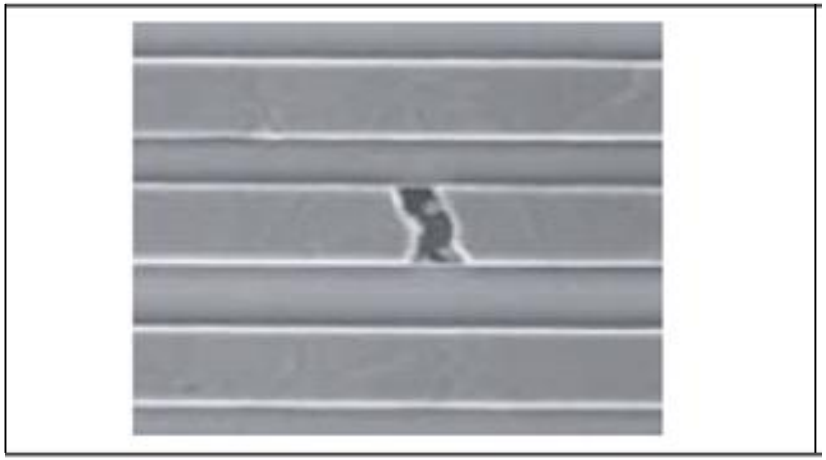


Figure 4.19 Electromigration of Al Wire

SM (Stress Migration)

The stress migration is one of the disconnection phenomena of metal wiring. The cause of disconnection is stress generated according to the difference of the thermal expansion coefficient of passivation film or interlayer film, and aluminum wiring.

The atom of Al or Cu moves by stress and slit-like void occurs.

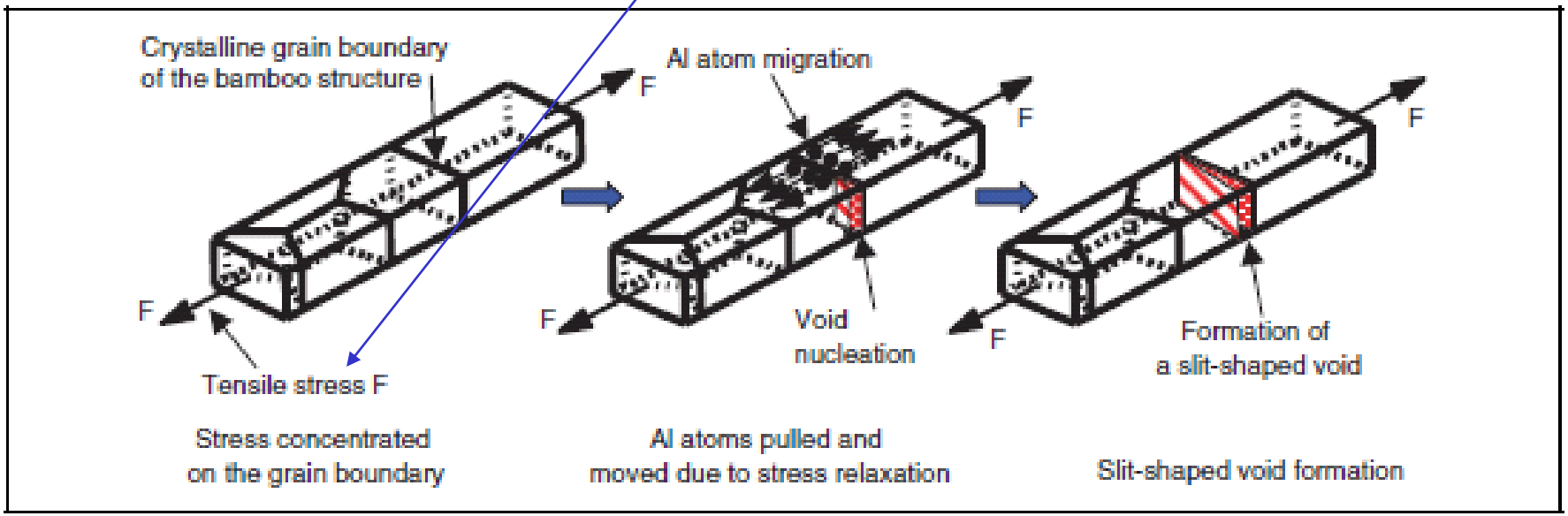


Figure 4.21 Mechanism of Slit-Shaped Void Formation

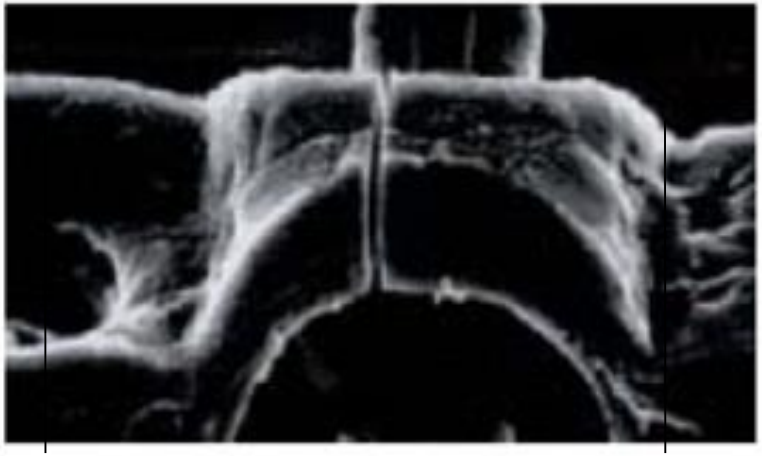


Figure 4.22 Slit-Shaped Void

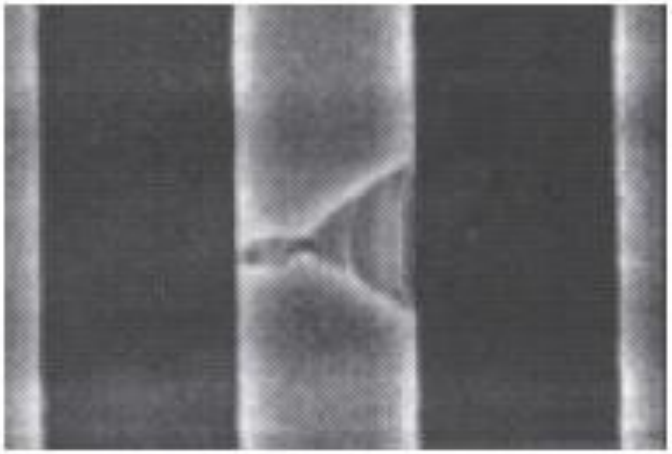


Figure 4.23 Wedge-Shaped Void

Soft error

LSI carries out malfunction !!

Radial rays
-Neutron
-Alpha rays

Alpha particle collide with atom of silicon

For cosmic (neutron) rays irradiation test, cyclotron is used.

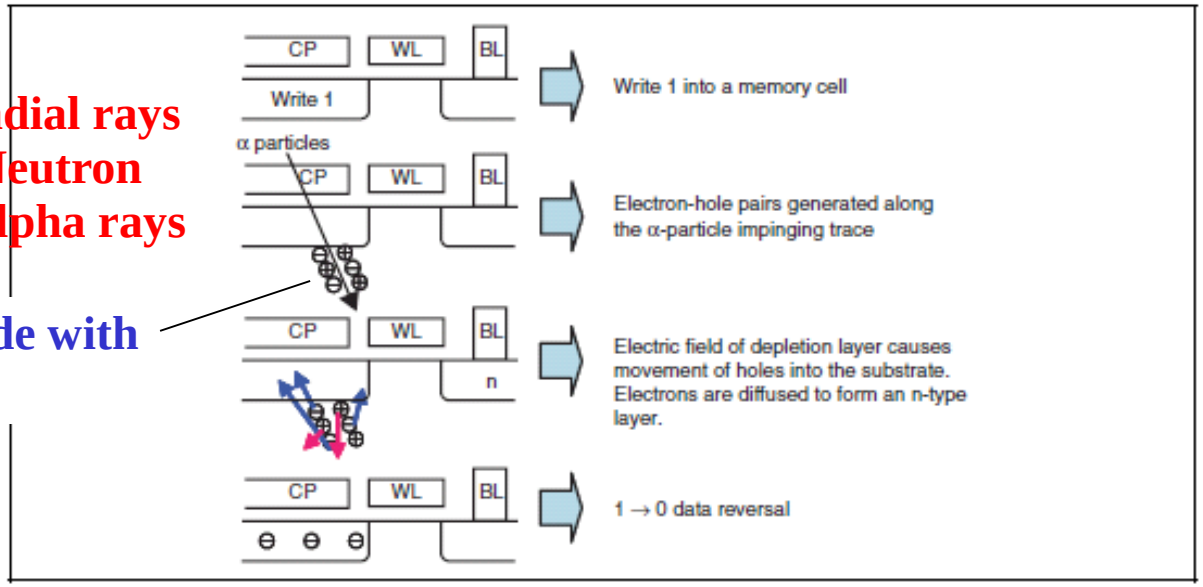


Figure 4.24 Incorrect Operation in Memory Cell

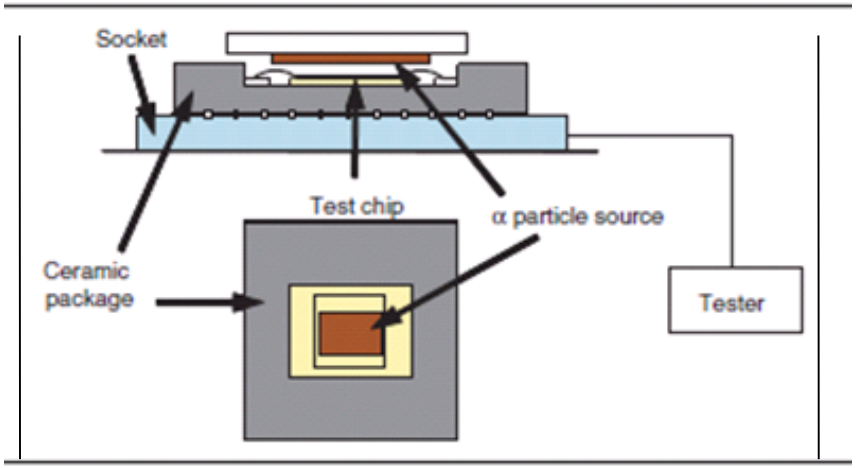


Figure 4.25 Accelerated Soft Error Evaluation System

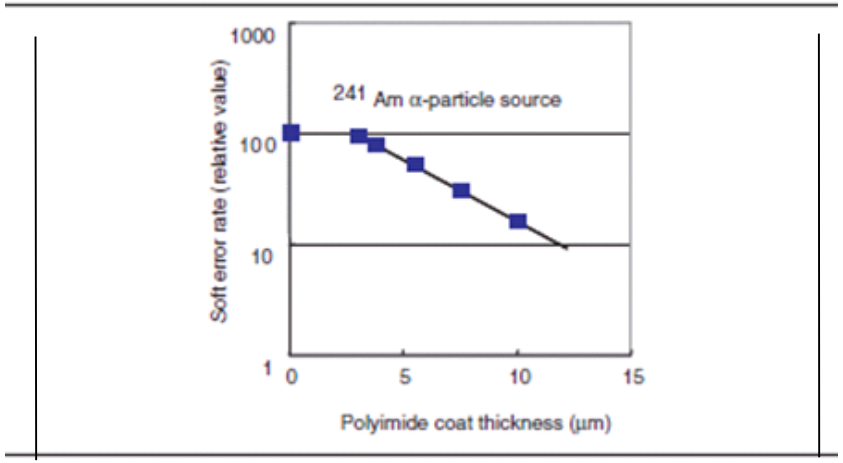


Figure 4.26 Soft Error Prevention Effect of Polyimide Coating

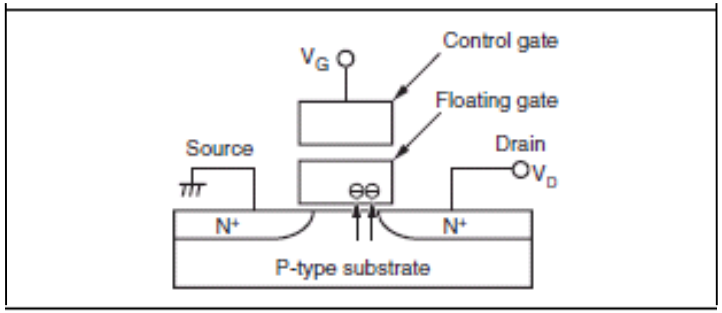


Figure 4.27 Stack Type Memory Cell Cross-section

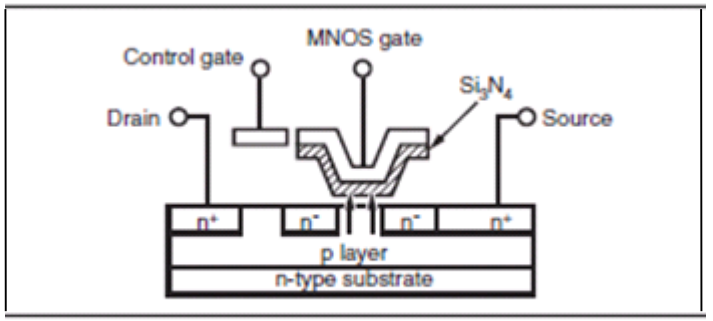


Figure 4.28 MNOS Memory Cell Cross-section

Data retention of Flash memory

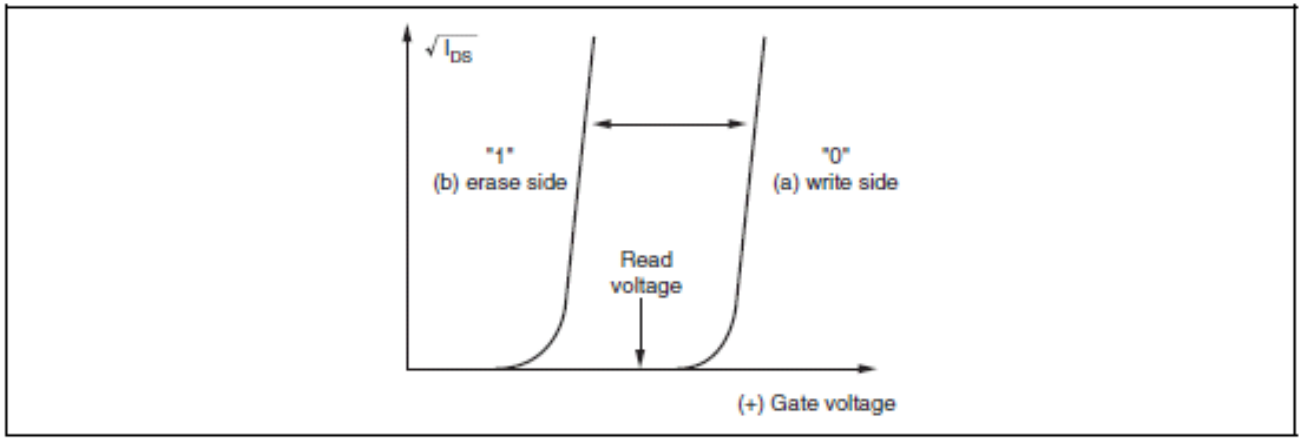


Figure 4.29 Stack-Type Memory Cell Vth Change

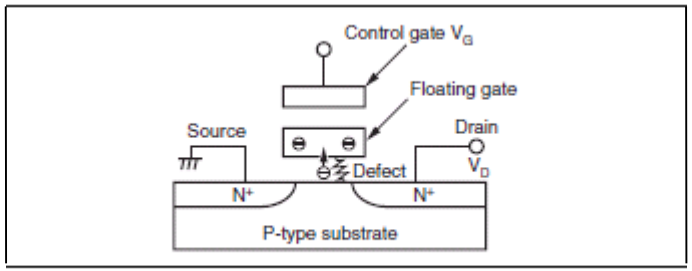


Figure 4.30 Gate Oxide Defect Mode (Charge Gain)

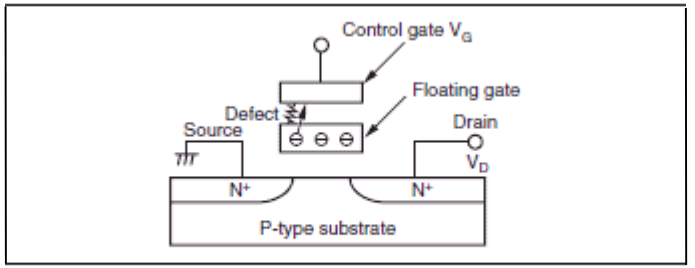


Figure 4.31 Interlayer Film Defect Mode (Charge Loss)

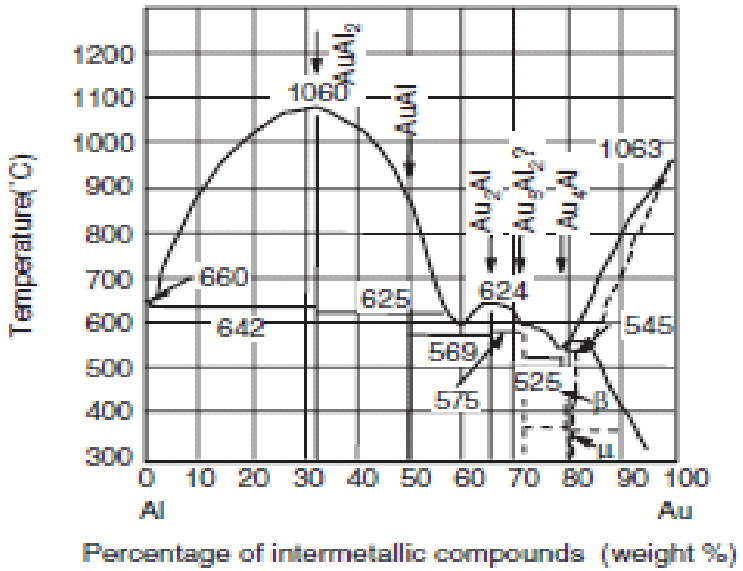


Figure 4.32 Phase Diagram for Au-Al Alloy

Table 4.4 Au-Al Alloy Characteristics

Chemical compound	Crystal structure	Expansion coefficient	Hardness (Hv)	Color
Al	f.c.c.	2.3×10^{-5}	20 to 50	Silver
$AuAl_2$	CaF_2 structure	0.94×10^{-5}	263	Purple
AuAl	ZnS structure	1.20×10^{-5}	249	Gray
Au_2Al	Unknown	1.26×10^{-5}	130	Yellowish golden
Au_5Al_2	γ-brass structure	1.40×10^{-5}	271	Ditto
Au_4Al	β-Mn structure	1.20×10^{-5}	334	Ditto
Au	f.c.c.	1.42×10^{-5}	60 to 90	Gold

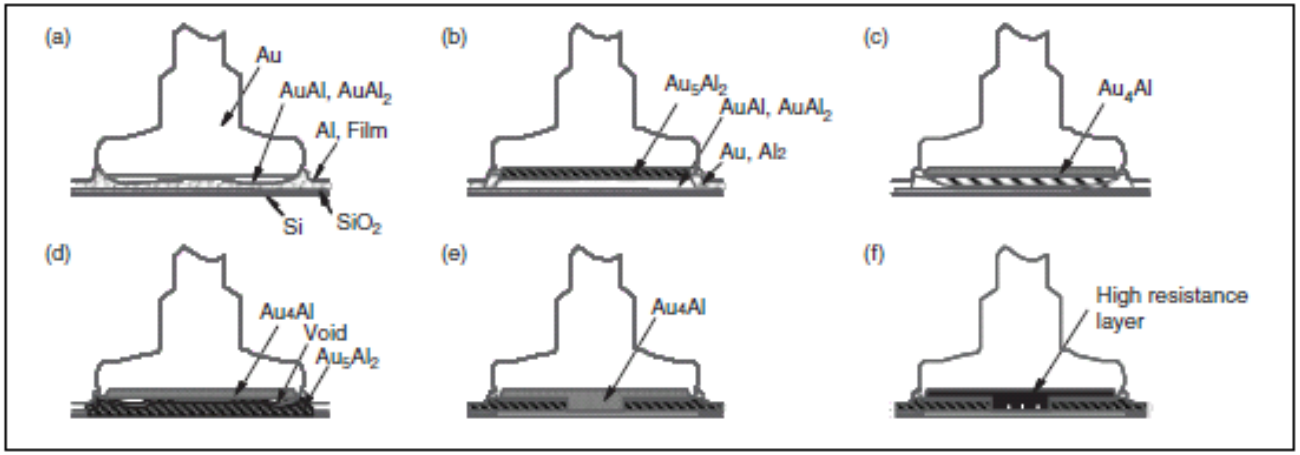
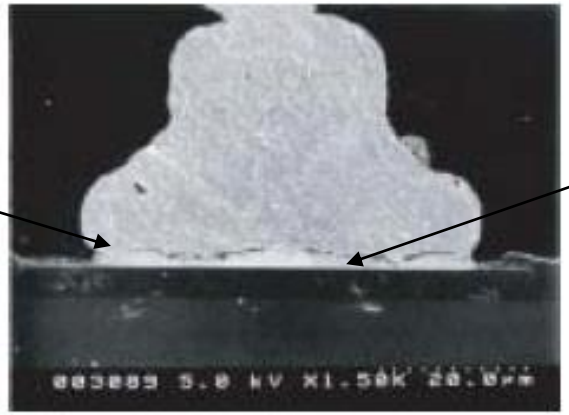


Figure 4.33 Au-Al Alloy State Chart

Halogen ion is supplied from resin by chemical decomposision.



Growing alloys & corrode metals, on condition of high temperature (over 160degC)

Figure 4.34 Cross-section of Au-ball Joint (SEM Image)

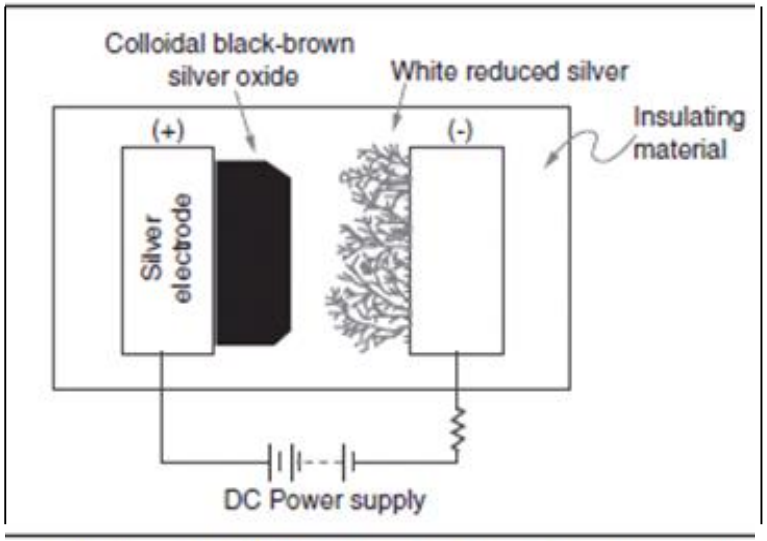


Figure 4.35 Generation of Silver Ion Migration

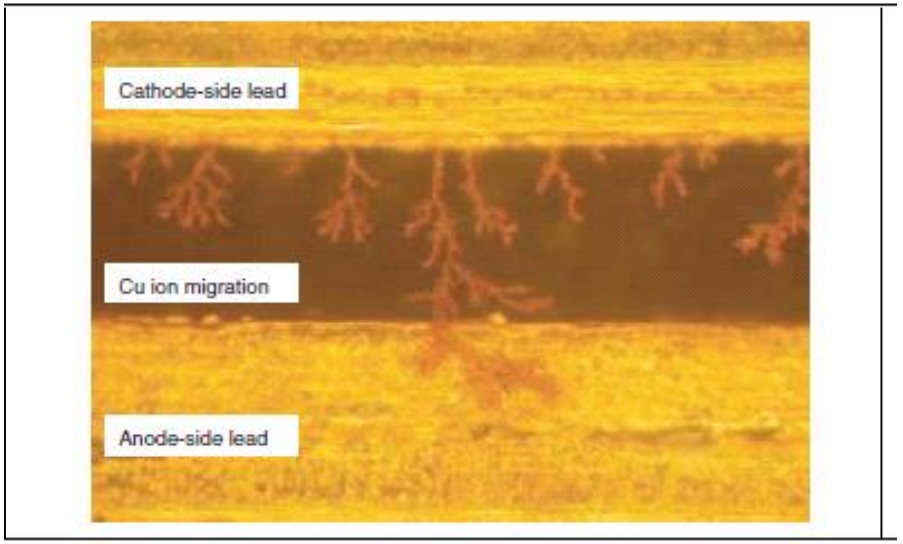


Figure 4.37 Example of Cu Ion Migration between Inner Leads

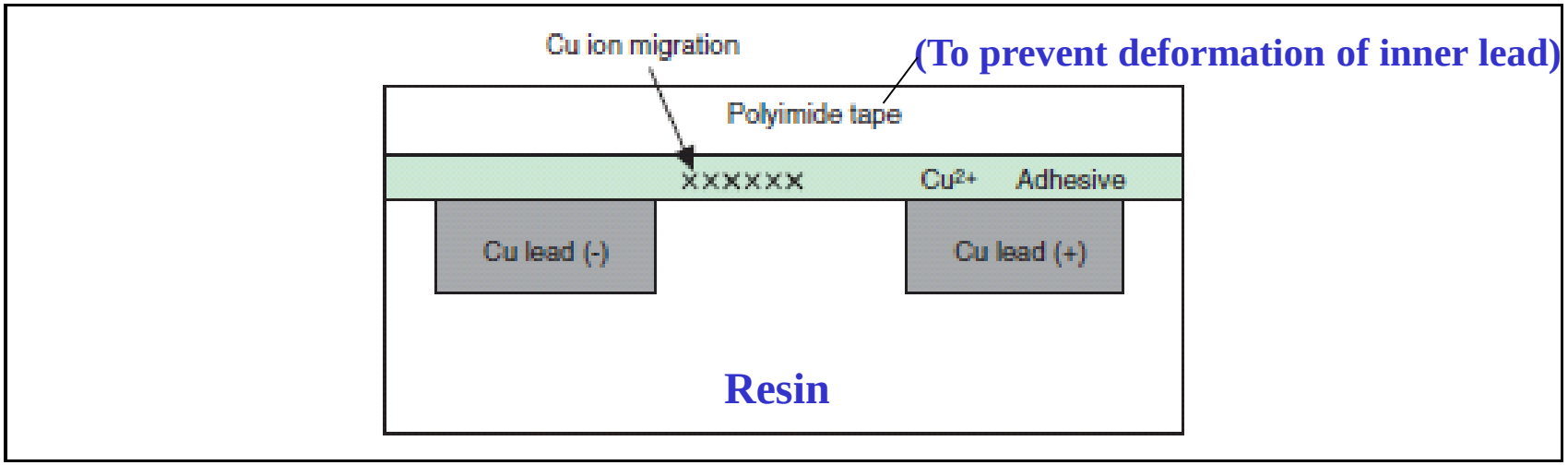


Figure 4.36 Cu Ion Migration (Package Cross-Section)

Force to center of die

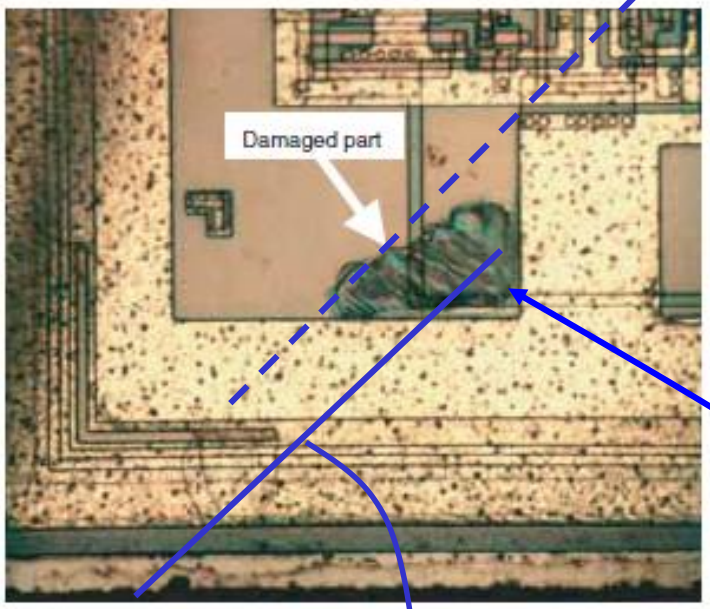
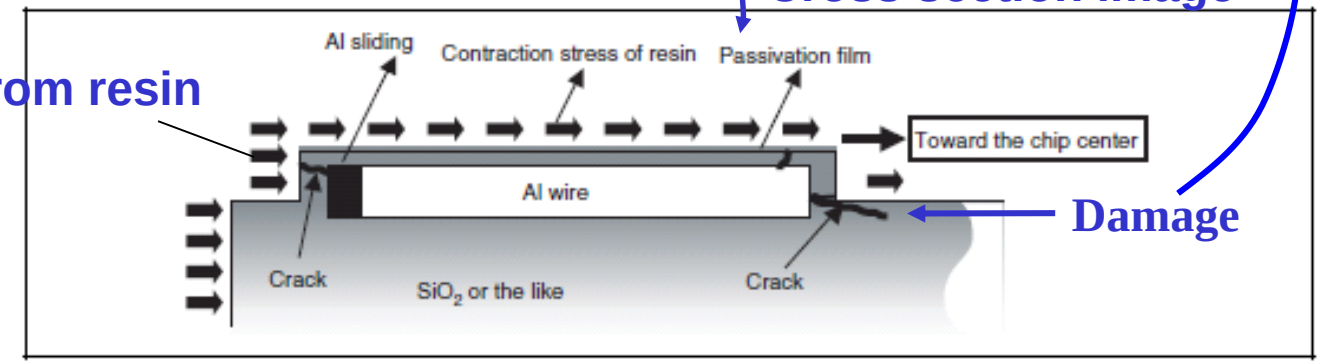


Figure 4.38 Example of Al Sliding

Cross section image

Force from resin



Damage

Figure 4.39 Chip Corner Al Wiring Cross Section

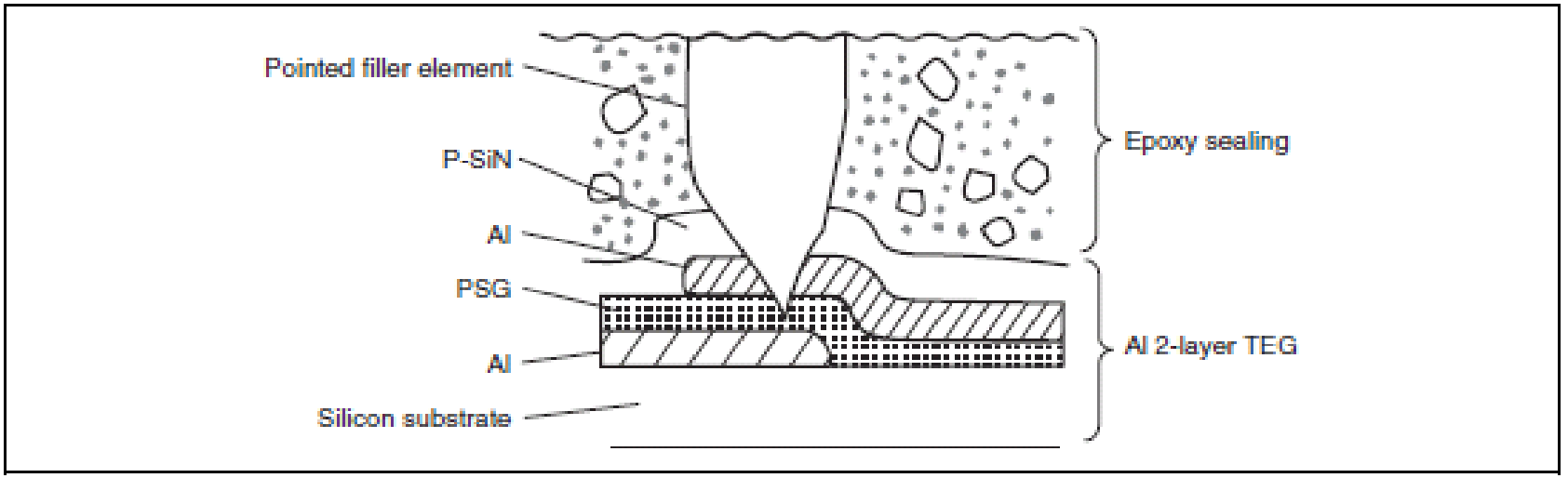


Figure 4.40 Cross Section of a Semiconductor Device in the Vicinity of the Chip Surface

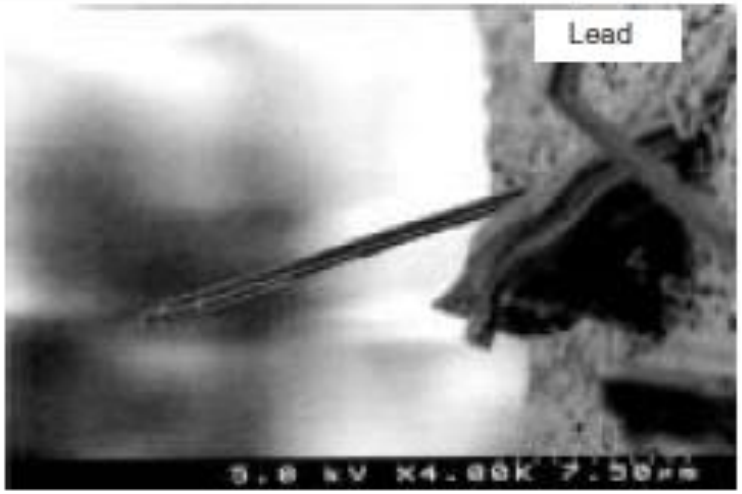


Figure 4.41 Example of Whisker Generation

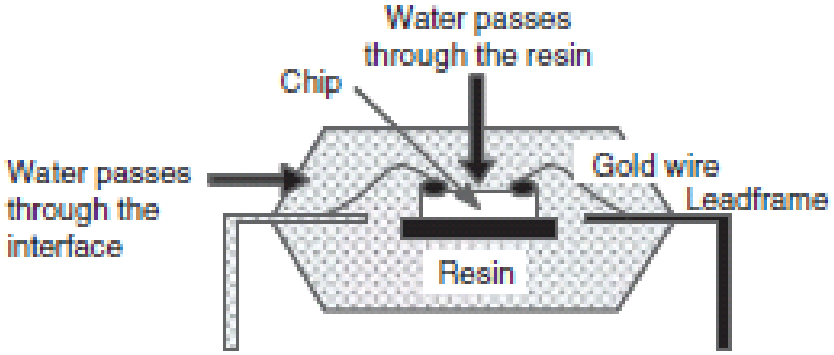


Figure 4.42 Water Penetration Path in a Plastic Mold Device

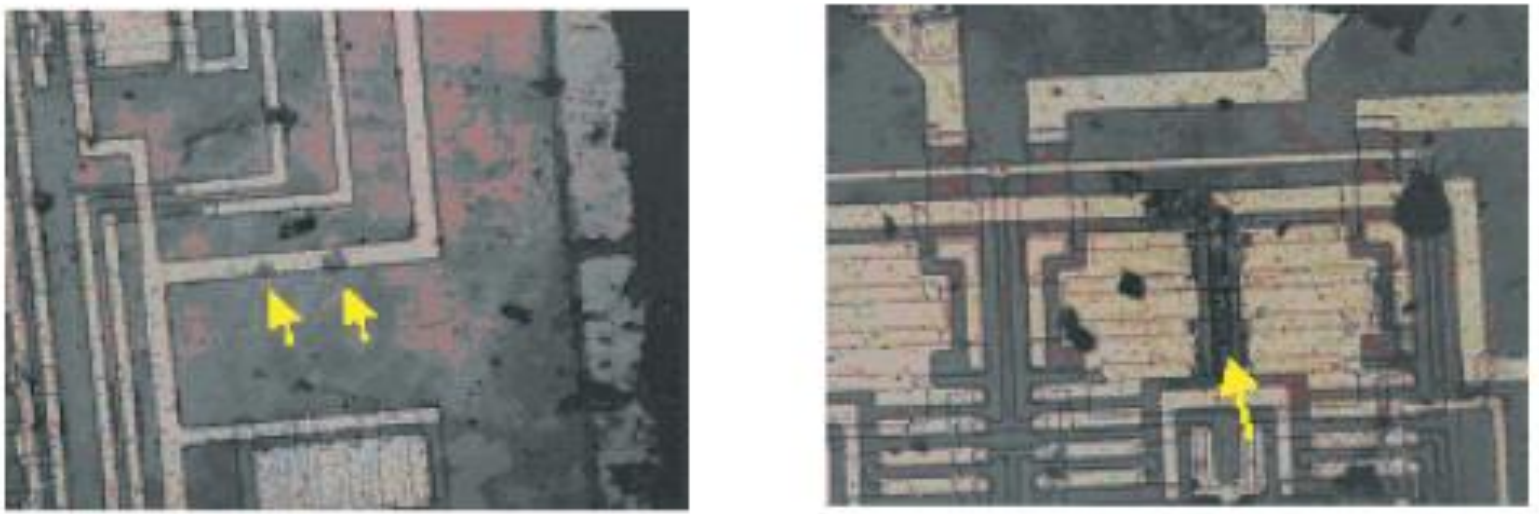


Figure 4.43 Al Corrosion During Storage with High Humidity and High Temperature

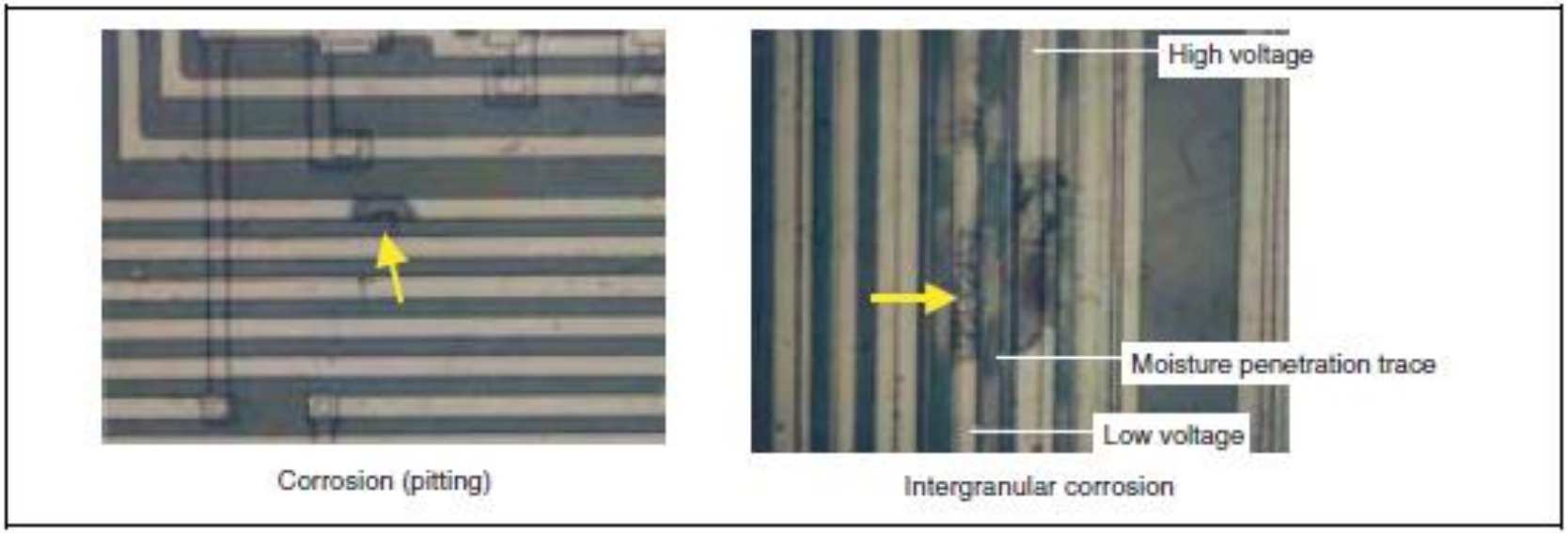


Figure 4.44 Al Corrosion on High Humidity and High Temperature Bias

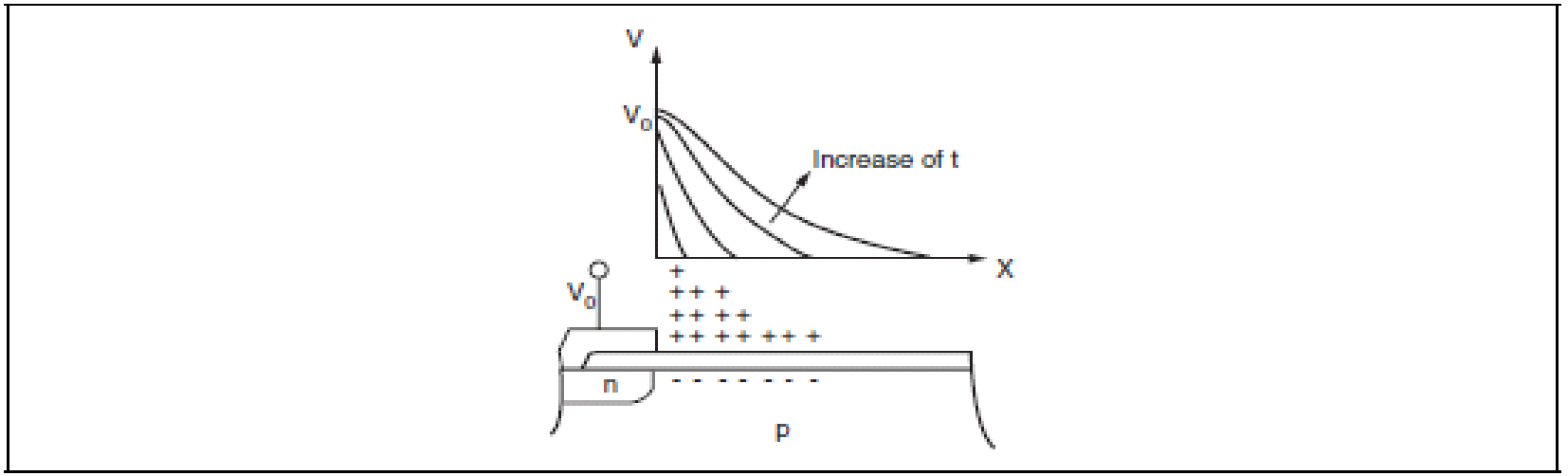


Figure 4.45 Surface Charge Expansion Phenomenon

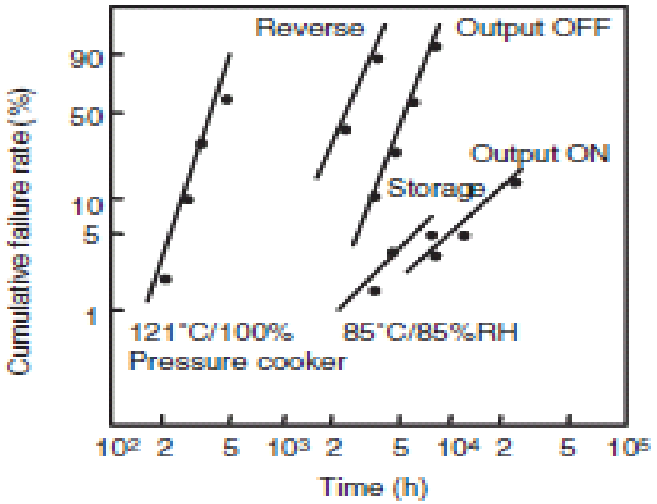


Figure 4.46 Effects of Bias Application Conditions

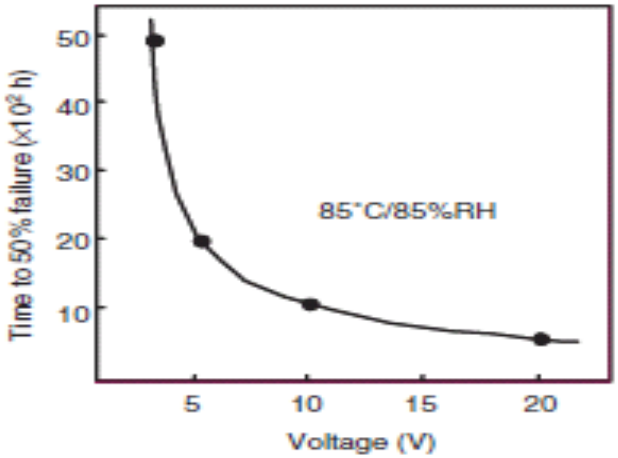


Figure 4.47 Effects of Bias Voltages

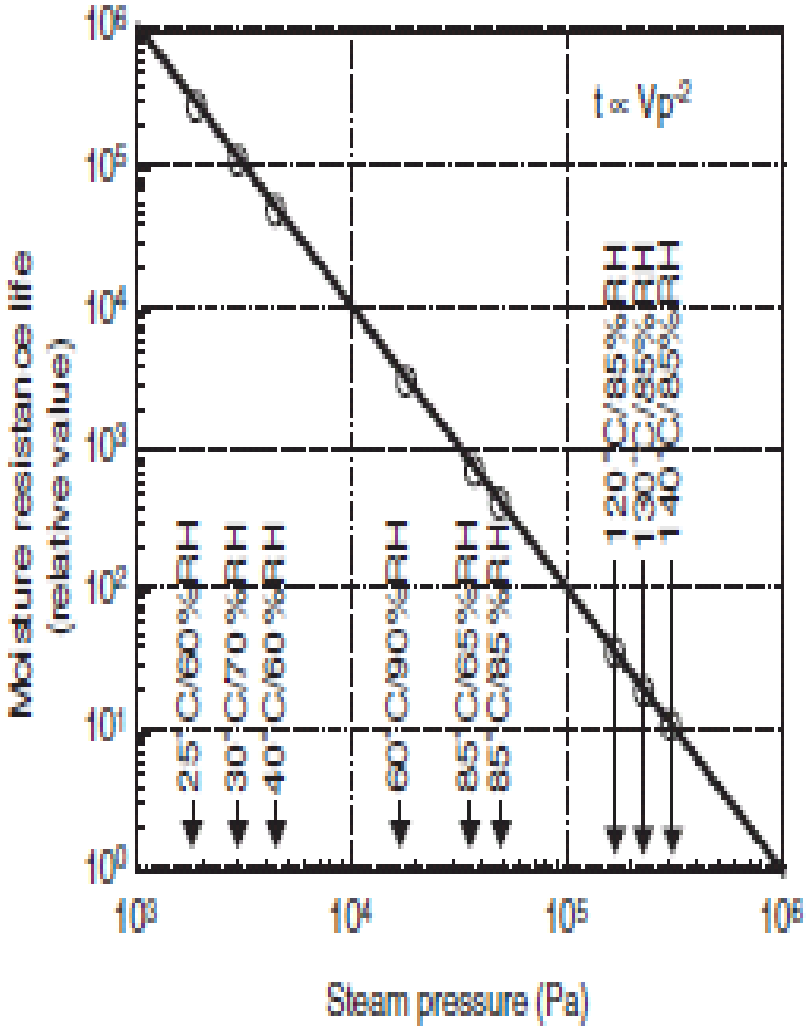


Figure 4.48 Example of Acceleration

Table 4.5 Major Methods for Evaluatating the Moisture Resistance

Evaluation method	Example of test conditions	Features
High temperature and high humidity storage test	85°C/85%RH	Has substantial correlation with actual conditions of use. Requires a long time for the evaluation.
High temperature and high humidity bias test	85°C/85%RH/ with bias applied	Has substantial correlation with actual conditions of use. Requires a long time for the evaluation.
Pressure cooker storage test	130°C/85%RH	Has substantial correlation with actual conditions of use.
Pressure cooker bias test (HAST)	110°C/85%RH/ with bias applied 120°C/85%RH/ with bias applied 130°C/85%RH/ with bias applied	Has substantial correlation with actual conditions of use. Allows the effects of the biasing to be evaluated.

Note: The saturation-type pressure cooker storage test (100% RH) is not recommended due to market correlation problems.

Soldering heat problem of SMDs

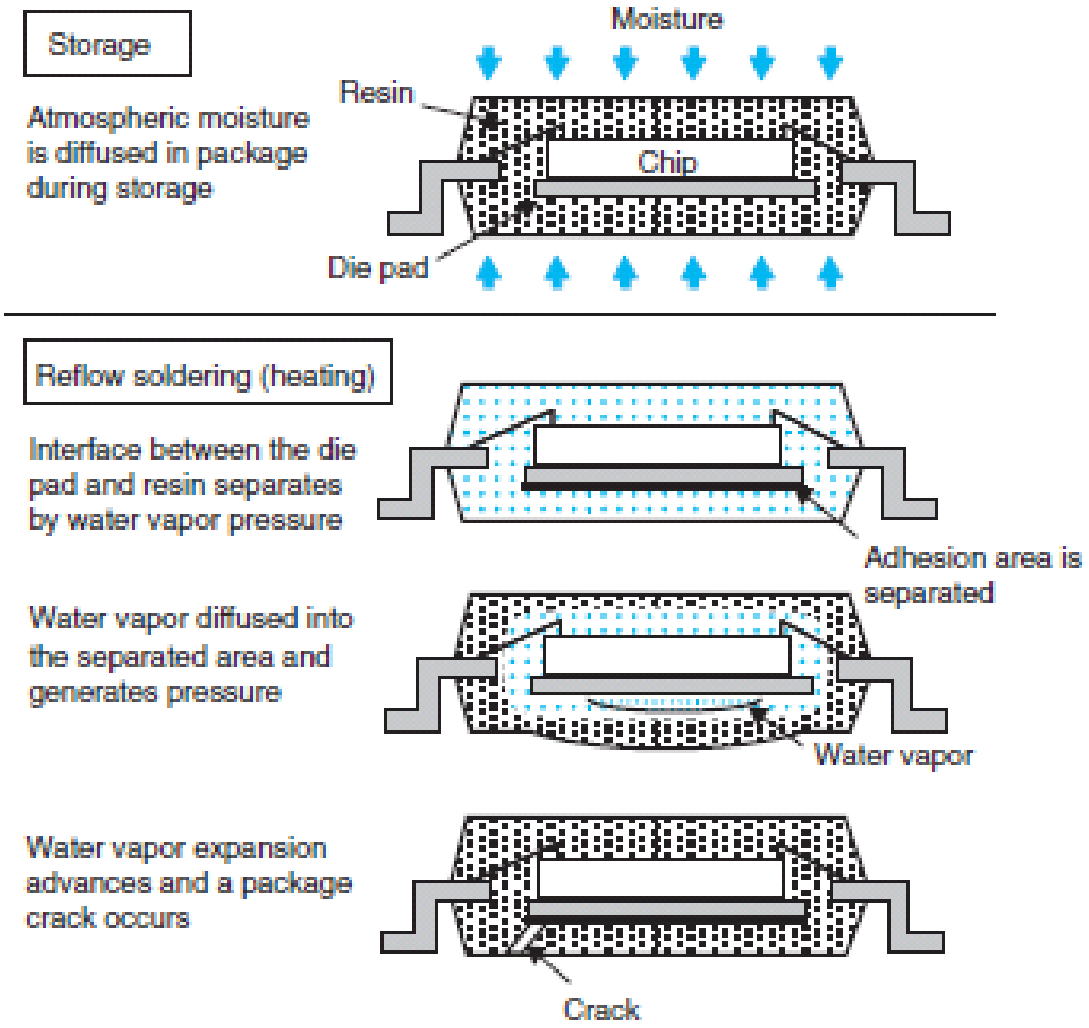


Figure 4.49 Model of Crack Generation in Reflow Soldering[54]

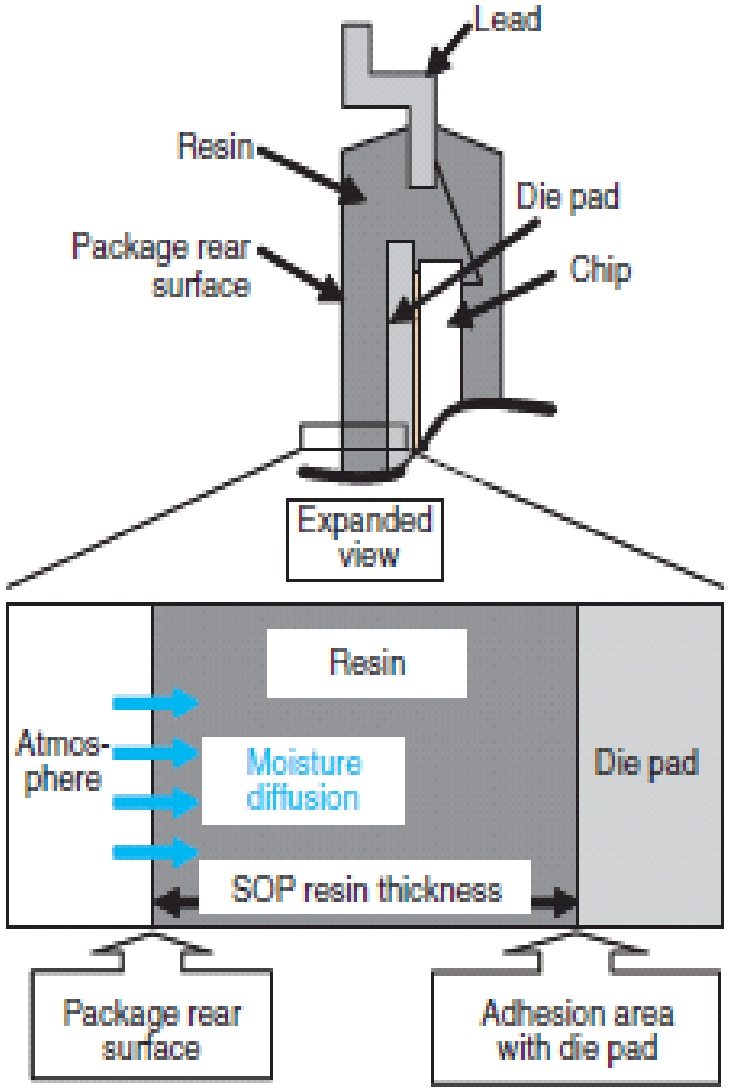


Figure 4.50 Model of Moisture Diffusion at Humidification[54]

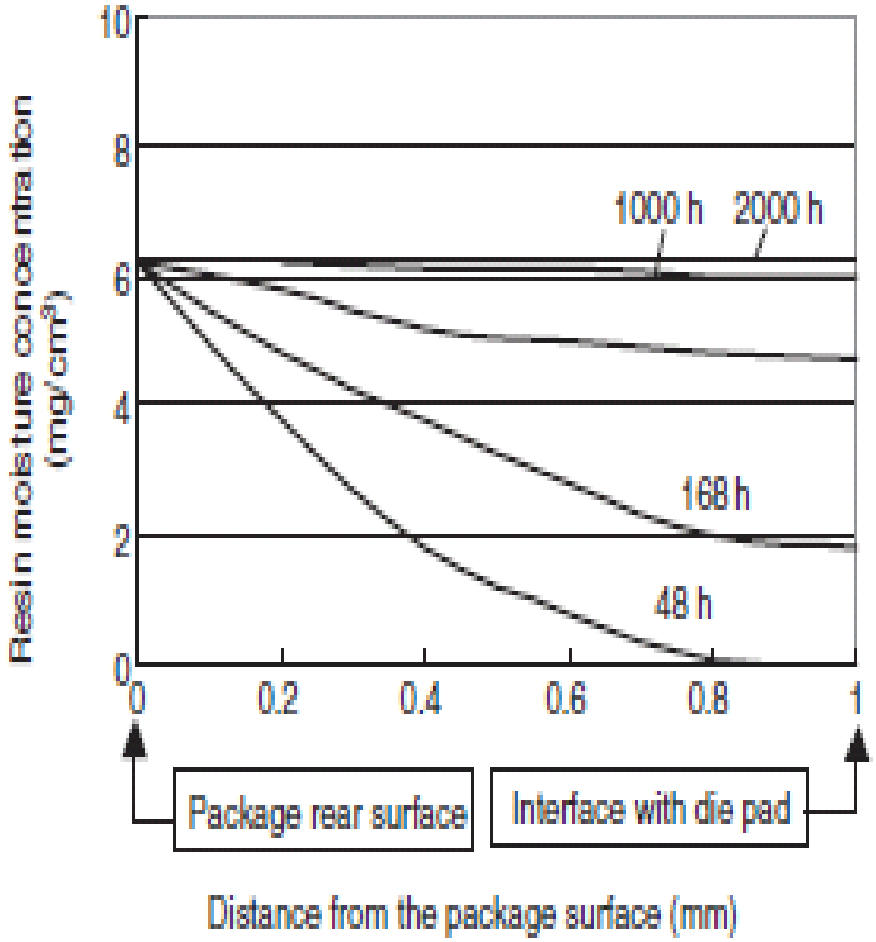


Figure 4.51 Example of Calculations of the Progress of Moisture Absorption for 1-mm Resin Thickness[54]

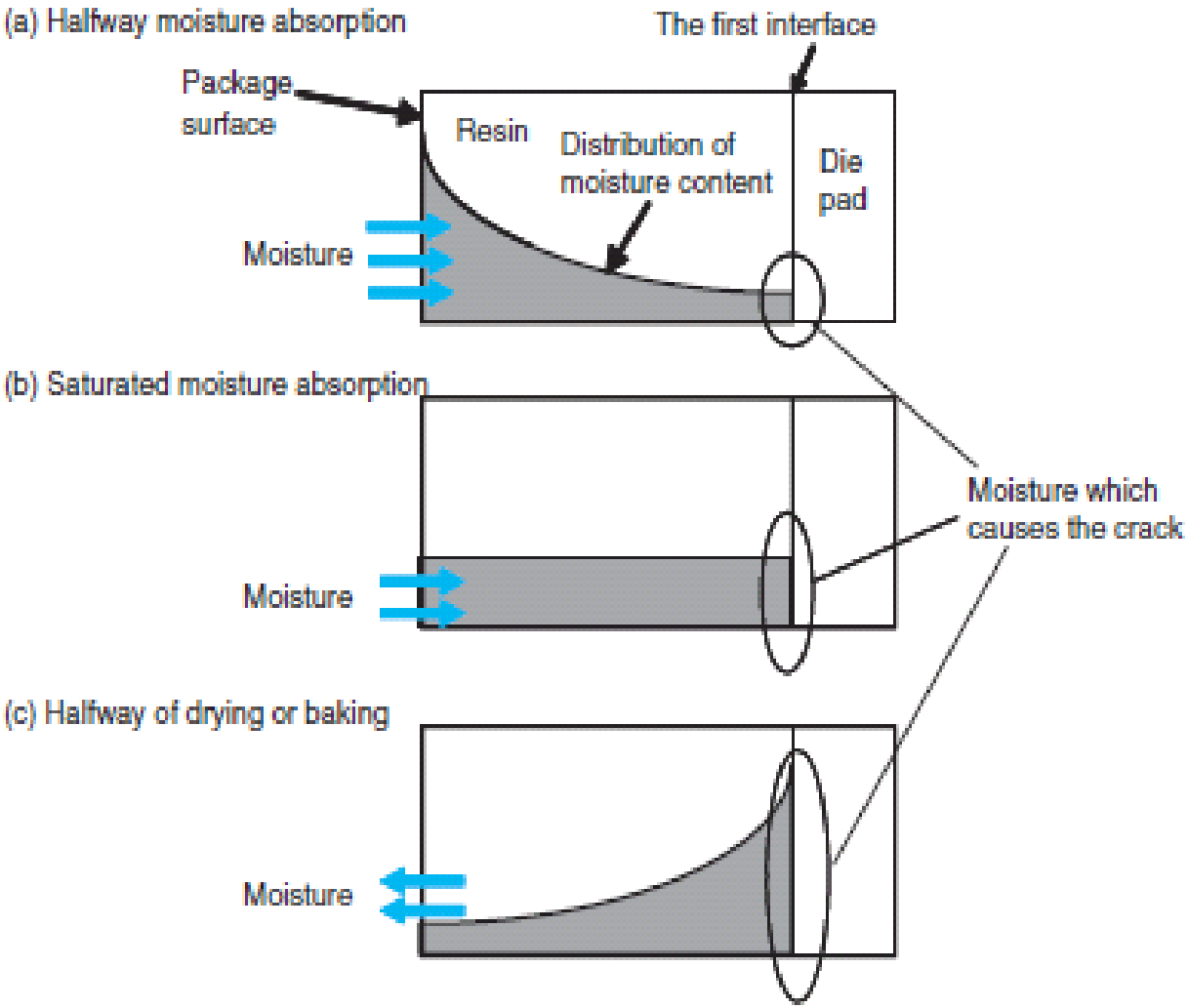


Figure 4.52 Moisture Distribution in Packages in Respective Stages (Comparison When Moisture Absorptivity Comparable)

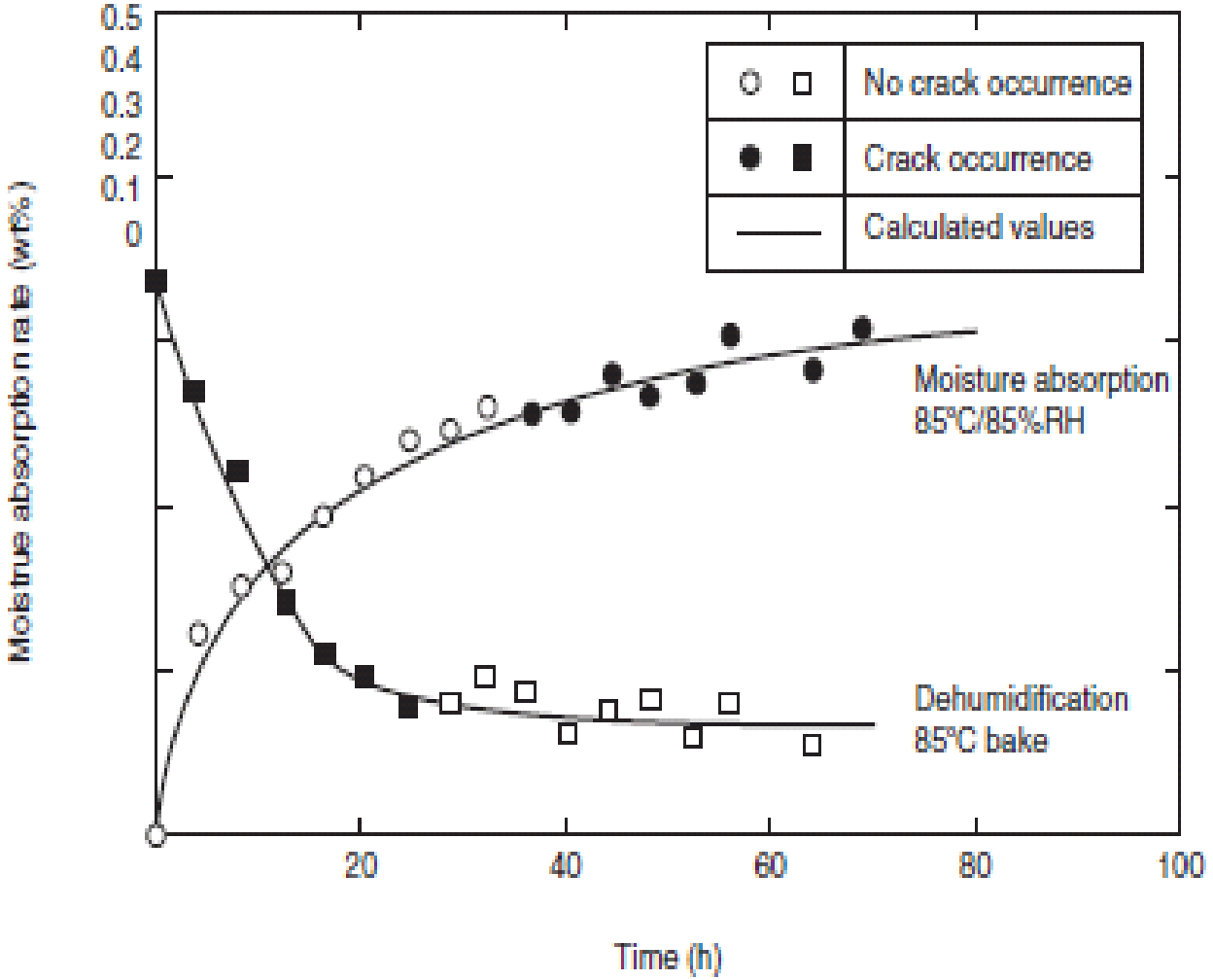


Figure 4.53 Moisture Absorptivity Changes for Moisture Absorption/Drying and Results of VPS Heating[56]

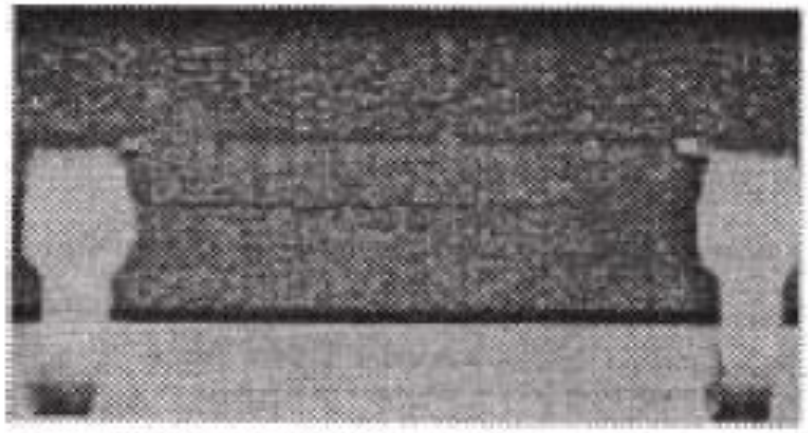
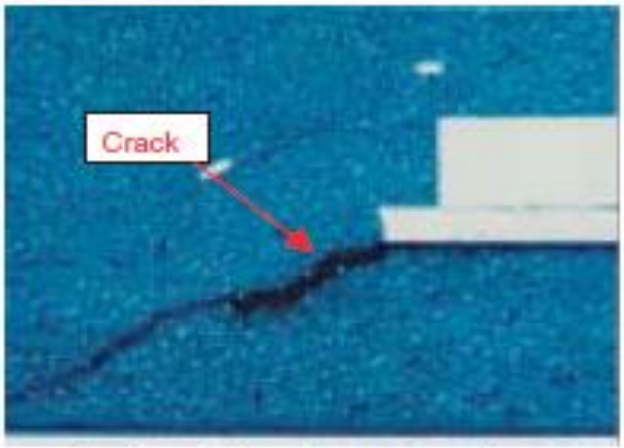


Figure 4.54 Example of Observing External Cracks with a Microscope



Cracks on the package rear surface
(no electrical effects)

Cracks on the package top surface
(wire disconnection with electrical effects)

Figure 4.55 Example of Observing Internal Cracks/Delamination by Cross-Section Polishing[59]

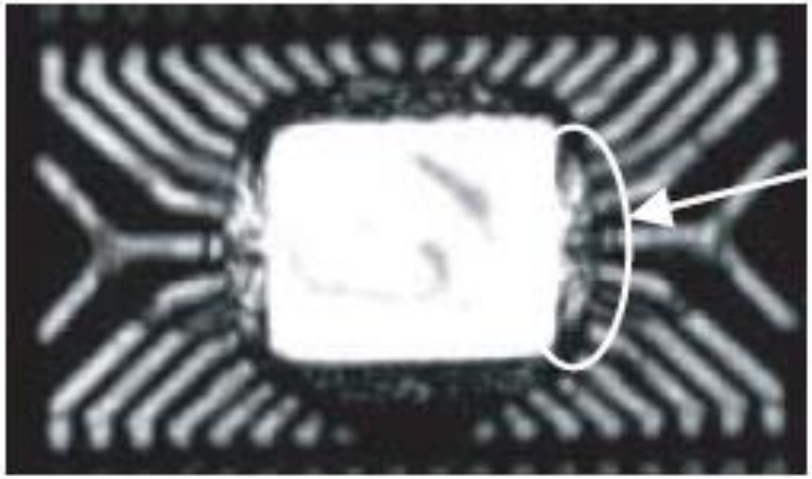
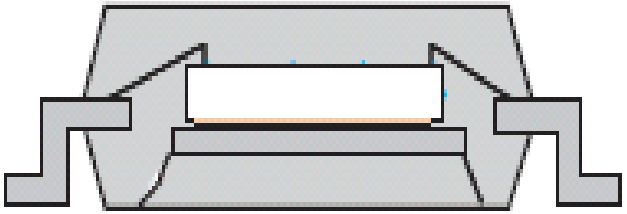
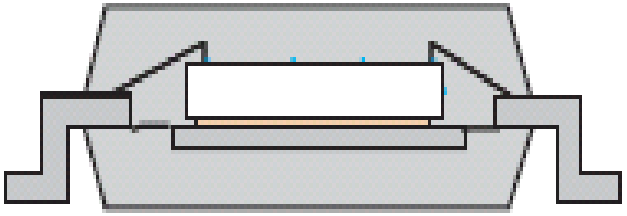


Figure 4.56 Example of Observing Internal Cracks/Delamination by SAT

Table 4.6 Package Cracking Types and Problems[59]

No.	Package Crack Type	Shape	Problems
1	Package rear-surface crack		. Moisture resistivity degradation (least degradation)
2	Package side crack		. Moisture resistivity degradation (small degradation)
3	Crack intersecting a bounding wire		. Wire damage, open . Moisture resistivity degradation
4	Package top-surface crack		. Wire damage, open . Wire bond peeled off . Moisture resistivity degradation

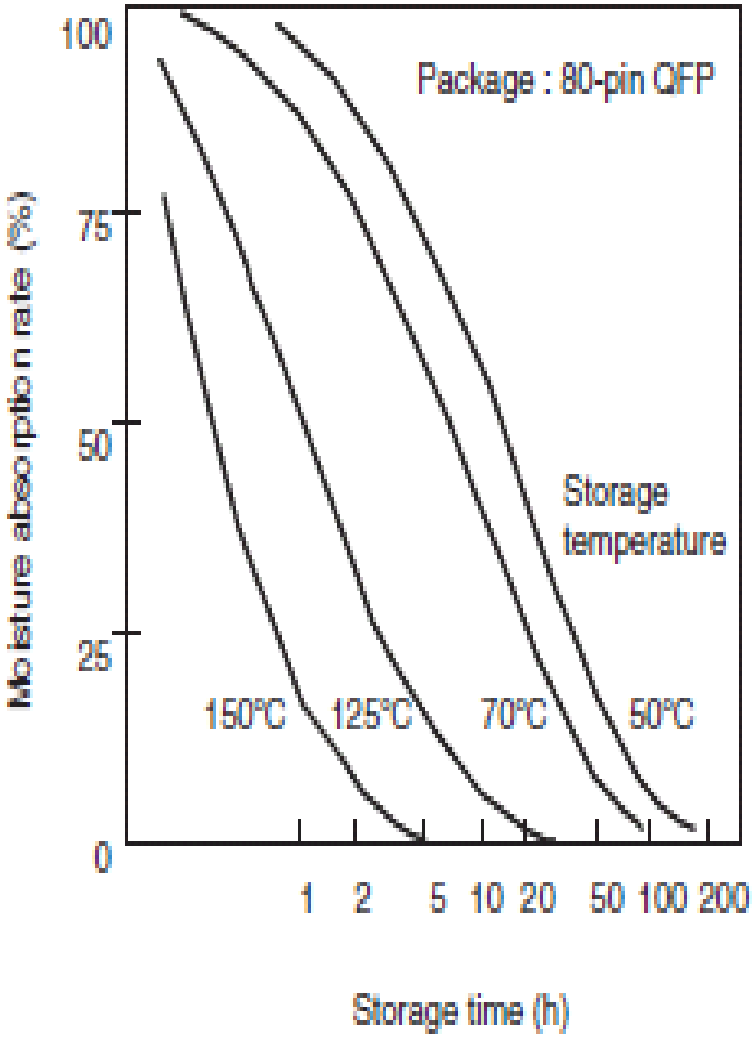


Figure 4.57 Dehumidification of Plastic Packages

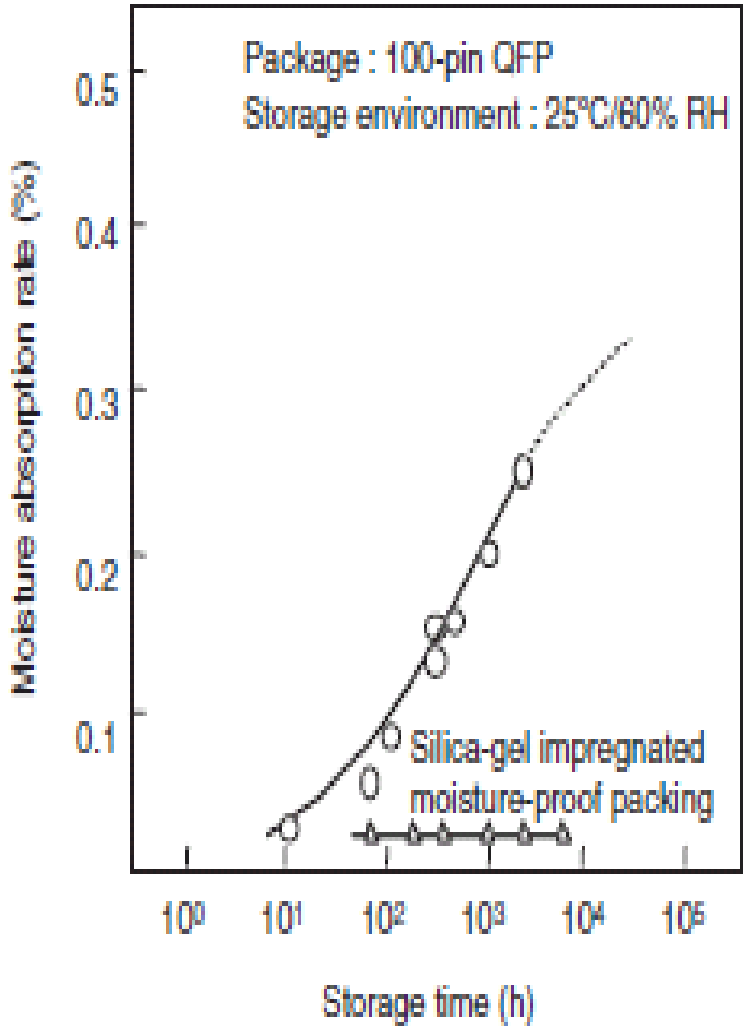


Figure 4.58 Effect of the Moisture-proof Pack

Table 4.7 Allowable Storage Conditions for Unpacked Moisture-Proof Packing

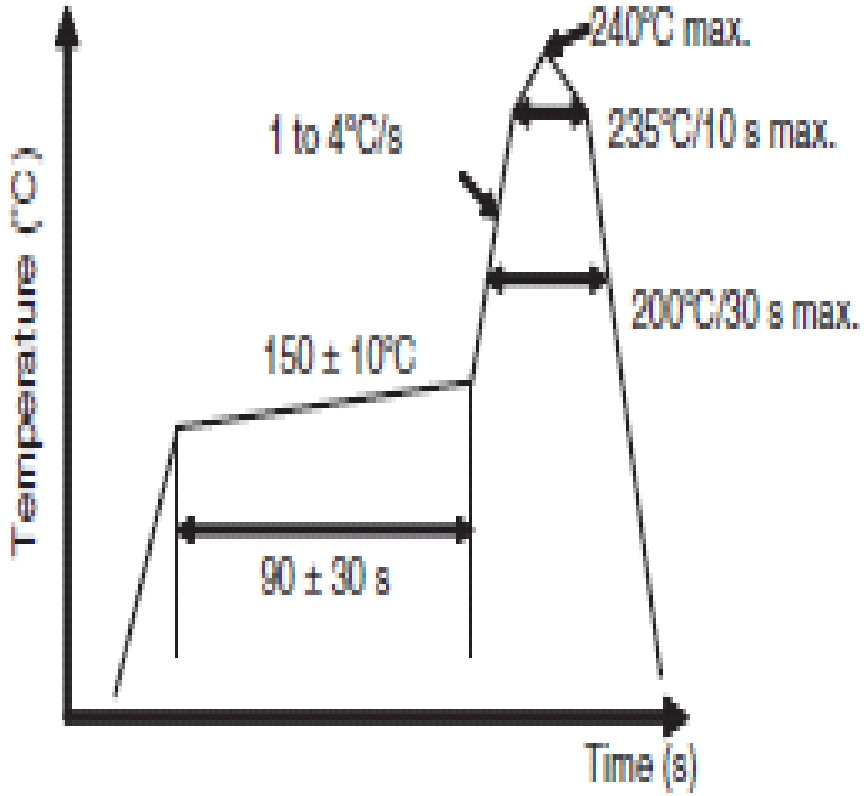
Level*1	JEDEC*2	Humidification Conditions	Classification	Storage Conditions after Unpacking
A	1	85°C, 85%, 168-hour storage	No moisture-proof packing required	30°C or less and 85% or less
B	2	85°C, 65%, 168-hour storage	1 year or less after unpacking	30°C or less and 70% or less
C	2a	30°C, 70%, (4 weeks + X) storage*3	4 weeks or less after unpacking	30°C or less and 70% or less
D	—	30°C, 70%, (2 weeks + X) storage*3	2 weeks or less after unpacking	30°C or less and 70% or less
E	3	30°C, 70%, (1 week + X) storage*3	1 week or less after unpacking	30°C or less and 70% or less
F	4	30°C, 70%, (72 hours + X) storage*3	3 days or less after unpacking	30°C or less and 70% or less
G	5	30°C, 70%, (48 hours + X) storage*3	2 days or less after unpacking	30°C or less and 70% or less
S	6	30°C, 70%, (Y + X) storage*3	Y days or less after unpacking	30°C or less and 70% or less

Notes: 1. Complies with JEITA standard EIAJ ED-4701/301 "Soldering Heat-Resistance Test (SMD)."

2. JEDEC-STD-020 levels corresponding to the moisture-sensitivity level (MSL) with moisture absorption conditions of 30°C, 60%.

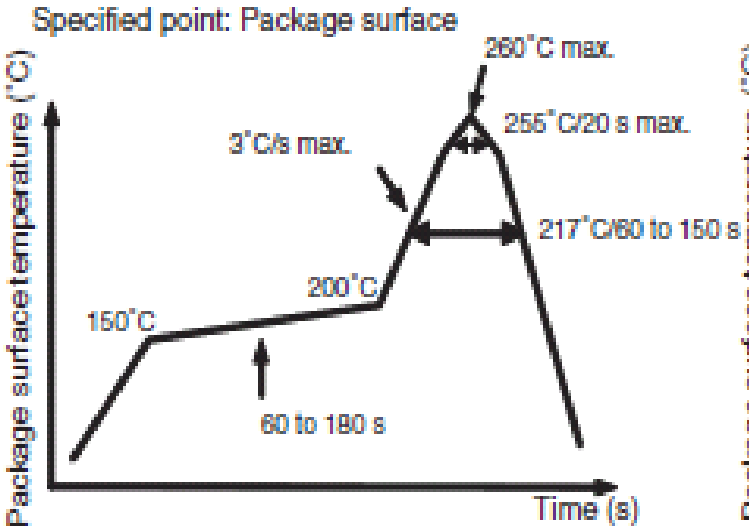
3. X: Period of time including the storage time to moisture-proof packing after assembly and the storage time after packing.

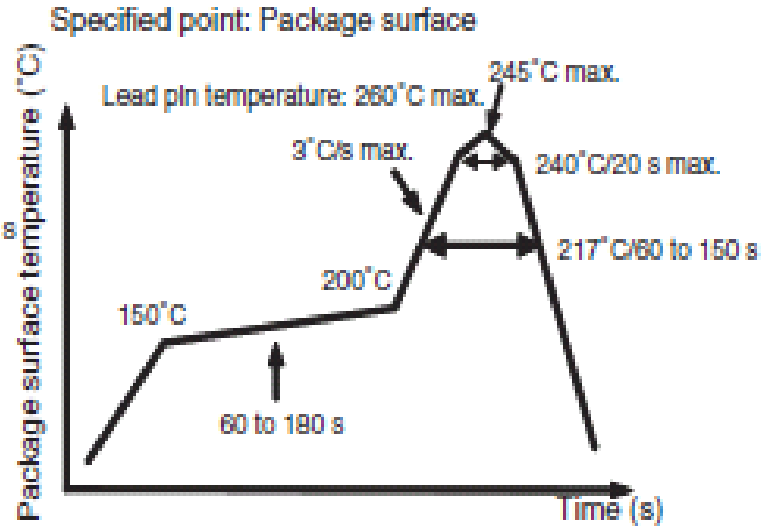
Y: Length of warranty period of unpacked storage after delivery



Note: For packages with a capacity of 2000 mm^3 or more
Peak temperature: 225°C max.
Retention at 220°C: 10 s max.

Figure 4.59 Reflow Heating Conditions for Eutectic Paste for Surface Mount Devices (Package Surface Temperature)





Target packages: Small, Thin Package

QFP (less than 28 mm□), LQFP, TQFP, SOP, TSOP, TSSOP, BGA, CSP (FBGA), MPAK, CMPAK, SRP, URP, UFP, TEFP, LFPA, etc.

Target packages: Large, Thick Pacakge

QFP (28 mm□ or larger), QFJ, DPAK, LDPAK, HSOP, HTQFP1010, and RP8P

Notes: 1. During the storage period after opening the moisture-proof packing until reflow mounting, storage conditions are 30°C/70% RH or less according to Renesas conventional moisture conditions. However, when following to the MSL standard of IPC/JEDEC, the storage conditions are 30°C/60% RH or less.

2. The reflow condition for the large and thick packages, more than 28 mm x 28 mm, installed heat sink is shown below.
Peak temperature: 240°C max.
Soldering temperature/time: 220°C or more/30 to 50 s
Pre-heating: 150 to 180°C/60 to 120 s

Figure 4.60 Reflow Heating Conditions for Pb-Free Paste for Surface Mount Devices (Package Surface Temperature)

Table 4.8 MOS Device Failure Types from the Standpoint of Electric Stress Factors

Failure Mechanism	Stress Factors	Failure Modes
Bonding wire disconnection due to melting	EOS*	Occurred by high current. The broken ends of wire are rounded.
Melting metal disconnection	Mainly EOS	Occurred by high current. Metal balls as in electromigration are not seen.
Melting polysilicon disconnection	EOS or ESD	For polysilicon, as resistance values are large, power concentrates and melting occurs easily.
Contact section damage	EOS or ESD	Due to reverse bias current in junction, heat is transferred to contact section and aluminum metallization melts.
Heat degradation of oxide film	EOS or ESD	Junction reverse bias current heat is transferred to oxide film, resulting in degradation.
Junction degradation	EOS or ESD	Occurred by junction reverse bias current heat and the like
Hot electron, Trapping	EOS or ESD	Carriers accelerated by high electric fields are trapped in MOS transistor oxide films
Oxide film degradation due to electric field	Mainly EOS	Occurred by application of voltage to gate oxide film

Note: * EOS: Electrical overstress

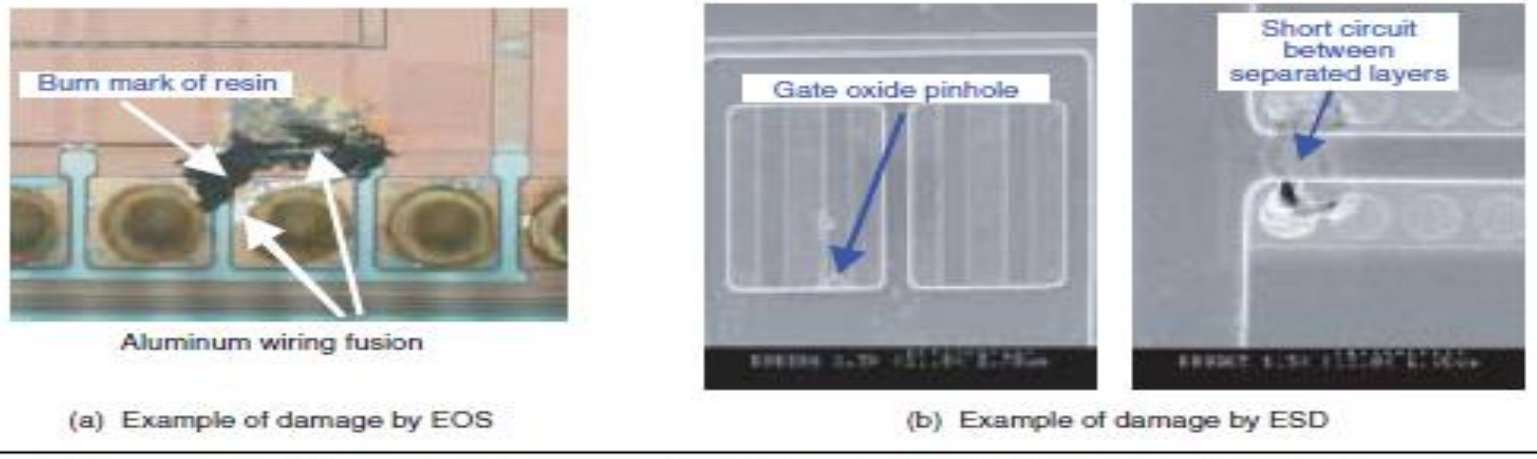


Figure 4.61 Example of Comparison between EOS Damage and ESD Damage

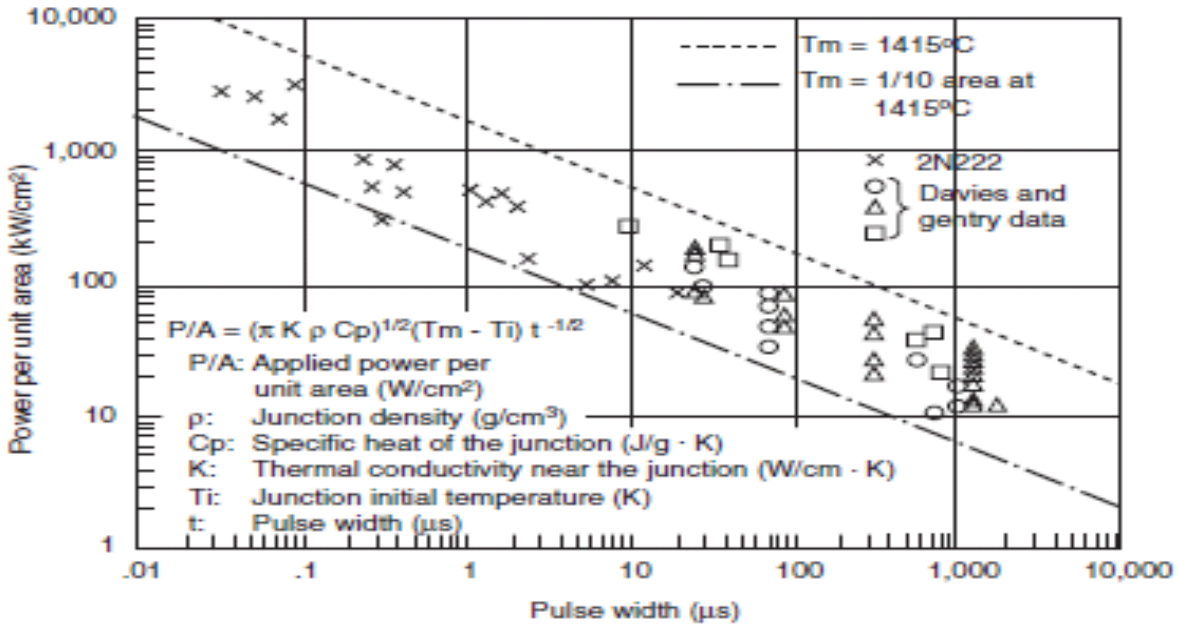


Figure 4.62 Wunsch & Bell Plot

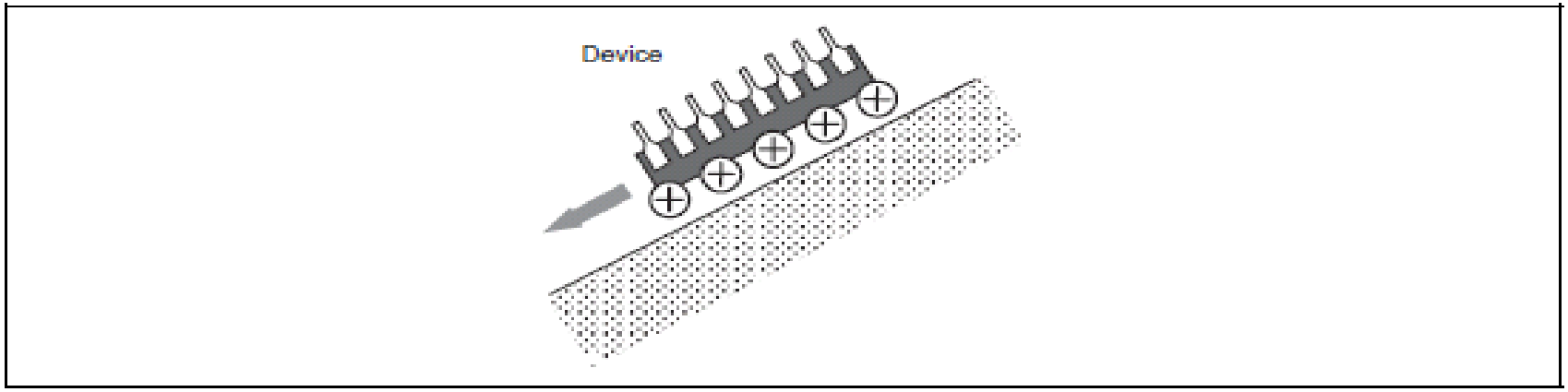


Figure 4.63 Triboelectric Charging

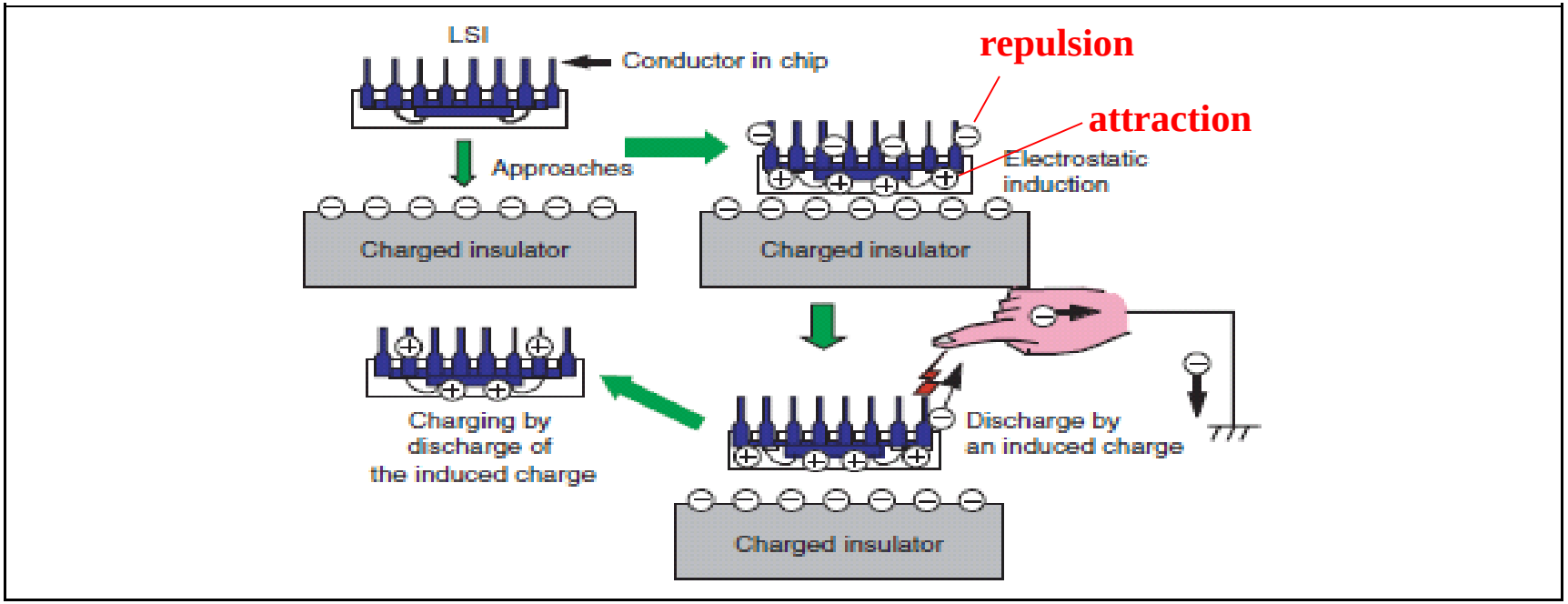


Figure 4.64 Discharge by Electrostatic Induction and Charging

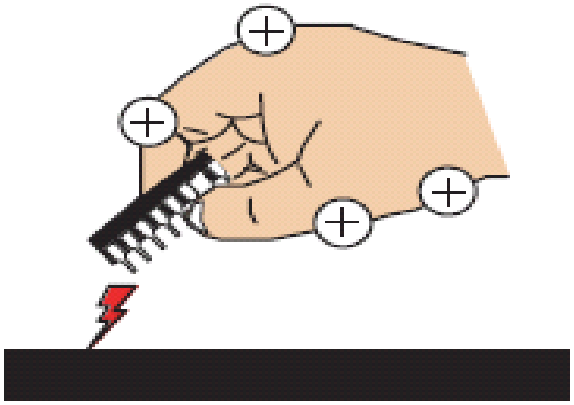


Figure 4.65 Contact Charging and Discharging

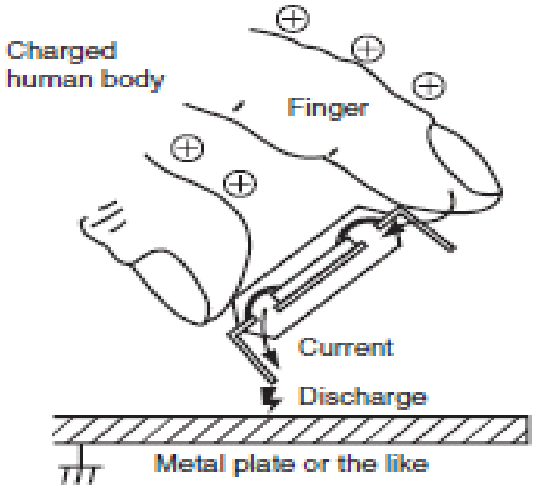


Figure 4.66 Discharge Model with Human Body
(Model in which a Conduction Current Flows between Device Pins)

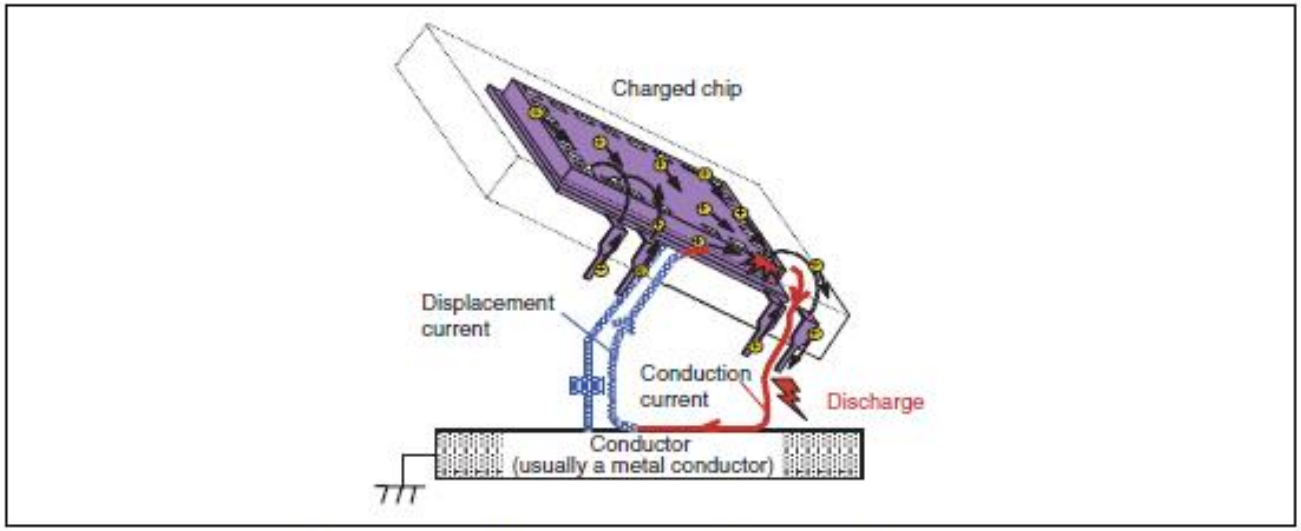
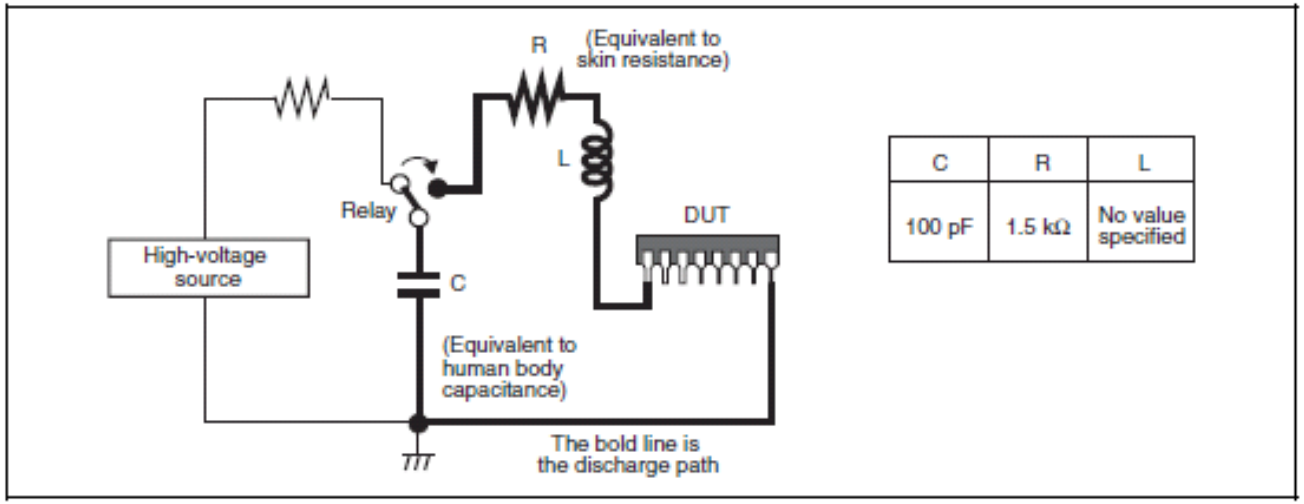
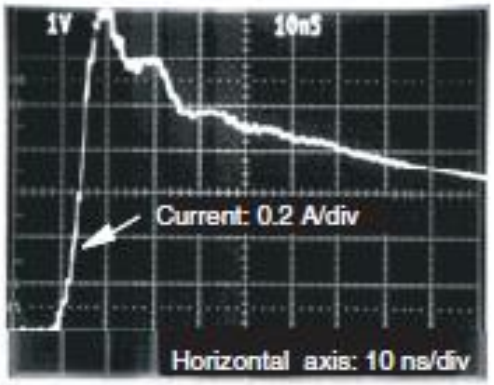


Figure 4.67 Discharge Model for Changed Device (Model in which an Conduction Current Flows to the Discharging Pin and a Displacement Current Flows to the Device Capacitance)

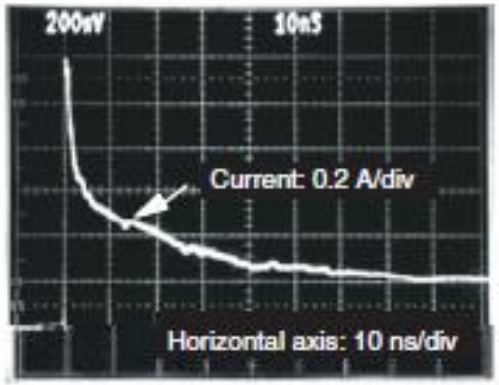


C	R	L
100 pF	1.5 kΩ	No value specified

Figure 4.68 Test Circuit for Human Body Model

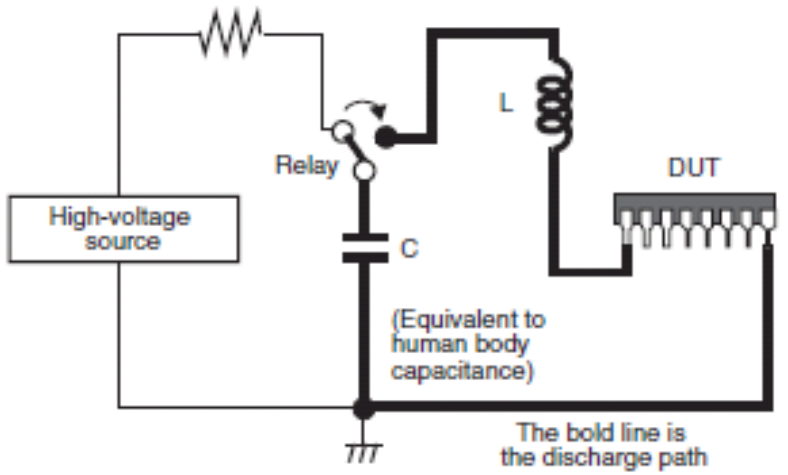


(a) Example of HBM tester discharge current
(conditions: 2000 V, short circuit)



(b) Example of discharge current from a fingertip
(charge voltage of human body: 2000 V)

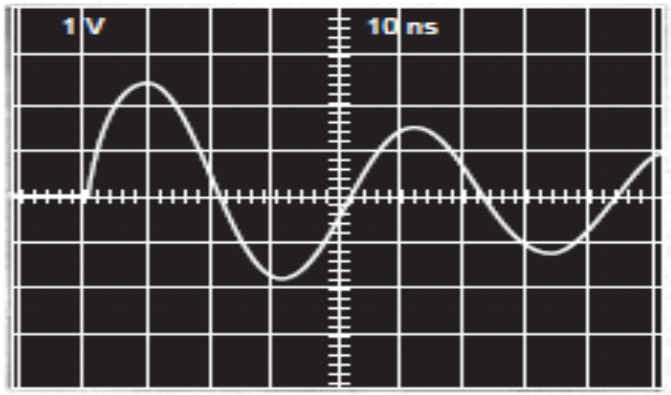
Figure 4.69 Comparison of Human Body and HBM Tester Discharge Currents[72]



C	R	L
200 pF	None (0 Ω)	No value specified*

Note: * The waveform assumes a predefined value of 750 nH.

Figure 4.70 Machine Model Test Circuit



Vertical axis: Current (2 A/div)
Horizontal axis: Time (10 ns/div)

Figure 4.71 Discharge Waveform for Machine Model Test (Example with a Low Inductance L)

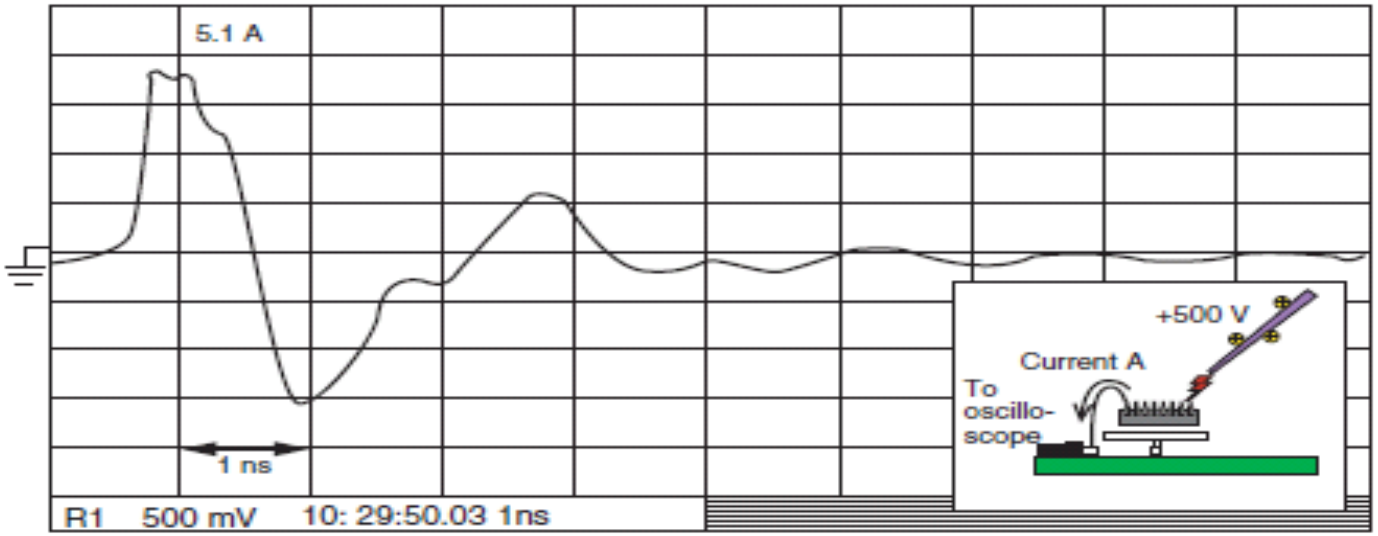


Figure 4.72 Discharge Waveform of Charged Metal Tweezers (Completely Different from That of the Machine Model)

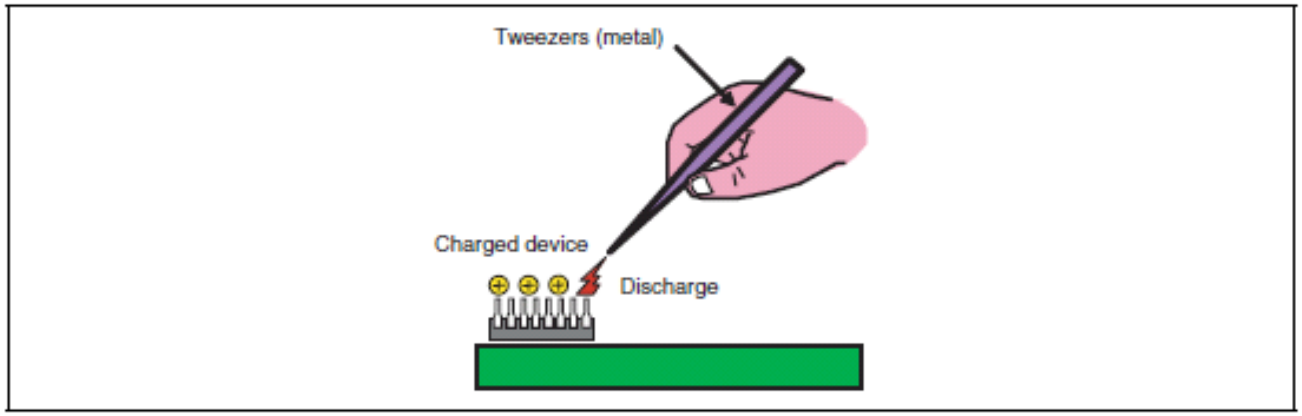


Figure 4.73 Discharge Example of the Charged Device Model (Example of a Discharge to a Metal Tool or the Like)

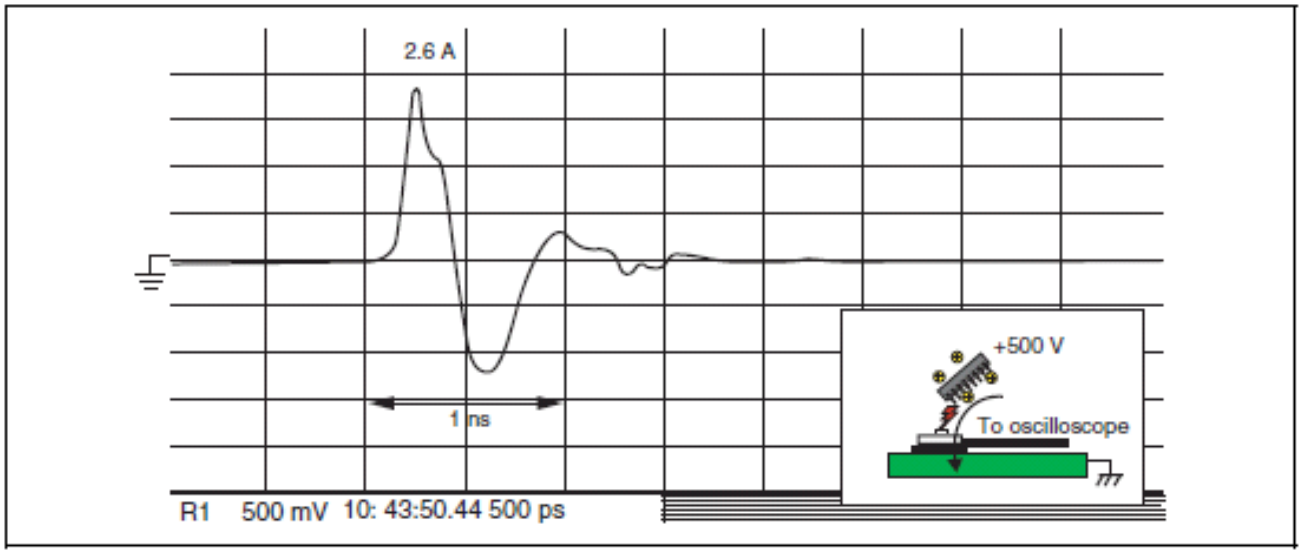


Figure 4.74 Discharge Waveform for Charged Device Model (Measured with a 3.5-GHz Oscilloscope)

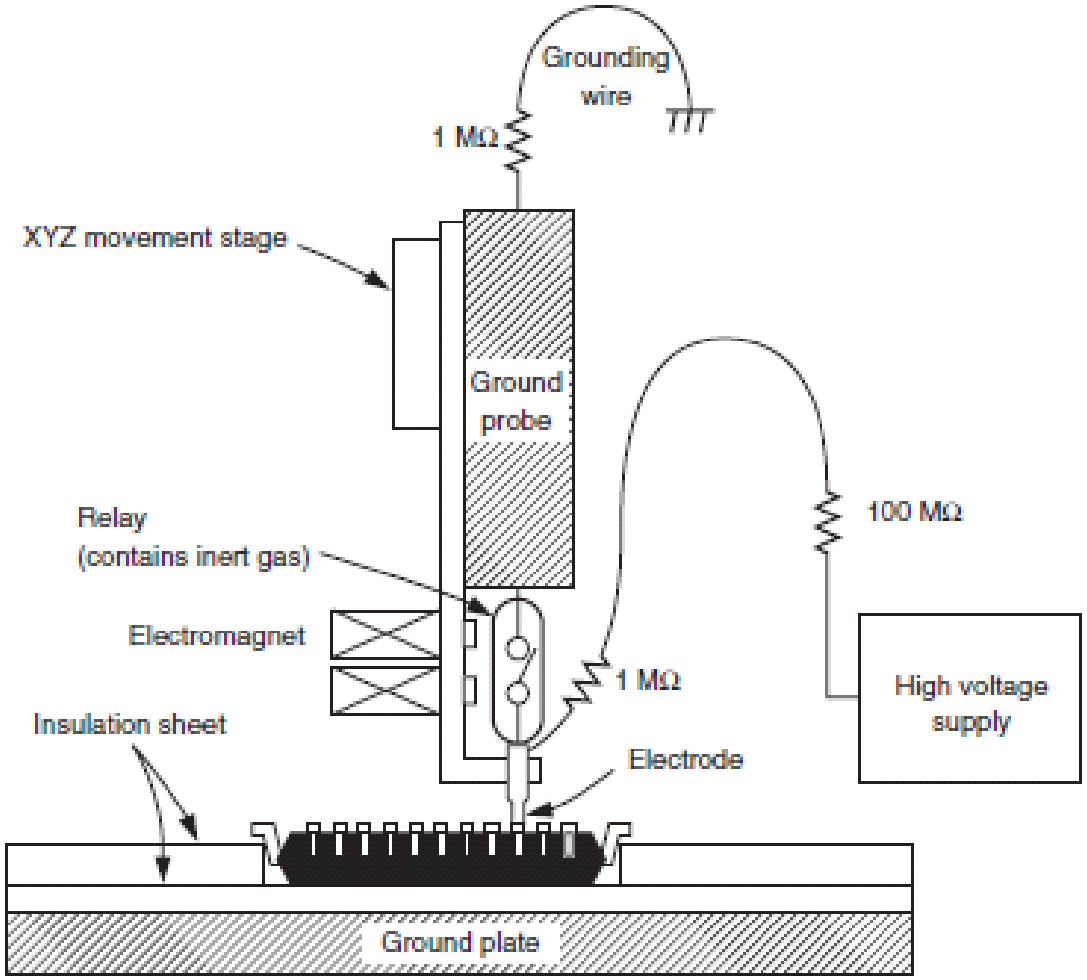


Figure 4.75 Example of CDM Test Circuit (Device is Charged from High-Voltage Source, Relay is Closed, and Device is Discharged to a Ground Bar)

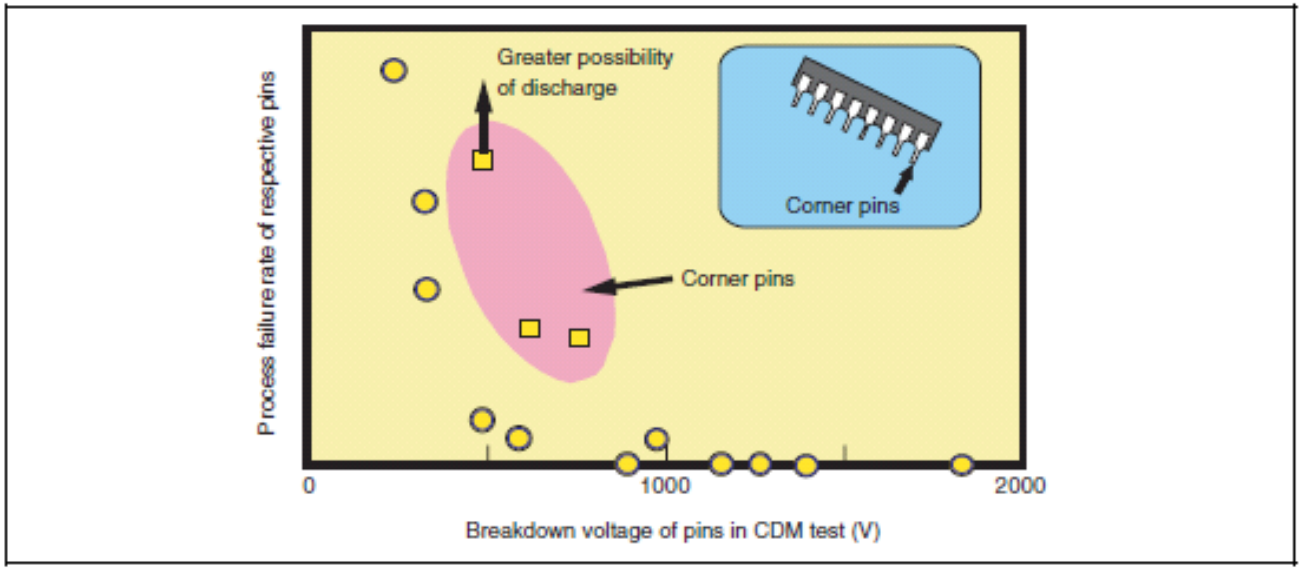


Figure 4.76 Relationship between Fraction Defective in Package Assembly Process and CDM Test Intensity

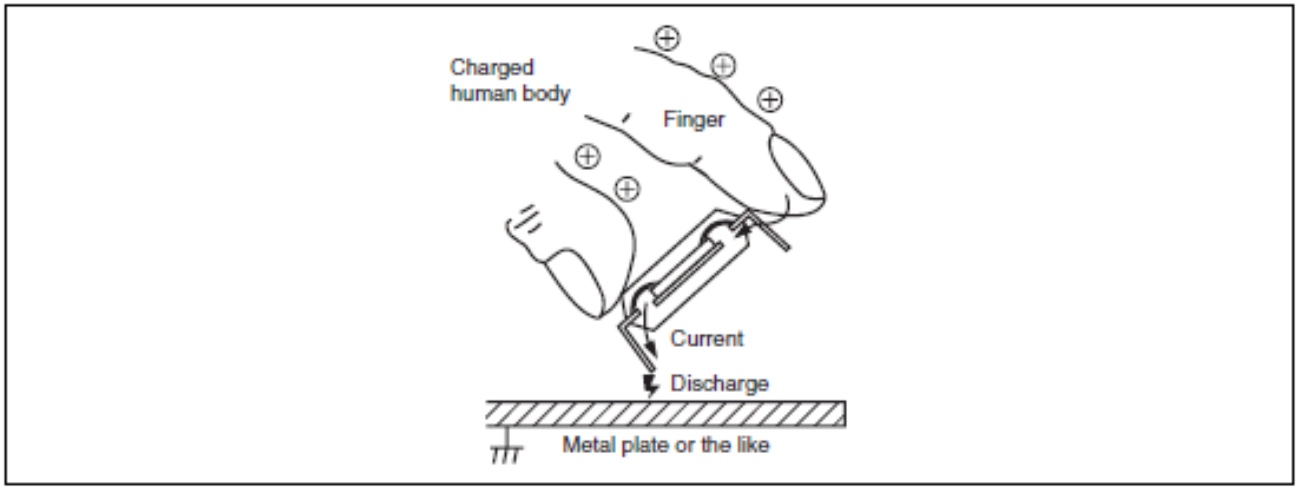


Figure 4.77 Example of Complex Discharge on HBM and CDM

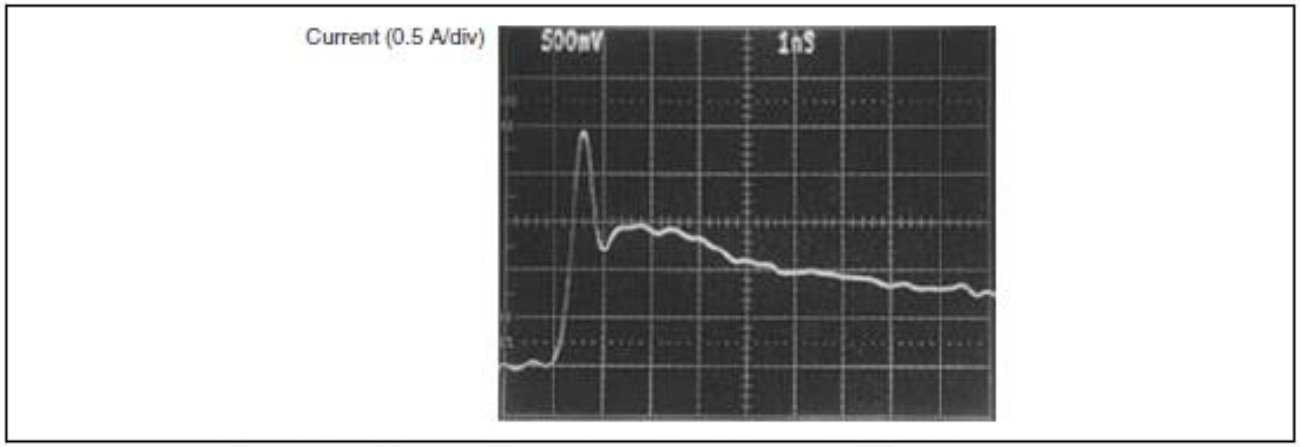


Figure 4.78 Example of Complex Discharge Current Waveform

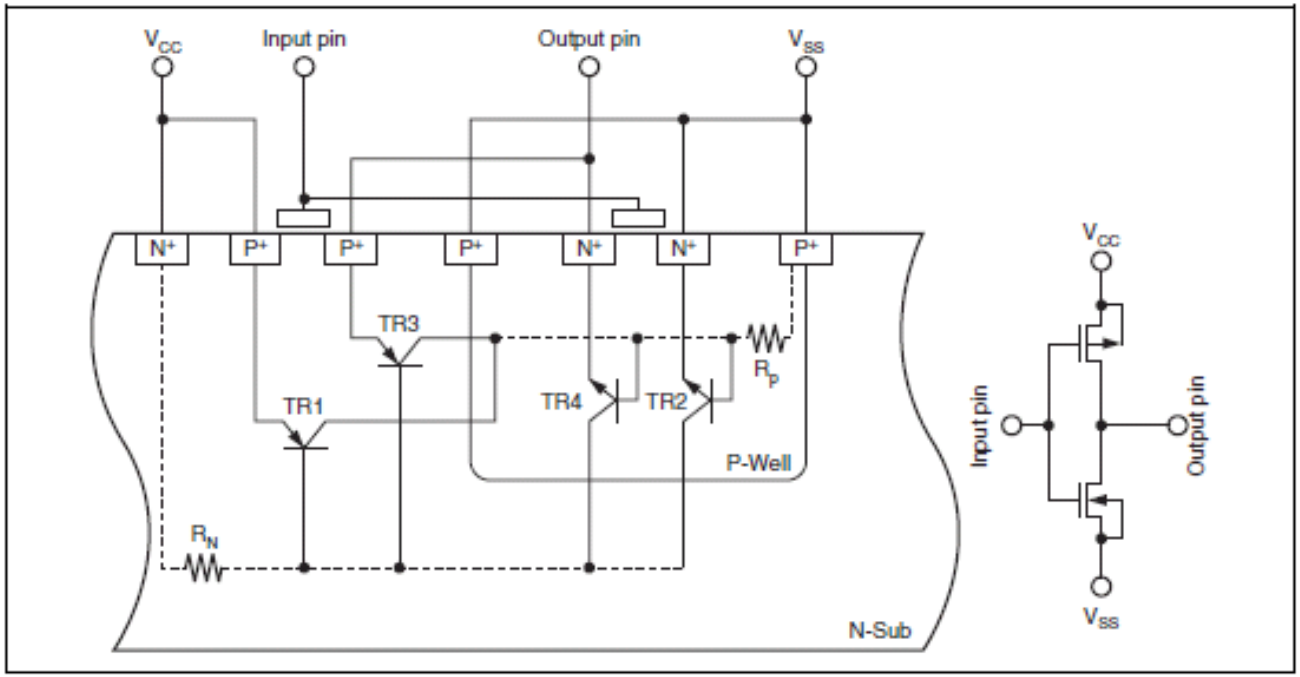


Figure 4.79 Cross Section of CMOS Inverter

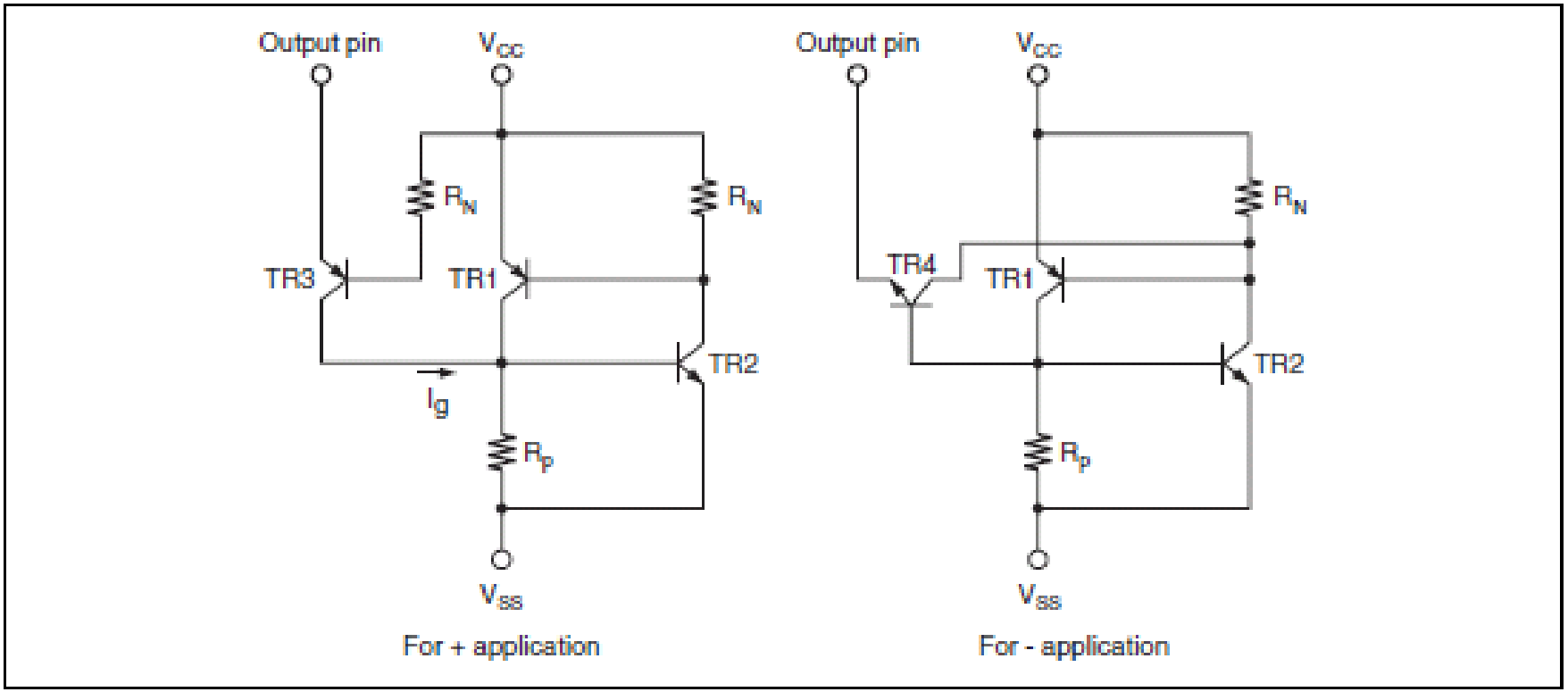


Figure 4.80 Parasitic Thyristor Equivalent Circuit

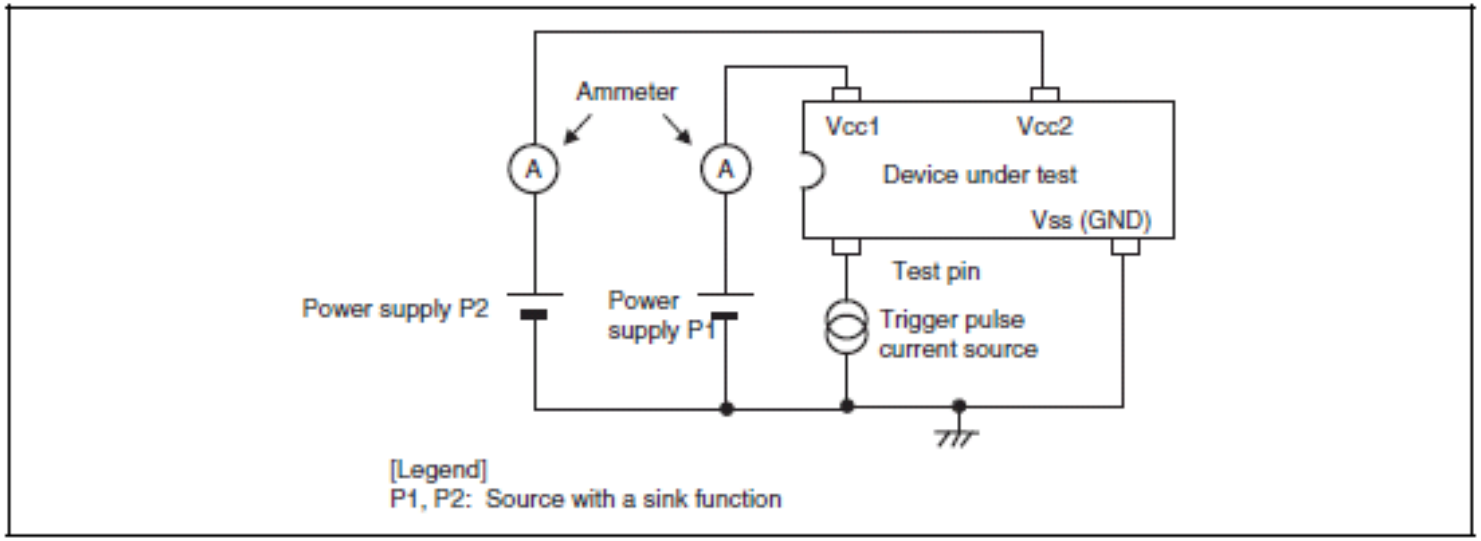


Figure 4.81 Latchup Test Circuit (Pulse Current Injection Method)

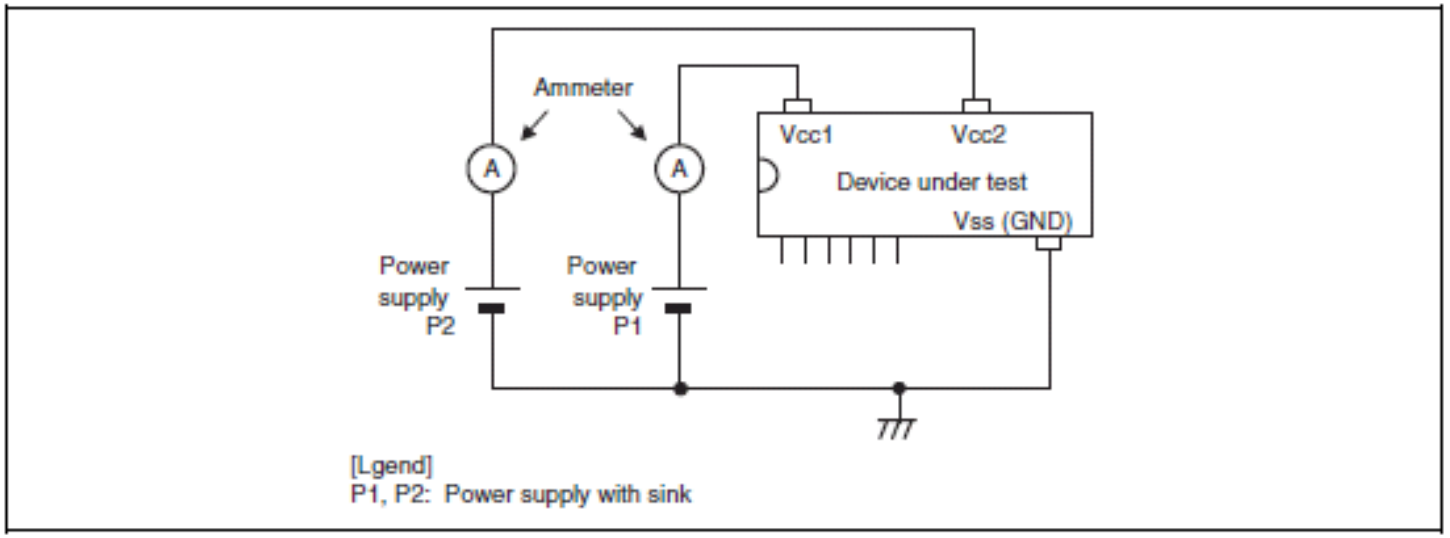


Figure 4.82 Latchup Test Circuit (Excessive Supply-Voltage Method)

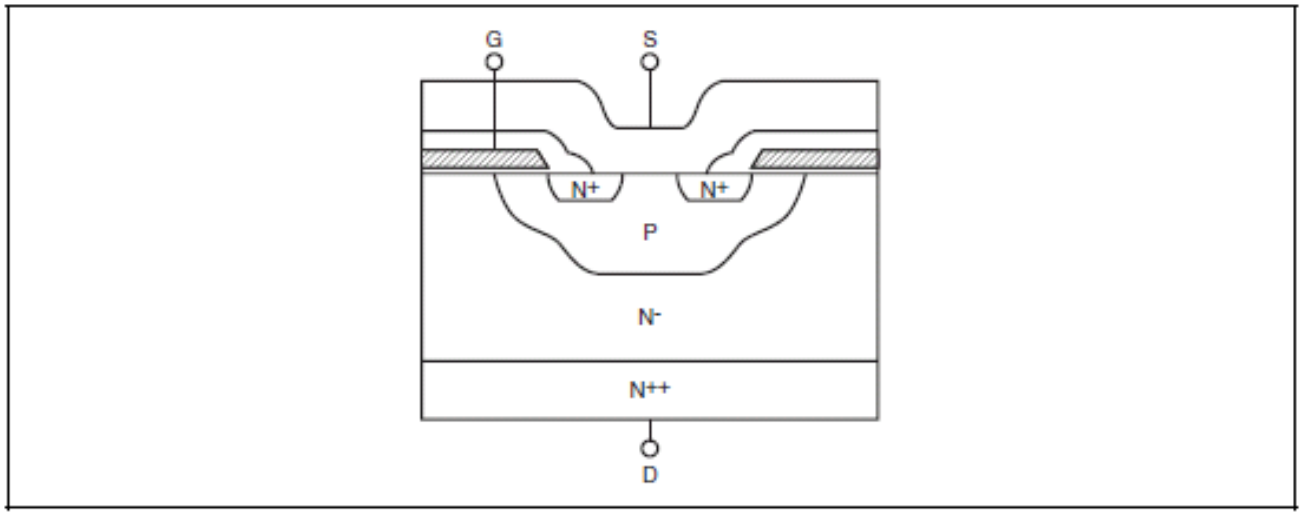


Figure 4.83 Cross Section of a Power MOS FET

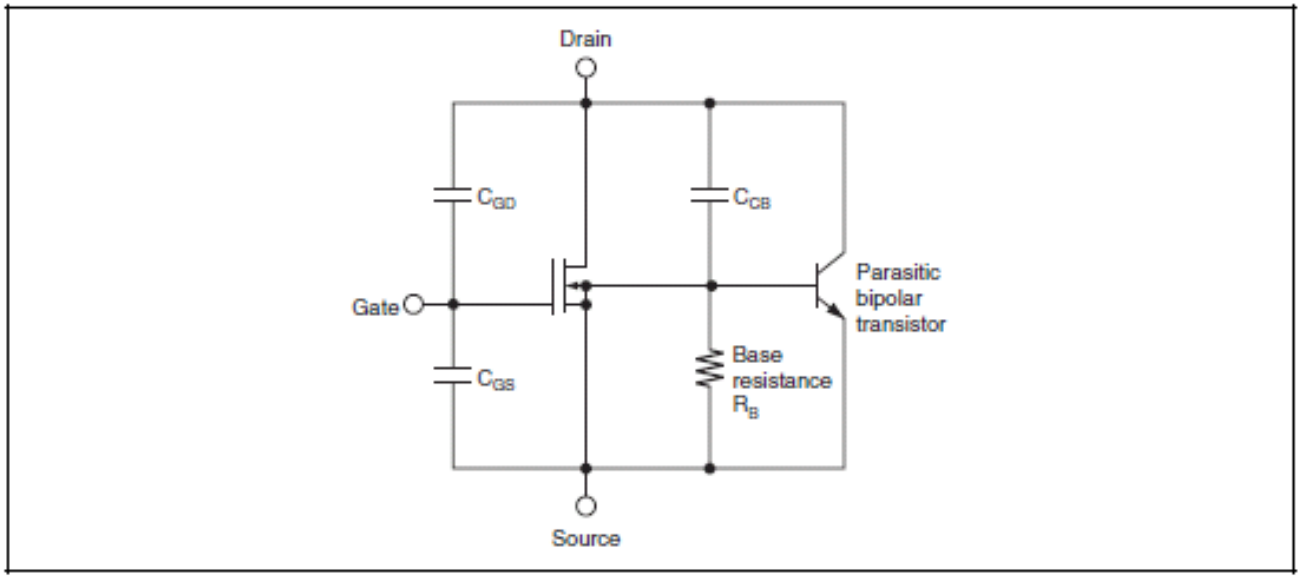


Figure 4.84 Equivalent Circuit of a Power MOS FET

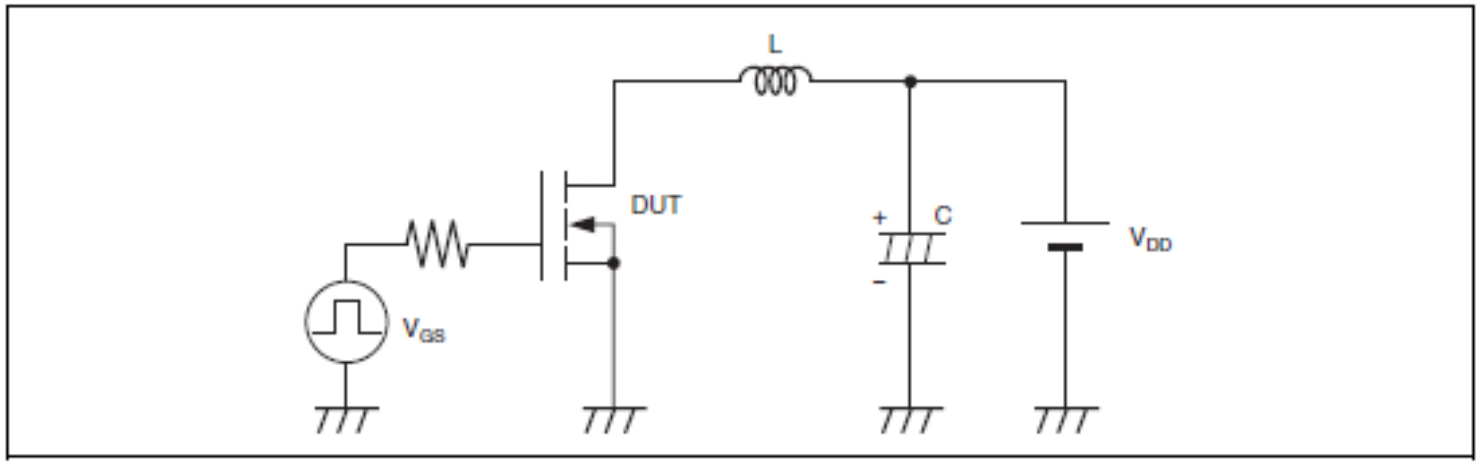


Figure 4.85 Avalanche Tolerance Evaluation Circuit Diagram

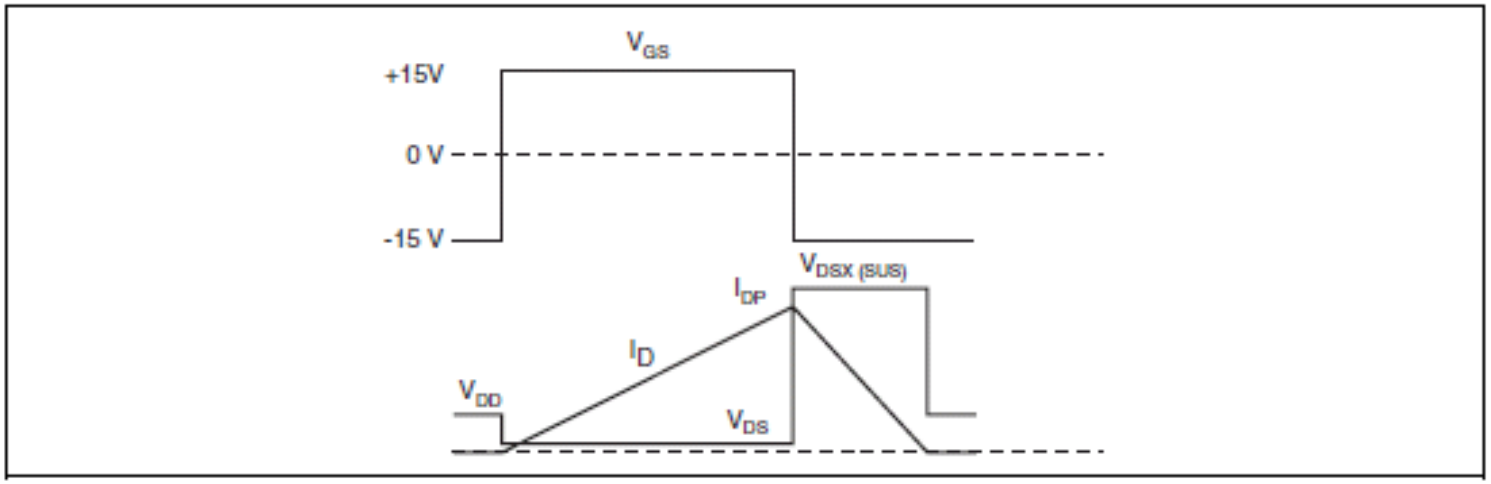


Figure 4.86 Avalanche Waveforms

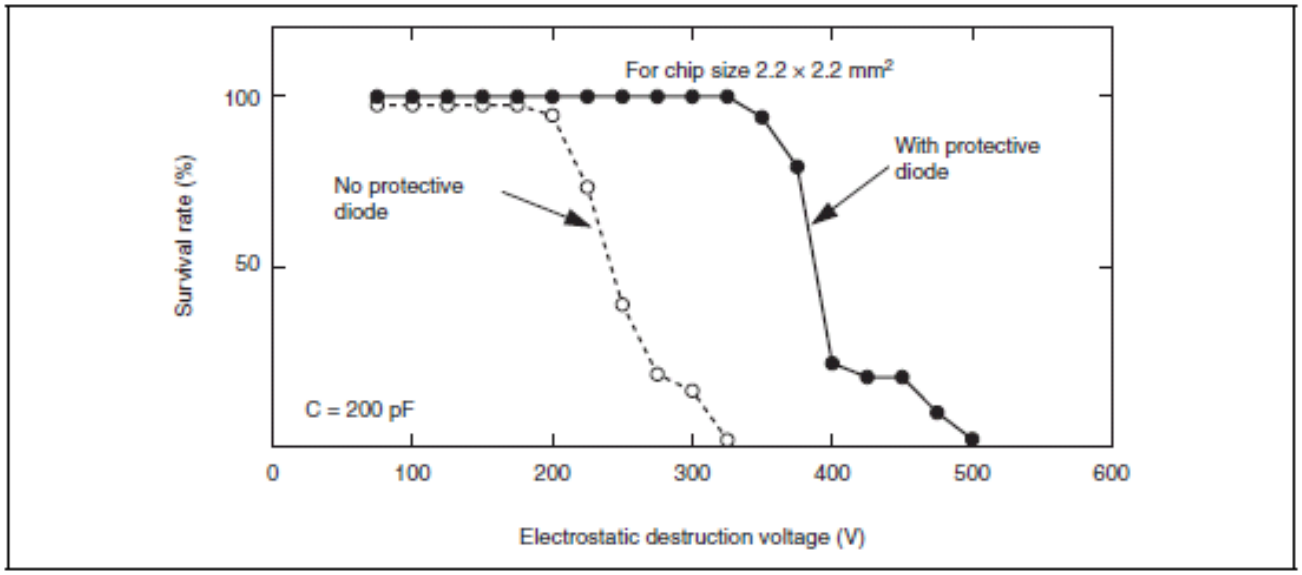


Figure 4.87 Electrostatic Discharge Strength of a Gate Oxide Film

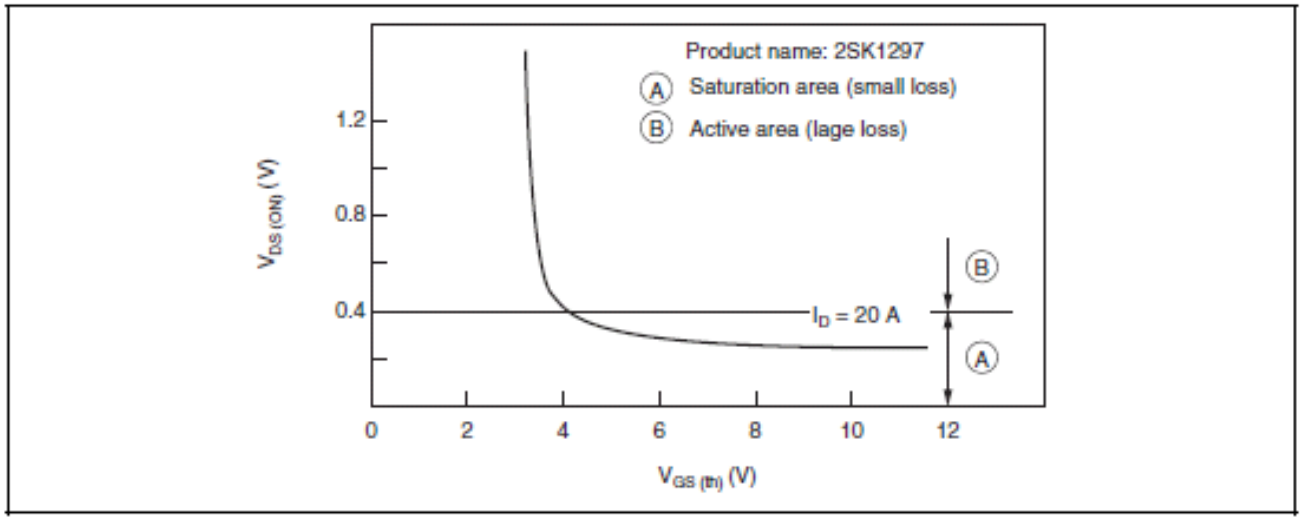


Figure 4.88 $V_{ds(ON)}$ - $V_{gs(th)}$ Characteristics in Practical Use

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