

### **MOS** Device: Basics

- MOSFET & Modeling -

Renesas Design Vietnam Co., Ltd. Phuoc Tran, Nguyen Phuoc Nguyen, RVC Training Center

Lecture 1

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### Introduction

Why we need to learn MOS Devices?

How the MOSFET model is used?

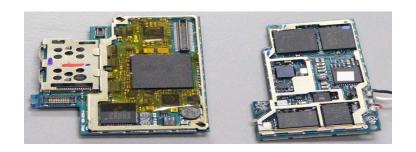
What is Key issue in MOSFET & Model?

These are basic questions for people who starts working in Semiconductor Industry.

Firstly, let's try to answer the questions before starting lecture on MOSFET & Modeling.

## Why we need to learn MOSFET & Model?

Micro Controller Memory, Game Data Communicate Windows (Software)



Mobile Phone E-mail, E-tag, Music Camera, Digital-TV



PC



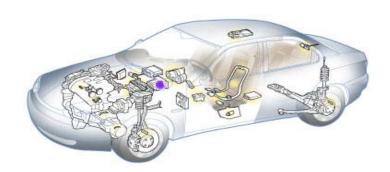
Mobile



Life

Car

Pace Maker (Health)
Robot
Sensor, Monitor
Environmental



Hybrid Car Navigation Anti-crash Control Gas Control

# LSI (Large Scale Integrated) is everywhere. Foundation of industry society!

Integrated Circuits (IC) are everywhere, now!

- Radio, TV, Mobile Phone, Camera, Computer, Car, Robot .....

Integrated Circuit is the product of "INTEGRATION" of:

- Knowledge
- Science
- Technology
- and Dream

IC: Integrated Circuit

LSI: Large Scale Integration

Both can be used equally, LSI more popular

It is composed of Transistors, that is MOSFET. Millions of MOSFETs are integrated in a small chip say 5.97mm\*5.99mm size (R2 chip from SoC Group – Tape out by RVC Backend Team)

So, to understand MOSFET; it is the basic knowledge in working at industry, not only Semiconductor but also IT, Car Industries etc.

### **Short Quiz**

- (1) How many ICs in a mobile phone?
- (2) How many ICs in a hybrid car?
- (3) How much the sales price of a typical processor?
- (4) How much the production cost in general?

### How the MOSFET model is used?

In designing Logic circuit, which is used in digital computation

In designing Analog circuit; amplifier, filter, sensor and drivers

To develop Standard Cell Library, which is used in designing LSI

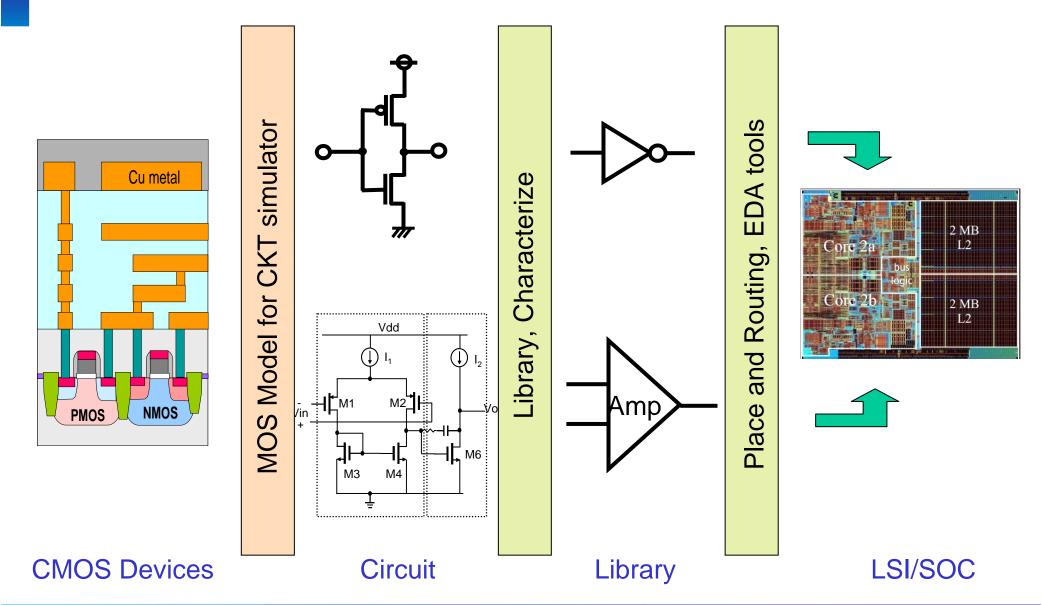
To compromise LSI (Large Scale Integration) performance & cost

And more....!

The performance of circuits have strong relation with fabrication process

MOS model is "Interpreter" between Process and Design! All the process information can be described through MOS model and its parameters.

# MOS model, Circuit, library, LSI or SOC (System on a chip)



## What is Key issue in MOSFET & Model?

To understand basic MOSFET I-V characteristics (Electrical operation)

To know updated small size effects down to 65nm\* process.

To depict MOSFET model parameters as their relationship to MOS process information.

To become used to utilize circuit simulators (SPICE), in your daily LSI design works when you want to know CKT level behavior of high level Instruction-set operations.

• Your hair-diameter is 0.1mm (=100,000nm), therefore 65nm corresponds to 1/2000 of your hair-diameter.

### **Education level of this course**

University Under Graduate School Level of Physics

University Under Graduate School of Math. & Statistics

Recommend to have studied at EE (Electronics Engineering) Department course such as;

Electronics

Circuit Theory

Semiconductor Physics

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### Lecture organization

Chapter 1: Basics

- Semiconductor Physics (basics)

- PN Diode

- MOS Diode

- MOSFET

- CMOS (Complimentary MOS)

- Scale Down of MOSFET

- Quiz and Test

In this Lecture, we learn Chapter 1,

Especially MOSFET electrical operation

Chapter 2: BSIM

- Compact MOS Model

- ....

Chapter 3: Charge Model

- .....

Chapter 4: Variability

- .....

Chapter 5: Analog CMOS

- .....

AND More!

### **Useful References (Textbooks)**

### Semiconductor Physics and Device:

Grove: Physics and technology of semiconductor devices, John Wiley & Sons, Inc., 1967.

Sze; Physics of semiconductor devices (2<sup>nd</sup> Edition), John-Wiley & Sons, Inc., 1981.

### Compact MOS Model:

Arora: MOSFET model for VLSI circuit design, Springer-Verlag, 1993.

Tsividis: Operation and modeling of the MOS transistor, McGraw-Hill, 1987.

BSIM4.5.0 MOSFET Model User's Manual: (U.C. Berkeley, CA, 2004).

#### **MOS Circuits:**

Uyemura: Circuit Design for CMOS VLSI, Kluwer Academic Publications, 1992.

Razavi: Design of analog CMOS integrated circuits, McGraw-Hill, 2001.

### **Chapter 1: Basics**

In this Chapter, again we learn:

- (1) Materials used in LSI; brief summary
- (2) What is semiconductor? Intrinsic and extrinsic semiconductor
- (3) Carrier (electron and hole) transport dynamics
- (4) Most simple devices: DiodesPN diode and its roleMOS diode and its electrical properties
- (5) MOSFET basic I-V characteristics
- (6) CMOS (Complimentary MOS)
- (7) Scaled-down and related Small Size effects
- (8) Futures on MOS Devices

### (1) Materials used in LSI

#### Various Material Structures:

a) Amorphous Not well defined structure

b) Poly Crystal Many small crystal

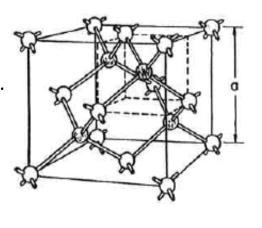
c) Crystal Long range 3D order of atoms

### Example:

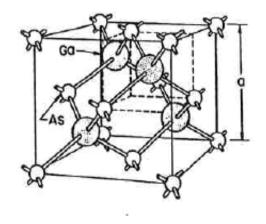
a): SiO2, SiN, Amorphous Si, ....

b): Poly Si, Metal (Al, Cu), TaO, ....

c) : <u>Si, Ge, GaAs</u>. ....



DIAMOND (C, Ge, Si, etc)



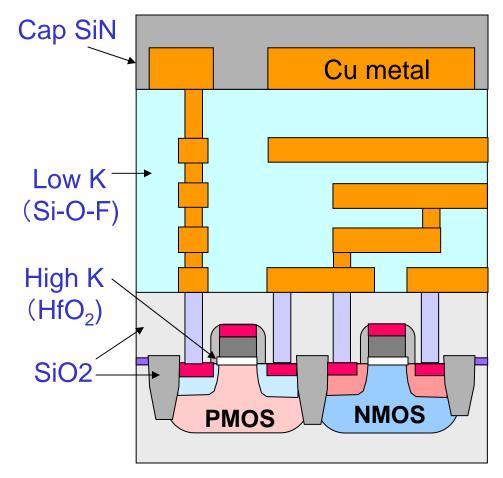
ZINCBLENDE (GaAs, GaP, etc)

Crystal lattice structure & Bonding to neighbors; this structure determines basic electrical nature of semiconductor crystal.

## LSI Structure: Type of materials **Passivation** Dielectric Wire Etch Stop Layer **Poly Crystal** Dielectric Capping Layer (Cu, W) Copper Conductor with Barrier/Nucleation Layer **Amorphous** (SiO2, SiN) Crystal Pre-Metal Dielectric Tungsten Contact Plug (Silicon) **MOSFETs**

Metal 1 Pitch

### Amorphous: many types of insulator films



45nm CMOS structure uses many Amorphous insulators

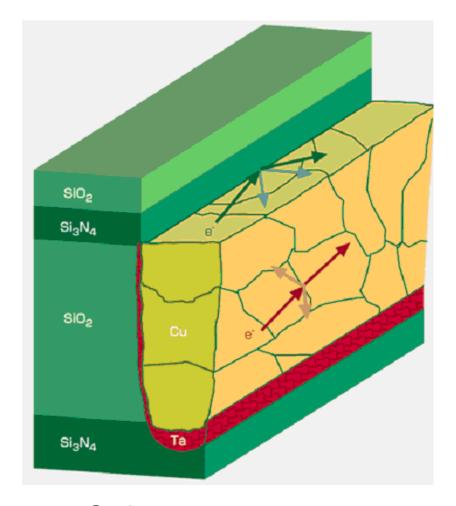
Amorphous is not-well-defined structure.



Its Role is "Electrical Isolation":

- Transistor Isolation
- Transistor gate insulator
- Interconnect Isolation
- Isolation (protection) the outer contamination

### Poly crystal: Cupper Metal



Cu interconnect structure

Poly-crystal material is a group of small crystals.

The electrical properties are determined by:

- Crystal size
- Crystal Boundary
- Boundary with other material

### In General:

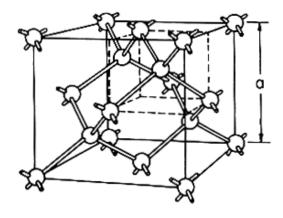
Mechanically tough (strong)
 compared with crystal body

Quiz: Why we need Ta film?

## **Silicon Crystal**



Silicon Crystal



DIAMOND (C, Ge, Si, etc)

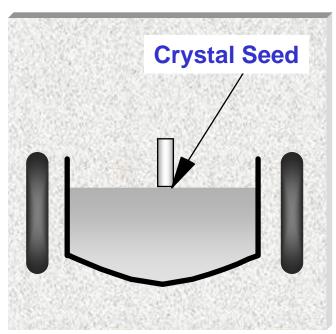
## **Key Properties**

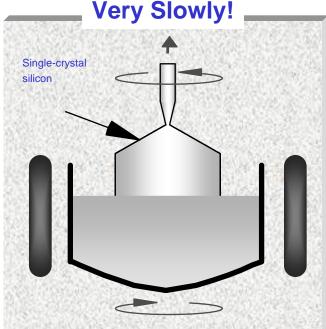
- (1) Silicon is everywhere!
  - Stones
  - Sand at sea shore
  - . . . .

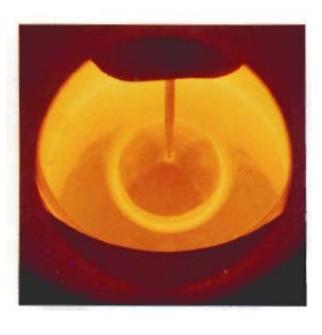
Unlimited resources on earth.

- (2) Very high melting temp. (1400°C) Therefore, very stable material.
- (3) Oxidized Silicon (SiO2) shows extremely good insulator & stable
- (4) Very good thermal conductor
- → Silicon is an ideal semiconductor material for LSI

## How to Fabricate Silicon Crystal Rod? (Review from Lecture "Wafer Process")







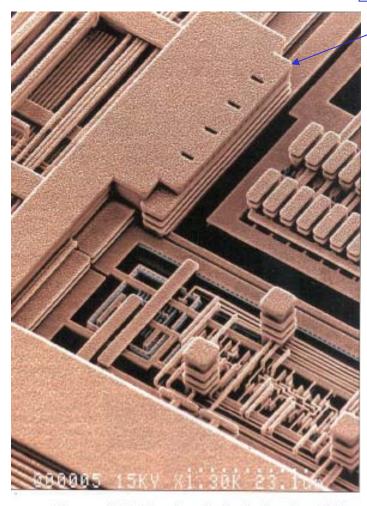
Crystal "seed" is touched at melted silicon liquid. Temperature of liquid silicon is high as 1400°C.

Ok! Then lets move up the "seed" very very slowly. Silicon crystal grows on the seed to 30cm Rod! Picture of real Silicon Rod Growth.

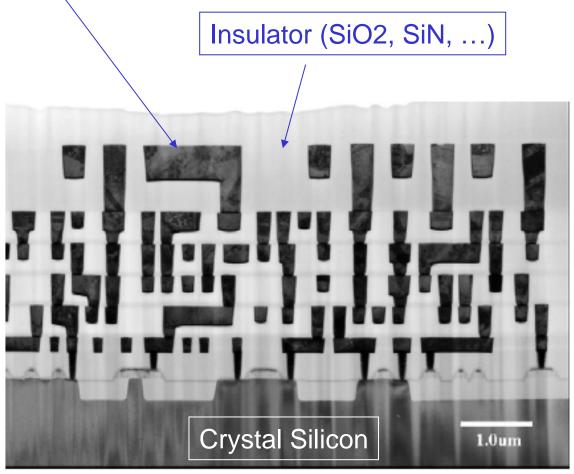
### **Actual views of microelectronics**

Interconnects

Metal (Cu, Ta, W, ...)







Renesas microprocessor



## Type of Conductor (Electrical property)

a) Good Conductor (Metal: Cu, Al)

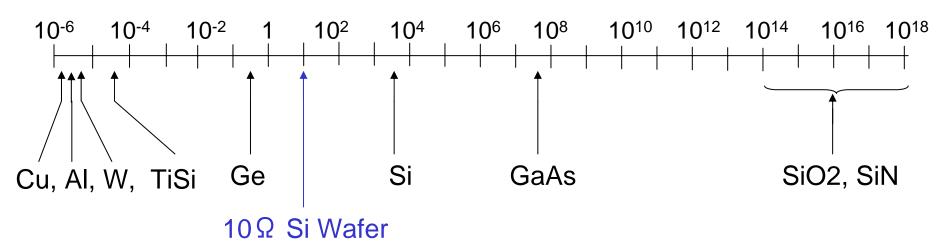
Electron (e-) free from atomic bound;  $\rho \approx 10^{-5} \Omega \cdot cm$ 

- b) Semiconductor (Si, Ge, GaAs)
  - e- loosely bounded;

$$\rho \approx 10^1 \sim 10^5 \Omega \cdot cm$$

- c) Insulator(SiO2, SiN)
  - e- tightly bounded;

$$\rho \approx 10^{16} \Omega \cdot cm$$



# To understand electrical properties of Material, we need to know Band Theory!

However, what we need to know is not so much; a couple of key images are required.

- 1. Electrical current is due to "Electron" movement in material.
- 2. To get more current, (1) many free Electrons and their (2) faster movement (mobility) are necessary requirement.
  - →High speed switching of circuits, High frequency operation.

Very very Simple!

### Continued...

3. Then, how many free Electrons in the Silicon?

**Energy Band Theory determine it!** 

Behind the Theory, "Quantum Electronics".

It says Electron can stay only pre-assigned Energy Levels in silicon. ...

4. How fast the Electrons moves in Silicon?

**Electron Scattering determine it!** 

Many Scattering mechanisms.....

Phonon scattering (electrons & lattice-atoms)

Surface scattering (electrons & surface-roughness)

etc.

## (2) What is semiconductor?

### Two Type of Semiconductor structures

Intrinsic semiconductor (P-Type and N-Type)

- Intrinsic Semiconductor (Pure Silicon)

Determine basic Band structure and temperature dependence

- Extrinsic Semiconductor (with Impurity atoms)

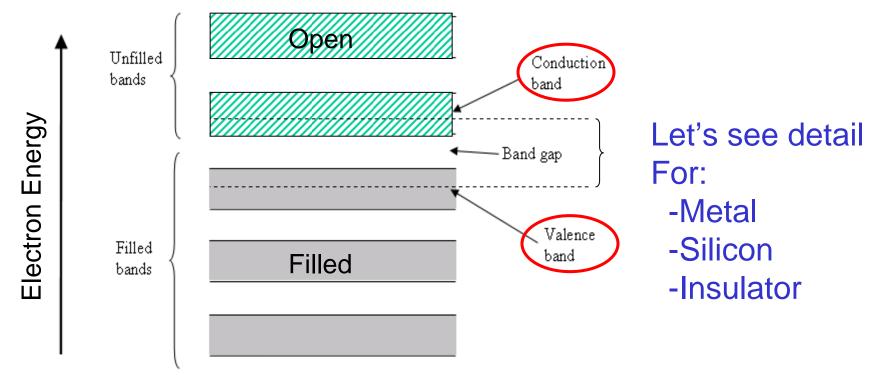
Determine practically "How many Free Electrons" Therefore, Impurity is very important pieces, just like spices in Vietnam delicious foods!

Q: Let me know what is your favorite spice for "Pho"?

# Conduction Band and Valence Band determine "How many Free Electrons in Si"

Firstly, Band Theory determine energy-levels, in which electrons can stay! In semiconductors. **Valence band** is the range of electron energy, in which the electrons are filled & strongly tied with Si atom.

Electrons stay in <u>Conduction band</u> move freely under the influence of an applied electric field.

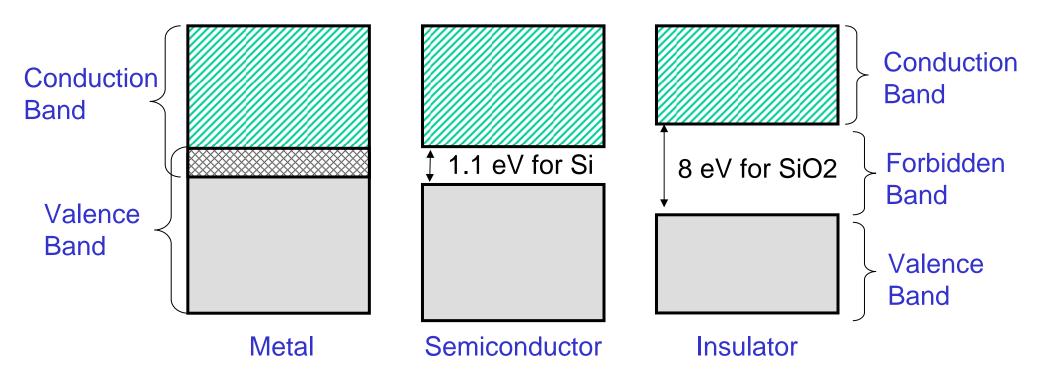


### Band Structure (Metal, S/C, Insulator)

Semiconductor (S/C) is something between Metal and Insulator.

One case the good electrical conductor, the other like insulator (no current conduction), which means it forms electrical "switch".

It can be done by introducing small amount of impurities in Si crystal!

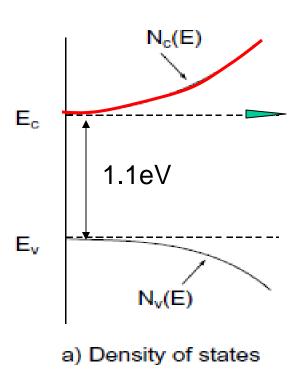


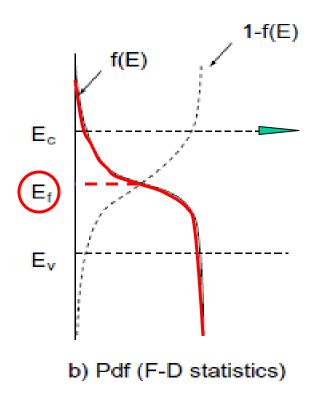
## (2-1) Intrinsic Semiconductor (No impurity dopant) : Energy band structure

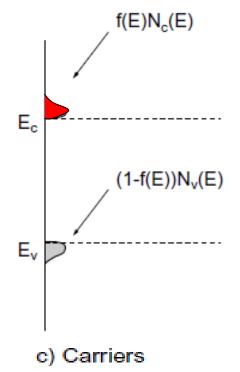
Rooms in which Electron can stay: ~ Nc(E)

Probability of Existence for electron as a function of electron-energy

Electron density (numbers of electrons)







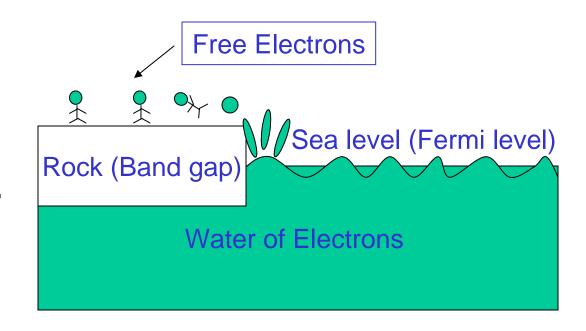
# Band theory tells us "how many free electrons existing in Silicon (Intrinsic)

One unclear parameter is Fermi Energy Level (Ef). What is this physical meaning?

Fermi Energy level is just like Sea-surface-level of "electron sea".

Happy electron who successfully jumps up the Rock, they become a Free-Electrons.

They work hard to carry current in Silicon!



What happen at high Temperature (rough sea surf waves)

### Temperature effect on: Intrinsic carrier density ni(T)

ni: Intrinsic carrier density (Temp. dependent)
For Silicon

@300K (27°C)  $ni=1.5X10^{10} cm^{-3}$ 

@400K  $ni=2.0X10^{13}$  cm<sup>-3</sup>

@500K  $ni=1.0X10^{15} cm^{-3}$ 

$$n_i = \sqrt{N_C N_V} e^{-E_g/2kT}$$

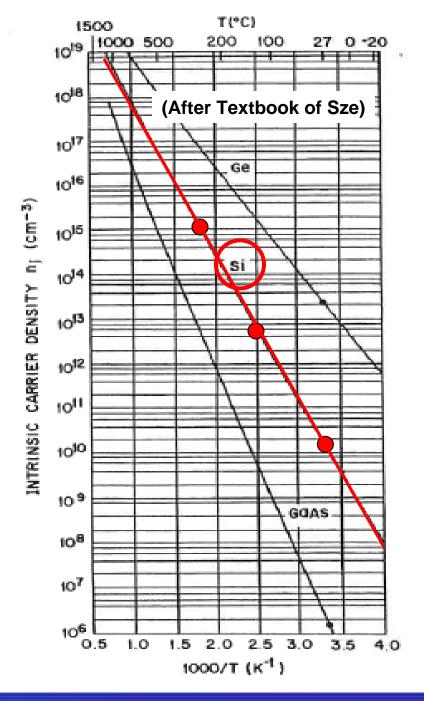
$$= 4.9 \times 10^{15} \left(\frac{m_{de} m_{dh}}{m_0^2}\right)^{3/4} T^{3/2} e^{-E_g/2kT}$$

$$np = n_i^2 = N_C N_V \exp(-E_g/kT)$$

- MOSFET: ni is used to calculate  $Vth(\phi_F(ni))$ 

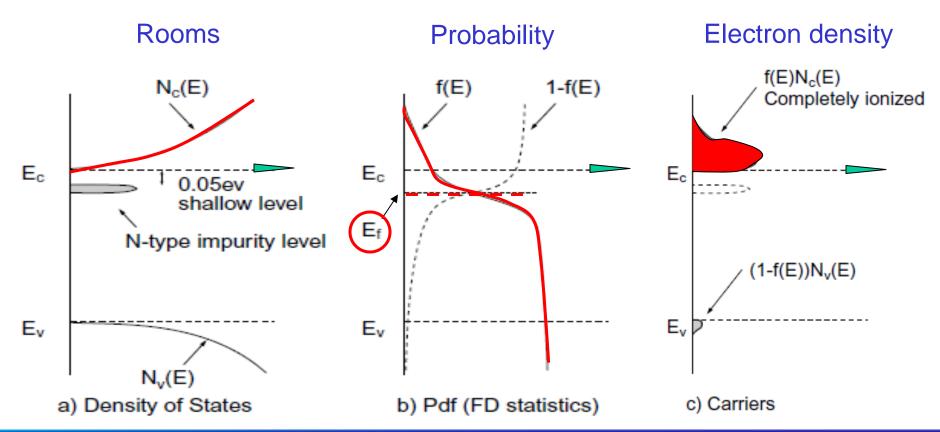
- PN diode: ni is used to calculate Vbi or  $\phi_{Bi}$ 

In equilibrium: np=ni<sup>2</sup>



# (2-2) Extrinsic Semiconductor (With impurity dopant): Energy band structure (N-Type)

Dopant: N-Type: P, As, Sb; P-Type: B Impurity dope is a "magical spice" to change S/C into devices

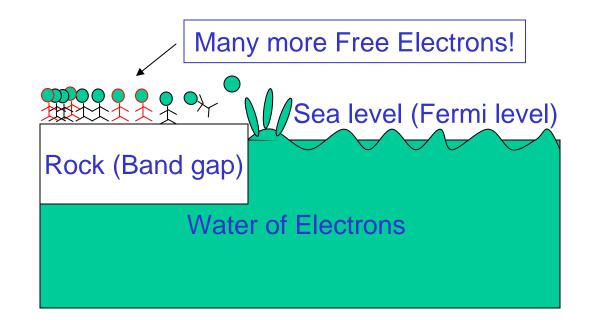


## Band theory tells us "N-Type Extrinsic Silicon generate a lot of Free Electrons"

In Extrinsic (N-Type Impurity is added) semiconductor, the Fermi Level moves-up near Conduction Band!

Since the sea-surface-level moves-up close to the Rock's upper surface, a lot of electrons are thrown upon.

Happy free electrons carry much more current!



What happen in "P-Type Extrinsic Silicon?

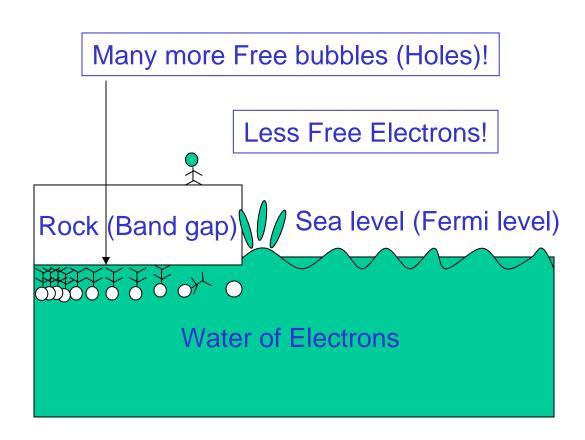
# Note on: What happen in P-Type Silicon ? → generate a lot of Holes!

In P-Type Silicon:

The Fermi-level stays close to balance band.

Rough surf-wave does generate air-bubbles under the Rock.

The bubble (Holes) can move under the Rock freely and carry current.



## Equations: Fermi level (Intrinsic & Extrinsic)

Now we understand what is Fermi Level, and how important it is! The Fermi level can be calculated by physical equation as follows:

- Fermi level:
- (0) Definition: E at which  $f(E) = \frac{1}{\exp[(E E_f)/kT] + 1} = \frac{1}{2}$
- (1) Intrinsic Fermi level:  $E_f = \frac{1}{2} (E_V + E_C) + \frac{3}{4} kT \ln \left( \frac{m_h}{m_e} \right)$
- (2) Extrinsic Fermi level:
- - N-Type  $E_f = E_C kT \ln \left( \frac{N_C}{N_D} \right)$
- - P-Type  $E_f = E_V + kT \ln \left( \frac{N_V}{N_A} \right)$

In extrinsic case the Fermi level is determined from impurity concentration of  $N_{\rm D}$  and  $N_{\rm A}$ .

## **Equations:**

Band structure: Density of state (Open rooms)

## Density of State:

- Conduction band; 
$$N_C(E) = \frac{4\pi}{h^3} (2m_e)^{3/2} \sqrt{E - E_C}$$

- Valence band; 
$$N_V(E) = \frac{4\pi}{h^3} (2m_h)^{3/2} \sqrt{E_V - E}$$

Note: 
$$N_C=2.8X10^{19} \text{ cm}^{-3}$$
,  $N_V=1.0X10^{19} \text{ cm}^{-3}$  @27°C

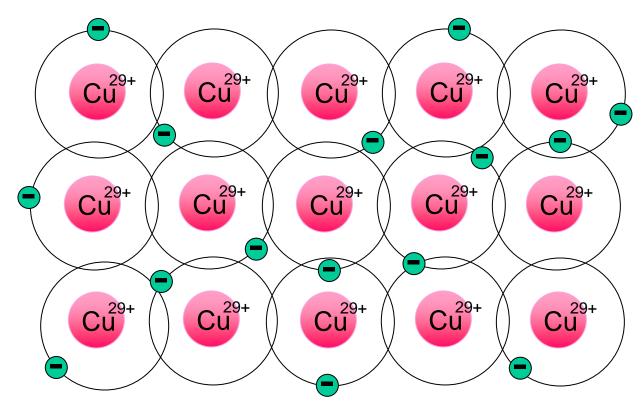
Fermi-Dirack statistics: 
$$f(E) = \frac{1}{\exp[(E - E_f)/kT] + 1}$$

E<sub>f</sub>: Again the Fermi energy level, strong function on N<sub>D</sub>, N<sub>A</sub>

### **Show Time!**

Metal Electron moves freely

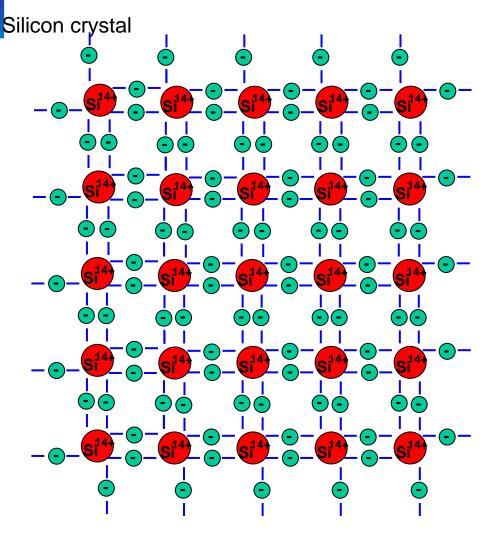
Semiconductor Crystal Energy Band Electron Movement Different from Silicon, Cupper (Cu) Metal atoms allow the electrons move freely within the solid Cu.



As the result, Cu becomes good conductor.

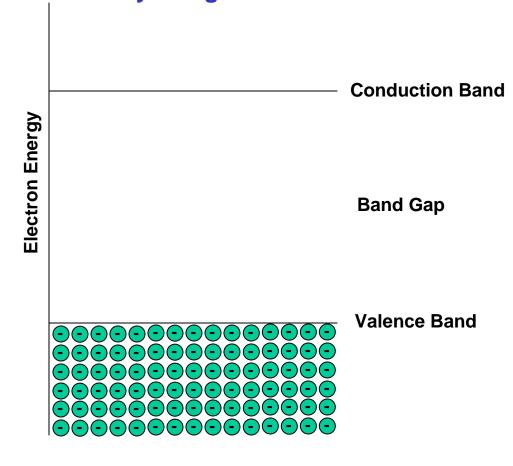
Why there are many free electrons in Cupper material?

### **Doped Silicon**

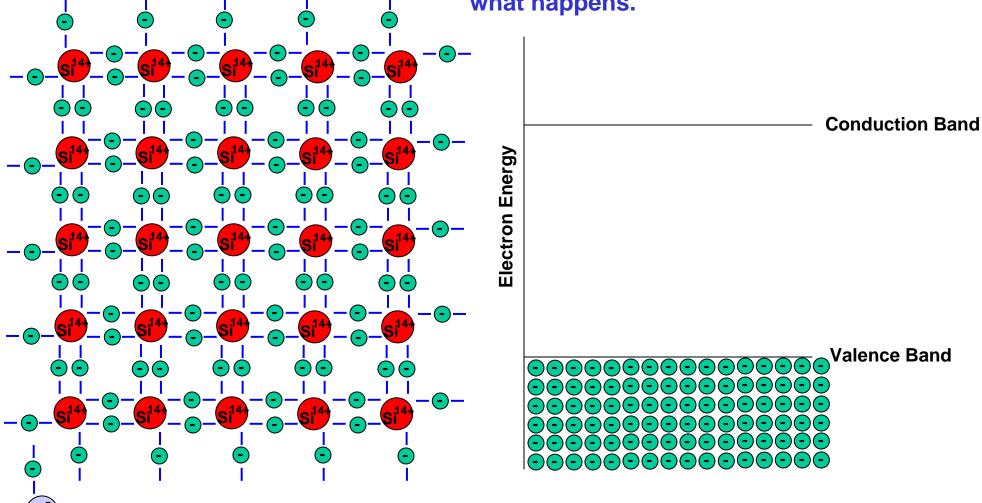


**Intrinsic Semiconductor** 

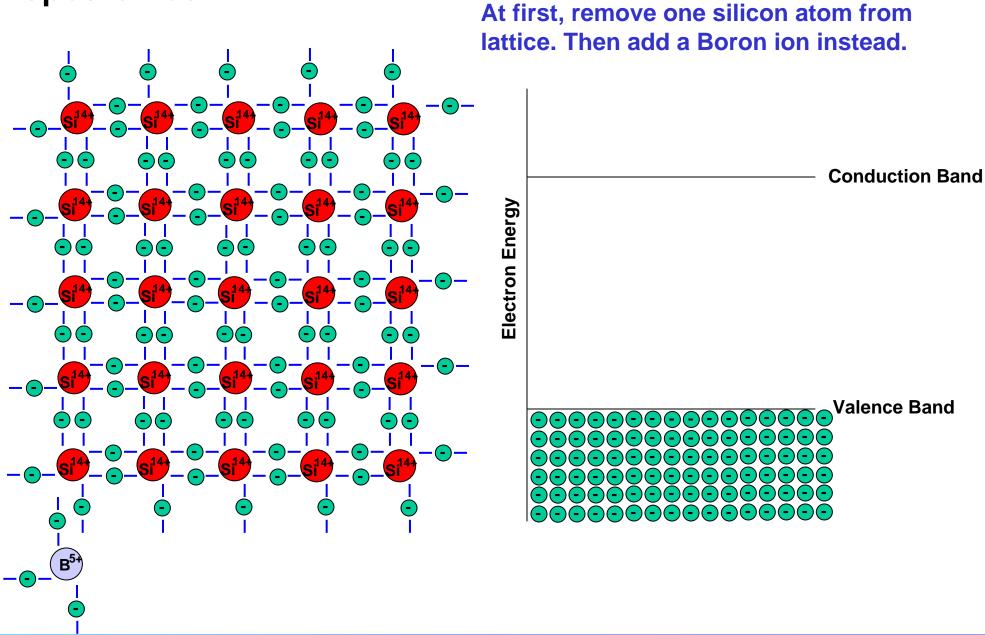
Since silicon has 4 hands (valence electrons) as covalent bond to neighbors, very few electrons moves freely. Therefore, the resistivity is high.

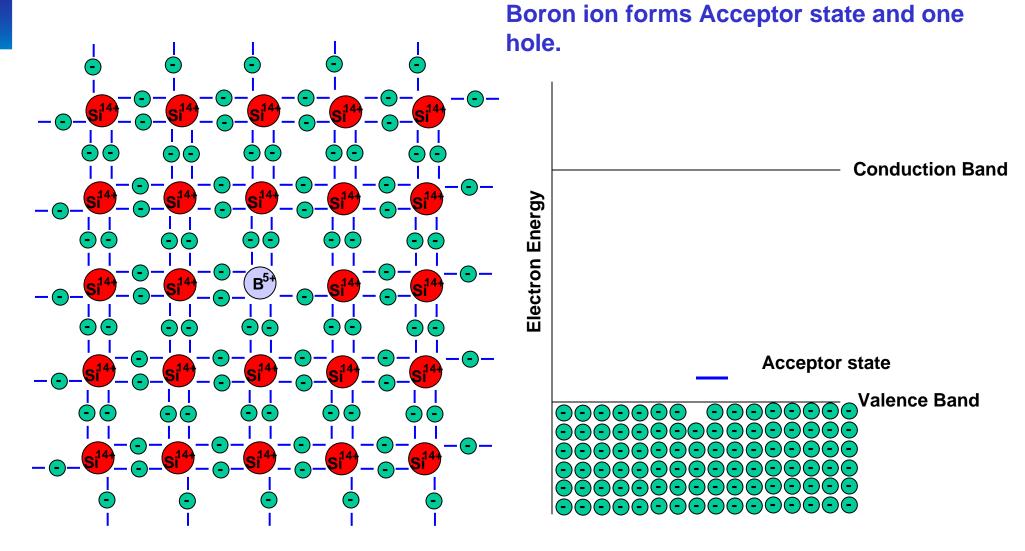


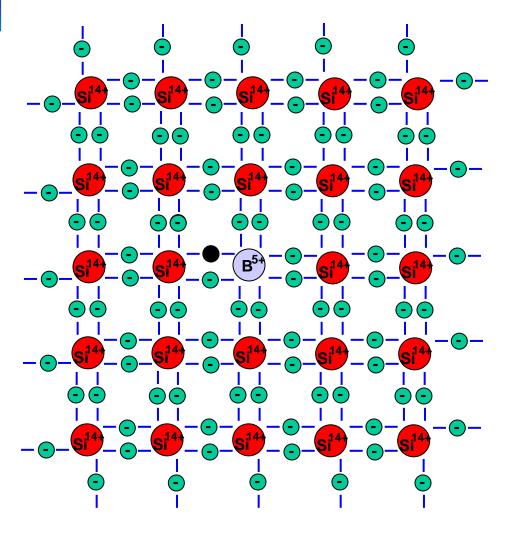
Let's add Boron ion of III Group (he has 3 hands) into intrinsic silicon lattice, and see what happens.



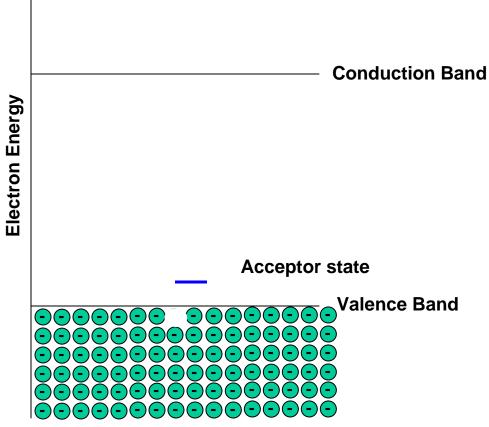
III group element becomes "Acceptor" for silicon (P-type Impurity)



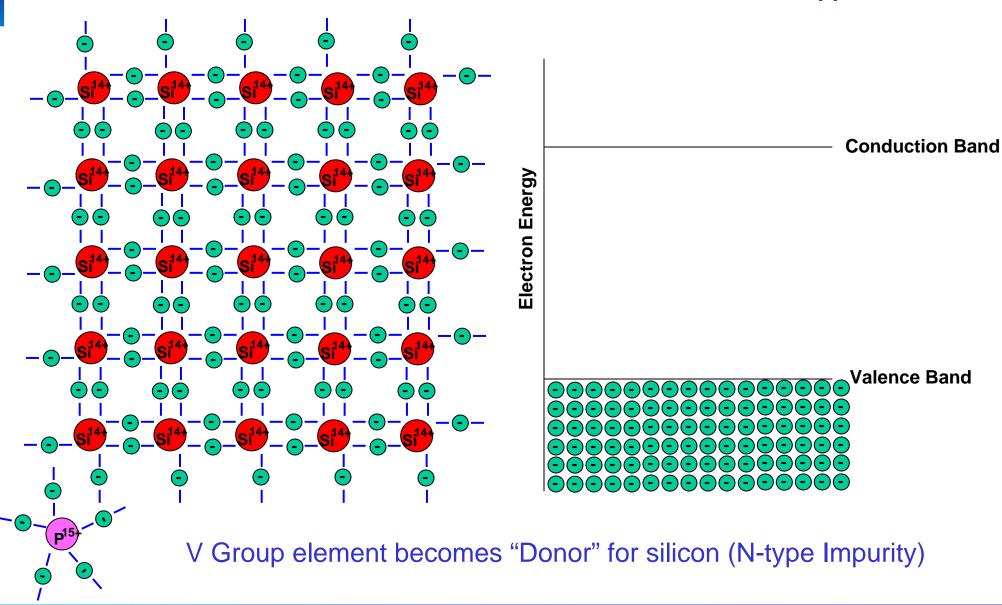


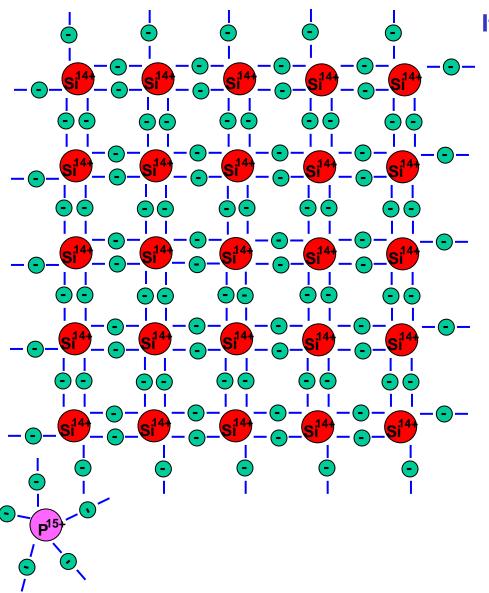


Generated hole is loosely tied with Boron ion. It can move around inside the Silicon crystal.



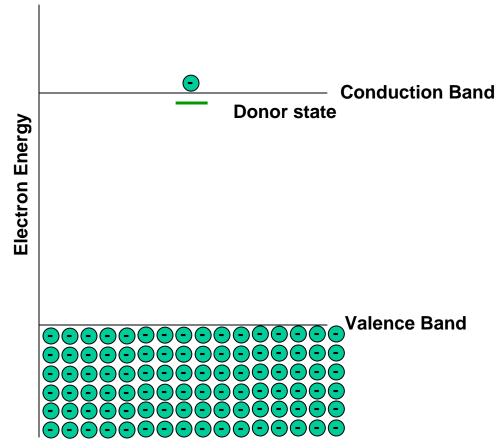
OK, let's add Phosphorous ion next time. He has 5 hands. See what happens!



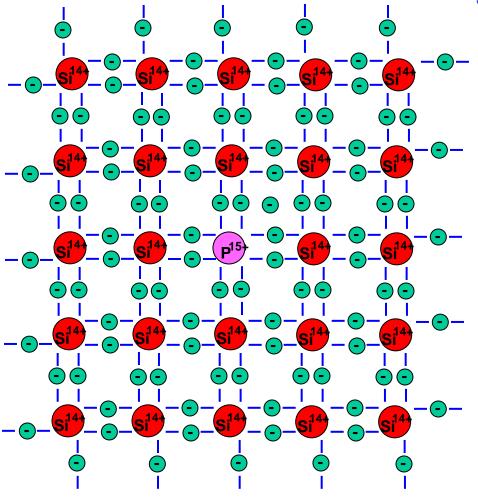


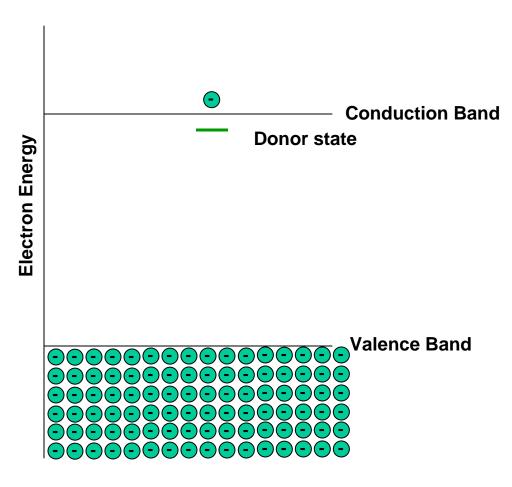
Remove one silicon atom from lattice and replace with a Phosphorous ion.

It generate Donner state and a free electron



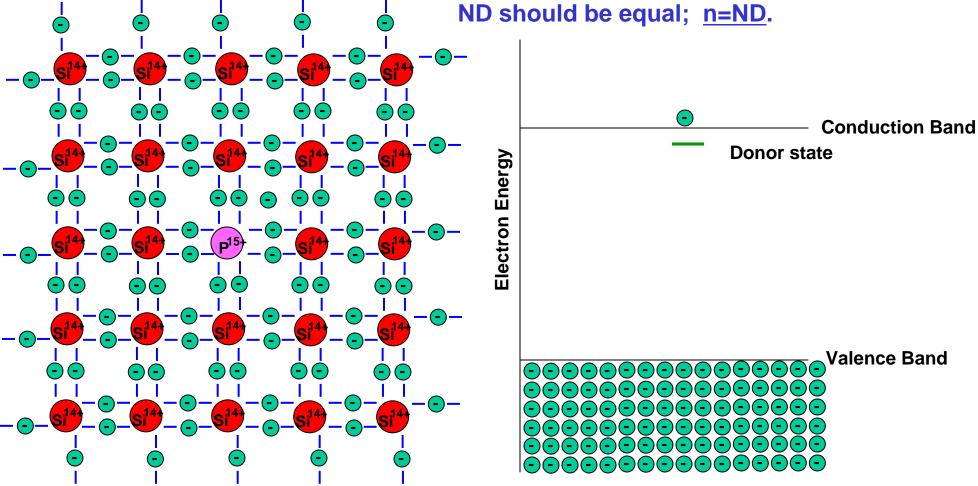
The electron also moves freely inside the Silicon crystal.





From 1 donor, 1 free electron is generated.

Thus, electron density n and donor density ND should be equal: n=ND.



#### **Summary on Free Electrons in Silicon**

### Intrinsic semiconductor

ni=1.5X10<sup>10</sup> cm<sup>-3</sup> @300K (27°C) Large Temperature dependent

### Extrinsic semiconductor

Fully ionized (in case of shallow level dopants)

1) n-Type:

$$n=N_D$$
,  $p=ni^2/N_D$   
Ef=Ec - kt In(2.8x10<sup>19</sup>cm<sup>-3</sup>/N<sub>D</sub>)

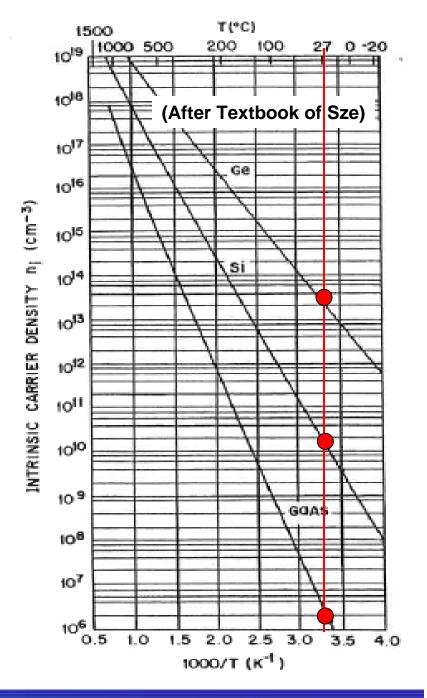
2) p-Type:

$$p=N_A$$
,  $n=ni^2/N_A$   
 $Ef=Ev + kt ln(1.0x10^{19}cm^{-3}/N_\Delta)$ 

#### Quiz

(1) Why the number of free electrons (ni) of intrinsic GaAs, Si and Ge shows quite different values? (See right Figure)

(2) In Figure in page 18, you can see resistivity value of intrinsic semiconductor (GaAs, Si and Ge) @ room temperature. How this observation relates to (1)?



### Copy of p.18: Type of Conductor (Electrical property)

a) Good Conductor (Metal: Cu, Al)

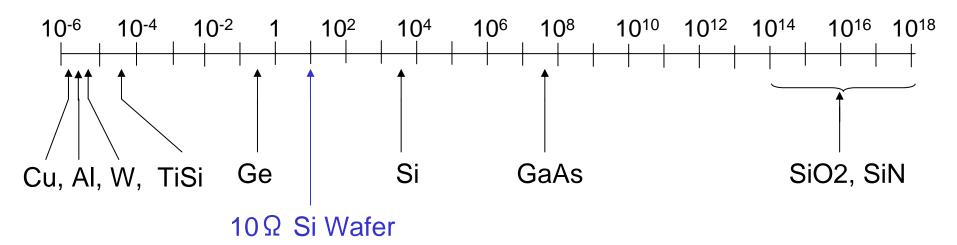
Electron (e-) free from atomic bound;  $\rho \approx 10^{-5} \Omega \cdot cm$ 

- b) Semiconductor (Si, Ge, GaAs)
  - e- loosely bounded;

$$\rho \approx 10^1 \sim 10^5 \Omega \cdot cm$$

- c) Insulator(SiO2, SiN)
  - e- tightly bounded;

$$\rho \approx 10^{16} \Omega \cdot cm$$



#### Quiz (Continued)

(3) Intrinsic Si has slightly higher  $E_f$  (Fermi energy level) over  $E_i$  (=(Ec+Ev)/2). How high is it? Assume  $m_h/m_e$ =2.

(4) Extrinsic Si with  $N_A$  (p-type impurity) =  $10^{15}$  cm<sup>-3</sup>; tell the electron and hole concentrations (n and p) of the material @ room temp.

(5) Location of  $E_f$  of (4)?

#### (3) Carrier transport mechanism: "How fast the free electron moves?"

Carrier (e-, h+) movement: Two mechanisms!

- 1) Drift (Moving force = Electric field "E")
- 2) Diffusion (Moving force = Carrier density gradient " $\partial n/\partial x$ ")

Current equations

- Current Equation: 
$$I_{n} = qA \left( \overbrace{\mu_{n} \, nE} + \overbrace{D_{n} \, \frac{\partial n}{\partial x}} \right) \qquad I_{p} = qA \left( \mu_{p} \, pE + D_{p} \, \frac{\partial p}{\partial x} \right)$$

- Einstein's Relation: 
$$D_n \approx \frac{kT}{q} \mu_n = 0.025 \mu_n$$
  $D_p \approx \frac{kT}{q} \mu_p = 0.025 \mu_p$ 

$$I_{p} = q A \left( \mu_{p} p E + D_{p} \frac{\partial p}{\partial x} \right)$$

$$D_p \approx \frac{kT}{q} \mu_p = 0.025 \mu_p$$

MOS on-current: Drift current

Diffusion current MOS sub-Vth current:

BJT current: Diffusion current

### How fast e- and h+ move ? : Mobility ( $\mu_n$ , $\mu_p$ )

#### Note:

Carrier mobility  $(\mu_n, \mu_p)$  is complicated "EFFECTIVE" physical parameter. Many empirical effect (Scattering mechanisms) are solely implemented into this parameter "mobility".

Brief comment on carrier transport:

- Two types of carrier transport mechanisms, in general:

e- in vacuum, Constant electric field E: Const. Acceleration

e- in S/C, Constant electric field E: Const. velocity

In S/C (semiconductor), various carrier scatterings cause above observation... Constant carrier mobility in electric field (moving force).

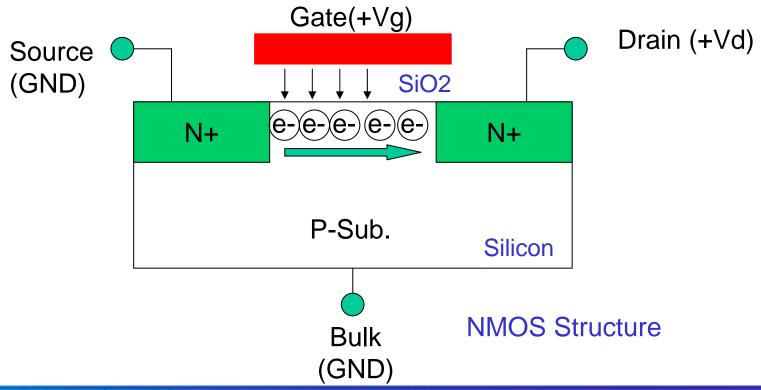
#### Carrier scattering mechanism

- Thermal movement (vibration) of atoms scatter the moving carrier (Phonon scattering)
- MOS structure; surface (@ SiO2-Si interface) potential roughness disturb (Surface scattering) the carrier movement
- Impurities; which cause disturbance of periodic potential structure in Si crystal (Impurity scattering)
- Defects; crystal imperfection cause also the disturbance of periodic potential structure (Defect scattering)
- Other carrier's charge scatters the moving carrier, e-/e-, e-/h+ scattering (Carrier/carrier scattering)
- In MOSFET, Surface scattering and carrier velocity saturation (Phonon scattering) are the two major scattering mechanisms.
  - → Degrade the MOSFET current (Ids) in Shrunk MOSFETs!

RENESAS

#### **About MOSFET (short break)**

- Electrons (e-) are induced at Si/SiO2 interface by gate electric field (+Vg)..... Surface scattering effect →significant
- The e- move from Source to Drain by drain bias (+Vd)......
   Velocity saturation effect (Phonon scattering) → dominate

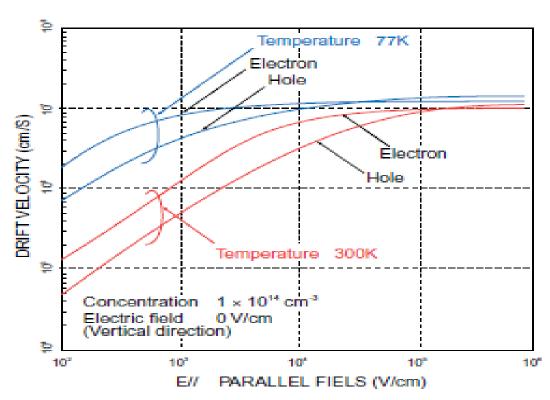


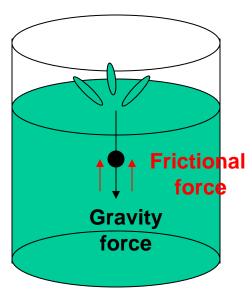
# Mobility: Depends on drift field (Phonon Scattering)

When you drop a small stone in water tank, the stone moves down in the water due to Gravity Force with "Constant Speed".

This happens because negative-force by friction with water works.

The same phenomena happens on Electron movement in crystal.





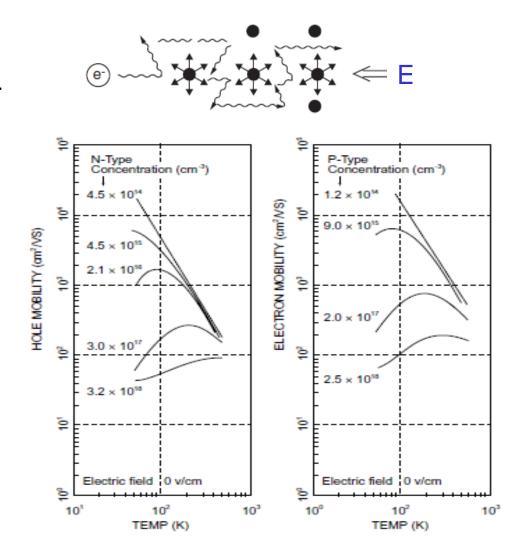
Stone sinking in Water

# Mobility: Depends on temperature (phonon scattering)

At High temperature, crystal atoms vibrate heavily and interrupt more the movement of Electrons. So, higher temperature results in lower carrier mobility (→less current=slow switching).

#### Note;

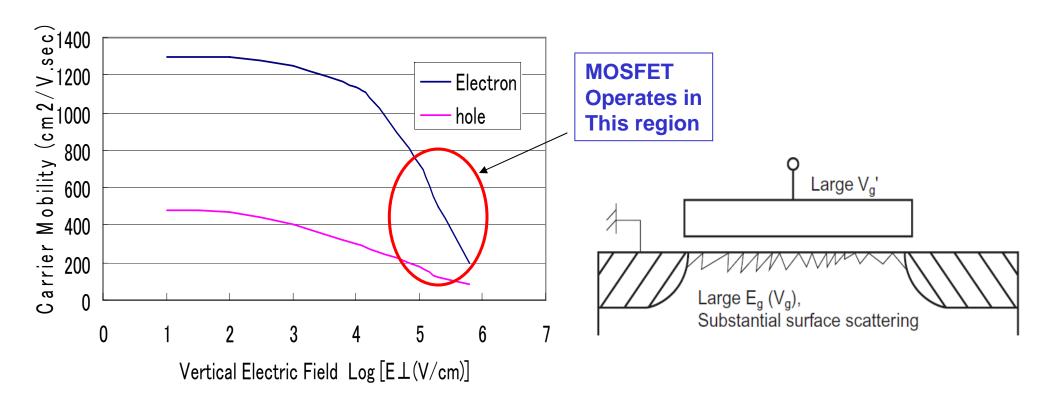
LSI can be used in Russia (-20°C) and/or Vietnam (40°C). We need to guarantee our LSIs work perfectly at any location in the world!



## Mobility: Depends on surface field (Surface Scattering)

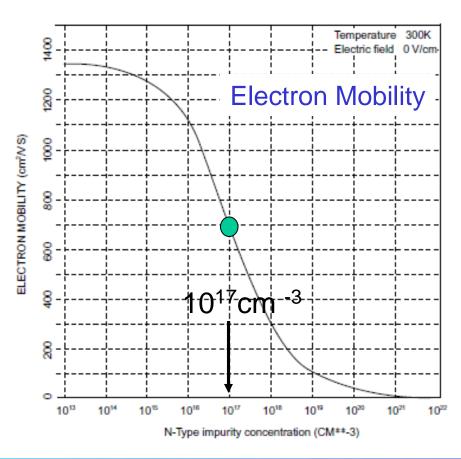
In MOSFET, induced electrons are pushed up to the Si surface, therefore Surface roughness disturbs its movement from source to drain. Electron mobility is degraded to ½ of bulk one's.

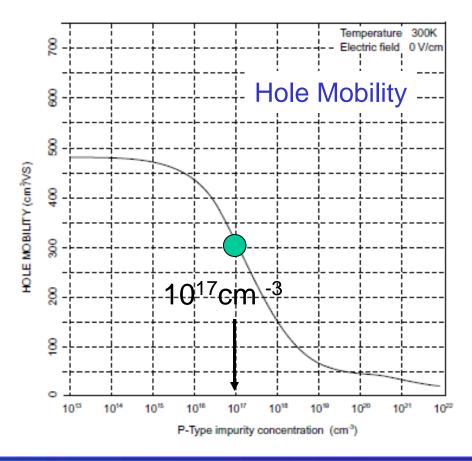
MOSFET operate at the  $E_{\perp}=10^5 \sim 10^6 \text{ V/cm}$ 



# Mobility: Depends on impurity concentration (Impurity Scattering)

@90nm MOSFETs, channel impurity concentration is some 10<sup>17</sup> cm <sup>-3</sup>.





#### **Summary of carrier transport**

Carrier transport equation

General Eq.: 
$$I_n = q A \left( \mu_n n E + D_n \frac{\partial n}{\partial x} \right)$$

MOSFET Eq.: 
$$I_n \approx q A \mu_n n E$$

Carrier mobility (µ) determine MOSFET current (switching speed):

- (1) μn, μp are characterized from various scattering mechanisms
- (2) In MOSFET, phonon & surface scatterings are major ones
  - ... the µ degraded due to carrier velocity saturation (vs) & surface scattering
- (3) In shrunk MOS, vs(n)=vs(p)= 10<sup>7</sup>cm/sec, @ critical field; Ecrit.=2X10<sup>4</sup>V/cm!

Note: In 90nm process, the electric field E=1.2V/90nm=1.3X10<sup>5</sup> V/cm>>Ecrit. These scatterings degrade mobility by a factor of ~4 compared to bulk.

#### Quiz

- (1) Current flow direction of e- and h+ along applied electric field E?
- (2) What kind of carrier transport mechanisms (type of movement), in case of MOSFET? What is the moving force of them?
- (3) In conductive material the carrier moves at constant velocity under a given E (electrical field). Why it comes?
- (4) In case (3), what happen when electric field E (in the material) is changed say to double?
- (5) When electric field E is increased to very large value, what kind of phenomena may happen?

(6) Tell three scattering mechanism which degrade carrier transport velocity. Which mechanism may affect on (5)?