



Nham Xuan Tung

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OBJECTIVE

Gain knowledge and develop skillset day by day, become a good engineer to bring a lot value to company and customer.. Learn new technologies is what I am passionate about. Besides, I hope I will become an active member of the group.

EDUCATION

Sept 2007 - Aug 2011 **Ho Chi Minh City University of Science**
Major: Maths and Computer Science
GPA: 7.2/10

WORK EXPERIENCE

Mar 2017 - Present **Renesas Design Vietnam**
Junior Engineer
Front-End 2 Department
Group: IP Design 3
I had join and experienced in some project of SystemC Modeling:

E2X-FCC2/ECM (Error Control Module):

- Make checklist
- Functional debug

New Unit Test Environment:

- Run regression test for all models
- Make INR (Verification Report).

U2A-ECM:

- Functional debug (had detected 24 bugs for this model)

Besides that, I had experienced with evaluation of some famous EDA tools which work with SystemC & RTL and improve productivity.

Stratus (many version from v17.20-beta to v18.20-p100)
(This tool is used to generate RTL from Synthesizable SystemC code)

- Evaluate and report based on intrinsic environment.

SSGen (The Synthesizable SystemC Code Generator)
(An in-house tool that allows to generate module template code, hierarchical module template code, test bench template code, and tool

scripts simply by defining hardware interface, internal information, etc)

- Make checklist and verify for enhancement

SLEC (Check equivalence of SystemC and RTL)

- Evaluate and report.

VCS FGP:

- Make User Guide

ZOIX & XFS:

- Compare the result of fault simulation between RTL & gate-level for sample data.
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