



# LSI Wafer Process

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Hai Pham reviewed and modified

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**Version 4.5**

# Contents of " LSI Wafer Process "

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- 1. What is Semiconductor?**
  - *Physics and Electrical Characteristics*
- 2. LSI Device on a Real Silicon Wafer**
  - *Structure of MOS Transistor and Interconnect*
- 3. Basic Steps of LSI Wafer Process**
  - *Module Processes*
- 4. LSI Wafer Process**
  - *An Example: 90nm SoC*
- 5. Process Defect and Yield**
- 6. Reliability**

# **What is Semiconductor?**

- Physical and Electrical Characteristics**

# What is Semiconductor?

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***A semiconductor is a material that behaves between a conductor and an insulator.***

***At room temperature, semiconductor has higher electric conductivity than an insulator, but lower than a conductor.***

***At very low temperatures, pure or intrinsic semiconductors behave like insulators.***

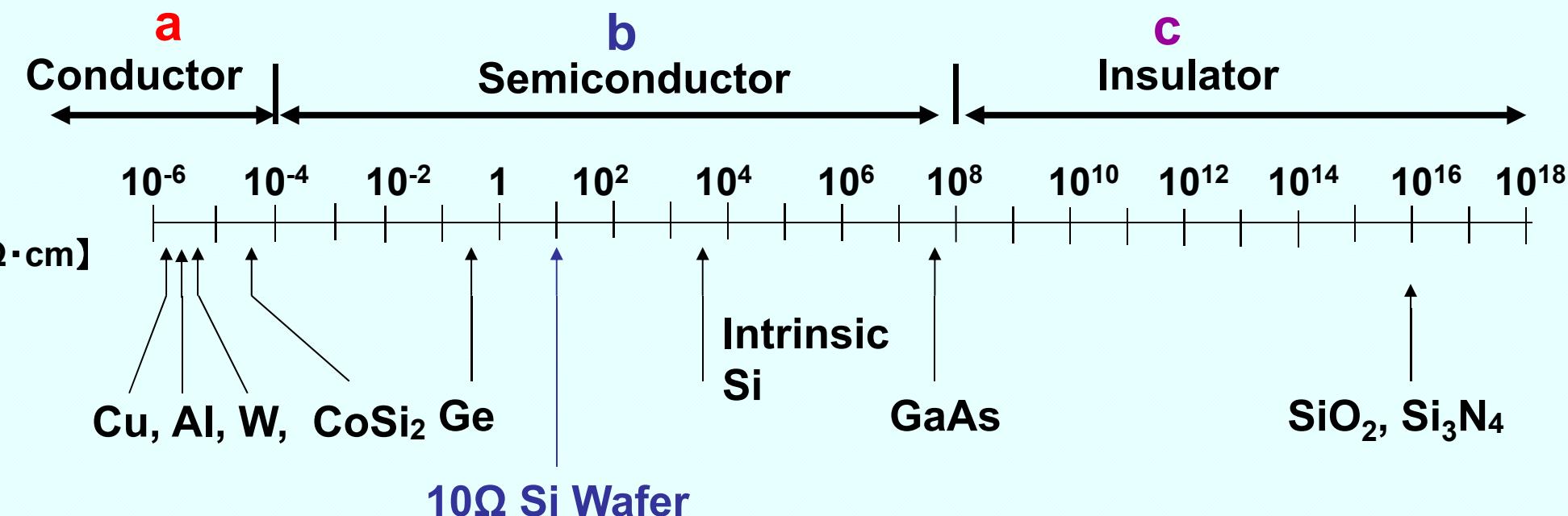
***At higher temperatures or under light, pure or intrinsic semiconductors can become conductive.***

***The addition of impurities to a pure semiconductor can also increase its conductivity.***

# What is Semiconductor?

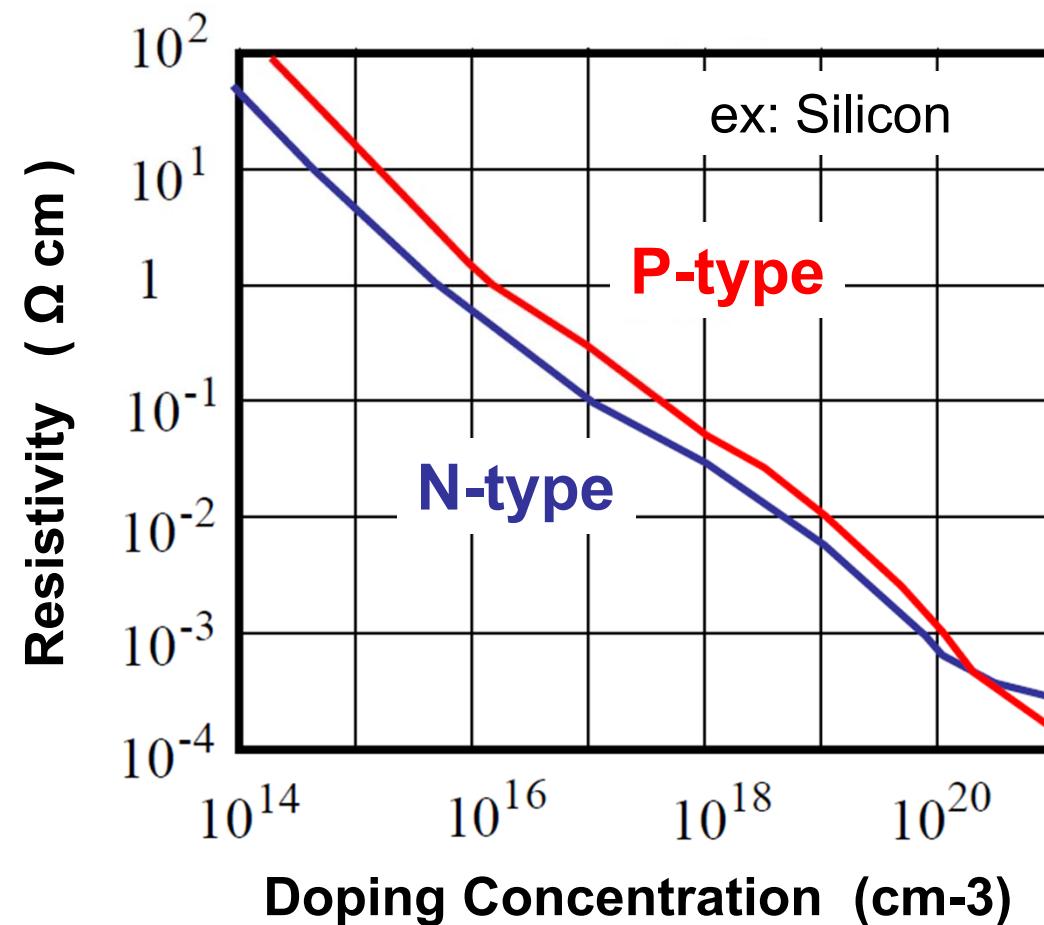
- a) **Conductor (Cu, Al)**  
electron free from atomic bound
- b) **Semiconductor (Si, Ge, GaAs)**  
electron loosely bounded to atom
- c) **Insulator ( $\text{SiO}_2$ ,  $\text{SiN}$ )**  
electron tightly bounded to atom

Materials are grouped by 3 types in electrical resistivity



# What is Semiconductor?

The addition of impurities (doping) to semiconductor can control electrical resistivity.



# Silicon Ingot and Wafer

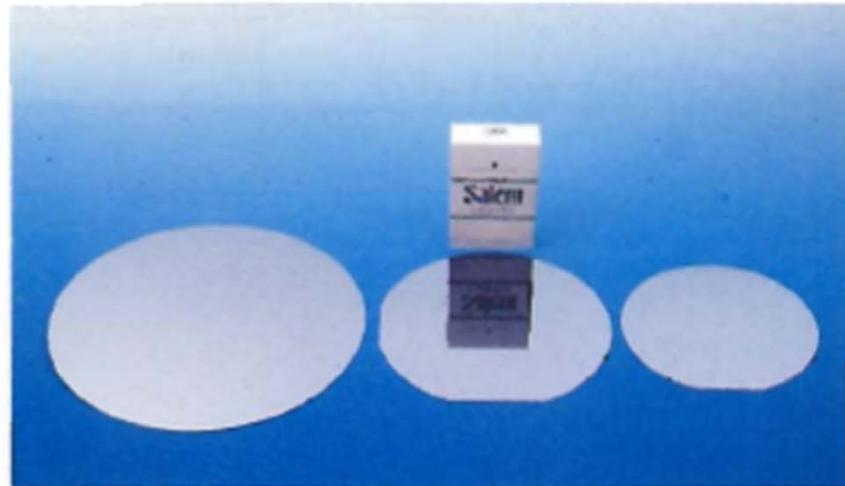


Single-crystal Silicon

Silicon (Si) wafer

Diameter: 300 mm (12 inch)

Thickness: 750  $\mu\text{m}$



Silicon wafer

Si ingot: purity 99.999999999 %

# Crystal Structure of Silicon

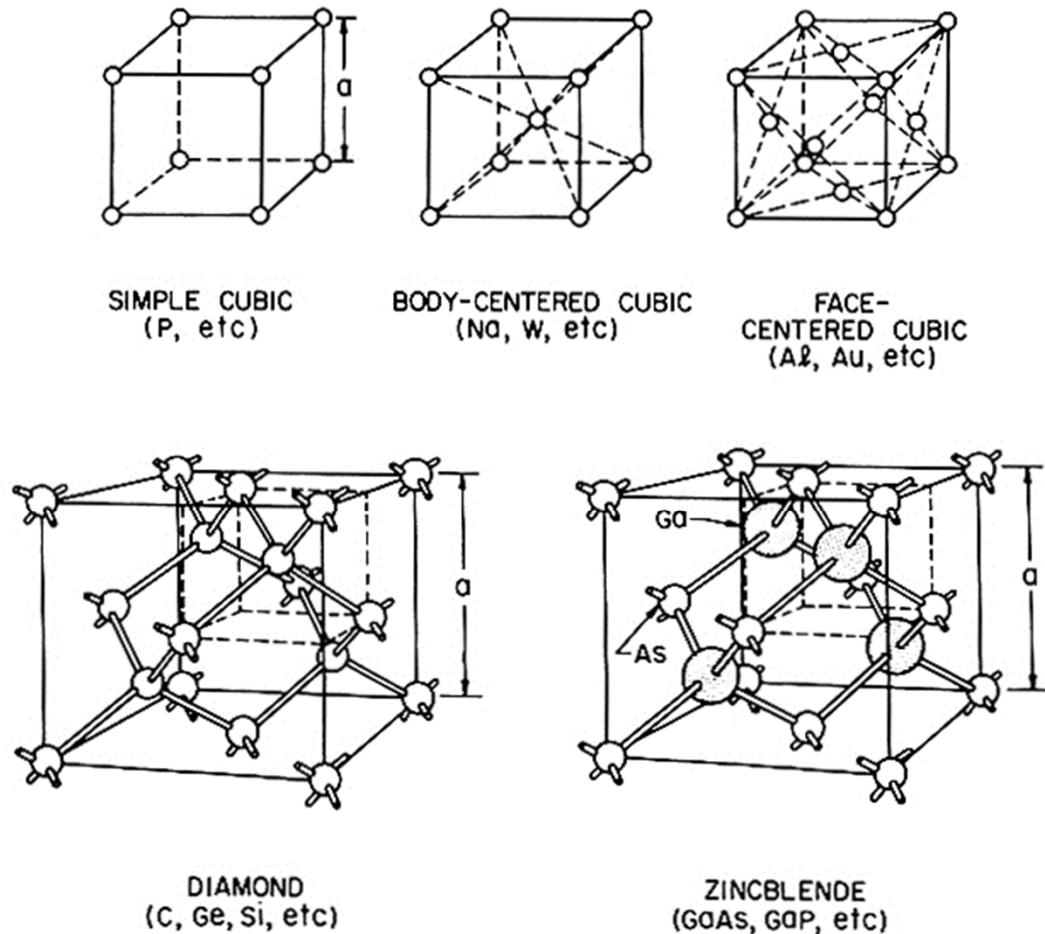
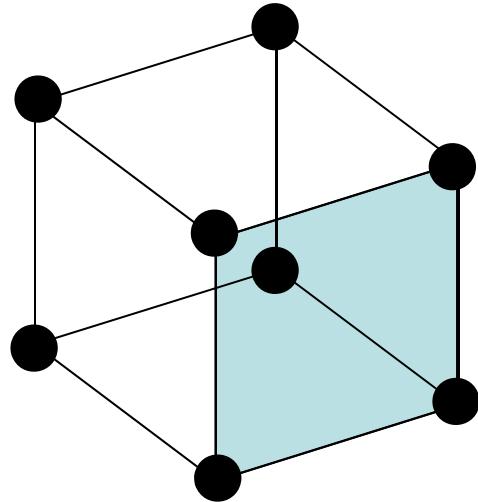


Fig. 1 Some important unit cells (direct lattices) and their representative elements or compounds; a is the lattice constant.

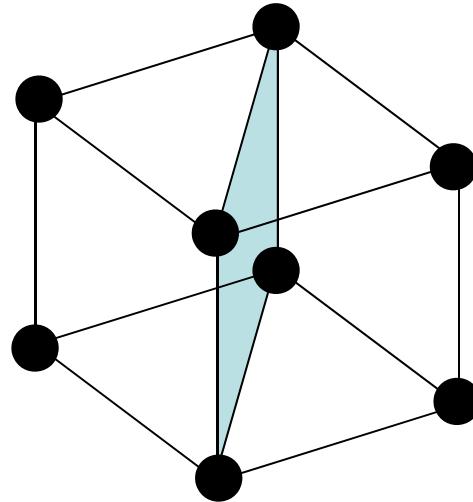
**Silicon belongs to the cubic crystal system and has a **diamond structure****

**This is characterized by having each atom symmetrically surrounded by four equally spaced neighbors**

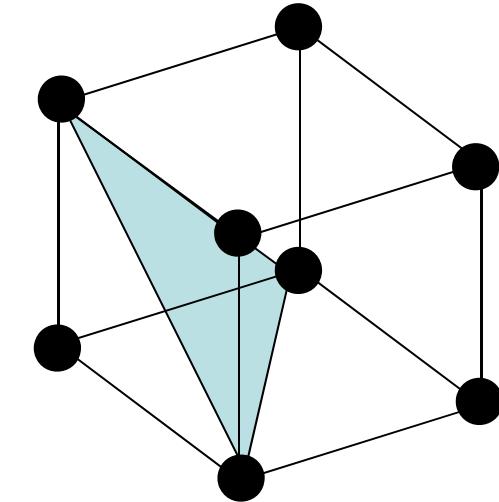
# Crystal Planes



**(100) plane**



**(110) plane**



**(111) plane**

# Semiconductor: Intrinsic and Extrinsic

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## Intrinsic semiconductor

A perfect semiconductor which has no impurities

Its characteristics comes from the semiconductor itself

## Extrinsic semiconductor

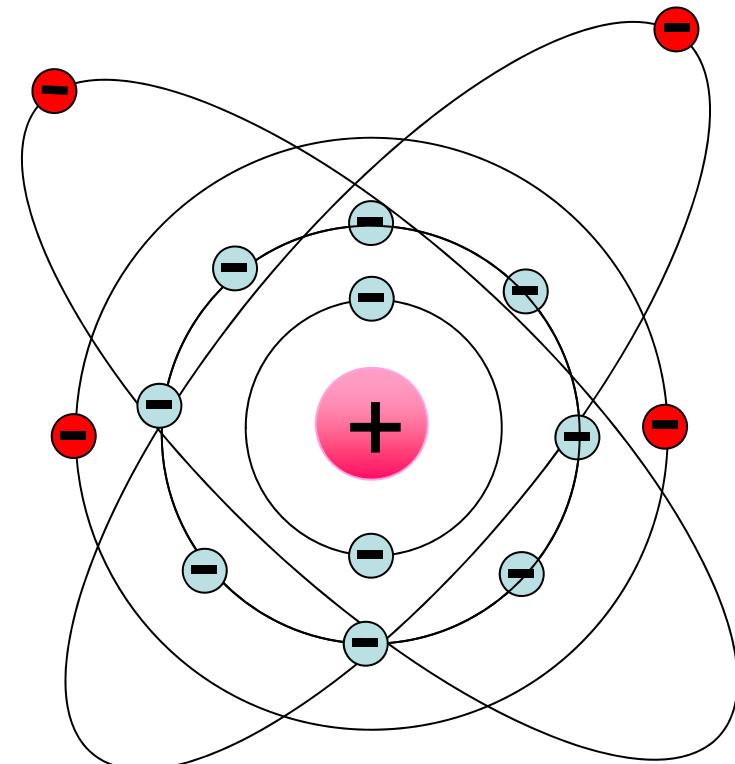
A semiconductor to which impurity is doped

Some part of its characteristics comes from the doped impurity

# Periodic Table

**Group III    IV    V**

5 B	6 C	7 N
13 Al	14 Si	15 P
31 Ga	32 Ge	33 As



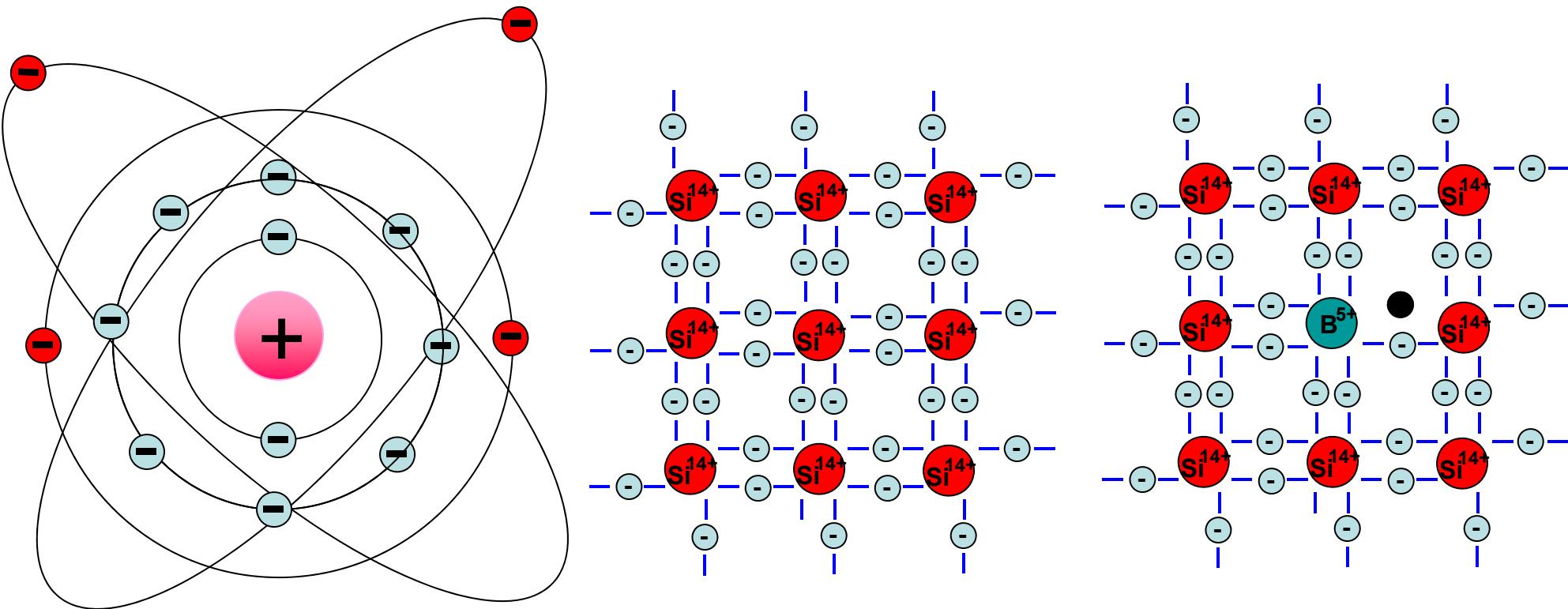
# Extrinsic Silicon

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**Silicon** crystal is rarely used in the pure state. Usually, some impurity called a dopant is added in small controlled amount

If a **Boron** atom is substituted for a **Silicon** atom in the **Silicon** lattice, the **Boron** atom with only three of available electrons would be able to form bonds to only three of the four adjacent **Silicon** atom and a hole would be formed

# P-type Silicon - Acceptor



## P-type Silicon - Acceptor

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It is very easy for an electron from a nearby **Silicon** to **Silicon** bond to fall into this hole and effectively move the hole away from the **Boron** atom

Since the **Boron** atom will accept an electron, **Boron** and the other elements of Group III (**B, Ga**) are referred to as **acceptors**

**Silicon** with acceptor is called as **P-type Silicon**, since “positive” holes are generated and contribute a current flow

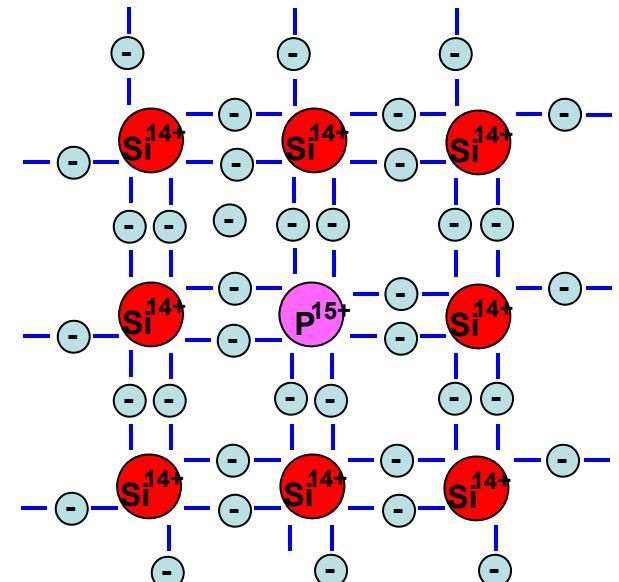
# N-type Silicon - Donor

If a Group V atom, such as **Phosphorus**, is introduced into the **Silicon lattice**, it will have an extra electron which may easily break away, becoming a conduction electron

The **Phosphorus** is referred to a **donor**, since it donates an electron to the conduction band.

Other donor is **As**

**Silicon with donor is called as N-type Silicon**, since “negative” electrons are generated and contribute the current flow



## Exercise

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If we dope “**acceptor**” to the intrinsic silicon, silicon becomes P-type. If we dope “**donor**” to the intrinsic silicon, silicon becomes N-type.

If we dope both “**acceptor**” and “**donor**” to the intrinsic silicon, what happens? and how about the physical properties?

(a) Dosage of Acceptor = that of Donor

(b) Dosage of Acceptor > that of Donor

(c) Dosage of Acceptor < that of Donor

# Properties of Silicon and Silicon Oxide

**TABLE I** Physical Properties of Si and SiO<sub>2</sub> at Room Temperature (300 K)

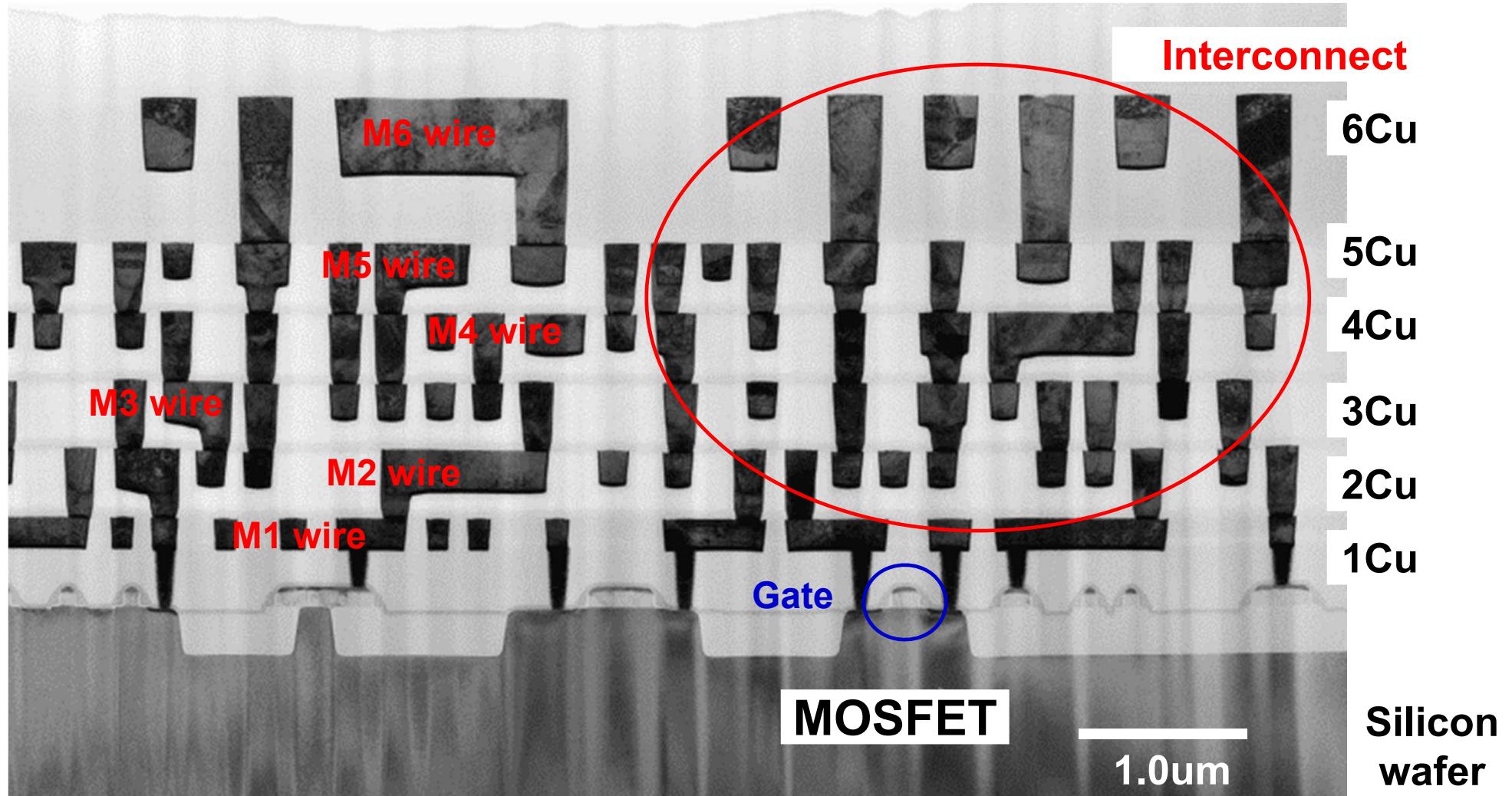
Property	Si	SiO <sub>2</sub>
Atomic/molecular weight	28.09	60.08
Atoms or molecules/cm <sup>3</sup>	$5.0 \times 10^{22}$	$2.3 \times 10^{22}$
Density (g/cm <sup>3</sup> )	2.33	2.27
Crystal structure	Diamond	Amorphous
Lattice constant (Å)	5.43	—
Energy gap (eV)	<u>1.12</u>	8–9
Dielectric constant	11.7	<u>3.9</u>
Intrinsic carrier concentration (cm <sup>-3</sup> )	<u><math>1.4 \times 10^{10}</math></u>	—
Carrier mobility (cm <sup>2</sup> /V-s)	Electron: 1430 Hole: 470	—
Effective density of states (cm <sup>-3</sup> )	Conduction band, $N_c$ : $3.2 \times 10^{19}$ Valence band, $N_v$ : $1.8 \times 10^{19}$	—
Breakdown field (V/cm)	$3 \times 10^5$	$>10^7$
Melting point (°C)	1415	1600–1700
Thermal conductivity (W/cm·°C)	1.5	0.014
Specific heat (J/g·°C)	0.7	1.0
Thermal diffusivity (cm <sup>2</sup> /s)	0.9	0.006
Thermal expansion coefficient (°C <sup>-1</sup> )	$2.5 \times 10^{-6}$	$0.5 \times 10^{-6}$

# **LSI Device on a Real Silicon Wafer**

**- Structure of MOS Transistor and Interconnect**

# LSI Final Cross-section

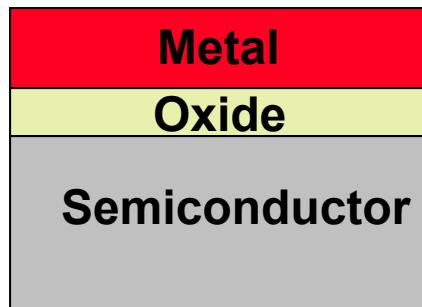
Cross-section SEM photograph of SoC Product Application (6 layers Cu metal wire)



# What is MOS

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**M**(Metal) - **O**(Oxide) - **S**(Semiconductor)



**MOS Structure**

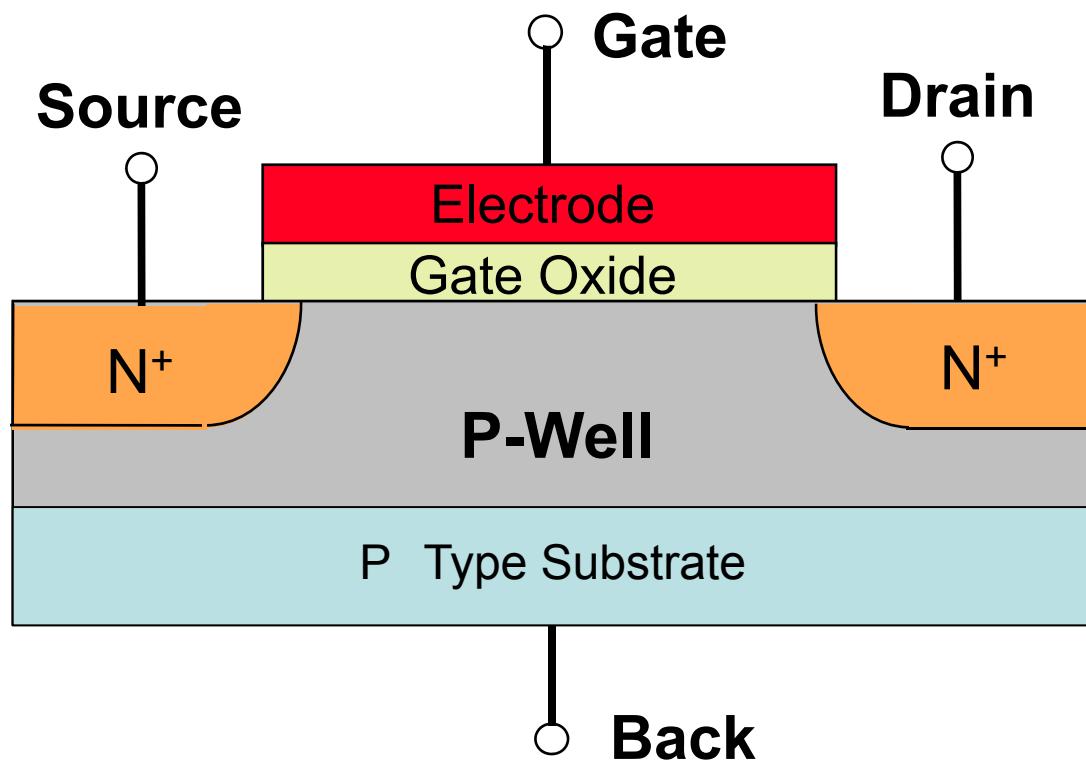
# Basic Structure of MOSFET - N channel MOS

**Electrode:** Highly doped Poly-Silicon

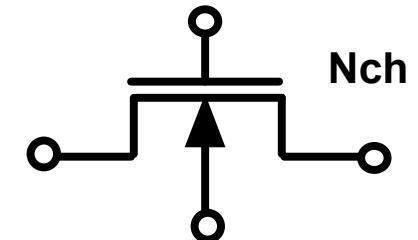
**Source and Drain:** Highly doped N-type ( $N^+$ )

**Gate Oxide:** Silicon Oxide

N channel MOS Transistor



Circuit symbol



# Basic Structure of MOSFET - Exercise

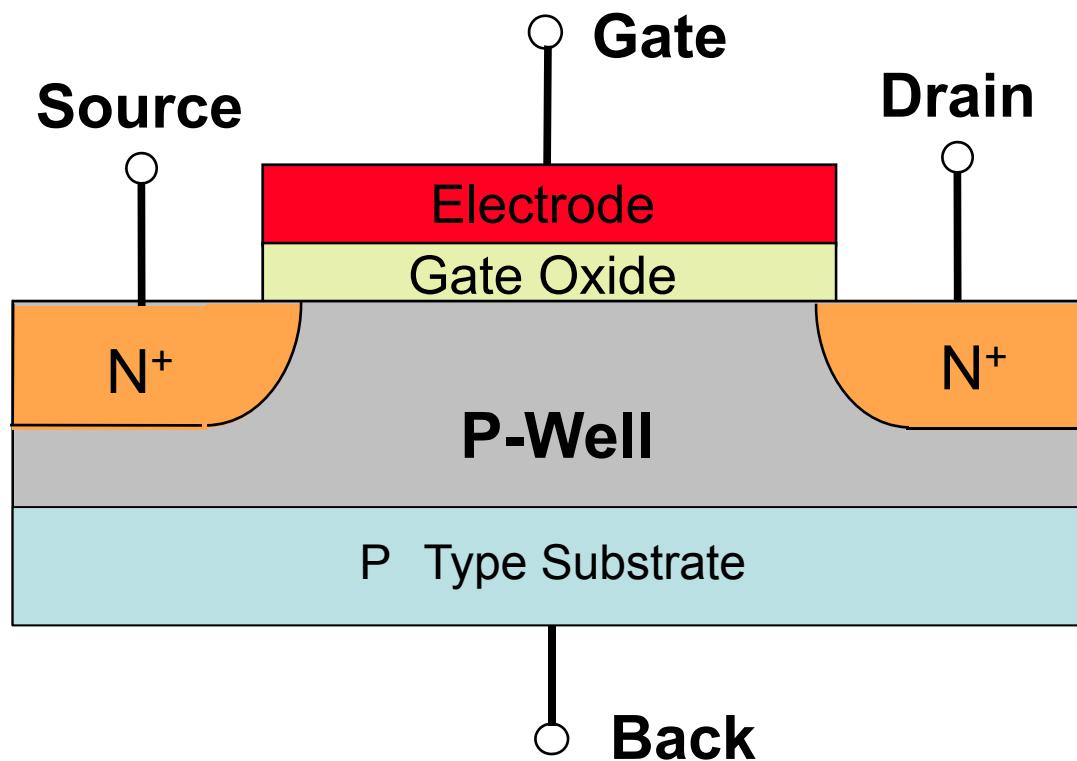
**Electrode:** Highly doped Poly-Silicon

**Source and Drain:** Highly doped N-type ( $N^+$ )

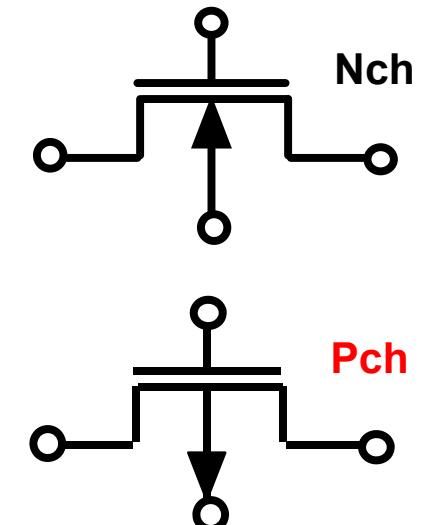
**Gate Oxide:** Silicon Oxide

**Short exercise (3 minutes)**

Draw the cross-section of P channel MOS transistor.



Circuit symbol



# Basic Structure of MOSFET - P channel MOS

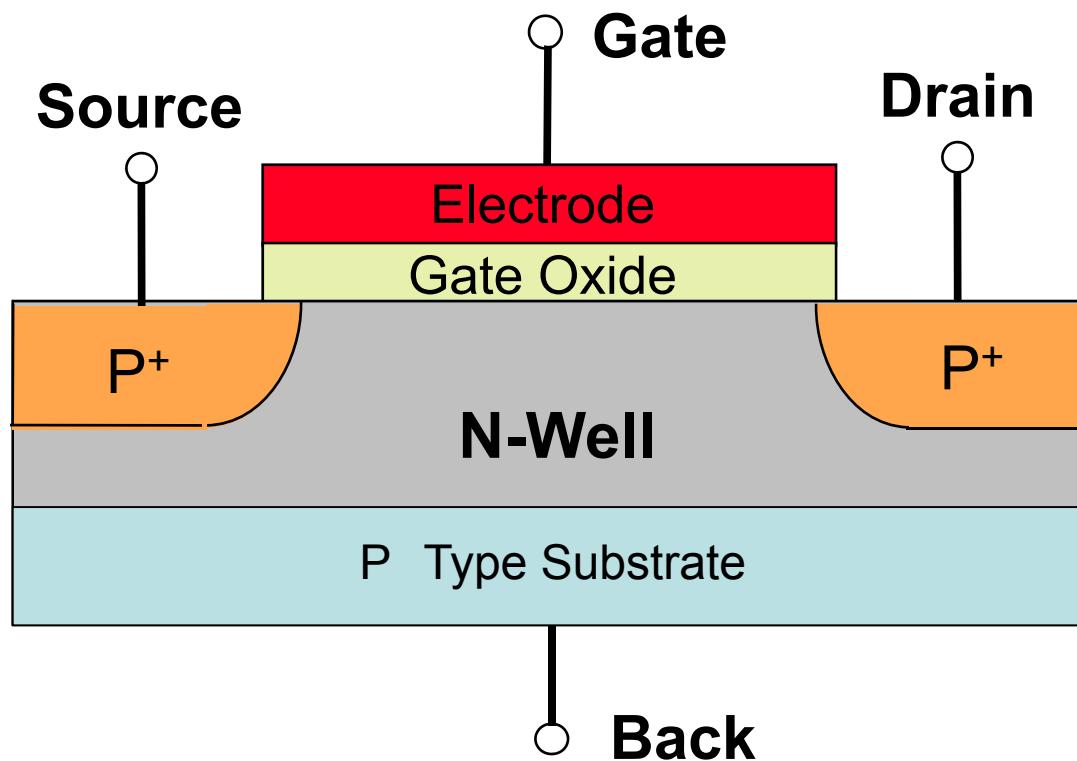
**Electrode:** Highly doped Poly-Silicon

**Source and Drain:** Highly doped P-type ( $P^+$ )

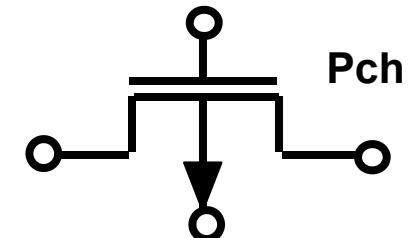
**Gate Oxide:** Silicon Oxide

**Short exercise (3 minutes)**

**Answer**



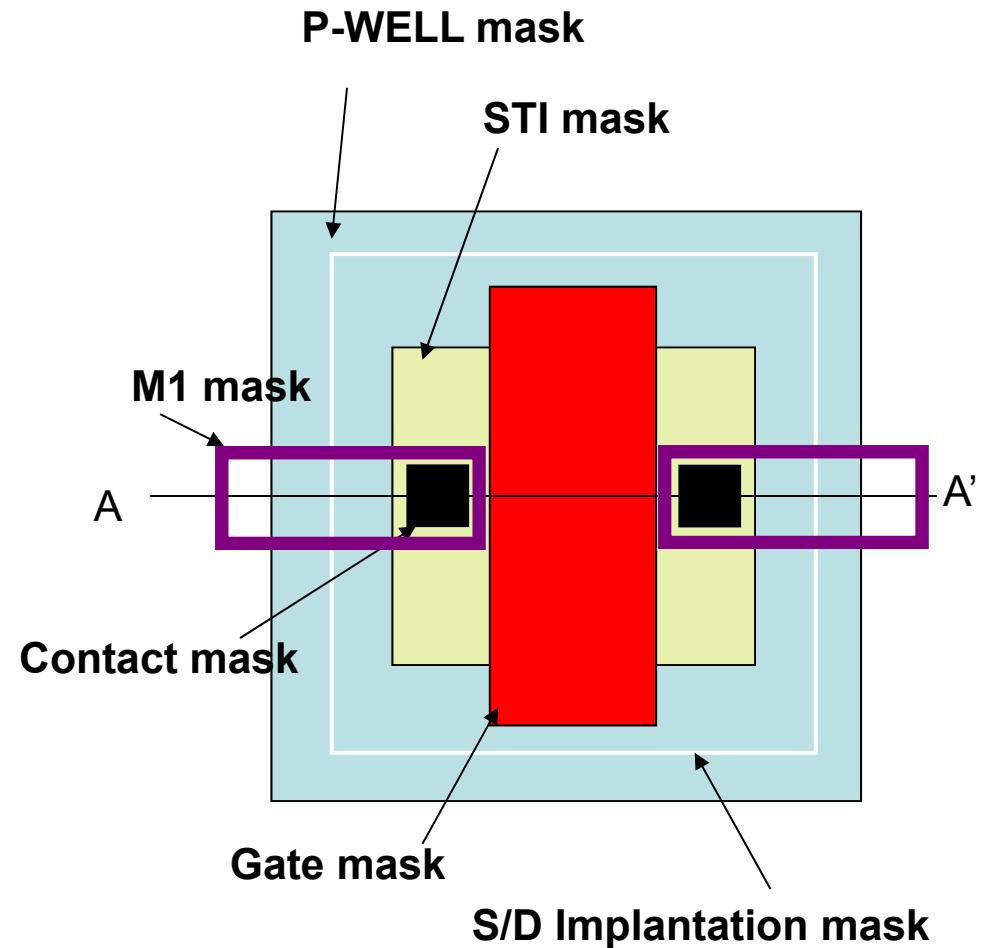
**Circuit symbol**



# MOSFET

Exercise (10 minutes)

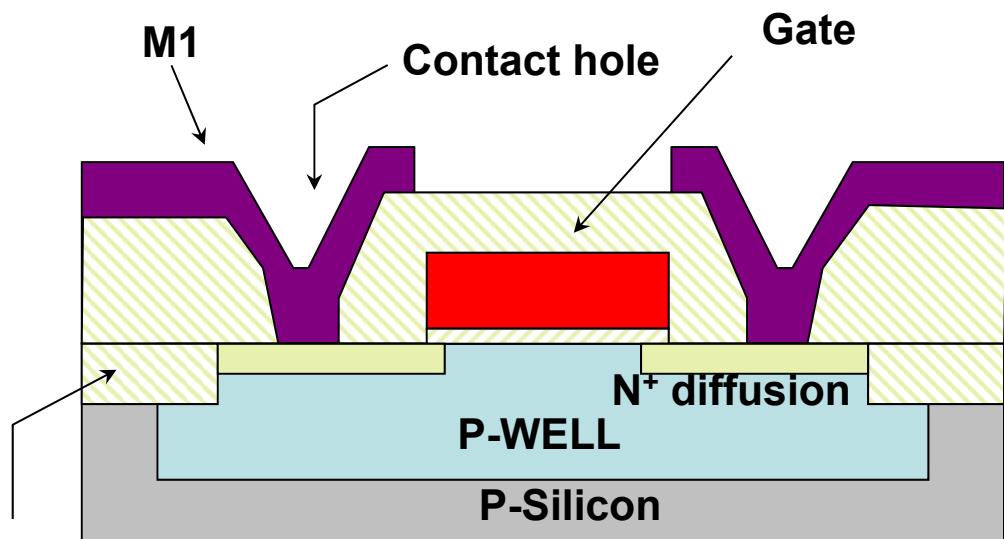
Draw the cross-section of  
the line A-A'.



Basic N Channel MOS  
(cross section view)

**MASK LAYOUT (top view)**

# MOSFET (with the cross-section)

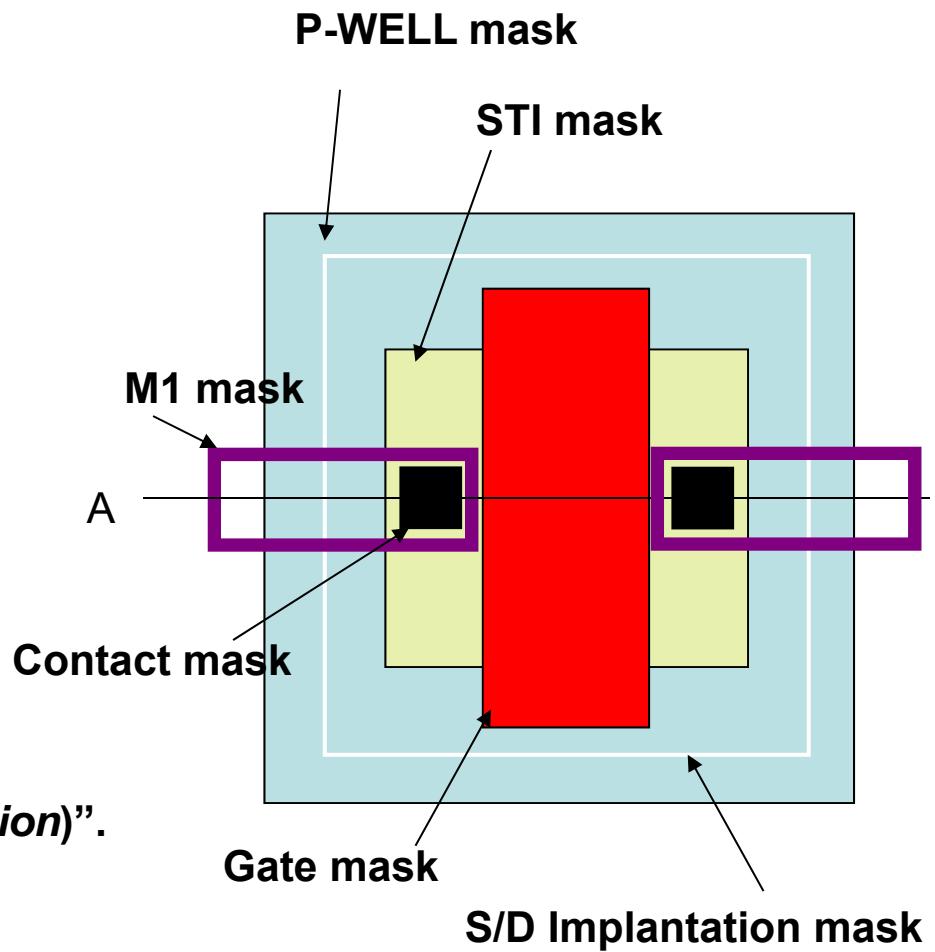


STI

The cross-section at A-A'.

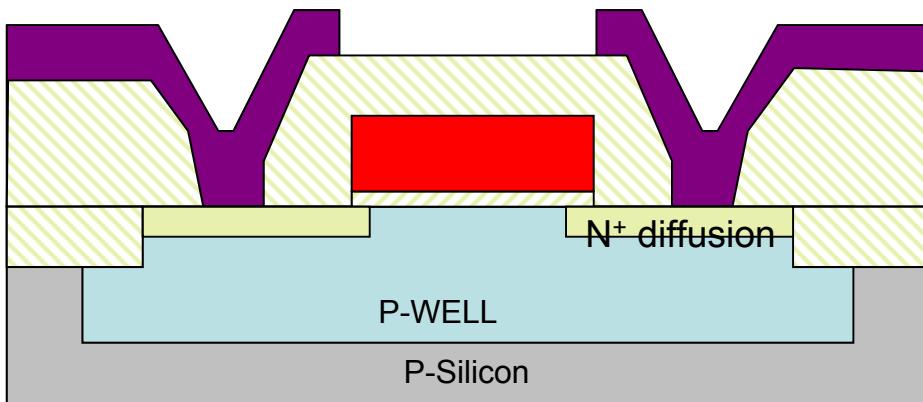
Device isolation is “STI (*Shallow Trench Isolation*)”.

**Basic N Channel MOS**  
(cross section view)

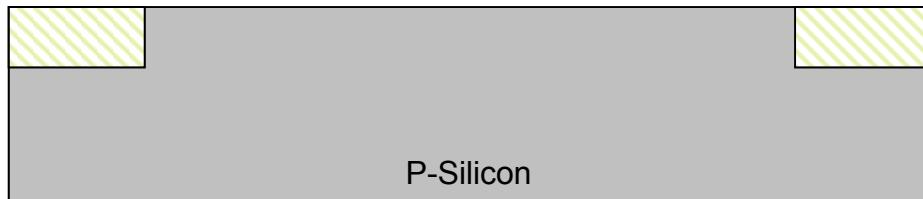


**MASK LAYOUT (top view)**

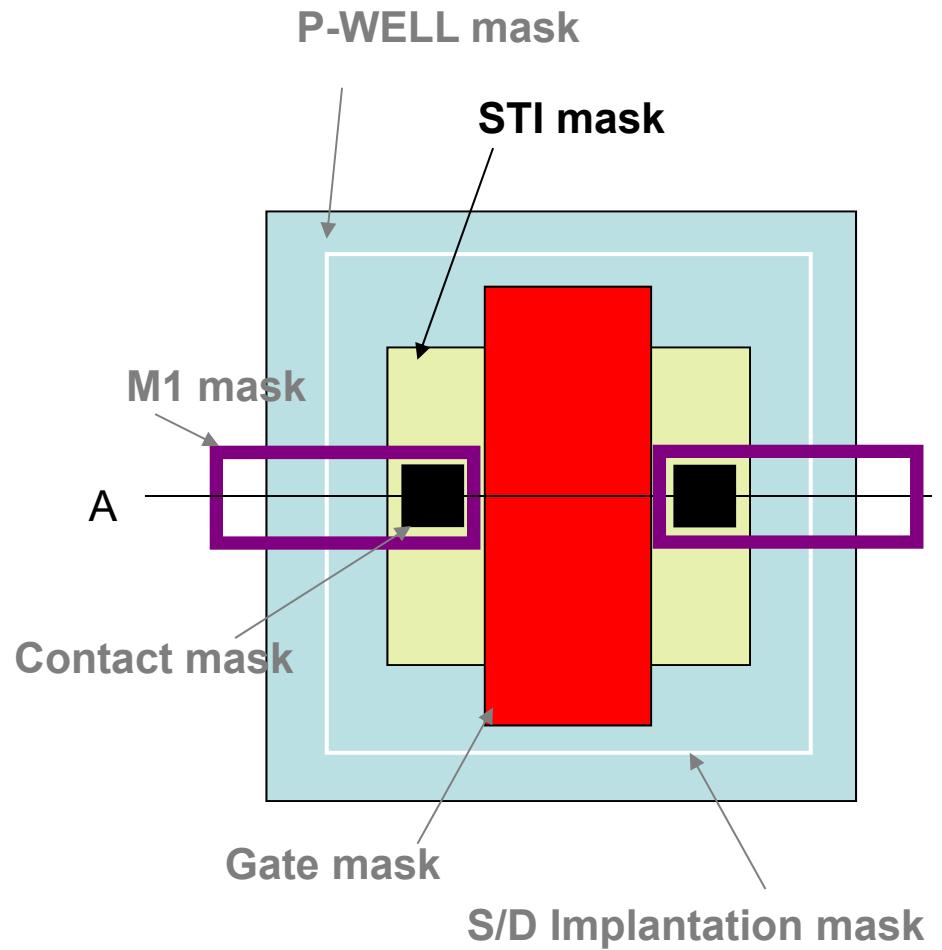
# MOSFET (with the cross-section)



## 1. STI : Shallow Trench Isolation

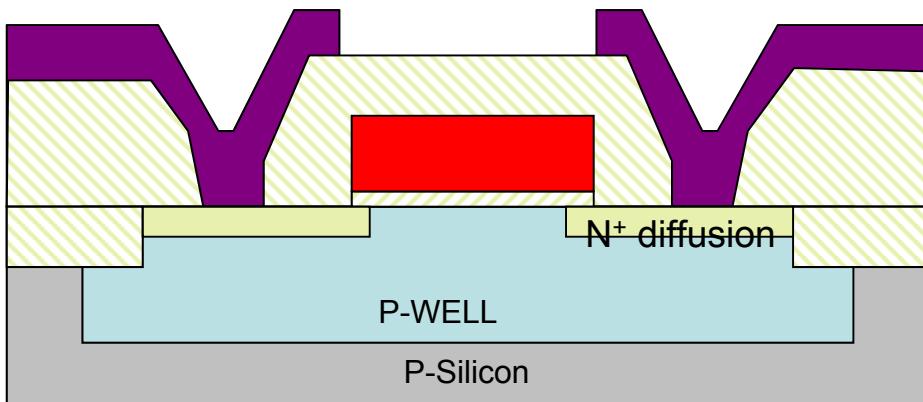


**Basic N Channel MOS  
(cross section view)**

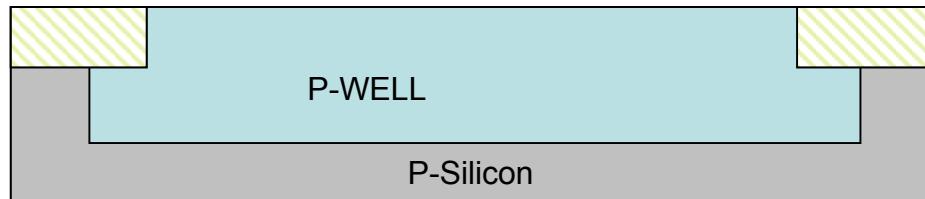


**MASK LAYOUT (top view)**

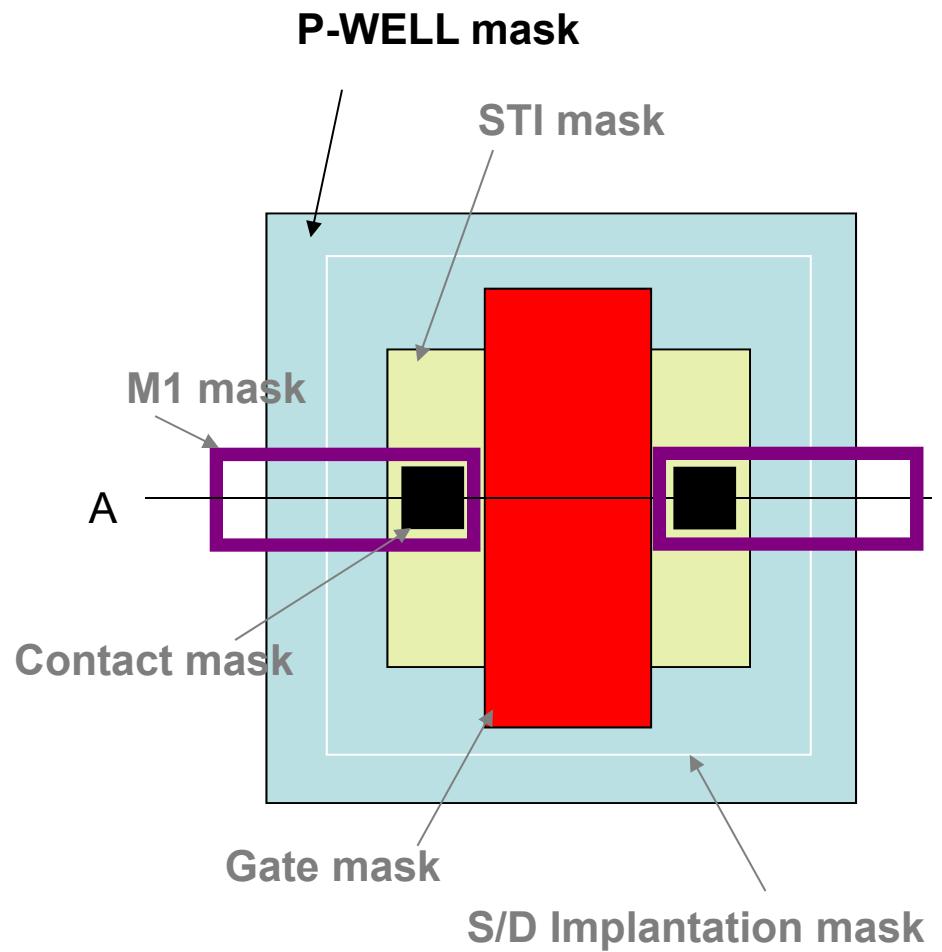
# MOSFET (with the cross-section)



## 2. WELL

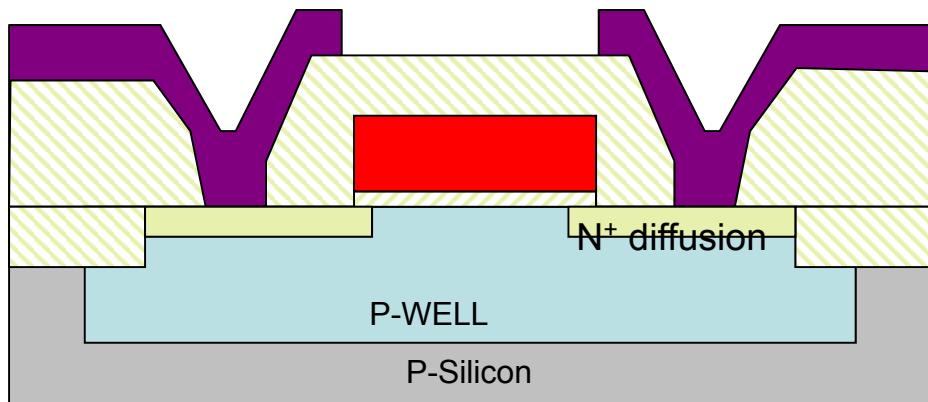


**Basic N Channel MOS  
(cross section view)**

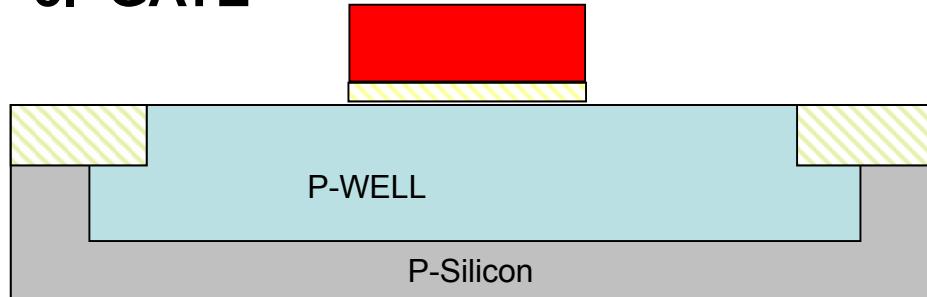


**MASK LAYOUT (top view)**

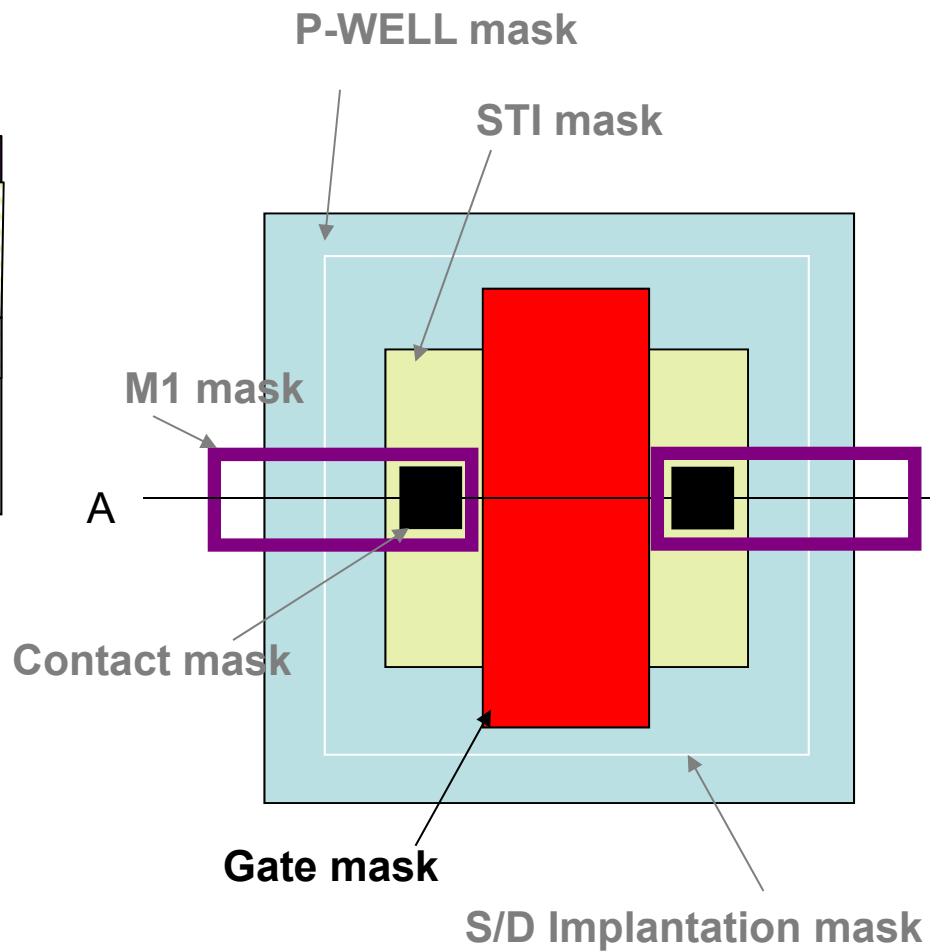
# MOSFET (with the cross-section)



## 3. GATE

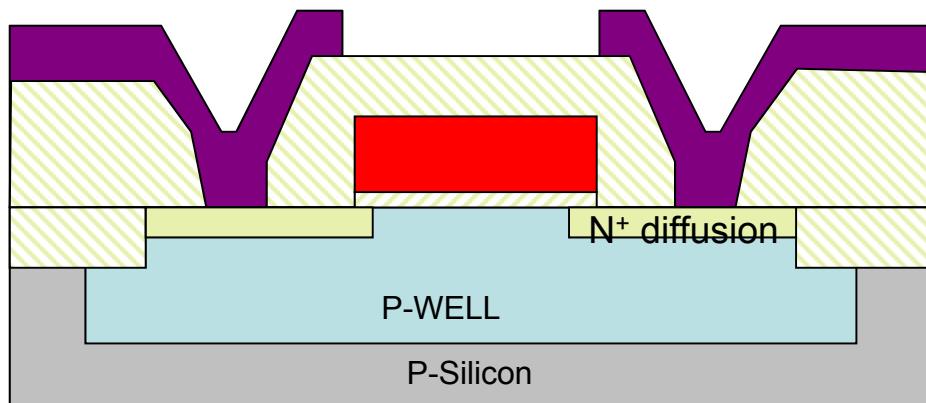


**Basic N Channel MOS  
(cross section view)**

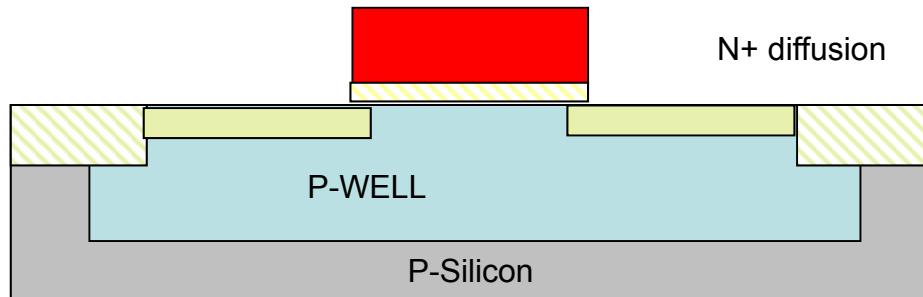


**MASK LAYOUT (top view)**

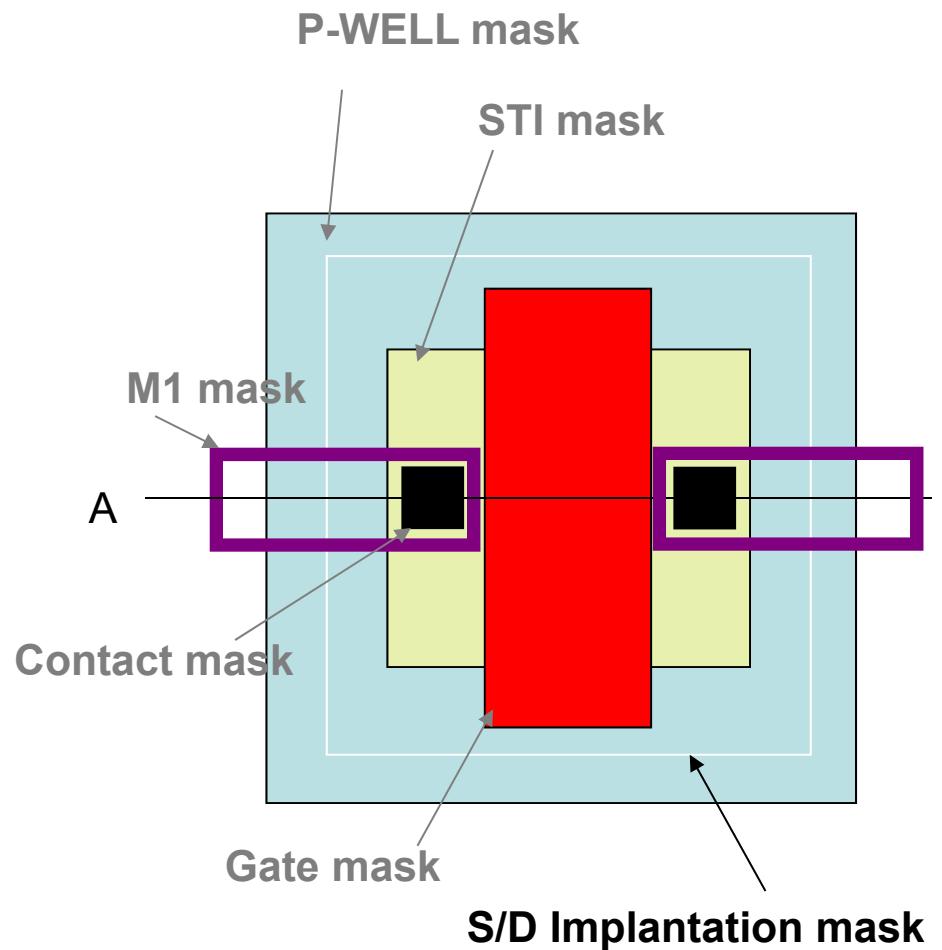
# MOSFET (with the cross-section)



## 4. Source/Drain

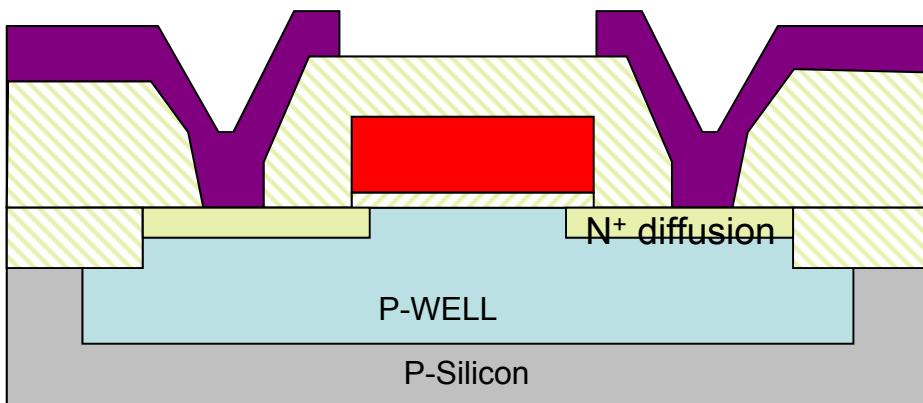


**Basic N Channel MOS  
(cross section view)**

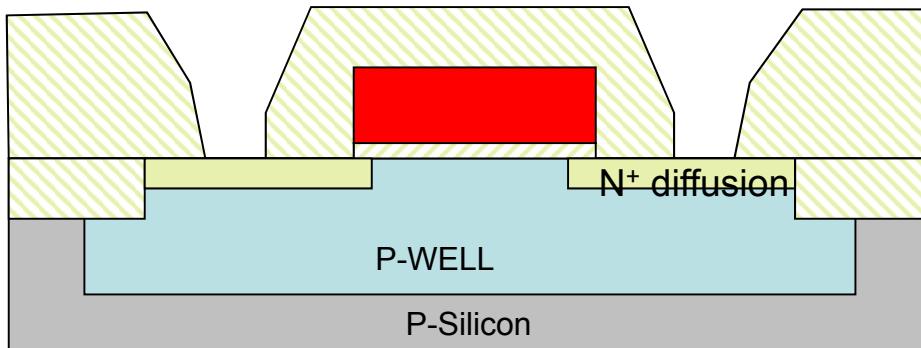


**MASK LAYOUT (top view)**

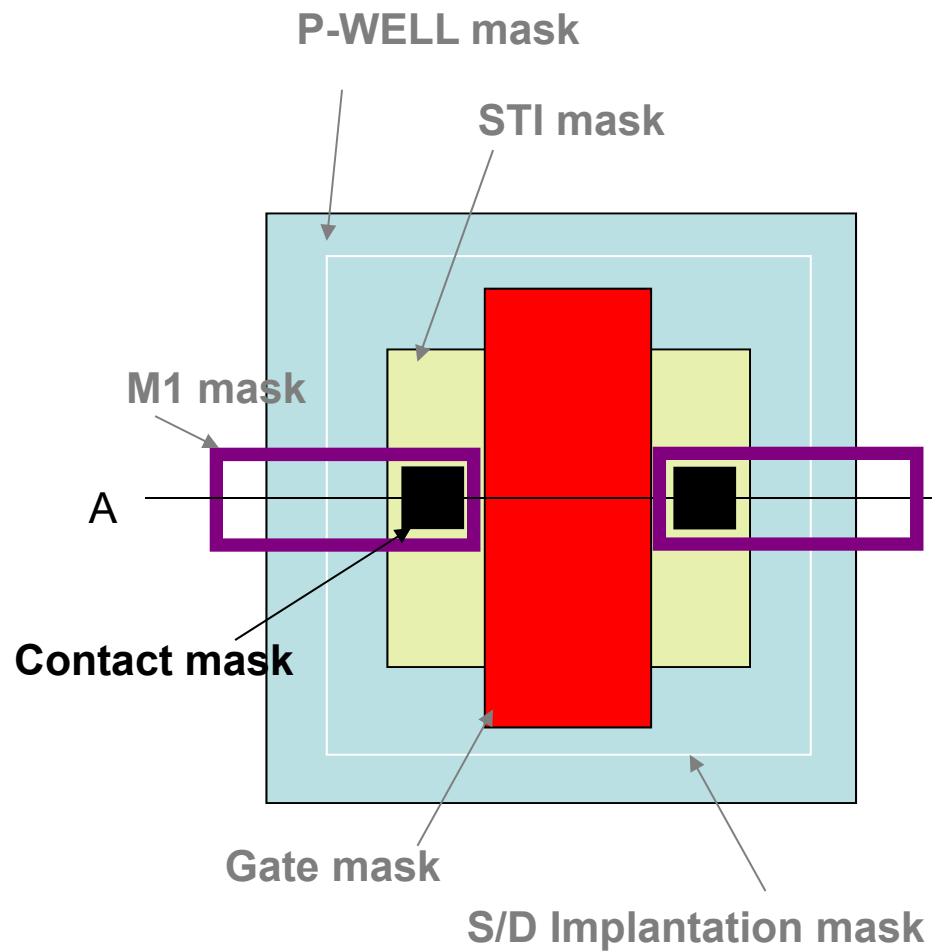
# MOSFET (with the cross-section)



## 5. Contact Hole

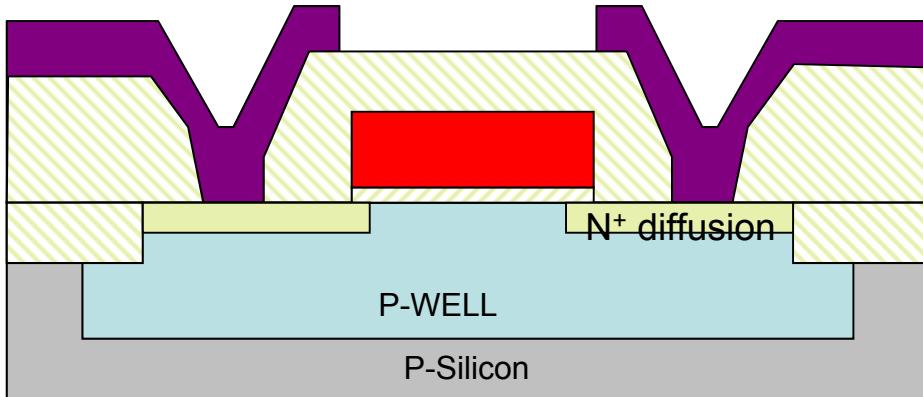


**Basic N Channel MOS  
(cross section view)**

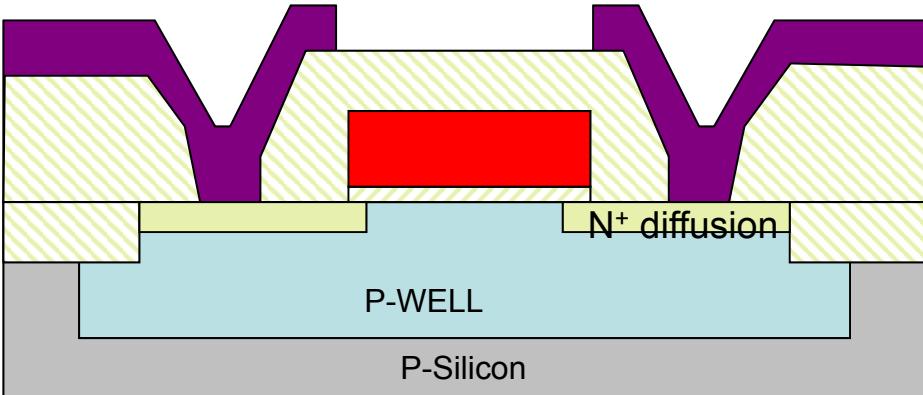


**MASK LAYOUT (top view)**

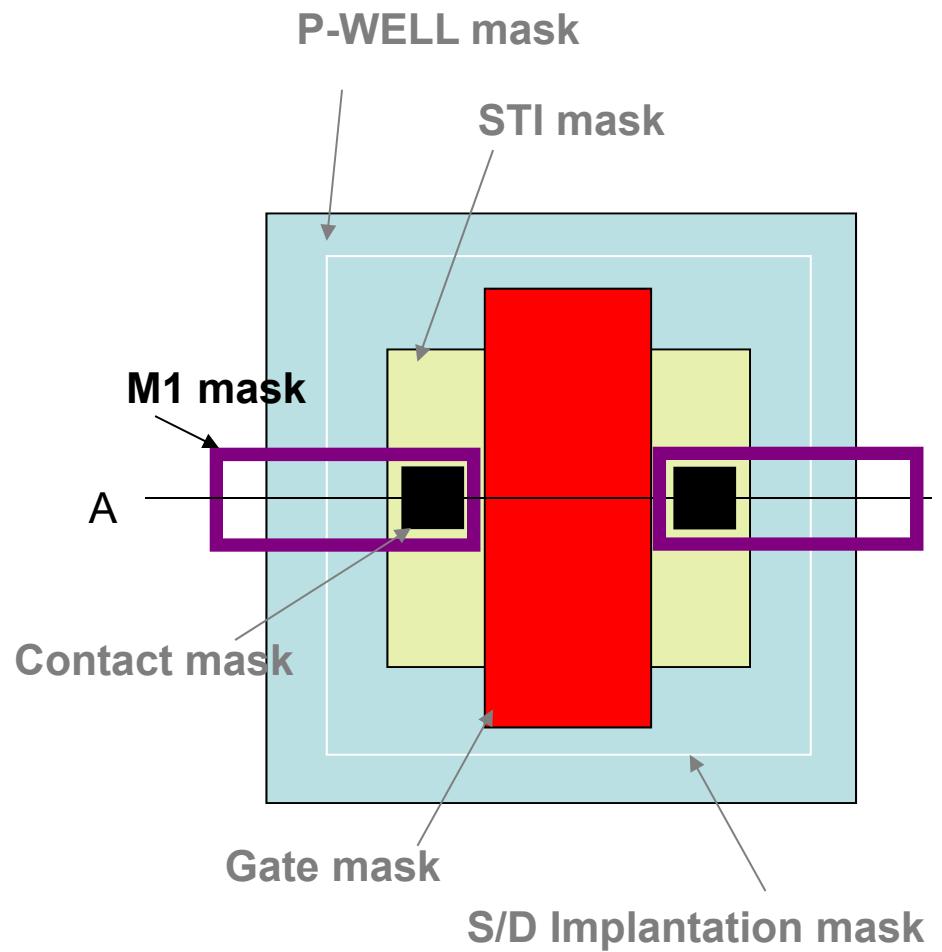
# MOSFET (with the cross-section)



## 6. METAL



**Basic N Channel MOS  
(cross section view)**

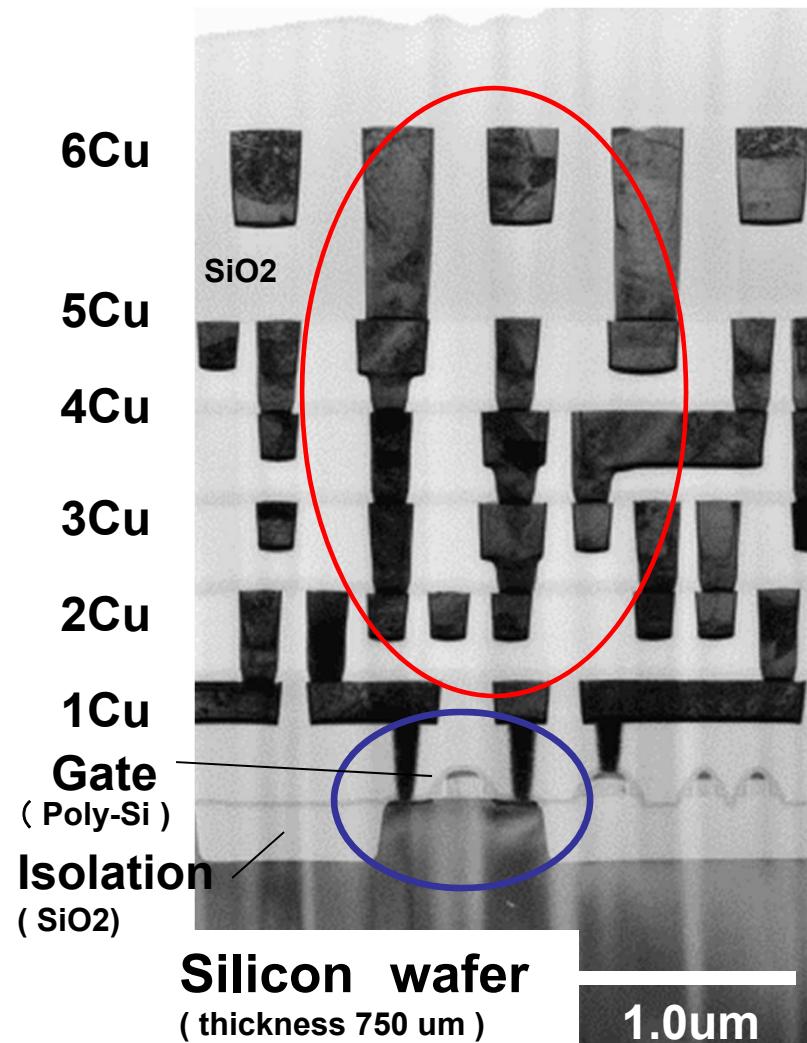


**MASK LAYOUT (top view)**

# **Basic Steps of LSI Wafer Process**

- Module Processes

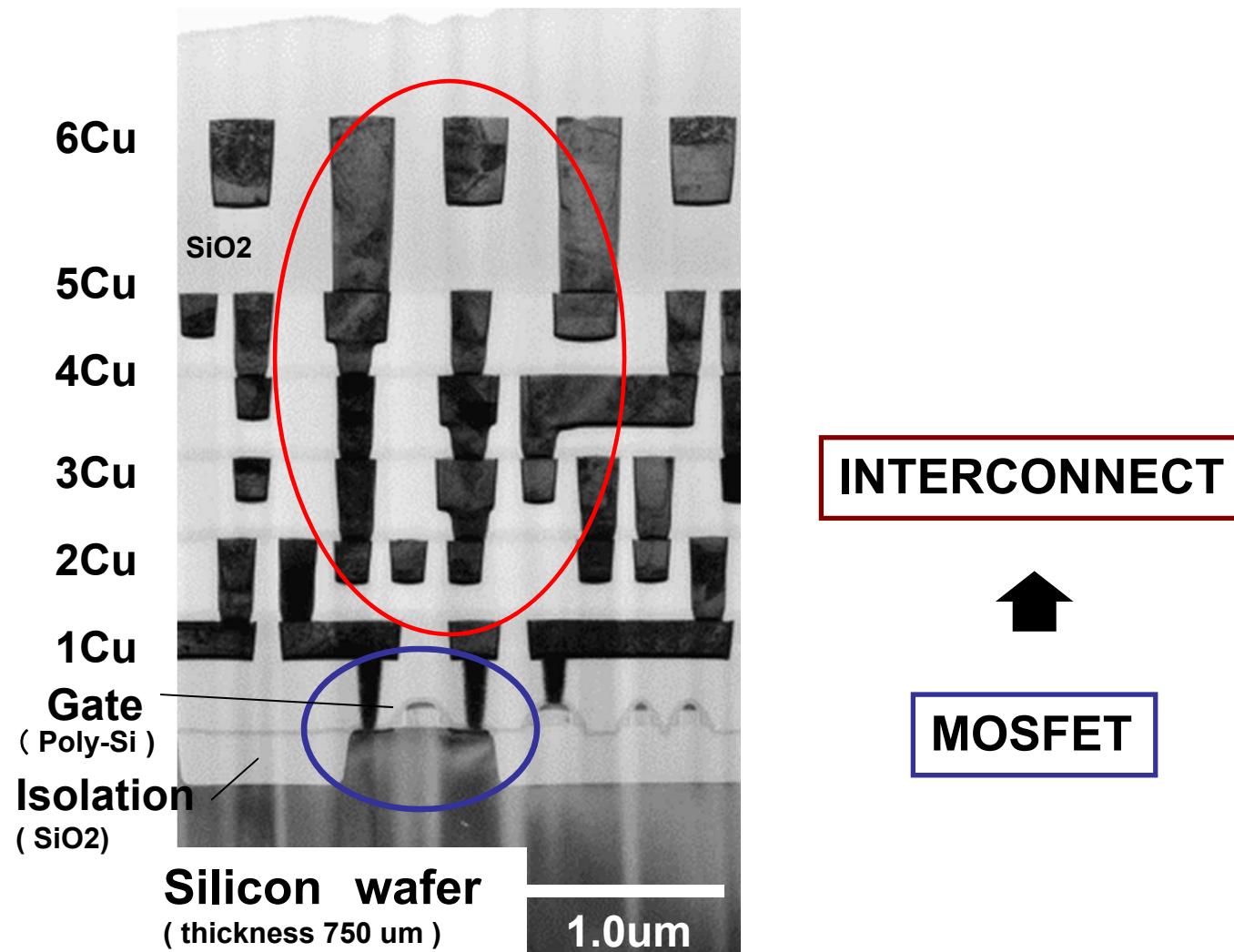
# LSI Wafer Process - Rough Overview



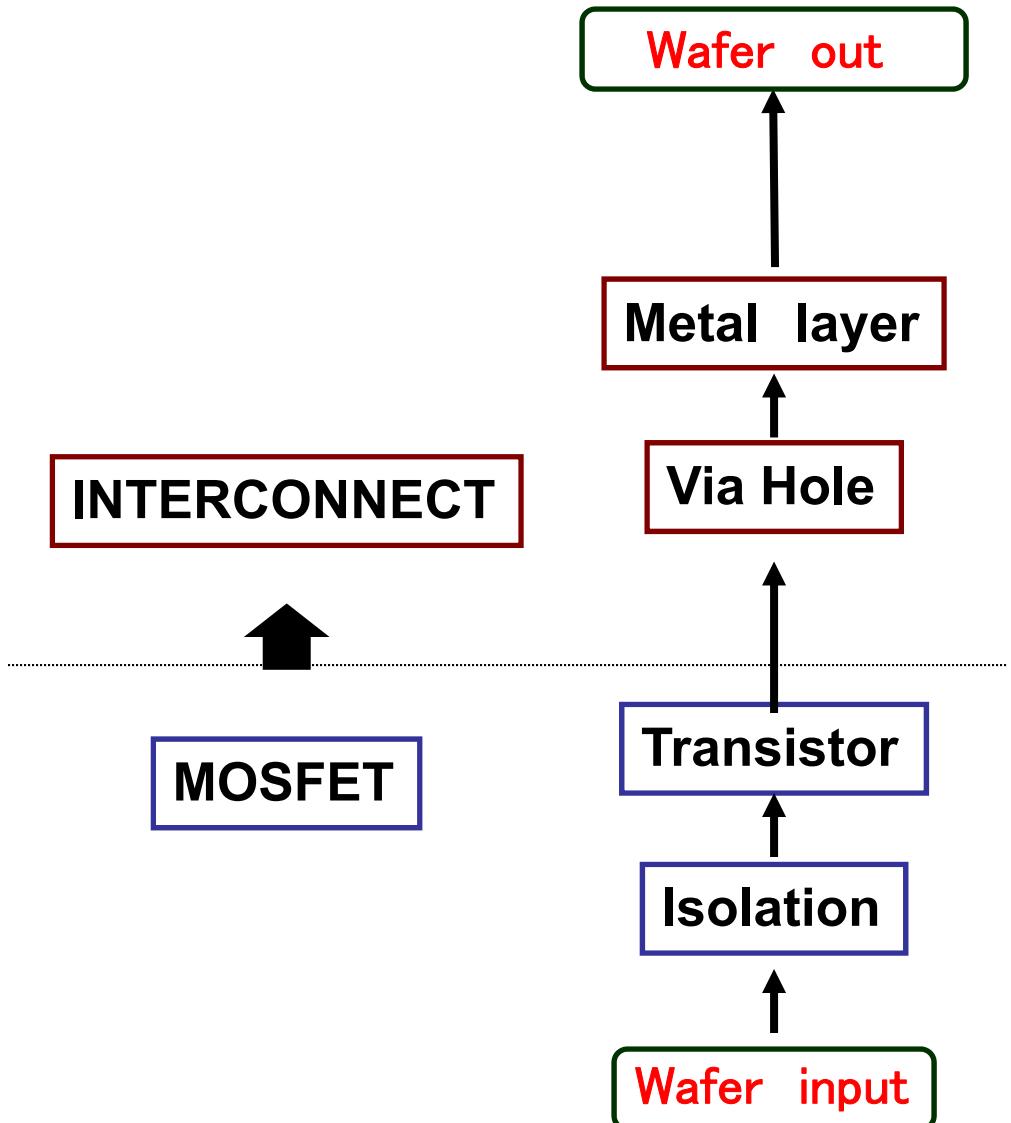
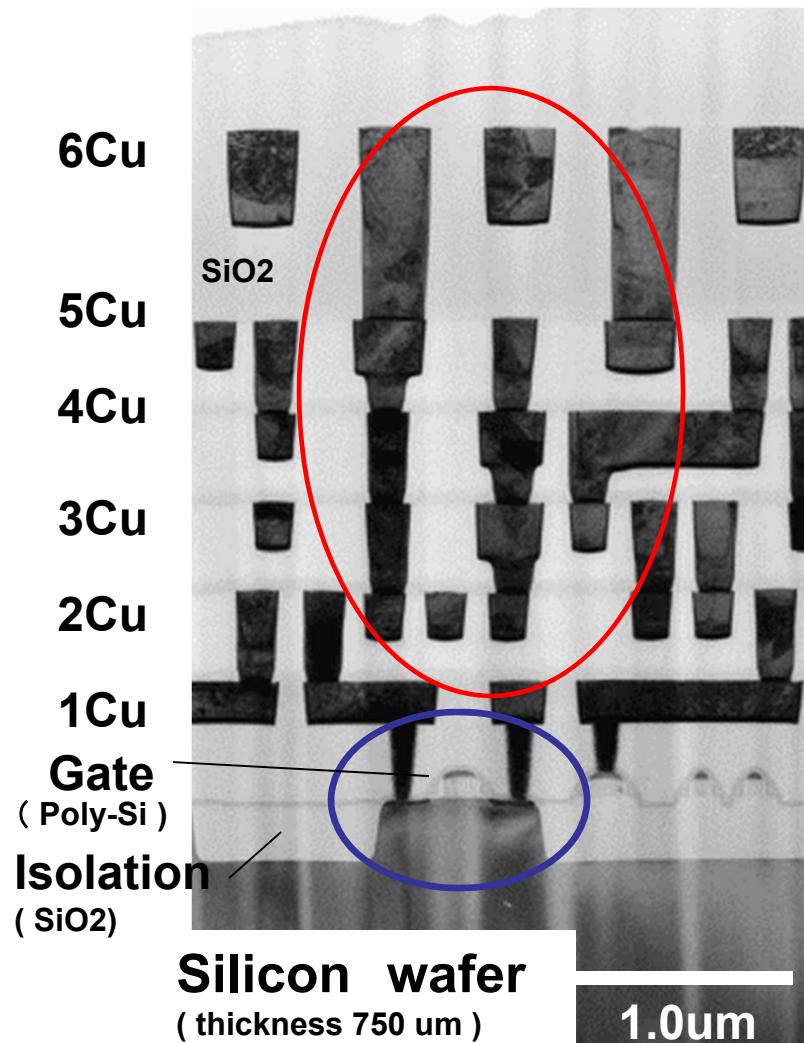
INTERCONNECT

MOSFET

# LSI Wafer Process - Rough Overview



# LSI Wafer Process - Rough Overview





# **Basic Steps of LSI Wafer Process**

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**These four steps are repeatedly performed during wafer process**

- A) Cleaning**
- B) Thin Film formation**
- C) Patterning**
- D) Doping**



# **Basic Steps of LSI Wafer Process**

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**A) Cleaning**

**B) Thin Film formation**

**C) Patterning**

**D) Doping**

# Basic Steps of LSI Wafer Process

---

**A) Cleaning**

WAFER

**B) Thin Film formation**

**C) Patterning**

**D) Doping**

# Basic Steps of LSI Wafer Process

## A) Cleaning

WAFER

## B) Thin Film formation

WAFER

## C) Patterning

## D) Doping

# Basic Steps of LSI Wafer Process

## A) Cleaning



## B) Thin Film formation



## C) Patterning - Photolithography



## D) Doping

# Basic Steps of LSI Wafer Process

## A) Cleaning



## B) Thin Film formation



## C) Patterning - Photolithography



## D) Doping



# Basic Steps of LSI Wafer Process

## A) Thin Film formation

- **Oxidation**: Thermal Oxidation
- **CVD (Chemical Vapor Deposition)**: Deposition of Poly-Silicon, Silicon Nitride, Silicon Oxide
- **Evaporation, Sputtering**: Aluminum, Metal, Silicide (Alloy of Silicon and other metal)
- **Plating**: Cu

## B) Patterning

- **Photolithography**: Forming photo-resist patterns using Ultra-Violet beam
- **Etching**: Wet or Dry etching using Photo-resist as a masking material

# Basic Steps of LSI Wafer Process

## C) Introduction of impurity

- Diffusion: Diffusion of Solid or vapor phase Ion
- Implantation: Ionized impurity bombardment using electric field

## D) Cleaning

- Wafer cleaning using acid or ultra pure water

# Module Processes

## A) Cleaning

WAFER

## B) Thin Film formation

WAFER

## C) Patterning

WAFER

## D) Doping

WAFER

more detailed

### (A) Cleaning

(B)

- Film Formation
- Thermal Process

• Chemical  
Mechanical  
Polishing

(C)

- Etching

- Photolithography

(D)

- Ion Implantation

# Principle of Oxidation

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## 1. Dry Oxidation

Oxidation in Dry Oxygen. Used to form the thin oxide



## 2. Wet Oxidation

Oxidation in steam. Used to form the thick oxide



**Since the diffusion coefficient of  $\text{H}_2\text{O}$  is larger than  $\text{O}_2$ , the wet oxidation can form thicker oxide in shorter time**

# Principle of CVD

**The material gas is transferred to wafer surface where the reaction occurs and the reaction product deposits on wafer**



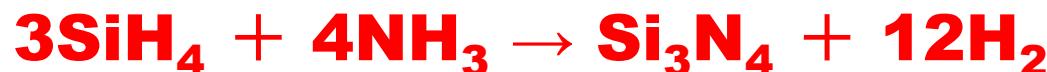
**Thermal decomposition:**



**Oxidation:**



**Reaction:**



# Plasma

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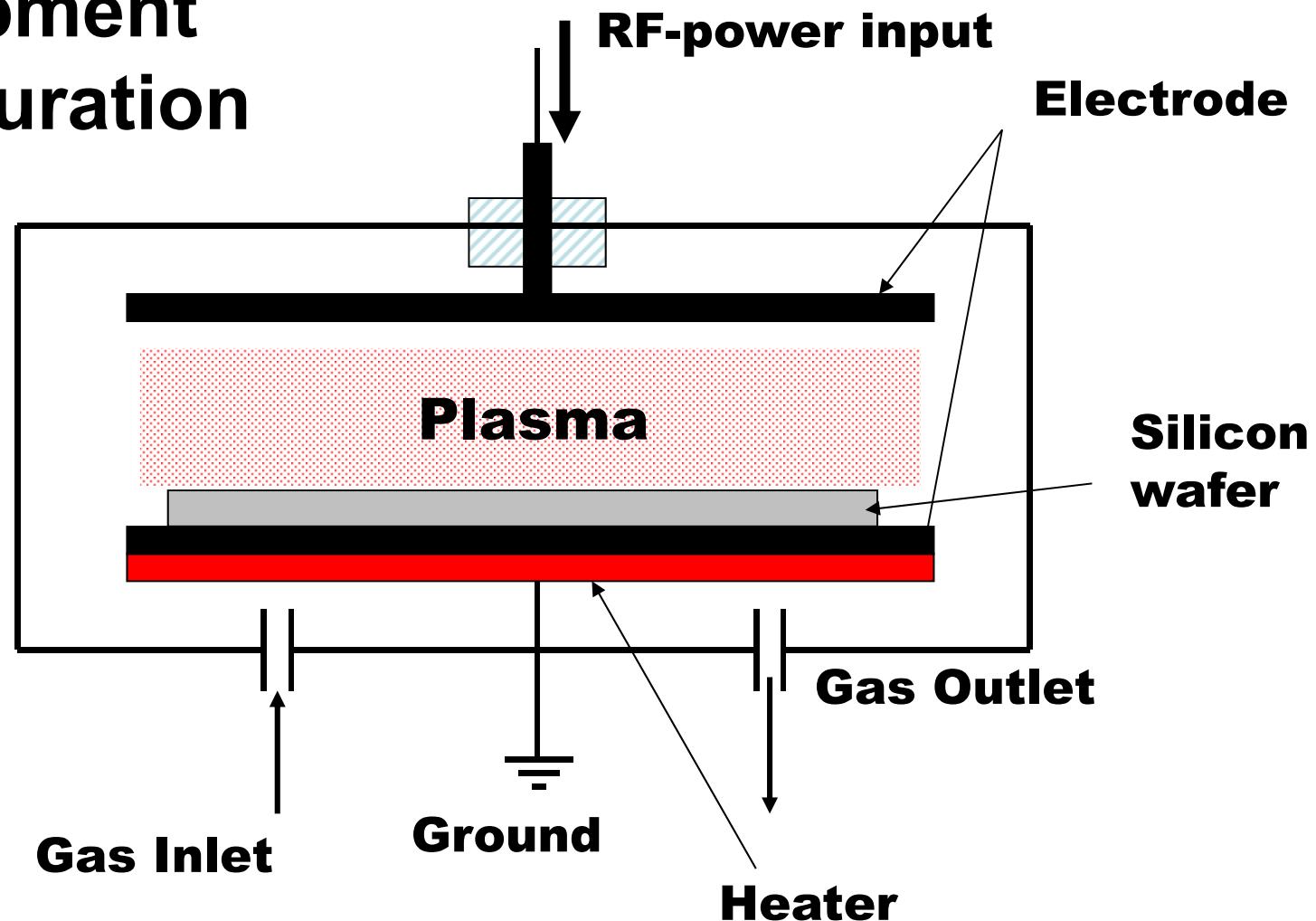
**A plasma is typically an ionized gas, and is usually considered to be a distinct phase of matter in contrast to solids, liquids, and gases because of its unique properties**

**“Ionized” means that at least one electron has been dissociated from a proportion of the atoms or molecules**

**The free electron charges make the plasma electrically conductive so that it responds strongly to electromagnetic fields**

# Typical PECVD (Plasma Enhanced CVD)

## Equipment Configuration



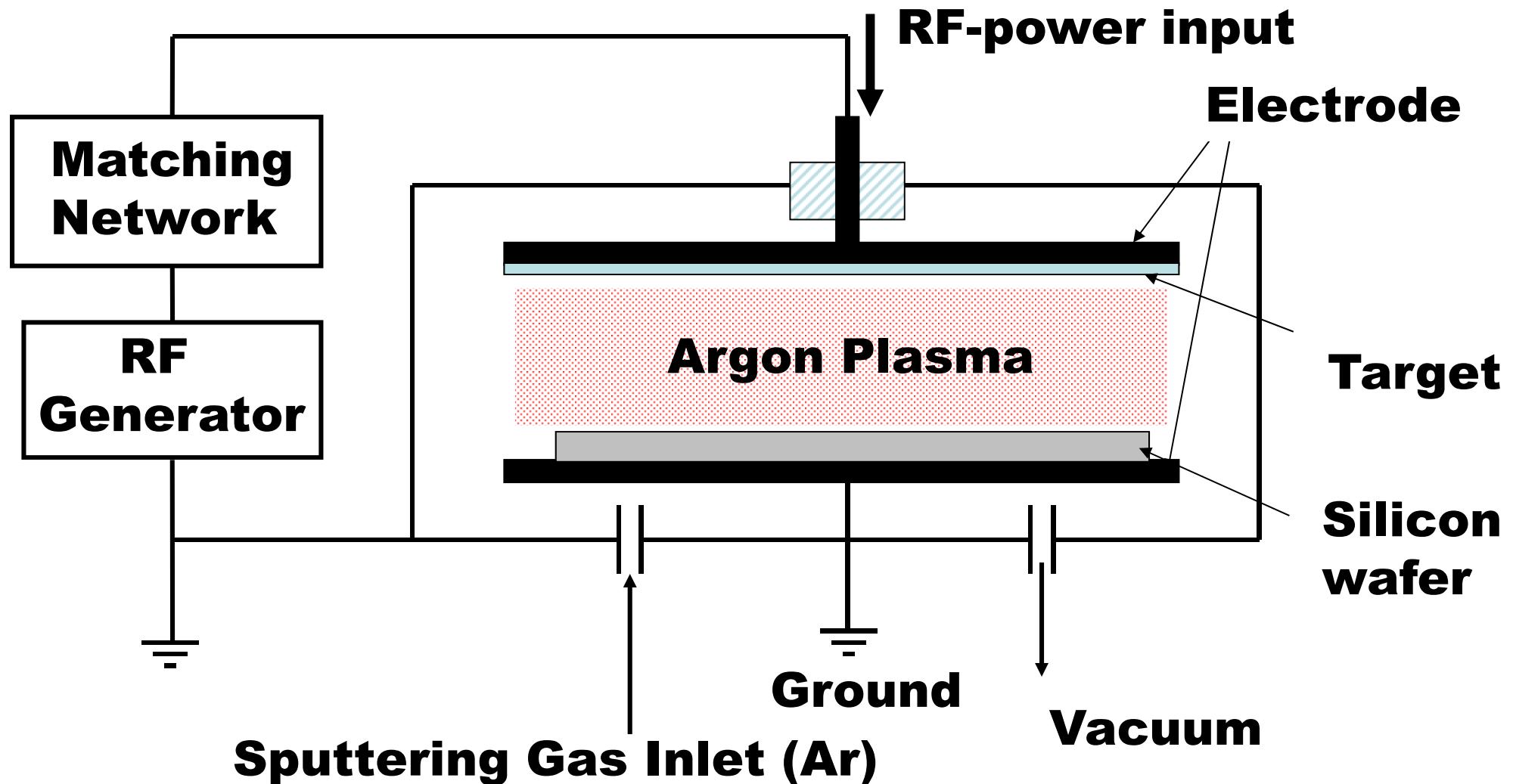
# Sputtering

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**Sputtering is a physical process whereby atoms in a solid target material are ejected into the gas phase due to bombardment of the material by energetic ions**

**It is commonly used for thin film deposition**

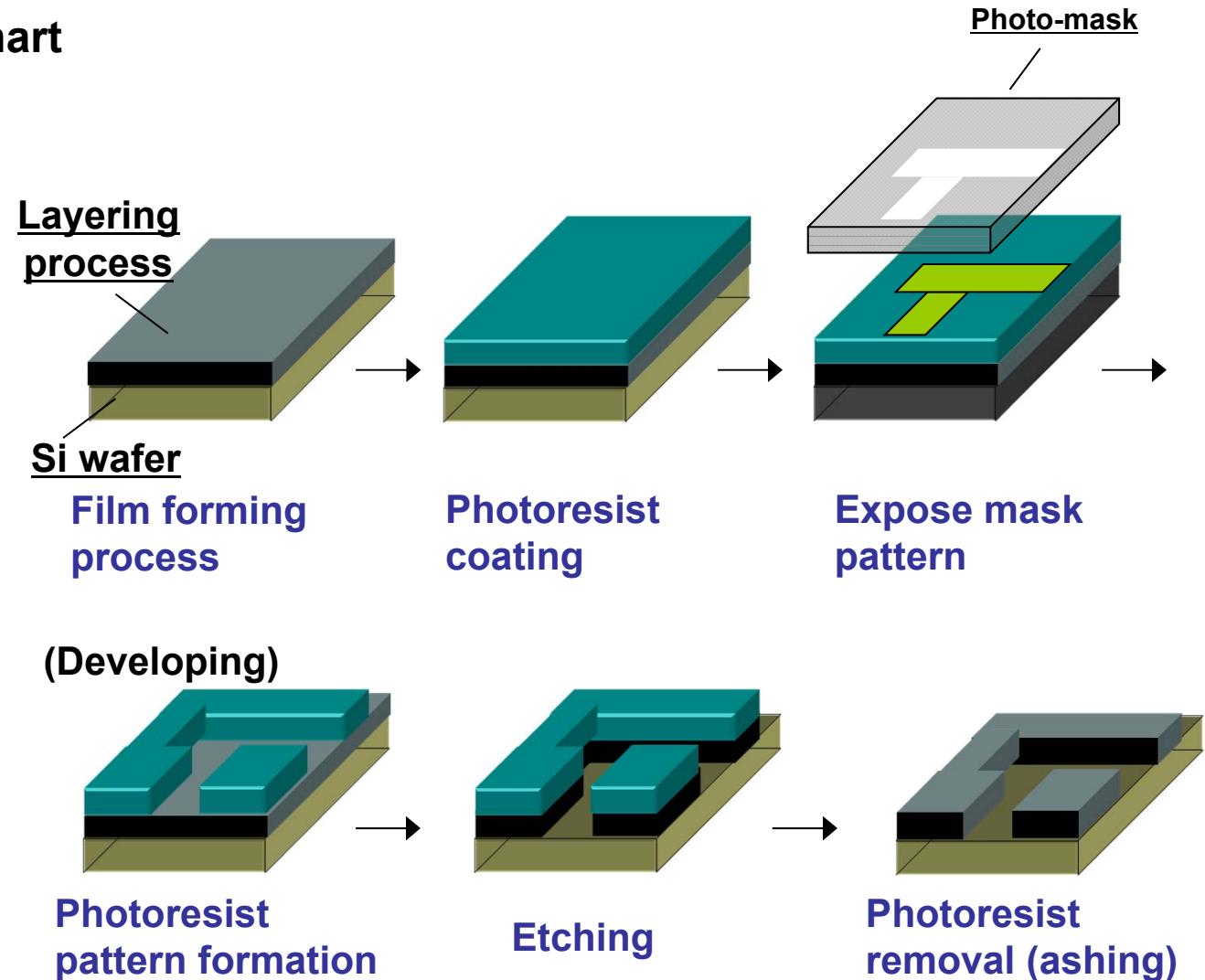
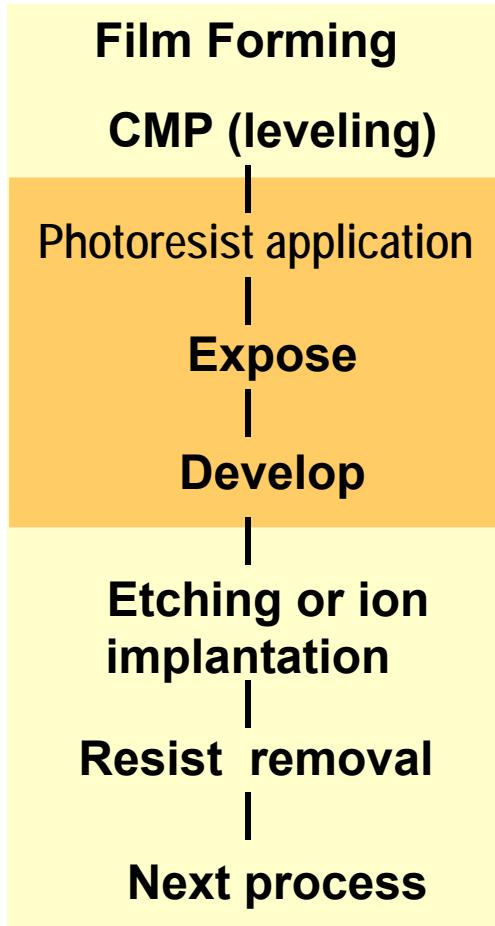
# Sputtering



# What is Lithography Technology?

This is a technology where semiconductor circuit patterns formed on photo-mask (mask) are repeatedly built on a wafer with high accuracy

Wafer process flow chart



# Photoresist

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**There are two types of photoresist, one is  
“positive (posi)” type resist and the other is  
“negative (nega)” type resist**

**When posi type resist is exposed and developed,  
the resist of exposed portion is dissolved and  
when nega type resist is exposed and developed,  
the exposed portion remains**

**We use posi type resist for fine patterning**

# Photoresist Coating

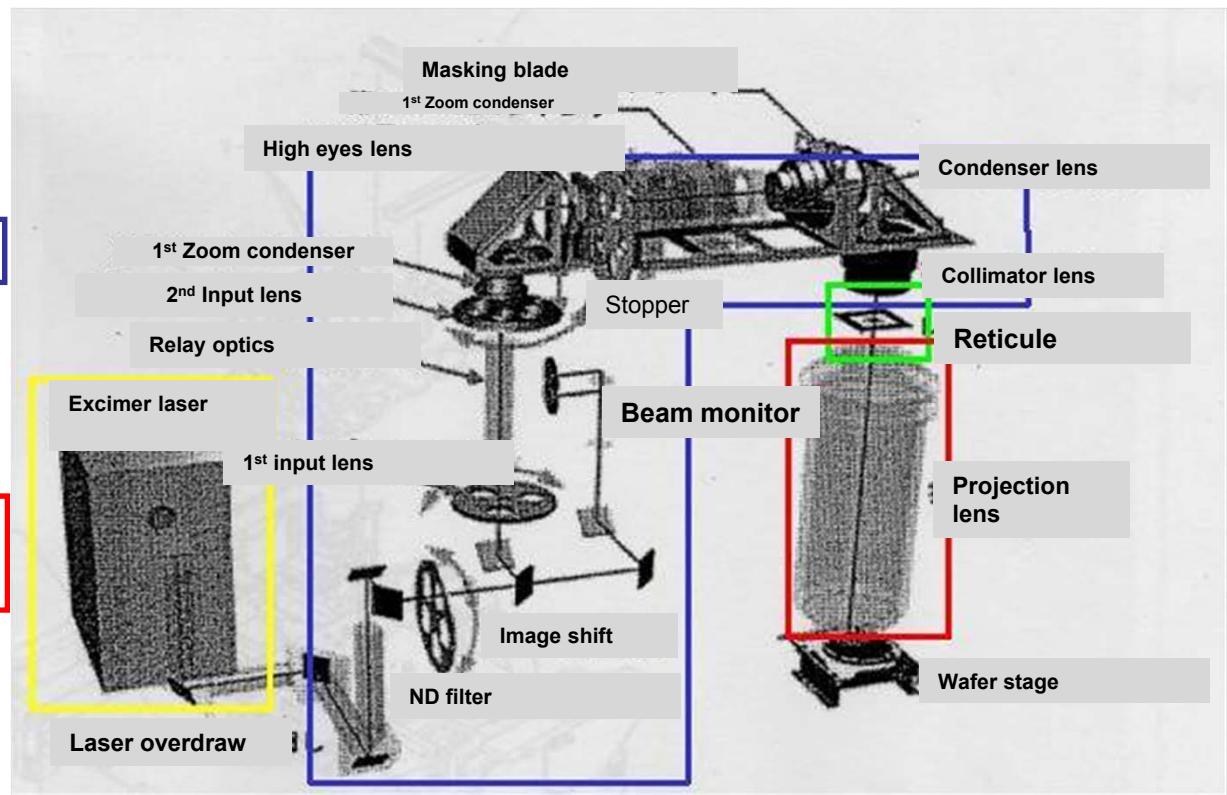
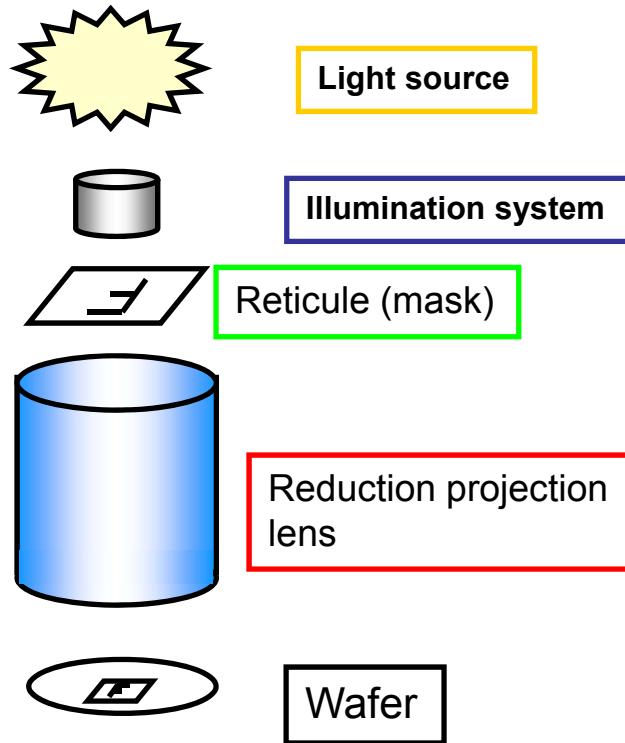


**Spin Coater**

**Photoresist is dropped on a wafer, then the wafer is spun to spread the resist**

**Photoresist is sensitive to a short wave length. So a light of longer wave length is used in the clean room**

# Photolithography Machine Formation



For example refer to Cannon KrF stepper FPA-3000EX6 illumination system

## Manufacturers

- Nikon
- Cannon
- ASML

### <Parameter related to exposure>

Light source	: Exposure wavelength
Illumination	: $\sigma$ , Variable illumination
Mask	: Phase shift mask, magnification

Reduction projection lens: NA, aberration

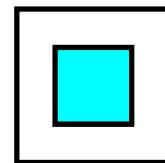
Wafer stage: X,Y, Z position, Positioning  
accuracy

# Types of Photolithography Machines - Stepper and Scanner

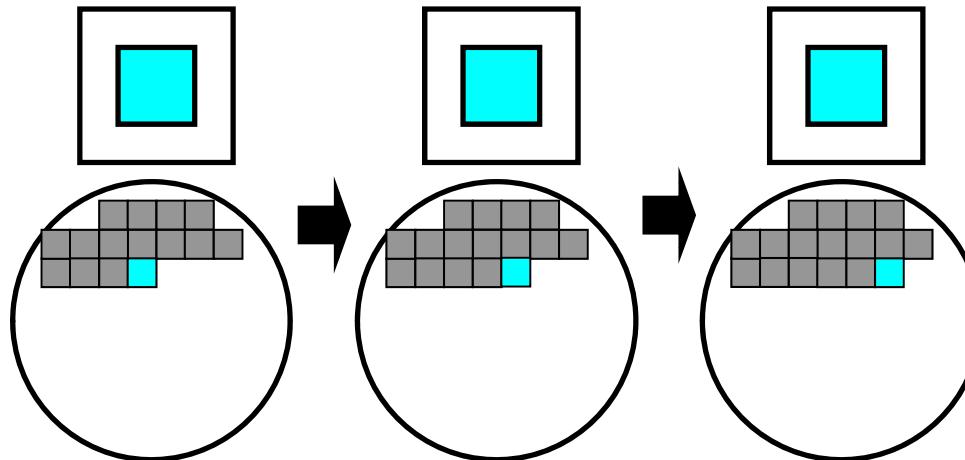
## Stepper

The target area for exposure (shot) is illuminated thoroughly and exposed entirely

Mask



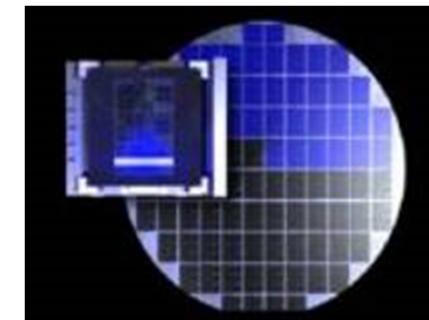
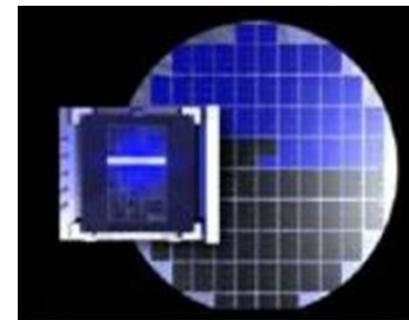
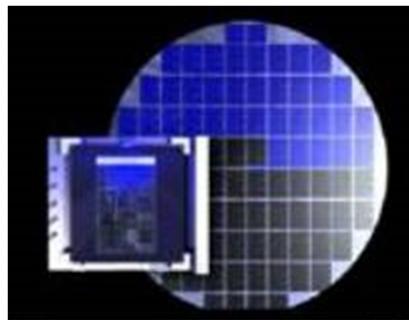
Wafer



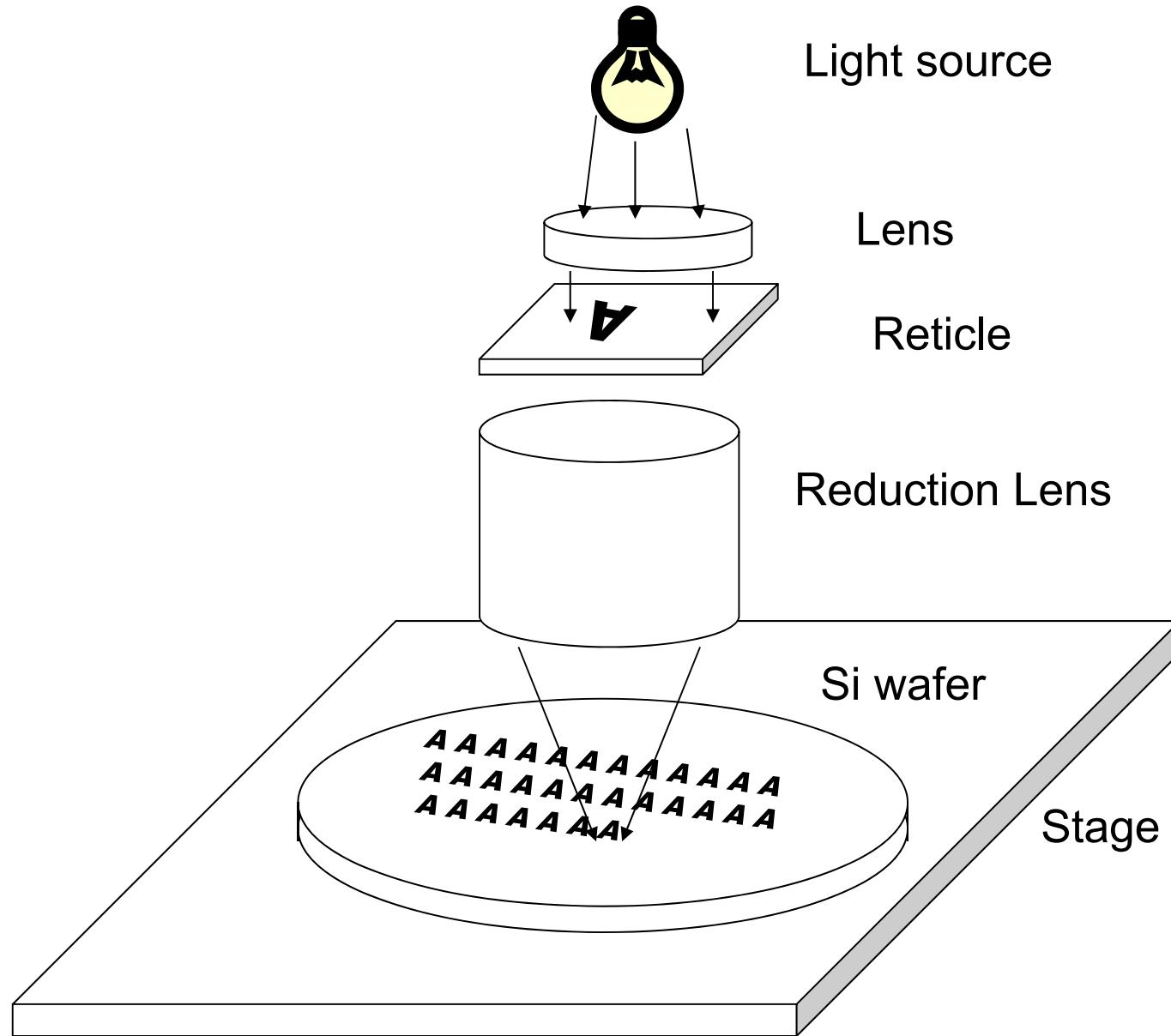
The area exposed to light

## Scanner

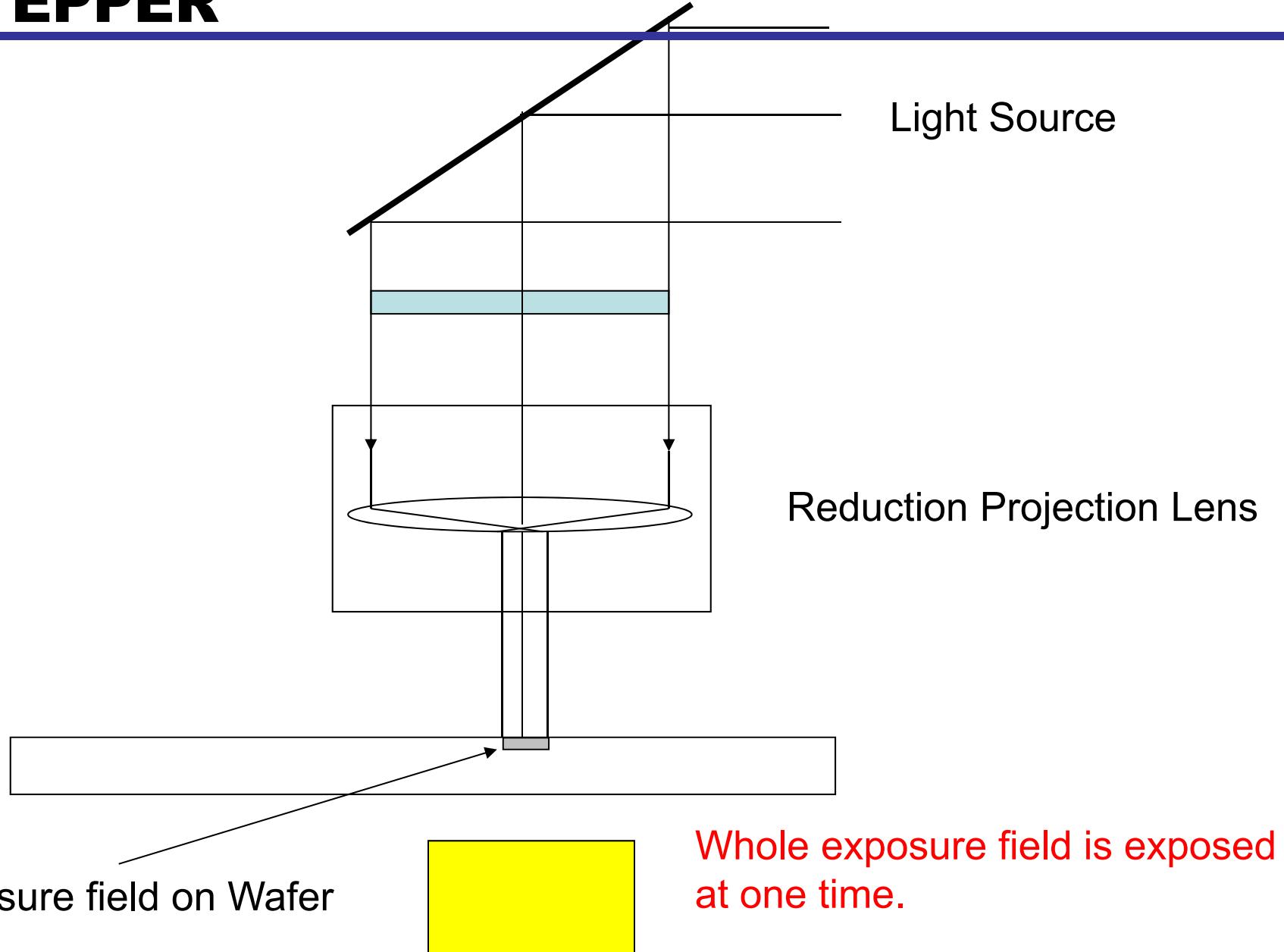
The target area for exposure (shot) is illuminated partially in the form of a slit, and exposed by synchronously scanning the reticule and the wafer stage.



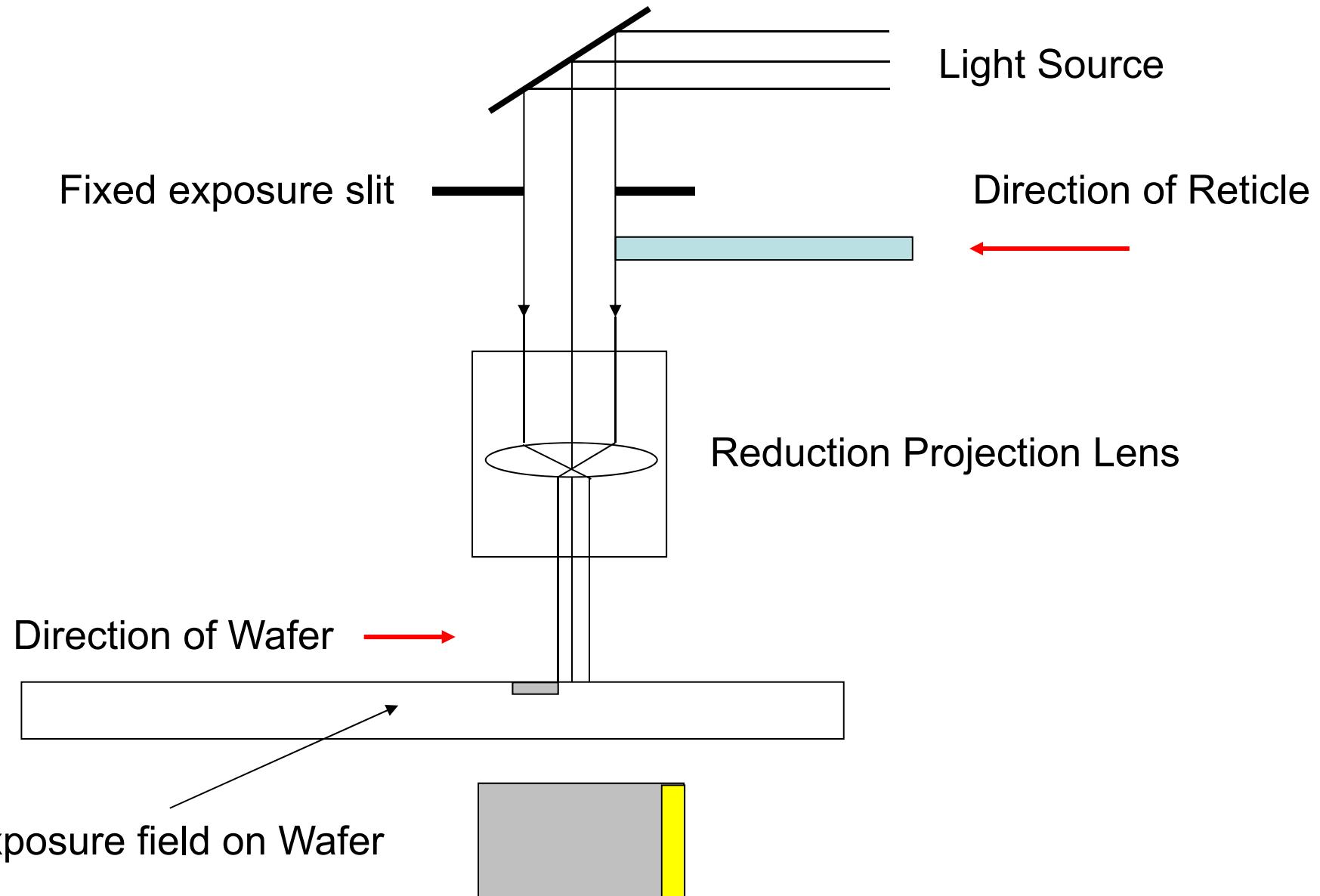
# Basic Principle of Patterning by Stepper and Scanner



# STEPPER



# SCANNER



# Dry Etching

Figure 1 Example of etching flow

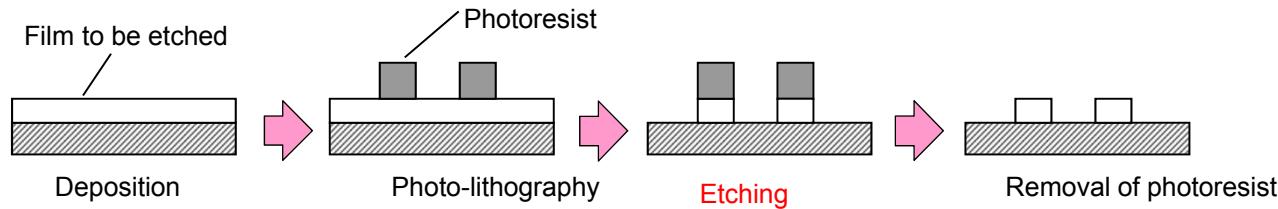


Table 1 Main processed film

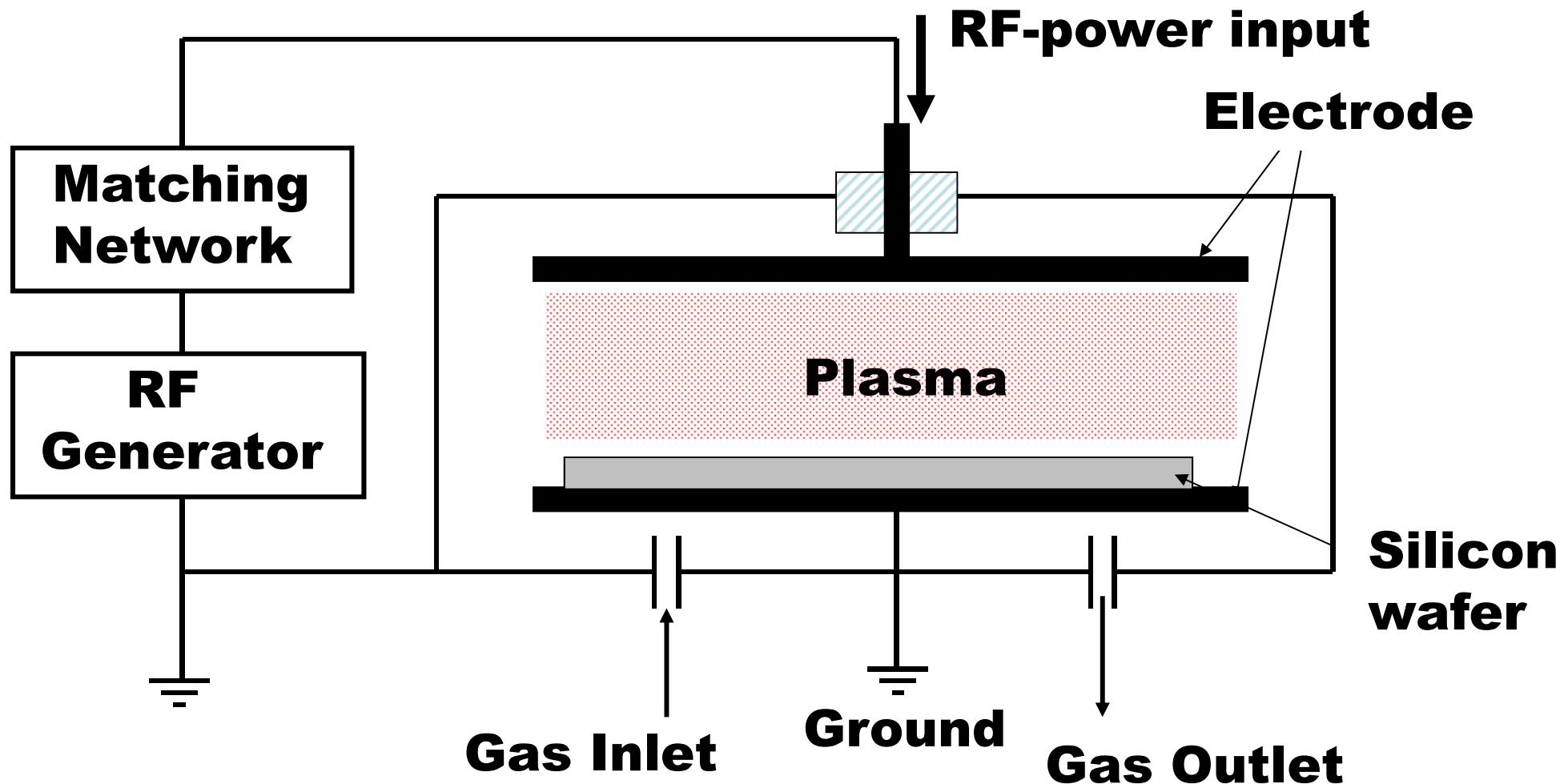
Insulation film	$\text{SiO}_2$ , $\text{Si}_3\text{N}_4$ , Low-k material
Wiring material	$\text{AlCu}$ , $\text{W}$ , $\text{WSi}_2$ , $\text{CoSi}$ , $\text{TiN}$ , poly - Si, Pt, Ru
High dielectric material	$\text{Ta}_2\text{O}_5$ , BST
Antireflection film	Organic ARC, InorganicARC (p-SiON, etc.)

BST: (Ba,Sr)  $\text{TiO}_3$   
ARC: Anti-Reflection Coating

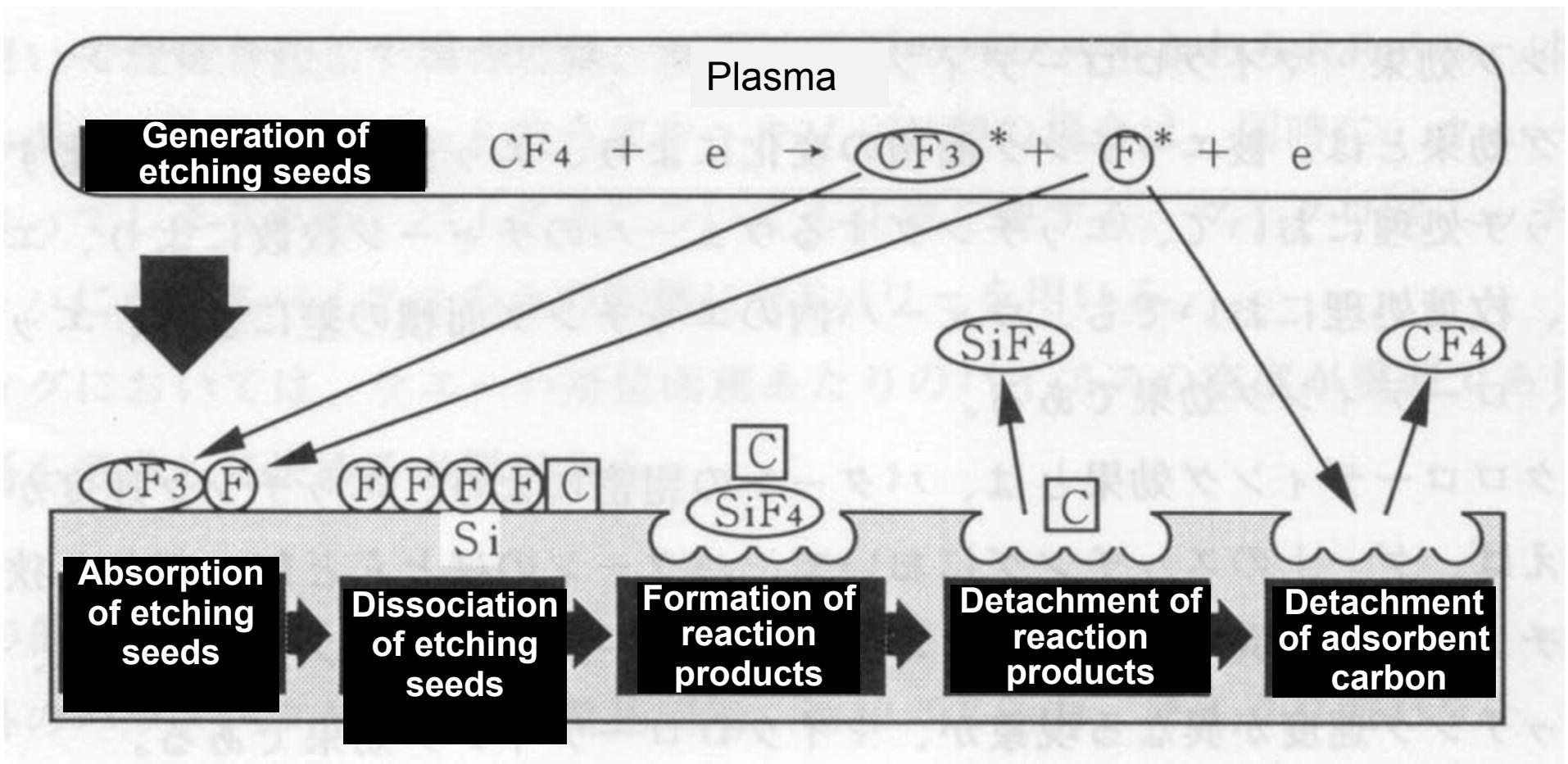
Figure 2 Cross-section of etching



# Schematic Diagram of an RF-powered Plasma Etching System



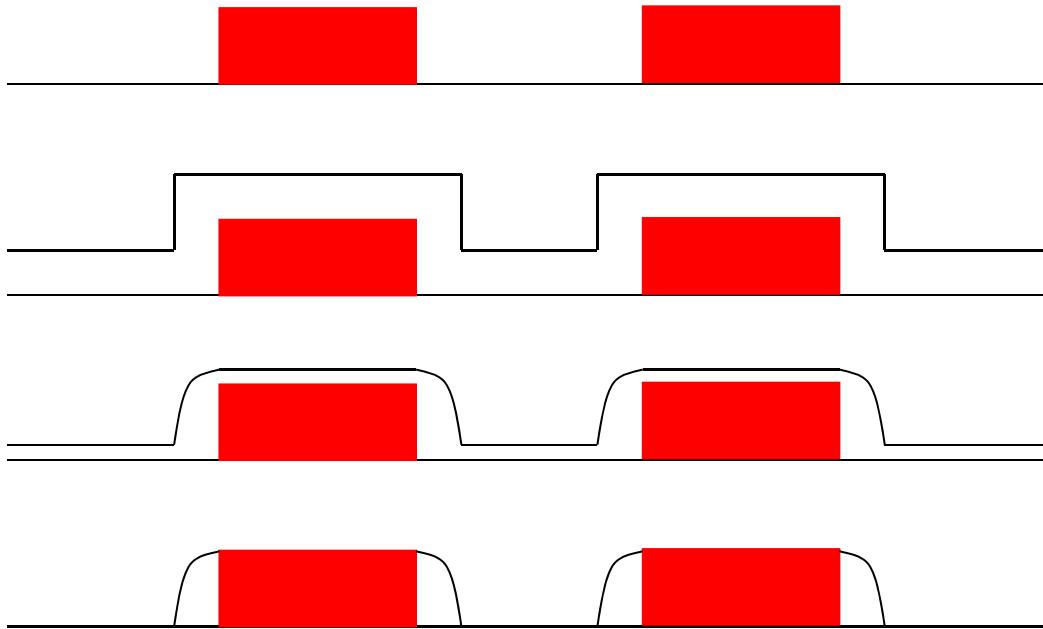
# Reaction During Dry Etching



\* is a radical: electrically neutral species that have incomplete bonding.

# Etch-back process

After oxide is deposited, and without any mask, oxide is etched using anisotropic dry etching. Oxide at the steps remains un-etched



Oxide deposition  
Deposition is isotropic.

Anisotropic dry etching

# Plasma Ashing

---

**In semiconductor manufacturing plasma ashing is the process of removing the photoresist from an etched wafer**

**Using a plasma source, a monatomic (single atom) reactive species is generated. Oxygen or fluorine are the most common reactive species**

**The reactive species combines with the photoresist to form ash which is removed with a vacuum pump**

**Typically, monatomic (single atom) oxygen plasma is created by exposing oxygen gas ( $O_2$ ) to ionizing radiation**

# Ion Implantation

**Ion implantation is used to alter the surface properties of semiconductor materials by doping the desired elements on the semiconductor substrate, or in the thin film on the substrate**

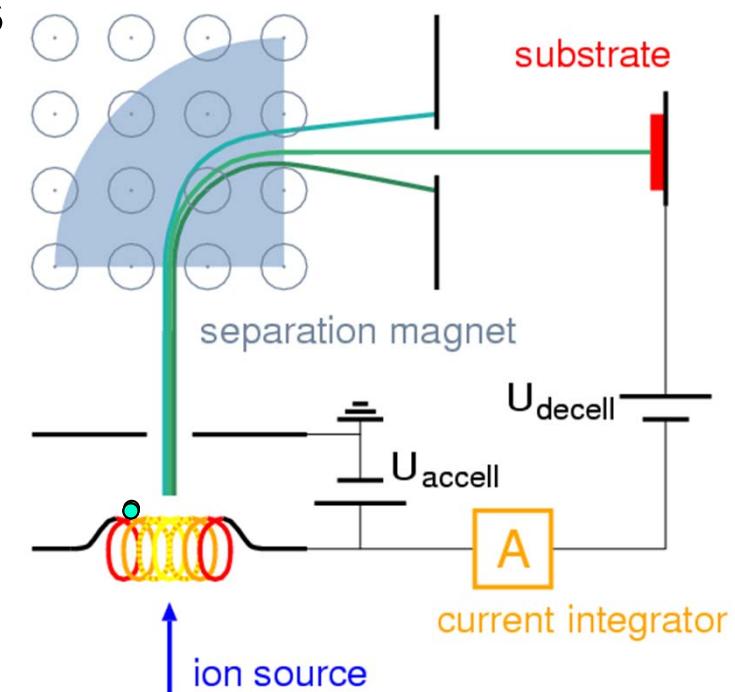
**PN junction is formed or surface properties are controlled by thermal treatment, recovery of dislocated crystal or implanted impurity atoms are substituted at the lattice point and activated electrically (Anneal)**

## **(Usage)**

- **Well formation**
- **Isolation between devices**
- **Source/Drain formation**

## **(Requirement from device)**

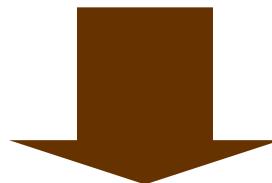
- **Shallow junction formation**



# Features of Ion Implantation

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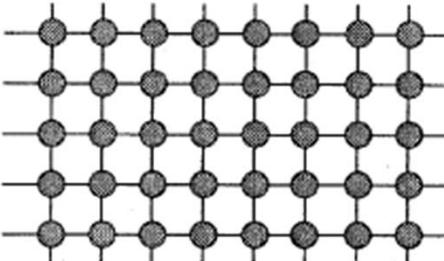
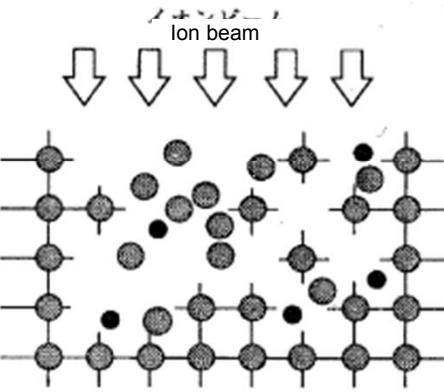
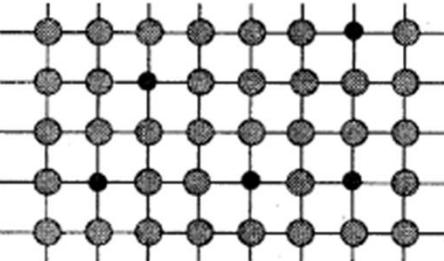
- **Can highly control the concentration and implantation depth**
- **Photoresist can be used as a mask for a selective implantation (Room temperature process)**
- **Can dope at low concentration**



**Conventional impurity doping technology such as thermal diffusion has replaced with ion implantation**

# Defect Recovery and Dopant Activation by Thermal Process

- Energy from thermal treatment can recover crystallinity
- Rapid thermal processes are adopted to LSI fabrication process  
( ex. 1000 °C, 30sec )

Process flow	Alignment model of Si atom	Description
Before implantation		Si atoms are aligned & bonded. However, only Si atoms may allow a small current to pass.
After implantation	 <p>Ion beam</p>	<p>Due to ion Implantation, dopant and Si atoms collide, alignment is disturbed (defect occurred), and the covalent bonds break.</p> <p>In this case, implanted ions are not bonded to Si atoms, but is in between Si atoms. (Interstitial atom)</p> <p>In this condition, a current does not flow even though dopant ion exists. (Inactive condition)</p>
After annealing		By annealing, the alignment of Si atoms is recovered, and ions also get bond to Si. Therefore a current can flow. (Ion activation)

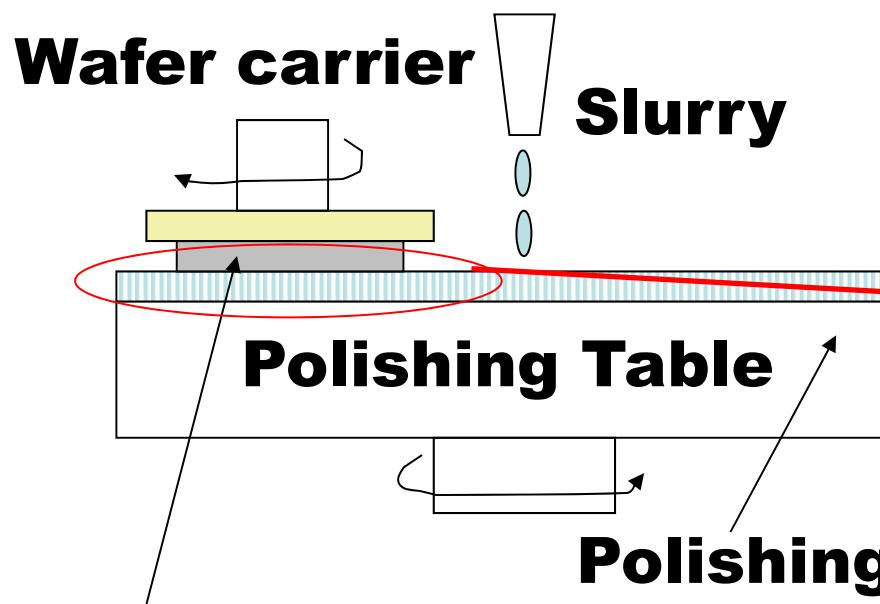
# **Purpose of Annealing**

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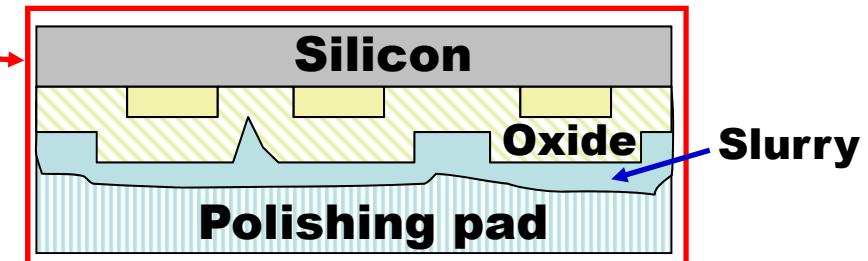
**Annealing is done for the purpose of**

- 1. Damage relaxation from the bombardment of impurity**
- 2. Activation of doped impurity**
- 3. Diffusion of doped impurity**

# CMP – Chemical Mechanical Polishing



**Close-up of  
wafer/pad interface**



**Wafer (facing down)**

**Slurry: An abrasive substance**

# **LSI Wafer Process**

**- An Example: 90nm SoC**

# Module Processes

## A) Cleaning



## B) Thin Film formation



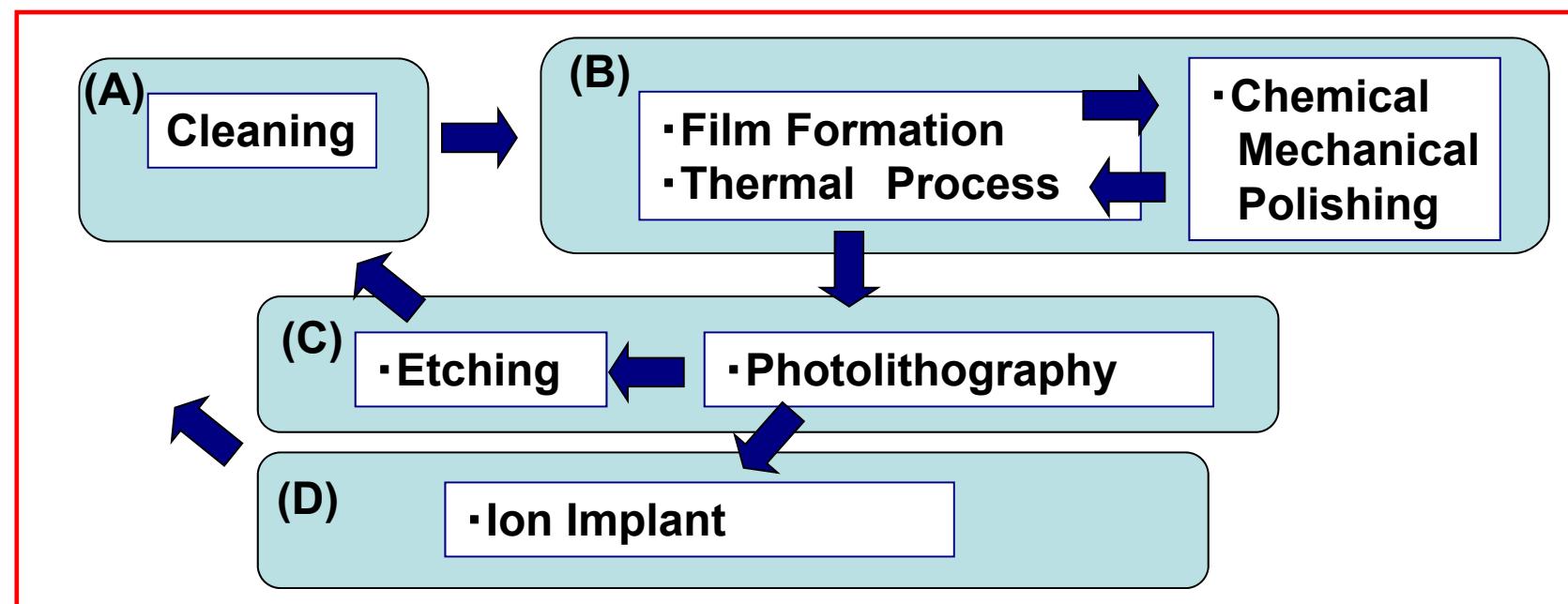
## C) Patterning - Photo lithography



## D) Doping



more detailed



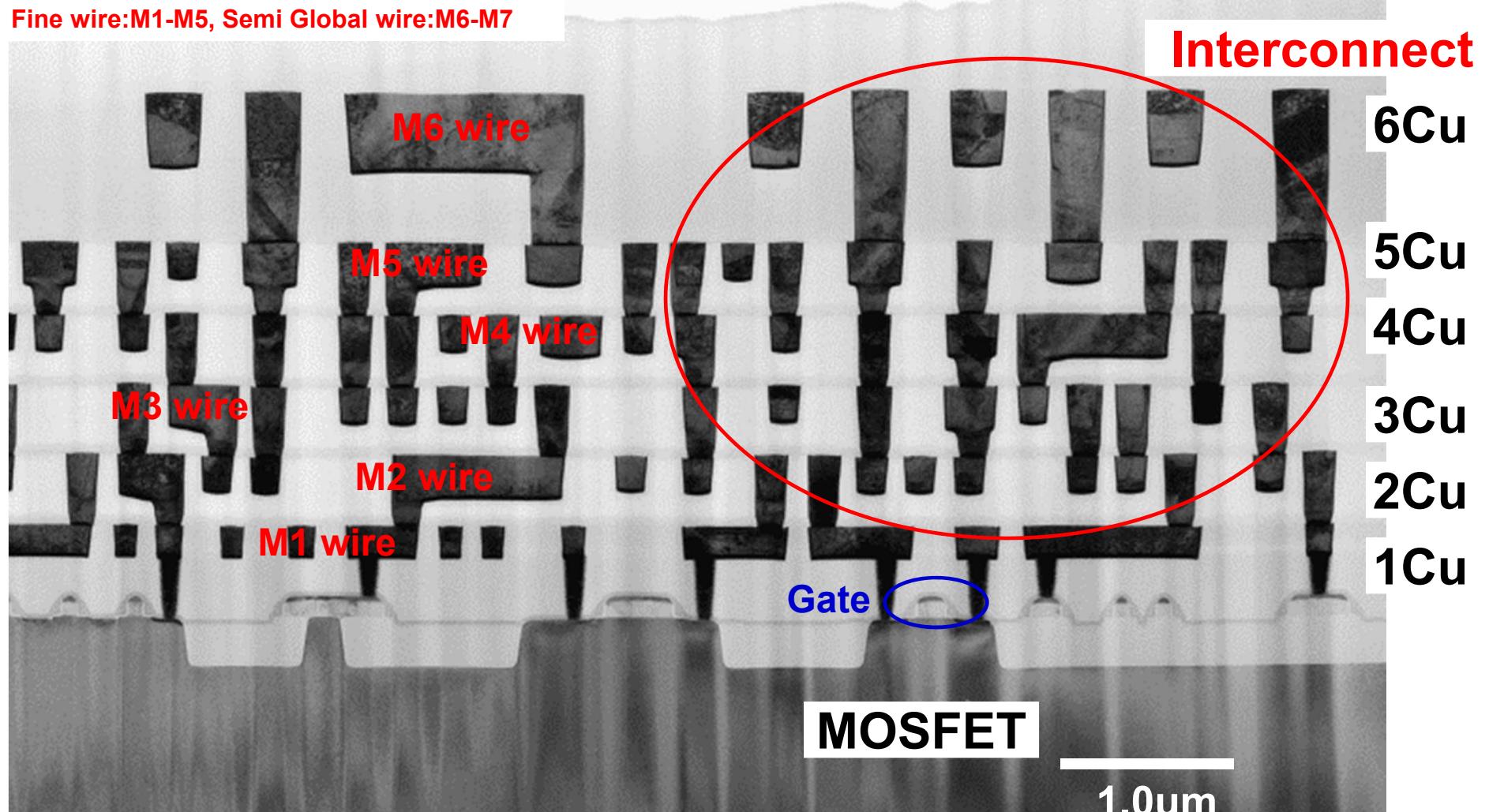
# **Example of Wafer Process**

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**Followings are simplified wafer process based on  
Renesas 90nm technology.**

# LSI Final Cross-section

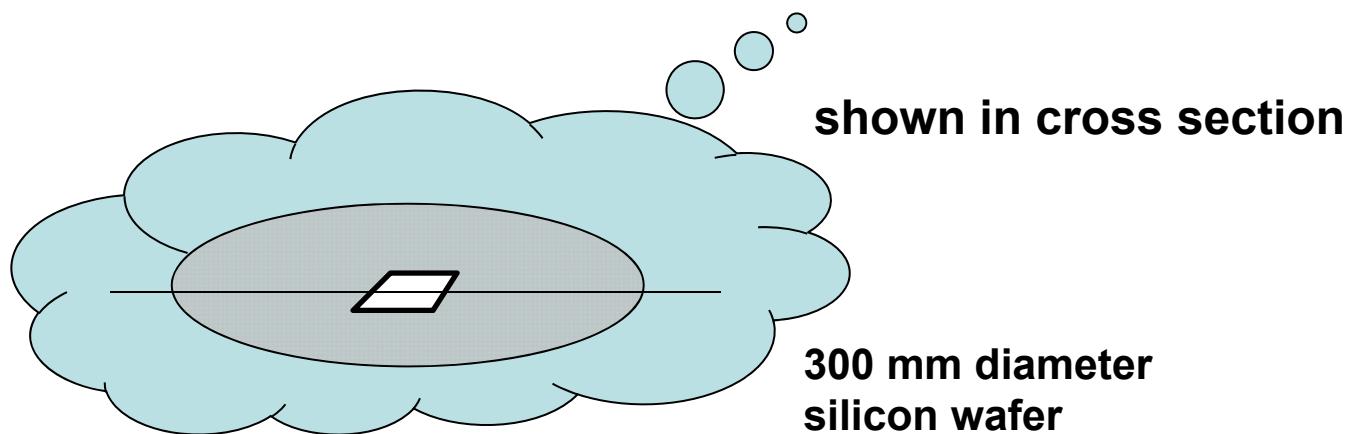
Cross-section SEM photograph of RC03 Product Application (6 layers Cu metal wire)



# Preparation of P-type Silicon Substrate

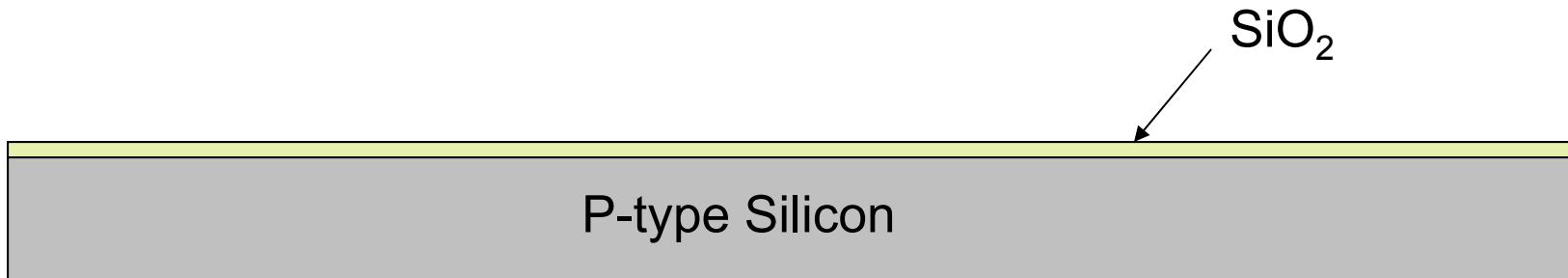
Starting material is **P-type Silicon** wafer.

P-type Silicon



## Formation of Silicon Oxide

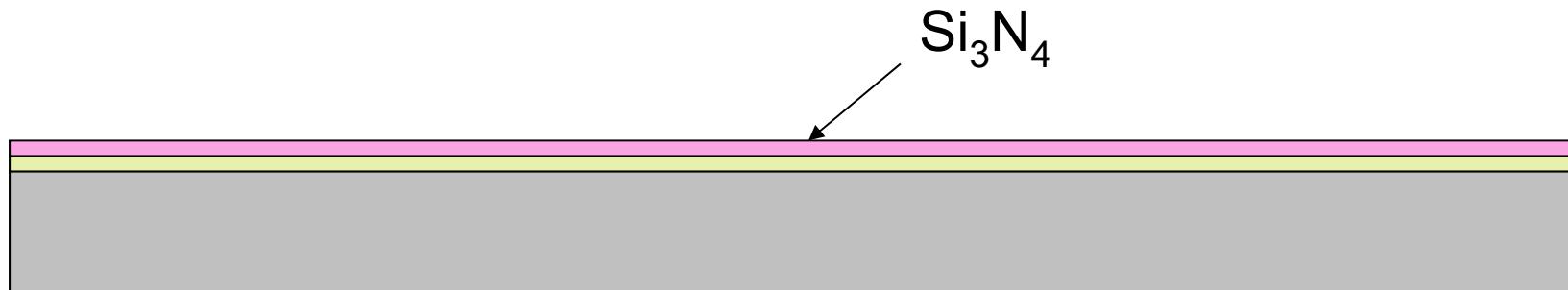
Thermal silicon oxide will be formed.



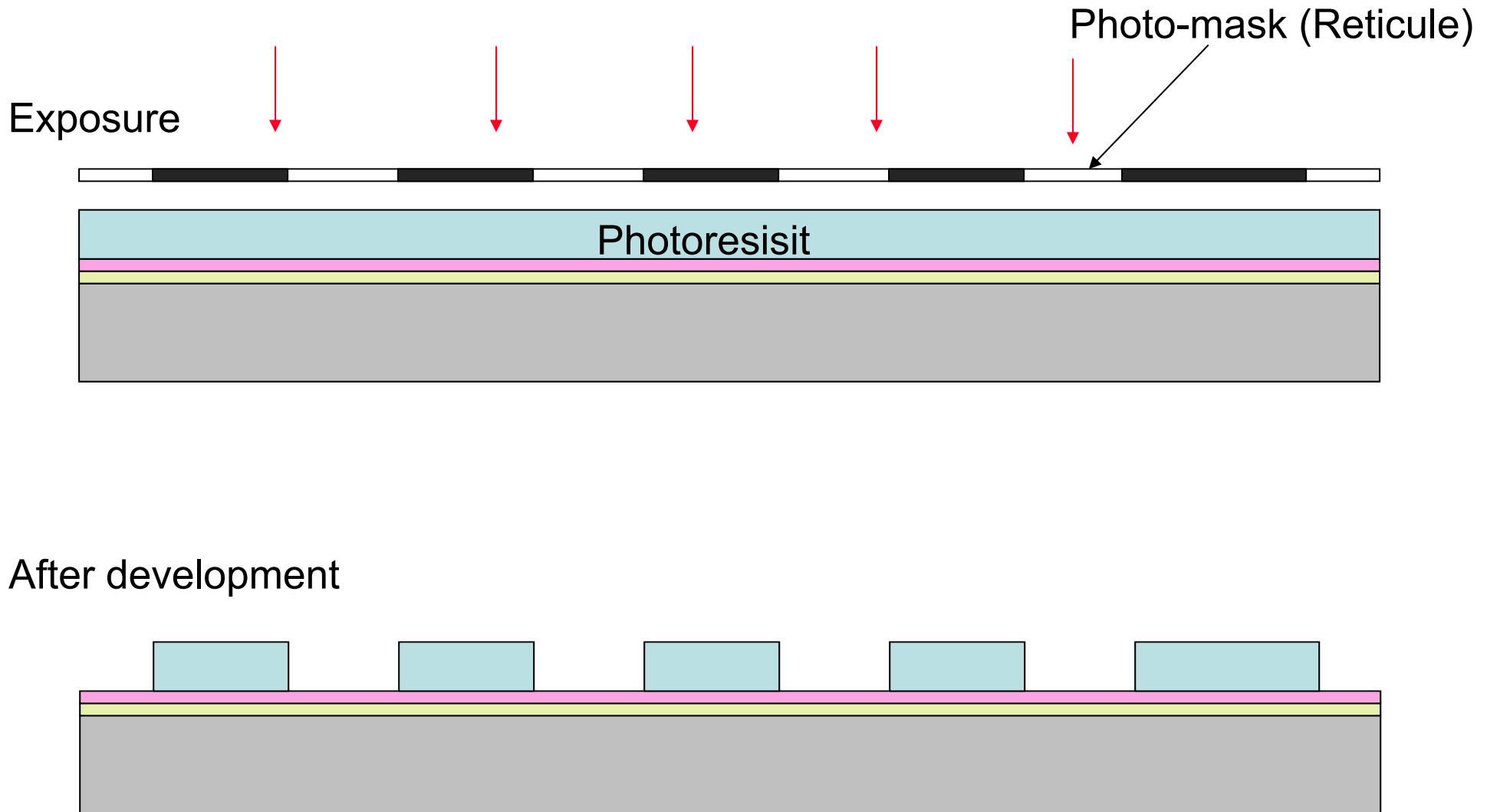
This oxide is used to relax the stress from the upper deposited layer.

## Deposition (Formation) of $\text{Si}_3\text{N}_4$

$\text{Si}_3\text{N}_4$  (P-SiN) will be deposited on  $\text{SiO}_2$  by using plasma enhanced CVD.



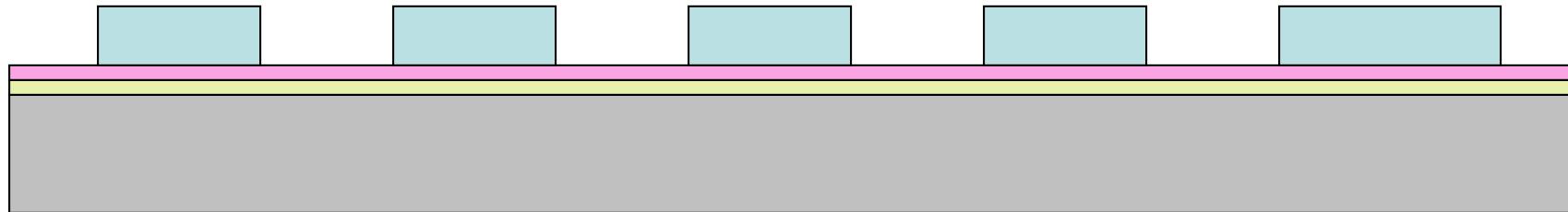
# STI Photo



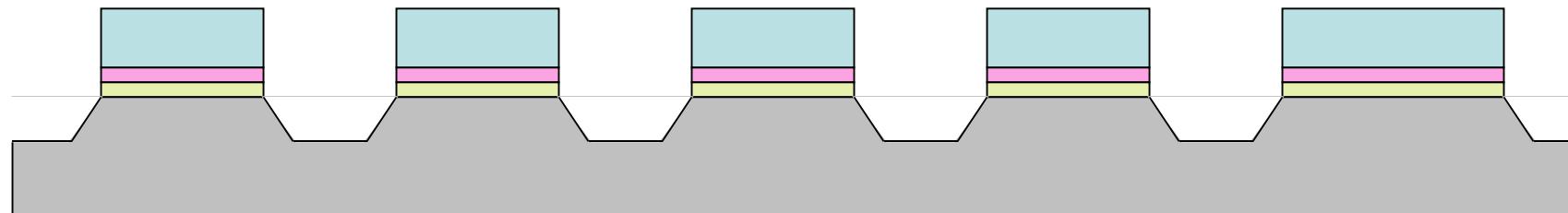
# Etching

$\text{Si}_3\text{N}_4$ ,  $\text{SiO}_2$  and Silicon substrate are etched using plasma enhanced dry etching

Before etching



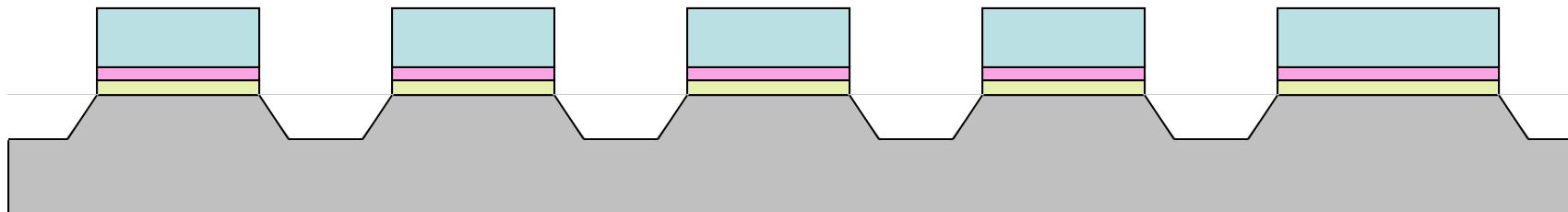
After etching



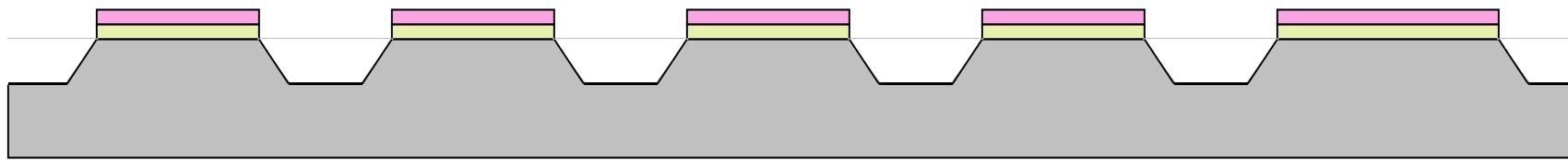
# Photoresist Removal (Ashing)

Photoresist is removed by using plasma ashing and acid cleaning.  
Now,  $\text{Si}_3\text{N}_4$  is used as a masking material for oxidation.

Before ashing

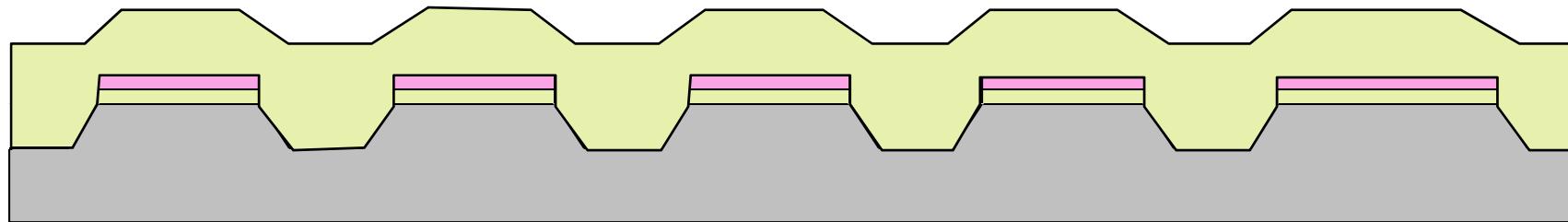


After ashing



# STI Oxidation and HDP Deposition

Oxidation of thin oxide formation and deposition of HDP-Oxide is done  
(HDP: high density plasma)

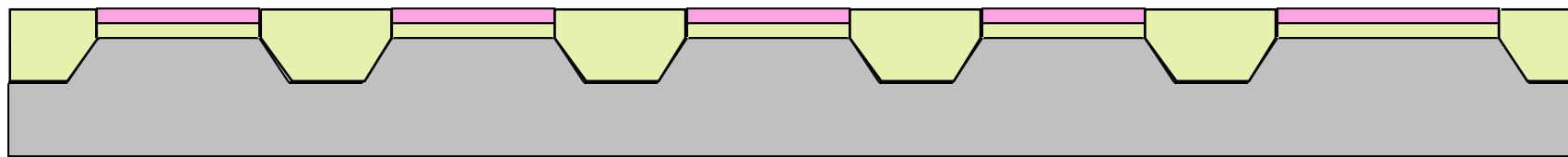


To densify HDP oxide, wafers are annealed

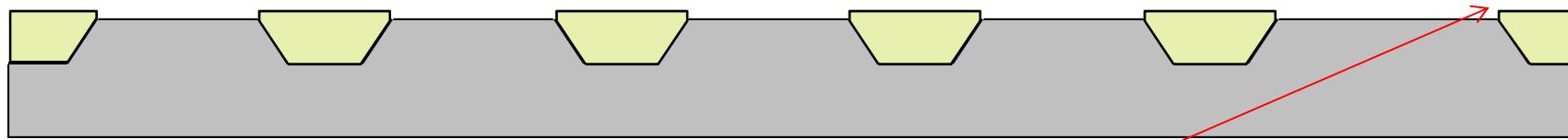
# CMP

**CMP: Chemical Mechanical Planarization or Chem. Mech. Polishing** is a technique used in semiconductor fabrication for planarizing the top surface of an in-process semiconductor wafer or other substrate

After CMP



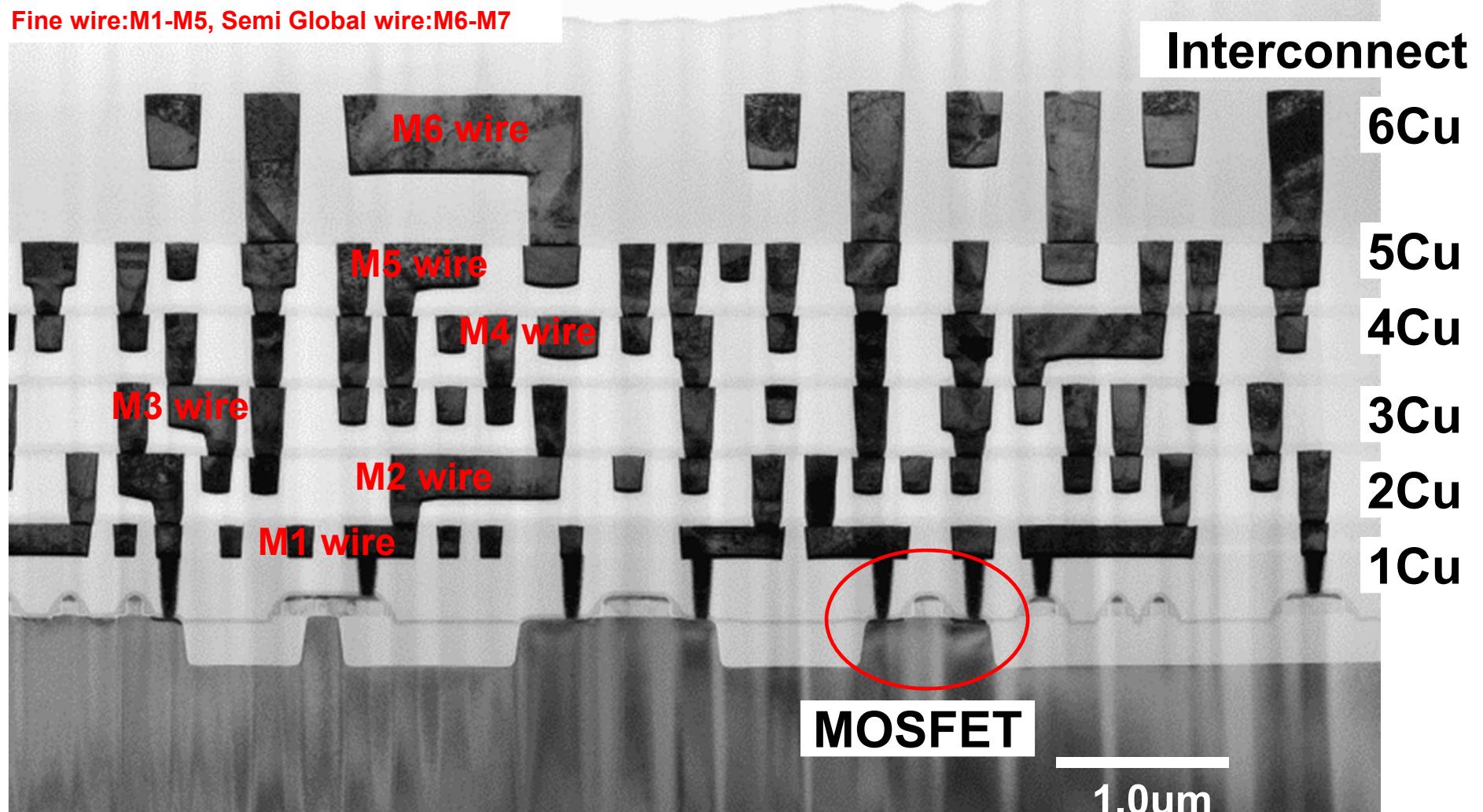
After STI etch back and Si<sub>3</sub>N<sub>4</sub> etching



To simplify the drawing, STI will be drawn as flat!

# L S I Final Cross-section

Cross-section SEM photograph of RC03 Product Application (6 layers Cu metal wire)



# Implantation for MOSFET $V_{th}$ Control (1)

In NMOS, if more acceptor ion is implanted to P-Well, then  $|V_{th}|$  of NMOS is increased

In PMOS, if more donor ion is implanted to N-Well, then  $|V_{th}|$  of PMOS is increased

Refer to “MOSFET” lecture:

$$\text{Threshold Voltage } V_{th} = \frac{\sqrt{2 \epsilon q N \phi}}{C_{ox}} + V_{fb}$$

N is controlled by ion implantation

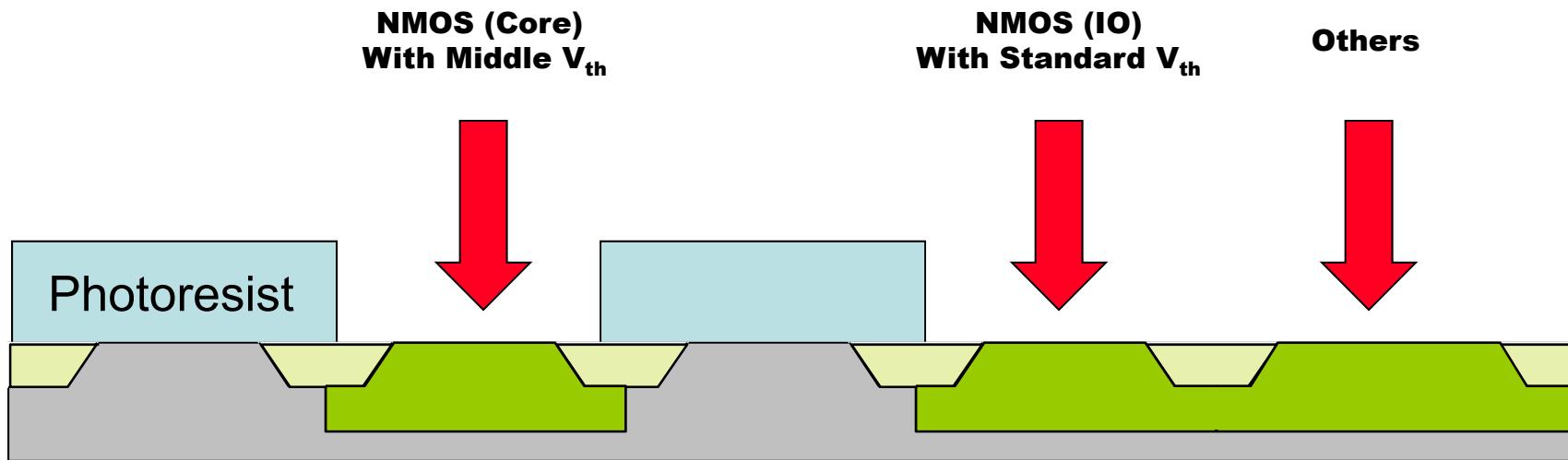
C<sub>ox</sub> is controlled by gate oxide thickness

N: DONOR or ACCEPTOR concentration  
ε : dielectric constant of Si  
q: elementary charge  
C<sub>ox</sub>: gate oxide capacitance  
 $\phi = 2\phi b = kT \ln(N/n_i)$

## P-WELL Formation and $V_{th}$ Control - NMOS

P-WELL photolithography is done and P-WELL implantation is done

Now by using the same resist mask,  $V_{th}$  control implantation for middle  $V_{th}$  of NMOS (Core) and standard  $V_{th}$  of NMOS (IO) is also performed



Core means devices using 1.0~1.2V used for logic circuit and memory

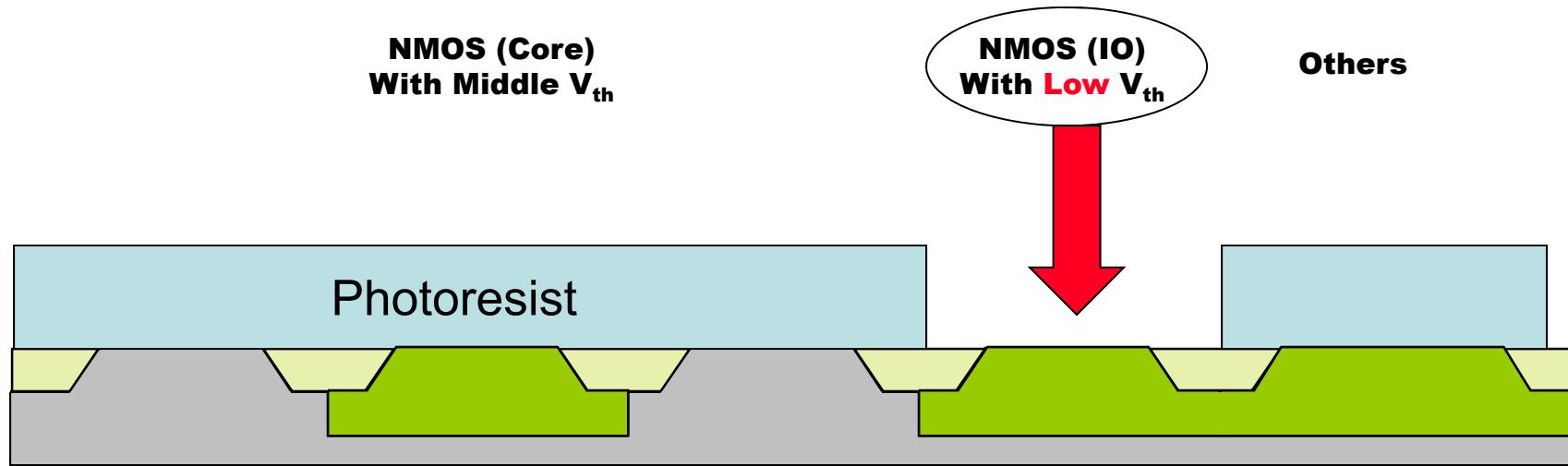
IO means devices using for IO pads which have thicker gate oxide than core devices to support higher power supply (2.5~3.3V)

# Implantation for MOSFET $V_{th}$ Control (2)

We support multi  $V_{th}$  for enhanced device capability

For IO devices: low and standard  $V_{th}$  are supported

For core devices: low, middle and high  $V_{th}$  are supported

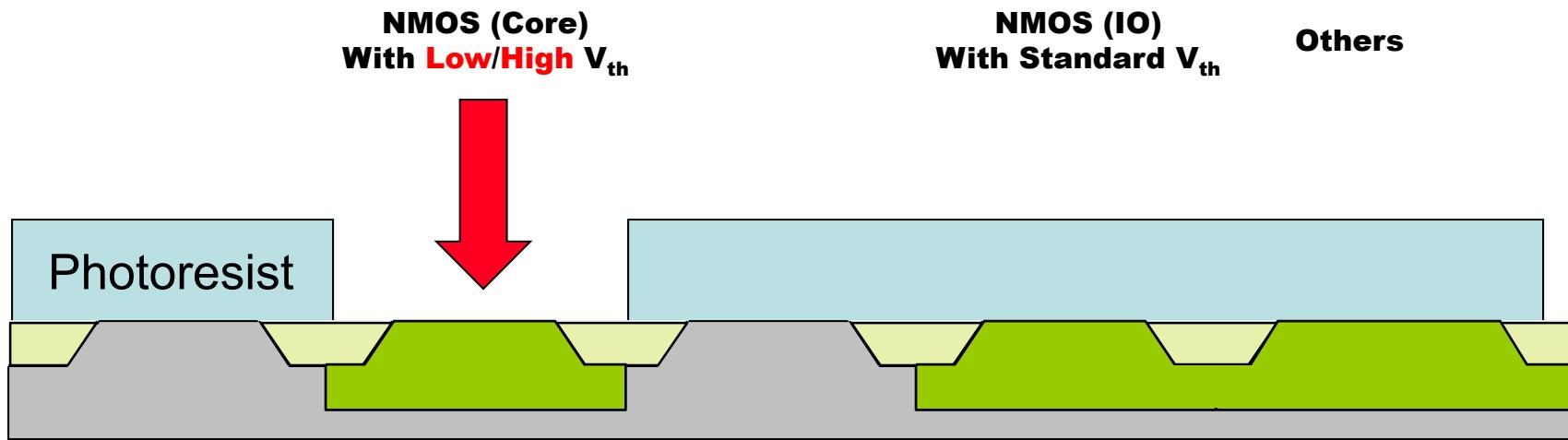


If the implantation for NMOS IO with Low  $V_{th}$  is done, NMOS IO with Standard  $V_{th}$  turns to Low  $V_{th}$ .

Quiz: Which dopant is implanted? And why?

# Implantation for MOSFET $V_{th}$ Control (3)

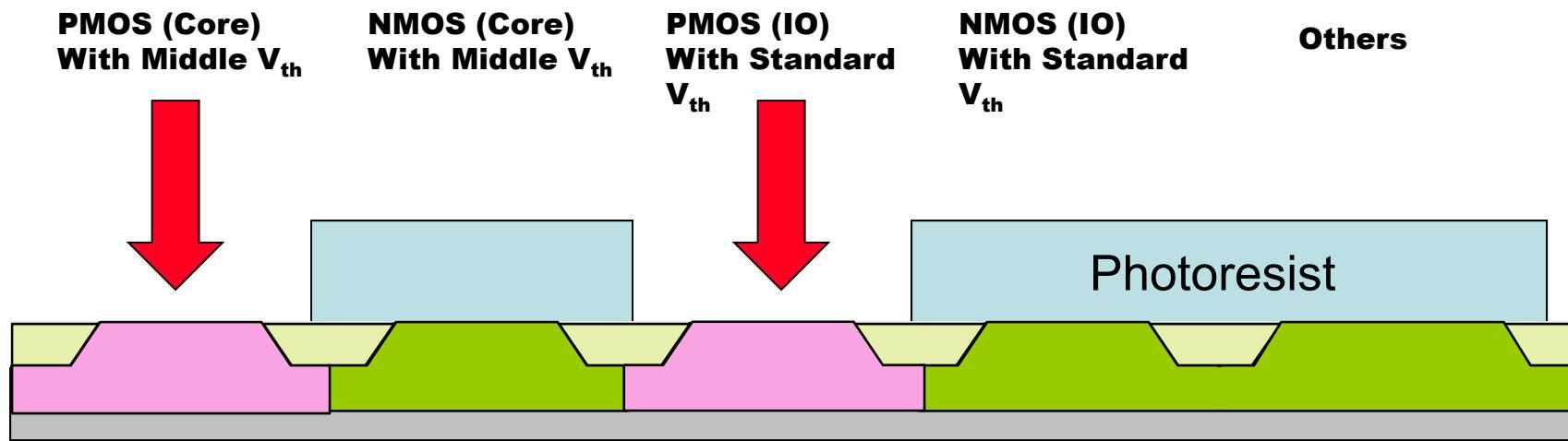
Same to IO devices, the implantation to core devices can change  $V_{th}$



## N-WELL Formation and $V_{th}$ Control - PMOS

N-WELL photolithography is done and N-WELL implantation is done

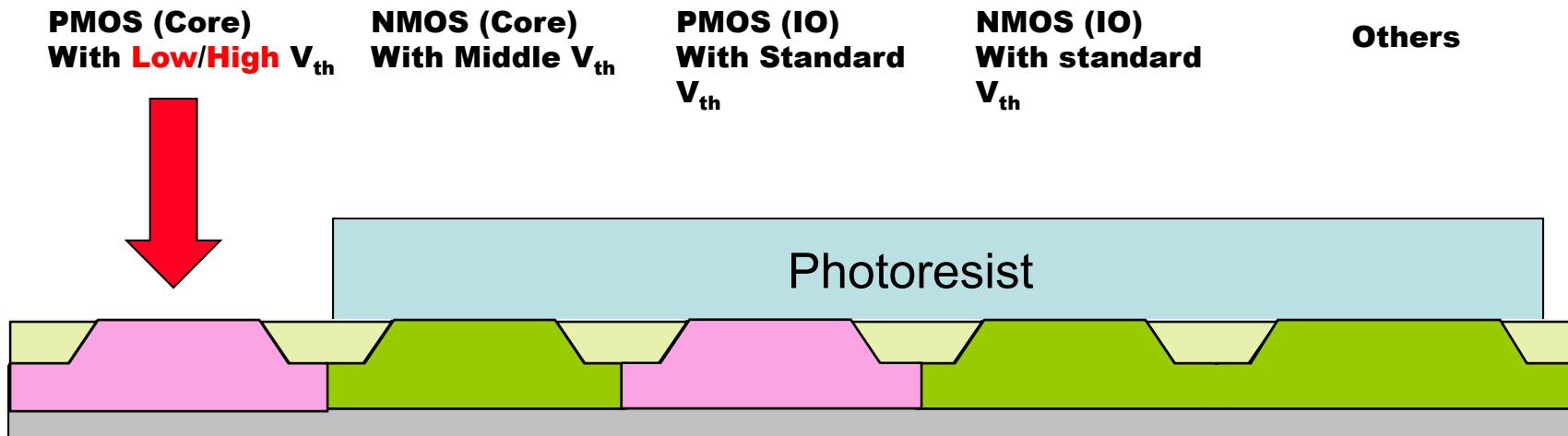
Now by using the same resist mask,  $V_{th}$  control implantation for middle  $V_{th}$  of PMOS (Core) and standard  $V_{th}$  of PMOS (IO) is also performed



**The starting material is P-type silicon, so the dosage of N-WELL implantation is very high to change P-type to N-Type**

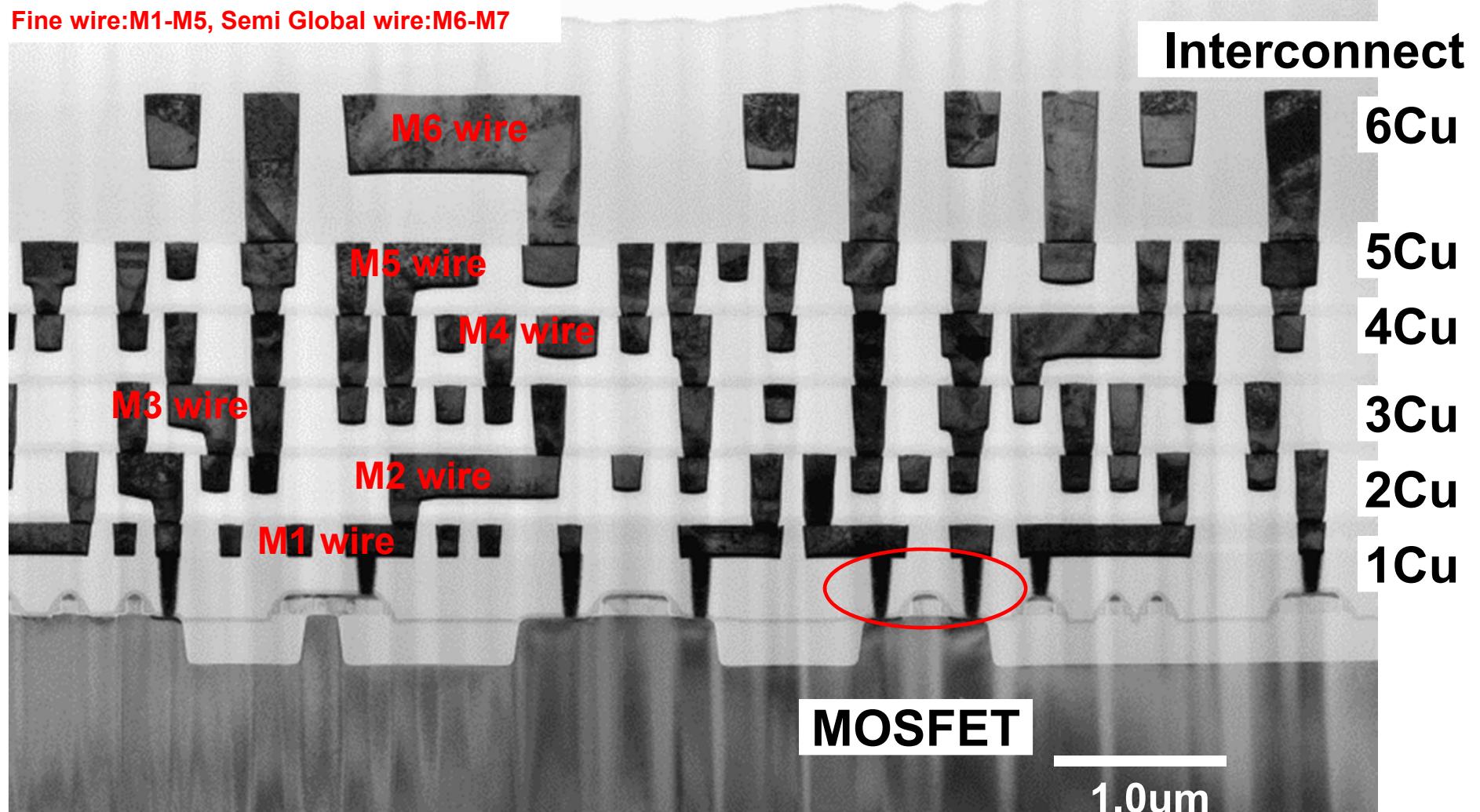
# Implantation for MOSFET $V_{th}$ Control (4)

The implantation to core devices can change  $V_{th}$



# L S I Final Cross-section

Cross-section SEM photograph of RC03 Product Application (6 layers Cu metal wire)



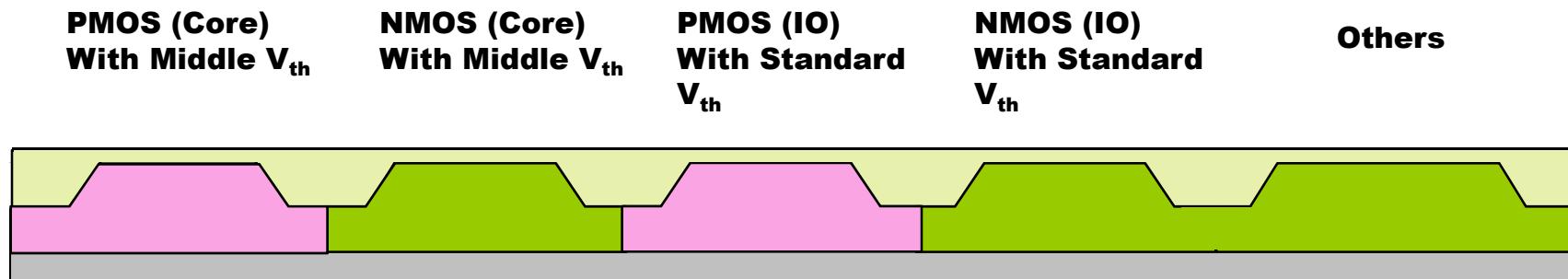
# Gate Oxide Formation (1)

Since core devices and IO devices use gate oxide of different thickness, there is a photolithography to form **dual gate oxide**

Before gate oxidation, WELL annealing is done

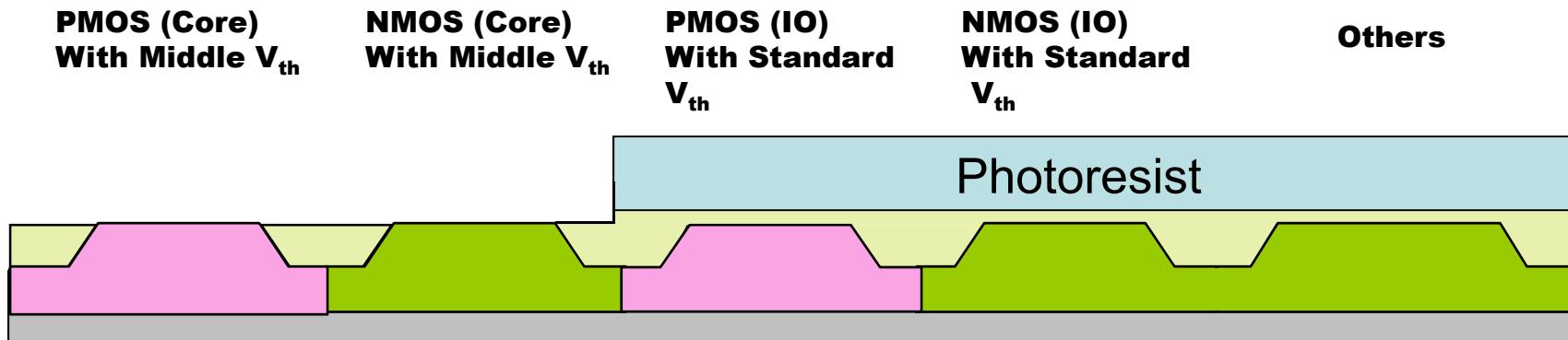
At first, thicker gate oxide is formed, then, removed from core devices portion and reformed thin gate oxide

Thick oxide is formed

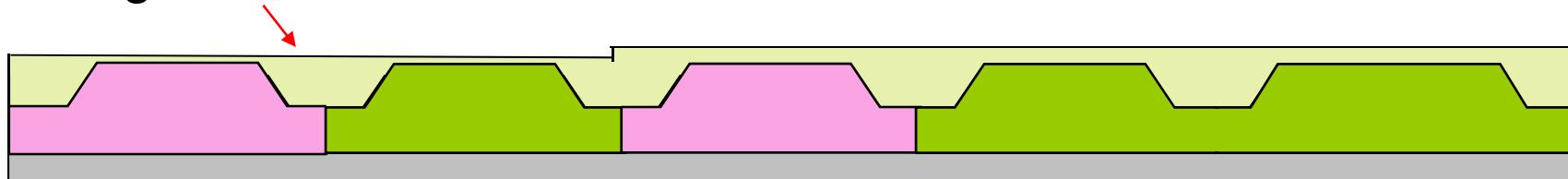


## Gate Oxide Formation (2)

Thick oxide is etched to prepare for thin oxide forming

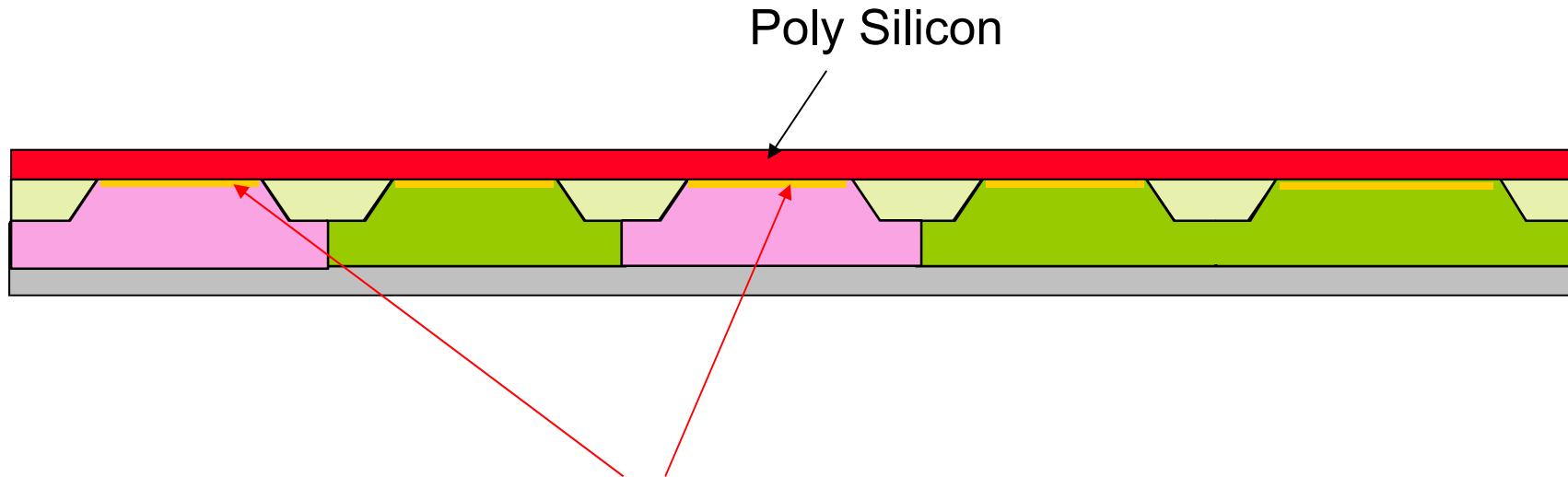


Thin gate oxide formation



# Poly Silicon Deposition

After gate oxide formation, poly silicon which is used as gate electrode is deposited (by CVD)



Gate oxide thickness is different in core device and IO device.  
But, to simplify the drawing, they are drawn as if they are the same.

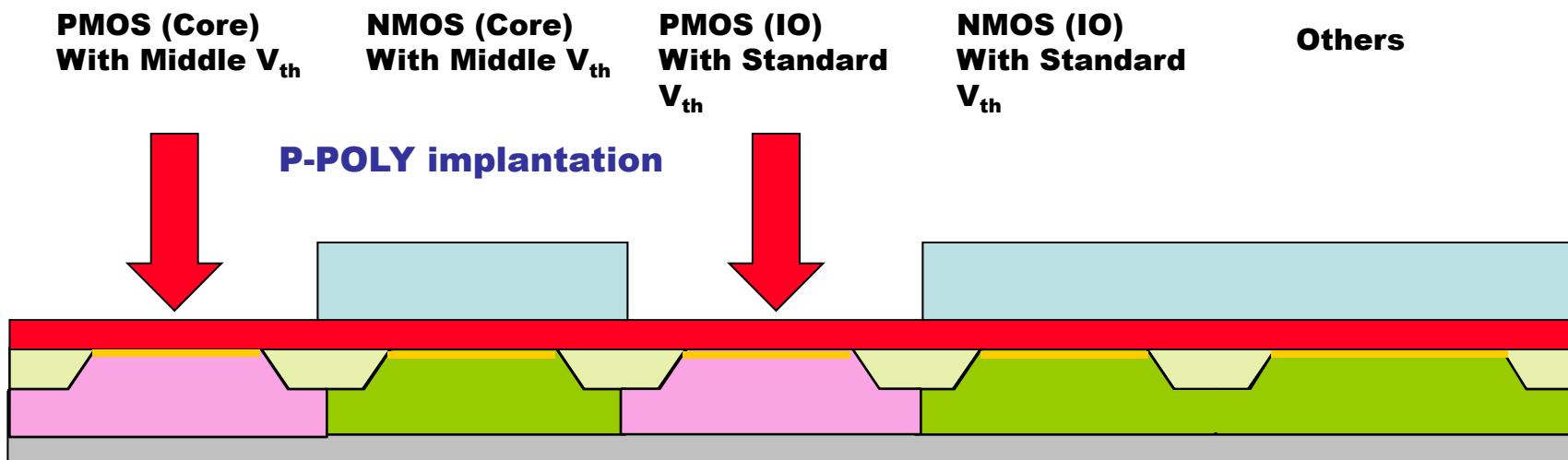
# Doping to Poly Silicon

Since deposited poly silicon is un-doped, its resistance is very high. We need to dope impurity to poly silicon to reduce the resistivity

$V_{th}$  of MOS transistor depends on which type of poly silicon is used

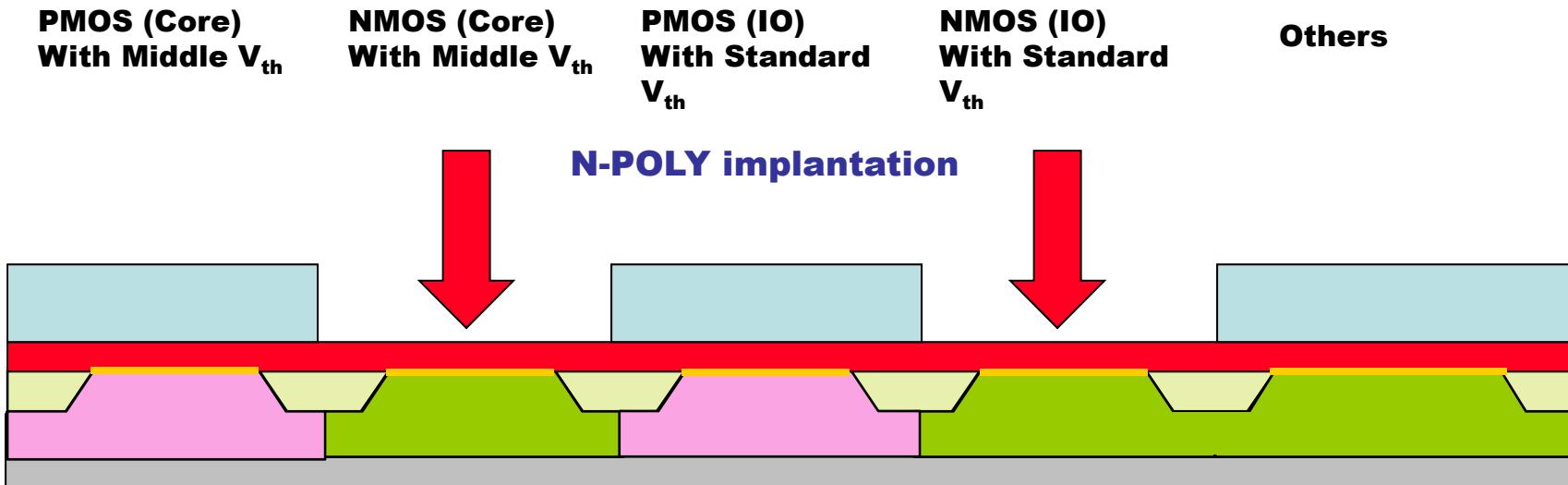
Typically, we use N-type poly silicon for NMOS, and P-type poly silicon for PMOS. To dope to poly silicon, the implantation is used

## Doping P-Poly to PMOS



# Doping to Poly Silicon (2)

Doping N-Poly to NMOS

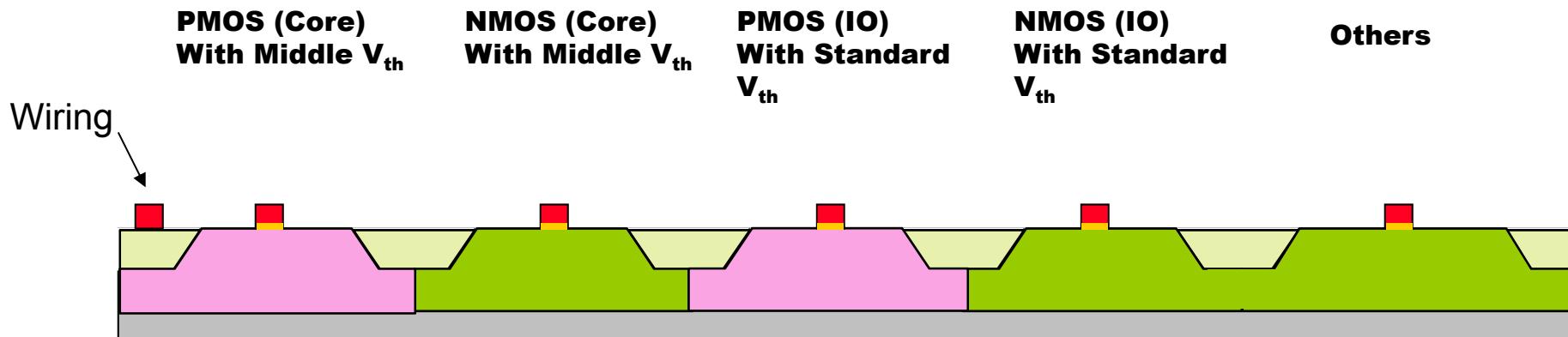


After the doping to poly silicon, the annealing is performed to activate doped impurity

# Gate Photolithography

Now, Poly silicon is etched to form gate electrode and wiring

Wiring: Poly silicon is not low enough, so it can be used for wiring but within cell only (short distance connection)



# LDD Formation - IO Devices (1)

Since the gate oxide is thin regarding to power supply, LDD (Lightly Doped Drain) structure is used to relax Electric Field which generates “hot carriers”

**PMOS (Core)  
With Middle  $V_{th}$**

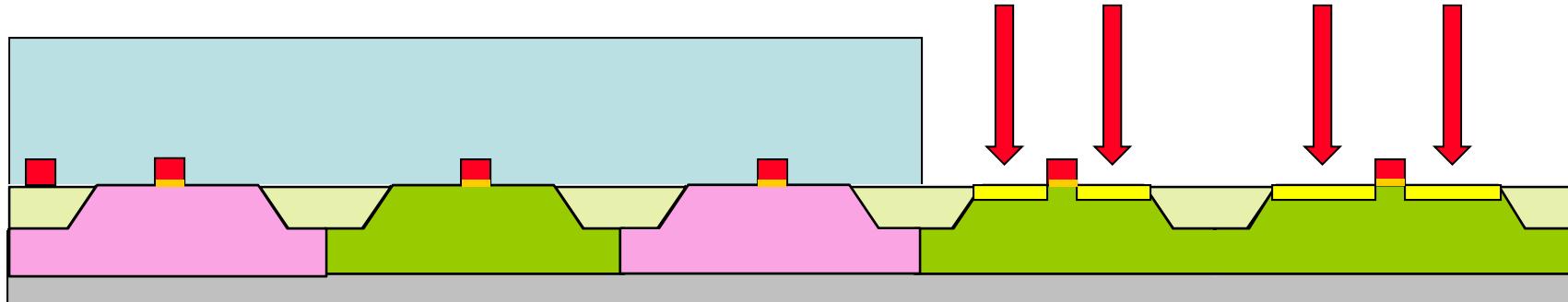
**NMOS (Core)  
With Middle  $V_{th}$**

**PMOS (IO)  
With Standard  
 $V_{th}$**

**NMOS (IO)  
With Standard  
 $V_{th}$**

**Others**

N-LDD photo and implantation



# LDD Formation - IO Devices (2)

**Pch Tr (Core)  
With Middle Vth**

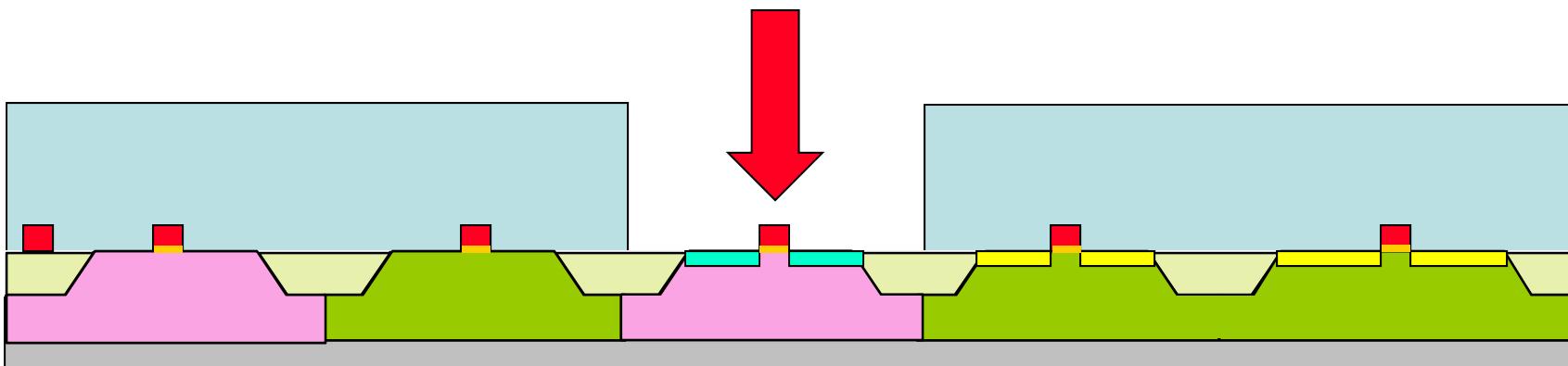
**Nch Tr (Core)  
With Middle Vth**

**Pch Tr (IO)  
With Standard  
Vth**

**Nch Tr (IO)  
With Standard  
Vth**

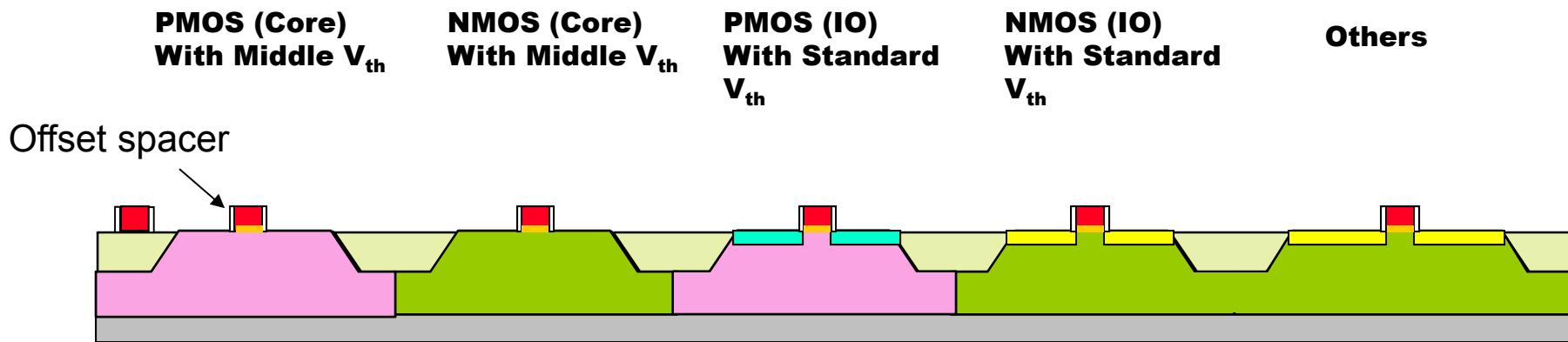
**Others**

P-LDD photo and implantation



# Offset Spacer Formation

Offset space for gate electrode (effect to core devices only) is formed using oxide deposition and etch-back process.



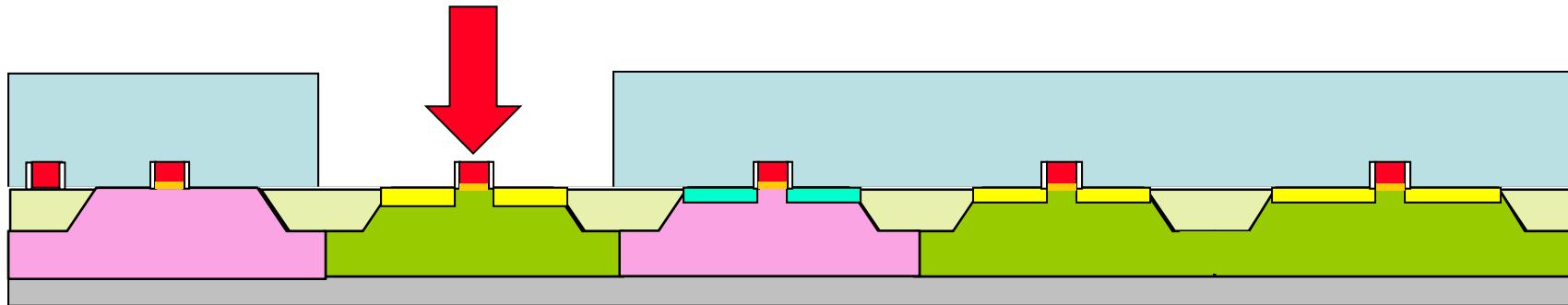
# Source/Drain - Extension Formation (1)

Since the power supply voltage to core devices is lowered to 1.2V or 1.0V, it is not necessary to adapt LDD structure to core devices. LDD structure makes larger parasitic resistance, then S/D-Extension structure is used for core devices

Extension implantation and Halo implantation are done

<b>PMOS (Core) With Middle <math>V_{th}</math></b>	<b>NMOS (Core) With Middle <math>V_{th}</math></b>	<b>PMOS (IO) With Standard <math>V_{th}</math></b>	<b>NMOS (IO) With Standard <math>V_{th}</math></b>	<b>Others</b>
--	--	--	--	---------------

Low voltage N-LDD photo and implantation



## S/D-Extention Formation (2)

**PMOS (Core)  
With Middle  $V_{th}$**

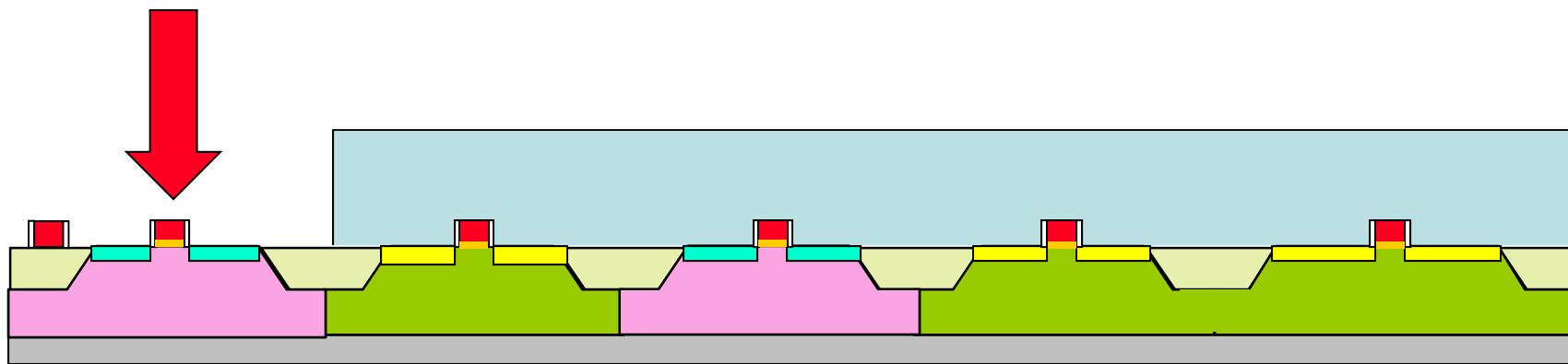
**NMOS (Core)  
With Middle  $V_{th}$**

**PMOS (IO)  
With Standard  
 $V_{th}$**

**NMOS (IO)  
With Standard  
 $V_{th}$**

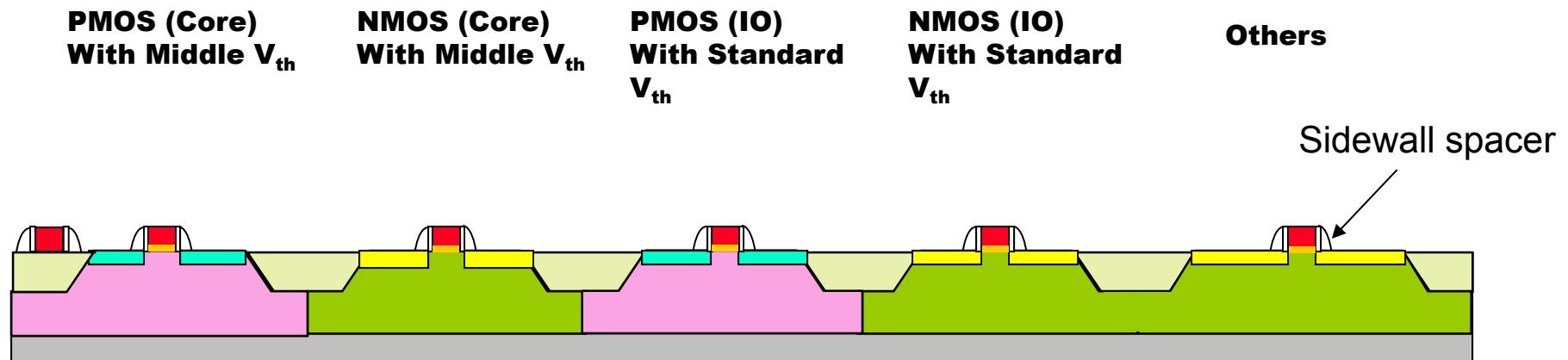
**Others**

Low voltage P-LDD photo and implantation



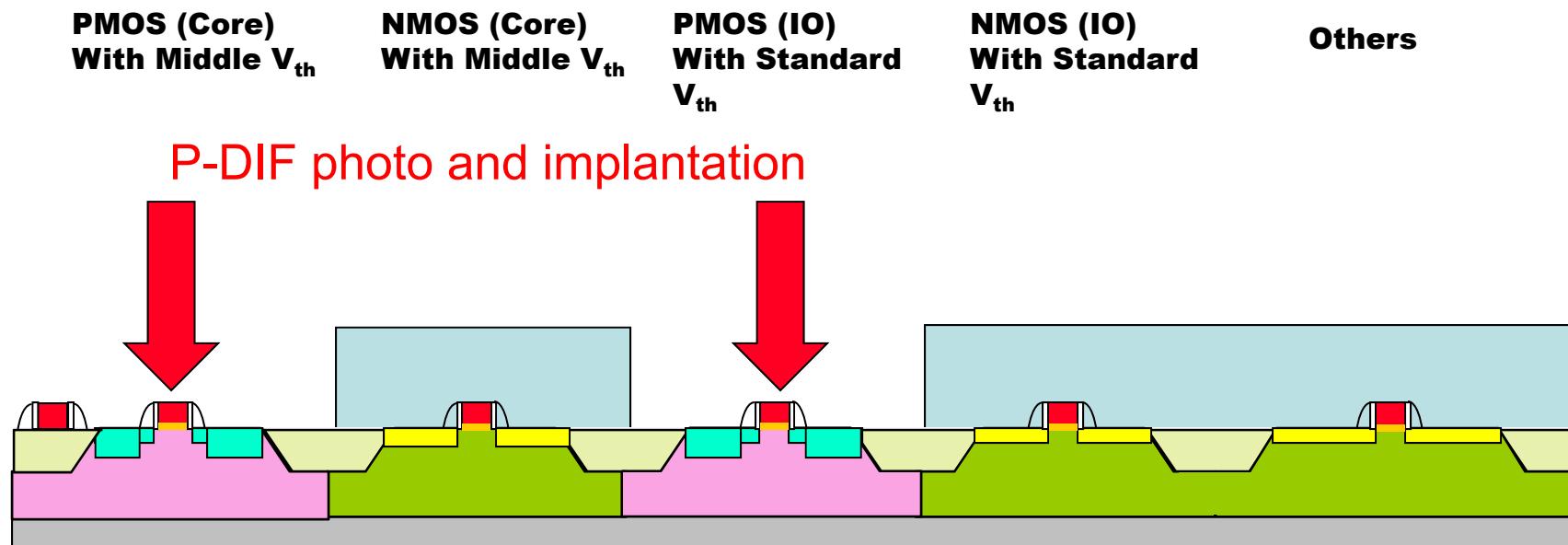
# Sidewall Spacer Formation

By applying CVD,  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$  are deposited and etched back to form sidewall spacer



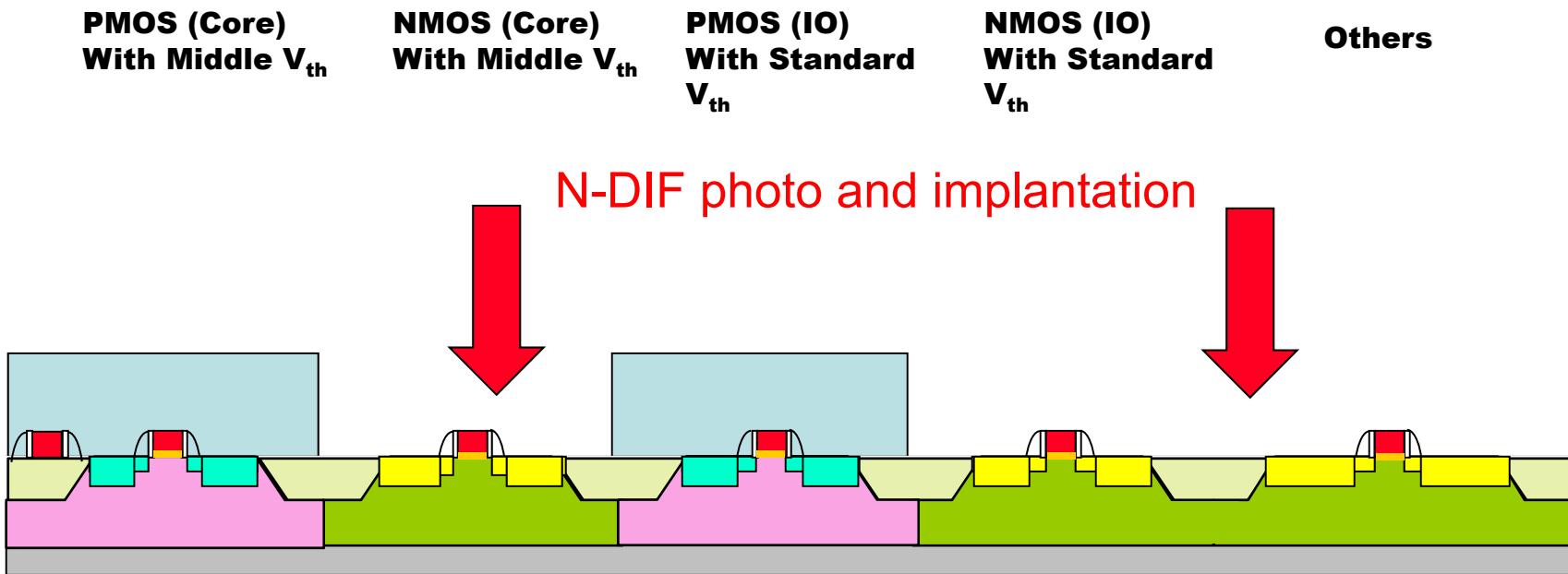
# Source and Drain Implantation (1)

High concentration ion implantation (Acceptor) is done and P+ diffusion is formed



# Source and Drain Implantation (2)

High concentration ion implantation (Donor) is done and N+ diffusion is formed

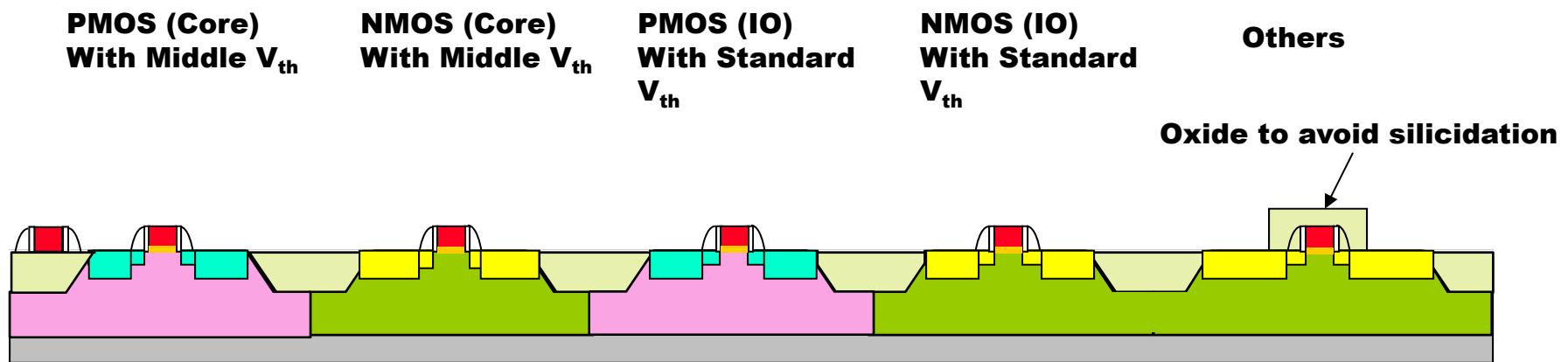


Diffusion annealing is performed

# Silicidation Formation

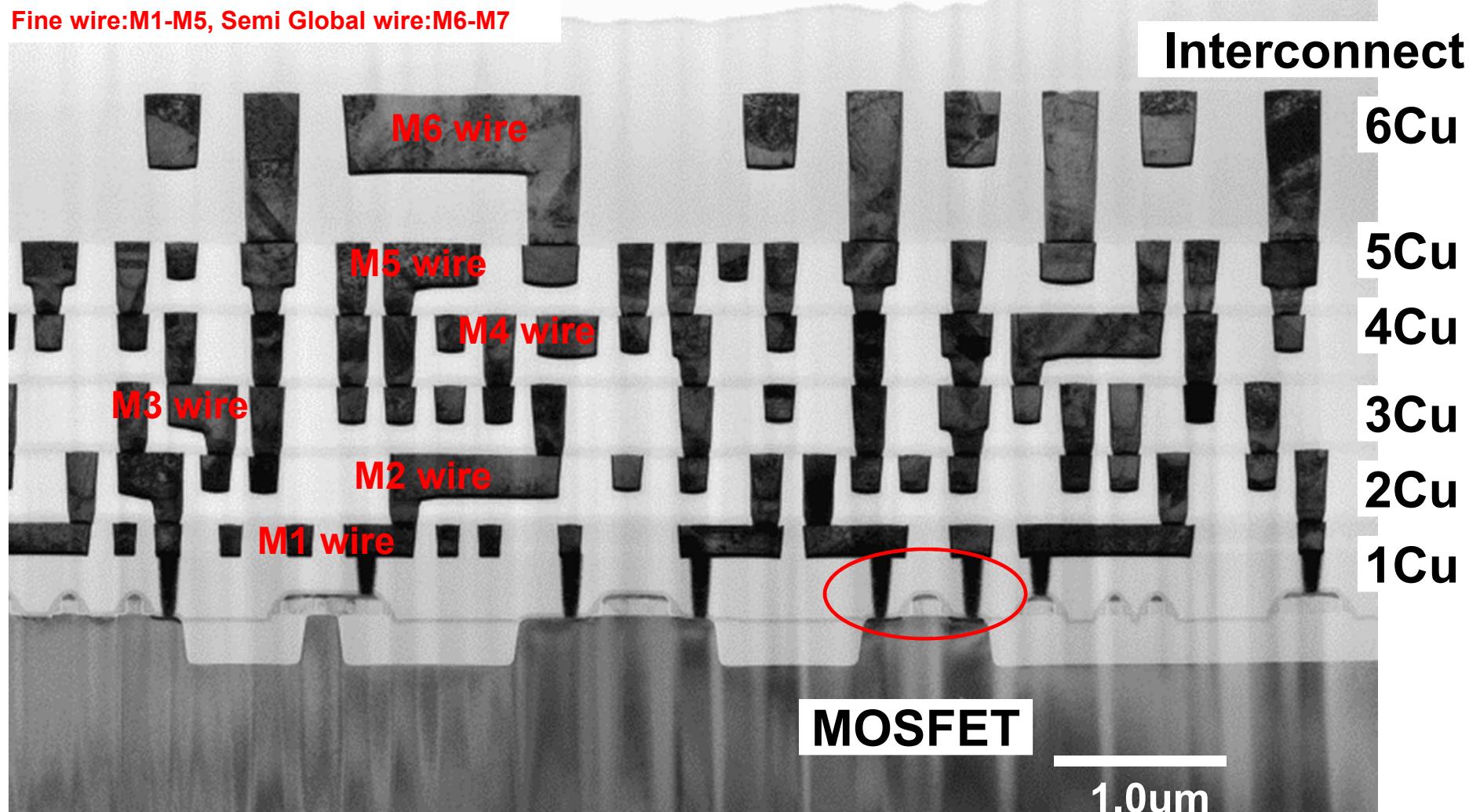
To lower the resistivity of diffusion layer and poly silicon, metal (Co, etc.) is deposited and sintered

Some hard macros, such as, analog modules or IO use high impedance poly silicon resistor. To avoid silicidation on such poly-silicon, oxide remains through photolithography (oxide deposition and photolithography)



# L S I Final Cross-section

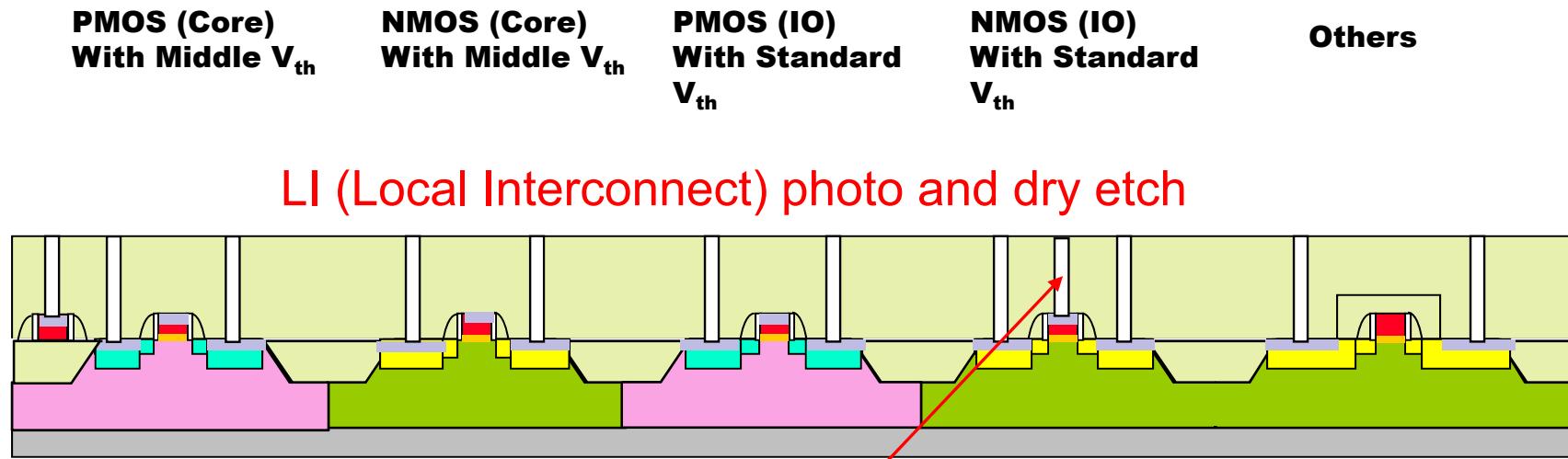
Cross-section SEM photograph of RC03 Product Application (6 layers Cu metal wire)



# Insulator Deposition and Contact Hole Formation

$\text{Si}_3\text{N}_4$  and CVD-Oxide are deposited as the insulator.

Contact holes for poly silicon and diffusion are opened through the insulator

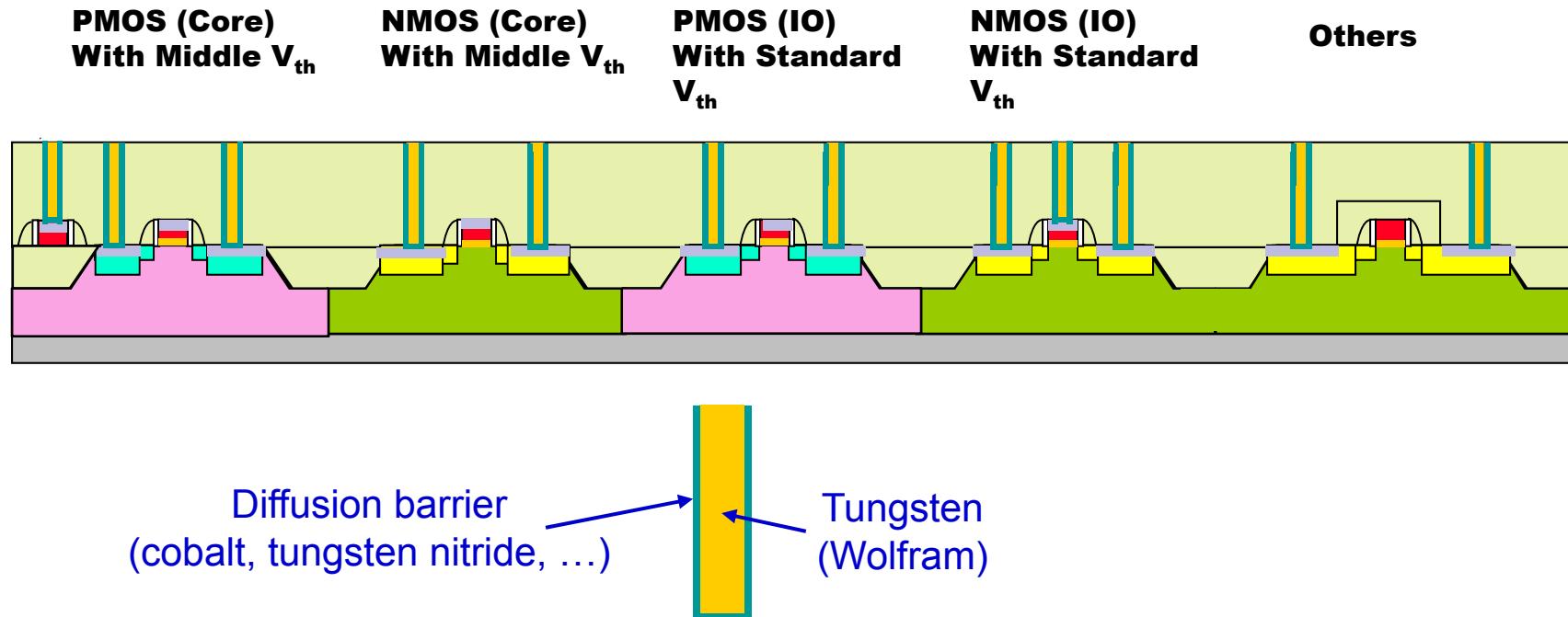


Note: Renesas Design Rule does not allow contact hole on gate.  
The above figure shows only for the explanation.

# Diffusion Barrier and Tungsten Plug Formation

Diffusion barrier (*thin layer of metal placed between two materials and acts as a barrier to protect either one of materials from corrupting the other*) is deposited and tungsten (W) is deposited.

Tungsten is planarized by CMP.

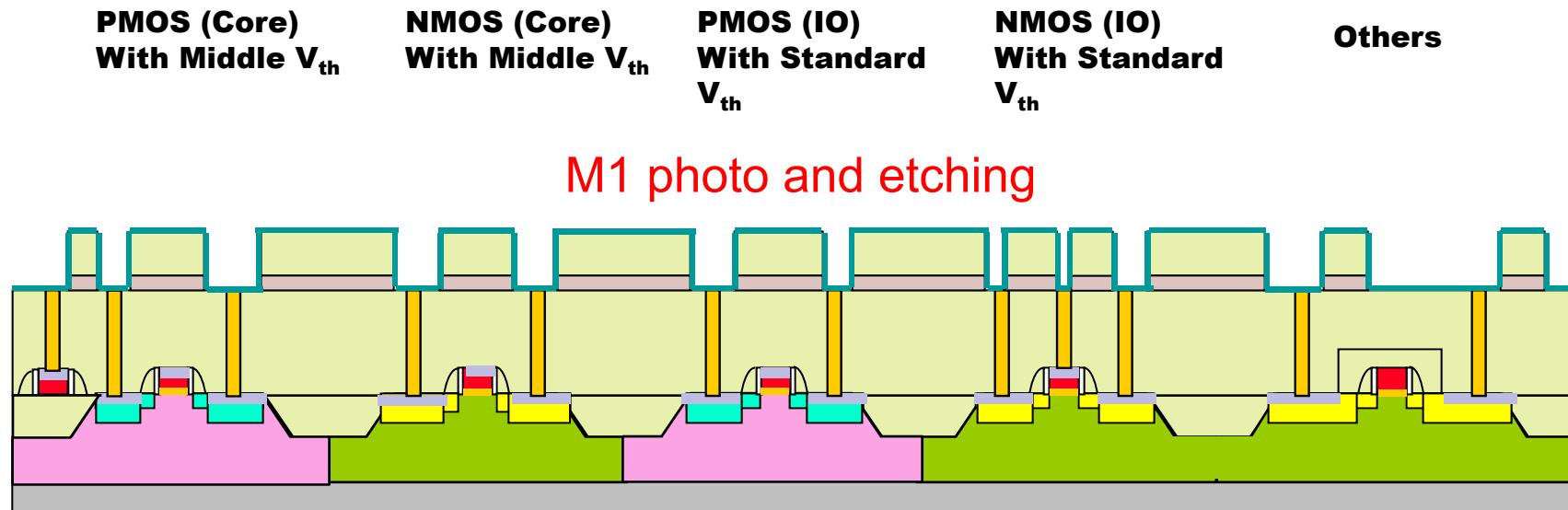


# Insulator Deposition and Metal 1 Photolithography

$\text{Si}_3\text{N}_4$  (etching stopper) and CVD-Oxide are deposited. Insulator is planarized by CMP.  $\text{Si}_3\text{N}_4$  also works as anti-diffusion layer of Cu.

Metal 1 photolithography is done and insulators are etched.

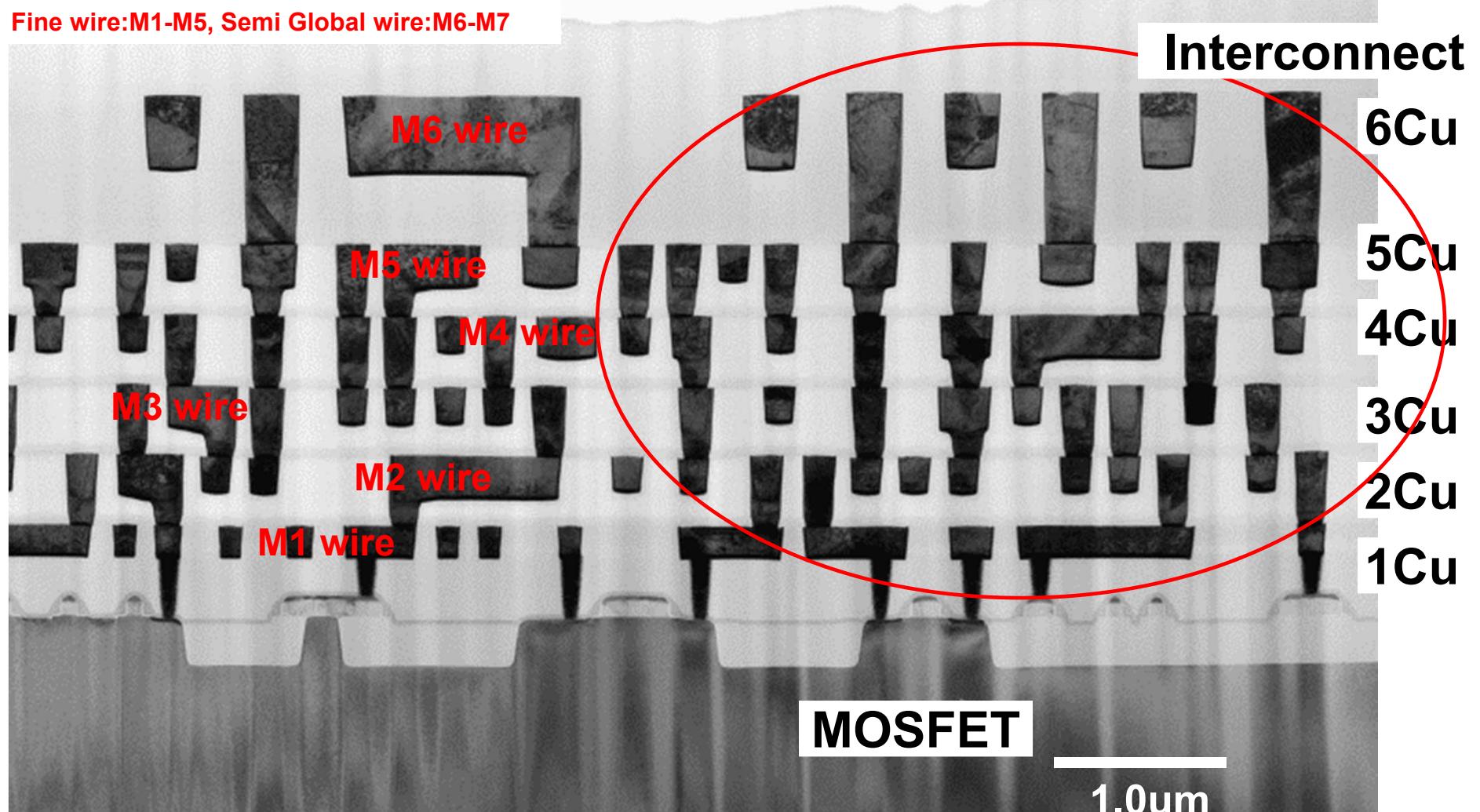
Diffusion barrier is deposited.



Note: To simplify the drawing, diffusion barrier for W is not drawn.

# L S I Final Cross-section

Cross-section SEM photograph of 90nm Product Application (6 layers Cu metal wire)



# The Advantage of Cu Wiring

---

The advantages of Cu wiring over Aluminum are as follows:

1. Lower resistivity than Aluminum.(Al:2.8 $\mu$  ohm cm, Cu:1.7 $\mu$  ohm cm)  
Can be thinner than Al with the same resistance, which reduces capacitance.
2. Higher melting point and less electro-migration.
3. Less stress-migration.

The disadvantages

1. Cu is one of the harmful elements to Si and SiO<sub>2</sub>.
2. Cannot be deposited by CVD.
3. Cannot be dry-etched.
4. Weak cohesion to SiO<sub>2</sub>
5. TDDB lifetime is shorter than Al and W.

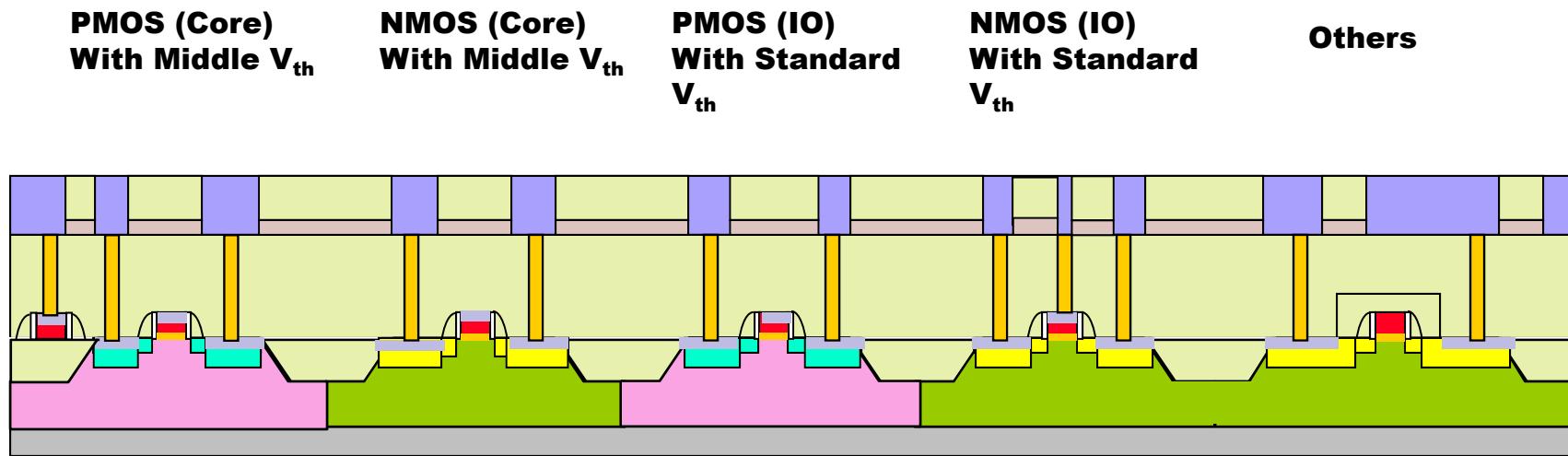
*(TDDB: Time Dependence on Dielectric Breakdown )*

→ Damascene process is the best one for Cu.

# Metal 1 Formation

Cu seed is sputtered, then plated to fill the recess.

Cu is polished back using CMP.

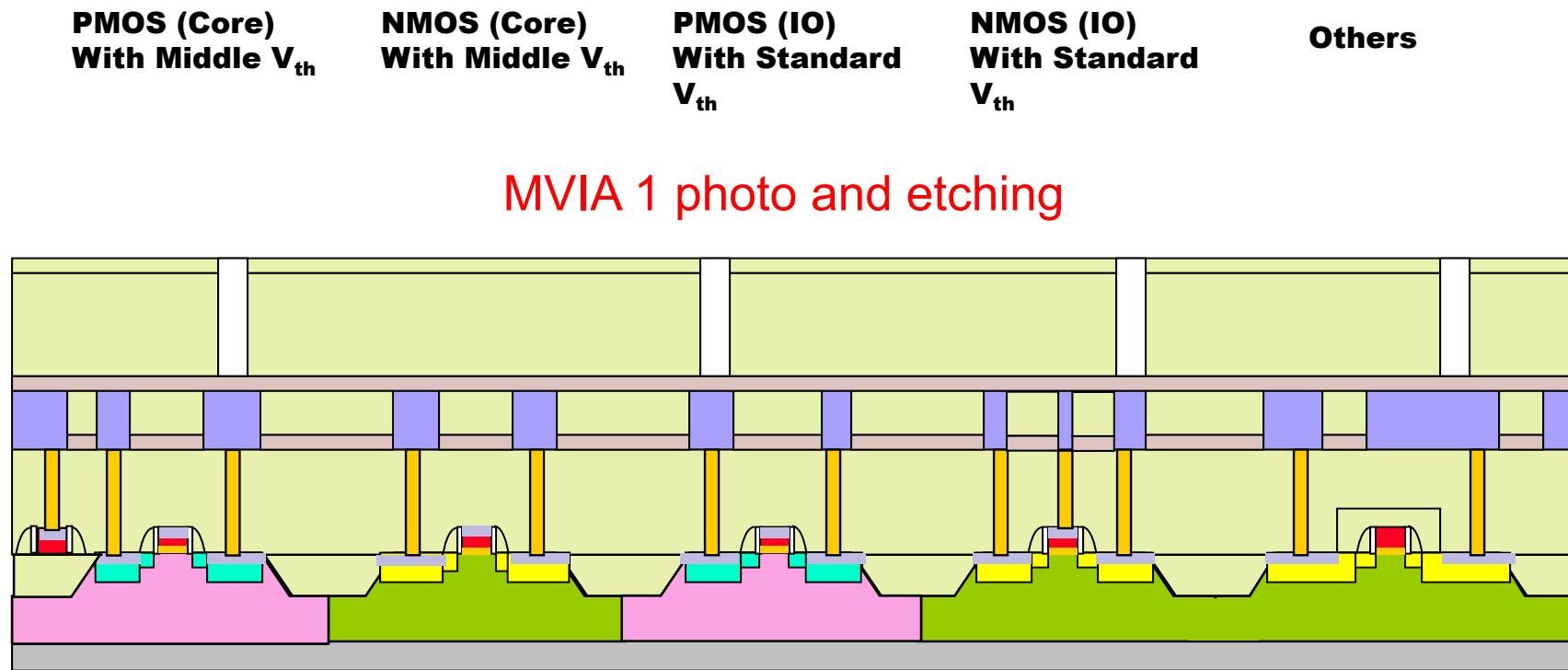


**Note:** Diffusion barrier exists at the bottom and wall of Via,  
but to simplify the drawing, it is not drawn

# Insulator Deposition and Via 1 Formation

Etching stopper and insulators between Metal 1 and Metal 2 are deposited.

Via 1 is opened.



# Metal 2 Photolithography

The portions where metal 2 to be formed are etched.

**PMOS (Core)  
With Middle  $V_{th}$**

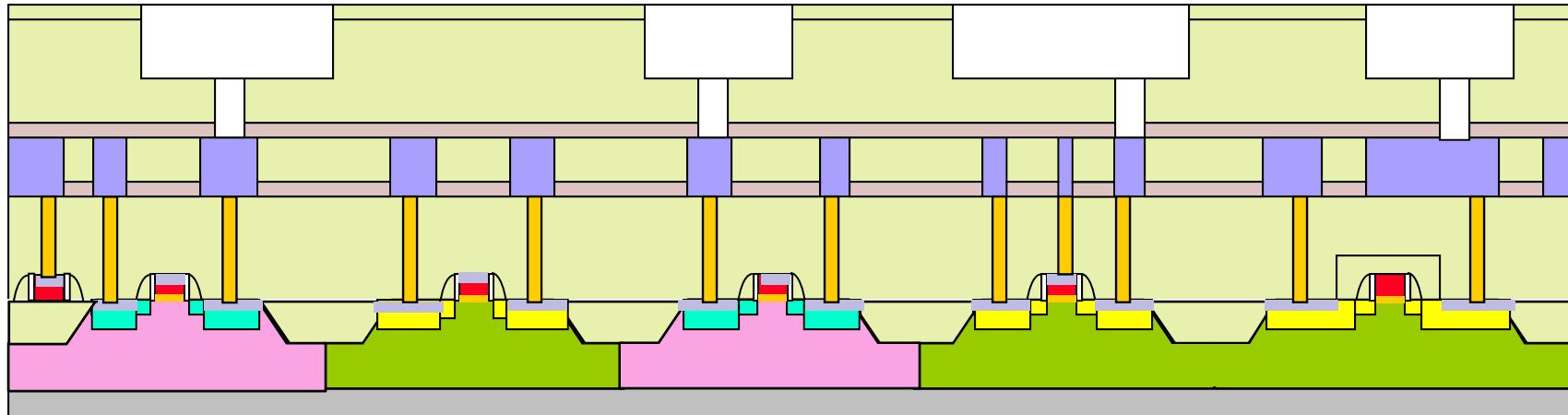
**NMOS (Core)  
With Middle  $V_{th}$**

**PMOS (IO)  
With Standard  
 $V_{th}$**

**NMOS (IO)  
With Standard  
 $V_{th}$**

**Others**

**M2 photo and etching**



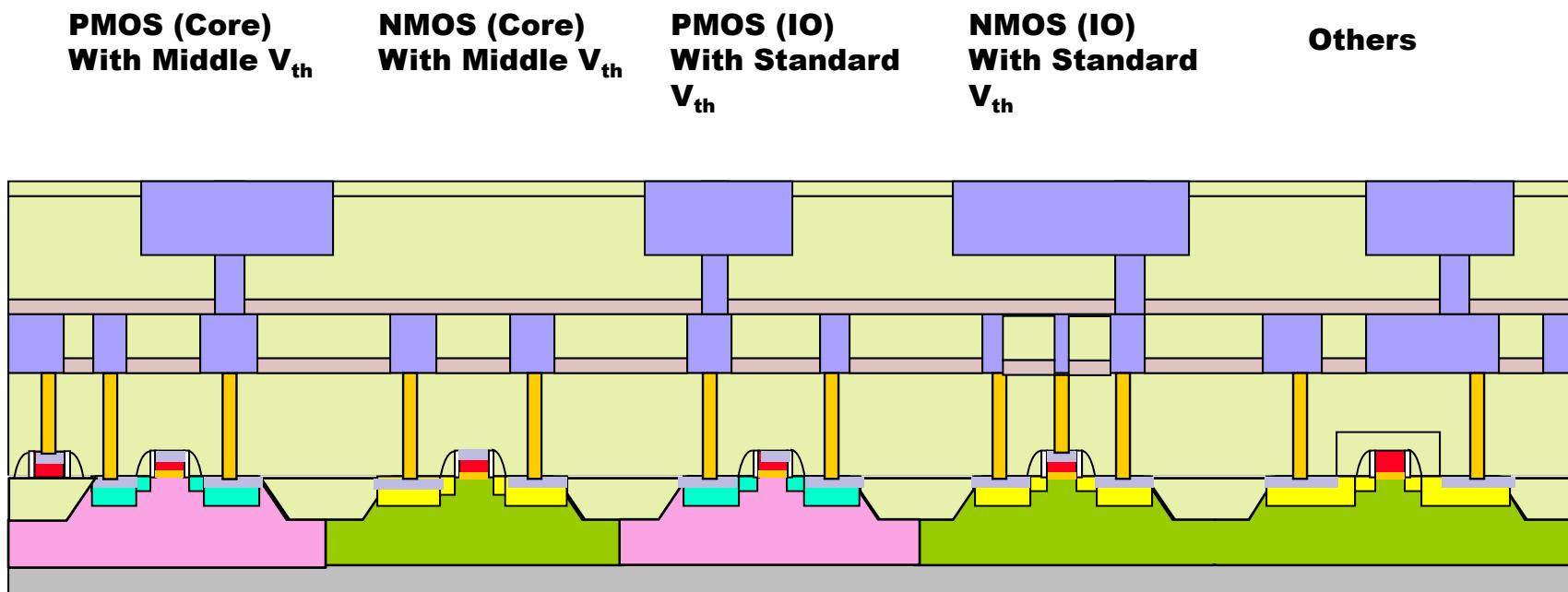
# Metal 2 Formation

Diffusion barrier is deposited (not drawn).

Cu (seed) is sputtered and plated to fill the recess.

Cu is polished back by using CMP.

Via and Metal recess formation is called **dual damascene process**.



## Via 2 to Metal 6 Formation

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Almost same procedures are taken to form via 2 to metal 6.

How many Cu layers are used depends the functions, target speed, chip price, etc. of the products.

## Pad Aluminum Formation

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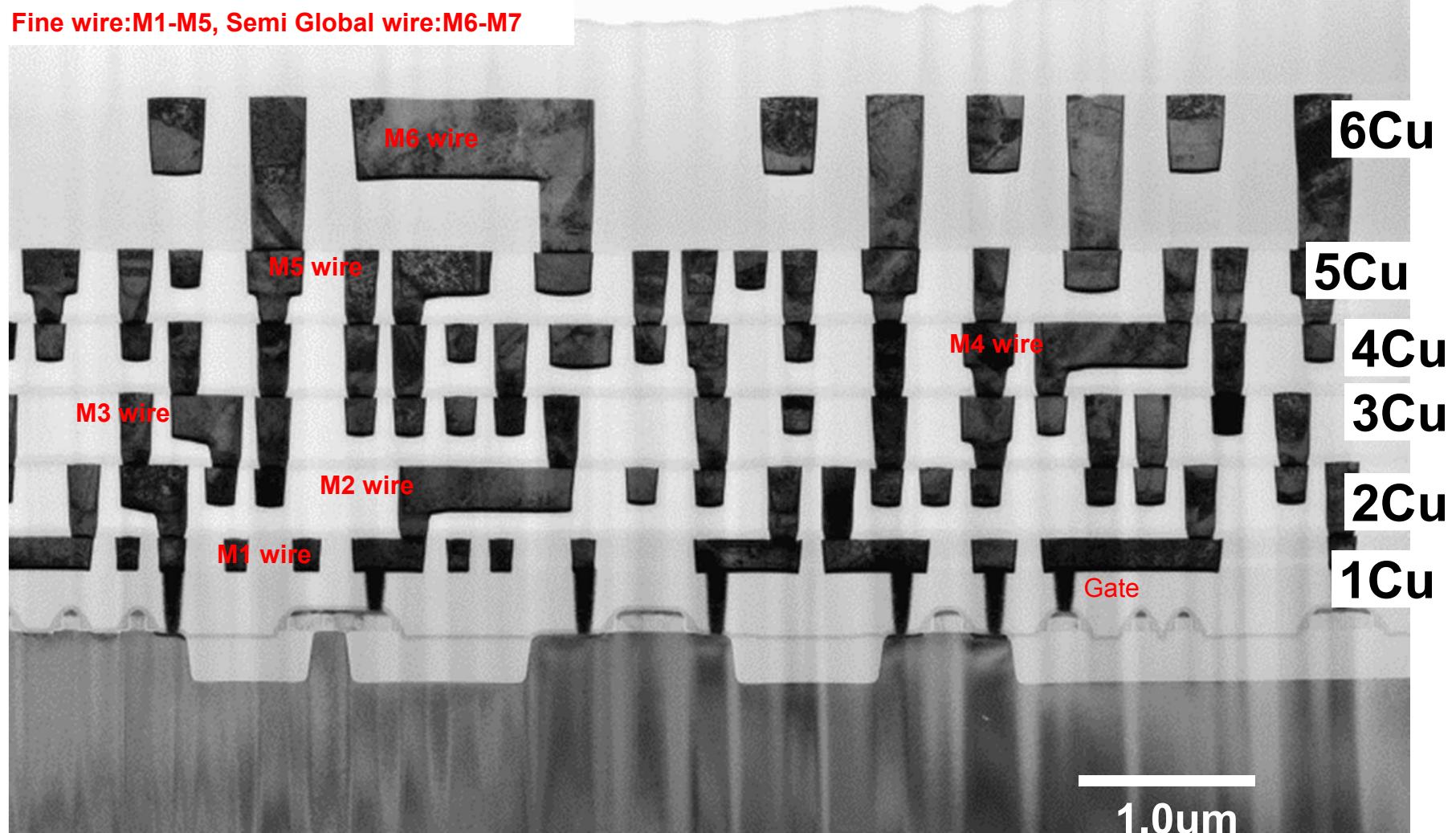
Cu is not a suitable material to bond to the lead of the package.

So thick aluminum is deposited as a final metal and uses as bonding pads.

It also uses as Power line on the chip.

# Final Cross-section

Cross-section SEM photograph of 90nm Product Application (6 layers Cu metal wire)



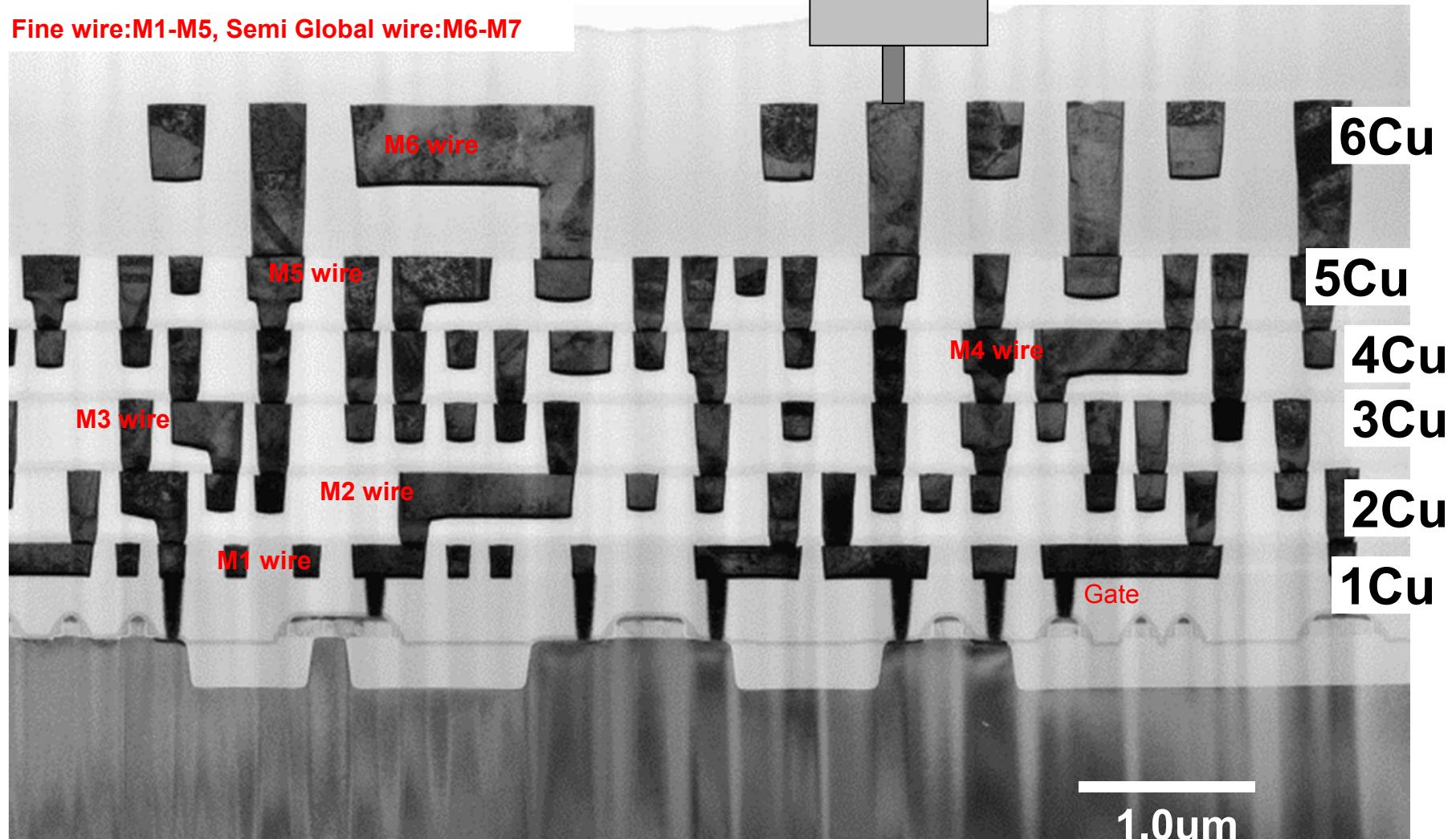
# Final Cross-section

Cross-section SEM photograph of 90nm Product A

PAD Al

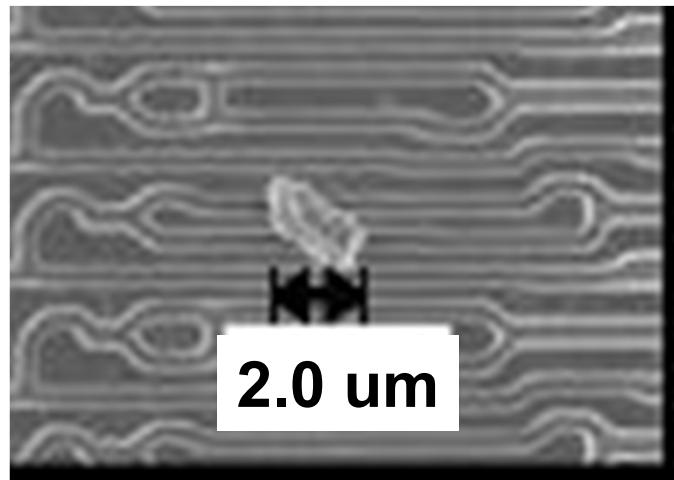
(6 layers Cu metal wire)

Fine wire:M1-M5, Semi Global wire:M6-M7

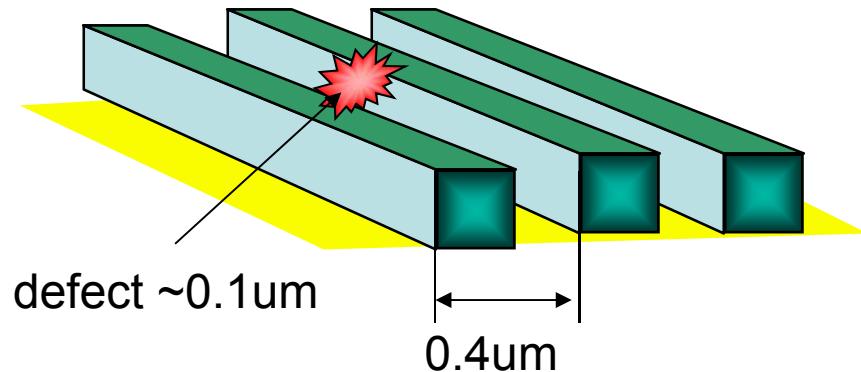


# **Process Defect and Yield**

# Pattern defect and Yield

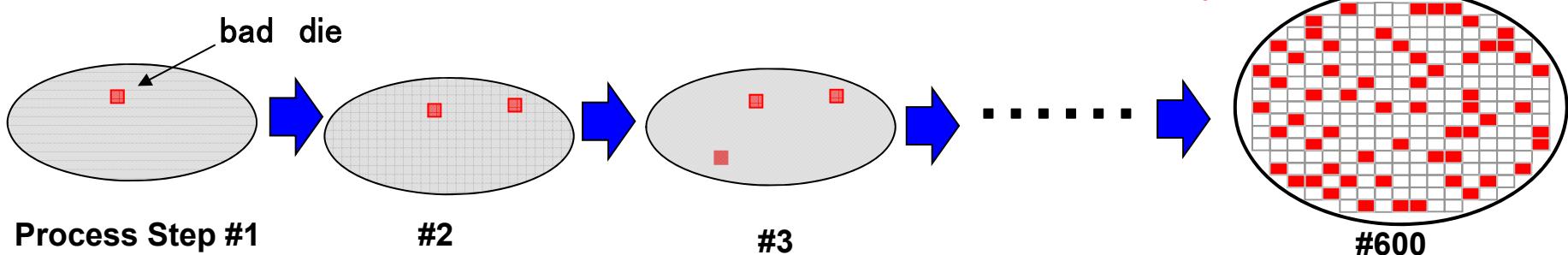


**Interconnect short !!**  $\Rightarrow$  bad die

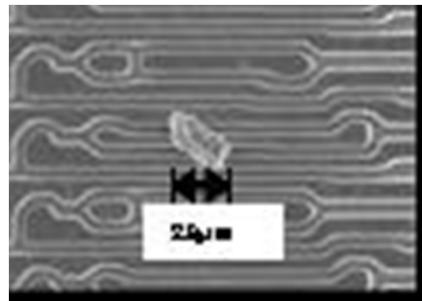


Even if we have 1 defect/wafer/step,    Important steps > 100

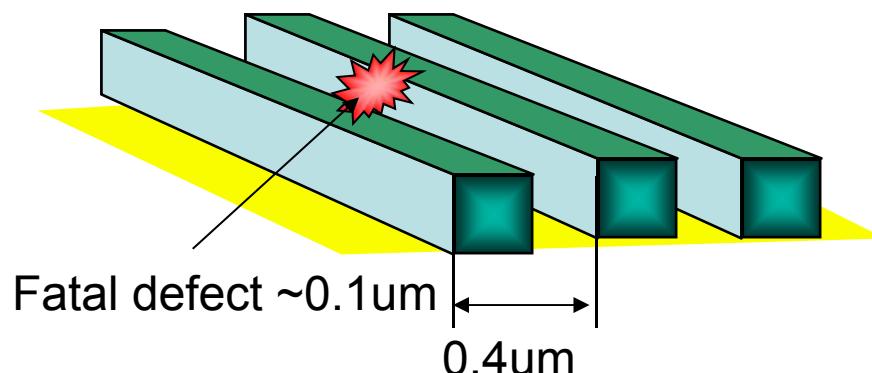
a lot of bad die !!  
low yield



# Pattern defect and Yield



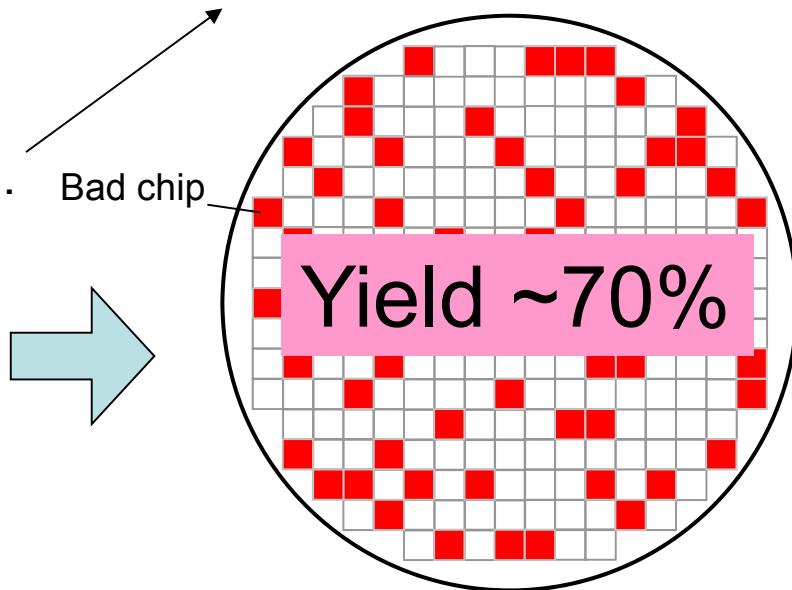
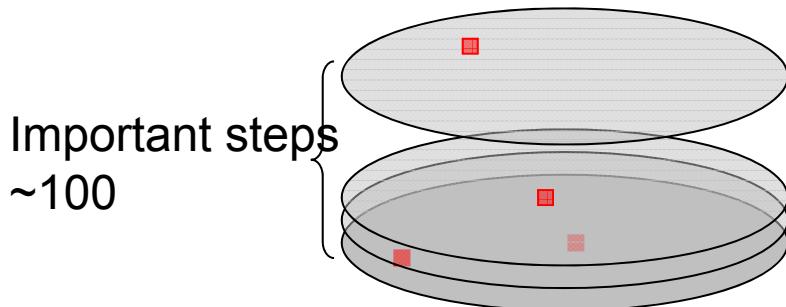
to analogy, in defect size on a wafer:



1 piece of foreign particle such as a tip of hair dropped in the area of 216mx216m.

Fatal defect  $\sim 0.1\mu\text{m}$

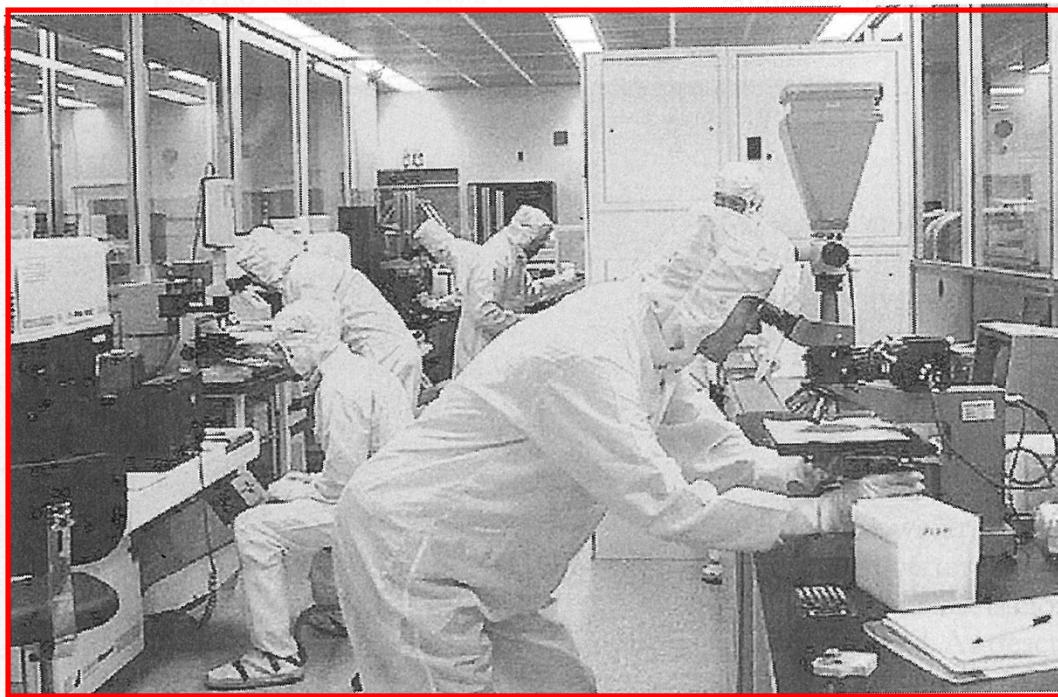
Even if we have 1 defect/wafer/step...



# Contamination Reduction

Human is one of the origin of contamination.

To reduce the contamination from human, we put a special cloth and all wafer process steps are done in the clean room.



**Figure 4-9** Configuration of typical modern cleanroom for IC fabrication. Photo courtesy of Stanford Nanofabrication Facility.

From SILICON VLSI TECHNOLOGY

# Yield

If the good chips can be gotten randomly in a wafer, the yield is expressed by the following formula.

$$Y = \exp[-(S \times D)]$$

Where S is the area of the chip ( $\text{cm}^2$ ) and D is a defect density( $/\text{cm}^2$ )

Example:

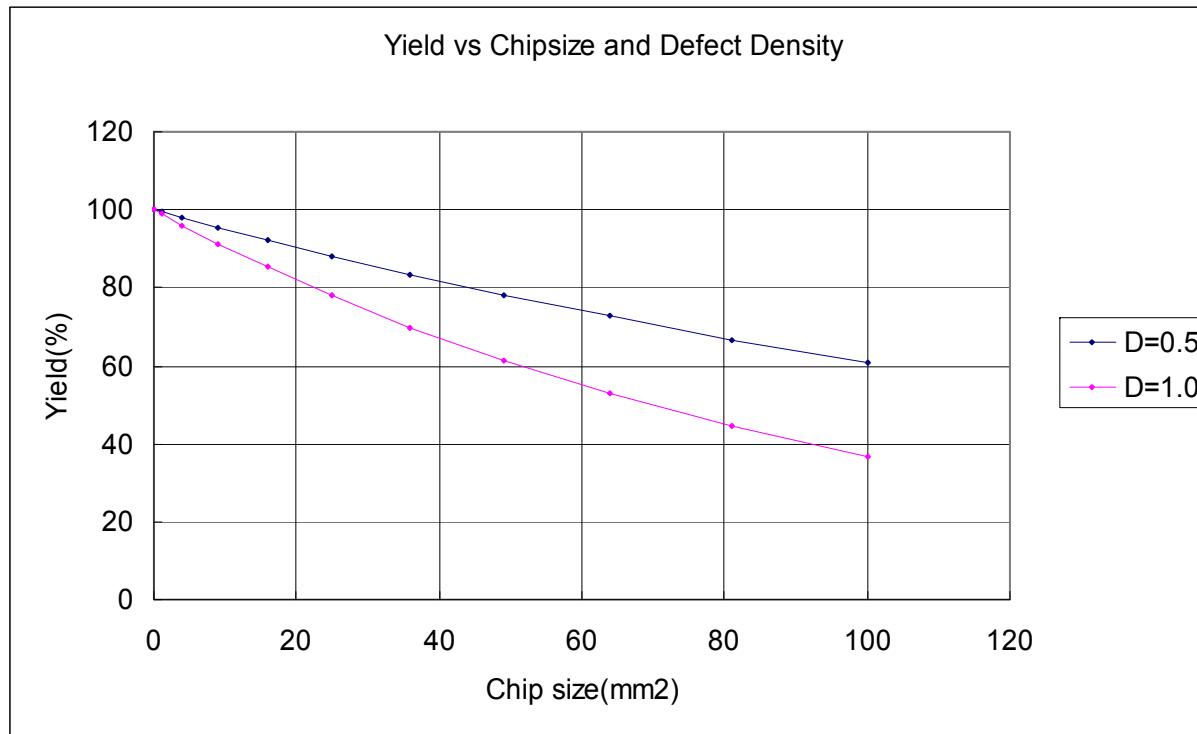
$$D = 1 / \text{cm}^2$$

$$S = 6.0 \text{ mm} \times 6.0 \text{ mm} = 36 \text{ mm}^2 = 0.36 \text{ cm}^2$$

$$Y = \exp[-(0.36 \times 1)] = 0.6976 \Rightarrow \text{Yield} = 69.8\%$$

# Yield

The yield is lowered as the chip size or defect density increases. It is LSI designer's responsibility to design smaller chips.



$$Y = \exp[-(S \times D)]$$

where, S is the area of the chip (cm<sup>2</sup>)  
and D is a defect density (/cm<sup>2</sup>)

# **Reliability**



## The reliability in wafer process

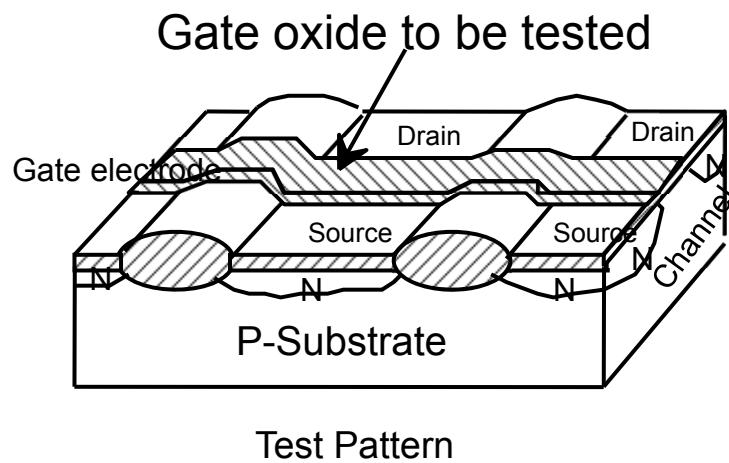
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1. TDDB (Time Dependent Dielectric Breakdown)
2. Hot carrier
3. Electro-migration
4. Stress-migration

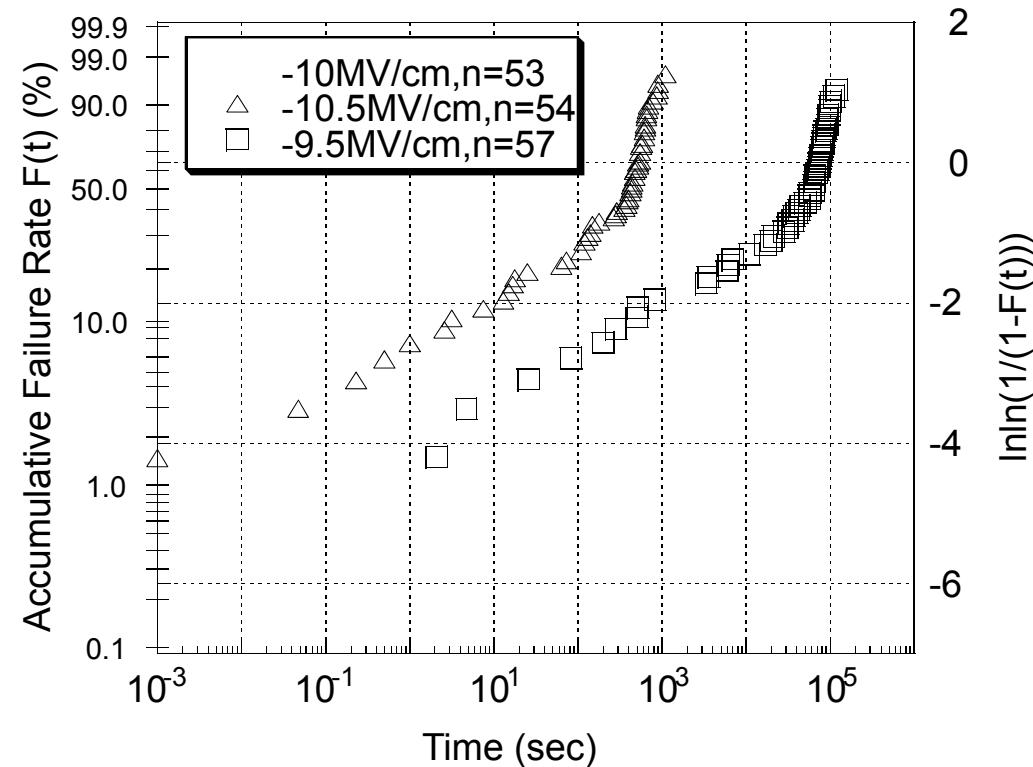
# Example of TDDB evaluation

## TDDB: Time Dependent Dielectric Breakdown

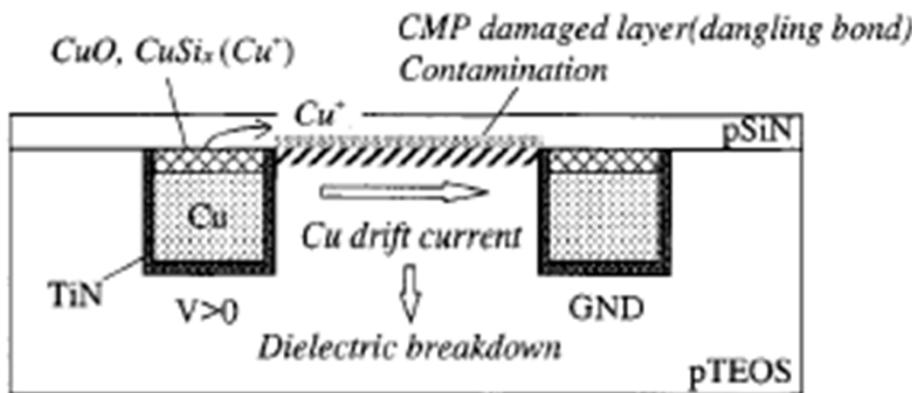
The phenomenon that the insulator breakdown occurs with time, when the electric field smaller than the absolute breakdown is being applied to the oxide for a long time.



We can estimate the lifetime of Oxide by accelerated TDDB test



# Why TDDB lifetime of Cu is shorter than Al and W



## TDDB degradation mechanism

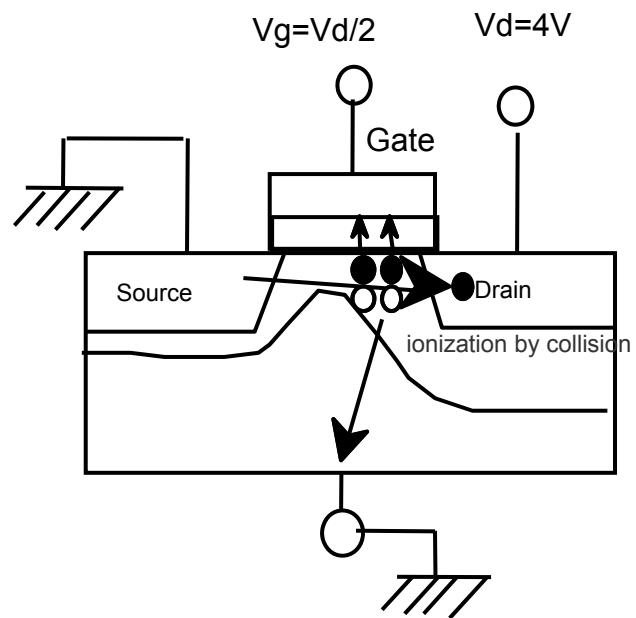
J.Noguchi et al. IRPS(2000) 339

- ① By CMP,
  - $Cu^+$  is generated on Cu surface
  - The damage occurs on insulator surface
- ② With biasing between Cu wiring,  $Cu^+$  diffuses into the damaged layer of the insulator
- ③ Oxide breakdown occurs

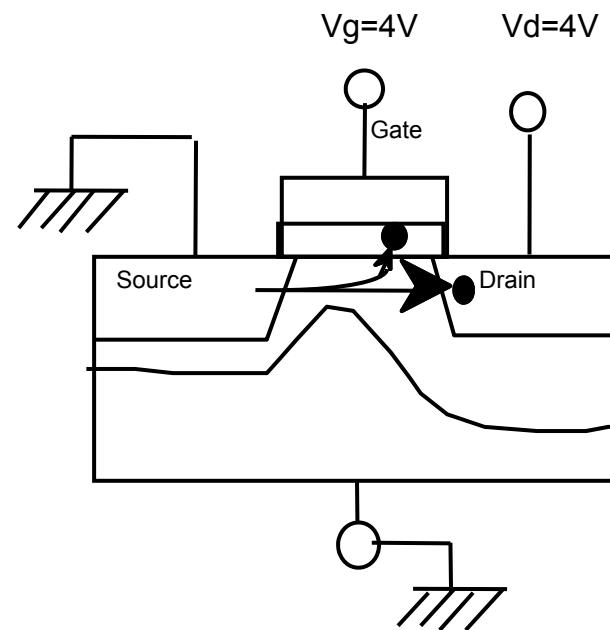
# Hot carrier injection to NMOS FET

Carriers in channel or pinch-off region becomes hot (getting high energy: electron temperature becomes higher than device temperature) due to acceleration by the electric field.

Hot carriers are injected to the gate oxide across the energy barrier at Oxide-Si interface and becomes trapped charges.



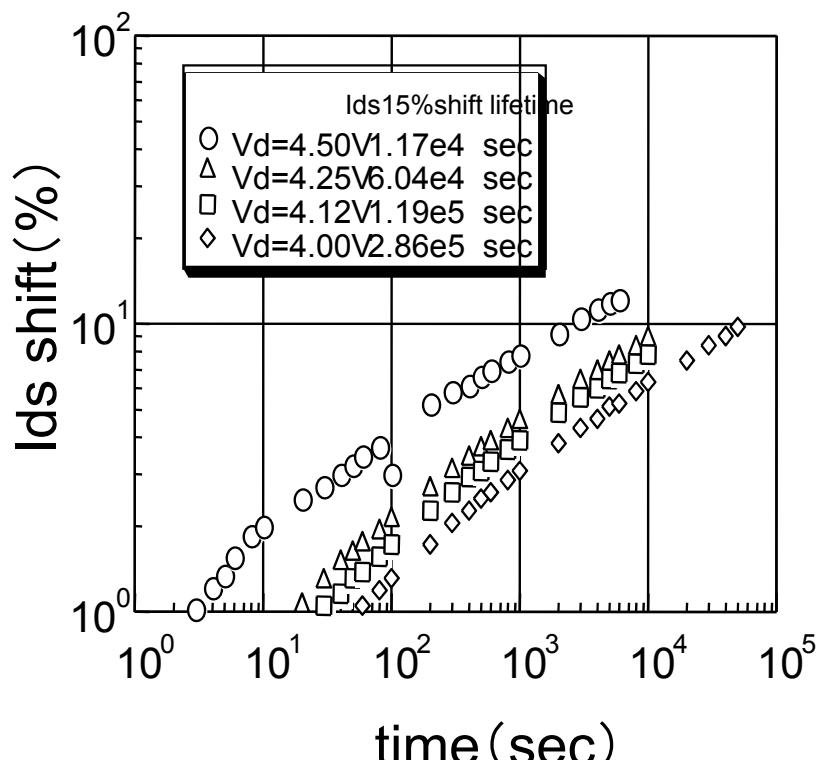
(a) Injection by Drain Avalanche Hot Carrier (DAHC)



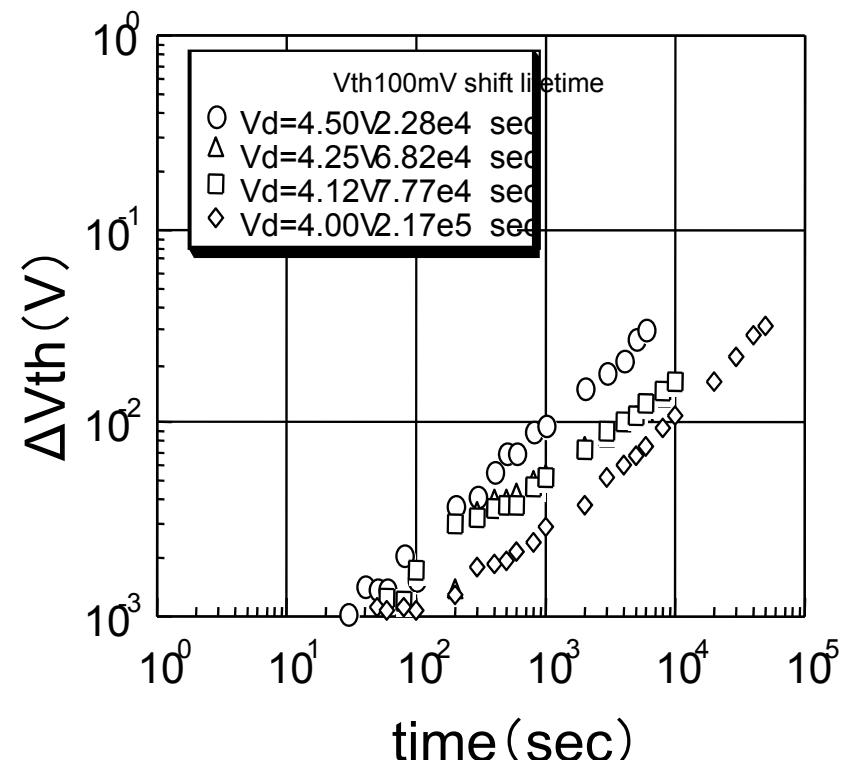
(b) Injection of Channel Hot Carrier (CHC)

# Degradation due to Hot carrier injection to NMOS FET

Example of characteristics degradation due to hot carrier injection:  
Increase of V<sub>th</sub>, Lowering of conductance



Stress applying time–  $I_{ds}$  shift



Stress applying time -  $\Delta V_{th}$

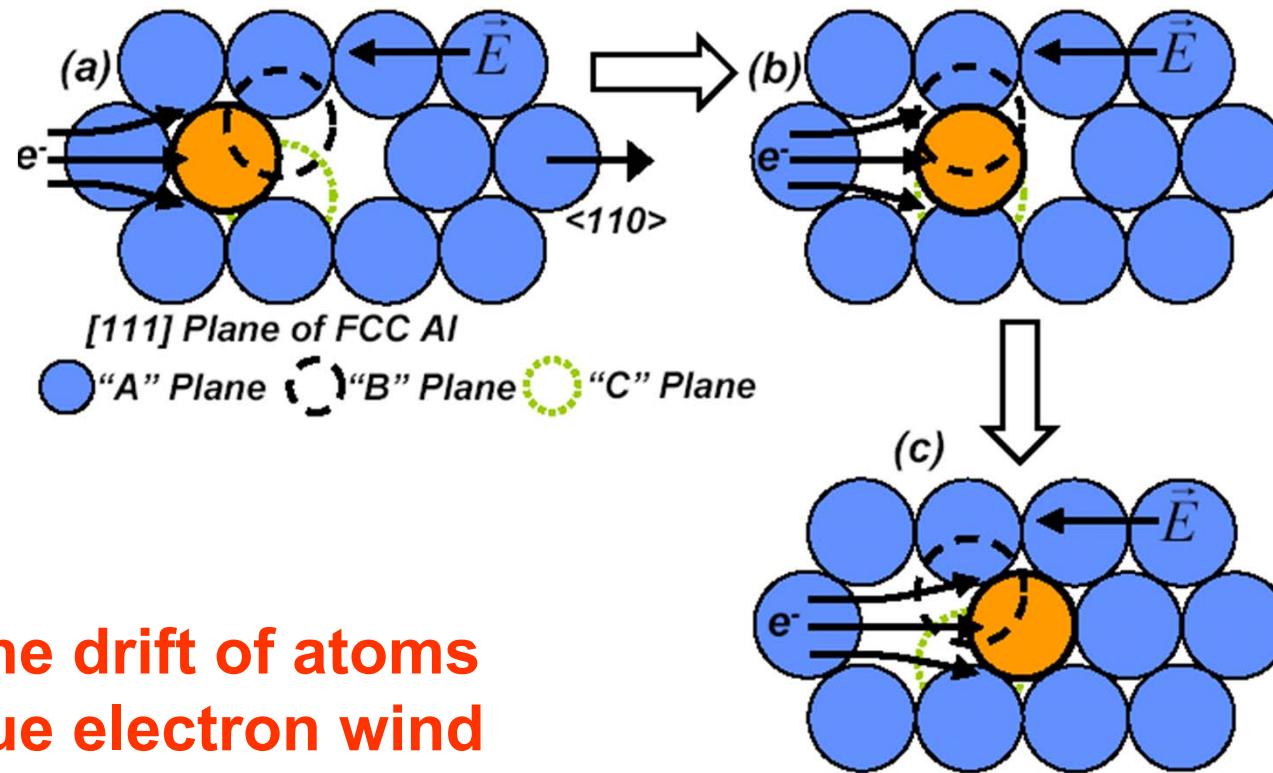
# **What is the Electro-migration?**

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**Electro-migration** refers to the gradual displacement of the metal atoms of a conductor as a result of the current flowing through that conductor. Because of the mass transport of metal atoms from one point to another during electro-migration, this mechanism leads to the formation of voids at some points in the metal line and hillocks or extrusions at other points.

It can therefore result in either: 1) an open circuit if the void(s) formed in the metal line become big enough to sever it; or 2) a short circuit if the extrusions become long enough to serve as a bridge between the affected metal and another one adjacent to it.

# Schematic of electro-Migration mechanism(1)



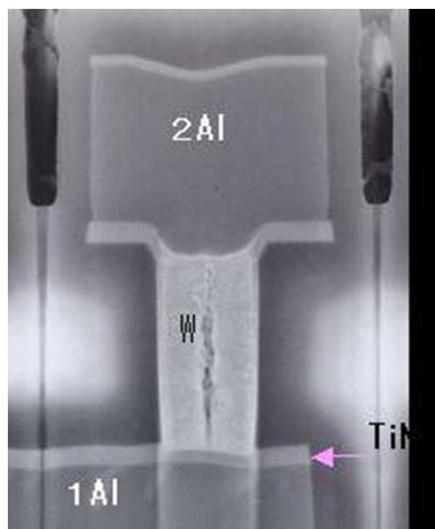
**The drift of atoms  
due electron wind**

=**The diffusion of voids  
→Growth of voids**

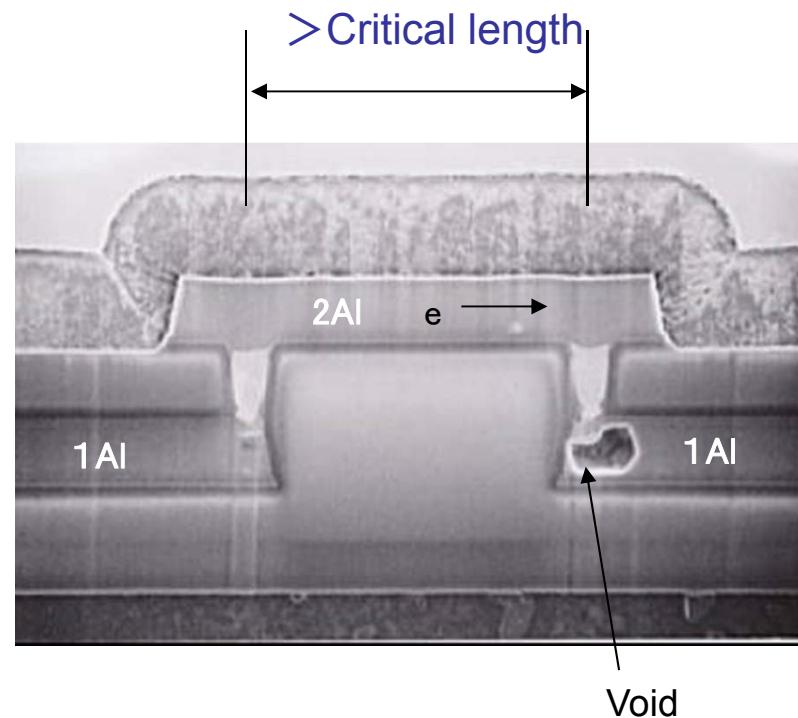
Ogawa(TI), 2002 IRPS

# Electro-Migration mechanism (1)

Aluminum atoms are transferred by the electron flow and void is formed at the discontinuous portion of flow.

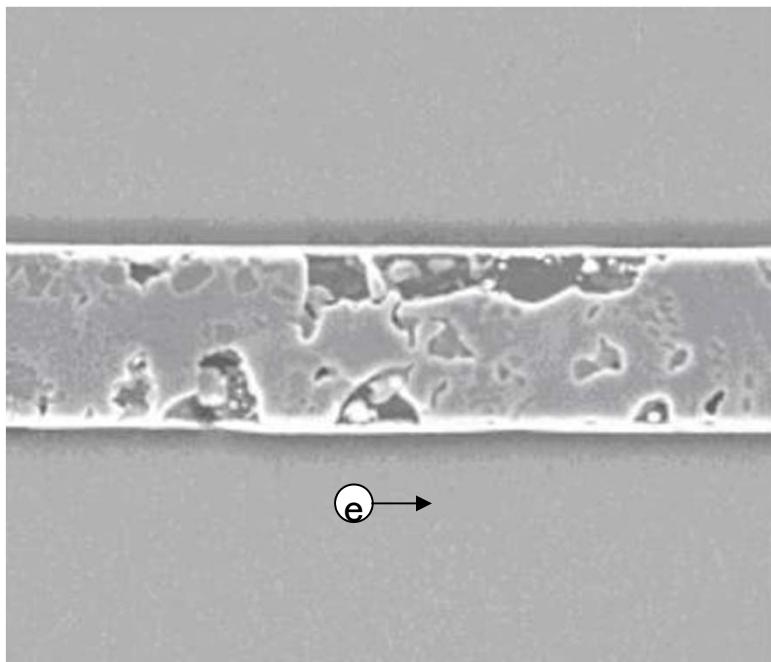


Cross-section of Via

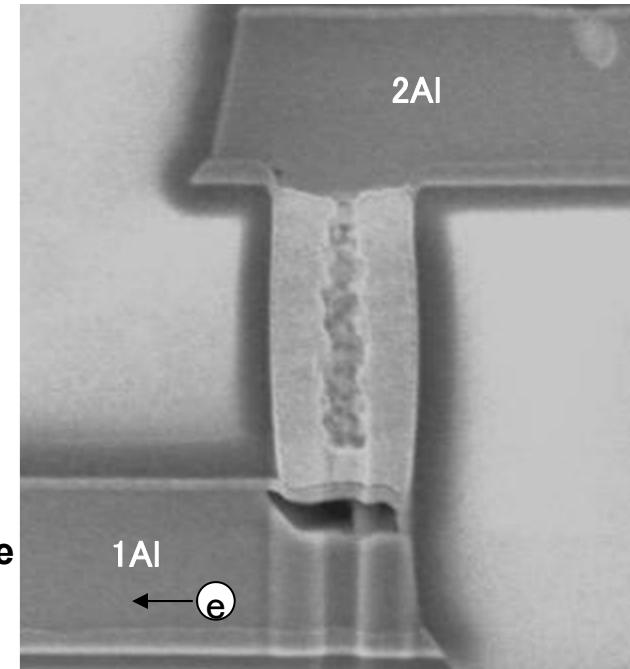


Cross-section after EM test  
 $T_a = 200^\circ\text{C}$ ,  $j = 1 \times 10^6 \text{ A/cm}^2$

## Electro-Migration mechanism(2)



Aluminum electro-migration  
along with grain boundary



Aluminum electro-migration at via

# **What is the Stress-migration?**

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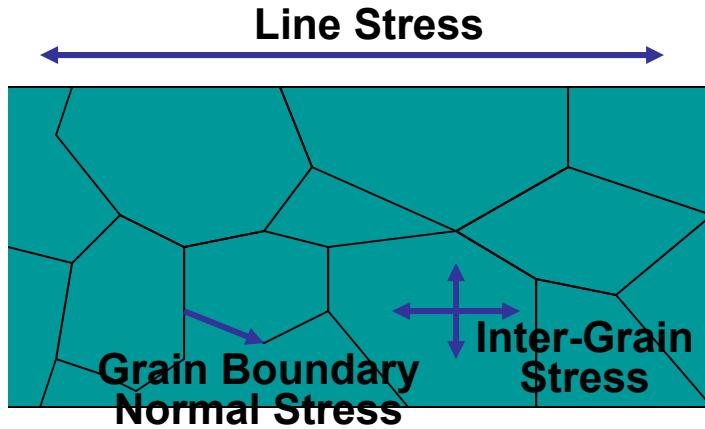
**Stress Migration is a failure mechanism that often occurs in Aluminum or Copper.**

**Voids form as result of vacancy migration driven by the hydrostatic stress gradient.**

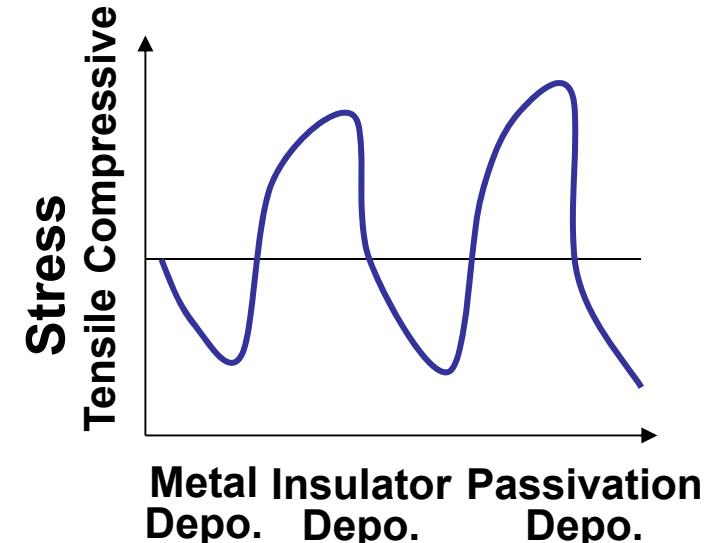
**Large voids may lead to open circuit or unacceptable resistance increase that degrades the LSI performance.**

# Schematic of Stress-Migration in bamboo structure.

Mean grain size of Al  
< Wire width



Mean grain size of Al  
≥ Wire width



**Bamboo structure** (Lower SM resistance)

**A phenomenon when wire becomes Bamboo structure, voids are generated along with grain boundary due to in process heat histories.**

# Reference for self-studying

- ◆ SILICON VLSI TECHNOLOGY
  - Fundamentals, Practice and Modeling —  
by J.D. Plummer, M.D. Deal and P.B. Griffin  
Pearson Prentice Hall, 2000 ( > \$ 100 ? )
  
- ◆ Modern Semiconductor Devices for Integrated Circuits
  - by Chenming Calvin Hu  
Pearson Prentice Hall, 2010 ( \$ 40 )

