Chip Layout Design

November, 2013

Renesas Technology Corp.

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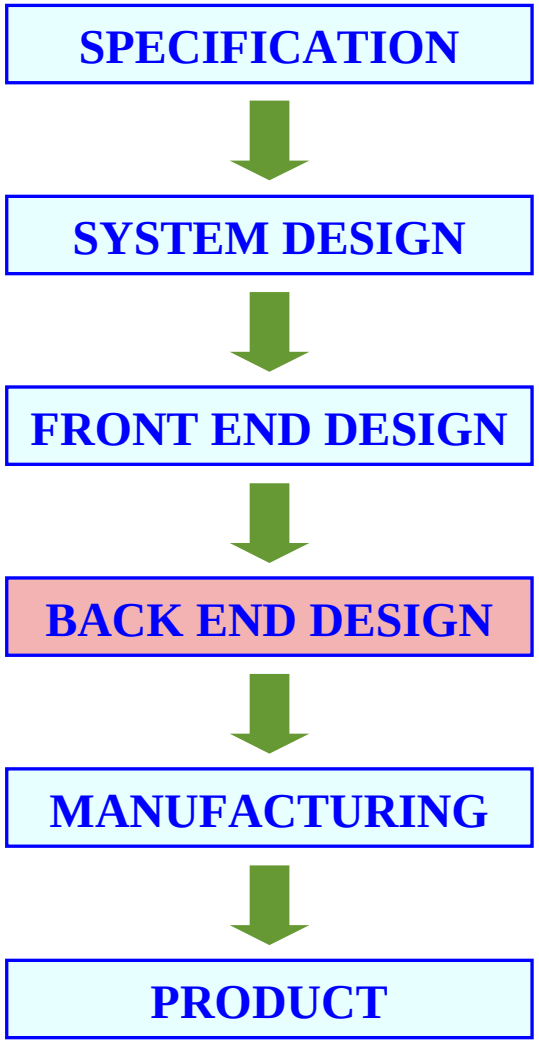
1/ Position of Chip layout design in SoC Design Flow

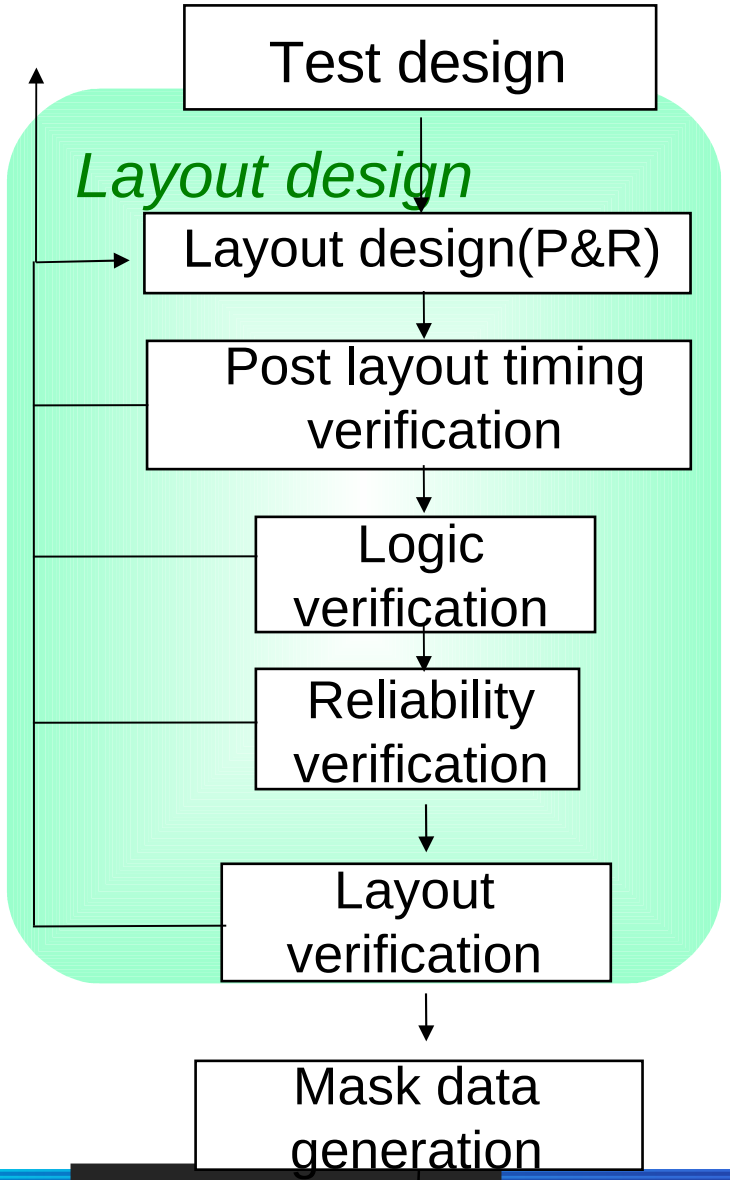


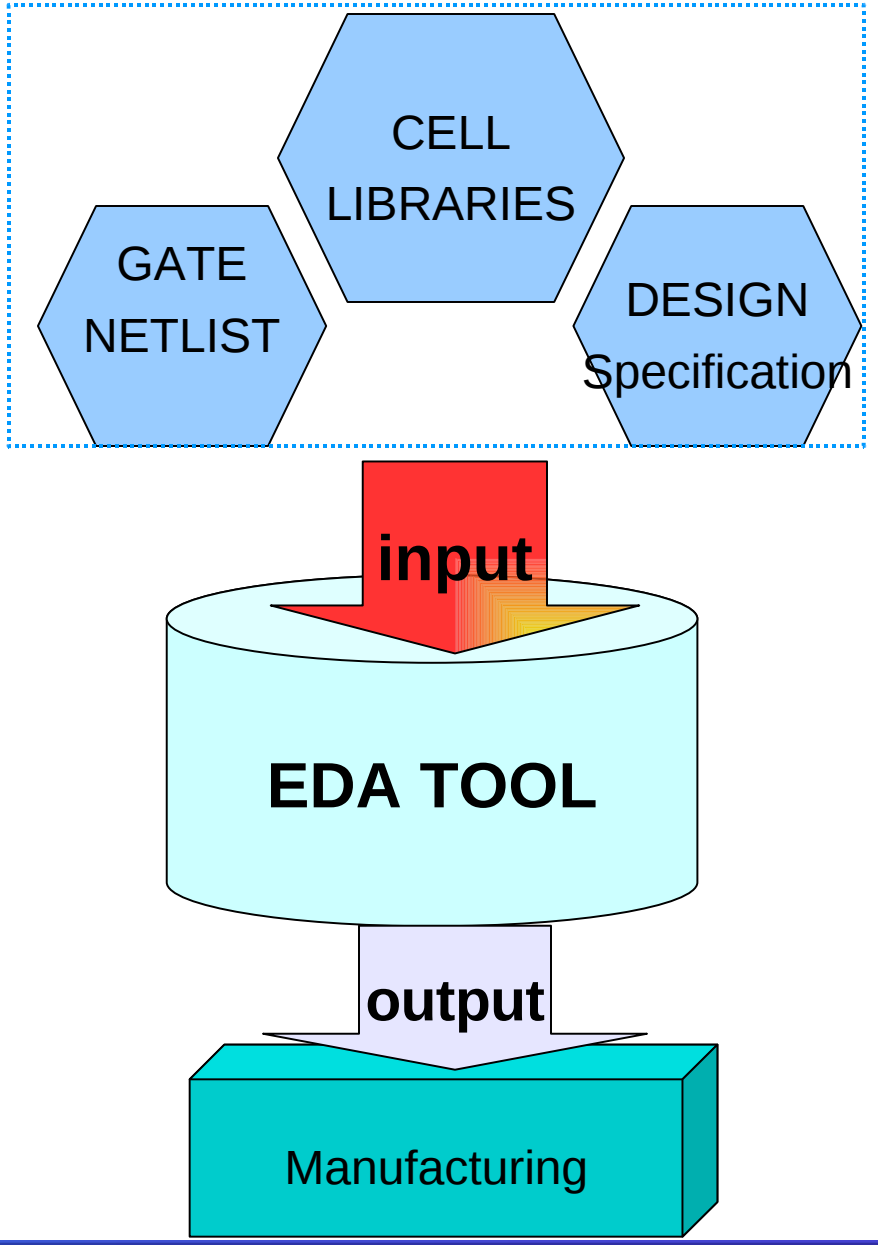
Chip layout design : Backend design

SoC : System on Chip

1/ Position of Chip layout design in SoC Design Flow

Chip Layout design flow



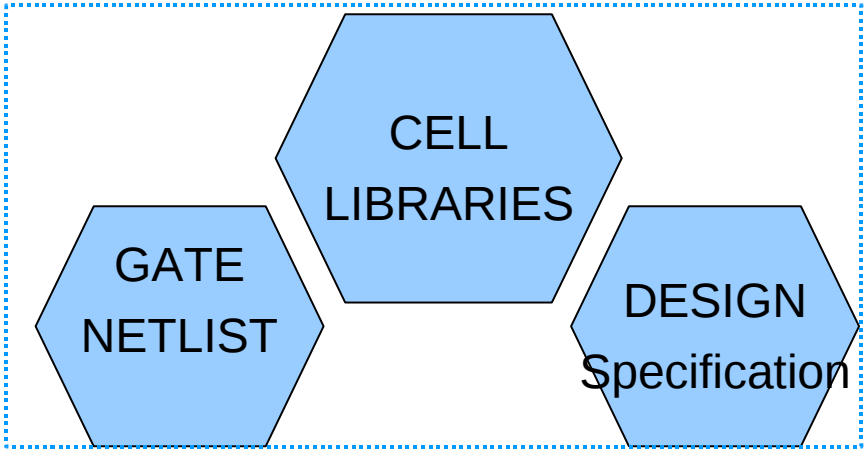


1/ Position of Chip layout design in SoC Design Flow

Chip Layout design flow

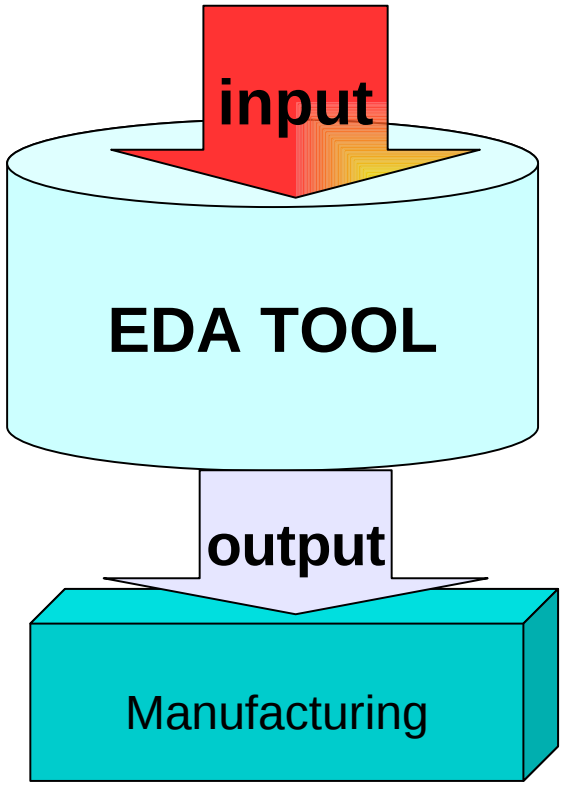
GATE NETLIST

Verilog gate from logic team (.V)



DESIGN Specification

Specification from customer:
- CPU speed
- GPU
- Technology 45nm, 28nm ..
- Chip size
....



2/ What is a Cell?

A cell is macro or functional unit that performs common operations and is used to build more complex logic blocks.

Example of cells: Inverter, NAND, NOR, Flip-Flop, latches and buffers.

3/ What is a cell library?

A cell library often refers to a collection of cells.

- Standard cell library (Primitive cell Library)
- I/O cell library
- Memory (Compiled memory, Fixed size memory)
- Analog (AD converter, DA converter, PLL,etc)

3/ What is a cell library?

Cell library consists of :

- Schematics (Transistor level circuits.Usually, not released)
- Frontend model (Verilog, VHDL, Liberty(.DB), other support libraries)
- Backend Model (LEF,ASTRO, GDS(Layout), CDL) :

  LEF and ASTRO are cell information which shows locations of ports, cell size, and prohibited area for wiring.

  + LEF is for Cadence P&R tool
  + ASTRO is for Synopsys P&R tool.
  + GDS is for manufacturing
  + CDL is a netlist for the verification of Layout versus Schematics (LVS).

3/ What is a cell library?

Example of Verilog model:Inverter(Portion)

```
`ifdef TS_OFF
`else
 `timescale 1ps/1ps
`endif
`celldefine
`ifdef verifault
  `suppress_faults
  `enable_portfaults
`endif

`ifdef FAST_FUNC
 `delay_mode_zero
`else
 `delay_mode_path
`endif

module TCAINVXC( A,YB );
output YB;
input A;
reg notifier;

not  (YB,A);

`ifdef FAST_FUNC
`else
…….
```

3/ What is a cell library?

Example of Liverty(.lib):Inverter(Portion)

```
cell(TCAINVXC){
 area : 3.0;
 cell_leakage_power : a;
 cell_footprint : INVX_;
 pin(YB){
  function : "!(A)";
  max_fanout : 50;
  max_capacitance : b;
  capacitance : 0.000000;
  direction : output;

  internal_power() {
   related_pin : "A";
   fall_power(pwr_tin_oload_3x3){
    index_1 (“ ,  ,  ");
    index_2 (“ ,  ,  ");
    values(“ ,  ,  ",   \
           "- ,  ,  ", \
           “ ,  ,  ");
   }
   rise_power(pwr_tin_oload_3x3){
    index_1 (“ ,  ,  ");
    index_2 (“ ,  ,  ");
    values(“ ,  ,  ",   \
           “ ,  ,  ", \
           “ ,  ,  ");
   }
  }
```

Usually, .lib is not released.
.DB is released, which is read by Tools.

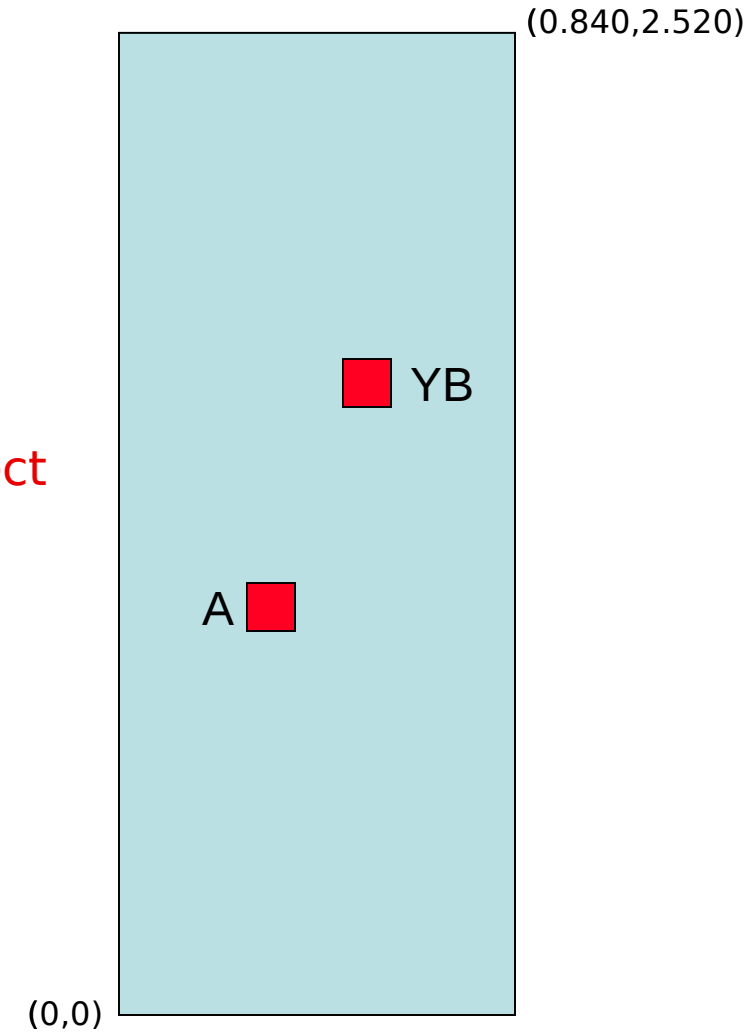
Actual numbers are deleted form original .lib

3/ What is a cell library?

Example of LEF:Inverter(Portion)

```
MACRO TCAINVXC
CLASS CORE ;
  FOREIGN TCAINVXC 0.000 0.000 ;
  SIZE 0.840 BY 2.520 ;
  SYMMETRY Y X ;
  ORIGIN 0.0 0.0 ;
  SITE CORE009 ;
  PIN A DIRECTION INPUT ;
      USE SIGNAL ;
       AntennaGateArea 0.144000 LAYER M1 ;
       AntennaPartialMetalArea 0.104400 LAYER M1 ;
      PORT
        LAYER M1 ;
        RECT 0.170 0.970 0.350 1.550 ;
      END
  END A
  PIN YB DIRECTION OUTPUT ;
      USE SIGNAL ;
       AntennaPartialMetalArea 0.242200 LAYER M1 ;
       AntennaDiffArea 0.331200 LAYER M1 ;
      PORT
        LAYER M1 ;
        RECT 0.490 0.380 0.630 2.110 ;
      END
  END YB
.....
```

Antenna Effect



3/ What is a cell library?

Example of CDL: Inverter

```
.SUBCKT TCAINVXC A YB
XI2 A YB VDD VSS / TCXINV wn=aaa u wp=bbb u
XI0 A YB VDD VSS / TCXINV wn=ccc u wp=ddd u
.ENDS
```

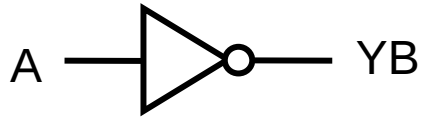
aaa~ddd is MOS size

4/ Cell layout

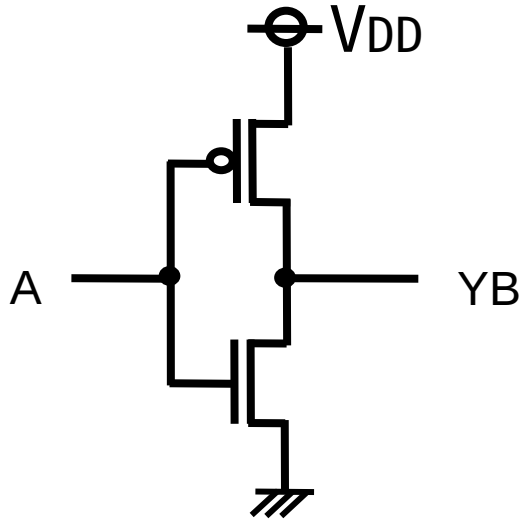
1std cell is formed by many transitors which connect together

Cell Example:Inverter

Logic Symbol

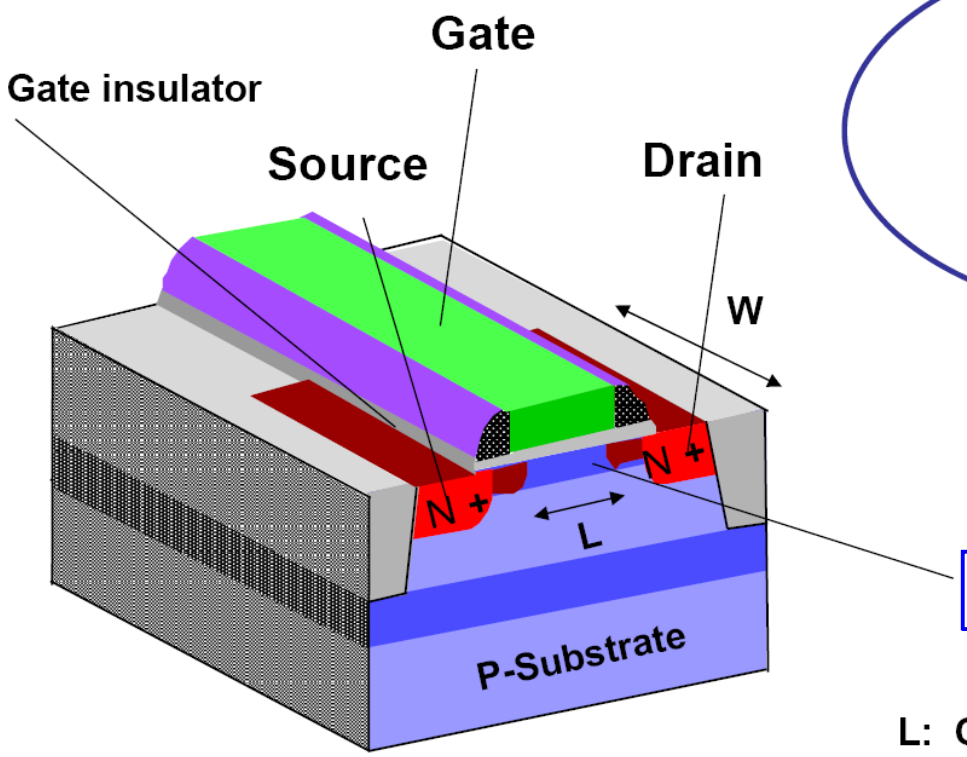


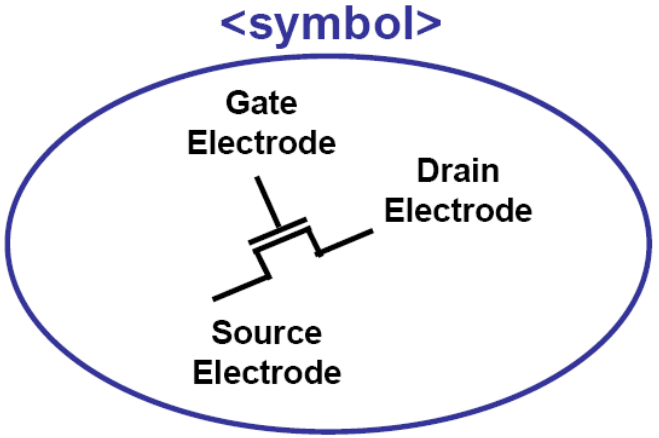
Circuit



4/ Cell layout

3D-image Transitor





Channel or diffusion area

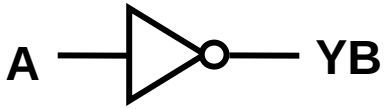
N+: heavily doped silicon
= low resistive electrode

L: Channel length
W: Channel width
FET: Field Effect Transistor

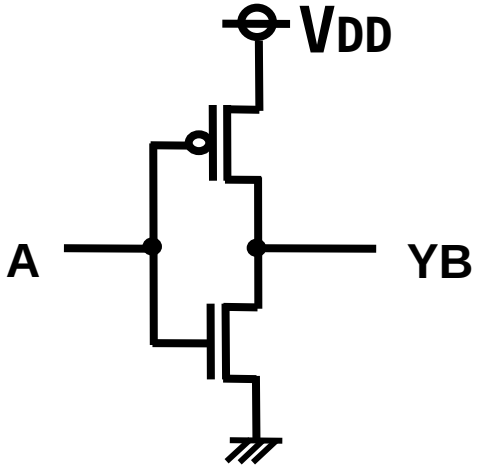
4/ Cell layout

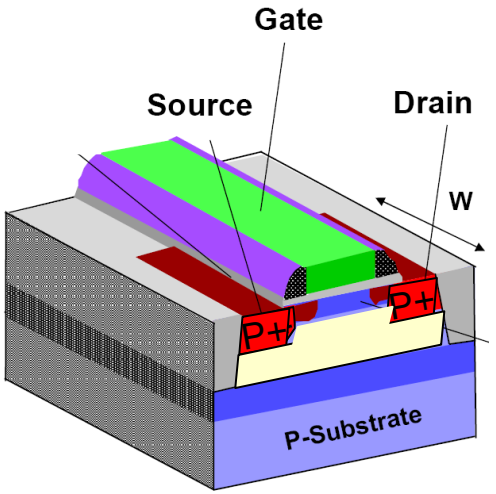
Cell Example:Inverter

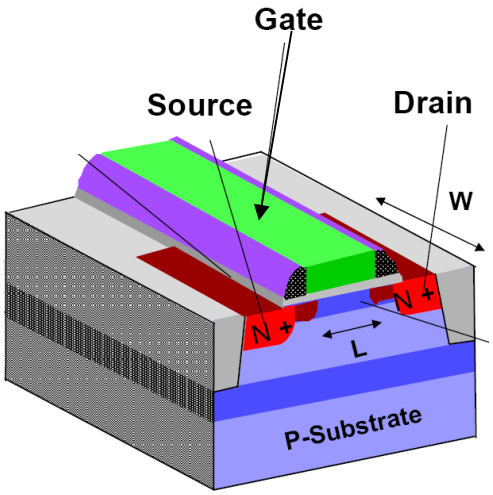
Logic Symbol

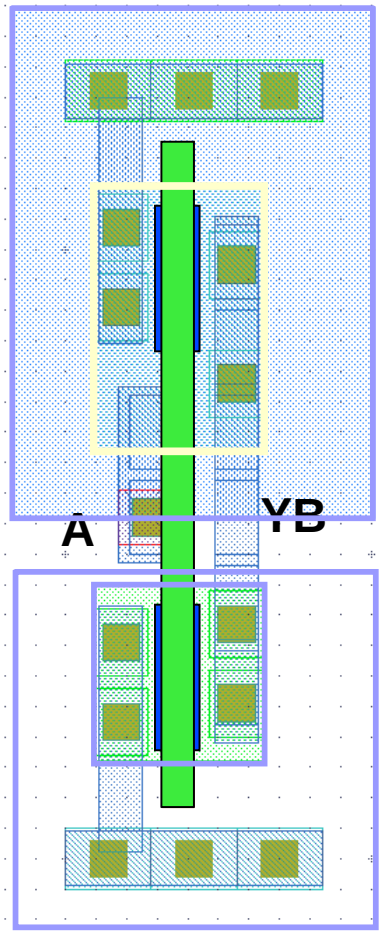


Circuit









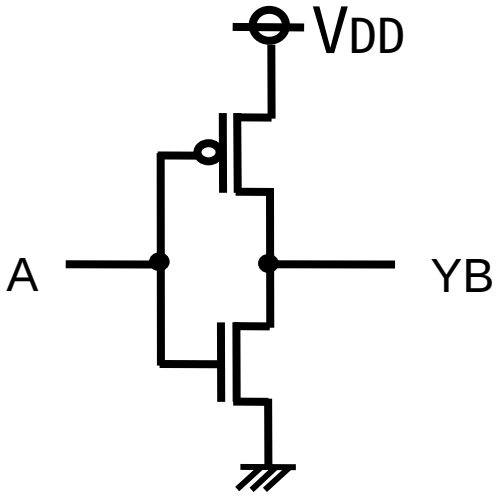
4/ Cell layout

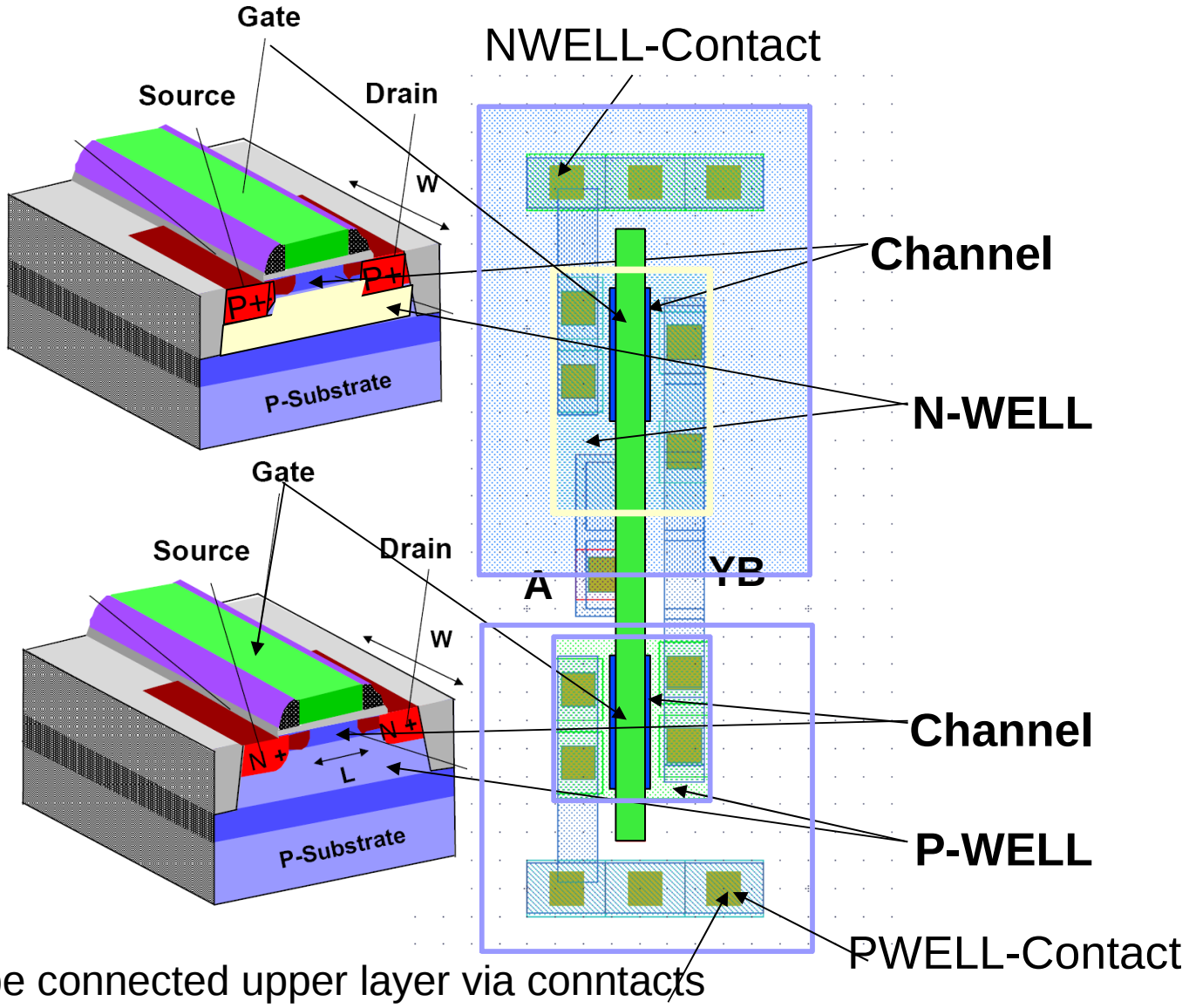
Cell Example:Inverter

Truth Table

Input	Output
A	YB
L	H
H	L

Circuit

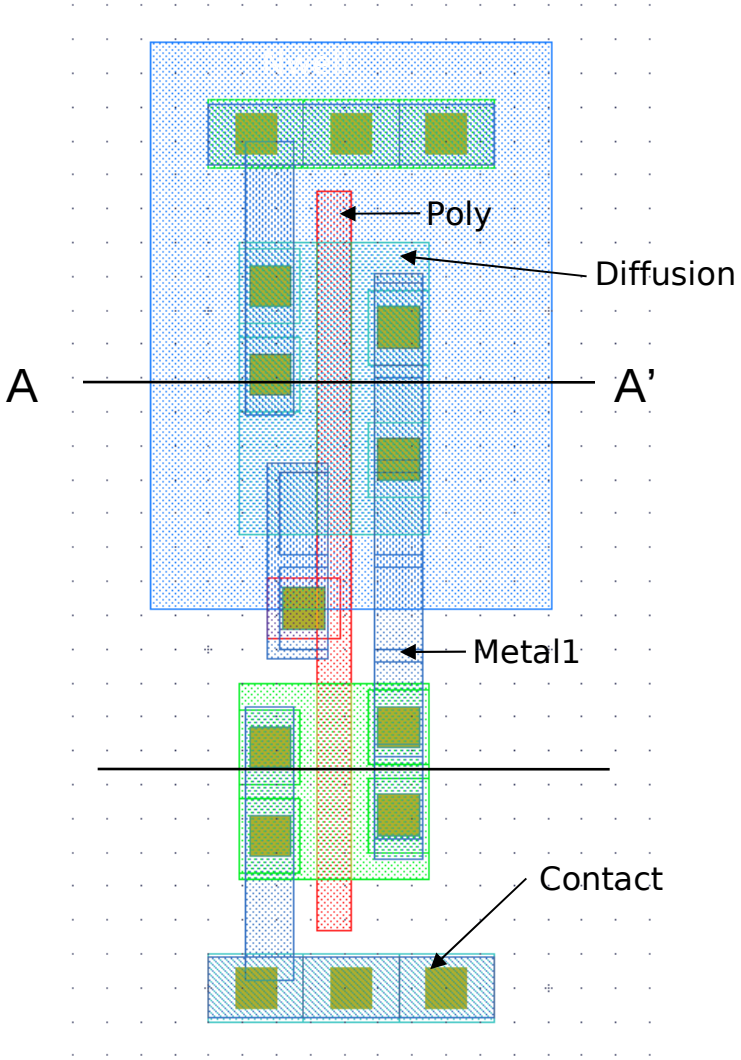


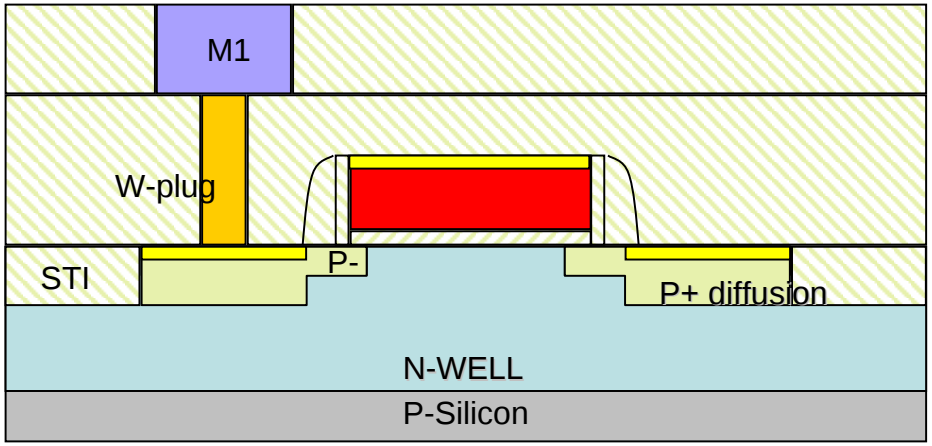


Drain/source pins will be connected upper layer via conntacts

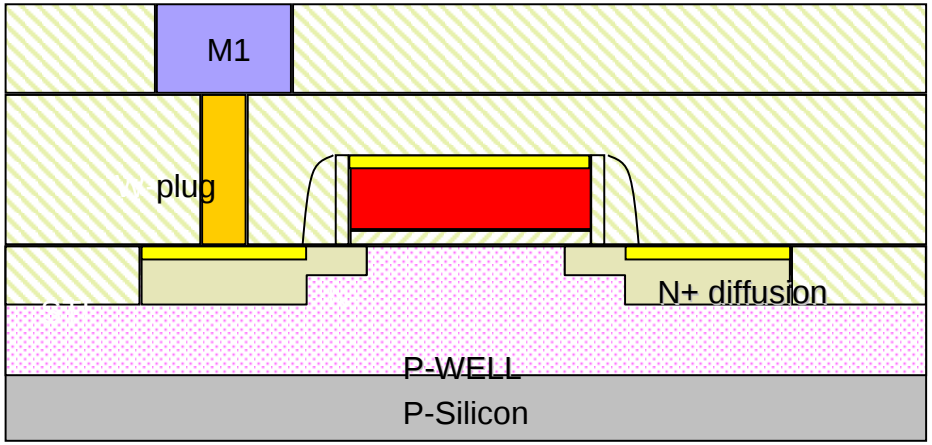
4/ Cell layout

Cross-section of Cell





The cross-section at A-A'.



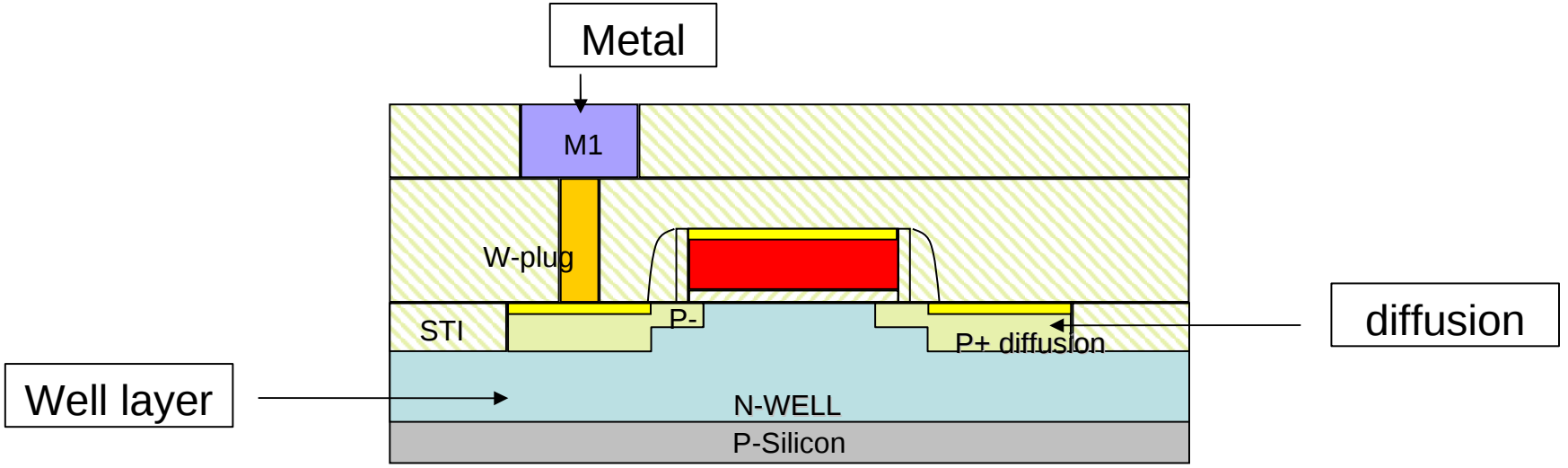
The cross-section at B-B'.

4/ Cell layout

LAYERS AND CONNECTIVITY

If we analyze most CMOS processes, we find that there are four basic layer types:

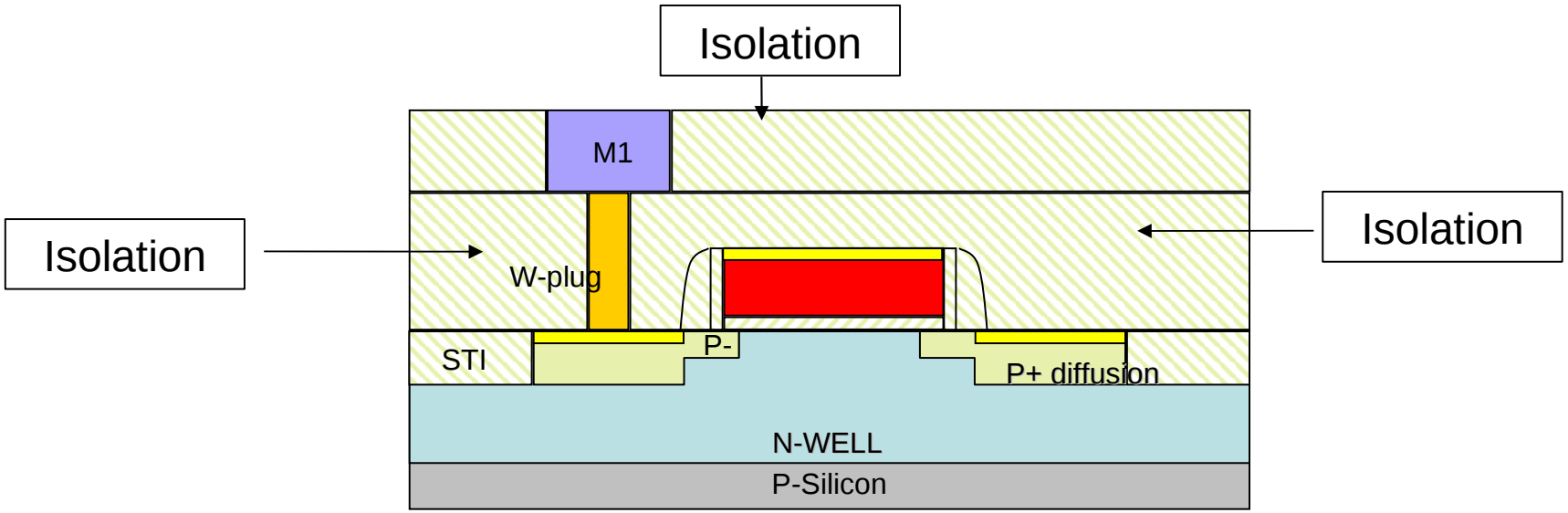
1 . Conductors: These layers are conducting layers in that they are capable of carrying signal voltages.
Diffusion areas, metal and polysilicon layers, and well layers are classified into this category.
For the cell layout, you need to consider the resistivity of each conductor. (metal< diffusion ~ poly<< well)



4/ Cell layout

LAYERS AND CONNECTIVITY

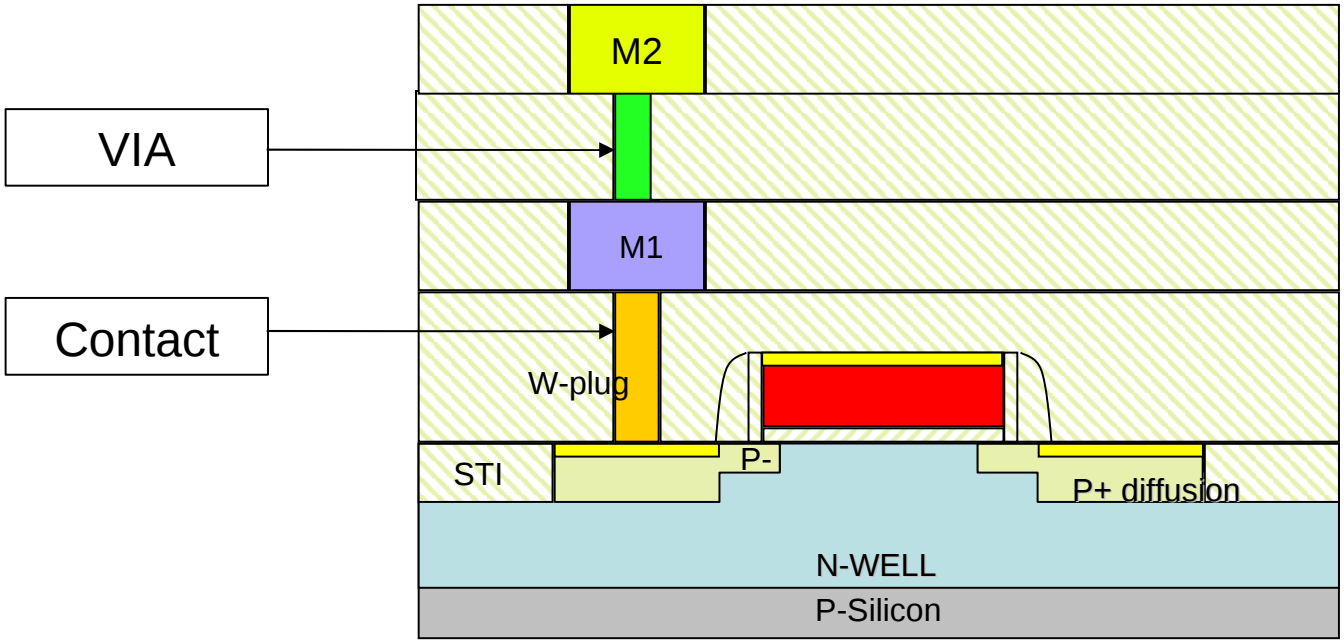
2. Isolation layers: These layers are the insulator layers that isolate each conductor layer from each other in vertical and horizontal directions.
   This isolation is required in both the vertical and horizontal direction to avoid "short circuits" between separate electrical nodes.



4/ Cell layout

LAYERS AND CONNECTIVITY

3. Contacts or vias: These layers define cuts in the insulation layer that separates conducting layers and allow the upper layer to contact down through the cut or "contact" hole. Metal vias or contacts are examples of these.



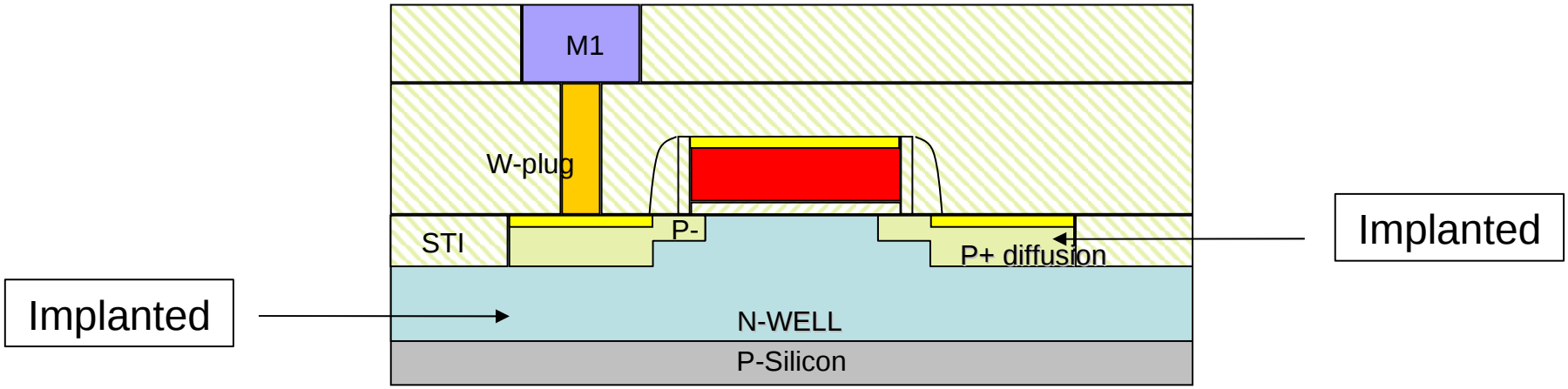
4/ Cell layout

LAYERS AND CONNECTIVITY

4. Implant layers: These layers do not explicitly define a new layer or contact, but customize or change existing conductor propriety. For example, diffusion or active areas for PMOS and NMOS transistors are defined simultaneously.

A P+ mask is used to create P+ implant areas that define certain diffusion areas to P-type by the use of a P-type implant.

Using a combination of these four types of layers, transistor devices, resistors, capacitors, and interconnections are created.



4/ Cell layout

LAYERS AND CONNECTIVITY

The mask layers, or the layer shapes that are translated to the optical masks, are sometimes different from the drawn layers. First, there may be many more mask than drawn layers. In this case, the additional mask layers are automatically generated from the drawn layers.

Additionally, the mask layers may be resized from the drawn layers to account for variances in the manufacturing process. This resizing is also done automatically by the mask-making process.

Note that isolation layers are never drawn but are always implied from the mask layers as part of the manufacturing process.

4/ Cell layout

INTRODUCTION TO TRANSISTOR LAYOUT

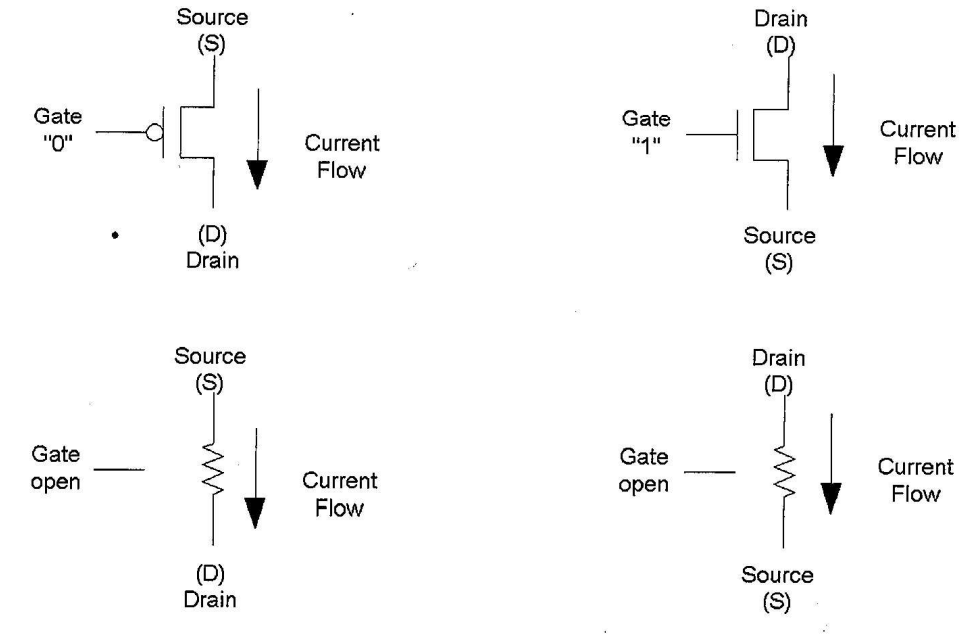
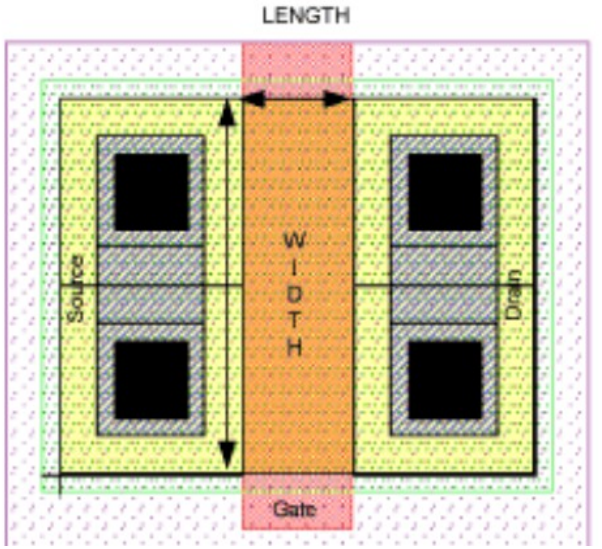


Fig. 6 PMOS and NMOS Transistors



Transitor layout from top view

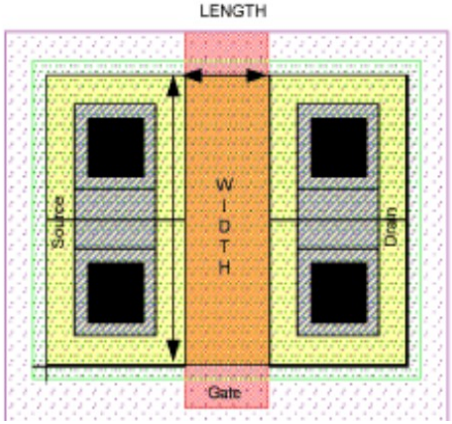
The top half of Figure 6 shows
the basic symbol representations of both
PMOS and NMOS transistors.

4/ Cell layout

INTRODUCTION TO TRANSISTOR LAYOUT

The length and width of a transistor are the two most important dimensions of a transistor .

When we talk about the gate size of a specific technology, they are referring to the minimum gate length.

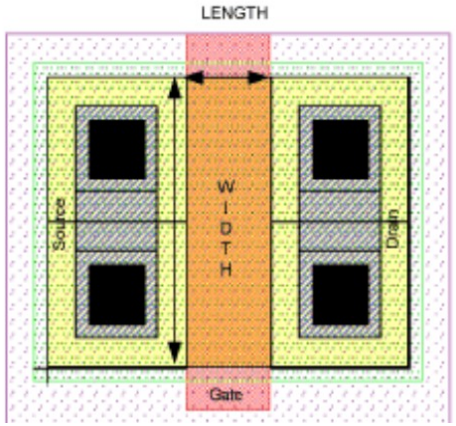


4/ Cell layout

INTRODUCTION TO TRANSISTOR LAYOUT

-In terms of layout design, the length of the transistor is the distance between the source and the drain of a transistor.

-The length of a transistor in terms of manufacturing capabilities is the narrowest possible piece of polysilicon (poly) that can be manufactured reliably. Smaller poly dimensions and thus smaller transistors results in smaller ICs, so it is attractive to use the minimum gate length to minimize chip area.



4/ Cell layout

INTRODUCTION TO TRANSISTOR LAYOUT

The first important thing to remember is the difference between the length and width of a transistor and how to apply this to transistor layout!

Figure 8 shows the layout of an NMOS transistor.

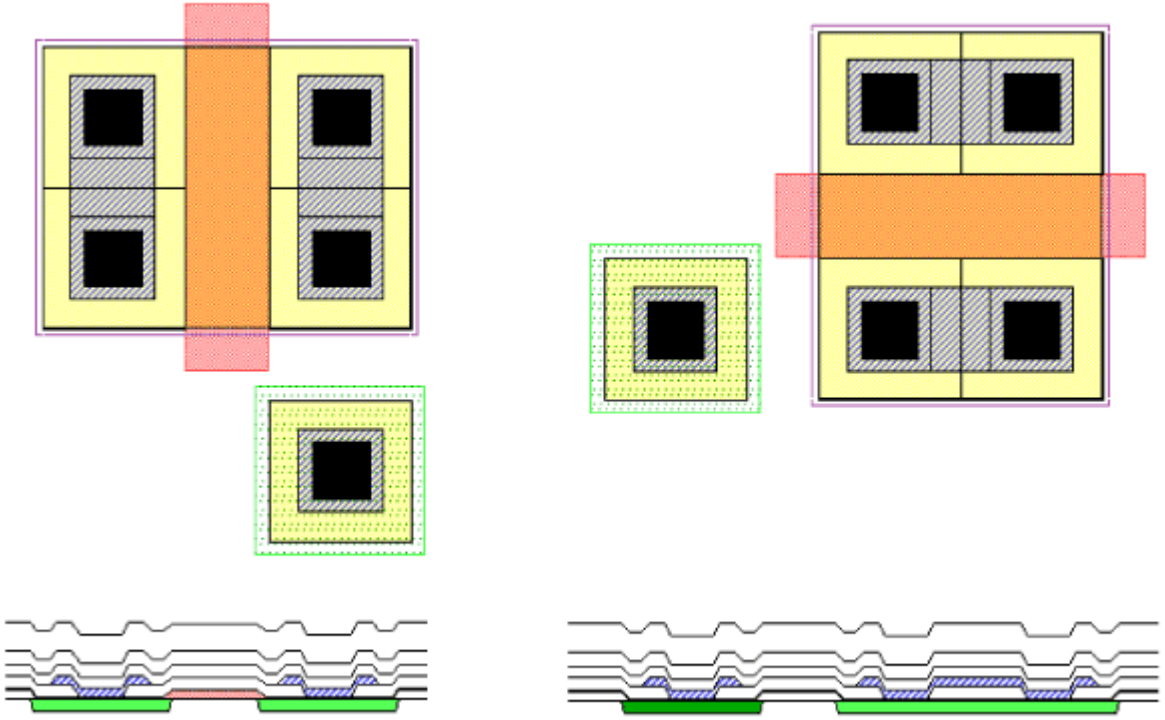
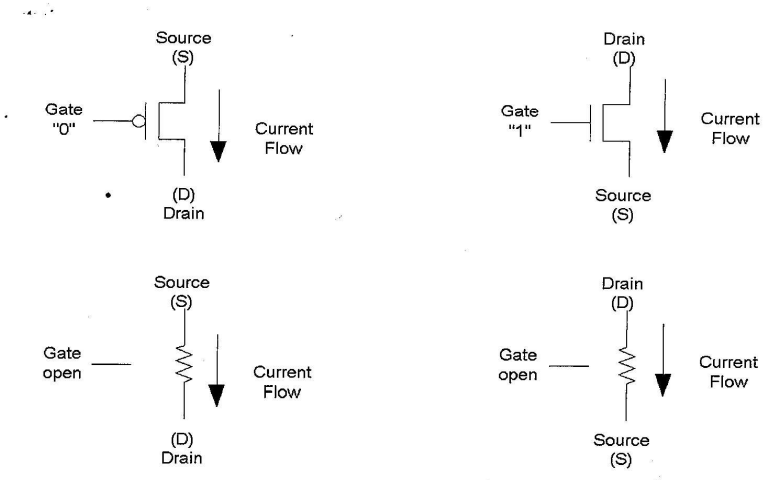


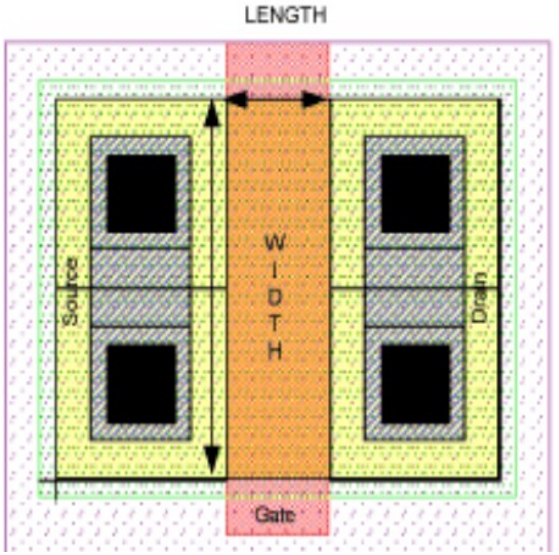
Fig. 8 Simple NMOS transistor layout

4/ Cell layout

INTRODUCTION TO TRANSISTOR LAYOUT

- In terms of transistor performance, the length of the transistor is the distance electrons have to travel when the gate is "on" or "open" to produce a measurable current flow. (Effective Channel Length)
  Remember, it is the gate voltage that controls the flow of current.
  If the distance between the source and drain is reduced, the gate voltage has a stronger influence in enabling current flow.





4/ Cell layout

INTRODUCTION TO TRANSISTOR LAYOUT

The amount of current flow is determined by the device size.

The current flow is increased as the width of the device is increased or the length of the device is decreased.

Figure 7 shows a simple MOS transistor layout.

The equation of Saturation current

$$Id = \frac{W}{2L}\mu\, Cox\, (Vg-Vth)^2$$

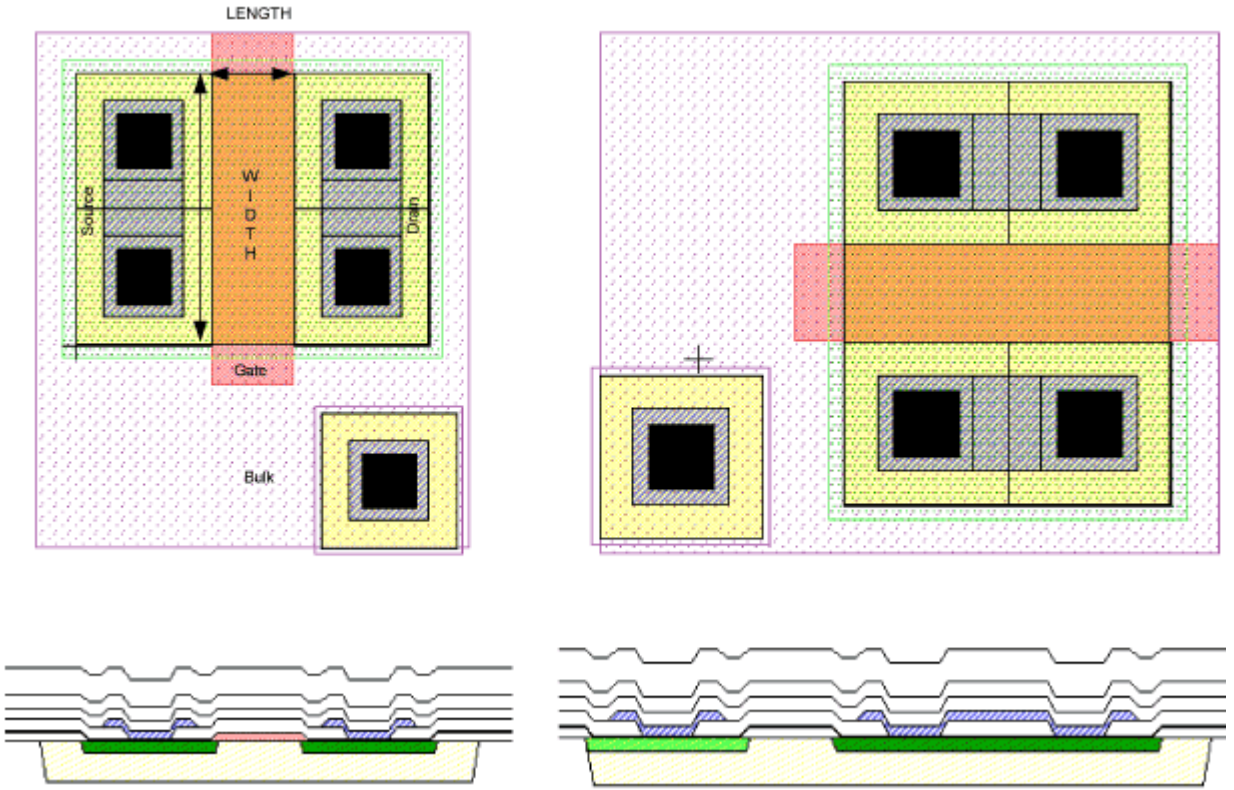
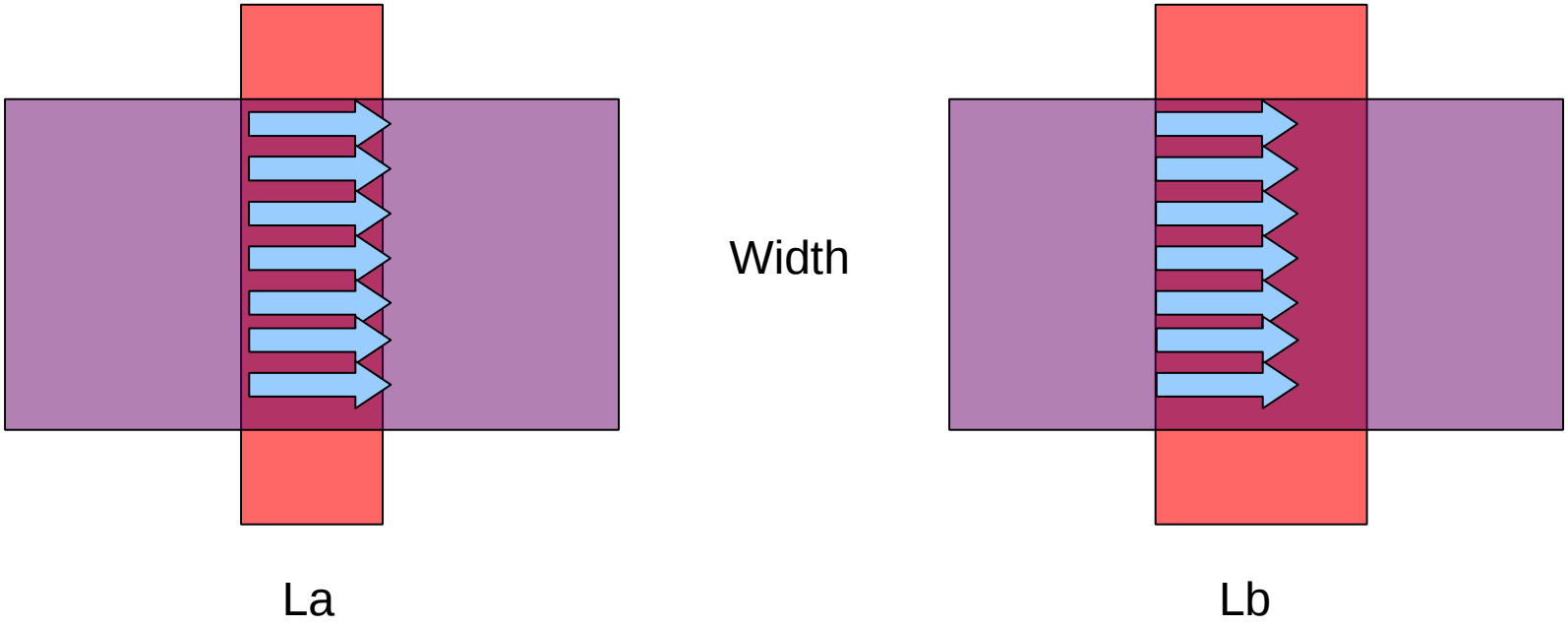


Fig. 7 Simple PMOS transistor layout

4/ Cell layout

INTRODUCTION TO TRANSISTOR LAYOUT

- In the same process technology, if two transistors have the same width but different lengths, the transistor with the shorter gate length will produce more current.
More current conceptually means faster performance.

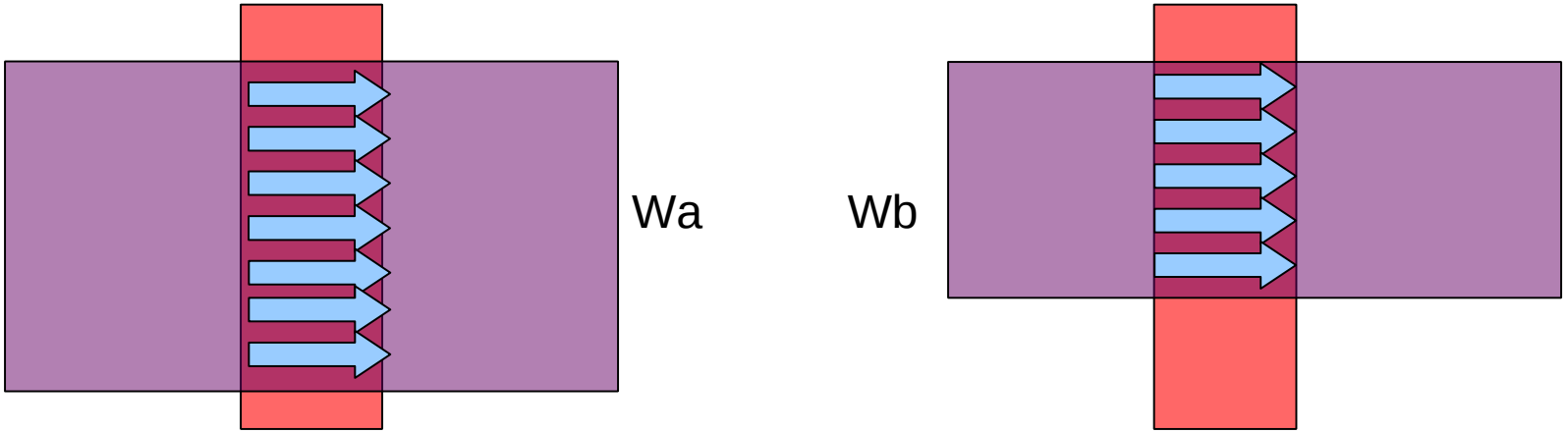


In the same period, the number of electrone move though La will be lagrer than moving through Lb

4/ Cell layout

INTRODUCTION TO TRANSISTOR LAYOUT

Let's now consider the width of a transistor.
The width of a transistor should be thought of as the number of parallel channels that are available for current to pass from the source to the drain.
Wider transistors have more channels available; more channels mean more current. Once again comparing two transistors, this time each having identical gate lengths but different gate widths, the transistor with the larger gate width will produce more current.



In the same period, the number of channel electrone move though La will be lagrer than moving through Lb

4/ Cell layout

Conductors and Contacts

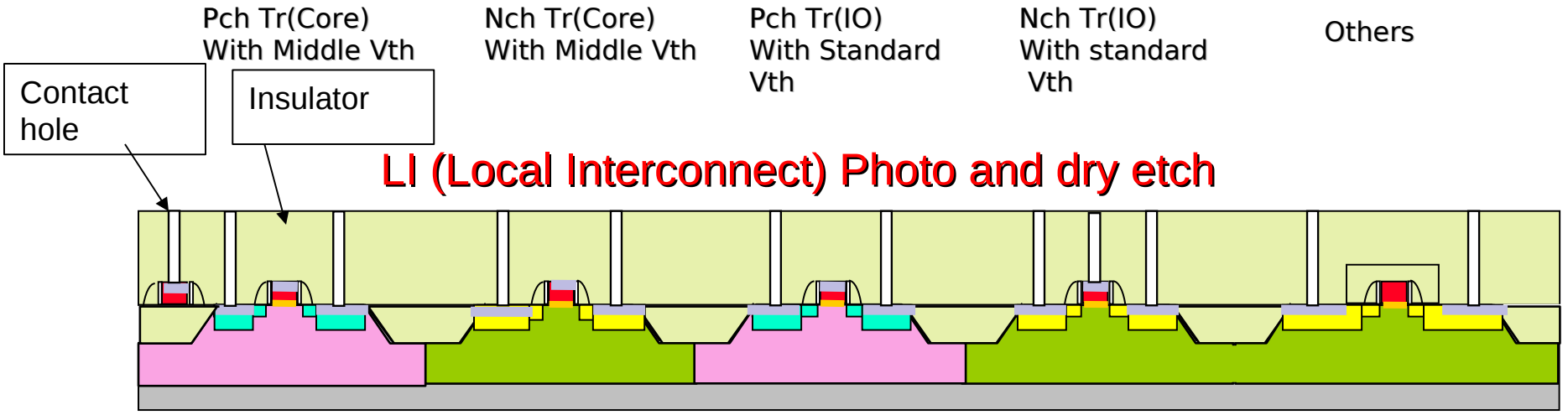
From a layout design point of view, conductors and contacts are straightforward.
Let's look at the formation of contacts from a manufacturing point of view so that as layout designers we can understand their use and limitations.

A typical SoC process has one type of polysilicon for the gate and two to four types of layers of metal for interconnection.
An advanced SoC process can have up to 10 layers of metal for interconnect and use a low-level metal called metal0 for source/drain connections (Local Interconnect).
A contact typically refers to the lowest level metal hole that contacts from the lowest level of metal to the polysilicon or diffusion layers. The holes that allow higher layers of metal to connect between each other (e.g., metal1 to metal2 or metal2 to metal3) are called "vias" or "through holes" .

4/ Cell layout

Insulator deposition and Contact hole formation

SiN and CVD-Oxide are deposited as the insulator.
Contact holes for poly silicon and diffusion are opened through the Insulator.

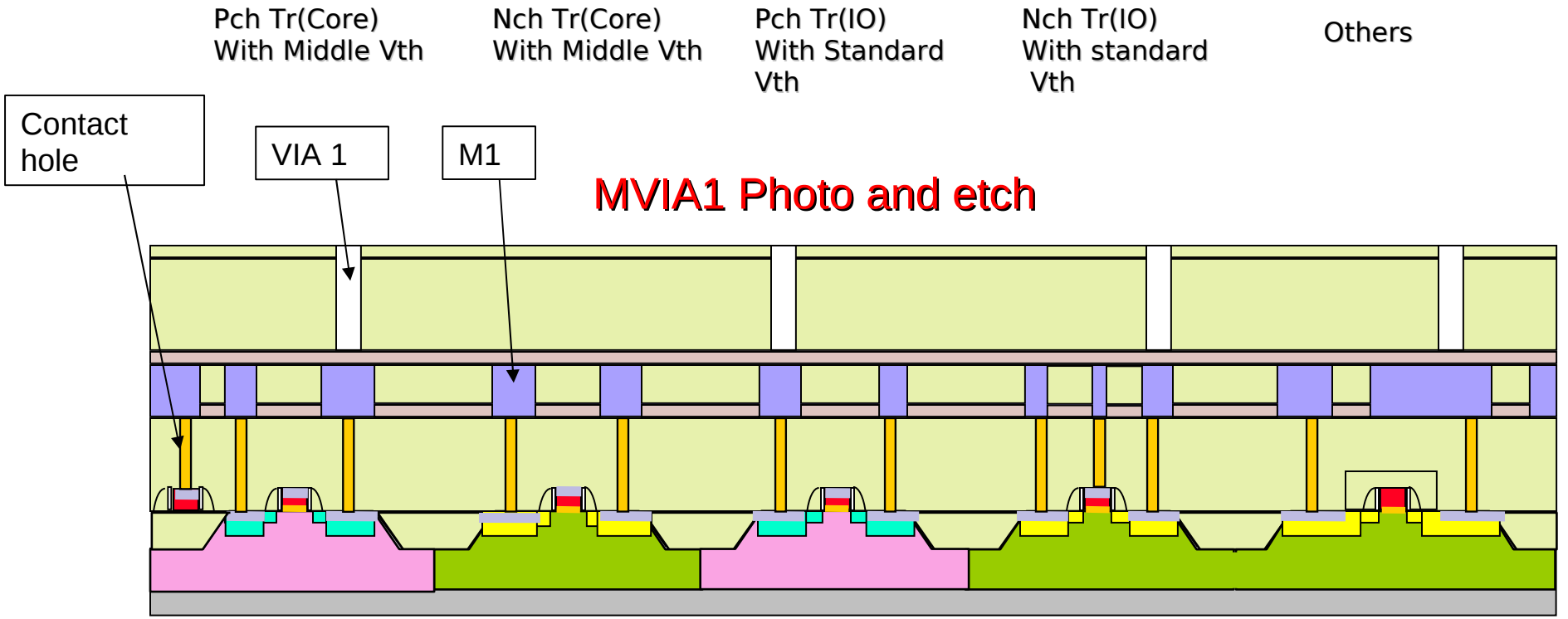


Note: Renesas Design Rule does not allow contact hole on gate.
The above figure shows only for the explanation.

4/ Cell layout

Insulator deposition and Via1 formation

Etching stopper and insulators between Metal1 and Metal2 are deposited.
Via1 is opened.



4/ Cell layout

Conductors and Contacts

In most cases there is a distance to respect between the "contact" hole and the "via" hole, but in most modern processes the via can be placed on top of the contact. In some very complicated processes where the chip size is very important, the process may allow all the vias to be aligned one on top of each other.
They are called "stacked" via processes.

Each metal has various characteristics in terms of resistance (R), capacitance (C) and topology requirements. Something to think about is that the higher metal layers in the process require more vias to connect down to the transistor layers. These vias add resistance. We need to analyze these electrical characteristics of the process.

4/ Cell layout

Exercise

Ids of unit width for NMOS is 20uA/um.
One contact can flow 50uA/piece.
Metal can flow 20uA/um width.
When you design cell which needs current flow of 200uA,
How many contact holes do you need to layout?
And which metal width do you draw?

4/ Cell layout

Exercise-Ans

Ids of unit width for NMOS is 20uA/um.
One contact can flow 50uA/piece.
Metal can flow 20uA/um width.
When you design cell which needs current flow of 200uA,
How many contact holes do you need to layout?
And which metal width do you draw?

Diffusion Width=200uA/20uA(per um), then width=10um
Idsmax=200uA, then 200uA/50uA(per contact)
→4 contacts for each diffusion.
Metal width 200uA/20uA(per um), then width =10um.

4/ Cell layout

PROCESS DESIGN RULES

Design rules are the rules that have to be respected when a given design is laid out. There are design rules for all of the components we have been introduced to:
polygons and paths, transistors, and contacts. Fundamentally, these design rules represent the physical limits of the manufacturing process.

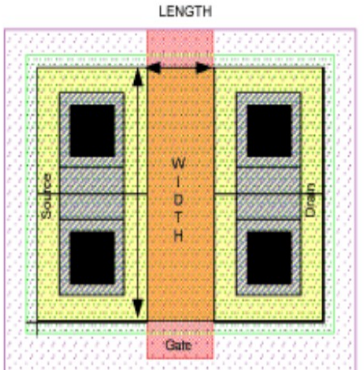
There are a lot of Rule in manufactoring phase, now we will investigate 3 basic rule:

- Width Rule
- Space Rule
- Overlap Rule

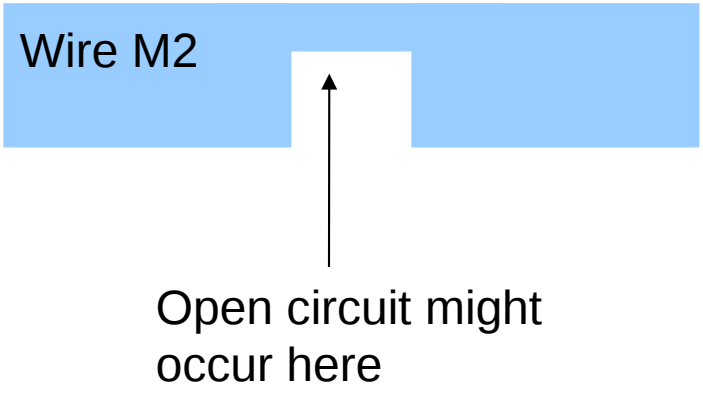
4/ Cell layout

Width Rule

The minimum width of a polygon (during mask-making; all paths are converted to polygons) is a critical dimension, which defines the limits of the manufacturing process.
The minimum gate length of a transistor is the prime example of this rule.



A violation in a minimum width rule potentially results in an open circuit in the layer.



4/ Cell layout

Width Rule

In addition to single polygons, width rules can also be applied to structures such as transistors or to single polygons with electrical or other special characteristics.

An example of a polygon with special electrical characteristics is a metal layer that is connected to a power supply. (Electro Migration)
Large currents passing through a narrow metal track cause the track to act like a fuse, and over time or during a large current peak the metal polygon will break under the stress.

The width of M1 should be wide enough to prevent th Electro Migration

4/ Cell layout

Width Rule

The length of a polygon (or path) is usually unlimited; however, in some processes there may be rules about minimum area requirements (for example, in the case of a contact or via where a width and a length rule together must be met).

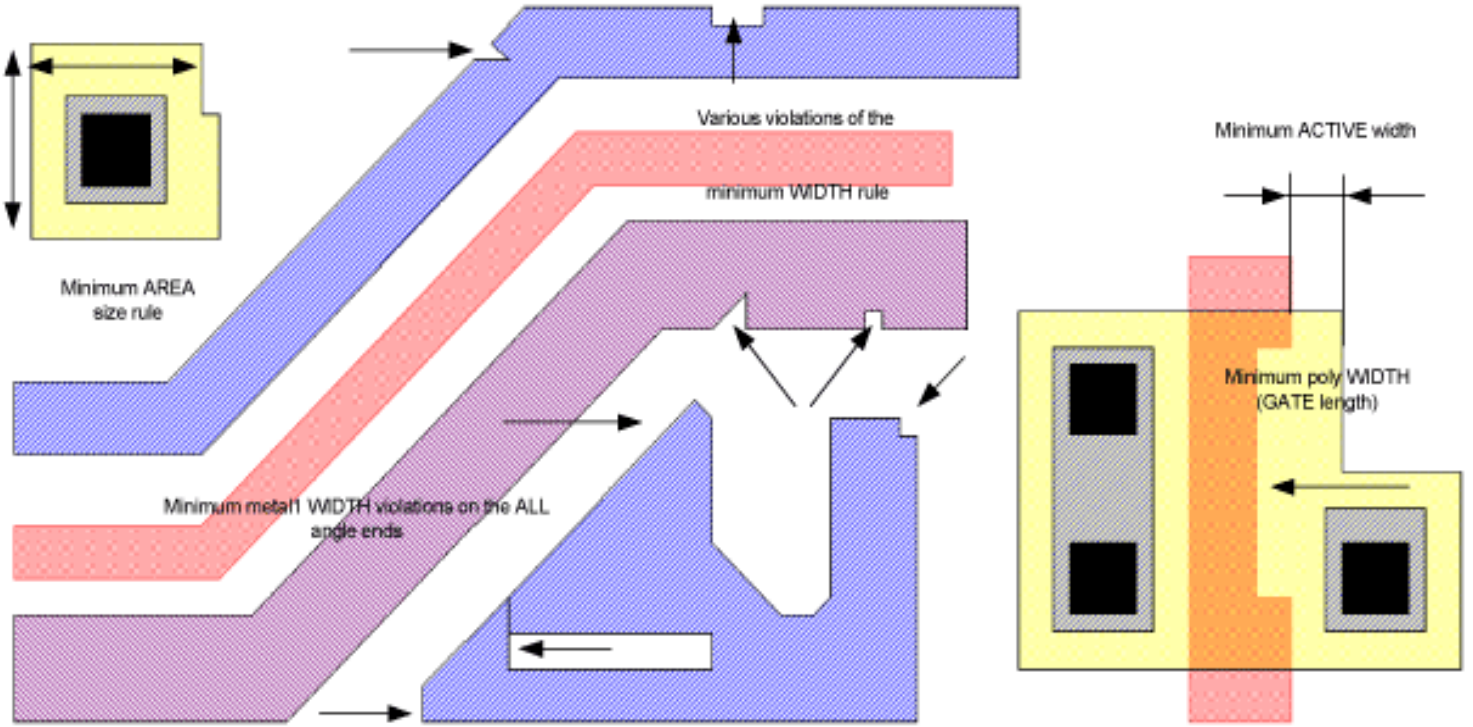
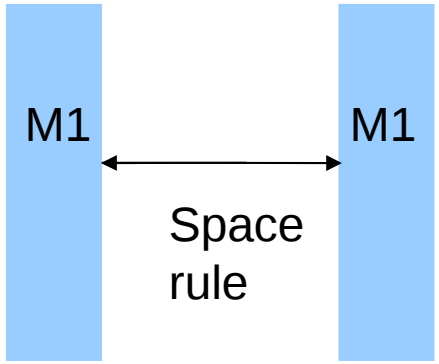


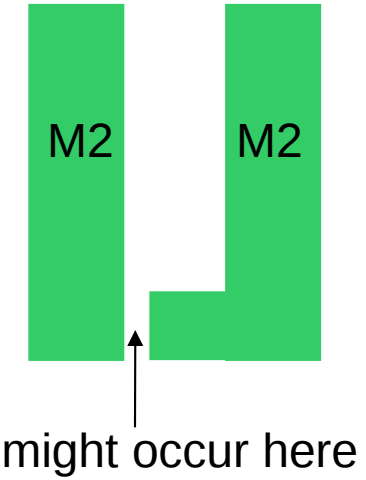
Fig. 13 Example of width rule

4/ Cell layout

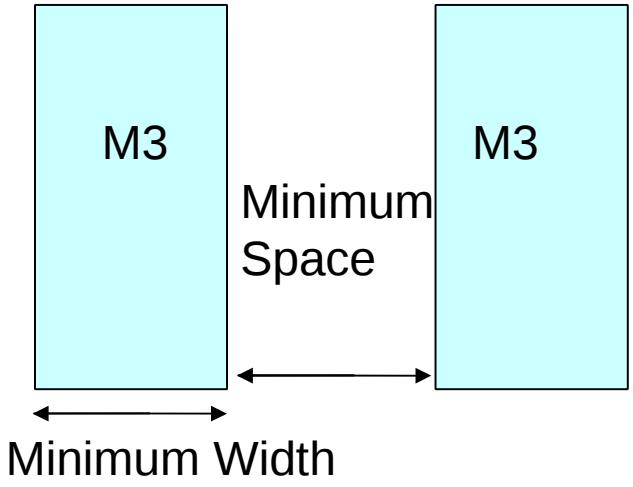
Space Rule

Another critical dimension is the space rule, which is the minimum distance between two polygons.
Generally, the space rule is applied to avoid an unwanted short circuit between the two polygons.





Together with the width rule on a single layer, the space and width rules define a layer pitch.
Minimum Width = Minimum Space = Layer pitch
Ex: T28nm layer pitch = 0.05 um

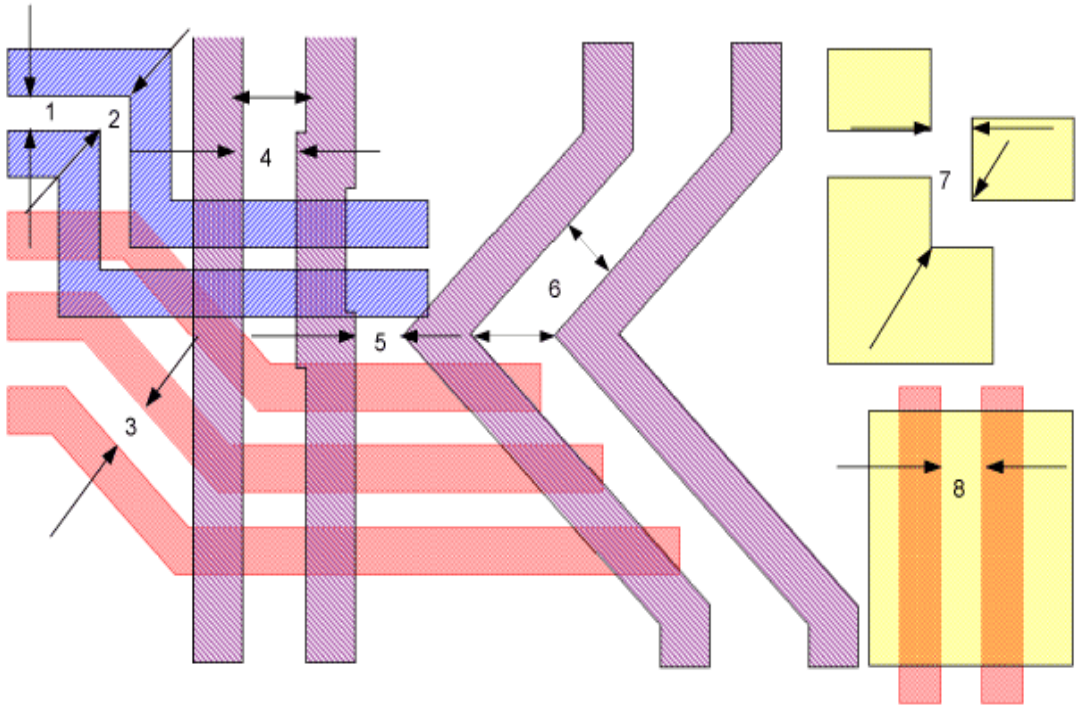


4/ Cell layout

Space Rule

Below Figure illustrates some exmaple of space rules :

- 1 and 2 are examples of the metal1 to metal1 minimum space rule checked in parallel and diagonally between corners.
- 3 is an example of the poly to poly space rule where the polygons are running in parallel at a 45-degree angle.
- 4, 5, and 6 are spacing rule examples related to metal2 to metal2 spacing for polygons at a 90- and 45-degree angle.



4/ Cell layout

Space Rule

- 7 is an example of the active to active spacing rule checked with a single distance (top example) or within a corner (bottom example).
- 8 is an exception to example 3-the spacing rule between two polysilicon polygons may depend on their location.

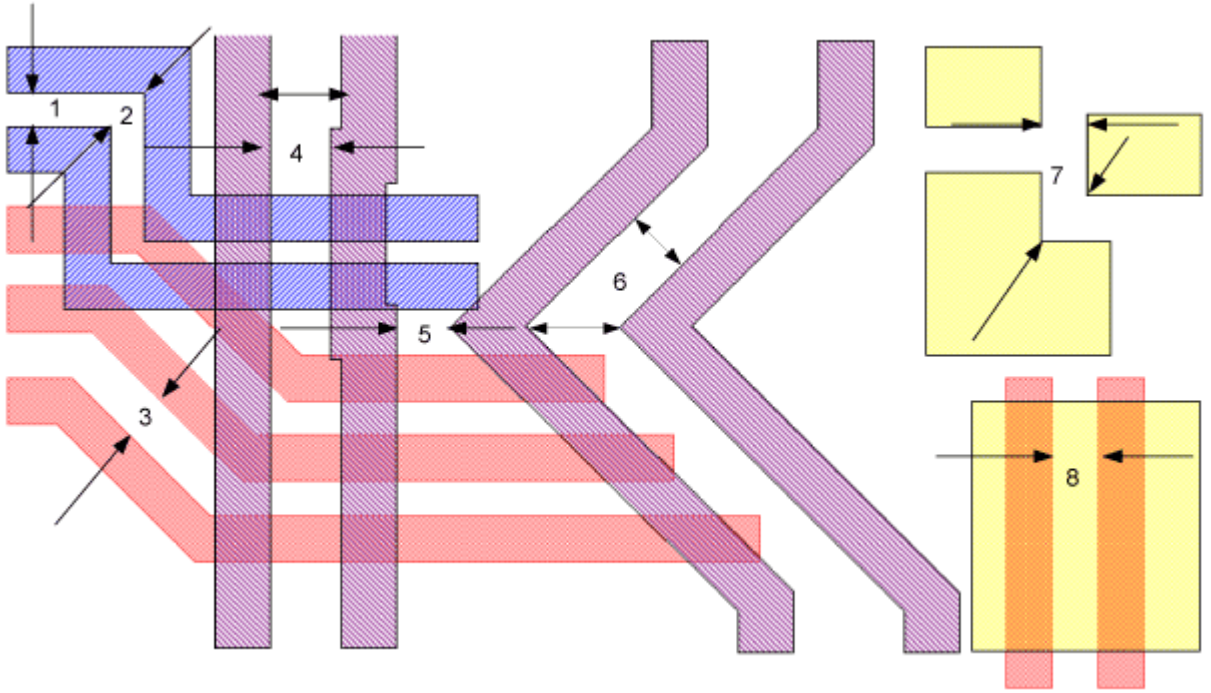
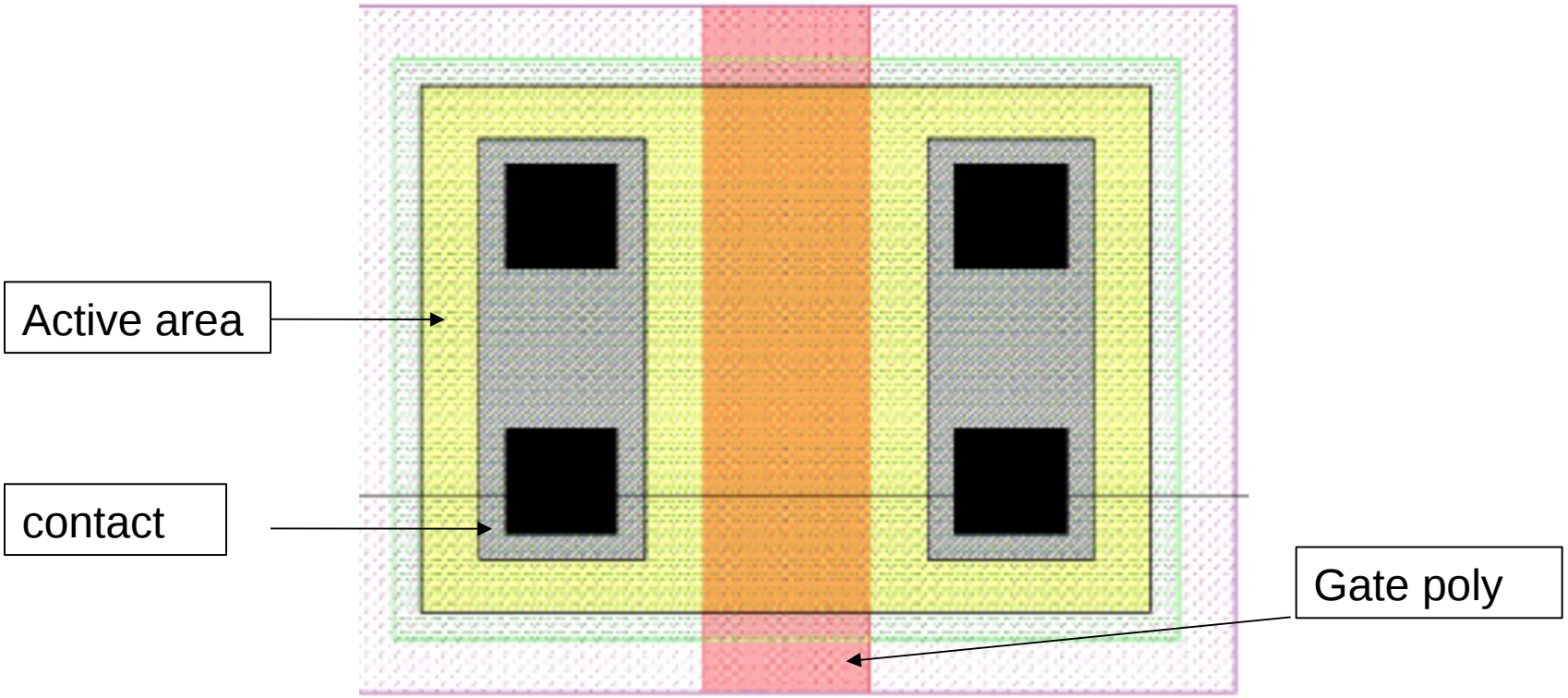


Fig. 14 Examples of space rule

4/ Cell layout

Space Rule

Like the width rule, spacing rules are applied to polygons on the same layer, but also to polygons or structures on different layers or under different conditions. An example of a spacing rule on different layers is the spacing required between a contact to active and gate polysilicon.



4/ Cell layout

Space Rule

In Figure 15 you can observe that the spacing between the gate polysilicon and the contacts is not the same in the two transistors.

The spacing “rule of the contact to the gate polysilicon” on the left-hand transistor has been violated to the extent that the gate polysilicon has been placed directly underneath the contact.

A short circuit between the metal and the gate polysilicon has been created. We can easily observe the problem in the three-dimensional view. The cross-section cut line was placed in the middle of the lower contacts.

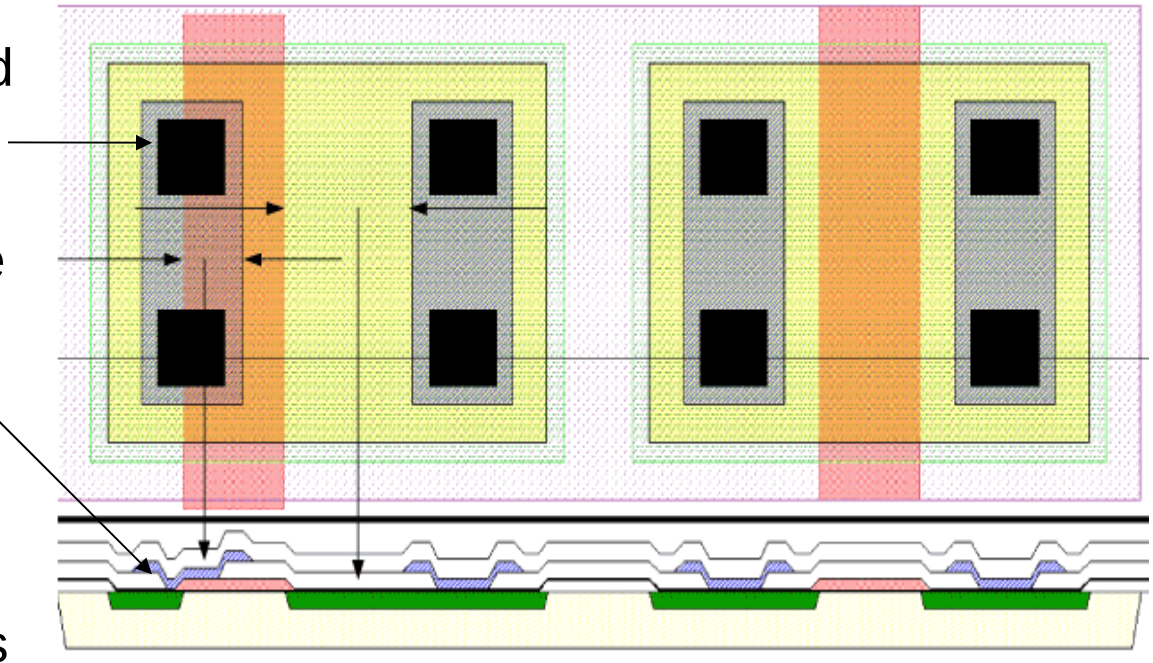
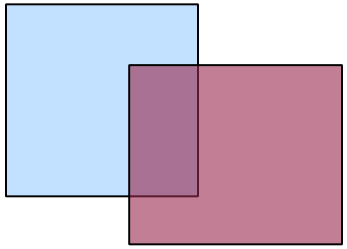


Fig. 15 Another example of the space rule

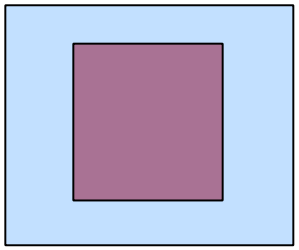
4/ Cell layout

Overlap Rule

The overlap rule is defined as the minimum overlap or surround of one polygon by another.
The overlap of a metal layer over a via or contact is a prime example of this rule.
Note that this rule always involves polygons that exist on different layers.



Minimum overlap



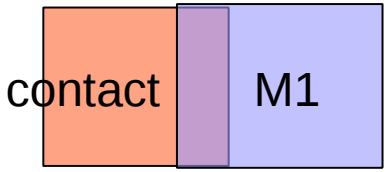
surround

When manufacturing using polygons on two different layers, there is a significant chance that there will be a misalignment between the desired and actual relative placement of the two polygons.
Misalignment between polygons can result in both undesired open and short circuit connections, depending on the layers involved.

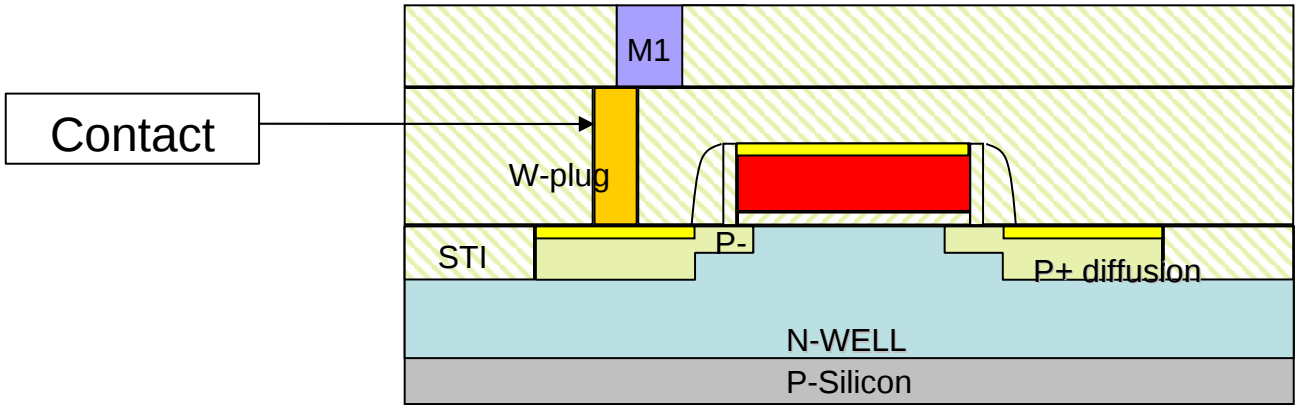
4/ Cell layout

Overlap Rule

Fundamentally, overlap rules reduce the impact of a small misalignment between layers in the manufacturing process by ensuring that the desired connectivity is maintained.
Let's consider an example where there is a contact between two interconnect layers. Physically, a contact polygon turns into a hole in the insulator between the two interconnect layers. The upper layer material must fill the hole and make contact with the underlying layer for the connection to be achieved.



misalignment

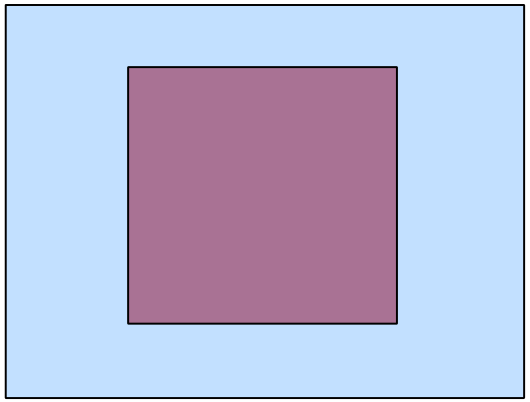


The connectivity between M1 and contact still maintaind although there is a misalignment

4/ Cell layout

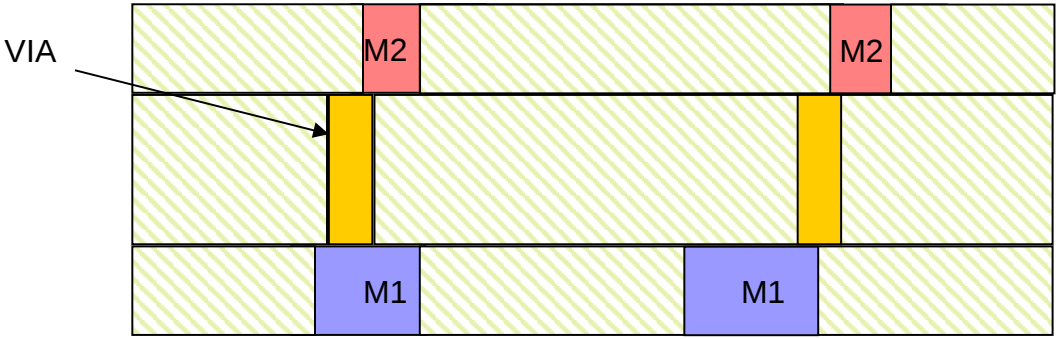
Overlap Rule

The overlap rule states that the two layers must not only overlap each other,
one layer must surround the other by a certain value. This value is the value for the overlap rule.
In the case of the contact, the upper and lower layers must completely overlap the contact and surround the contact hole by the overlap rule value.



Surround with certain value

If one of the layers does not sufficiently overlap and surround the contact hole, then the connection will not be reliable under all manufacturing conditions.



The connectivity between M1 and M2 is week or poor

The open might occur here

4/ Cell layout

Overlap Rule

In Figure 16, in examples 1 and 2, observe the result of poor contacts between active and metal1.
If the active is not completely overlapping the contact polygon, the contact base is not wide enough.
If the metal is not completely overlapping the contact polygon, then the contact hole is not completely filled and the contact will again result in a smaller connection surface area.

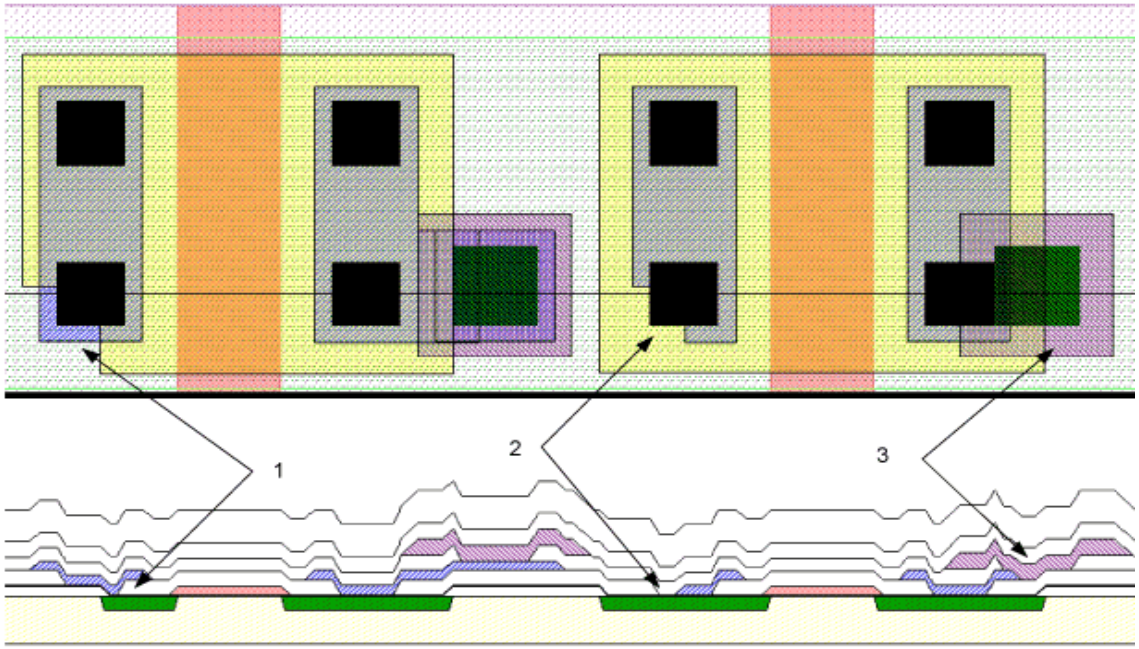


Fig. 16 Examples of the overlap rule

4/ Cell layout

Overlap Rule

In the third case we have an overlap problem between metal1 and metal2.
The via has no metal1 overlap, so the connection, if any, is minimal.
The example in the figure demonstrates a case where an open circuit has a greater likelihood of happening.

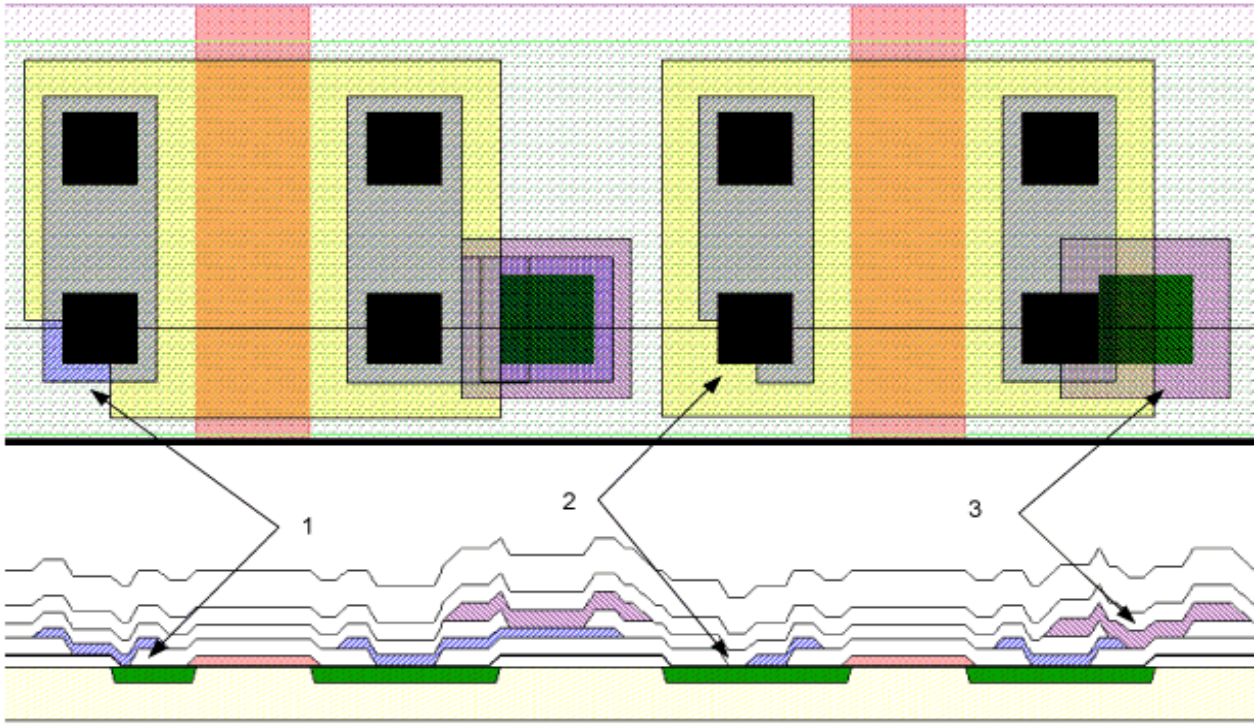


Fig. 16 Examples of the overlap rule

4/ Cell layout Overlap Rule

There are also below Overlap rules:
active overlapping the gate and the gate overlapping the active areas.
Figure 17 shows four different cases.
Node Out4 is an example of adequate overlap of the gate layer by the active polygon.
Node Out4 is well defined. Contrast this example to node Out3.
It is likely that the thin area of node Out3 will not be created.

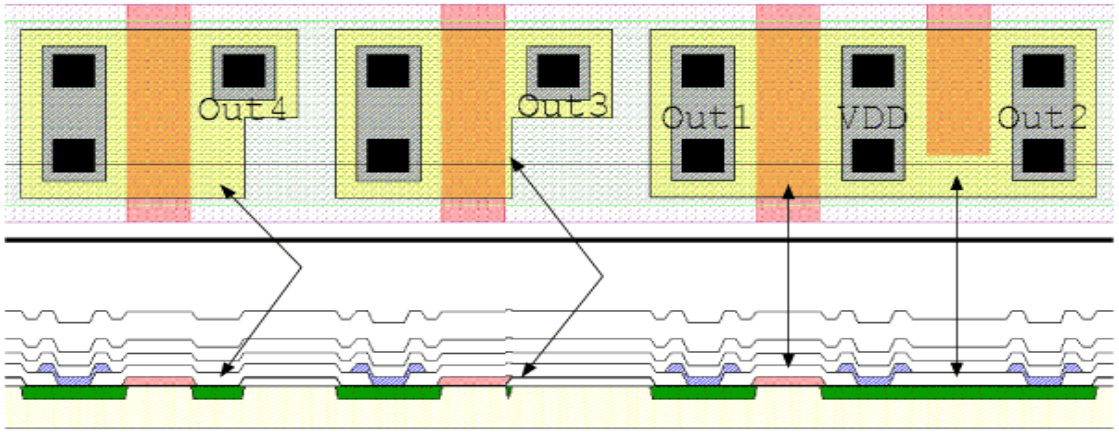


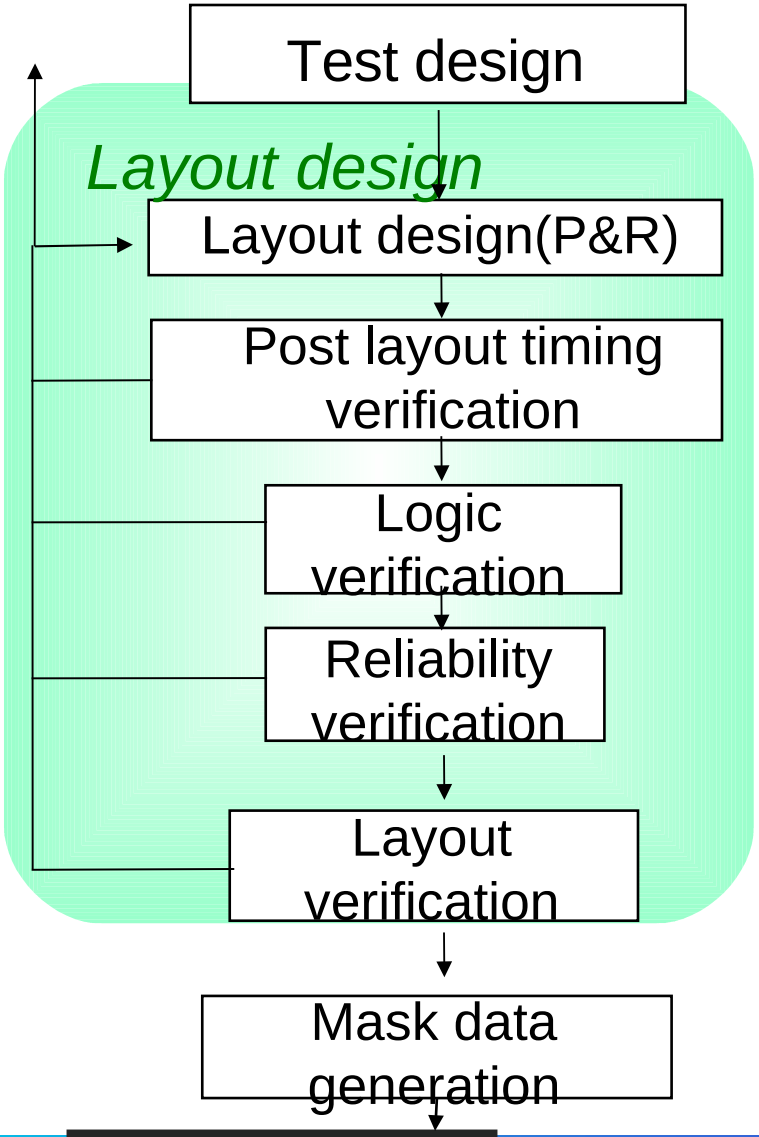
Fig. 17 More example of the overlap rule

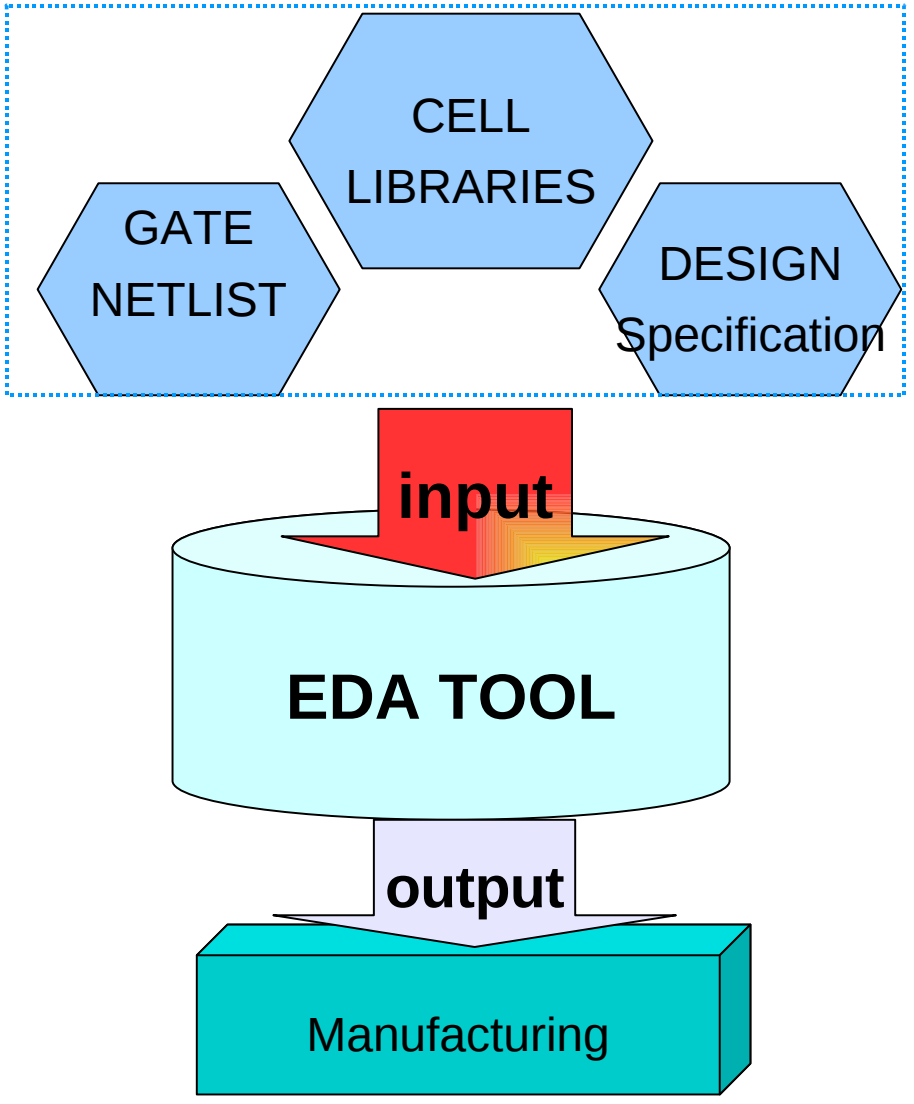
Out1 and Out2 are examples of the gate layer overlapping the active layer.
You can see that because the gate layer does not fully overlap the active area, nodes Out2 and VDD are shorted to each other, as they are part of one polygon of active.

Design rule can be checked by using Design Rule Checker (DRC).

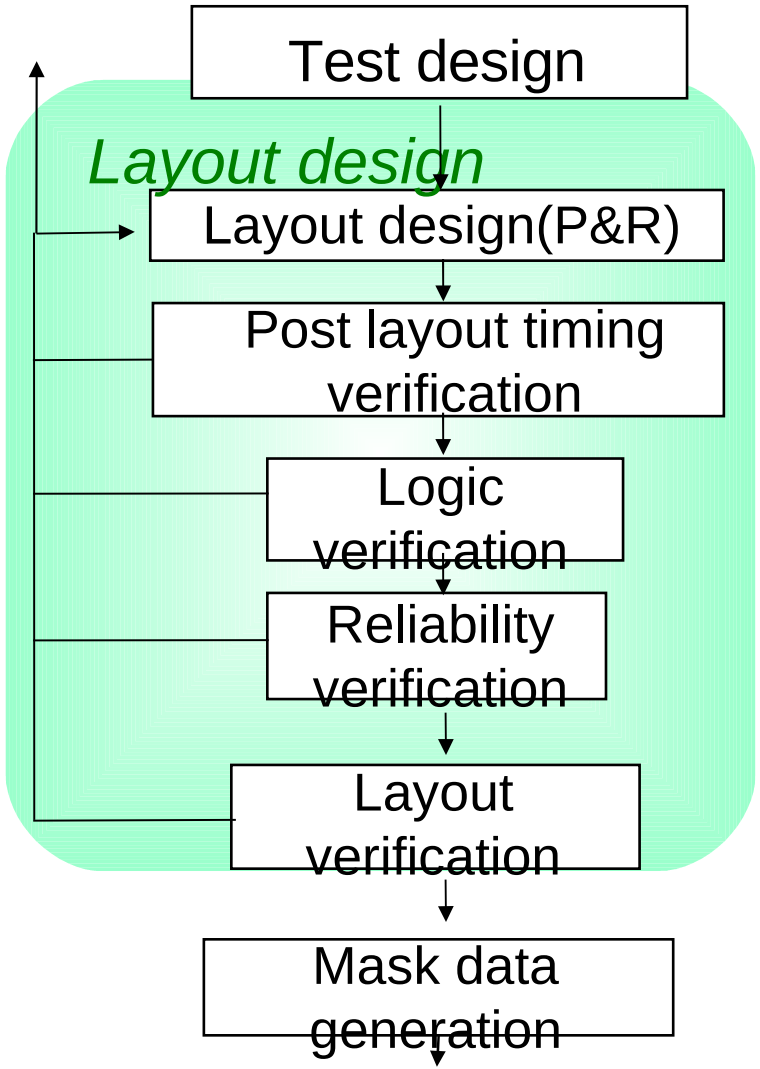
5/ Chip Layout Design Flow

Following slides show the chip design flow using cell libraries.





5/ Chip Layout Design Flow



Automatic layout design by Place & Router tool, Model generation for post layout □Encounter/Astro □Star-RCXT □

Delay calculation/confirmation of timing due to post layout □ PrimeTime, Verilog_XL/NC-Verilog □

Logic verification using Post P&R net(Confirmation of original logic circuit operation) □ Verilog_XL/NC-Verilog/Conformal-LEC L

Confirmation of reliability due to post layout(IR-Drop, Cross-Talk, Hot Carrier resistance, Electro-migration resistance) □ AstroRail, PrimeTimeSI □□

Physical verification of mask data(DRC,LVS,ERC, etc) L □Calibre □

Why we need Post Layout Timing Verification?

5/ Chip Layout Design Flow

Layout design methodology

1) Individual design method

Design with interactive mode EDA tool (interactive design)

→It applies by cell/module design.

2) Master slice method (gate array method) P&R

Common master layout with buried transistors is ready and automatic wiring tool is applied to metal wiring layout.

The development cost is small because of slice layout design.

Since base wafers are already prepared, the manufacturing period is short.

Need to route 100% in a constant wiring area.

← Need to consider to reduce unwiring.

3) Cell base method P&R

P&R area of cell/module are changeable.

← It is necessary to minimize the chip size.

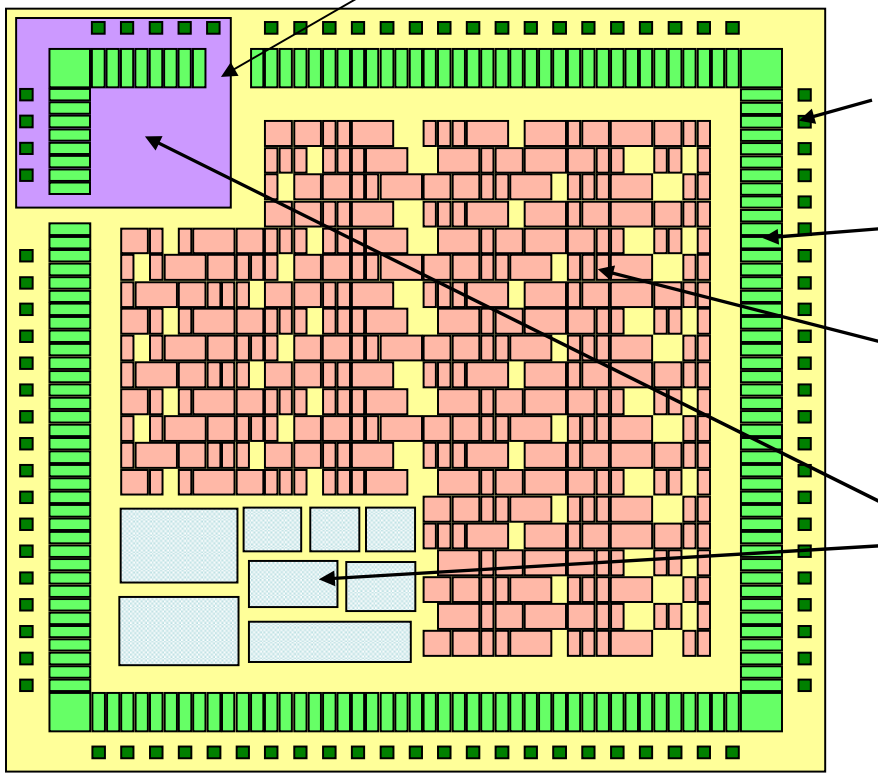
4) Hierarchical cell base method P&R

A hierarchical design of method(3) where logic is split from the top down, and layout is done from the bottom-up.

5/ Chip Layout Design Flow

◆Cell based method

Because cells can be arbitrarily placed, it is adopted by the layout design for general SoC. Automatic P&R is applied. Multi-layer metals are used.

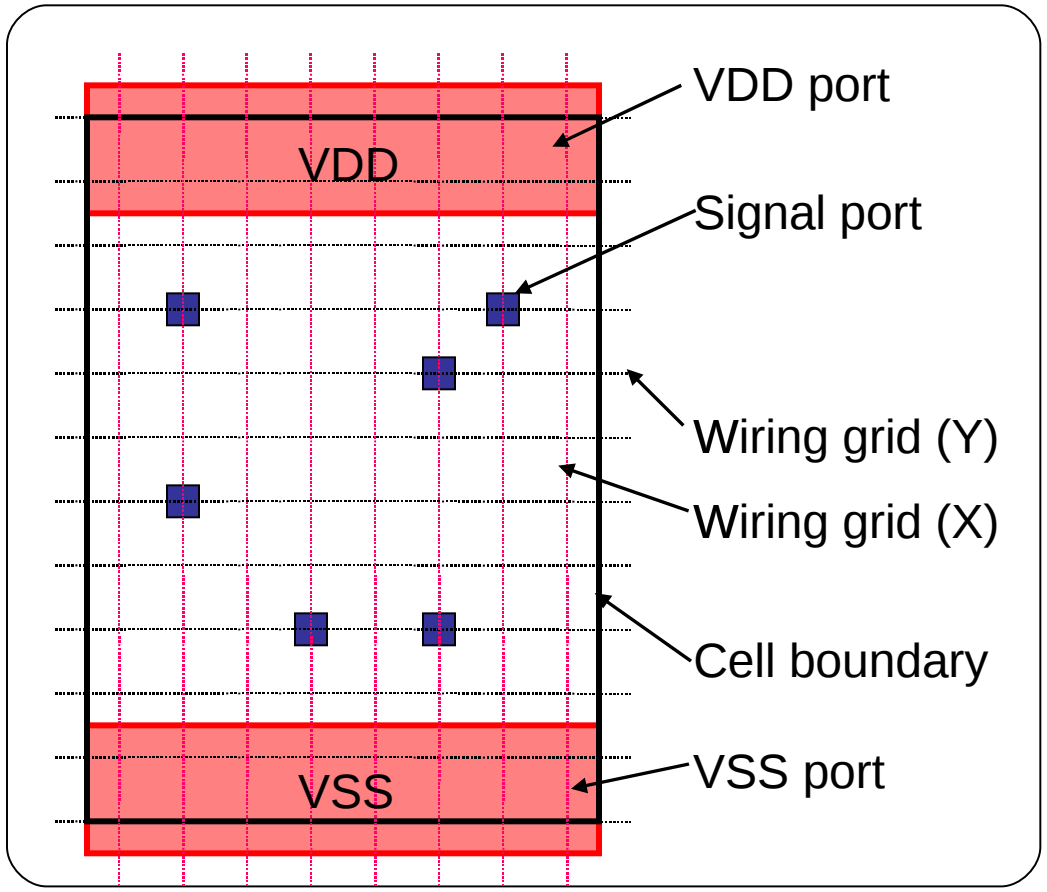


5/ Chip Layout Design Flow

Cell based method

◆Standard cell structure of cell based method

Standard cell structure



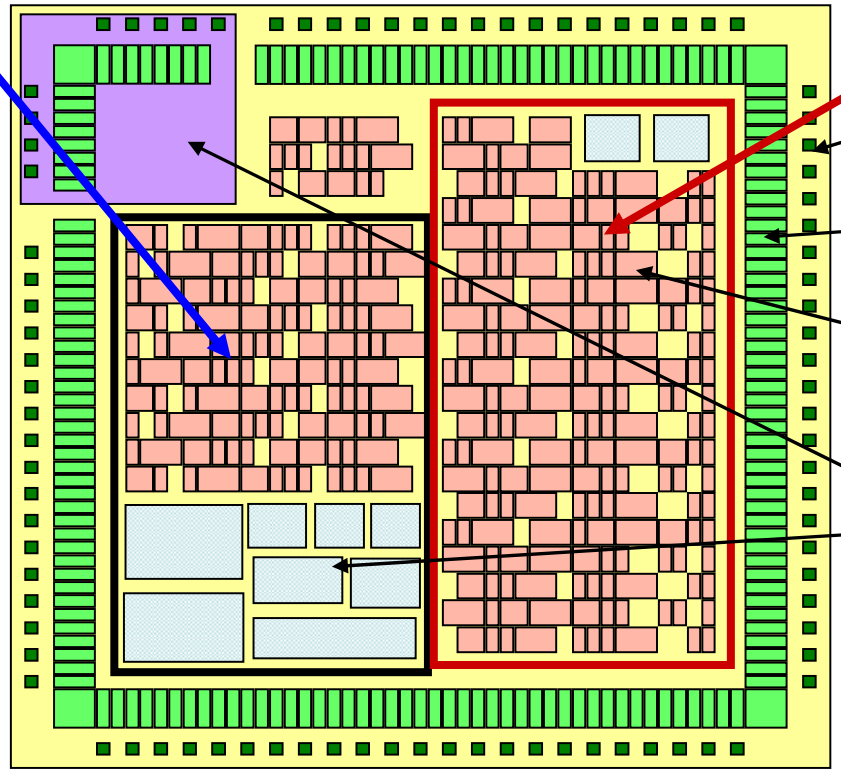
- The width of the cell is changeable.
(integral multiples in X wiring grid)
- The height of the cell is constant.
(integral multiples in Y wiring grid)
- The signal port is “on grid”.
- Power supply ports are fixed in the cell. Y location is same to all cells.
- Metal wirings can run over cells.

5/ Chip Layout Design Flow

Hierarchical cell based method

The standard cell placement area is laid out hierarchically depending on the hierarchical logical structure of the gate level net. Automatic P&R is applied.

Hierarchical logic B



Hierarchical logic A

Bonding PAD

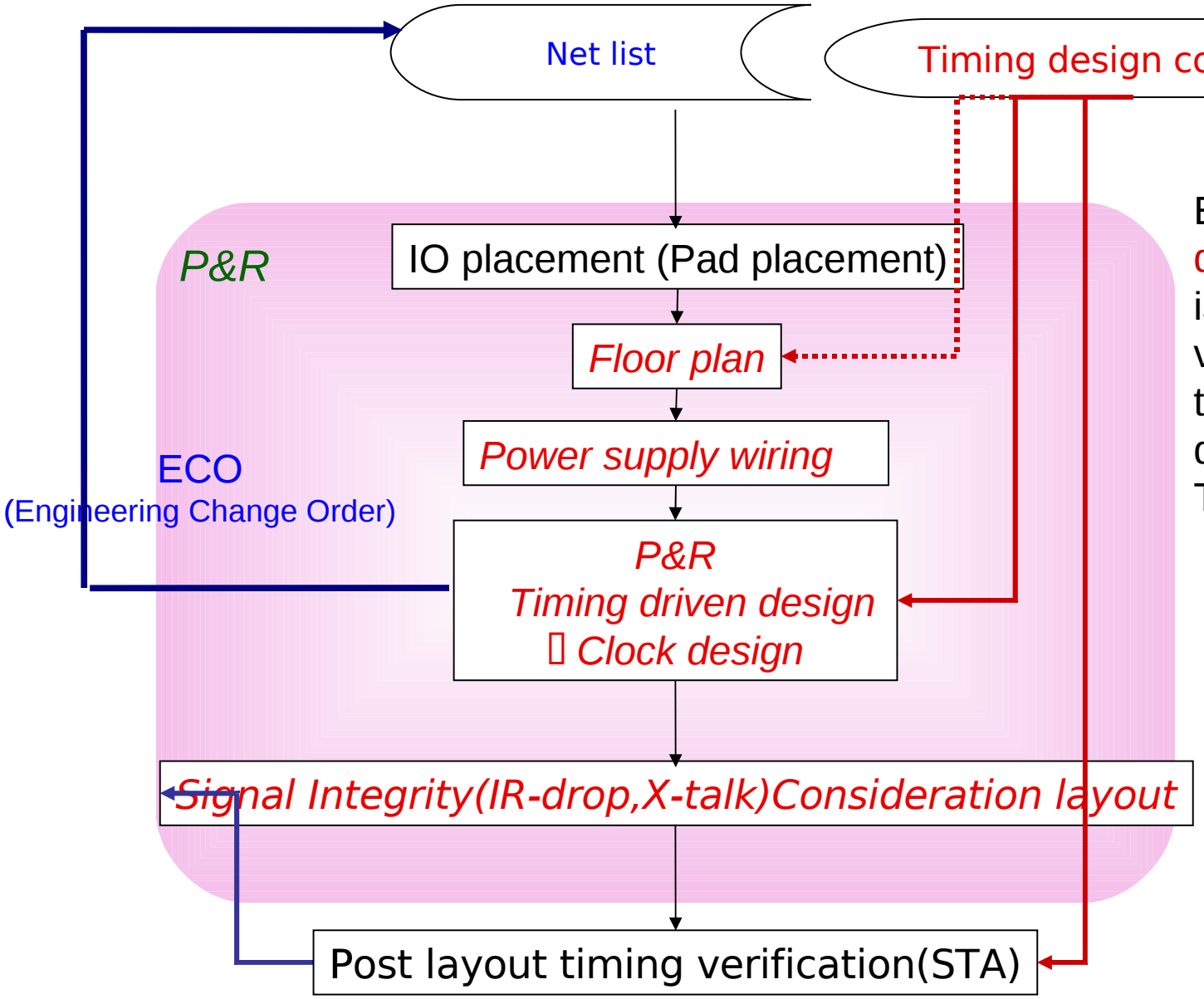
IO cell (free placement)

Internal cell row
(standard cell placement area, flat placement

IP modules (memory and analog, etc) area (free placement)

All areas are for the wiring areas.
(free channel and wiring can run though over cells)

6/ P&R design flow

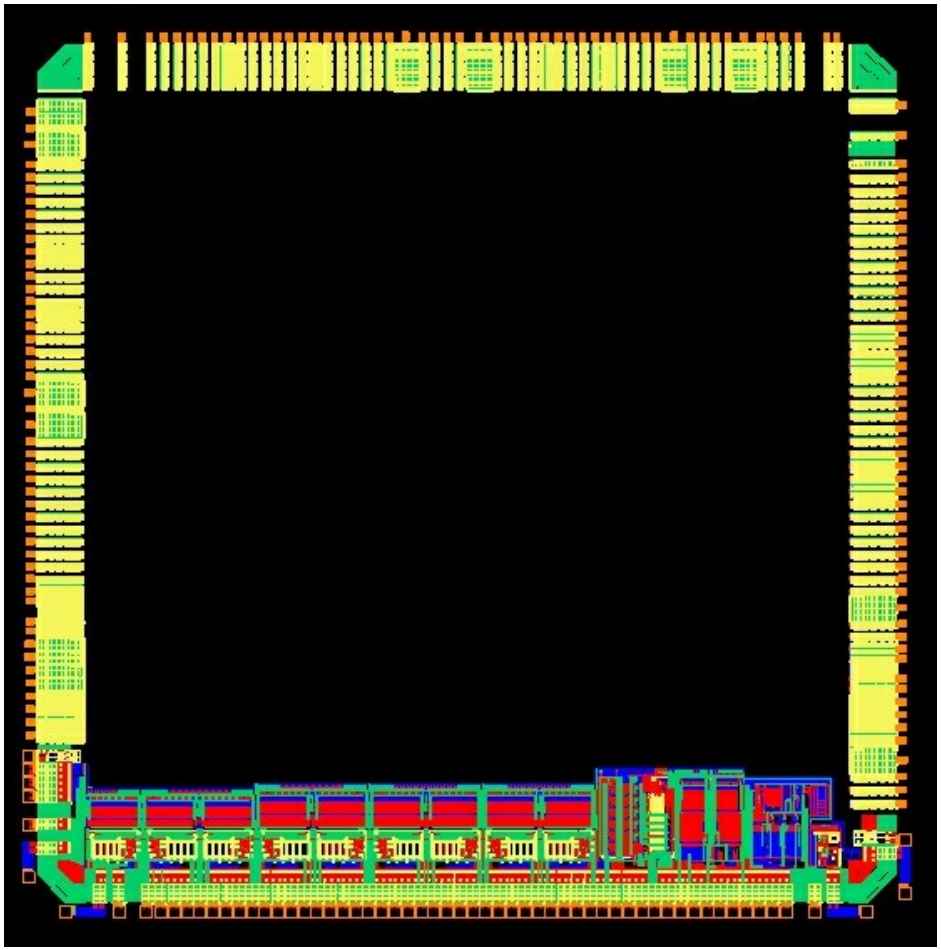


By applying "Timing design constraint" which is applied to logic verification to P&R tool, the reduction of layout design TAT(Turn Around Time) is realized.

Actually, several ECOs (re-layout,average 4~8 times) are happened due to incomplete floor plan optimization, lack of P&R tool functions, etc.

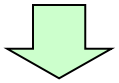
6/ P&R design flow

I/O placement
(Pad placement)

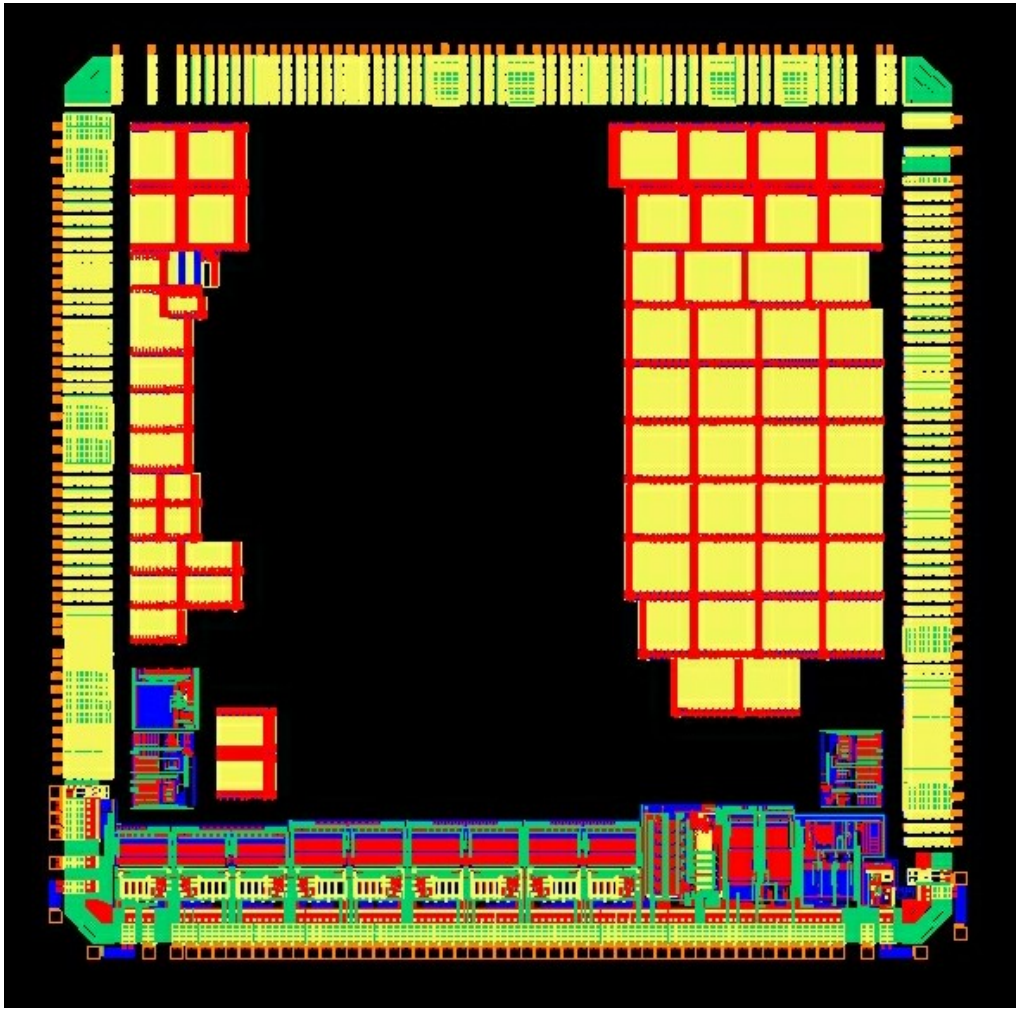


6/ P&R design flow

I/O placement
(Pad placement)

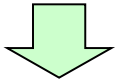


Floor plan

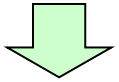


6/ P&R design flow

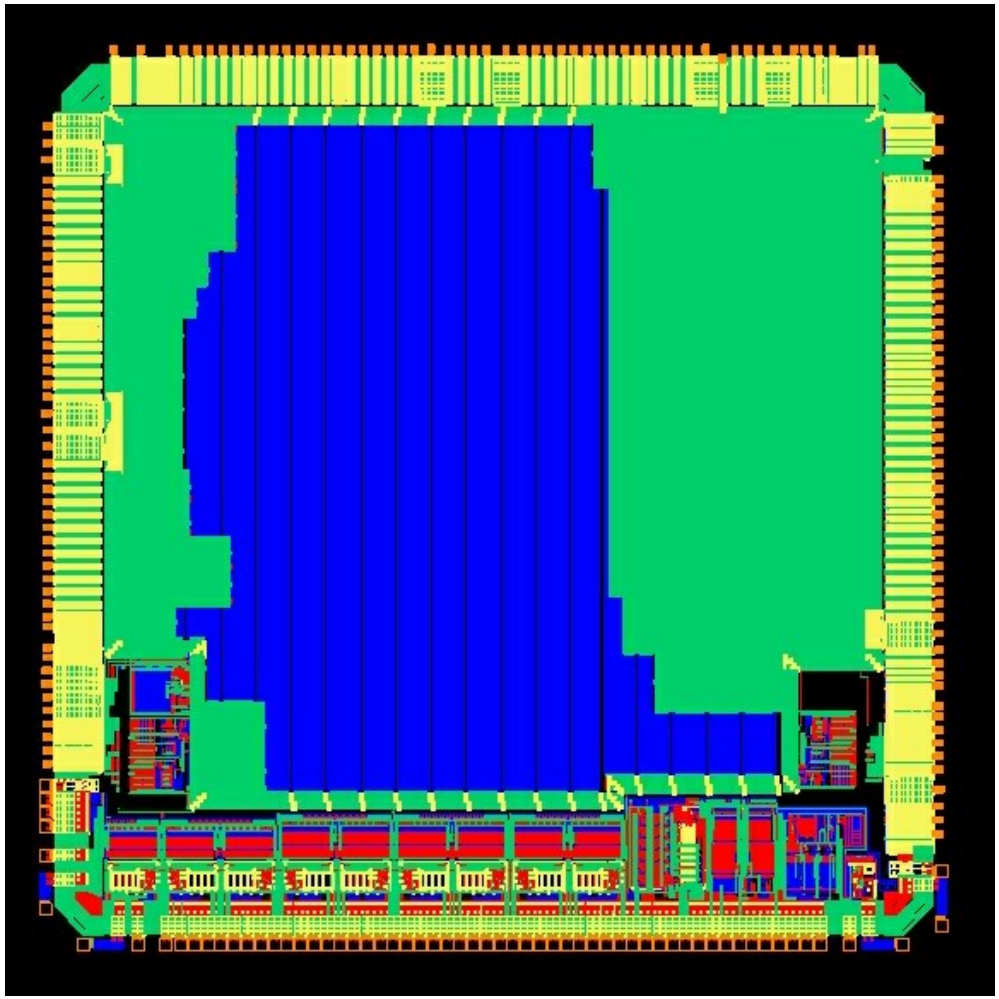
I/O placement
(Pad placement)



Floor plan

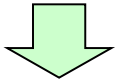


Power supply wiring

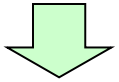


6/ P&R design flow

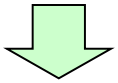
I/O placement
(Pad placement)



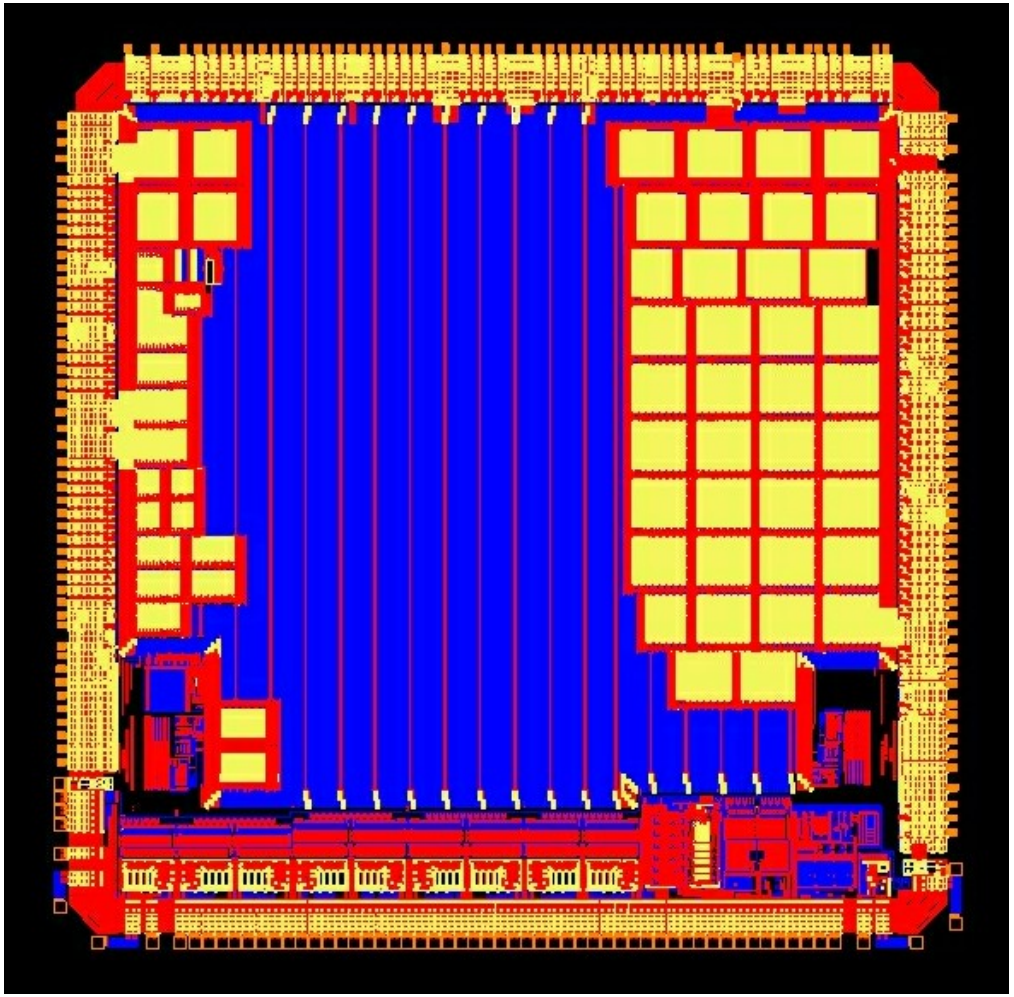
Floor plan



Power supply wiring



Automatic placement



6/ P&R design flow

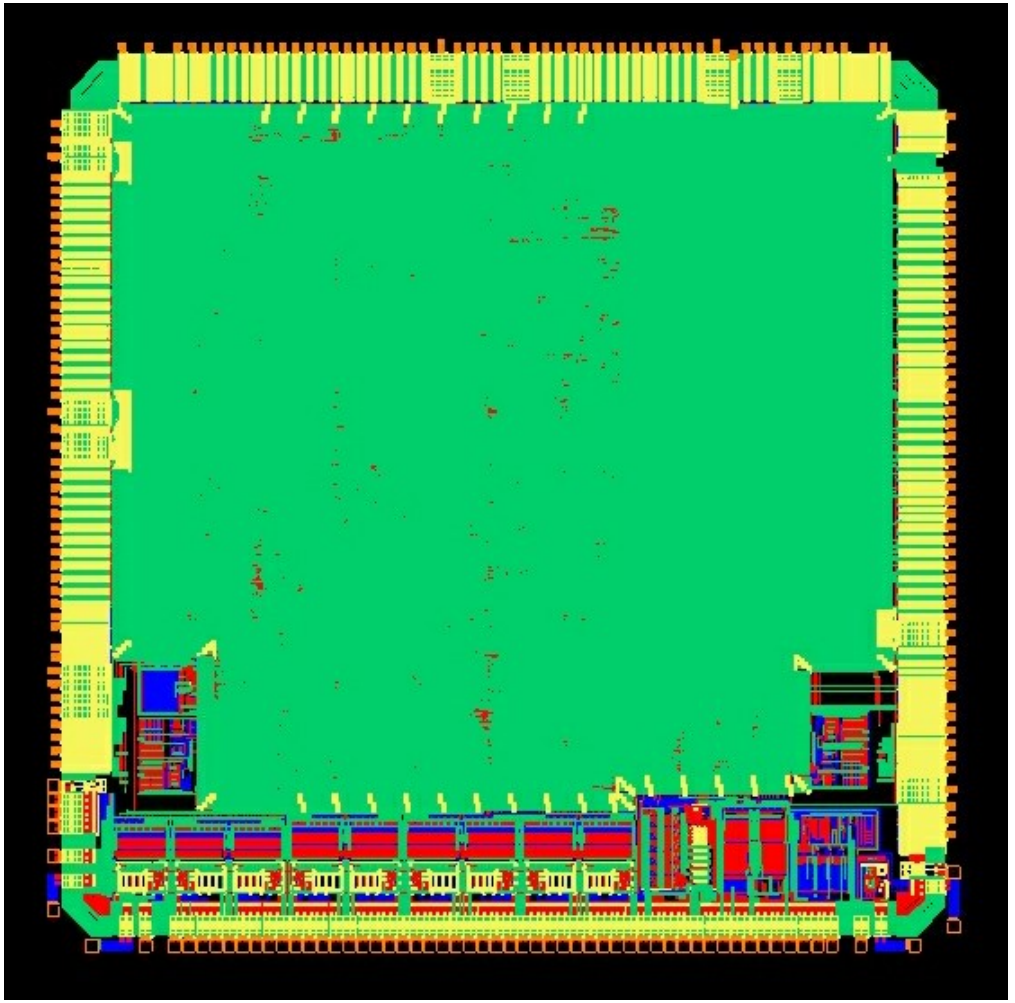
I/O placement
(Pad placement)

Floor plan

Power supply wiring

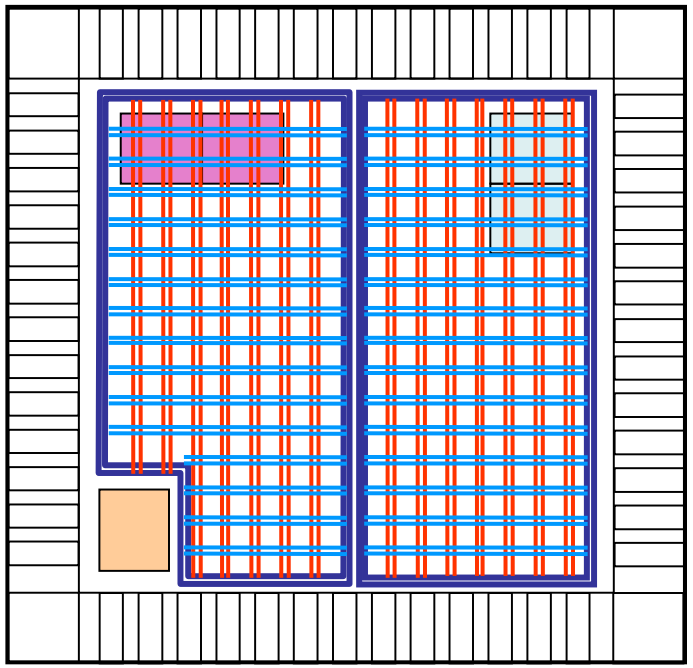
Automatic placement

Automatic routing



6/ P&R design flow Power supply design

"Power supply design" targets to establish power routing to keep the specifications of design rule, IR-Drop, EM, etc and to supply sufficient current to each cell, considering to minimize the chip size.



<Design approach>

1) Manual design

C The designer decides numbers of power routing and metal width using the layout editor and the P&R tool.

2) Semi-automatic design

□□□ Design semi-automatically using Angel@Ring (Renesas in-house tool) and pre-determined power routing cells.

3) Automatic power design tool

□□□ Developed and implemented to EDA tools

Under development of partially shutdown function(support of voltage island).

6/ P&R design flow Power supply design

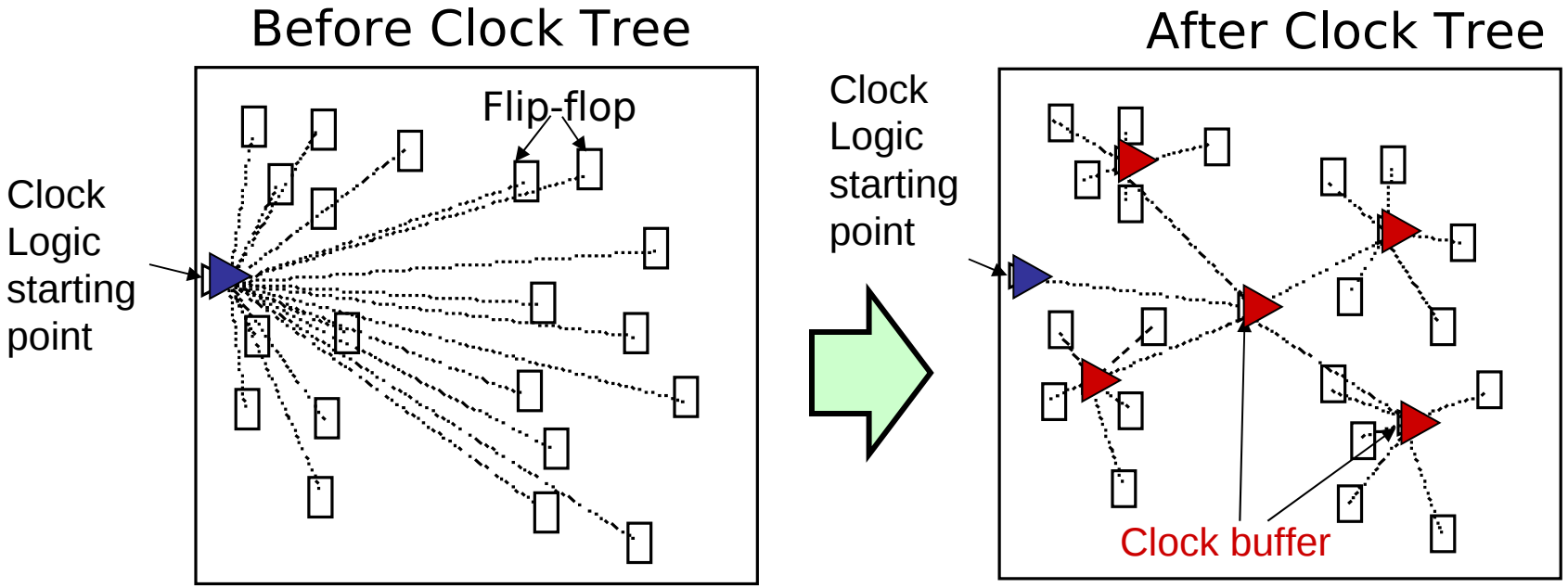
◆In addition, the each product needs special care depending on its layout.

Product usage	Design issues	Design approach of power supply
Low power consumption Product	Optimization of cells and the clock generation are necessary, considering the reduction of power consumption.	Use of low voltage operating cells, high Vth(low leak/low speed) cell library
Low standby current product	The systematic power reduction is needed by controlling power supply positively.	Separate power supply at each block and control On/Off of each power supply
General-purpose product	The reduction of IR-Drop/EM estimation and design TAT by modeling power supply trunk	Selection of power sypply model which guarantees IR-Drop/EM and automatic power layout
High spped product	A strong power supply trunk line which suuports big power consumption is necessary.	Ensure power supply dedicated layer and power supply to LSI with bump IO

6/ P&R design flow　Clock design

◆In the clock design, it is necessary to reduce Skew of the clock.

0 → Clock skew is adjusted by inserting clock dedicated buffers and by dividing net into tree structure(clock tree design).



What is Clock Skew:

Maximum value minus minimum value of the delay from starting point of clock to ports of each FF/latch.

6/ P&R design flow　Clock design

The excellent clock design means:

- Skew of the clock is small.
  → For the operation guarantee of a synchronous circuit

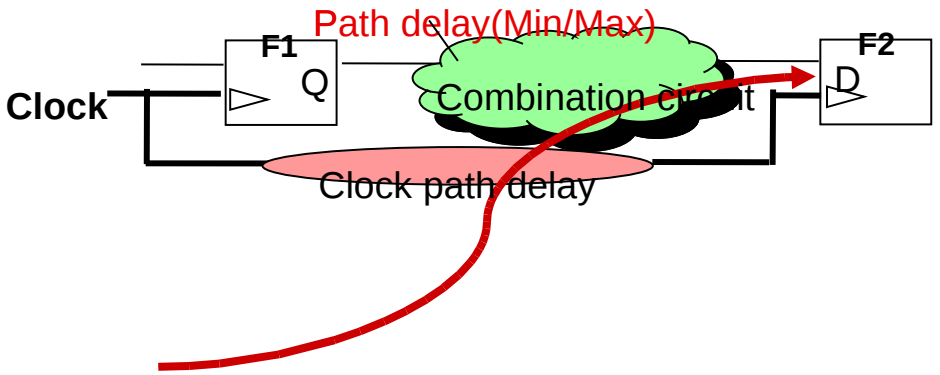
- The number of the clock buffer is few.
  → For the reduction of gate counts and reduction of power consumption
- The maximum delay value of the clock path is small.
  → For the reduction of dispersion within a wafer and within a chip.
- The delay value of the clock path is close to a specified value.
  → To adjust delays of different phase between different clocks.

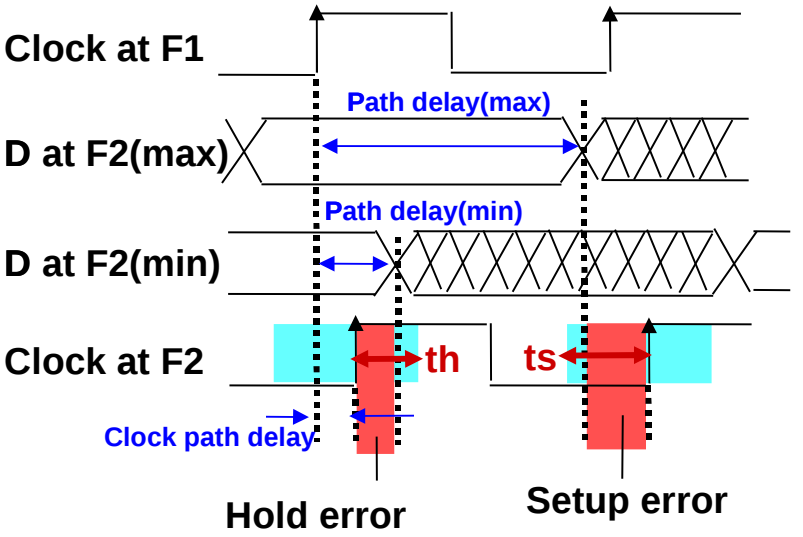
6/ P&R design flow Timing driven design

◆Timing driven design means that Automatic P&R tool designs layout considering timing constraints specified at logic design.

◆Timing constraint means that timing(path delay value, setup time, hold time) between clock port and data port of flip-flop.

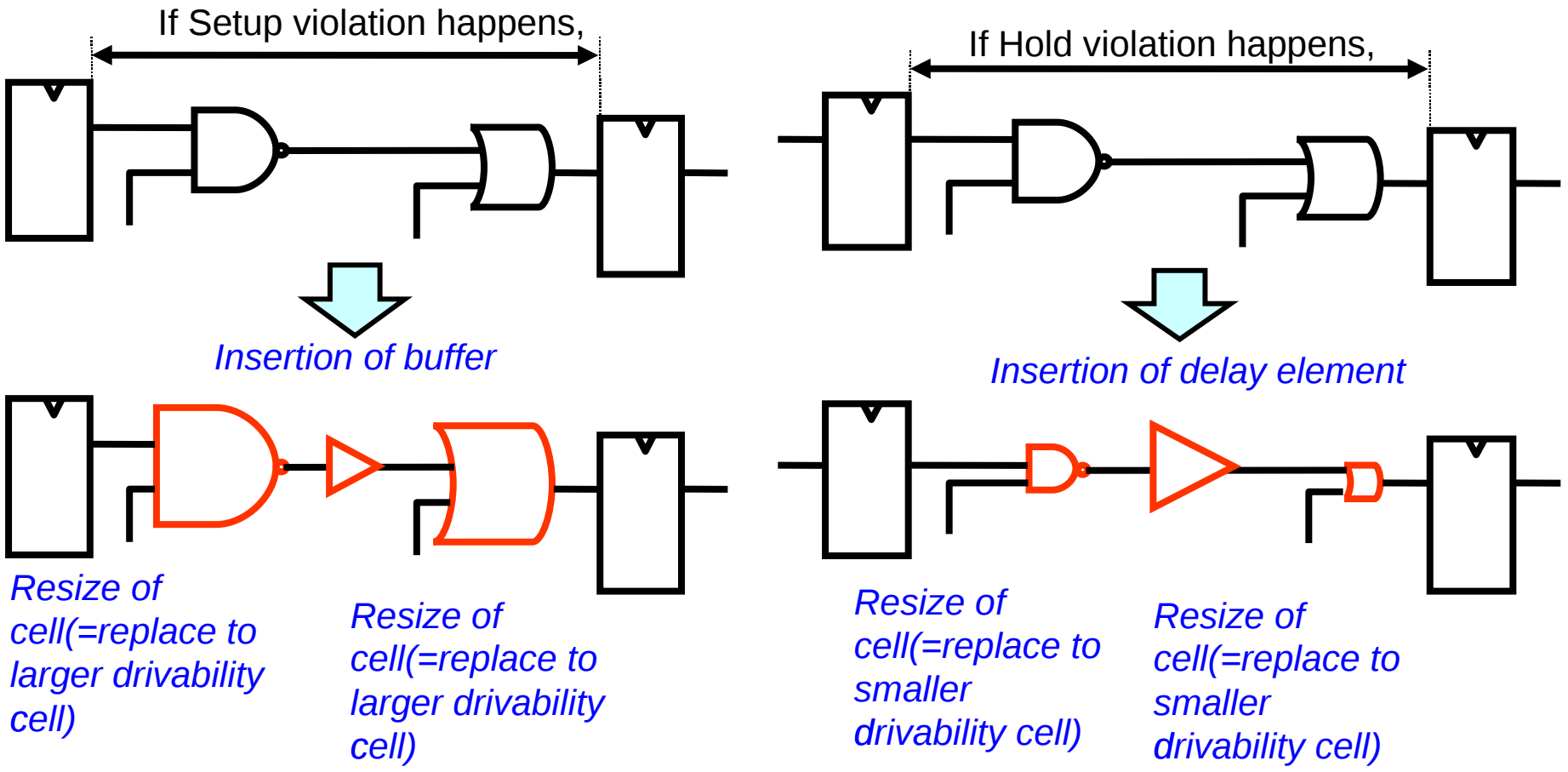
Constraint of Setup time: Data should reach by (the reach time of clock- ts)
Constraint of Hold time: Data should not change by (the reach time of clock + th)





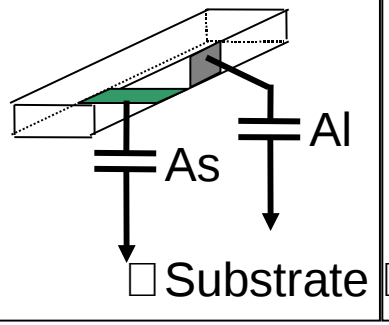
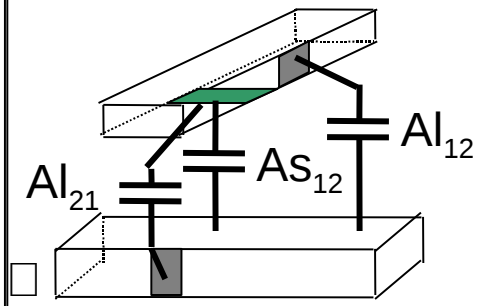
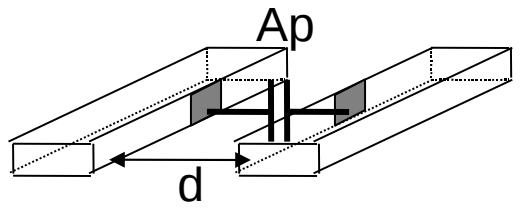
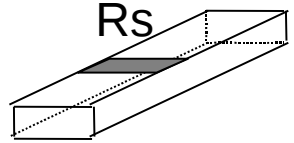
6/ P&R design flow

Example of Timing optimization



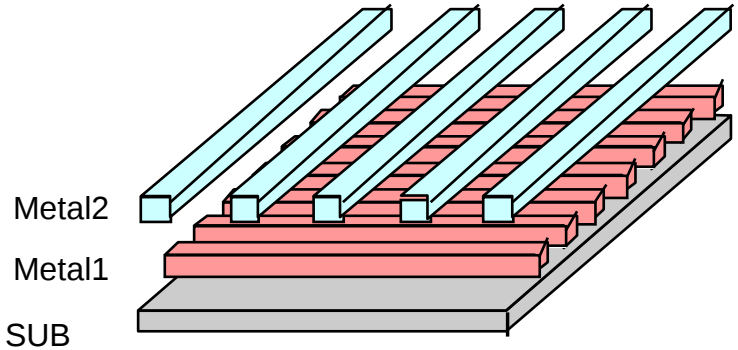
6/ P&R design flow RC extraction

◆Post layout extraction means that the extraction of wiring loads (stray capacitance and resistance) from layout after P&R.

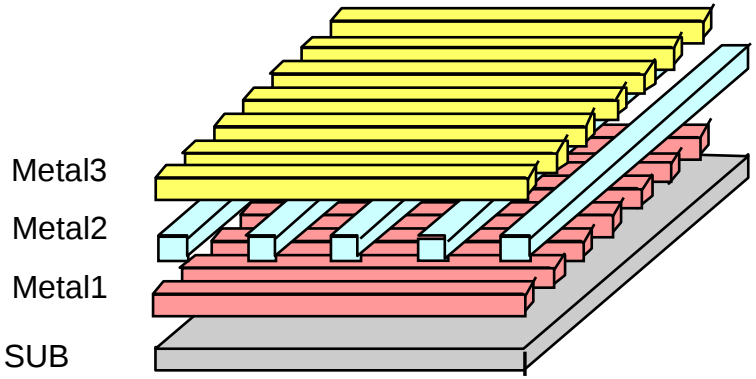
Field capacity	Crossing wiring capacity	Parallel wiring capacity	Sheet resistance
			

The parasitic capacitance parameter changes depending on peripheral wiring (with/with out adjacent wire, top and bottom, coarse or dense).

Dense Metal1 and coarse Metal2



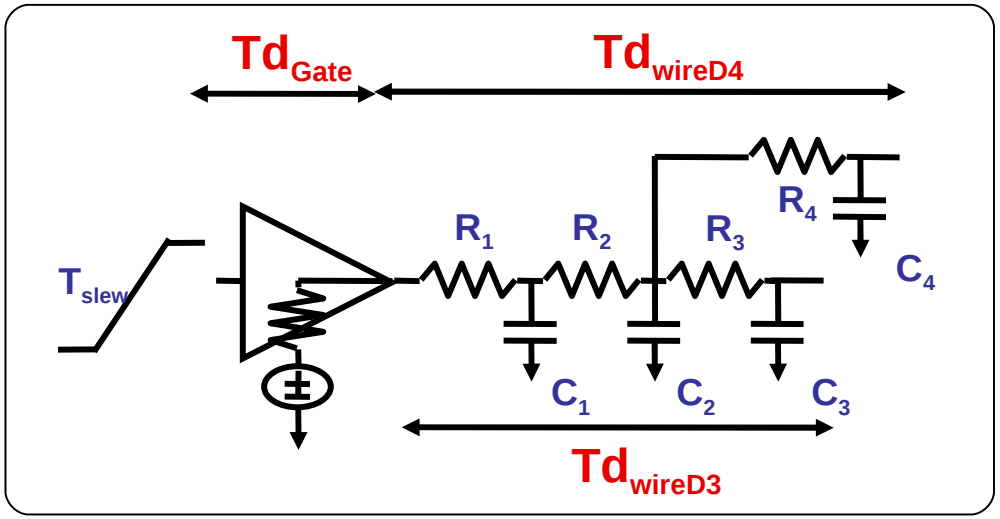
Dense Metal1 and Metal3, and coarse Metal2



6/ P&R design flow Delay calculation

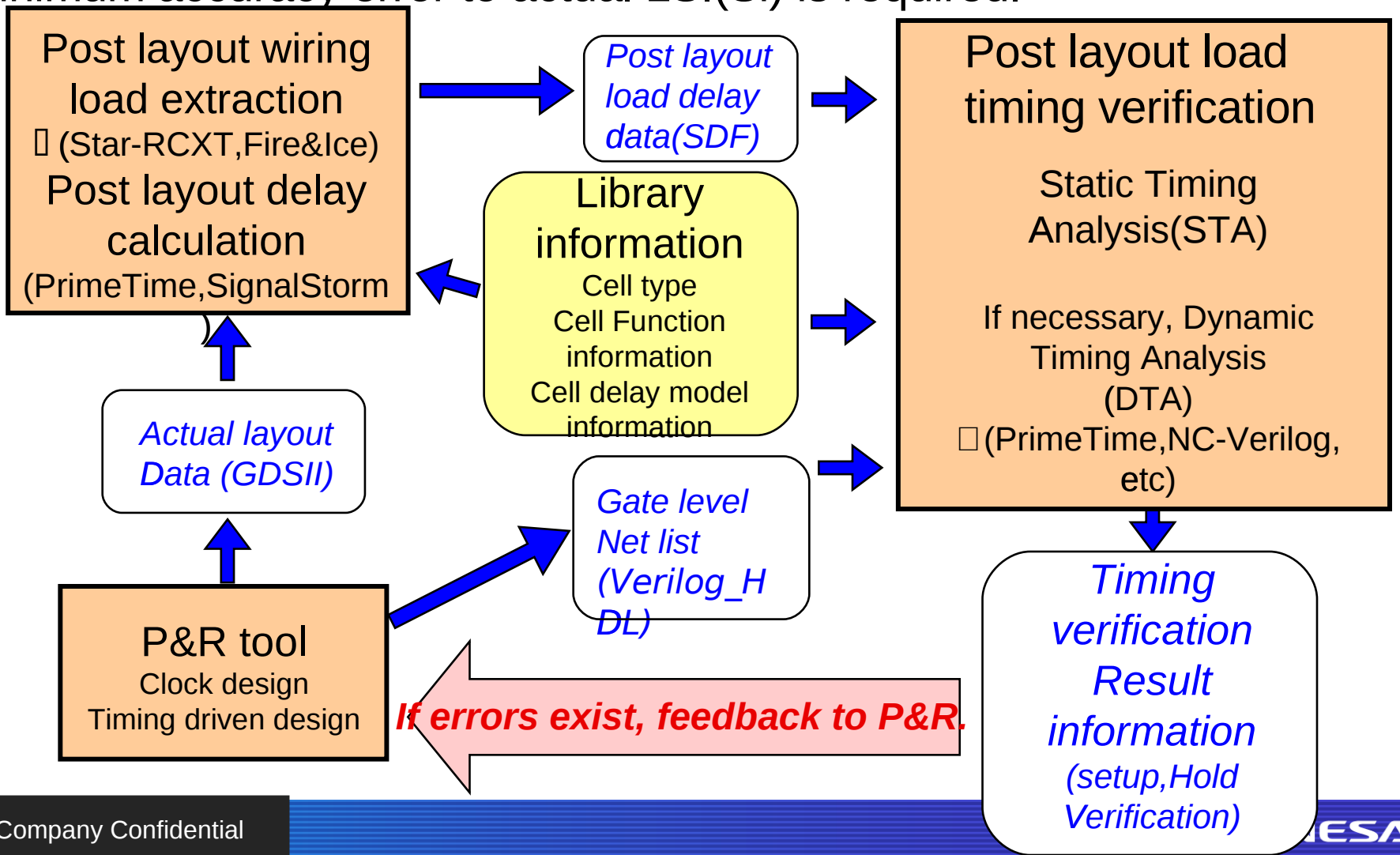
◆ The wire load delay calculation is done by using the post layout wiring model (stray C/R) and the cell delay model.

The calculation method for 0.15um-90nm technology
Gate delay : Input slew/output load capacity dependence model
Wiring delay: AWE and Arnordi method



6/ P&R design flow　Post layout timing verification

◆Post layout timing verification means that timing verification is done based on post layout delay data extracted from post layout wire load. Minimum accuracy error to actual LSI(Si) is required.



6/ P&R design flow　Signal integrity

◆For LSI of the deep submicron/nano-technology, signal integrity design/verification is needed.

◆Signal Integrity means following phenomena.

(1) Power-supply voltage drop (Rising of grand voltage) (IR-Drop)

Tr/Gate mal-operation and timing change due to power-supply voltage drop

(2) Cross-Talk (X-Talk)

Tr/Gate mal-operation and timing change due to noise between signal wirings

(3) Electro Migration (EM)

Disconnection of wiring due to excess current(wiring stress occurs)

(4) Hot Carrier (HC)

Tr breakdown due to excessive Tr activation (Tr stress occurs)

6/ P&R design flow

IR Drop verification/EM analysis

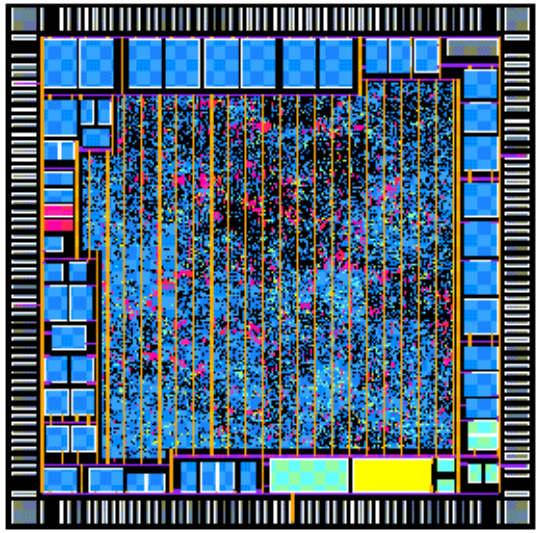
◆The purpose of IR-Drop verification/EM analysis is to realize the low voltage and high performance LSI.

□□ IR-Drop verification □ can analyze the defective operation part due the internal voltage drop

□□ EM analysis □□□ can analyze current density shortage part of wiring (Currently, power supply wirings are analyzed.)

6/ P&R design flow

Analysis of power consumption distribution



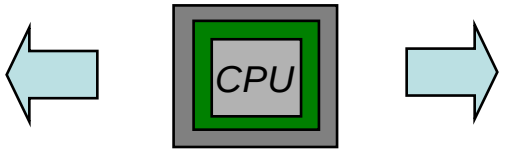
Cells are displayed with several colors based on power consumption.

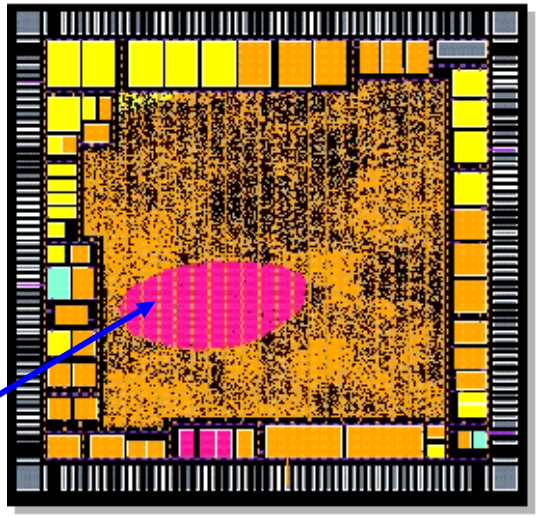
IR-Drop is displayed based on IR-Drop values.

↓

Need to reinforce power supply if reference value is exceeded (manual correction (automatic correction is not applicable).

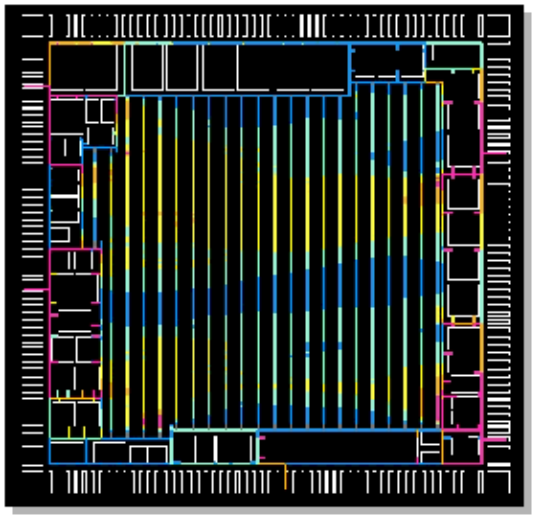
Layout data





Analysis of power-supply voltage drop distribution

Analysis of power supply wiring electromigration



Wires are displayed with several colors based on current density.

↓

Need to lower current density if reference value is exceeded (manual correction (automatic correction is not applicable).)

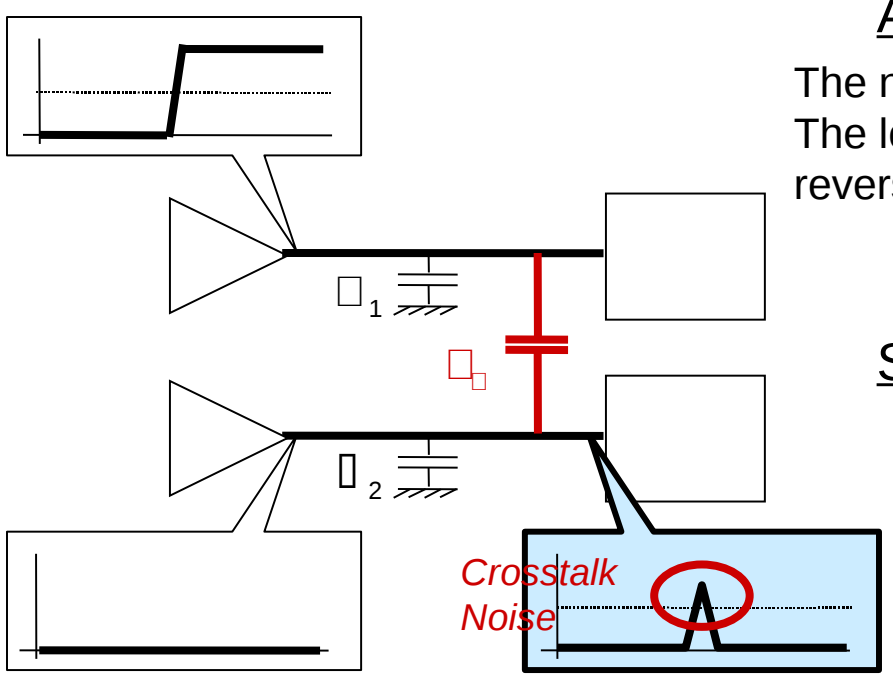
6/ P&R design flow Cross-talk

◆Cross-talk is that noise generated due to signal operation of adjacent wiring causes mal-function of signal.

□ →f Logic mal-function and timing change make mal-operation of LSI.

A * □ Due to finer wiring spacing, the possibility of cross-talk increases.

◆Logic mal-function due to cross-talk



Logic value is reversed.

Asynchronization signal system

The noise is generated in the set and the reset signal.
The logic value of the asynchronization signal is reversed..

Logic mal-function

Synchronous signal system

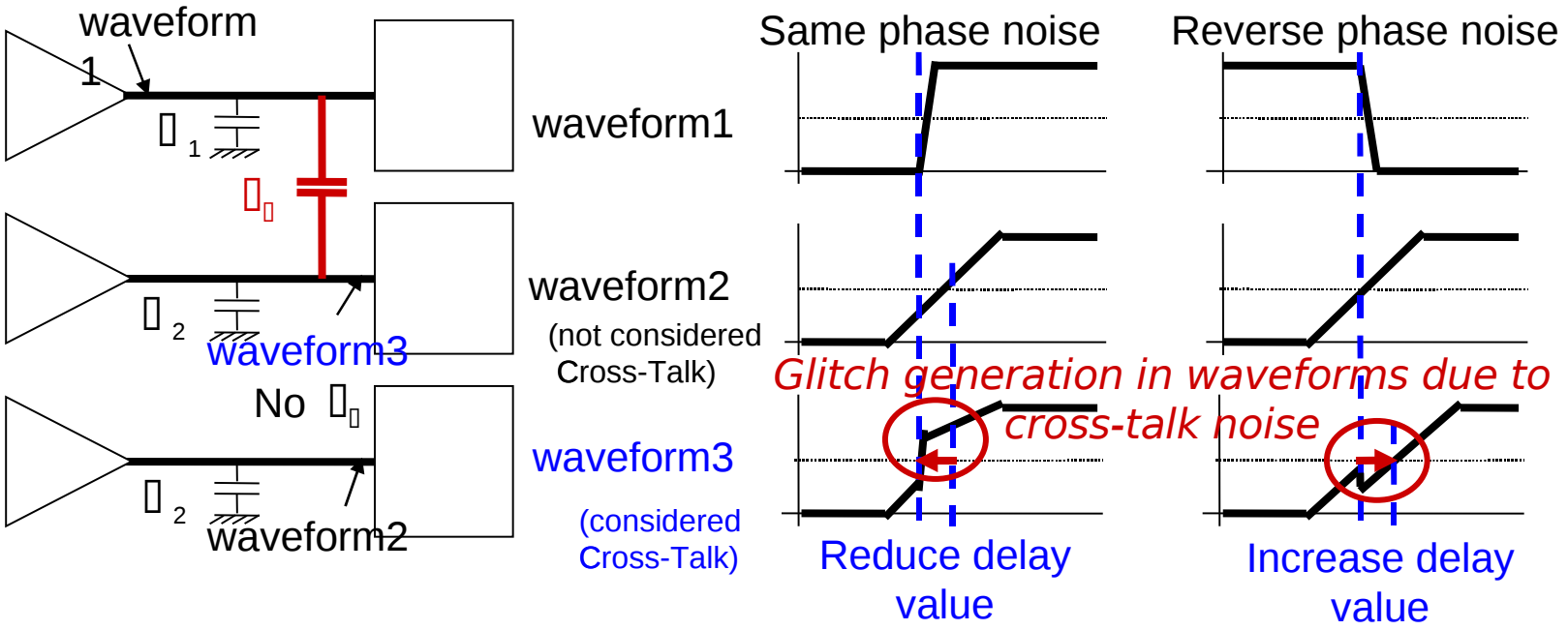
The noise is generated in clock signals.
The logic value (FF output) synchronizing with clock is reversed.

Logic mal-function

6/ P&R design flow

Timing analysis due to cross-talk

◆Timing change due to cross-talk

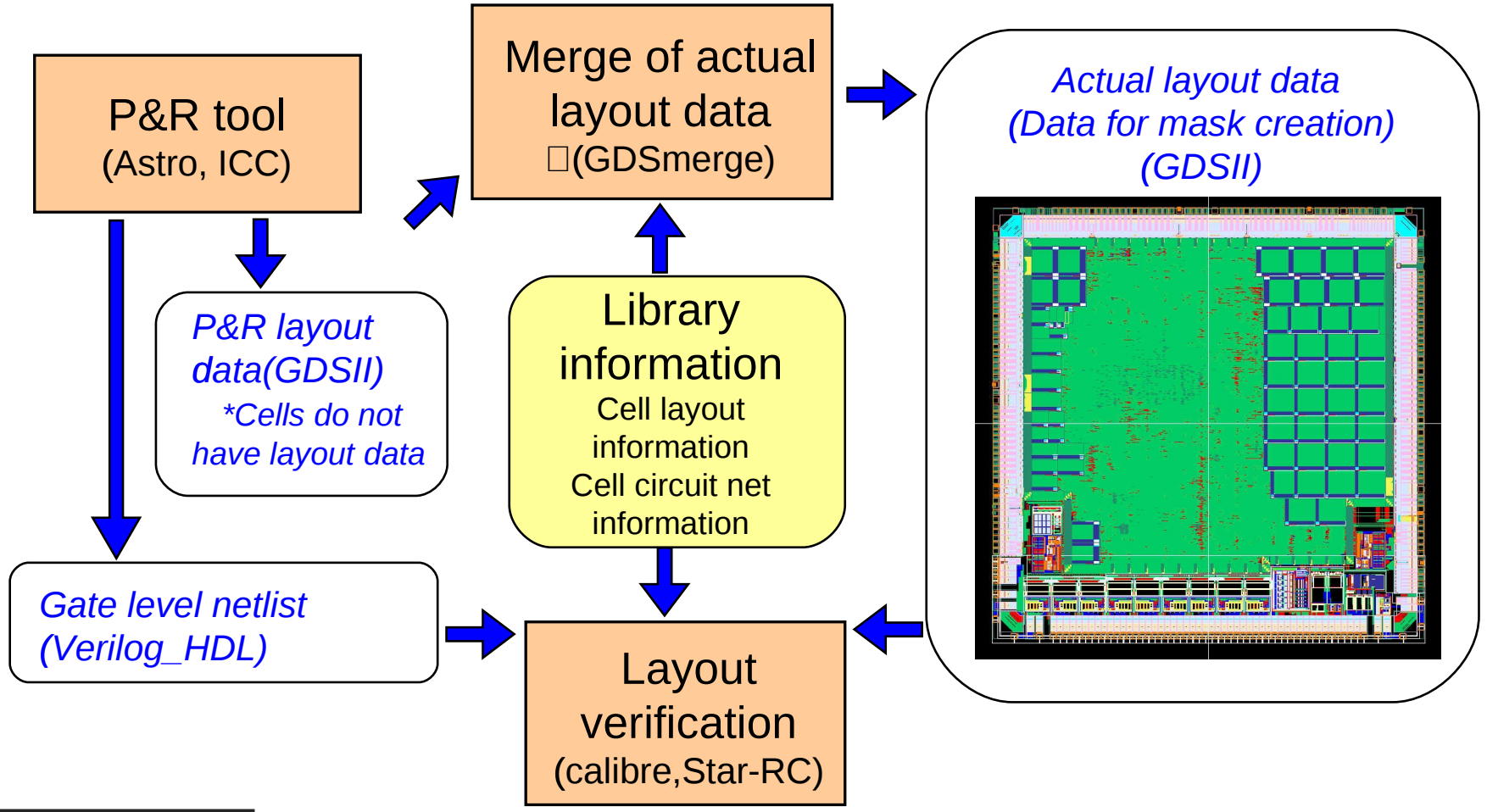


The delay value is reduced due to same phase noise and increased due to reverse phase noise.

There is a possibility of new timing constraint violation.

6/ P&R design flow Actual data generation

◆The actual layout data (data for the mask creation) is generated by merging with P&R layout result(placement information) and a cell layout data from library.



6/ P&R design flow　Layout verification

◆Layout verification is the physical verification of data for mask creation.
□□ Main features are as follows.

Verification item	Input data	Content of verification
Connection check (LVS)	Logic net data Layout data	Extracts devices and connections topologically from layout data, and compares device connection of logic net data.
Electric rule check(ERC)	Layout data	Electric rule check of power supply, components, etc.
Design rule check(DRC)	Layout data	Geometrical dimension and Position check between figures in layout data.

- LVS □Layout vs Schematic □,ERC(Electrical Rule Check)
- DRC(Design Rule Check □

6/ P&R design flow

Layout verification for advanced technology

◆Following layout verification items are needed for deep sub-micron/nano technology except LVS,ERC and DRC.

□(1) Antenna effect verification

Since MOS Transistors are broken due to the charge applied to metal layers during wafer process, Antenna effect verification checks the ratio of Poly area and metal area which are in the same potential.

* Layout modification such as pulling up wirings to metal layer, addition of protection diodes is needed to the portions where antenna errors are found.

Antenna effect verification spec is described in process design manual.

(2) CMP occupation verification

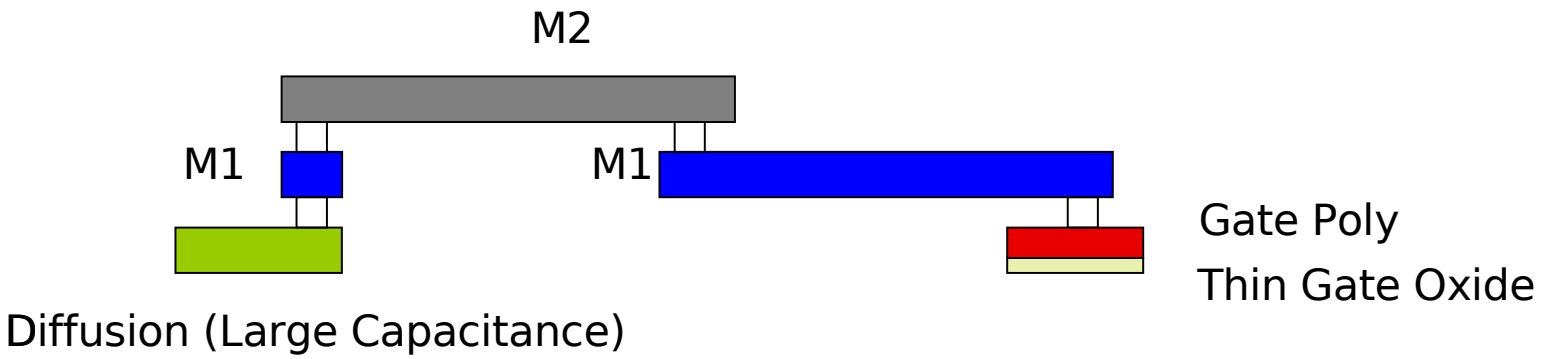
Chemical Mechanical Polishing(CMP) is adopted to make plane surface in wafer process, and to ensure uniform plane surface within a chip, a certain data occupation rule is needed.
CMP occupation verification checks this rule.

* If the rule is violated, the dummy patterns are added manually or automatically to the layers which do not satisfy the rule.
CMP occupation verification spec is described in process design manual.

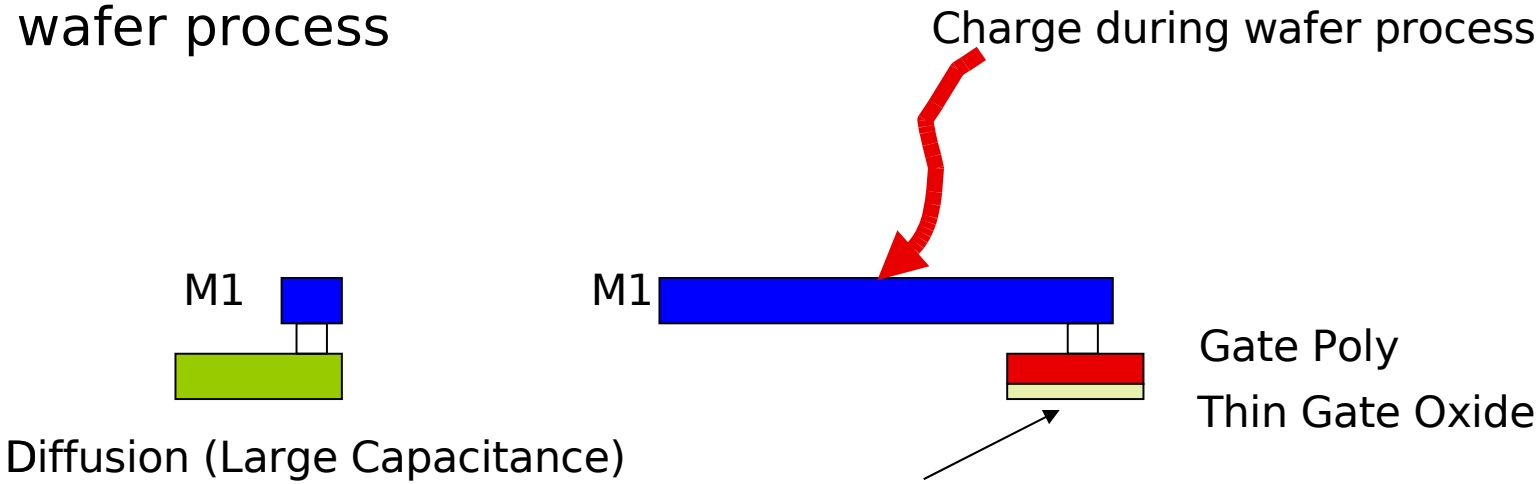
6/ P&R design flow

Antenna Effect

Finished structure



During wafer process

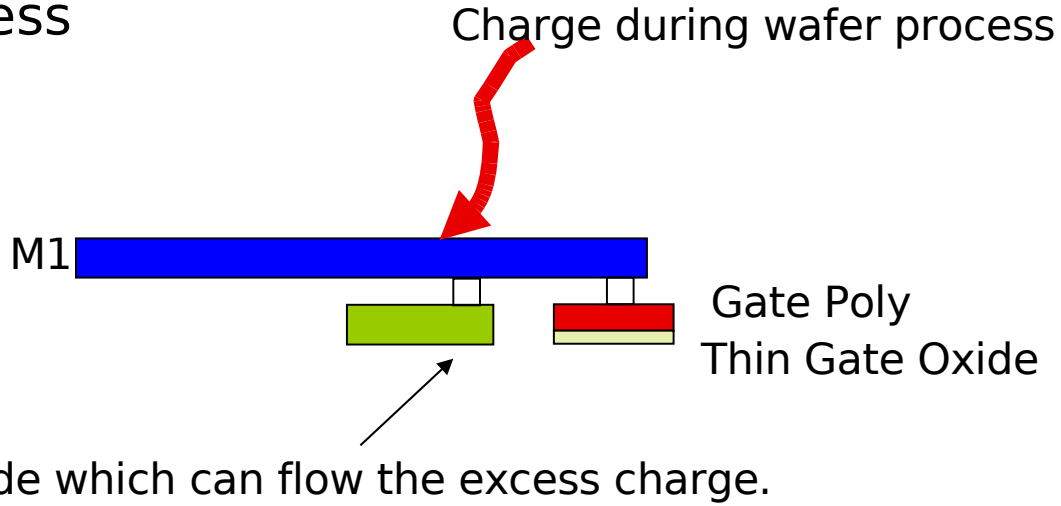


Due to the excess charge, gate oxide breaks down.

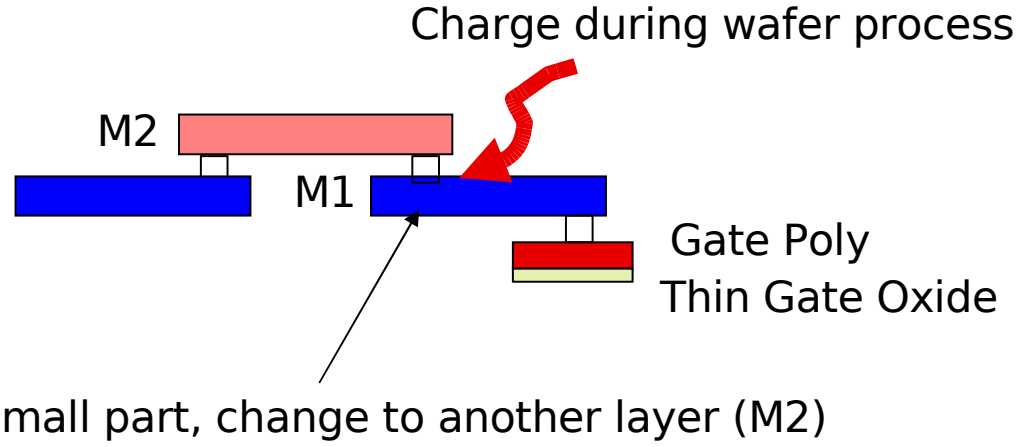
6/ P&R design flow

Protection of Antenna Effect

During wafer process



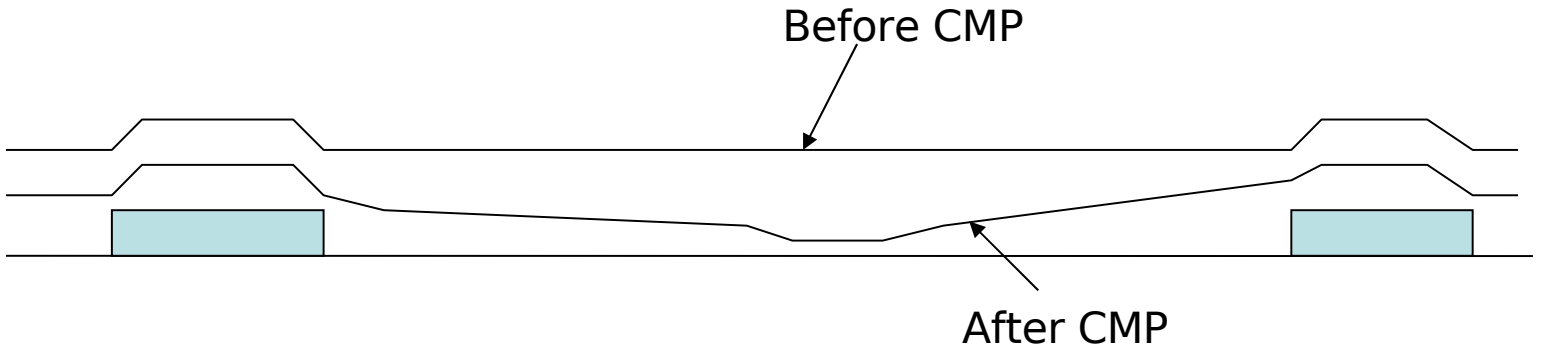
Prevent of Antenna Effect at layout phase



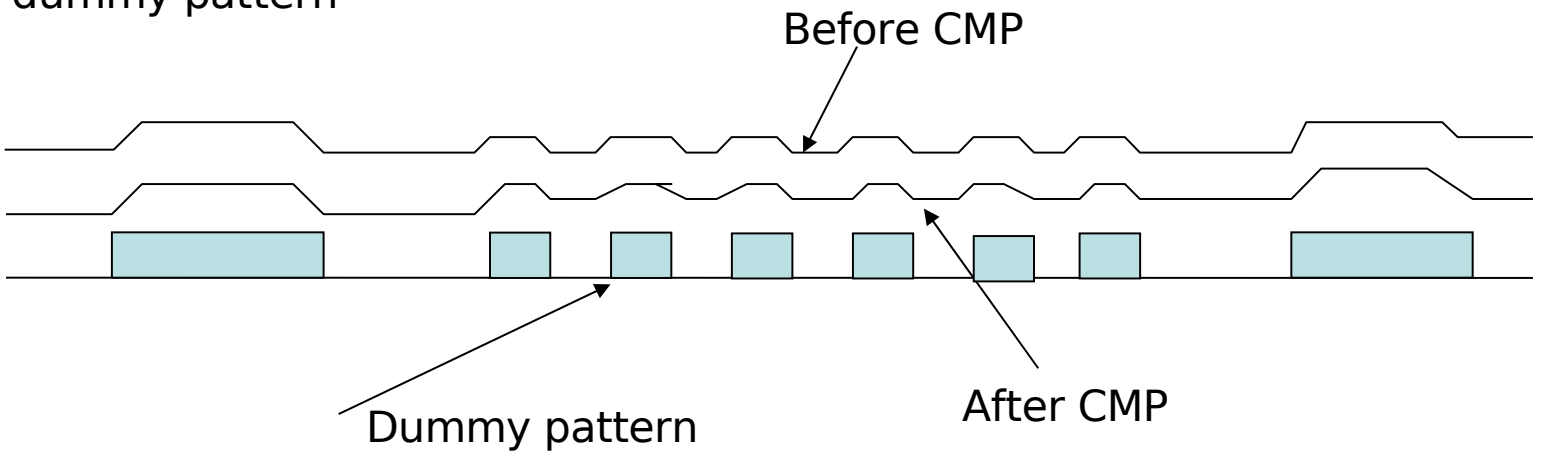
6/ P&R design flow CMP occupation verification

Dummy pattern insertion

Without dummy pattern



With dummy pattern



6/ P&R design flow

ECO(Engineering Change Order)

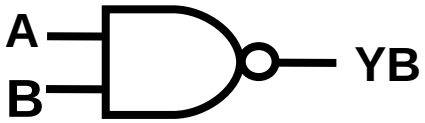
As explained in P&R design flow, we need ECO several times before fixing the layout data.
It is not practical to re-layout from the beginning.
For easy ECO, we place spare gates(about 2% of logic) to the original design.
When we need to replace cells with much drivability to meet the timing constraints or fix the design errors, we use these spare gates and revise the design by modifying metal wirings.

Reference

CMOS IC LAYOUT
– Concepts, Methodology, and Tools
By Dan Clein
Newnes, 2000

Cell Example:2 inputs NAND

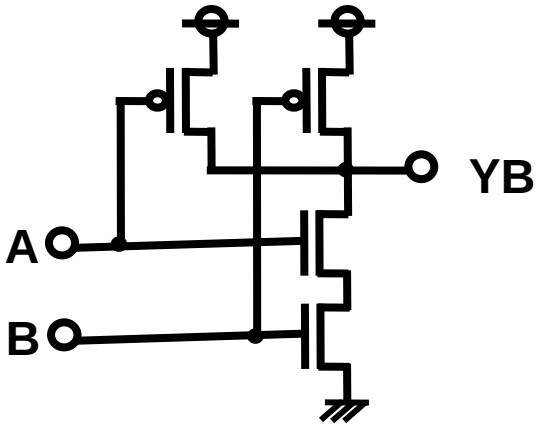
Logic Symbol

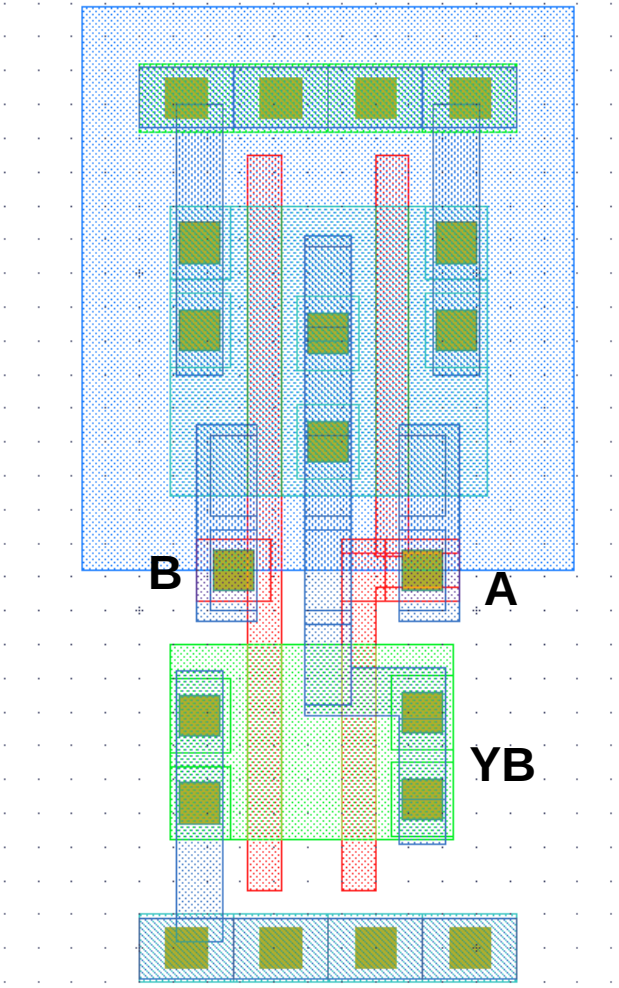


Truth Table

Input		Output
A	B	YB
H	H	L
L	X	H
X	L	H

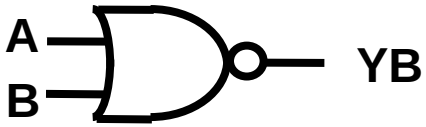
Circuit





Cell Example:2 inputs NOR

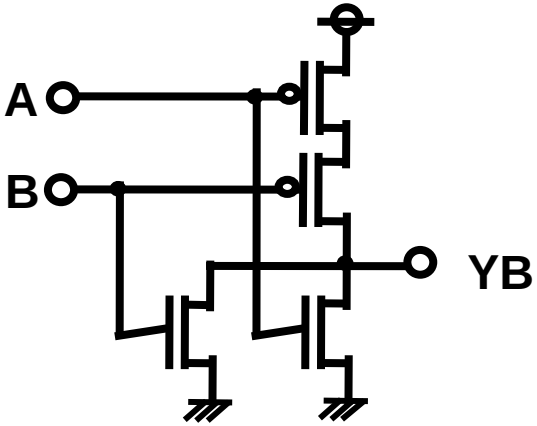
Logic Symbol

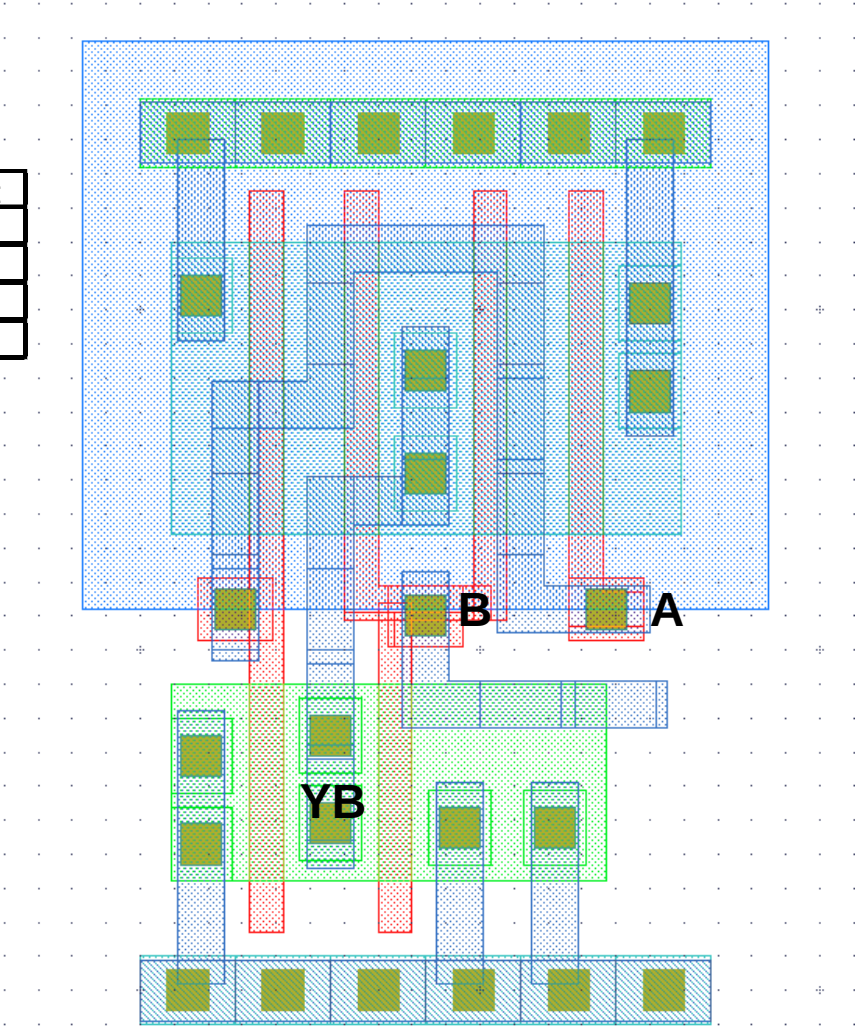


Truth Table

Input		Output
A	B	YB
H	X	L
X	H	L
L	L	H

Circuit





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