MOS Device: Basics

- MOSFET & Modeling -

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Lecture 4

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(6) CMOS (Complimentary MOSFET)

We have learned N-channel MOSFET (NMOS) and its operation, so far.

Current carrier is Electron!

The same model for P-channel MOSFET (PMOS) can be derived by just changing Impurity type and biasing polarity.

Current carrier is Hole in PMOS!

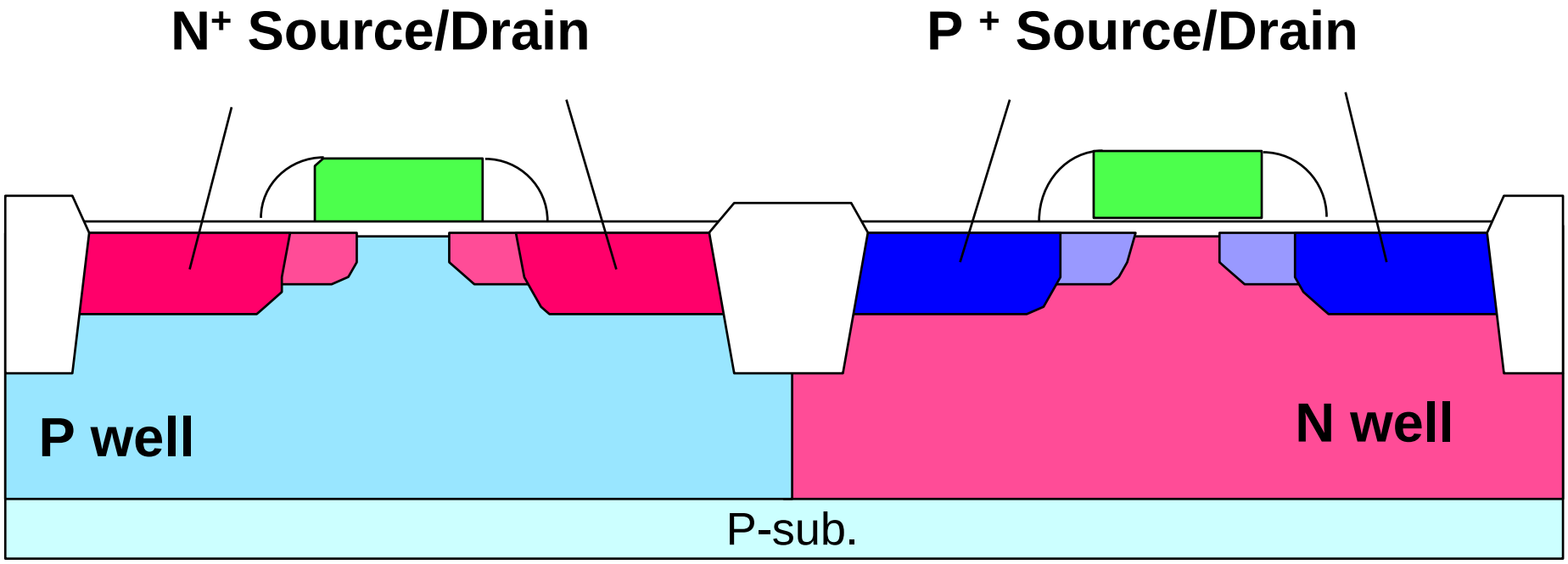
CMOS is circuit composed with both NMOS and PMOS:

- It provide ideal switch (charging & discharging)
- Low power circuit can be achieved with CMOS

→All the updated LSIs are fabricated with CMOS process!

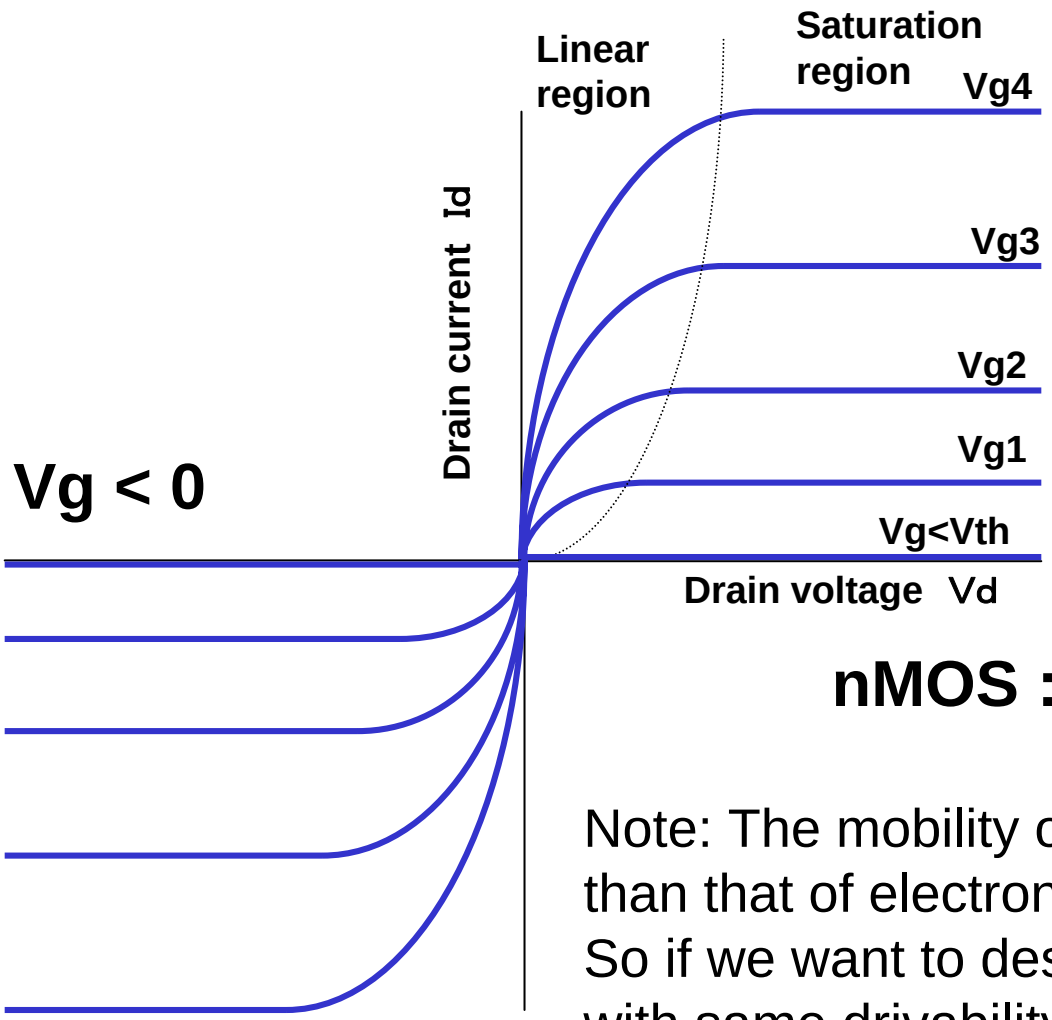
CMOS Structure

CMOS stands for Complementary MOS and both NMOS and PMOS transistors are formed on the same substrate.



N channel MOSFET(NMOS) **P channel MOSFET(PMOS)**

Characteristics of CMOS



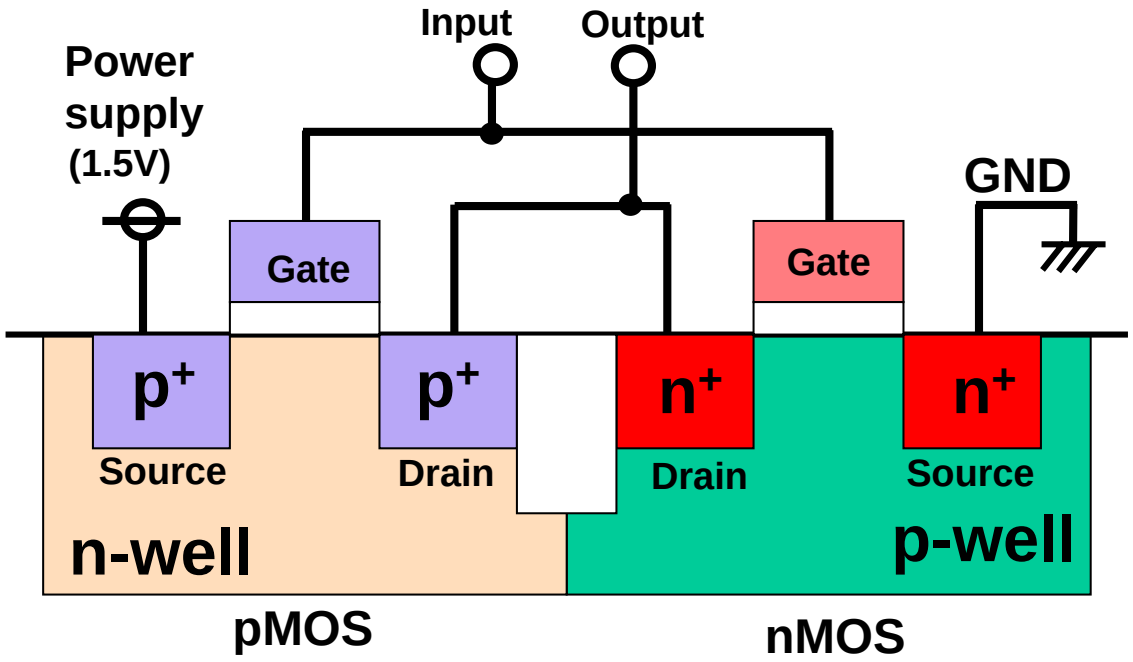
pMOS : Vg < 0

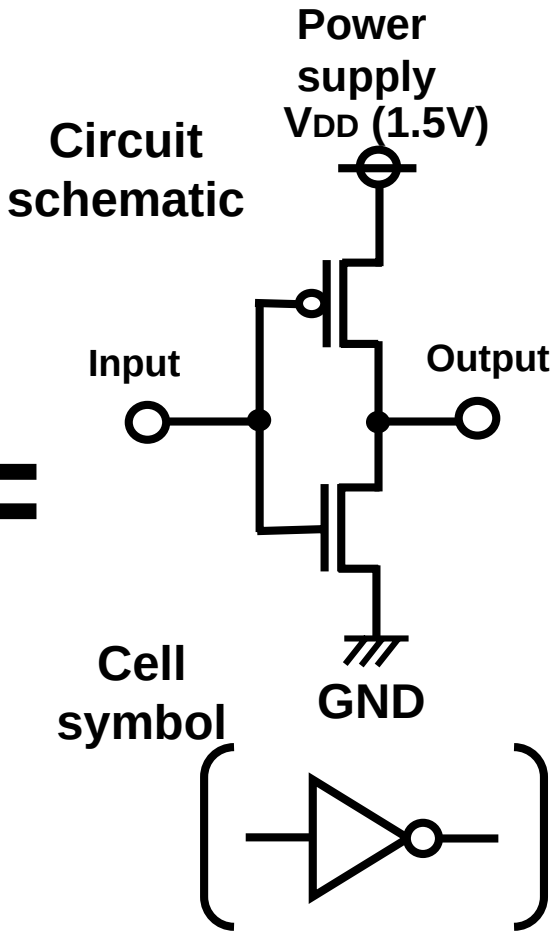
nMOS : Vg > 0

Note: The mobility of hole is smaller than that of electron (~1/2).
So if we want to design NMOS and PMOS with same drivability, Wp should be larger than Wn.
Wp,Wn: Gate width of PMOS and NMOS.

CMOS Inverter Circuit

<CMOS inverter Structure >

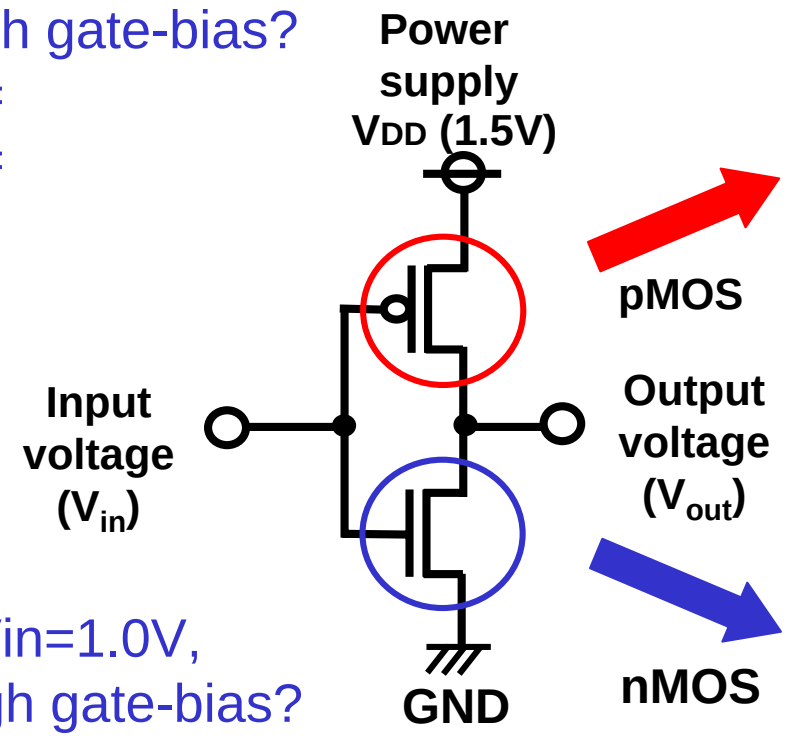




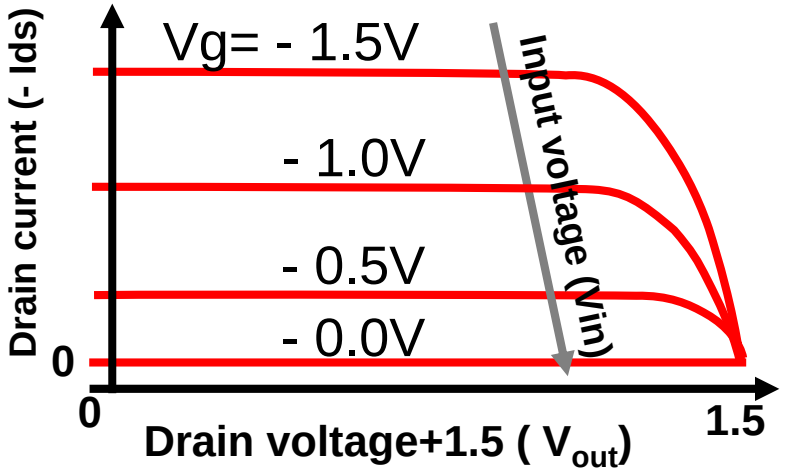
Simplest logic circuit with a pair of pMOS and nMOS transistors

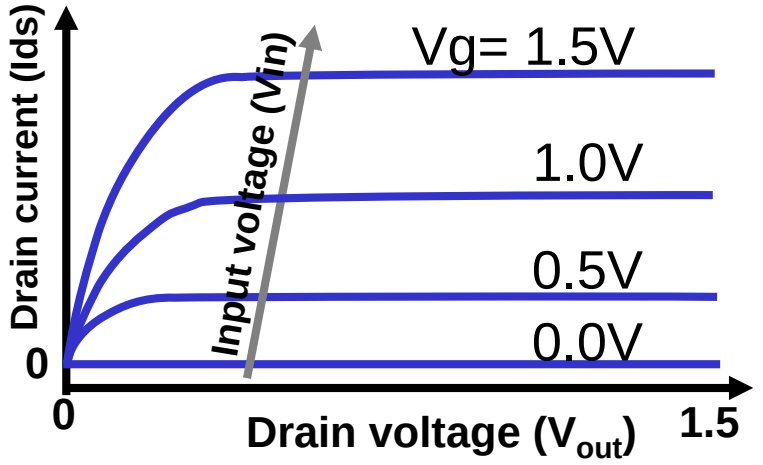
Current Characteristics

When Vin=0.5V,
How high gate-bias?
nMOS=
pMOS=



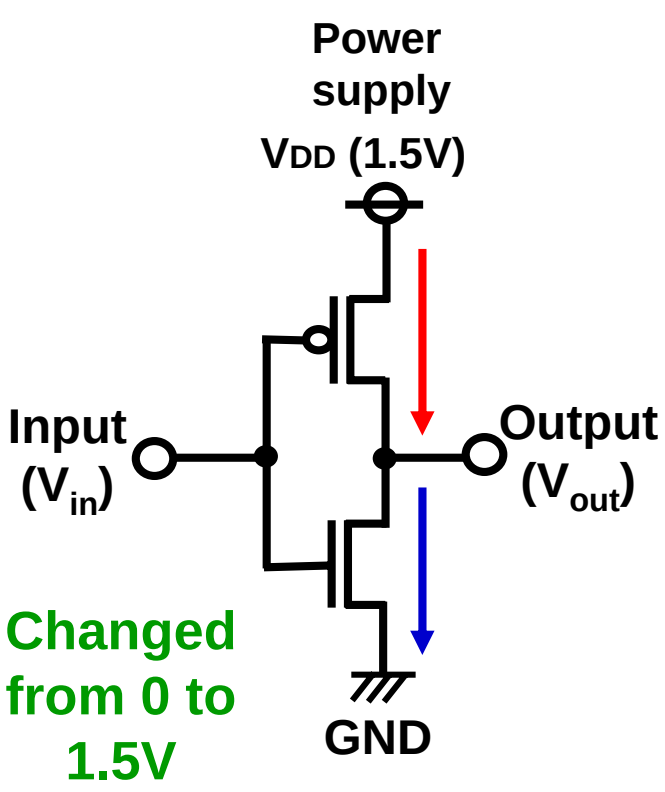
When Vin=1.0V,
How high gate-bias?
nMOS=
pMOS=

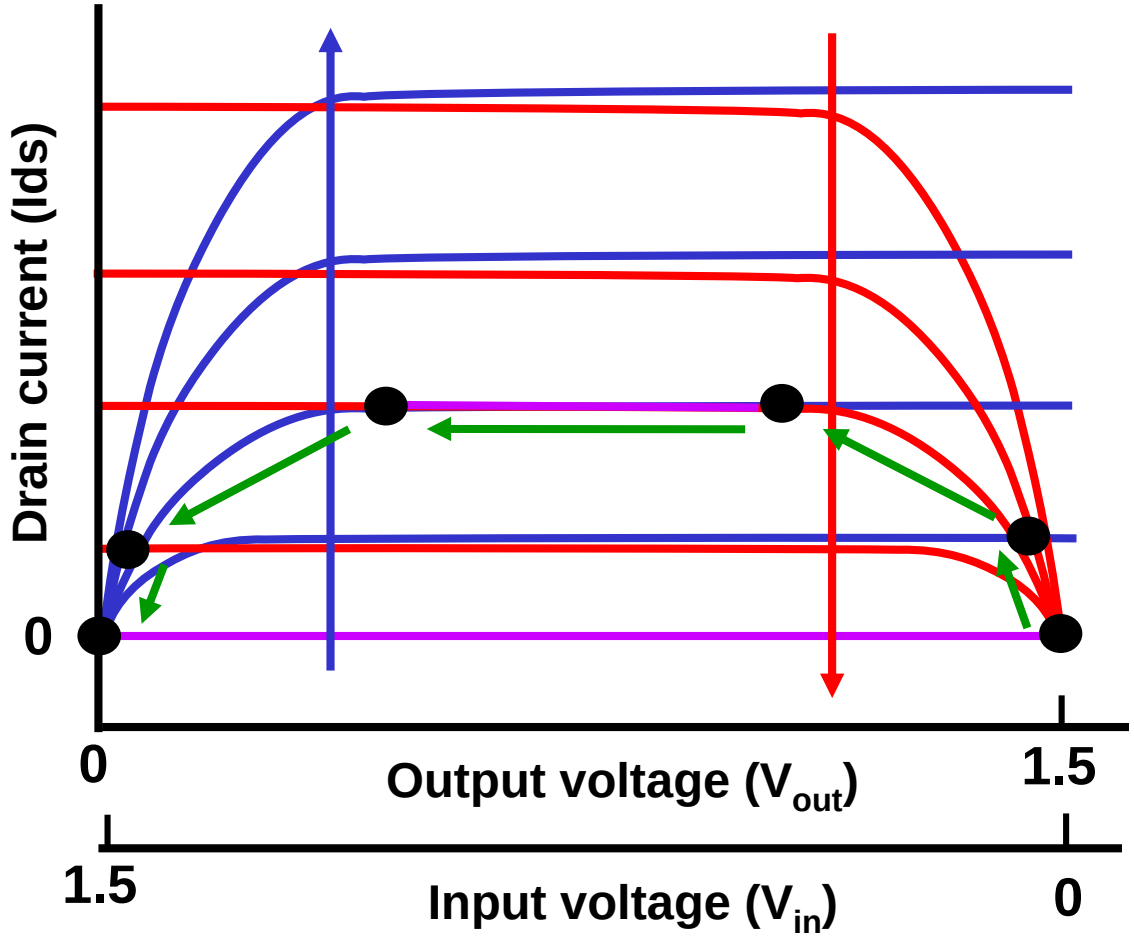




Inverter characteristics are defined by current characteristics of both transistors.

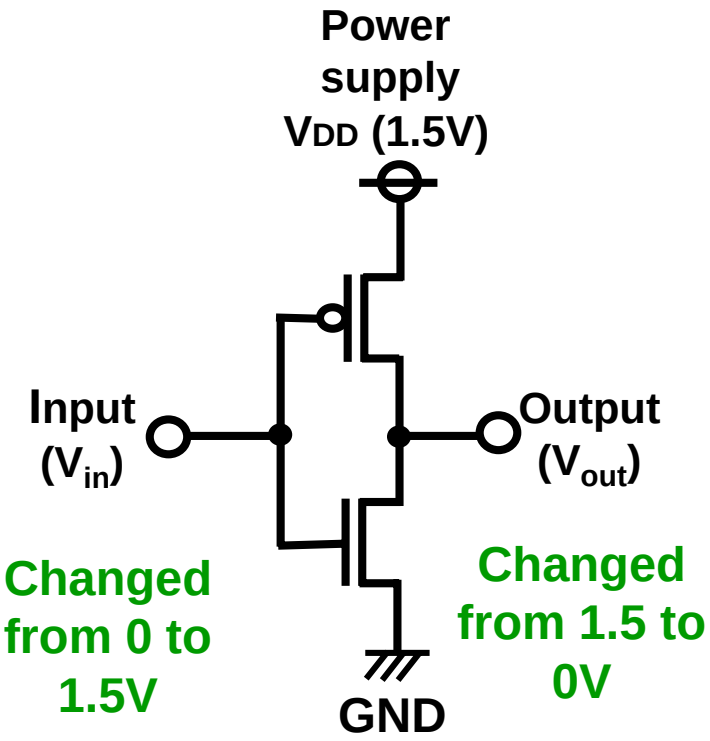
Behavior

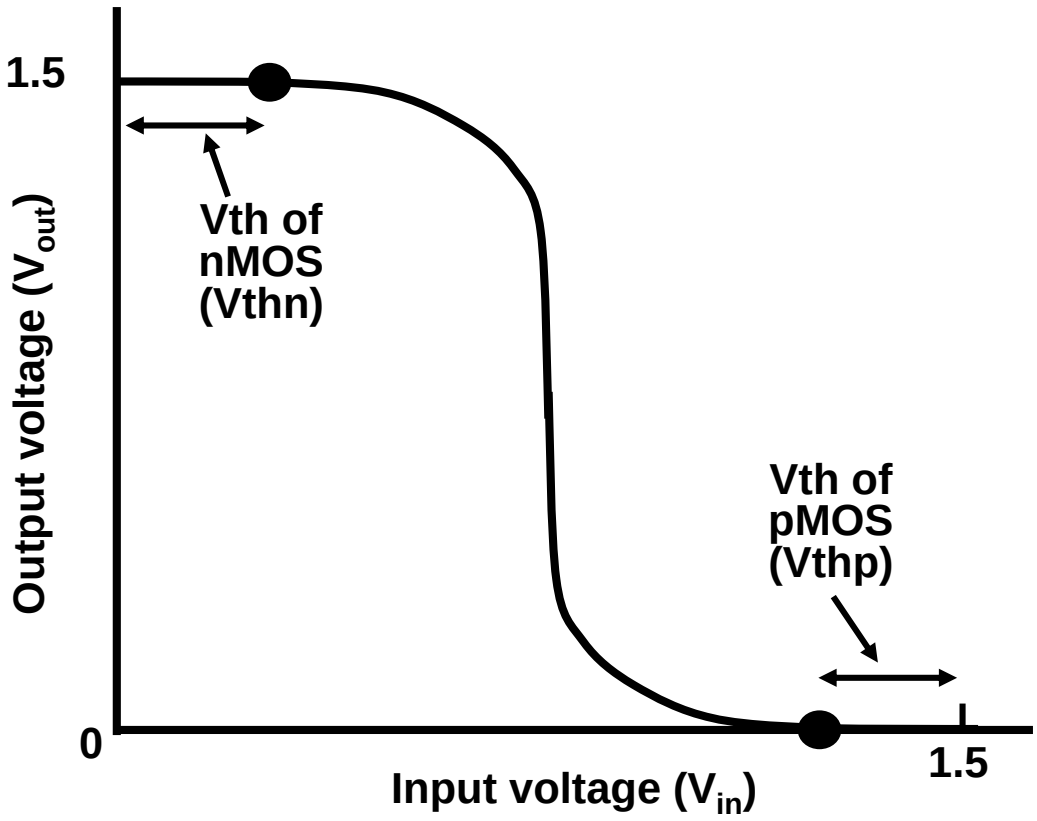




Output voltages (V_{out}) are determined by intersection points (● mark) of pMOS and nMOS current curves.

I/O Characteristics





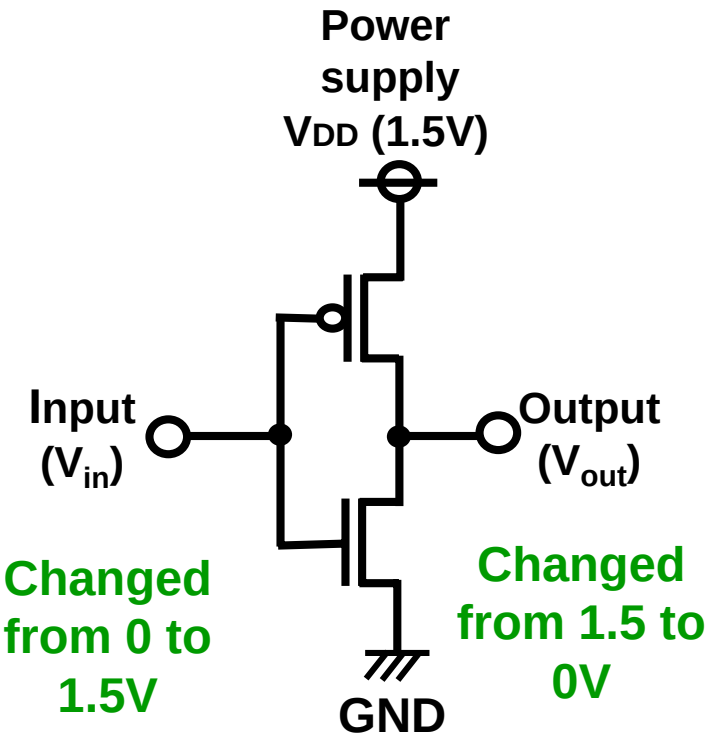
Signal logically inverted from input appears at output: inverter

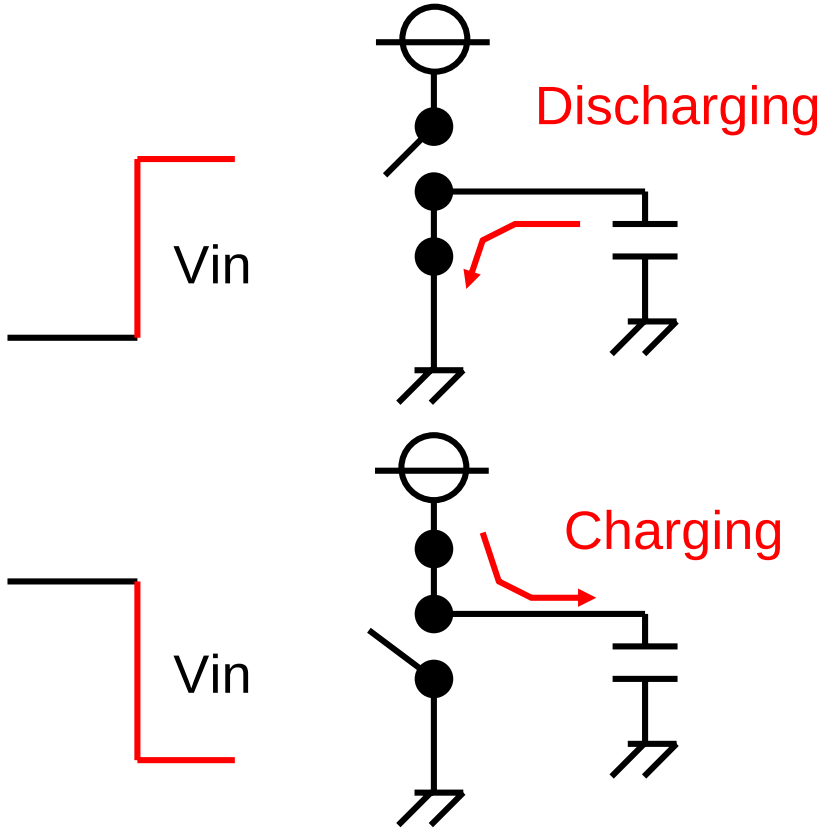
Ideal switch operation of CMOS

When Vin swings from 0 to 1, NMOS=ON and PMOS=OFF

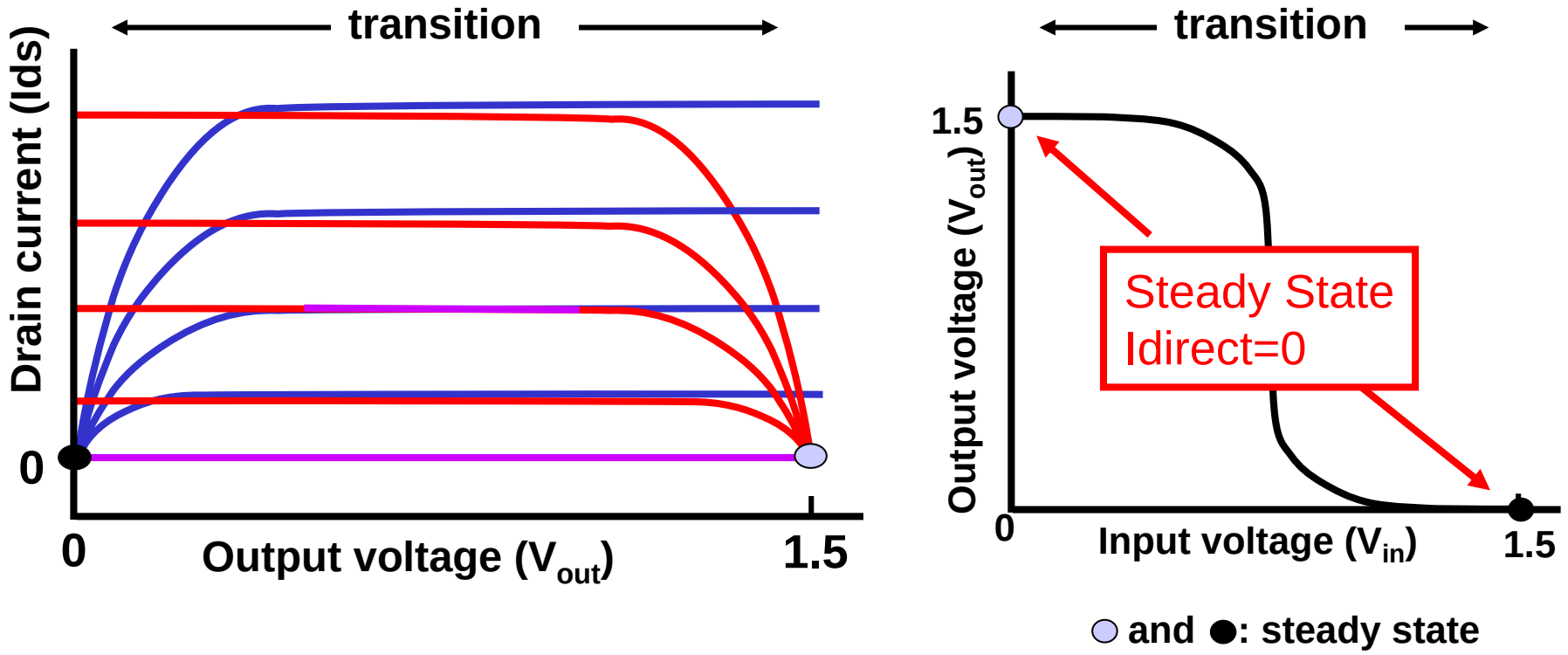
When Vin swings from 1 to 0, PMOS=ON and NMOS=OFF

It gives ideal switching operation.





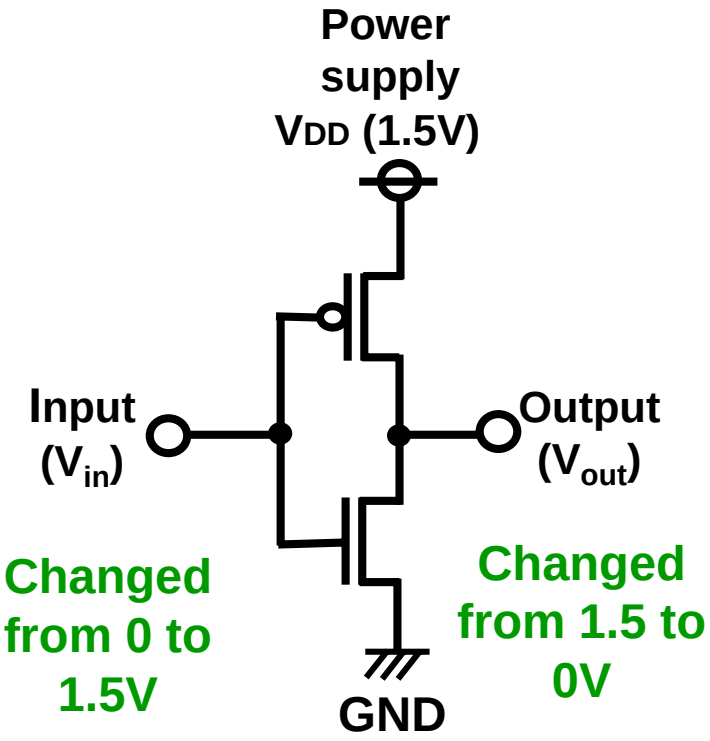
Another Merits of CMOS Inverter

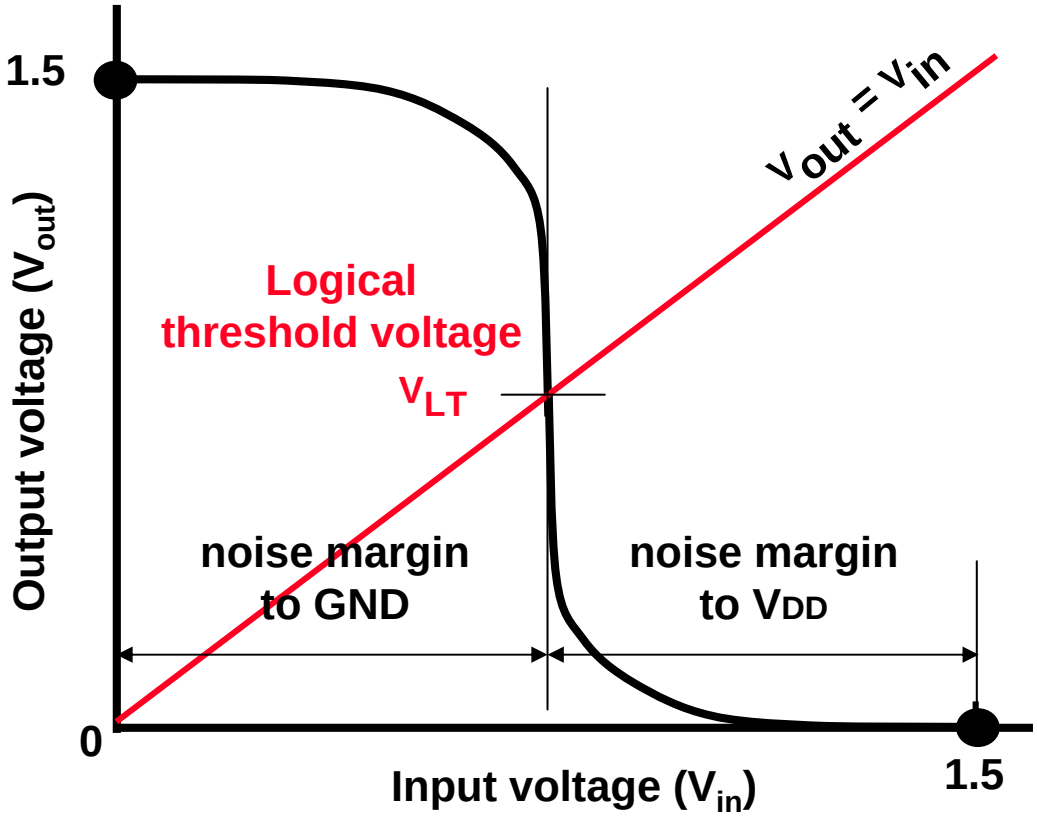


Complementary Operation

Either nMOS or pMOS is ON in steady state: no direct current flow.
Input and output voltages swing from 0 to 1.5v (V_{DD}).

Logical Threshold Voltage





To set logical threshold voltage of each gate at the same level is important to secure noise margin: $V_{LT} = V_{DD}/2$

Features of CMOS Circuit (Summary)

Advantage	Disadvantage
(1) Low power dissipation	(1) Subject to Latch up
(2) Wide operating voltage range	(2) Complicated wafer process
(3) Large noise margin	(3) Large device area
(4) Wide operating temperature	

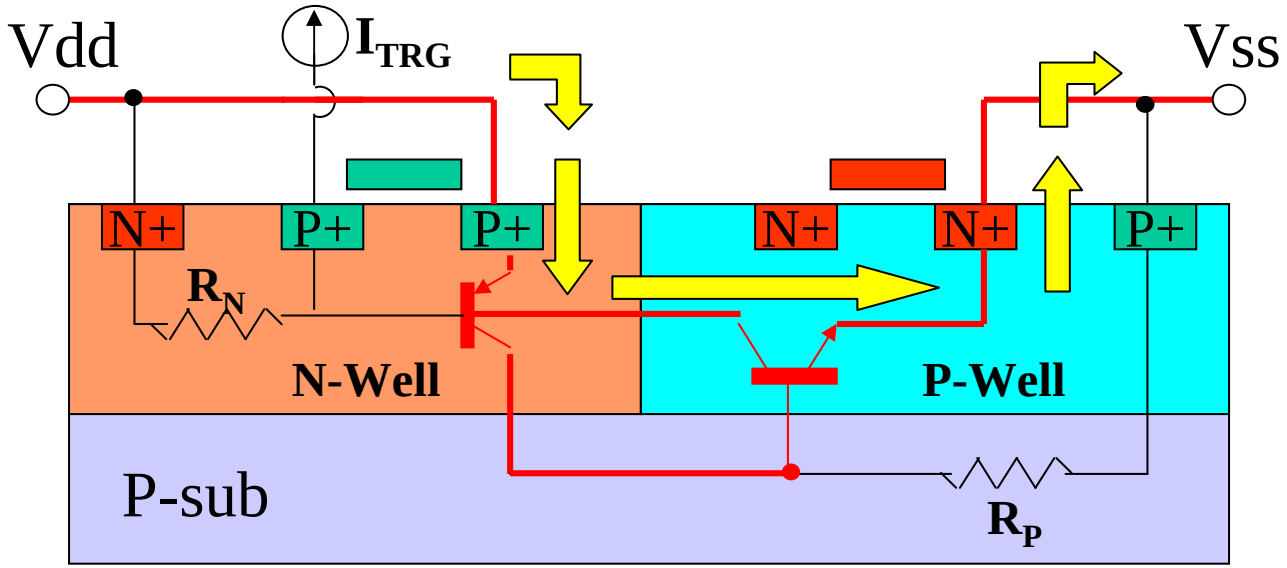
What is Latchup in CMOS?

One of the critical reliability phenomena of CMOS circuits.

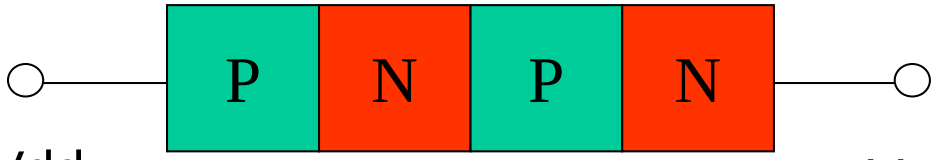
Parasitic PNPN structure (Thyristor) of CMOS causes latchup, which may give fatal damage on LSI.

Parasitic CMOS-Thyristor and Equivalent Circuit

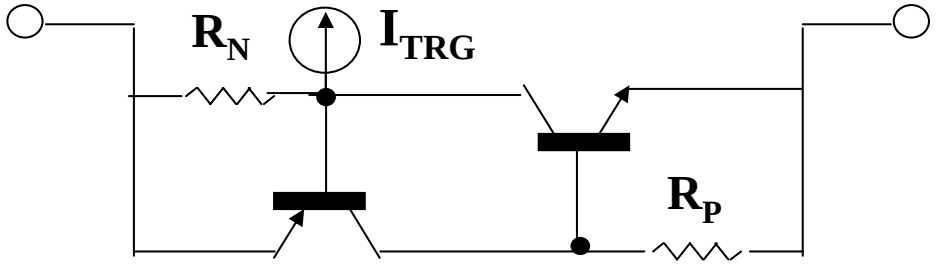
CMOS &
Parasitic Thyristor



Basic Thyristor model



Equivalent CKT



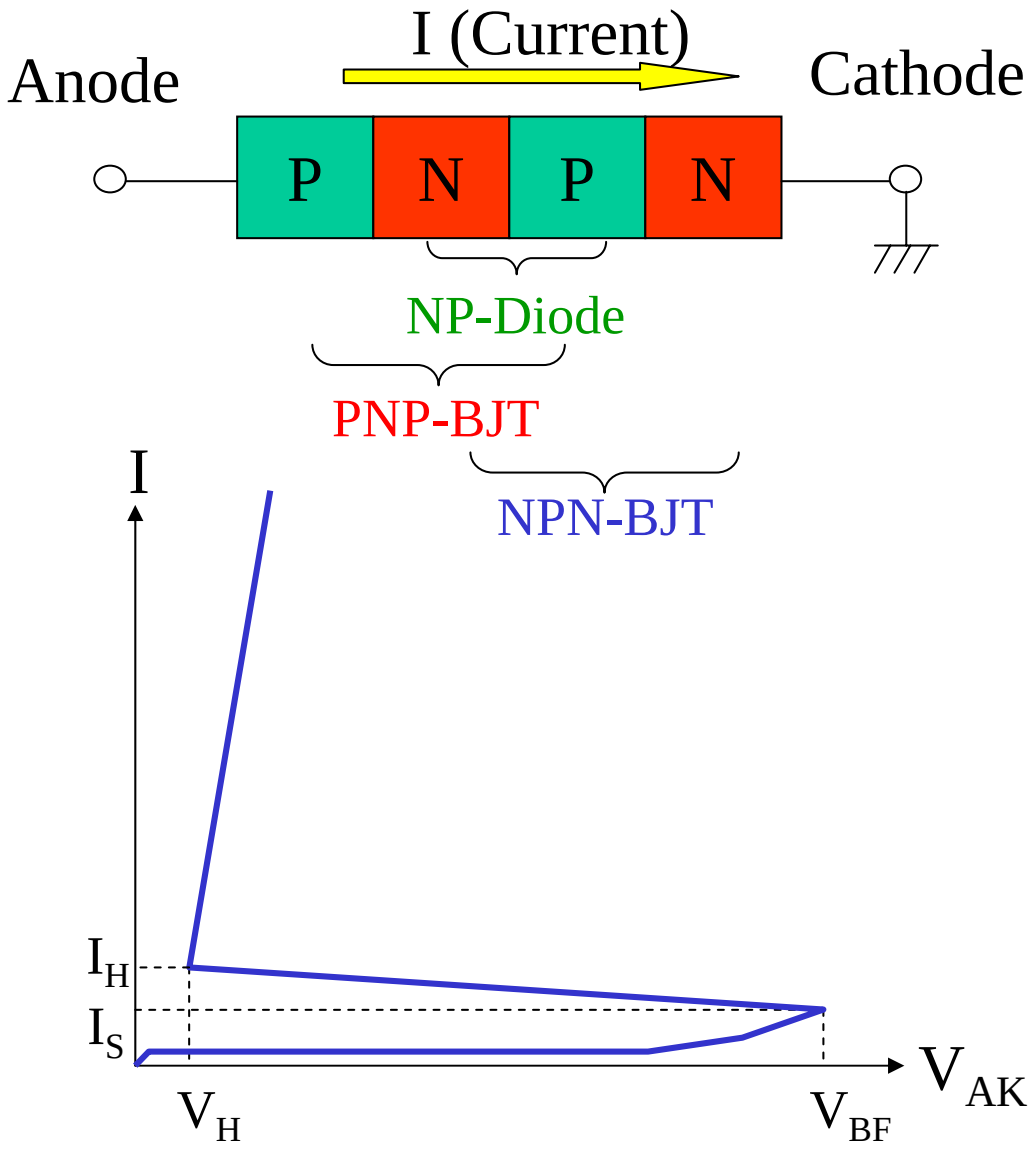
Thyristor I-V characteristics

When you apply Anode voltage V_{AK}, NP-Diode at the center is reverse-biased.

When the V_{AK}, $>V_{BF}$, high electric field across the NP-Diode causes electrical breakdown and generate Electrons and Holes.

Generated Electrons trigger on the PNP-BJT! Resulting Hole current turns on the NPN-BJT.

Therefore, both of PNP & NPN-BJTs turn on, which results in large current flow from Anode to Cathode.



How to prevent Latchup?

To achieve hard to turn-on the PNP & NPN-BJT

- Reduce the R_N and R_P
- Closed layout of well-contact to active MOS-FETs (to suppress a rise of substrate-bias) → Layout Rule

To reduce current gain h_{FE} for both of the BJTs

- Deep Wells
- Retrograde Well (doping profile control)
- Keep long-distant between N-Well and P-Well (to reduce the h_{FE} of Lateral BJTs) → Layout Rule

Practical solution can be described in Layout Design Rule!

Summary of CMOS

CMOS is the device we are using now, since it provide perfect complimentary operation for digital switching.

Low power, say in Mobile Phone, can be achieved with only CMOS device and circuits.

If you know NMOS operation and model equation, PMOS is a simple (but sometimes confusing) extension.

Structure: Just replace N⇔P-Type impurities

Biasing: Just changing polarity

NMOS; Vs=0, Vd>0, Vg>0, Vth>0, Vb≦0

PMOS; Vs=0, Vd<0, Vg<0, Vth<0, Vb≧0

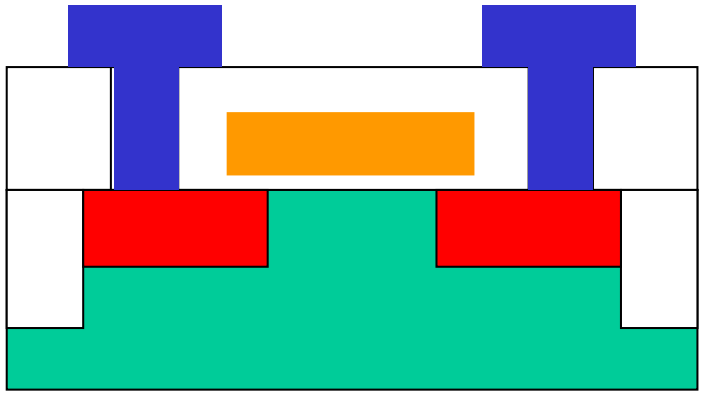
Quiz

(1) Tell CMOS's best advantage over NMOS or PMOS circuits.

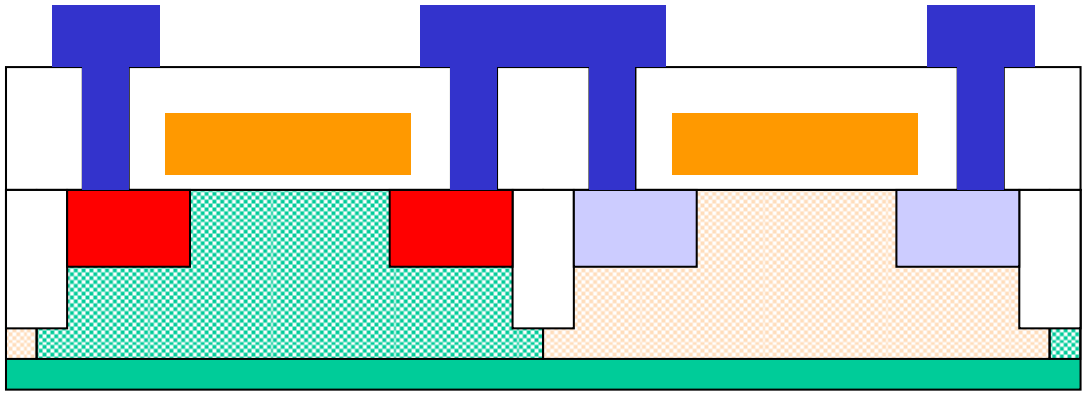
(2) Tell CMOS's worst disadvantage over NMOS or PMOS circuits.

(3) How many masks is required to form the NMOS structure.

(4) How many masks is required to form the structure of CMOS.



NMOS



CMOS

(7) Scaled-down of MOSFET

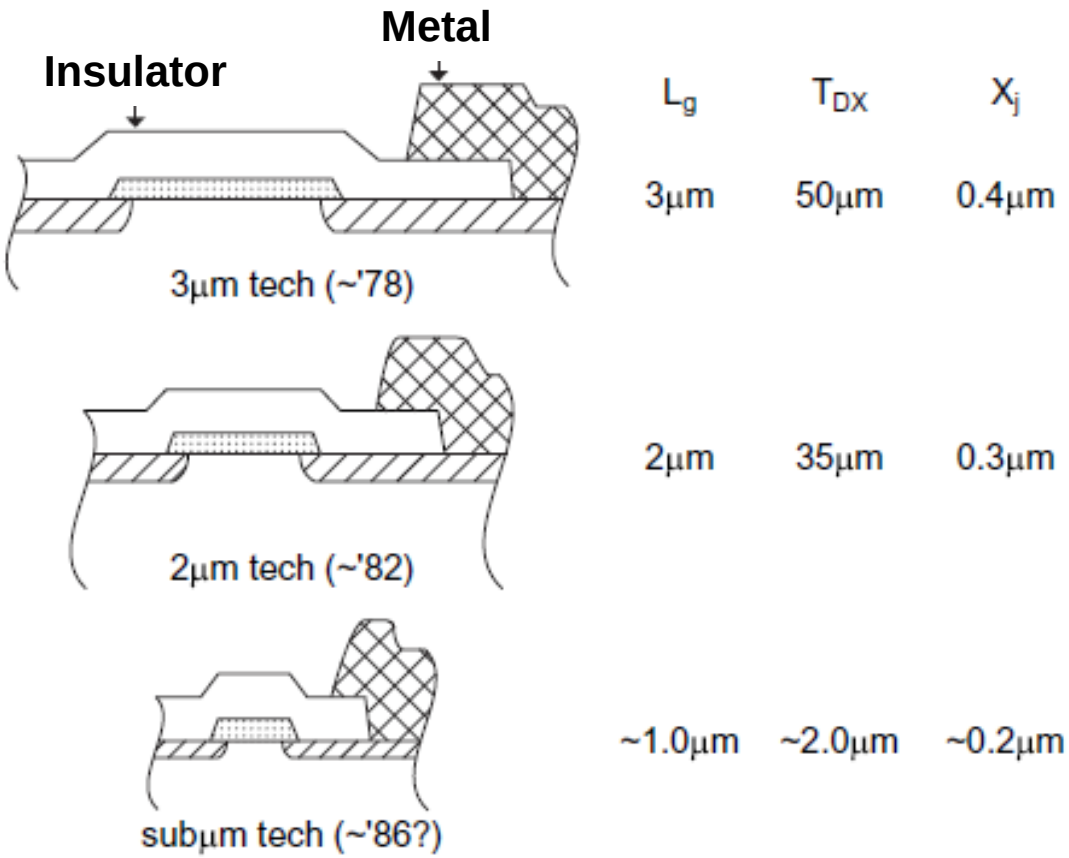
Why we need scale-down MOSFET and Process?

Better LSI performances:
- High speed
- Low power

High integration and functionality:
- Many functions
- Many logics
- Many MOSFETs

Low cost:
- Small chip
- Many chips/wafer

Shrunk an MOSFET: Trend of scale-down in dimensions



	L_g	T_{DX}	X_j
3μm tech (~'78)	3μm	50μm	0.4μm
2μm tech (~'82)	2μm	35μm	0.3μm
subμm tech (~'86?)	~1.0μm	~2.0μm	~0.2μm

Example of Shrinking MOSFET

Historically, LSI performance has been improved by Scale-down (Shrunk) of MOSFET and Process.

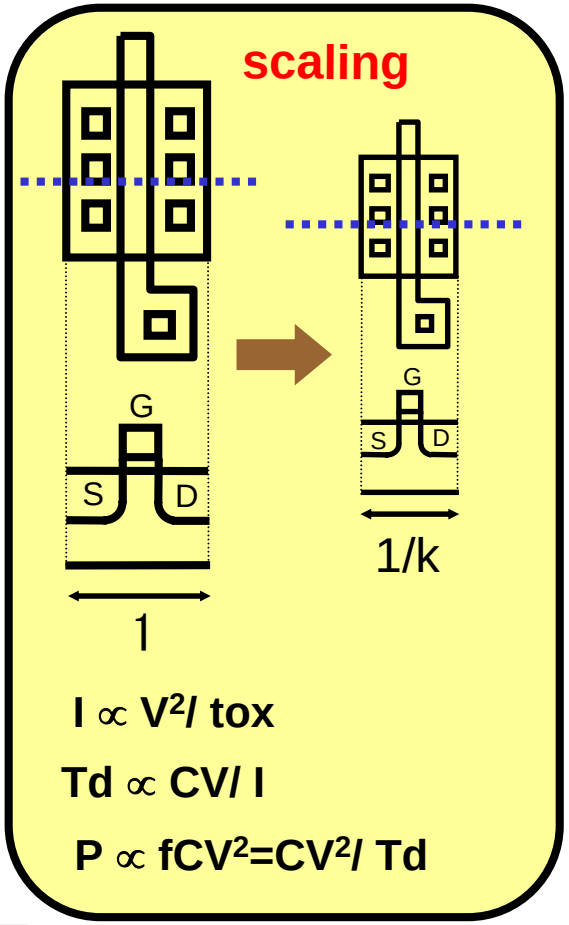
New LSI technology development totally rely on this trend.

Now in 2007, we are developing 45nm technology.

Scaling rules (ideal)

k: scaling factor

	To keep voltage constant (Old)	To keep electric field Constant (Now)
One side of length (X)	1/k	1/k
Gate oxide thickness (tox)	1/k	1/k
Power supply voltage (V)	1	1/k
Electric field strength (E)	k	1
Electric current (I)	k	1/k
Capacity (C)	1/k	1/k
Delay time (Td)	$1/k^2$	1/k
Power consumption (P)	k	$1/k^2$
Power density (P/X^2)	k^3	1



$I \propto V^2/ tox$

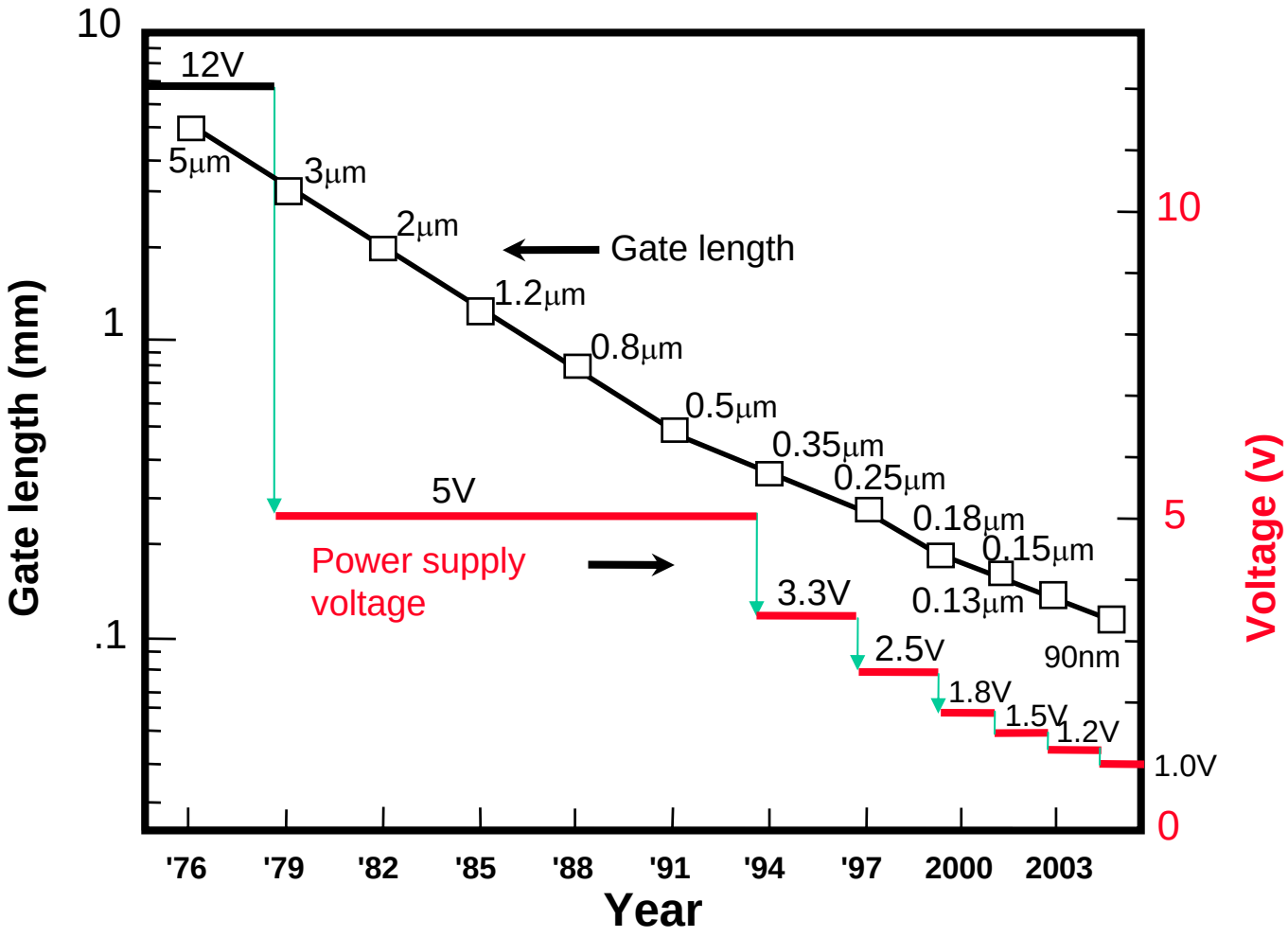
$Td \propto CV/ I$

$P \propto fCV^2=CV^2/ Td$

- The effects of scaling are prominent in establishing high speed, low power consumption, and high density.
- Till now, these effects have been realized by continuously developed process generations.

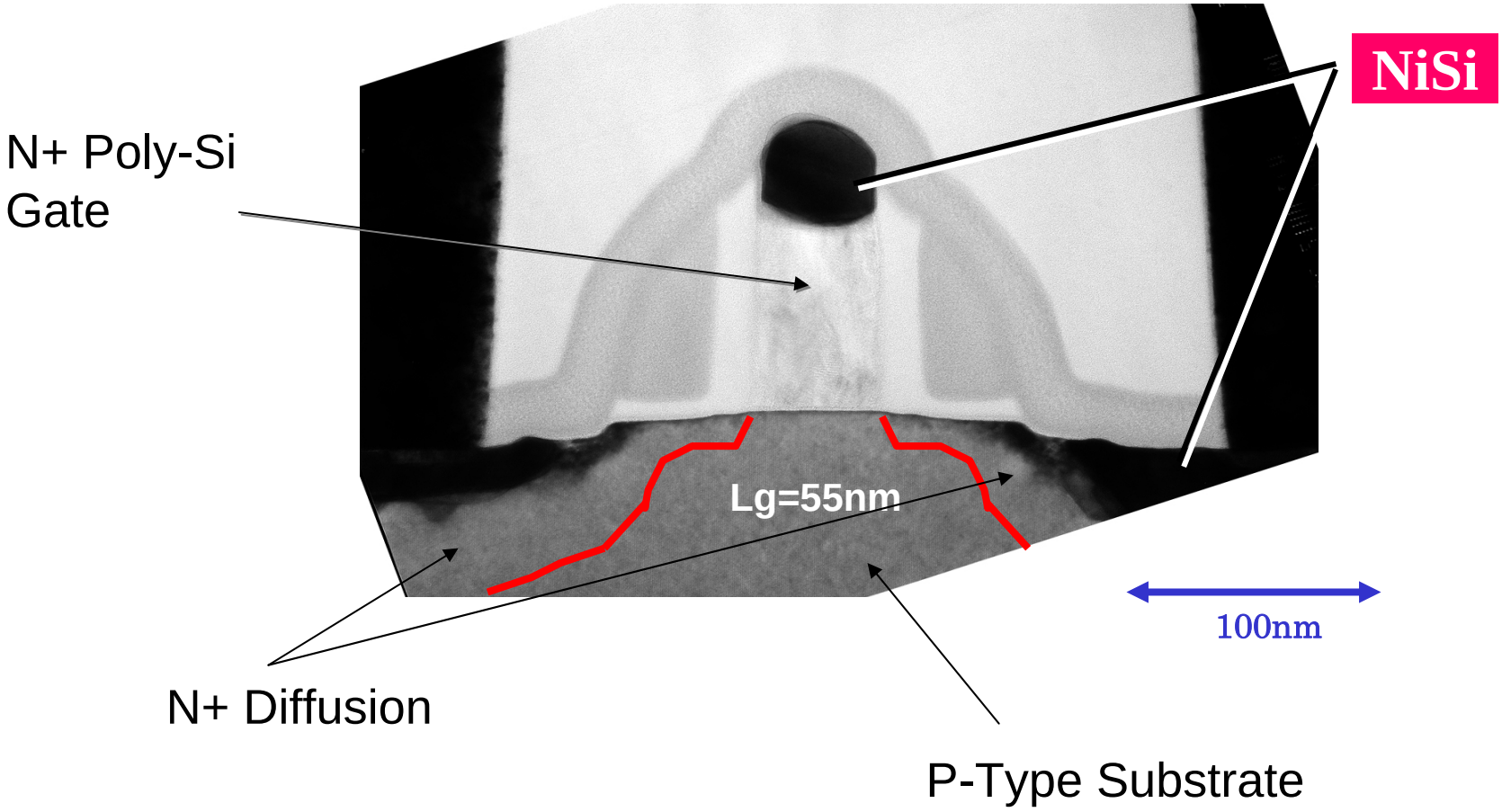
Success history of semiconductor development !! However…

Trend of Scaling & Power Supply Voltage



After 0.35 μm generation, power supply voltage has been reduced to maintain electric field constant in gate oxide.

Updated sub-100nm MOSFET Structure



Limitation on Scaling Rule

1. Some items are not fully scaled

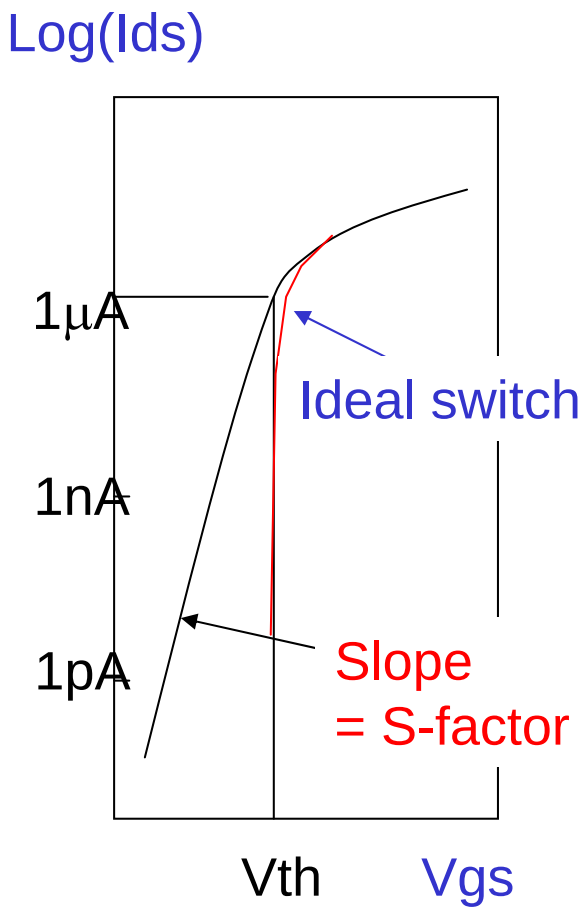
L: 1.0um -> 0.06um (1/17)…Aggressive
Tox: 20nm -> 1.5nm (1/13)
Vdd: 5V -> 1.2V (1/4)….Moderate

2. Drivability

I: 1/k
I/W: 1

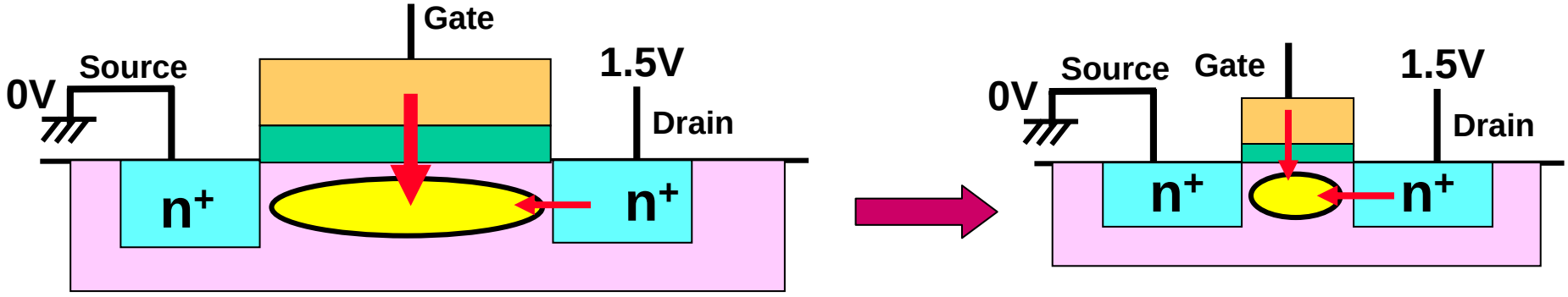
3. Un-scalable factors

Vth
S factor (Sub-threshold slope of drain current)
Inversion surface potential….



Short Channel Effect becomes glowing

Drawbacks: Short Channel Effect



Channel is controlled by gate

Channel is controlled by gate and drain

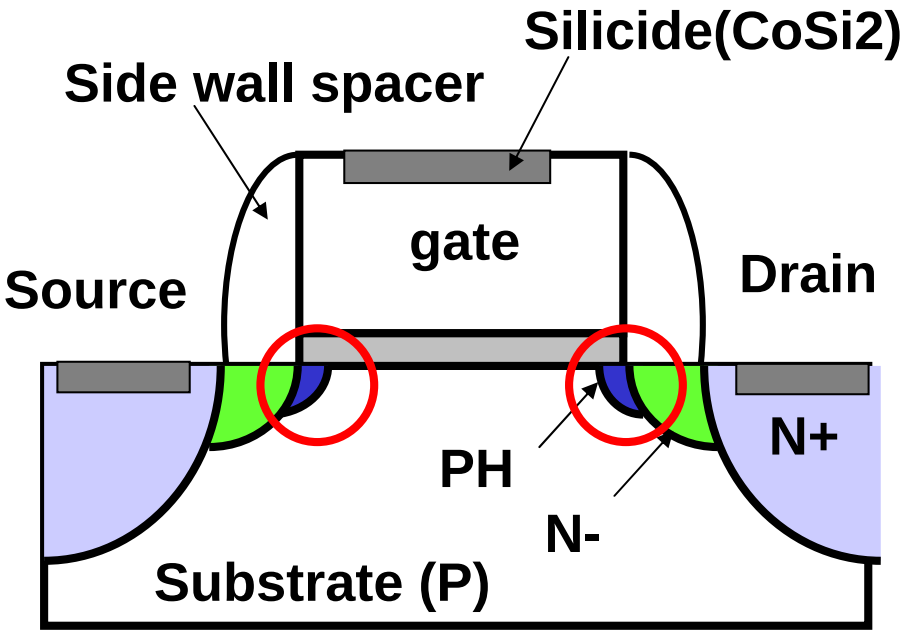
1. Increase in off state leakage current & poor Vth control

- Vth decrease (roll off) in shorter channel
- Vth is varied by drain voltage (Vth decrease)
- S factor increase

2. Ids does not increase in proportion to 1/L

→ How to prevent?

To overcome short channel effect: Impurity profile control becomes key issue



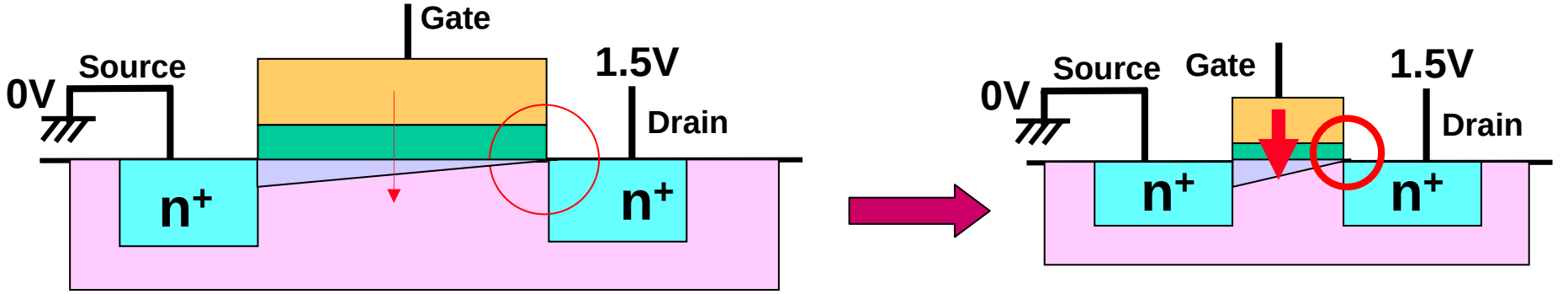
NMOS (Advanced structure)

To prevent Vth related problems (leakage current):

- lateral P^+ diffusions at S/D ends (PH layer)

The newly introduced P^+ impurities mitigate drain electric field effect, which results in a better Vth control.

Another Drawbacks: Reliability



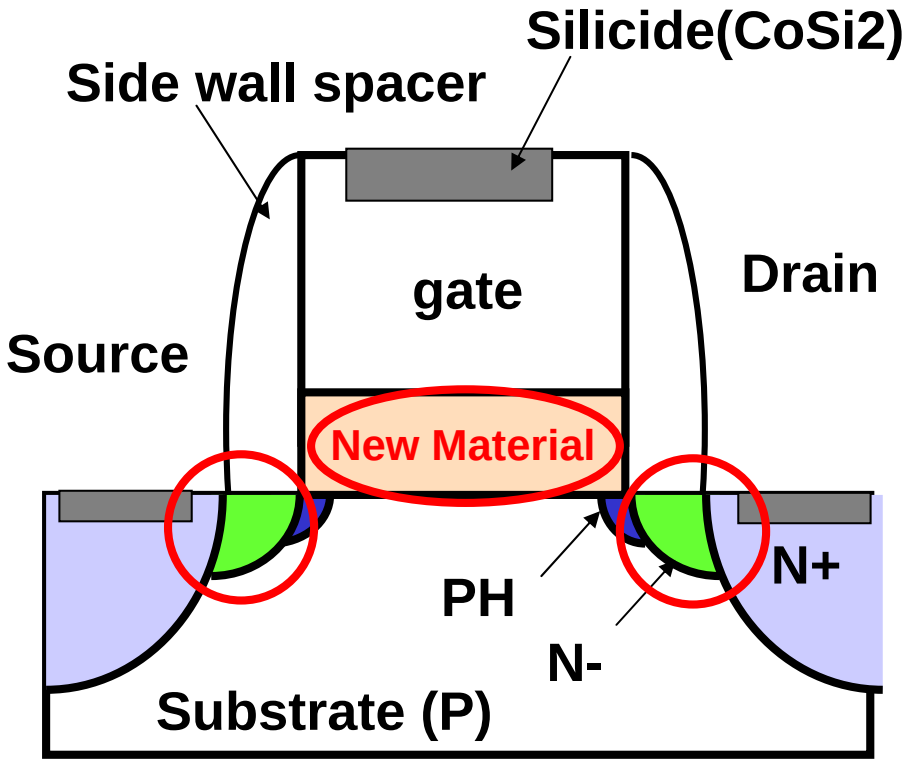
Negligible gate leak
Small local drain field

Increased gate leak to breakdown
Large local drain field

1. Gate oxide breakdown
   - Increased gate leak current
   - No MOSFET action (short circuited)
   → Functional failure during operation
2. Hot electron causes Isub and Vth-shift during operation
   → Long term performance degradation (reliability problem)

→ How to prevent?

To overcome Reliability problems: Impurity profiling and Material are key issue



NMOS (Advanced structure)

To prevent gate oxide breakdown (gate leakage current):

- New materials for gate oxide

  SiON, High-K(in Research)

To prevent hot carrier effect:

- N- diffusion at S/D ends

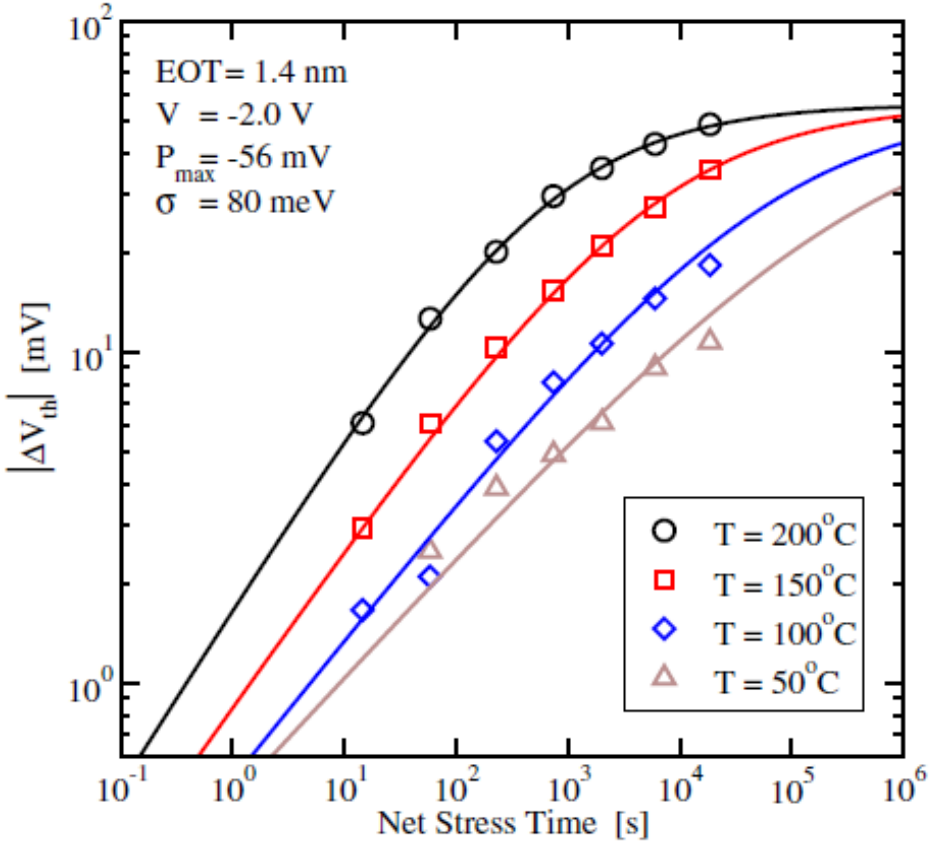
→mitigate local drain field

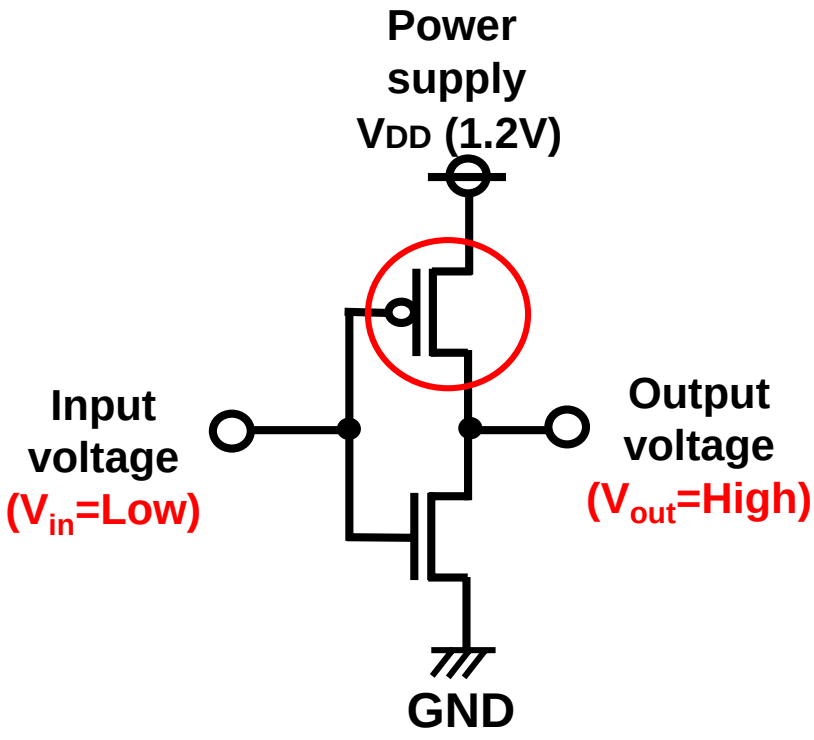
45-60nm process reliability: NBTI (Negative Bias Temperature Instability) in PMOS

IVthI increase during stand-by operation

@ Vgs=-Vdd, Vds=0V

The degradation is relaxed when stress-off





How to mitigate ?

- gate insulator material →High K
- circuit design →guard banding
- use relaxation mode

Summary of Shrink Process & Device

Shrink process is a royal road in LSI fabrication:

- It results in small chip and many-chips/wafer
  - Small chip → high yield!
  - many chip/wafer → allow low cost in production!

Therefore, even if there are many drawback in shrinking:

- short-channel effects,
- reliability problems,
- higher cost in fabrication tools, ….

many managers prefer:

"Continuous shrink the process and devices!"

What happen in < 45nm MOS Device? :

Performances

- Performance improvement is leveled-off
- Single core → Multi-core; higher performance by circuits

Power limit

- Increase leak-current (Sub-threshold, Ig)
- Multi-Vth circuit & Back-bias control; circuit level mitigation

Variability

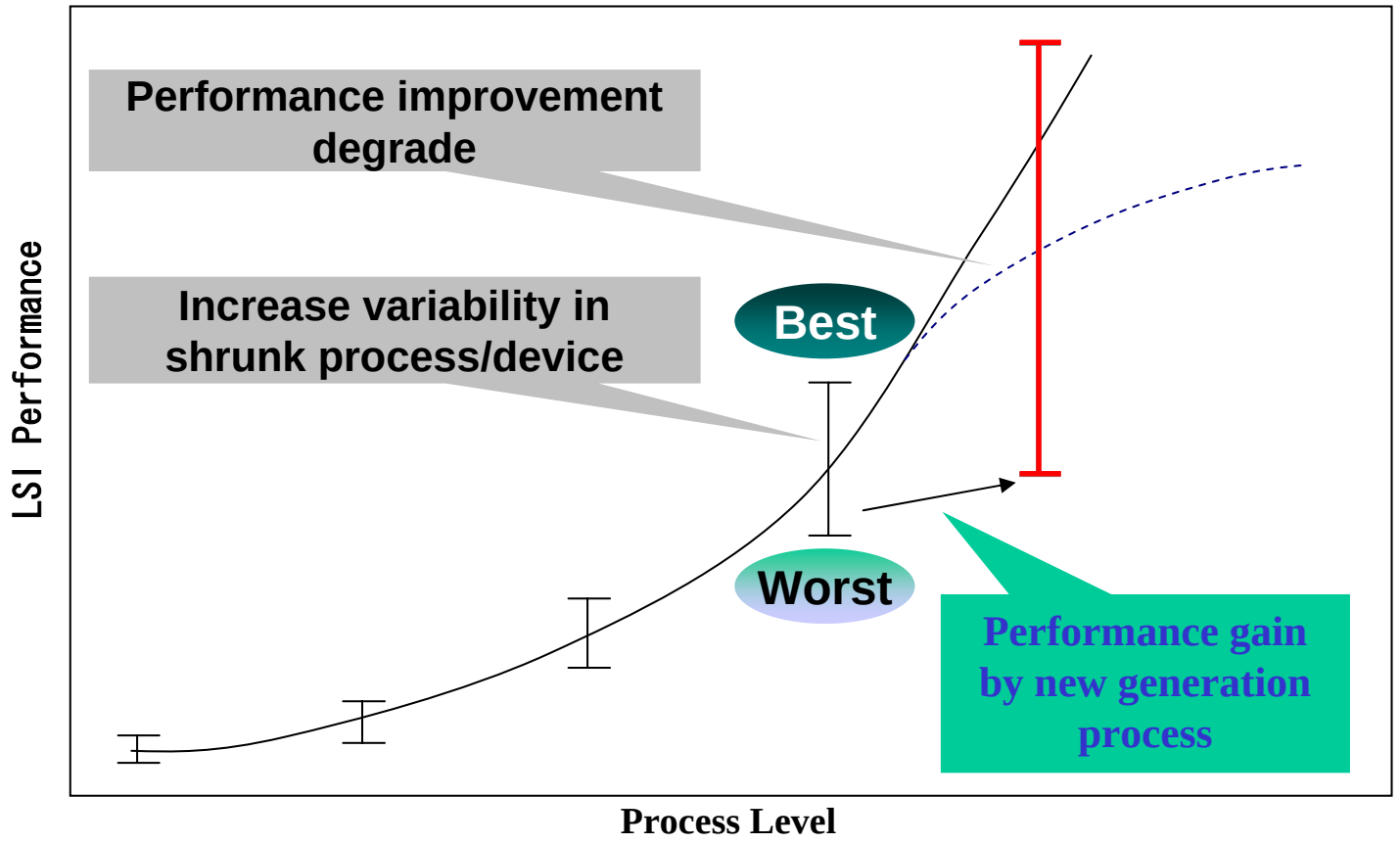
- Within-chip variation of device performance increase
- Process tuning & Device structure improvement

Manufacturing

- Expensive equipments ($1B/Machine)
- Foundry by multiple industries (IBM+Toshiba+Samsung …)

Performance trends:

Performance improvement is leveled-off,
Within-chip variation of device performance increase.



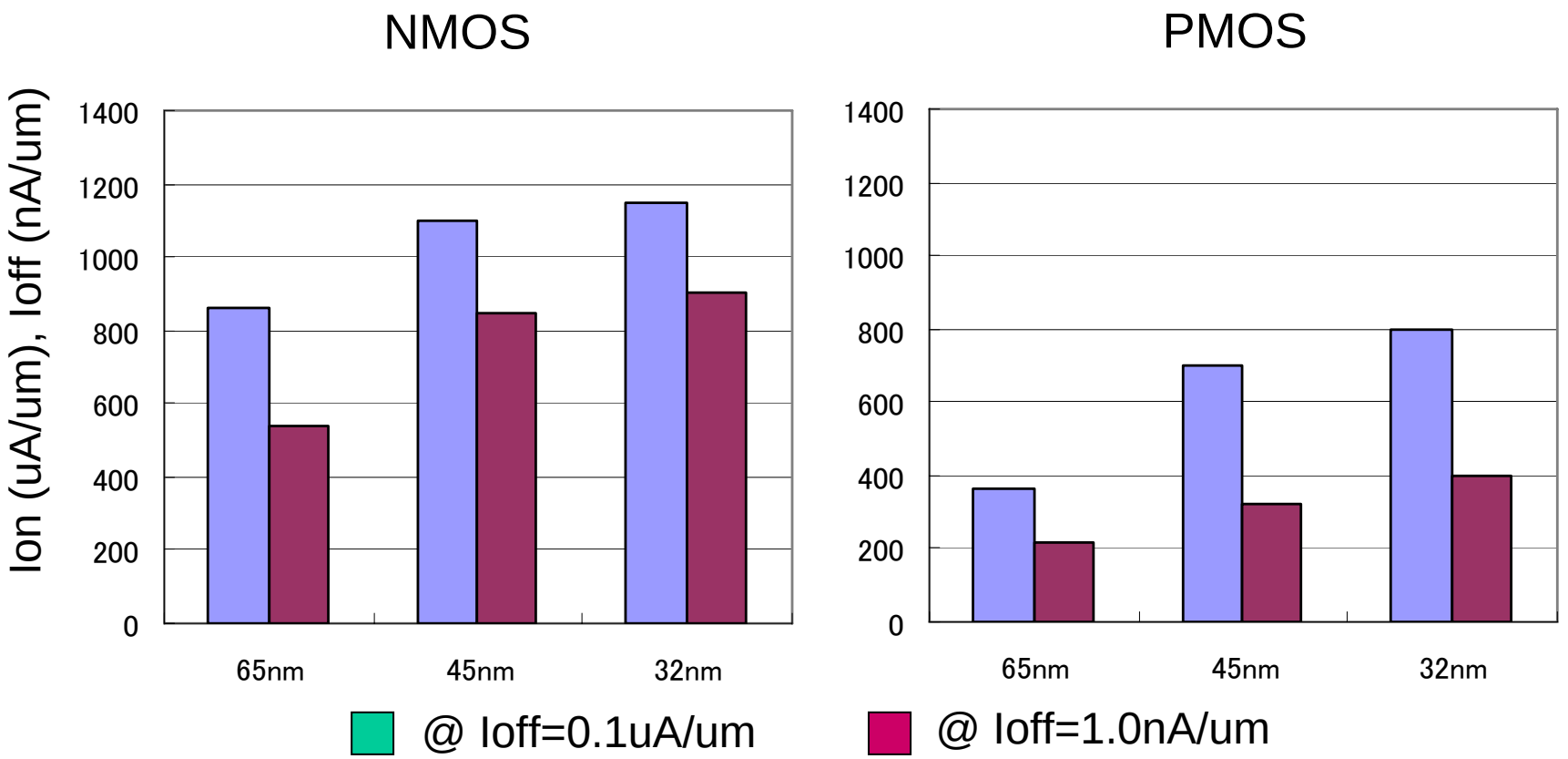
On current (Ion) leveled-off (IEDM data):

Characters;

-Ion; On current improvement is leveled-off in every new generations

-Ioff Off current is increased,

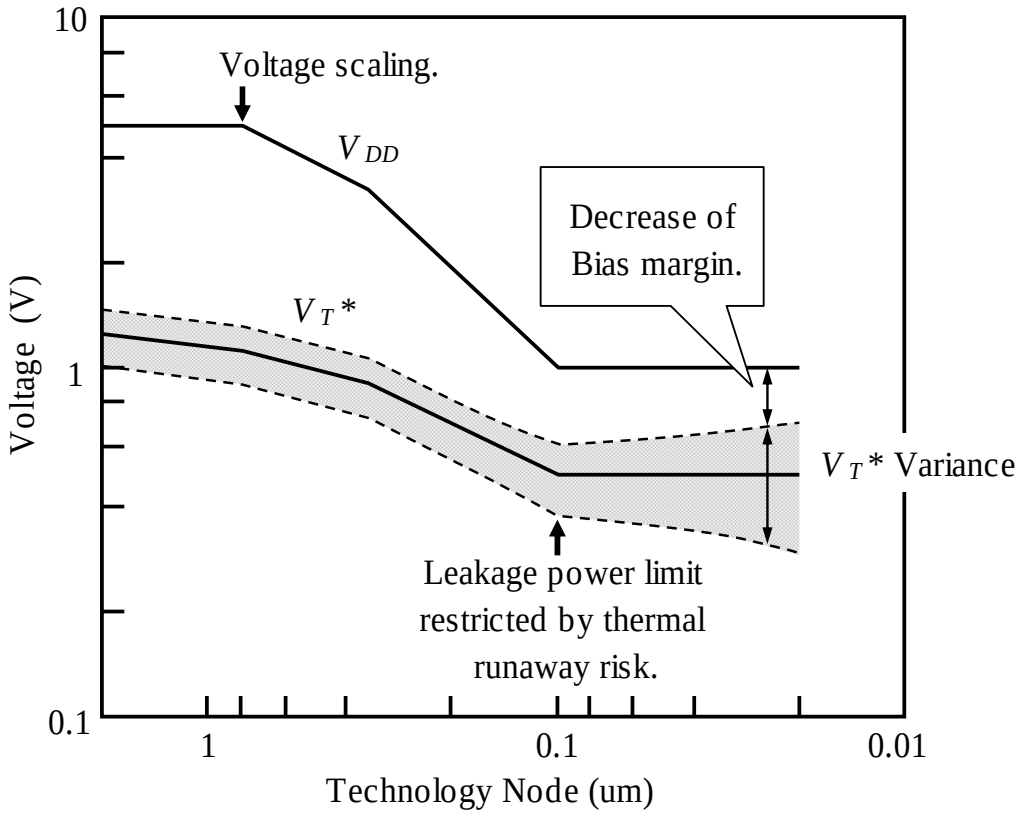
-NMOS vs PMOS Ion ratio is decreased.

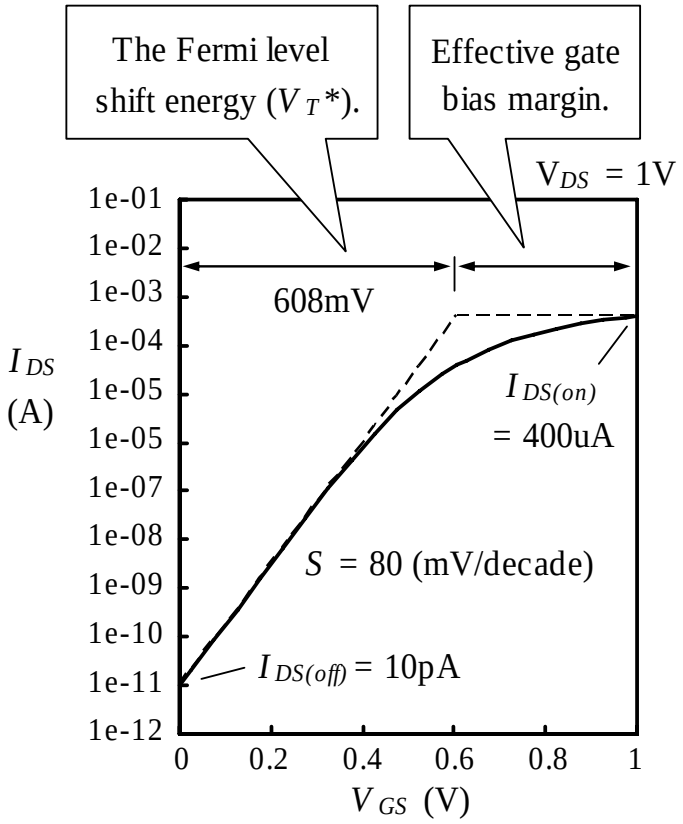


Physical limitation for high speed: #1

Voltage-loss in sub-threshold slope and increased variation limit;

Effective gate bias margin vs. sub-threshold leak current trade-off





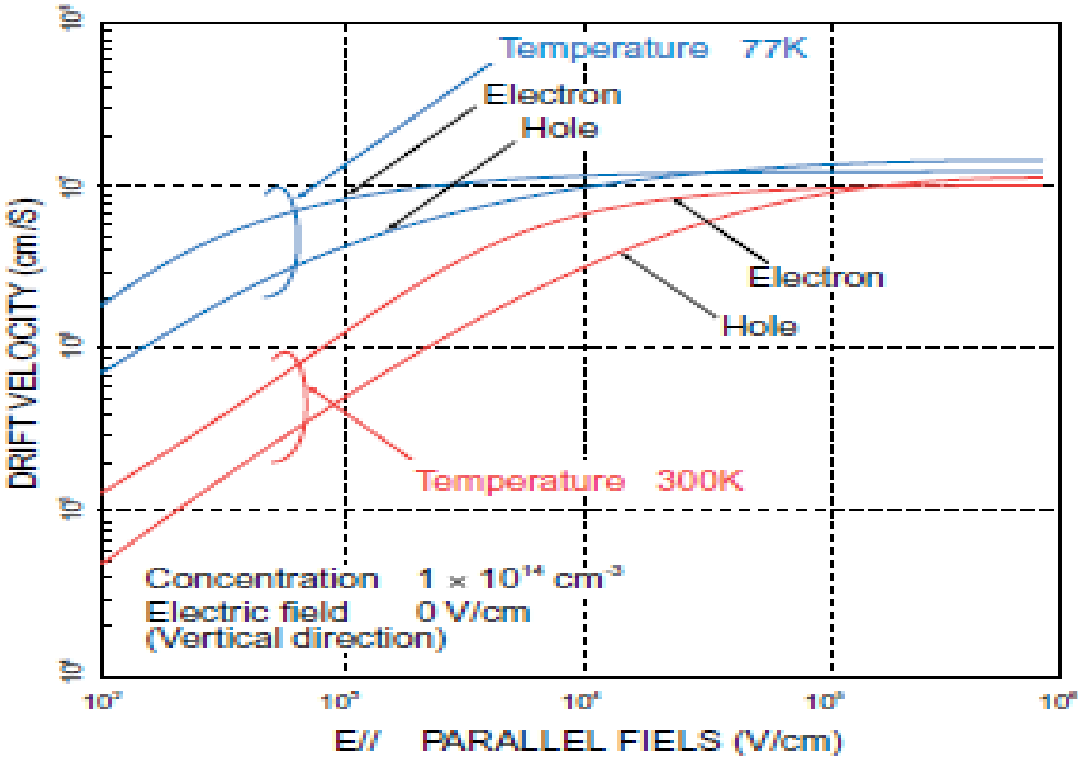
S. Ohkawa; IEEE TSM, 2004

Physical limitation for high speed: #2

Carrier velocity saturation;

Physical limitation of on-current is carrier velocity saturation:

Shrunk gate length → No improvement in current, still good for high integrity purpose (many circuit in unit area)



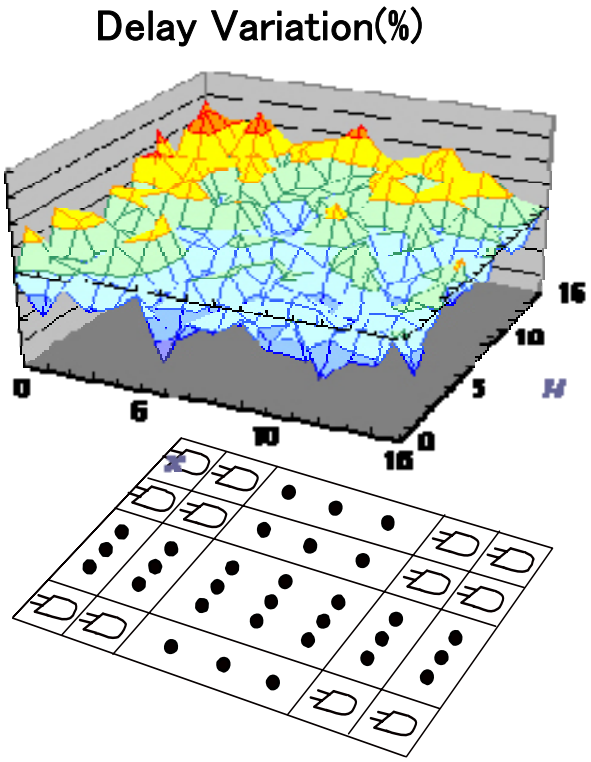
Saturation velocity:
- NMOS ≒ PMOS
- Temp. insensitive

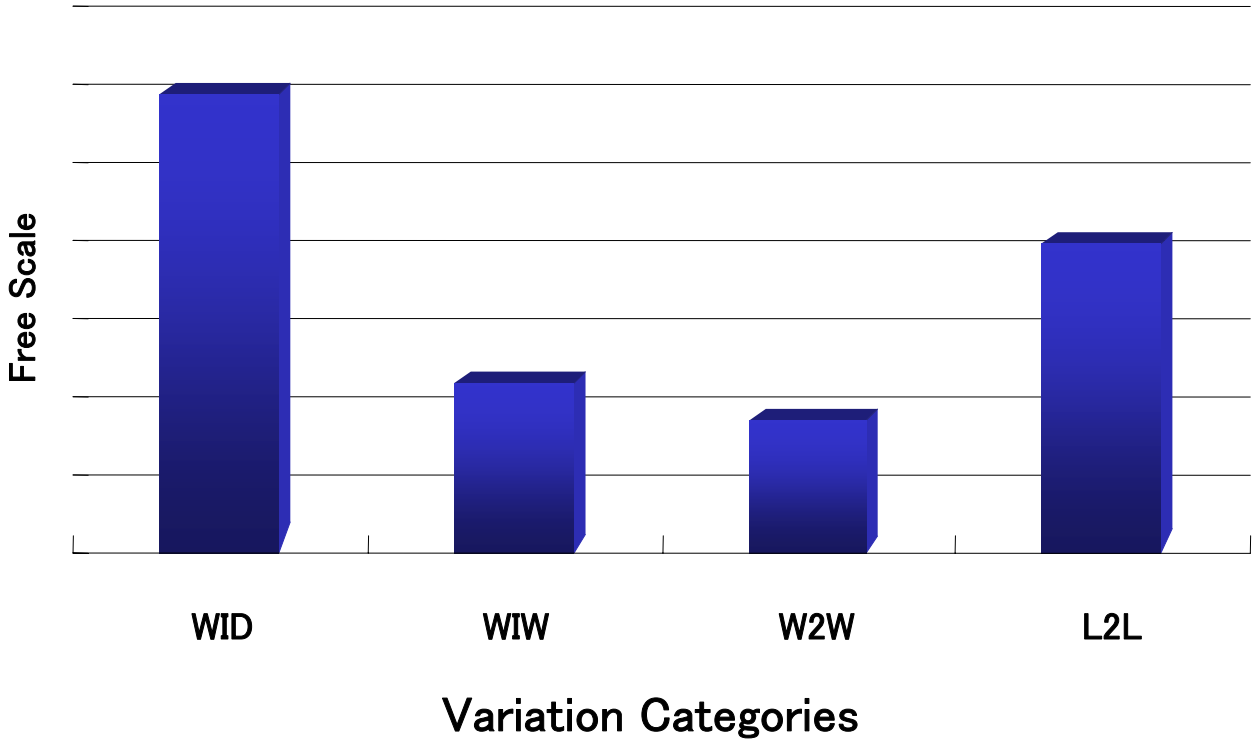
To improve performance:
- Double-gate, Fin-FET
- Nano-wire transistor
- New invention!

Physical limitation for high speed: #3

Variability; Within die, transistors operate differently when the size is small and low-voltage.

SRAM is very critical since it uses minimum feature transistor to shrink area.





Performance design in 45nm processes: Summary of notes

Transistor performance cannot be improved any more!

Therefore, processor performance is leveled-off.

Industries make effort to continue improving performance by multi-core system.

Variability will be increased a lot especially within a die!

Process improvement and new device structure may mitigate it.

On-chip circuits of power/variation/temperature sensors and the signal feedback system becomes popular. It helps further performance improvement.

So, 45nm process era, “More Than Moor” will works well.

(8) Futures of MOS devices

To continue scale-down trend, various researches have been conducted in all over the world.

Material science:

- Gate oxide material (High-K)
- Interlayer dielectric (Low-K)

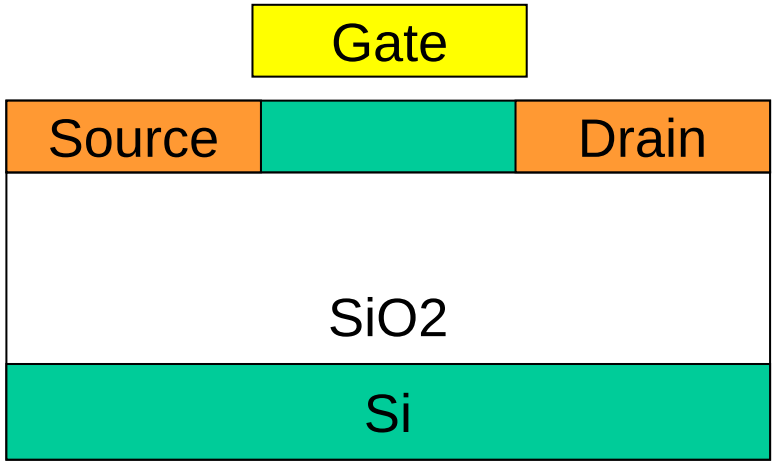
Device science:

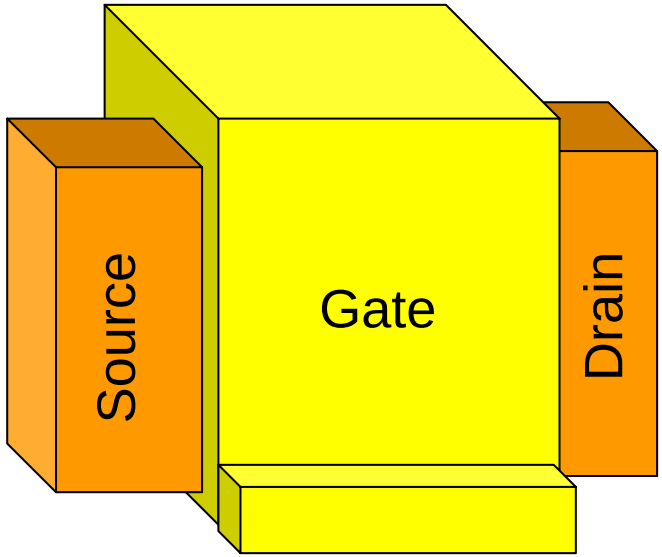
- SOI-MOS
- Strained MOS
- Fin-FET

In this lecture, we have learned “Semiconductor Devices”, however interconnect issue is also very important. This is because the speed-performance is known to be limited interconnect delay (R and C) rather than MOSFET drivability, in sub-100nm processes.

Example of Future MOSFET

Many challenges and new ideas, for continuous improvement of MOS devices and LSI performances.





SOI-MOS

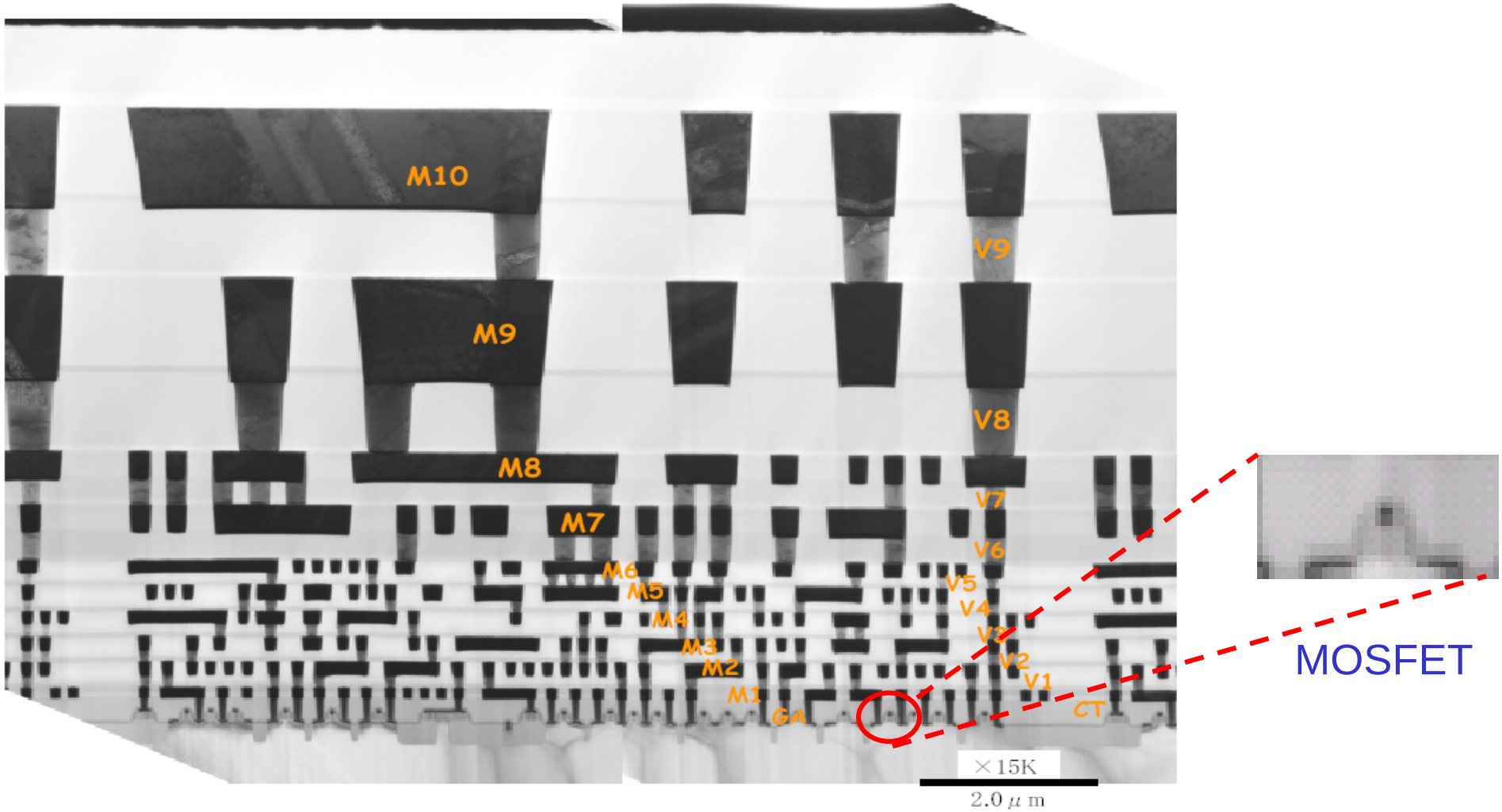
- **Thin Si-film as active area**
- **Buried SiO2 to reduce Capacitance**

Fin-FET

- **Thin Si-film vertically**
- **Surrounded gate increases W**
- **Reduces short-channel effect**

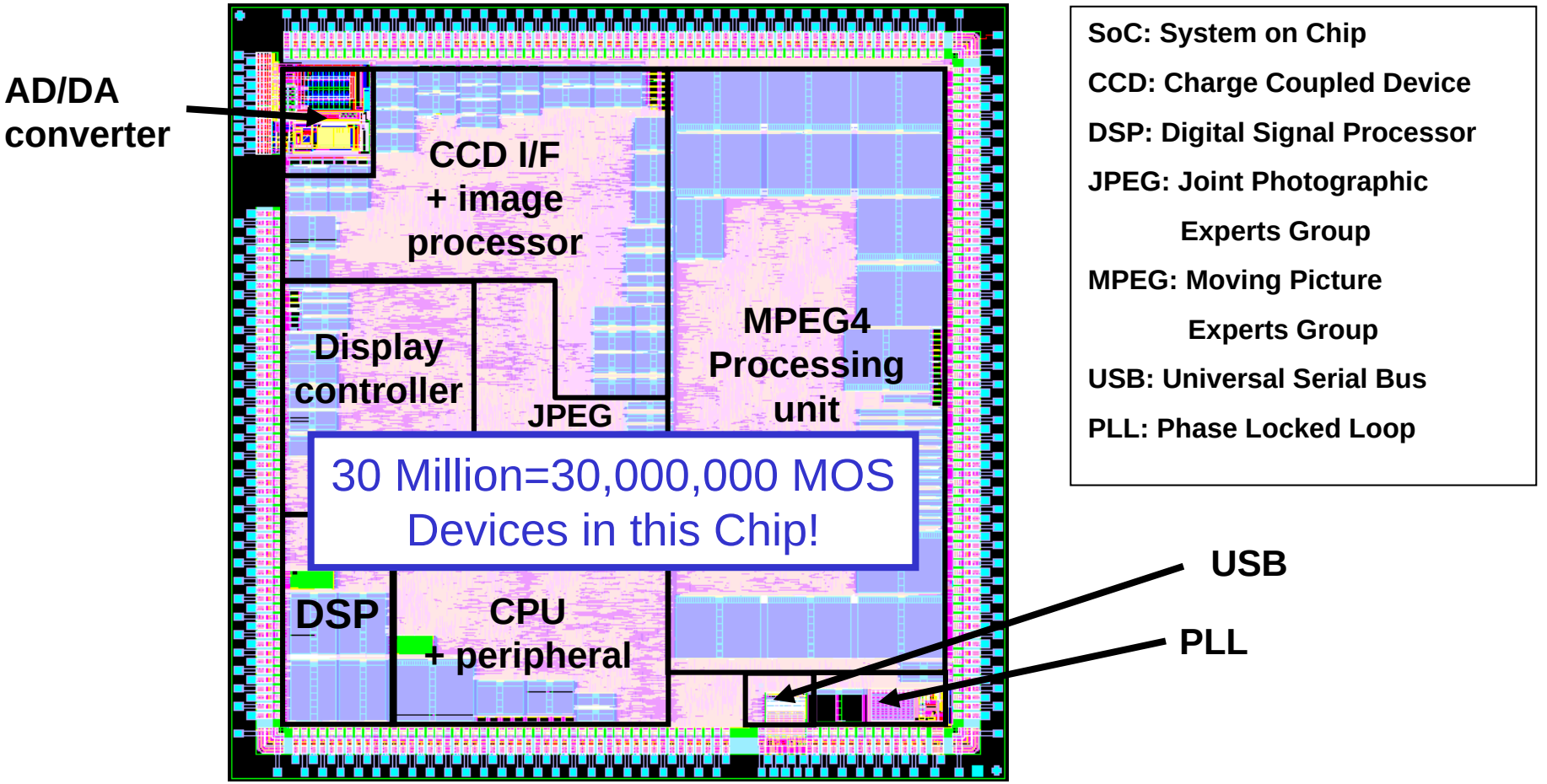
Sub-100nm Interconnect Structure

Scaled interconnect also requires technology challenges such as: Low resistive metal (Al→Cu), Reliability in Electro Migration etc.



MOS Device supports LSI products: Example in Renesas

< Layout plot of SoC chip for Digital Still Camera (DSC)>



SoC: System on Chip
CCD: Charge Coupled Device
DSP: Digital Signal Processor
JPEG: Joint Photographic Experts Group
MPEG: Moving Picture Experts Group
USB: Universal Serial Bus
PLL: Phase Locked Loop

Wide variety of functional units are integrated on a single chip to configure an SoC

Lecture Summary on MOS Devices: Basics

We have learned MOS Devices in this seminar, in a quick manner.

If you want to know deep in MOS devices, another couple of seminars will be necessary, with hard self-learning of Textbooks.

Following area will be helpful for your future learning:

- Compact MOSFET Modeling for circuit simulation
- MOS device variability and its design methodology
- Reliability of MOS Devices
- Analog MOS devices and circuits

.....

Hoping you to fight and learn deeper on MOS devices, to get success in your engineering carrier!

Quiz

(1) What is the general approach to shrink MOS structure?

(2) Why it has been successful, so far?

(3) List up the problems on MOSFET scaling down.

(4) How the process engineer overcome the each problem?

(5) If carrier (electron, hole) moves in velocity saturation in short channel MOS, further shrink in L does not increase Ids. What is the physical reason?

(6) Even in the condition of (5), people prefer to shrink L. Why it comes?