2013/07/04

M40-PF
Error Control Module Module
“uhiapecm0020”
Target Specification

Rev. 3.0

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LLWEB-00026493		
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Document History

Date	Version	Name	Part	Details
2012/04/22	1.0	K.Sako	All	・ Initial description
2012/06/06	2.0	K.Sako	3.2	・ Update block-diagram
			3.3.1	・ Correct address ・ Correct bitwidth of ECMDTMCMP/ECMEOCCFG
			3.3.2	・ Add hs and pshap2 sub block
			4.1	・ Correct ecmterroz and ecmterroutz initial value to “L” ・ scan_mode mask information updated
			4.2.2	・ Add note (for sync monitor bit)
			4.2.20 4.2.21 4.2.22	・ Add note when writing to ECMESSTC0/1/2
			4.2.27	・ Add note when writing to ECMDTMCTL (for handshake description)
			4.2.29	・ Add note when writing to ECMDTMCMP ・ Expand bitwidth for handshake status
			4.2.36	・ Add note when writing to ECMEOCCFG ・ Expand bitwidth for handshake status
			4.3.5	・ Add information for dtmsta bit
			4.3.6	・ Add implementation and notes for error clear mask logic
			5.1	・ Add false path information
2012/07/04	3.0	K.Sako	3.2	・ Correct typo (duplicated delay timer trigger generation (one is error clear timer trigger generation) in SGO)
			3.3.1	・ Correct to W for ECMMPCMD0/ECMCPCMD0
			4.2.2	・ Remove comment (not implemented on uhiapecm0020)
			4.2.24	・ Add missing section.
			4.2.27	・ ECMPE227 is changed to reserved bit.
			4.2.5	・ Correct typo of bit assign
			4.3.5	・ Add description for register update
			4.3.6	・ Modify description
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				・

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1. Introduction

1.1. Purpose

This document is the target specification of Error control module(uhiapecm0020).

Target persons to read this document is :

- RTL Designer
- 1chip/PF-SS designer
- Verification engineer of this module
- Designer responsible on synthesis and STA by using this module

1.2. Scope

Target specification of uhiapecm0020 is described in this document.
This module include several sub-modules designed for common use. (Please see section 1.5)

1.3. Abbreviations, Acronyms, Terminologies

No	Abbreviations	Definition
1	ECC	Error Check and Correct
2	ECM	Error Control Module
3	??b (? is 0 or 1)	binary number
4	??h (? is 0 or 1)	hexadecimal number

1.4. Requirement specification

No	Document Number	Title
[1]	LLWEB-00012779 [ver4]	ECM Requirement specification for P1x

1.5. References

No	Document Number	Title	Description
[2]	-	PFC1A_ECM_目標仕様書	
[3]	-	PFC1A_ECM_機能仕様書	

2. Requirement items

2.1. LLWEB-00012779 [ver1] : ECM Requirement specification for P1x

No	Requirement Specification of LLWEB-00012779		Applicability (A or N/A)	Chapter Described	Note
	Details	Chapter			
1	Safety processing can be chosen depending on the error factor. ・Error flag setting ・ Non-maskable / Maskable interrupt request ・Internal reset ・Error output	1 6.3 6.6.1	A	4.2	Will be implemented
2	With regard to latest error factor for RH850/P1x, please refer to 6.6.1. Acceptable user defined error source have to be expanded from 48 to 93 (maximum).	1 6.6.1	A	3.3.1 4.1	Will be implemented (parameterize is planned, but, T.B.D.) bit 92 is internal usage.
3	It is possible to start a delay timer automatically simultaneously with interrupt request occurrence. *) [Refer to 6.2 and 6.6.3] Synchronous clock shall be changed.	1 6.2 6.6.3	A	4.3.5	Will be implemented based on upf12hecm0010_wp
4	It is possible to select either toggle output or level fixed output.	1	A	4.3.1	Dynamic mode and Fixed value mode is implemented same as base macro.
5	High robustness is achieved by duplication of a module.	1	A	3.2	Duplicated core module like upf12hecm0010_wp will be done
6	Register is protected from the rewriting which is not intended by special sequence.	1	A	3.3.1	Will be implemented as the extension of base macro.
7	Pseudo-error occurrence	1	A	4.3.2	Will be implemented (bit expansion)
8	Diagnosis of error output by using loop-back function.	1	A	4.1	ecmterrlbz is prepared
9	Wait timer for making safe-state of ERROROUT by SW. (New function)	1 6.2 6.3.2 6.6.2	A	4.3.6	Will be implemented (Call clear mask timer)
10	Subdividing of reset-signals for ECM. Three kinds of reset signals are required. 1)For error status registers only. 2)For ERROR pin logic only. 3)For others	6.2 6.6.4	A	3.5	Will be implemented
11	ECM glue logic	1 6.6.5	A	3.2	Will be implemented.
12	Deleting write back function for error status register	1 6.6.6	A	4.2.3 4.2.4 4.2.5	Will be implemented

2.2. Confirmation / Q&A with PJ1)

No	Issued specification		Applicability (A or N/A)	Chapter Described	Conclusion
	Details	Chapter			
13	Error input is expansion to 93	1	A	-	See No.2
14	Masking error out clear for max 10ms	1	A	3.3.1	Will be implemented (See No.9)
15	Delay timer has been already implemented for PFC1A/B	1	A	3.3.1	See No.3
16	Redundant ECM is the same feature as PFC1A/B	1	A	3.2	See No.5
17	Control register newly added is the target of special sequence	1	A	3.3.1	See No.6
18	The scope of PRESET is changed 2) and 3) in No.10 is the target of PRESET in previous macro.	1	A	3.3.1 4.1	See No.10 Reset for ERROROUT will be separated.
19	Remove the write-back feature at read triplication status register	1	A	4.2.3 4.2.4 4.2.5	See No. 12 This is the feedback of Px4 defect. X is propagated at unintended timing.
20	Sgatpe (pseudo erro rpin) numbering	6.3.18 6.3.19 6.3.20	A	3.2	Currently register number+bit assign. There is no requirement from PJ1. (PJ2 issues)
21	erroutz should be via AND of master and checker side.This is the change point from PFC1B	6.6.5	A	4.3.2 (Fig. 4-3)	Will be implemented Detailed logic is not described in this document.
22	Error status synchronous to clk other than clock related error	None	A	4.2.3 4.2.4 4.2.5	Conclusion is that error status register set is remain asynchronous logic. PJ1 cannot get agreement from the customer. So, implement same as base macro.
23	reset value of ECMIRCFG0 is only bit 0 is 1. Others are 0	6.3.11	A	3.3.1	Will be implemented.
24	Error clear mask logic does not restart if same error is occured because error status register is not plus.	6.6.2	A	4.3.6	Implement as requirement specification.
25	Delay timer should be from 3 to 5 (0-1 for maskable, 3-5 for non maskable)	6.3.21 – 6.3.25	A	3.3.1	Will be implemented
26	Triple error status register is needed?	6.6.6	A	3.3.1	Triple status register requirement is dropped. Will be removed.
27	clock divider will be implemented on 1-chip	6.6.2	N/A	-	
28	Reset for errout clear mask timer	6.6.2	A	3.3.1	erroroutresz should be used (by PJ1).
29	scan_mode mask for error intpu/output	6.6.5	A	4.1	ecmterroroutz : needed ercmterroz : needed ecmti : not needed ecmnmi : not needed ecmtresz : needed exor logic terroz -> feedbak : needed (described in terrin spec)
30	scan_mode mask does not consider the polarity of input signal	6.6.5	A	4.1	Will be implemented
31	Bit 31 does not need scan_mode mask	6.6.5	A	4.1	Will be implemented
32	bit 92 of pseudo error mask	6.6.5	A	4.1	Mask for master/checker is prepared by this module. Mask setting will be implemented outside ECM module.

3. Overview

Error control module (ECM) has the features to generate error signal to outside MCU, interrupt, and reset request by the error input signals from various error sources and monitor logics.
This macro designed based on the upf12hecm0010_wp which is used for PFC1B.

[Note] Product dependent logic in upf12hecm0010_wp is not implemented in this module.

- **Smart-BIST (Comparator of redundant ecc module)**
- **Product dependent signal name (Does not assign the error input signal name with error source meaning. Just numbering pin)**
- **The polarity of error input is not considered. Error input pin is considered as high active.**
- **Tis module does not generated OR-ed error input signal from multiple error source. This should be outside this module.**

3.1. Functions

Tab. 3-1 indicates the abstract of functions prepared by ECM.
For the detail of individual functions please see section 4.3.

Tab. 3-1 Functions

Items	Description
Safety processing (Error handling and report)	Execute following safety processing from the error signal input from each module. ・Set error flag ・Generate maskable interrupt Selectable mask/non-mask of generating maskable interrupt for each error input ・Generate non-maskable interrupt Selectable mask/non-mask of generating non-maskable interrupt for each error input ・Generate internal reset request Selectable generate/non-generate reset request for each error input ・Generate error output signal (See section 4.3.1) Selectable mask/non-mask of generate error output signal for each error input. Selectable dynamic mode (using timer input)/non-dynamic mode (fixed level output)
Error Status	This module prepares the error status register. Error status register only cleared by pclk synchronized terminal reset (rststg1z_pclkin(*1)(*2)) or software. Internal reset, which is distributed as PRESETn, does not clear the error status and the status value is kept. So, reset factor can be checked by reading the status register value after reset.
Debug / Self-diagnostics	・Pseudo error generation for debug and self-diagnostic purpose (See section 4.3.2) The action of ECM for pseudo error is same as the one for actual error report. The setting for error output pin signal, interrupt, and internal reset request generation is also valid for pseud error injection. ・Can monitor errorout pin status for checking the path to error output pin of MCU. (See section 4.3.3) By connecting the error out signal by loop-back via I/O buffer, the status of error output pin is monitored by ECM register and CPU can check the status of error output pin by reading this register.
Timeout feature	ECM starts the delay timer at the same time of interrupt generation and generate internal reset request when CPU cannot stop the delay timer in the interrupt handling routine and the delay timer counter value reaches the delayer timer compare register value. This timer is implemented inside this module.
Error out clear mask timer	This is the additional feature. ECM has the feature that masks the error output pin clear action by CPU for the configured period defined by the register inside ECM.
Register protection	To protect the control register from unintended write action, the special access sequence is required to write control registers.
Robustness	Error control module is duplicated and the error out (ERROUTZ) of master and checker is reported via AND of two errorout signal.

(*1) For the purpose of error status register, resstg1z and pclkin_resstg1z should not include the internal reset factor.

(*2) For the status register reset, pclkin_resstg1z is synchronized to PCLK rising edge because this register has asynchronous set signal for error set. So, this module has both asynchronous reset and synchronous reset inside this module and has synchronous reset input to data input pin of FF for status register.

3.2. Combined modules

Tab. 3-2 indicates the modules included in uhiapecm0020. **These modules are not included in uhiapecm0020.**

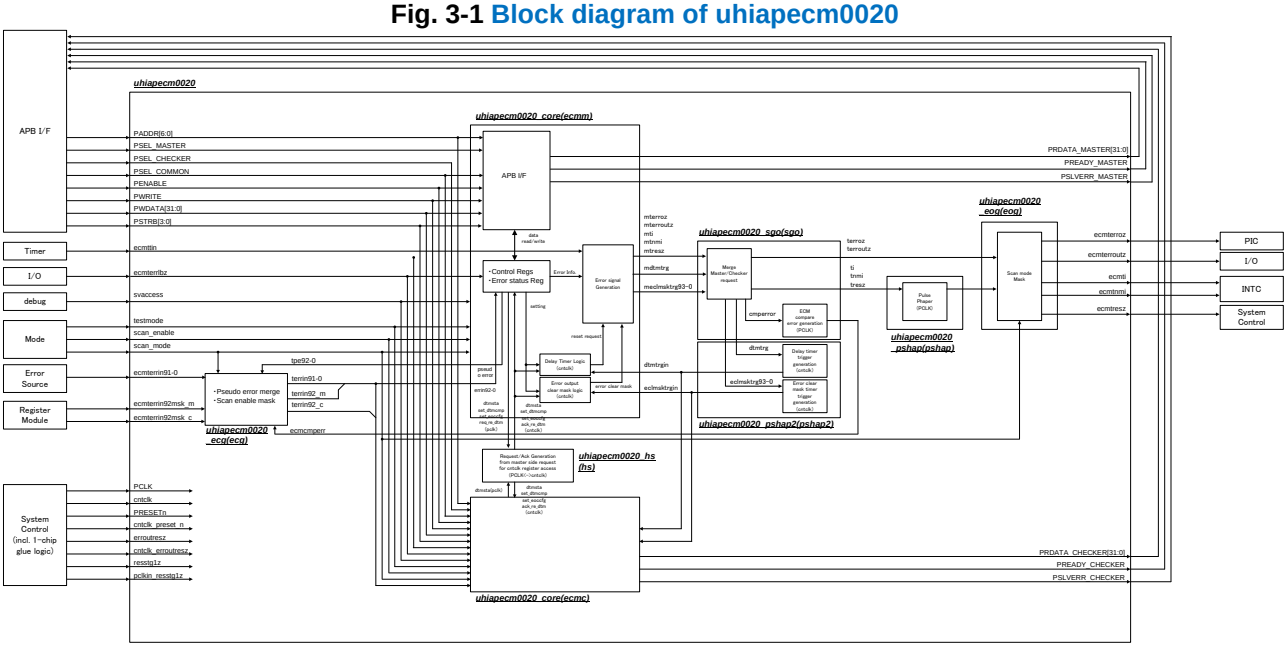
Tab. 3-2 Combined module

module	Description
QL85EPSHAPS2V2	Pulse shaper (send side) for asynchronous signal (*1)
QL85ESYNC1V1	Synchronizer macro
QL85EPSHAPR1V1	Pulse shaper (receive side)

(*1) This module has the spyglass rule violation of "RC_ClkVector". The clock input of FF in this module is normal control signal, NOT clock signal, and is used as asynchronous hand shaking purpose. So, shield wiring possibility for clock signal does not need to be considered. So the above error is handled as pseudo error.

3.2. Block Diagram

Fig. 3-1 Block diagram of uhiapecm0020



3.3. Architecture

3.3.1. Register map

ECM module is divided into 3 PSEL regions.

- PSEL_ECMCOMMON : Access to ECM master/checker common registers. (*1)
- PSEL_ECMMASTER : Access to ECM master side registers.
- PSEL_ECMCHECKER : Access to ECM checker side registers.

(*1) Registers themselves are instanced both master side and checker side because uhiapecm0020 just implements the duplicated ECC core module. PRDATA of master side and checker side is common to common registers and master/checker registers. So, if CPU attempts to read PSEL_ECMCOMMON registers, PRDATA both from master side and checker side has a valid data. This is not changed from base design.

Tab. 3-3 Registers of ECM master

Register simbol	Register name	R/W	Reset	Reset value	Write sequence protection	Address
ECMMESET	ECM master error set trigger	W	-(PRESETn)	00H	Required	<ECMM_base>
ECMMECLR	ECM master error clear trigger	W	-(PRESETn)	00H	Required	<ECMM_base>+04h
ECMMESSTR0	ECM master error source status register0	R	pclkin_resstg1z	00000000H	-	<ECMM_base>+08h
ECMMESSTR1	ECM master error source status register1	R	pclkin_resstg1z	00000000H	-	<ECMM_base>+0Ch
ECMMESSTR2	ECM master error source status register2	R	pclkin_resstg1z(*1)	00000000H	-	<ECMM_base>+10h
ECMMPCMD0	ECM master protection command register0	W	PRESETn	Undefined	-	<ECMM_base>+14h

(*1) Bit 30 is cleared by resstg1z.

Tab. 3-4 Registers of ECM checker

Register simbol	Register name	R/W	Reset	Reset value	Write sequence protection	Address
ECMCESET	ECM checker error set trigger	W	-(PRESETn)	00H	Required	<ECMC_base>
ECMCECLR	ECM checker error clear trigger	W	-(PRESETn)	00H	Required	<ECMC_base>+04h
ECMCESSTR0	ECM checker error source status register0	R	pclkin_resstg1z	00000000H	-	<ECMC_base>+08h
ECMCESSTR1	ECM checker error source status register1	R	pclkin_resstg1z	00000000H	-	<ECMC_base>+0Ch
ECMCESSTR2	ECM checker error source status register2	R	pclkin_resstg1z(*1)	00000000H	-	<ECMC_base>+10h
ECMCPCMD0	ECM checker protection command register0	W	PRESETn	Undefined	-	<ECMC_base>+14h

(*2) Bit 30 is cleared by resstg1z

Tab. 3-5 Registers of ECM master/checker common

Register simbol	Register name	R/W	Reset	Reset value	Write sequence protection	Address
ECMEPCFG	ECM error pulse configuration register	R/W	PRESETn	00h	Required	<ECM_base>
ECMMICFG0	ECM maskable interrupt configuration register 0	R/W	PRESETn	00000000h	Required	<ECM_base>+04h
ECMMICFG1	ECM maskable interrupt configuration register 1	R/W	PRESETn	00000000h	Required	<ECM_base>+08h
ECMMICFG2	ECM maskable interrupt configuration register 2	R/W	PRESETn	00000000h	Required	<ECM_base>+0Ch
ECMNMICFG0	ECM non-maskable interrupt configuration register 0	R/W	PRESETn	00000000h	Required	<ECM_base>+10h
ECMNMICFG1	ECM non-maskable interrupt configuration register 1	R/W	PRESETn	00000000h	Required	<ECM_base>+14h
ECMNMICFG2	ECM non-maskable interrupt configuration register 2	R/W	PRESETn	00000000h	Required	<ECM_base>+18h
ECMIRCFG0	ECM internal reset configuration register 0	R/W	PRESETn	00000001h	Required	<ECM_base>+1Ch
ECMIRCFG1	ECM internal reset configuration register 1	R/W	PRESETn	00000000h	Required	<ECM_base>+20h
ECMIRCFG2	ECM internal reset configuration register 2	R/W	PRESETn	00000000h	Required	<ECM_base>+24h
ECMEMK0	ECM error mask register 0	R/W	PRESETn	00000000h	Required	<ECM_base>+28h
ECMEMK1	ECM error mask register 1	R/W	PRESETn	00000000h	Required	<ECM_base>+2Ch
ECMEMK2	ECM error mask register 2	R/W	PRESETn	00000000h	Required	<ECM_base>+30h
ECMESSTC0	ECM error source status clear trigger register 0	W	-(PRESETn)	00000000h	Required	<ECM_base>+34h
ECMESSTC1	ECM error source status clear trigger register 1	W	-(PRESETn)	00000000h	Required	<ECM_base>+38h
ECMESSTC2	ECM error source status clear trigger register 2	W	-(PRESETn)	00000000h	Required	<ECM_base>+3Ch
ECMPCMD1	ECM protection command register 1	W	-(PRESETn)	Undefined	-	<ECM_base>+40h
ECMPS	ECM protection status register	R	PRESETn	00000000h	-	<ECM_base>+44h
ECMPE0	ECM pseudo error trigger register 0	W	-(PRESETn)	00000000h	Required	<ECM_base>+48h
ECMPE1	ECM pseudo error trigger register 1	W	-(PRESETn)	00000000h	Required	<ECM_base>+4Ch
ECMPE2	ECM pseudo error trigger register 2	W	-(PRESETn)	00000000h	Required	<ECM_base>+50h
ECMDTMCTL	ECM delay timer control register	R/W	PRESETn	00000000h	Required	<ECM_base>+54h
ECMDTMR	ECM delay timer register	R	PRESETn	00000000h	-	<ECM_base>+58h
ECMDTMCMP	ECM delay timer compare register	R/W	PRESETn	00000000h	Required	<ECM_base>+5Ch
ECMDTMCFG0	ECM delay timer configuration register 0	R/W	PRESETn	00000000h	Required	<ECM_base>+60h
ECMDTMCFG1	ECM delay timer configuration register 1	R/W	PRESETn	00000000h	Required	<ECM_base>+64h
ECMDTMCFG2	ECM delay timer configuration register 2	R/W	PRESETn	00000000h	Required	<ECM_base>+68h
ECMDTMCFG3	ECM delay timer configuration register 3	R/W	PRESETn	00000000h	Required	<ECM_base>+6Ch
ECMDTMCFG4	ECM delay timer configuration register 4	R/W	PRESETn	00000000h	Required	<ECM_base>+70h
ECMDTMCFG5	ECM delay timer configuration register 5	R/W	PRESETn	00000000h	Required	<ECM_base>+74h
ECMEOCCFG	ECM error output clear invalidation configuration register	R/W	erroutresz	00000000h	Required	<ECM_base>+78h

3.3.2. Hierarchy

Tab. 3-6 shows the module hierarcy.

Tab. 3-6 Module hierarchy

Module name (*1)	Instance name	Module name (base) (upf12hecm0010_wp)	Function
uhiapecm0020	(top)		TOP module
core	ecmm	upf12hecm0010	ECM core
core	ecmc	upf12hecm0010	ECM core
ecg	ecg	upf12hecg0000	Error input generation from error input pin, pseudo error generation, and scan_mode.
sgo	sgo	upf12hsgo0010	Generate OR-ed signal from ecmm/ecmc
hs	hs	New	Handshke for master/checker synchronized data transfer(*4)
pshap (*3)	pshap	upf12hecm0010_pshap	Pulse generation for reset request and interrupt. (PCLK domain)
pshap2 (*3)	pshap2	upf12hecm0010_pshap	Pulse generation for reset request and interrupt. (cntclk domain)
eog	eog	upf12heog0000	Reset request gating logic by scan_mode

(*1) The name of sub-module has prefix uhiapecm0020_. (e.g. core means that uhiapecm0020_core).
(*2) Base module is upf12hecg0000. But, This module deos not generate OR-ed signal from multiple error source.
(*3) This module has the spyglass rule violation of "RC_ClkVector". The clock input of FF in this module is normal control signal, NOT clock signal, and is used as asynchronous hand shaking purpose. So, shield wiring possibility for clock signal does not need to be considered. So the above error is handled as pseudo error. Please also see section 3.2.
(*4), For common register, same timing data transfer between PCLK<->cntclk is achived by using master side request signal. Target is folloings:

- **DTMSTA bit (use OR of master/checker side DTMSTA in pclk domain)**
- **DTMCMP register data set to cntclk domain (use master side data set signal)**
- **ECMEOUTCLRT register data set to cntclk domain (use master side data set signal)**
- **DTMR read (capture timing of cntclk and PCLK domain) (use master side read request)**

3.4. Clock Tree

This module is work with PCLK and cntclk. cntclk is used for delay timer and clear mask timer logics, which include timer start trigger signal generation. PCLK and cntclk is asynchronous.

Tab. 3-7 Clock

Name	Width	In/ Out	Active level	Reset level	clock	Function
cntclk	1	In	-	-	-	Clock for delay timer and error out clear mask timer (incl. trigger generation) (diveided from 8MHz ROSC(1/2 of ROSC))
PCLK	1	In	-	-	-	Clocks for other FFs (Max. 100Mhz)

3.5. Reset Tree

Tab. 3-8 Reset

Name	Width	In/ Out	Active level	Reset level	clock	Function
resstg1z	1	In	L	-	PCLK(*1)(*2)	asynchronous external reset (Used only for reset bit 30 of ECMmESSTR2n)
pclkin_resstg1z	1	In	L	-	PCLK(*3)	pclk synchronous resstg1g. (Used only for ECMmESSTR other than ECMmESSTR1n bit 30.)
erroutresz	1	In	L	-	PCLK(*2)	Reset for error out clear related logic incl. ECMEOCCFG register.
cntclk_erroutresz	1	In	L	-	cntclk(*2)	Reset for error out clear related logic incl. ECMEOCCFG register. (cntclk domain)
PRESETn	1	In	L	-	PCLK(*2)	APB reset
cntclk_preset_n	1	In	L	-	cntclk(*2)	APB reset (cntclk domain)

(*1) For the purpose of this status bit asynchronous external reset is used as asynchronous reset for ECMmESSTR2n. Other error status register is reset by synchronous reset.
(*2) Reset release should be synchronous to clock because the these resets are used as FF asynchronous reset.
(*3) Reset should be synchronous to pclk because this is used as synchronous reset.

Considered reset pattern is as followings

Tab. 3-9 Reset pattern

Patterm	resstg1z pclkin_resstg1z	errout_resz cntclk_erroutresz	PRESETn cntclk_preset_n	
1	o	o	o	System power up
2	-	o	o	Internal reset 1 (all logics clear)
4	-	-	o	Internal reset 2 (clear except error out clear mask logics)

Reset policy is as following.

Tab. 3-10 Reset policy

reset target	Reset signal		
	resstg1z pclkin_resstg1z	erroutresz cntclk_erroutresz	PRESETn cntclk_preset_n
ECMmESSTR0: ECMm Error Source Status register 0	x	-	-
ECMmESSTR1: ECMm Error Source Status register 1	x	-	-
ECMmESSTR2: ECMm Error Source Status register 2	x	-	-
Error Pin Logic (include relevant logic)	-	x	-
ECM Output Clear Invalidation Configuration Register	-	x	-
ECM Output Clear Invalidation counter	-	x	-
All other circuit except for above.	-	-	x

x: reset, -: do not reset

4. Specification

4.1. Signals

Tab. 4-1 Signals for uhiapecm0020

Terminal name	In/Out	Active Level	Reset Level	Clock	Reset (*1)	bit width	Function
clock/reset							
PCLK	In	-	-	-	-	1	Bus clock
cntclk	In	-	-	-	-	1	Delay timer/Error clear mask timer clock
PRESETn	In	L	-	PCLK (*2)	-	1	APB reset
cntclk_preset_n	In	L	-	cntclk(*2)	-	1	APB reset (cntclk domain)
erroutresz	In	L	-	PCLK(*2)	-	1	errout logic reset incl. error clear mask timer
cntclk_erroutresz	In	L	-	cntclk(*2)	-	1	errout logic reset incl. error clear mask timer
resstg1z	In	L	-	PCLK(*2)	-	1	External reset
pclkin_resstg1z	In	L	-	PCLK	-	1	PCLK synchronized external reset
APB I/F							
PADDR[6:0]	In	-	-	PCLK	-	7	APB address bus
PSEL_MASTER	In	H	L	PCLK	-	1	APB PSEL signal (Master side)
PSEL_CHECKER	In	H	L	PCLK	-	1	APB PSEL signal (Checker side)
PSEL_COMMON	In	H	L	PCLK	-	1	APB PSEL signal (Both side)
PENABLE	In	H	-	PCLK	-	1	APB strobe signal
PWRITE	In	H	-	PCLK	-	1	APB write/read signal
PWDATA[31:0]	In	-	-	PCLK	-	32	APB write data bus
PRDATA_MASTER[31:0]	Out	-	All"0"	PCLK	PRESETn	32	APB read data bus (Master side)
PRDATA_CHECKER[31:0]	Out	-	All"0"	PCLK	PRESETn	32	APB read data bus (Checker side)
PSTRB[3:0]	In	-	-	PCLK	-	4	Write strobe
PREADY_MASTER	OUT	-	-	PCLK	PRESETn	1	
PREADY_CHECKER	OUT	-	-	PCLK	PRESETn	1	
PSLVERR_MASTER	OUT	H	L	Fixed	PRESETn	1	APB Slave error (0 fixed for this module)
PSLVERR_CHECKER	OUT	H	L	Fixed	PRESETn	1	APB Slave error (0 fixed for this module)
Error input signal/Signal for dynamic mode							
ecmterrin91-0	In	H	L	Async(*3)	-	92	Error input(*6)
ecmterrin92msk_m	In	H	L	Async(*3)	-	1	ecmterrin92 mask signal (master side)
ecmterrin92msk_c	In	H	L	Async(*3)	-	1	ecmterrin92 mask signal (checker side)
ecmterrlbz	In	H	L	Async(*3)	-	1	Loopback from ERROROUT (Error status register bit 96)
ecmttin	In	-	L	PCLK	-	1	Timer input for dynamic mode
Error output signal							
ecmterroz	Out	L	L	Async	erroutresz(*4)	1	Error output compare signal (To PIC)
ecmterroutz	Out	L	L	Async	erroutresz(*4)	1	ERROROUT output
ecmti	Out	H	L	PCLK	PRESETn	1	Maskable interrupt output
ecmtnmi	Out	H	L	PCLK	PRESETn	1	Non-maskable interrupt output
ecmtresz	Out	L	H	Async	PRESETn(*5)	1	ECM internal reset request
Error input signal							
testmode	In	H	L	-	-	1	Test mode
svaccess	In	H	L	PCLK	-	1	Break
scan_mode	In	H	L	-	-	1	Scan mode
scan_enable	In	H	L	-	-	1	Scan enable信号

(*1) Output pin (or related logic) reset. Reset includes both PCLK domain and cntclk domain. (e.g. if indicated PRESETn, it means PRESETn and cntclk_preset_n)
(*2) Reset release is expected as PCLK synchronized even if asynchronous reset.
(*3) This signal captured by this signal asynchronously (e.g. input to set pin of FF). So, these error input pins should be glitchless.
(*4) ecmterroz and ecmterroutz become reset status by erroutresz. When only PRESETn is asserted, the status depends on ERSTR register and other configuration status.
(*5) This signal is asynchronous signal. Once this reset request is asserted, this value is kept until PRESETn is asserted.
(*6) Bit 92 is reserved for internal use (ECM compare error)

Scan mode mask policy for error input output related is as following.

Terminal name	in scan_mode	Note
Error input signal/Signal for dynamic mode		
ECMmESSTR bit 30	masked	Only clock is stopped.
ECMmESSTR bit 29	masked	Delay timer overflow
ecmterrin92(internal use)	masked	ECM compare error logic
ecmterrin91	non-masked	assigned unintended activated BIST
ecmterrin90-0	masked	
ecmterrin92msk_m	(masked)	Masked as the input of ecmterrin92 to core module
ecmterrin92msk_c	(masked)	Masked as the input of ecmterrin92 to core module
ecmterrlbz	non-masked	not an error input
ecmttin	non-masked	not an error input
Error output signal		
ecmterroz	masked low	unsafe state
ecmterroutz	masked low	unsafe state
ecmti	non-masked	-
ecmnmi	non-masked	-
ecmtresz	masked high	reset request not activated

4.2. Registers

Address maps are described in section 3.3.1
In following sections, ECMm means ECMM for master side and ECMC for checker side.
About write sequence protection target, please see section 3.3.1.

4.2.1. ECMm error set trigger register (ECMmESET)

ECMm error set trigger register is to activate the ecmterroutz and ecmterroz (set to low).
If writing this register to 1, low level signal is asserted from ecmterroutz and ecmterroz.
This output signal cannot be masked.
Read value of this register is always “0”.

bit	7	6	5	4	3	2	1	0
	-	-	-	-	-			ECMmEST
Reset value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W

bit	name	Reset	R/W	Definition
7-1	-	all “0”	R	Reserved
0	ECMmEST	0	W	Error set trigger bit 0 : ignored 1 : activate (low level) ecmterroutz and ecmterroz

[Note]
By setting/clearing error output signal using ECMmESET/ECMmECR register, ECMmESSTR2 bit 28(ecmterrin92) which will be assigned as ECM compare will be asserted.
So, if user would like to execute self-diagnostics without interrupt/error output, user should set the bit 28 of ECMMICFG2/ECMNMICFG2/ECMIRCFG2 register properly.

4.2.2. ECMm error clear trigger register (ECMmECLR)

ECMm error clear trigger register is to inactivate the ecmterroutz and ecmterroz (set to high).
If writing this register to 1, ecmterroutz and ecmterroz become high level so far as no error, which activates ecmterroutz and ecmterroz, remains.
Read value of this register is always “0”.

bit	7	6	5	4	3	2	1	0
	-	-	-	-	-			ECMmECT
Reset value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W

bit	name	Reset	R/W	Definition
7-1	-	all “0”	R	Reserved
0	ECMmECT	0	W	Error clear trigger bit 0 : ignored 1 : inactivate (high level) ecmterroutz and ecmterroz

[Note]
・Clearing ecmterroutz can be executed only the case that all errors have been already cleared except erros masked by ECMEMK0/1/2.
・About notification, please also see section 4.2.1.

~~**[Note] To detect the situation described in 4.3.6 by S/W, sync (used for set/release ecmterroutz/ecmterroz) monitor bit will be implemented on bit 4 as read only register. This will be described in the next version of this document.**~~

4.2.3. ECMm error source status register 0(ECMmESSTR0)

This is read only register. This register indicates individual error status. Value of this register is independent from error mask setting by ECMEMK0.
Alls bit of this register are reset by “pclkin_resstg1z”, which is synchronous reset. So, internal reset, such as PRESETn and erroutresz, does not affect the value of this register.
This register can be cleared by writing ECMESSTC0.
[Note] This register value is set completely asynchronous using async set pin of FF. So, read value may be check by S/W handling (read twice etc.)
[Note] This register should be outside the scope of Field BIST.
[Note] This register does not have write back at read access different from base macro.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECMmSSE031	ECMmSSE030	ECMmSSE029	ECMmSSE028	ECMmSSE027	ECMmSSE026	ECMmSSE025	ECMmSSE024	ECMmSSE023	ECMmSSE022	ECMmSSE021	ECMmSSE020	ECMmSSE019	ECMmSSE018	ECMmSSE017	ECMmSSE016
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMmSSE015	ECMmSSE014	ECMmSSE013	ECMmSSE012	ECMmSSE011	ECMmSSE010	ECMmSSE009	ECMmSSE008	ECMmSSE007	ECMmSSE006	ECMmSSE005	ECMmSSE004	ECMmSSE003	ECMmSSE002	ECMmSSE001	ECMmSSE000
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	name	Reset	R/W	Definition
31-1	ECMmSSE031-001	all “0"	R	Error factor status bit ECMmSSE031-ECMmSSE001 is for error factor 31-1 (ecmterrin31-1) 0:No error 1:Error
0	ECMmSSE000	0	R	Error factor status bit ECMmSSE000(ecmterrin0) is considered that WDT error is asserted. (So, the reset value of ECMIRCFG0 bit 0 is 1.) 0:No error 1:Error

4.2.4. ECMm error source status register 1(ECMmESSTR1)

This is read only register. This register indicates individual error status. Value of this register is independent from error mask setting by ECMEMK1.
Alls bit of this register are reset by “pclkin_resstg1z”, which is synchronous reset. So, internal reset, such as PRESETn and erroutresz, does not affect the value of this register.
This register can be cleared by writing ECMESSTC1.
[Note] This register value is set completely asynchronous using async set pin of FF. So, read value may be check by S/W handling (read twice etc.)
[Note] This register should be outside the scope of Field BIST.
[Note] This register does not have write back at read access different from base macro.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECMmSSE131	ECMmSSE130	ECMmSSE129	ECMmSSE128	ECMmSSE127	ECMmSSE126	ECMmSSE125	ECMmSSE124	ECMmSSE123	ECMmSSE122	ECMmSSE121	ECMmSSE120	ECMmSSE119	ECMmSSE118	ECMmSSE117	ECMmSSE116
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMmSSE115	ECMmSSE114	ECMmSSE113	ECMmSSE112	ECMmSSE111	ECMmSSE110	ECMmSSE109	ECMmSSE108	ECMmSSE107	ECMmSSE106	ECMmSSE105	ECMmSSE104	ECMmSSE103	ECMmSSE102	ECMmSSE101	ECMmSSE100
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	name	Reset	R/W	Definition
31-0	ECMmSSE131-100	all “0"	R	Error factor status bit ECMmSSE131-ECMmSSE100 is for error factor 63-32 (ecmterrin63-32) 0:No error 1:Error

4.2.5. ECMm error source status register 2(ECMmESSTR2)

This is read only register. This register indicates individual error status. Value of this register is independent from error mask setting by ECMEMK2.
From bit 31-28 is assigned as special usage.
Bit 31 is just read the status of ecmterrlbz which is usually connected to the loopback path of ERROUTZ pin. this bit has no reset.
Bit 30 is assigned “writing status of ECMmSET”, this bit is reset **by resstg1z, not by pclkin_resstg1z**.
Bit 29 is used for “Delay timer overflow”. this is reset by pckin_resstg1z
Bit 28 is used for ECM compare error. This is reset by pclkin_resstg1z.
Bit 27 is used for unintended activated BIST. This is reset by pclkin_resstg1z. This bit does not have scan_mode mask. So, after the BIST incl. start-up Filed-BIST, this bit is set to “1”. User should determine whether this is truly unintended or not in consideration of current operation mode.
Internal reset, such as PRESETn and erroutresz, does not affect the value of this register.
This register can be cleared by writing ECMESSTC2 except ECMmSSE231(ecmterrlbz value).
[Note] This register value is set completely asynchronous using async set pin of FF. So, read value may be check by S/W handling (read twice etc.)
[Note] This register should be outside the scope of Field BIST.
[Note] This register does not have write back at read access different from base macro.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECMmSSE231	ECMmSSE230	ECMmSSE229	ECMmSSE228	ECMmSSE227	ECMmSSE226	ECMmSSE225	ECMmSSE224	ECMmSSE223	ECMmSSE222	ECMmSSE221	ECMmSSE220	ECMmSSE219	ECMmSSE218	ECMmSSE217	ECMmSSE216
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMmSSE215	ECMmSSE214	ECMmSSE213	ECMmSSE212	ECMmSSE211	ECMmSSE210	ECMmSSE109	ECMmSSE108	ECMmSSE107	ECMmSSE106	ECMmSSE105	ECMmSSE104	ECMmSSE103	ECMmSSE102	ECMmSSE101	ECMmSSE100
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	name	Reset	R/W	Definition
31	ECMmSSE231	0	R	This is read path of loop-back for ERROUTZ pin (ecmterrlbz) 0:ERROUTZ is low 1:ERROUTZ is high This bit does not have reset, but ERROUTZ is usually low after external reset. After internal reset, the value depends on the status of ERROUTZ.
30	ECMmSSE230	0	R	Error factor status bit ECMmSSE230 is used for writing status of ECMmESET. 0:No error 1:Erro is set by ECMmESET
29	ECMmSSE229	0	R	Error factor status bit ECMmSSE229 is used for delay timer overflow 0:No overflow 1:Overflow
28	ECMmSSE228	0	R	Error factor status bit ECMmSSE228 is used for ECM compare error. 0:No error 1:Error
27	ECMmSSE227	0	R	Error factor status bit ECMmSSE227 is used for unintended activated BIST error 0:No error 1:Error
26-0	ECMmSSE226-200	all “0”	R	Error factor status bit ECMmSSE226-ECMmSSE100 is for error factor 90-64 (ecmterrin90-64) 0:No error 1:Error

4.2.6. ECMm protection command register 0(ECMmPCMD0)

ECMm protection command register is the write only register and allows 32bit write access.
Write sequence protection register is indicated in section 3.3.1.
Write sequence is described and
This register have undefined reset value.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-															
Reset value	Undefined															
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-								ECMm0REG[7:0]							
Reset value	Undefined								Undefined							
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	name	Reset	R/W	Definition
31-8	-	Undefined	W	Reserved bit
7-0	ECMm0REG7-ECMm0REG0	Undefined	W	Write protected ECMm register command bits. To start write sequence, write 000000A5h to this register.

4.2.7. ECM error pulse configuration register (ECMEPCFG)

ECMEPCFG is read/write register and select dynamic mode and non-dynamic mode of ecmterroutz.

bit	7	6	5	4	3	2	1	0
	-	-	-	-	-			ECMSL0
Reset value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W

bit	name	Reset	R/W	Definition
7-1	-	all “0”	R	Reserved bit
0	ECMSL0	0	R/W	Setting the mode of ecmterroutz 0: non-dynamic mode 1:dynamic mode. In this mode, output the value of ecmttin as the ecmterroutz during no error.。

4.2.8. ECM maskable interrupt configuration register 0(ECMMICFG0)

ECMMICFG0 is read/write register and 8bit access is allowed. This register configure the ecmti.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECMMIE031	ECMMIE030	ECMMIE029	ECMMIE028	ECMMIE027	ECMMIE026	ECMMIE025	ECMMIE024	ECMMIE023	ECMMIE022	ECMMIE021	ECMMIE020	ECMMIE019	ECMMIE018	ECMMIE017	ECMMIE016
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMMIE015	ECMMIE014	ECMMIE013	ECMMIE012	ECMMIE011	ECMMIE010	ECMMIE009	ECMMIE008	ECMMIE007	ECMMIE006	ECMMIE005	ECMMIE004	ECMMIE003	ECMMIE002	ECMMIE001	ECMMIE000
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-0	ECMMIE031-000	all “0"	R/W	ECM maskable interrupt control bit ECMMIE031-ECMMIE000 is for error factor 31-0 (ecmterrin31-0) 0:Maskable interrupt is not allowed 1:Maskable interrupt is allowed.

4.2.9. ECM maskable interrupt configuration register 1(ECMMICFG1)

ECMMICFG1 is read/write register and 8bit access is allowed. This register configure the ecmti.

bit	31	30	29	28	27	26	25	24	23	22	21	21	19	18	17	16
	ECMMIE131	ECMMIE130	ECMMIE129	ECMMIE128	ECMMIE127	ECMMIE126	ECMMIE125	ECMMIE124	ECMMIE123	ECMMIE122	ECMMIE121	ECMMIE120	ECMMIE119	ECMMIE118	ECMMIE117	ECMMIE116
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMMIE115	ECMMIE114	ECMMIE113	ECMMIE112	ECMMIE111	ECMMIE110	ECMMIE109	ECMMIE108	ECMMIE107	ECMMIE106	ECMMIE105	ECMMIE104	ECMMIE103	ECMMIE102	ECMMIE101	ECMMIE100
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-0	ECMMIE131-100	all “0"	R/W	ECM maskable interrupt control bit ECMMIE131-ECMMIE100 is for error factor 63-32 (ecmterrin63-32) 0:Maskable interrupt is not allowed 1:Maskable interrupt is allowed.

4.2.10. ECM maskable interrupt configuration register 2(ECMMICFG2)

ECMMICFG2 is read/write register and 8bit access is allowed. This register configure the ecmti.

bit	31	30	29	28	27	26	25	24	23	22	21	21	19	18	17	16
	-	-	-	ECMMIE228	ECMMIE227	ECMMIE226	ECMMIE225	ECMMIE224	ECMMIE223	ECMMIE222	ECMMIE221	ECMMIE220	ECMMIE219	ECMMIE218	ECMMIE217	ECMMIE216
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMMIE215	ECMMIE214	ECMMIE213	ECMMIE212	ECMMIE211	ECMMIE210	ECMMIE209	ECMMIE208	ECMMIE207	ECMMIE206	ECMMIE205	ECMMIE204	ECMMIE203	ECMMIE202	ECMMIE201	ECMMIE200
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-29	-	all “0”	R	Reserved
28-0	ECMMIE228-200	all “0"	R/W	ECM maskable interrupt control bit ECMMIE228-ECMMIE200 is for error factor 92-64 (ecmterrin92-64) 0:Maskable interrupt is not allowed 1:Maskable interrupt is allowed.

4.2.11. ECM non-maskable interrupt configuration register 0(ECMNMICFG0)

ECMNMICFG0 is read/write register and 8bit access is allowed. This register configure the ecmtnmi.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECMNMIE031	ECMNMIE030	ECMNMIE029	ECMNMIE028	ECMNMIE027	ECMNMIE026	ECMNMIE025	ECMNMIE024	ECMNMIE023	ECMNMIE022	ECMNMIE021	ECMNMIE020	ECMNMIE019	ECMNMIE018	ECMNMIE017	ECMNMIE016
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMNMIE015	ECMNMIE014	ECMNMIE013	ECMNMIE012	ECMNMIE011	ECMNMIE010	ECMNMIE009	ECMNMIE008	ECMNMIE007	ECMNMIE006	ECMNMIE005	ECMNMIE004	ECMNMIE003	ECMNMIE002	ECMNMIE001	ECMNMIE000
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-0	ECMNMIE031-000	all “0"	R/W	ECM non-maskable interrupt control bit ECMNMIE031-ECMNMIE000 is for error factor 31-0 (ecmterrin31-0) 0:Non-maskable interrupt is not allowed 1:Non-maskable interrupt is allowed.

4.2.12. ECM non-maskable interrupt configuration register 1(ECMNMICFG1)

ECMNMICFG1 is read/write register and 8bit access is allowed. This register configure the ecmtnmi.

bit	31	30	29	28	27	26	25	24	23	22	21	21	19	18	17	16
	ECM NMIE 131	ECM NMIE 130	ECM NMIE 129	ECM NMIE 128	ECM NMIE 127	ECM NMIE 126	ECM NMIE 125	ECM NMIE 124	ECM NMIE 123	ECM NMIE 122	ECM NMIE 121	ECM NMIE 120	ECM NMIE 119	ECM NMIE 118	ECM NMIE 117	ECM NMIE 116
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECM NMIE 115	ECM NMIE 114	ECM NMIE 113	ECM NMIE 112	ECM NMIE 111	ECM NMIE 110	ECM NMIE 109	ECM NMIE 108	ECM NMIE 107	ECM NMIE 106	ECM NMIE 105	ECM NMIE 104	ECM NMIE 103	ECM NMIE 102	ECM NMIE 101	ECM NMIE 100
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-0	ECMNMIE131-100	all “0"	R/W	ECM non-maskable interrupt control bit ECMNMIE131-ECMNMIE100 is for error factor 63-32 (ecmterrin63-32) 0:Non-maskable interrupt is not allowed 1:Non-maskable interrupt is allowed.

4.2.13. ECM non-maskable interrupt configuration register 2(ECMNMICFG2)

ECMNMICFG2 is read/write register and 8bit access is allowed. This register configure the ecmtnmi.

bit	31	30	29	28	27	26	25	24	23	22	21	21	19	18	17	16
	-	-	-	ECM NMIE 228	ECM NMIE 227	ECM NMIE 226	ECM NMIE 225	ECM NMIE 224	ECM NMIE 223	ECM NMIE 222	ECM NMIE 221	ECM NMIE 220	ECM NMIE 219	ECM NMIE 218	ECM NMIE 217	ECM NMIE 216
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECM NMIE 215	ECM NMIE 214	ECM NMIE 213	ECM NMIE 212	ECM NMIE 211	ECM NMIE 210	ECM NMIE 209	ECM NMIE 208	ECM NMIE 207	ECM NMIE 206	ECM NMIE 205	ECM NMIE 204	ECM NMIE 203	ECM NMIE 202	ECM NMIE 201	ECM NMIE 200
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-29	-	all “0”	R	Reserved
28-0	ECMNMIE228-200	all “0"	R/W	ECM non-maskable interrupt control bit ECMNMIE228-ECMNMIE200 is for error factor 92-64 (ecmterrin92-64) 0:Non-maskable interrupt is not allowed 1:Non-maskable interrupt is allowed.

4.2.14. ECM internal reset configuration register 0(ECMIRCFG0)

ECMIRCFG0 is read/write register and 8bit access is allowed. This register configure the ecmtresz.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECMIRE031	ECMIRE030	ECMIRE029	ECMIRE028	ECMIRE027	ECMIRE026	ECMIRE025	ECMIRE024	ECMIRE023	ECMIRE022	ECMIRE021	ECMIRE020	ECMIRE019	ECMIRE018	ECMIRE017	ECMIRE016
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMIRE015	ECMIRE014	ECMIRE013	ECMIRE012	ECMIRE011	ECMIRE010	ECMIRE009	ECMIRE008	ECMIRE007	ECMIRE006	ECMIRE005	ECMIRE004	ECMIRE003	ECMIRE002	ECMIRE001	ECMIRE000
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-1	ECMIRE031-001	all “0"	R/W	ECM internal reset control bit ECMIRE031-ECMIRE000 is for error factor 31-1 (ecmterrin31-1) 0:Internal reset is not allowed 1:Internal reset is allowed.
0	ECMIRE000	1	R/W	ECM internal reset control bit ECMIRE000 is for error factor 0 (ecmterrin0) and used for WDT overflow. 0:Internal reset is not allowed 1:Internal reset is allowed.

4.2.15. ECM internal reset configuration register 1(ECMIRCFG1)

ECMIRCFG1 is read/write register and 8bit access is allowed. This register configure the ecmtresz.

bit	31	30	29	28	27	26	25	24	23	22	21	21	19	18	17	16
	ECMIRE131	ECMIRE130	ECMIRE129	ECMIRE128	ECMIRE127	ECMIRE126	ECMIRE125	ECMIRE124	ECMIRE123	ECMIRE122	ECMIRE121	ECMIRE120	ECMIRE119	ECMIRE118	ECMIRE117	ECMIRE116
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMIRE115	ECMIRE114	ECMIRE113	ECMIRE112	ECMIRE111	ECMIRE110	ECMIRE109	ECMIRE108	ECMIRE107	ECMIRE106	ECMIRE105	ECMIRE104	ECMIRE103	ECMIRE102	ECMIRE101	ECMIRE100
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-0	ECMIRE131-100	all “0"	R/W	ECM internal reset control bit ECMIRE131-ECMIRE100 is for error factor 63-32 (ecmterrin63-32) 0:Internal reset is not allowed 1:Internal reset is allowed.

4.2.16. ECM internal reset configuration register 2(ECMIRCFG2)

ECMIRCFG2 is read/write register and 8bit access is allowed. This register configure the ecmtresz.

bit	31	30	29	28	27	26	25	24	23	22	21	21	19	18	17	16
	-	-	ECMIRE229	ECMIRE228	ECMIRE227	ECMIRE226	ECMIRE225	ECMIRE224	ECMIRE223	ECMIRE222	ECMIRE221	ECMIRE220	ECMIRE219	ECMIRE218	ECMIRE217	ECMIRE216
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMIRE215	ECMIRE214	ECMIRE213	ECMIRE212	ECMIRE211	ECMIRE210	ECMIRE209	ECMIRE208	ECMIRE207	ECMIRE206	ECMIRE205	ECMIRE204	ECMIRE203	ECMIRE202	ECMIRE201	ECMIRE200
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-30	-	all “0”	R	Reserved
29-0	ECMIRE229-200	all “0"	R/W	ECM internal reset control bit ECMIRE228-ECMIRE200 is for error factor 92-64 (ecmterrin92-64) ECMIRE229 is for delay timer overflow 0:Internal reset is not allowed 1:Internal reset is allowed.

4.2.17. ECM error mask register 0(ECMEMK0)

ECMEMK0 is read/write register and 8bit access is allowed. This register configure the ecmterroz/ecmterroutz.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECMEMK031	ECMEMK030	ECMEMK029	ECMEMK028	ECMEMK027	ECMEMK026	ECMEMK025	ECMEMK024	ECMEMK023	ECMEMK022	ECMEMK021	ECMEMK020	ECMEMK019	ECMEMK018	ECMEMK017	ECMEMK016
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMEMK015	ECMEMK014	ECMEMK013	ECMEMK012	ECMEMK011	ECMEMK010	ECMEMK009	ECMEMK008	ECMEMK007	ECMEMK006	ECMEMK005	ECMEMK004	ECMEMK003	ECMEMK002	ECMEMK001	ECMEMK000
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-0	ECMEMK031-000	all “0"	R/W	ECM error output signal mask control bit ECMEMK031-ECMEMK000 is for error factor 31-0 (ecmterrin31-0) 0:Error output signal is not masked 1:Error output signal is masked.

4.2.18. ECM error mask register 1(ECMEMK1)

ECMEMK1 is read/write register and 8bit access is allowed. This register configure the ecmterroz/ecmterroutz.

bit	31	30	29	28	27	26	25	24	23	22	21	21	19	18	17	16
	ECMEMK131	ECMEMK130	ECMEMK129	ECMEMK128	ECMEMK127	ECMEMK126	ECMEMK125	ECMEMK124	ECMEMK123	ECMEMK122	ECMEMK121	ECMEMK120	ECMEMK119	ECMEMK118	ECMEMK117	ECMEMK116
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMEMK115	ECMEMK114	ECMEMK113	ECMEMK112	ECMEMK111	ECMEMK110	ECMEMK109	ECMEMK108	ECMEMK107	ECMEMK106	ECMEMK105	ECMEMK104	ECMEMK103	ECMEMK102	ECMEMK101	ECMEMK100
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-0	ECMEMK131-100	all “0"	R/W	ECM error output signal mask control bit ECMEMK131-ECMEMK100 is for error factor 63-32 (ecmterrin63-32) 0:Error output signal is not masked 1:Error output signal is masked.

4.2.19. ECM error mask register 2(ECMEMK2)

ECMEMK2 is read/write register and 8bit access is allowed. This register configure the ecmterroz/ecmterroutz.

bit	31	30	29	28	27	26	25	24	23	22	21	21	19	18	17	16
	-	-	ECMEMK229	ECMEMK228	ECMEMK227	ECMEMK226	ECMEMK225	ECMEMK224	ECMEMK223	ECMEMK222	ECMEMK221	ECMEMK220	ECMEMK219	ECMEMK218	ECMEMK217	ECMEMK216
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMEMK215	ECMEMK214	ECMEMK213	ECMEMK212	ECMEMK211	ECMEMK210	ECMEMK209	ECMEMK208	ECMEMK207	ECMEMK206	ECMEMK205	ECMEMK204	ECMEMK203	ECMEMK202	ECMEMK201	ECMEMK200
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-30	-	all “0”	R	Reserved
29-0	ECMEMK229-200	all “0"	R/W	ECM error output signal mask control bit ECMEMK228-ECMEMK200 is for error factor 92-64 (ecmterrin92-64) ECMEMK229 is for delay timer overflow 0:Error output signal is not masked 1:Error output signal is masked.

4.2.20. ECM error source status clear trigger register 0(ECMESSTC0)

ECMESSTC0 is write only register and only 32bit access is allowed. This register is used for clearing ECMmESSTR0 (both master side and checker side are cleared).

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECM CLSSE 031	ECM CLSSE 030	ECM CLSSE 029	ECM CLSSE 028	ECM CLSSE 027	ECM CLSSE 026	ECM CLSSE 025	ECM CLSSE 024	ECM CLSSE 023	ECM CLSSE 022	ECM CLSSE 021	ECM CLSSE 020	ECM CLSSE 019	ECM CLSSE 018	ECM CLSSE 017	ECM CLSSE 016
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECM CLSSE 015	ECM CLSSE 014	ECM CLSSE 013	ECM CLSSE 012	ECM CLSSE 011	ECM CLSSE 010	ECM CLSSE 009	ECM CLSSE 008	ECM CLSSE 007	ECM CLSSE 006	ECM CLSSE 005	ECM CLSSE 004	ECM CLSSE 003	ECM CLSSE 002	ECM CLSSE 001	ECM CLSSE 000
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	name	Reset	R/W	Definition
31-0	ECMCLSSE031-000	all “0"	W	Error factor reset trigger ECMCLSSE031-ECMCLSSE000 is for error factor 31-0(ECMmSSE031-ECMmSSE000) 0:No action 1:Clear error status.

4.2.21. ECM error source status clear trigger register 1(ECMESSTC1)

ECMESSTC1 is write only register and only 32bit access is allowed. This register is used for clearing ECMmESSTR1 (both master side and checker side are cleared).

bit	31	30	29	28	27	26	25	24	23	22	21	21	19	18	17	16
	ECM CLSSE 131	ECM CLSSE 130	ECM CLSSE 129	ECM CLSSE 128	ECM CLSSE 127	ECM CLSSE 126	ECM CLSSE 125	ECM CLSSE 124	ECM CLSSE 123	ECM CLSSE 122	ECM CLSSE 121	ECM CLSSE 120	ECM CLSSE 119	ECM CLSSE 118	ECM CLSSE 117	ECM CLSSE 116
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECM CLSSE 115	ECM CLSSE 114	ECM CLSSE 113	ECM CLSSE 112	ECM CLSSE 111	ECM CLSSE 110	ECM CLSSE 109	ECM CLSSE 108	ECM CLSSE 107	ECM CLSSE 106	ECM CLSSE 105	ECM CLSSE 104	ECM CLSSE 103	ECM CLSSE 102	ECM CLSSE 101	ECM CLSSE 100
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	name	Reset	R/W	Definition
31-0	ECMCLSSE131-100	all “0"	W	Error factor reset trigger ECMCLSSE131-ECMCLSSE100 is for error factor 63-32(ECMmSSE131-ECMmSSE100) 0:No action 1:Clear error status.

4.2.22. ECM error source status clear trigger register 2(ECMESSTC2)

ECMESSTC2 is write only register and only 32bit access is allowed. This register is used for clearing ECMmESSTR0 (both master side and checker side are cleared).

bit	31	30	29	28	27	26	25	24	23	22	21	21	19	18	17	16
	-	ECM CLSSE 230	ECM CLSSE 229	ECM CLSSE 228	ECM CLSSE 227	ECM CLSSE 226	ECM CLSSE 225	ECM CLSSE 224	ECM CLSSE 223	ECM CLSSE 222	ECM CLSSE 221	ECM CLSSE 220	ECM CLSSE 219	ECM CLSSE 218	ECM CLSSE 217	ECM CLSSE 216
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECM CLSSE 215	ECM CLSSE 214	ECM CLSSE 213	ECM CLSSE 212	ECM CLSSE 211	ECM CLSSE 210	ECM CLSSE 209	ECM CLSSE 208	ECM CLSSE 207	ECM CLSSE 206	ECM CLSSE 205	ECM CLSSE 204	ECM CLSSE 203	ECM CLSSE 202	ECM CLSSE 201	ECM CLSSE 200
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	name	Reset	R/W	Definition
30-0	ECMCLSSE230-200	all “0"	W	Error factor reset trigger ECMCLSSE028-ECMCLSSE000 is for error factor 92-0(ECMmSSE028-ECMmSSE000) ECMCLSSE029 is for delay timer overflow (ECMmSSE029) ECMCLSSE030 is for ECM error status (ECMmSSE030) 0:No action 1:Clear error status.

4.2.23. ECM protection command register 1(ECMPCMD1)

ECM protection command register is the write only register and allows 32bit write access.
Write sequence protection register is indicated in section 3.3.1.
Write sequence is described and
This register have undefined reset value.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-															
Reset value	Undefined															
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-								ECM1REG[7:0]							
Reset value	Undefined								Undefined							
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	name	Reset	R/W	Definition
31-8	-	Undefined	W	Reserved bit
7-0	ECM1REG7-ECM1REG0	Undefined	W	Write protected ECM register command bits. To start write sequence, write 000000A5h to this register.

4.2.24. ECM protection status register (ECMPS)

ECM protection status register is the read only register. This register indicates whether the sequence protected register write access has been completed successfully or not.
Details are described in section 4.3.7.

bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ECMPRERR
Reset value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

bit	name	Reset	R/W	Description
31-1	-	all “0”	R	Reserved
0	ECMPRERR	0	R	ECM protectio status bit Indicates whether the sequence protected register write access has been completed successfully or not. 0:Write sequence is succeeded. 1:Write sequence is failed.

4.2.25. ECM pseudo error trigger register 0(ECMPE0)

ECMPE0 is write only register and only 32bit access is allowed. Writing this register generate a pseudo error for test. The action on this pseudo error is the same as the actual error, such as the error report by ecmterrin.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECMPE031	ECMPE030	ECMPE029	ECMPE028	ECMPE027	ECMPE026	ECMPE025	ECMPE024	ECMPE023	ECMPE022	ECMPE021	ECMPE020	ECMPE019	ECMPE018	ECMPE017	ECMPE016
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMPE015	ECMPE014	ECMPE013	ECMPE012	ECMPE011	ECMPE010	ECMPE009	ECMPE008	ECMPE007	ECMPE006	ECMPE005	ECMPE004	ECMPE003	ECMPE002	ECMPE001	ECMPE000
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	name	Reset	R/W	Definition
31-0	ECMPE031-000	all “0"	W	Generate pseudo error ECMPE031-ECMPE000 is for error factor 31-0(ecmterrin31-0) 0:No action 1:Generate pseudo error signal

4.2.26. ECM pseudo error trigger register 1(ECMPE1)

ECMPE1 is write only register and only 32bit access is allowed. Writing this register generate a pseudo error for test. The action on this pseudo error is the same as the actual error, such as the error report by ecmterrin.

bit	31	30	29	28	27	26	25	24	23	22	21	21	19	18	17	16
	ECMPE131	ECMPE130	ECMPE129	ECMPE128	ECMPE127	ECMPE126	ECMPE125	ECMPE124	ECMPE123	ECMPE122	ECMPE121	ECMPE120	ECMPE119	ECMPE118	ECMPE117	ECMPE116
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMPE115	ECMPE114	ECMPE113	ECMPE112	ECMPE111	ECMPE110	ECMPE109	ECMPE108	ECMPE107	ECMPE106	ECMPE105	ECMPE104	ECMPE103	ECMPE102	ECMPE101	ECMPE100
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	name	Reset	R/W	Definition
31-0	ECMPE131-100	all “0"	W	Generate pseudo error ECMPE131-ECMPE100 is for error factor 63-32(ecmterrin63-32) 0:No action 1:Generate pseudo error signal

4.2.27. ECM pseudo error trigger register 2(ECMPE2)

ECMPE2 is write only register and only 32bit access is allowed. Writing this register generate a pseudo error for test. The action on this pseudo error is the same as the actual error, such as the error report by ecmterrin.

bit	31	30	29	28	27	26	25	24	23	22	21	21	19	18	17	16
	-	-	ECMPE229	ECMPE228	-	ECMPE226	ECMPE225	ECMPE224	ECMPE223	ECMPE222	ECMPE221	ECMPE220	ECMPE219	ECMPE218	ECMPE217	ECMPE216
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	W	W	R	W	W	W	W	W	W	W	W	W	W	W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMPE215	ECMPE214	ECMPE213	ECMPE212	ECMPE211	ECMPE210	ECMPE209	ECMPE208	ECMPE207	ECMPE206	ECMPE205	ECMPE204	ECMPE203	ECMPE202	ECMPE201	ECMPE200
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

bit	name	Reset	R/W	Definition
29	ECMPE229	all “0"	W	Generate pseudo error This is for the delay timer overflow (ECMmSSE229) 0:No action 1:Generate pseudo error signal
28	ECMPE228	all “0"	W	Generate pseudo error ECMPE228 is for error factor 92 0:No action 1:Generate pseudo error signal
27	ECMPE27	all “0"	R	Reserved (This register can be written actually. But no effort)
26-0	ECMPE226-200	all “0"	W	Generate pseudo error ECMPE226-ECMPE200 is for error factor 90-64(ecmterrin90-64) 0:No action 1:Generate pseudo error signal

4.2.28. ECM delay timer control register(ECMDTMCTL)

ECMDTMCTL is read/write register and can be written with 8bit width access. This register control the delay timer.

[Note1] This register setting need to be passed to cntclk domain and require several period to pass the signals to cntclk.

[Note2] To avoid meta stable status, this register can be written only when DTMSTA = DTMSTACNTCLK. Please check again whether DTMSTA is updated after your write action.

[Note3] Other than writing “1” to DTMSTP, writing “0” to DTMSTA is executable same as previous version of this macro.

bit	7	6	5	4	3	2	1	0
	-	-	-	DTMSTACNTCLK	-	-	DTMSTP	DTMSTA
Reset value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	W	R/W

bit	name	Reset	R/W	Definition
7-2	-	all “0”	R	Reserved
4	-	all “0”	R	Delay timer start bit from cntclk domain (this signal itself is pclk synchronized) DTMSTA 0: Does not start timer 1:Start timer
3-2	-	all “0”	R	Reserved
1	DTMSTP	0	~~R~~/W	Delay timer stop bit By writing “1” to this bit, delay timer is stopped (0 write is ignored). ECMSTA bit will be 0 at the same time. During this stop request is passed to cntclk domain and stoppped. This bit is cleared and ECMSTA bit is cleared. 0: Stop request is completed/not executed. 1: Stop request is on execution
0	DTMSTA	0	R/W	Delay timer start bit The action of delay timer at interrupt is configured by this bit. 0:Does not start timer 1:Start timer

4.2.29. ECM delay timer register(ECMDTMR)

ECMDTMR is read only register. By setting ECMSTA of ECMDTMCTL register from “1” to “0”, the delay timer counter is initialized.

[Note] This register is placed in cntclk domain. So, in order to read this register, PREADY is negated during read the value from cntclk domain counter to PCLK domain APB I/F.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ECMTDMR[15:0]															
Reset value	0000h															
R/W	R															

bit	name	Reset	R/W	Definition
15-0	ECMTDMR[15:0]	all “0"	R	Delay timer counter value

4.2.30. ECM delay timer compare register(ECMDTMCMP)

ECMDTMCMP is read/write register. When the delay timer counter value reaches the value of this register, delay timer overflow is generated and ECMmSSE229 bit is set. Update of this register have to be executed while delay timer is stopped. Access by 16-bit units is possible for writing.

[Note1] This register setting need to be passed to cntclk domain. So, CMPW indicates that this setting is onexecution. While CMPW bit is “1”, the write to this register is ignored. Please access this register after checking CMPW=0 and start from protection sequence. (CMPW does not suppress the access/ignore the protection sequence before final writing to this register. But, not guaranteed.)

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CMPW
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ECMDTMCMP[15:0]															
Reset value	0000h															
R/W	R/W															

bit	name	Reset	R/W	Definition
31-17	RFU	all “0"	R	Reserved
16	CMPW	all “0"	R	Indicates on execution of ECMDTMCMP register setting to cntclk domain 0: Not executed 1: On execution of setting ECMDTMCMP
15-0	ECMTDMCMP[15:0]	all “0"	R/W	Delay timer compare value

4.2.31. ECM delay timer configuration register 0(ECMDTMCFG0)

ECMDTMCFG0 is read/write register. The value of this register controls whether delay timer starts or not when maskable error occurs.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECMTE031	ECMTE030	ECMTE029	ECMTE028	ECMTE027	ECMTE026	ECMTE025	ECMTE024	ECMTE023	ECMTE022	ECMTE021	ECMTE020	ECMTE019	ECMTE018	ECMTE017	ECMTE016
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMTE015	ECMTE014	ECMTE013	ECMTE012	ECMTE011	ECMTE010	ECMTE009	ECMTE008	ECMTE007	ECMTE006	ECMTE005	ECMTE004	ECMTE003	ECMTE002	ECMTE001	ECMTE000
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-0	ECMTE031-000	all “0"	R/W	Delay timer start control at maskable interrupt ECMPE031-ECMPE000 is for error factor 31-0(ecmterrin31-0) 0:Not start 1:Start

4.2.32. ECM delay timer configuration register 1(ECMDTMCFG1)

ECMDTMCFG1 is read/write register. The value of this register controls whether delay timer starts or not when maskable error occurs.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECMTE131	ECMTE130	ECMTE129	ECMTE128	ECMTE127	ECMTE126	ECMTE125	ECMTE124	ECMTE123	ECMTE122	ECMTE121	ECMTE120	ECMTE119	ECMTE118	ECMTE117	ECMTE116
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMTE115	ECMTE114	ECMTE113	ECMTE112	ECMTE111	ECMTE110	ECMTE109	ECMTE108	ECMTE107	ECMTE106	ECMTE105	ECMTE104	ECMTE103	ECMTE102	ECMTE101	ECMTE100
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-0	ECMTE131-100	all “0"	R/W	Delay timer start control at maskable interrupt ECMPE131-ECMPE100 is for error factor 63-32(ecmterrin63-32) 0:Not start 1:Start

4.2.33. ECM delay timer configuration register 2(ECMDTMCFG2)

ECMDTMCFG2 is read/write register. The value of this register controls whether delay timer starts or not when maskable error occurs.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	ECMTE228	ECMTE227	ECMTE226	ECMTE225	ECMTE224	ECMTE223	ECMTE222	ECMTE221	ECMTE220	ECMTE219	ECMTE218	ECMTE217	ECMTE216
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMTE215	ECMTE214	ECMTE213	ECMTE212	ECMTE211	ECMTE210	ECMTE209	ECMTE208	ECMTE207	ECMTE206	ECMTE205	ECMTE204	ECMTE203	ECMTE202	ECMTE201	ECMTE200
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-29	-	all “0"	R	Reserved
28-0	ECMTE228-200	all “0"	R/W	Delay timer start control at maskable interrupt ECMPE228-ECMPE200 is for error factor 92-64(ecmterrin92-64) 0:Not start 1:Start

4.2.34. ECM delay timer configuration register 3(ECMDTMCFG3)

ECMDTMCFG3 is read/write register. The value of this register controls whether delay timer starts or not when non-maskable error occurs.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECMTE331	ECMTE330	ECMTE329	ECMTE328	ECMTE327	ECMTE326	ECMTE325	ECMTE324	ECMTE323	ECMTE322	ECMTE321	ECMTE320	ECMTE319	ECMTE318	ECMTE317	ECMTE316
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMTE315	ECMTE314	ECMTE313	ECMTE312	ECMTE311	ECMTE310	ECMTE309	ECMTE308	ECMTE307	ECMTE306	ECMTE305	ECMTE304	ECMTE303	ECMTE302	ECMTE301	ECMTE300
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-0	ECMTE331-300	all “0"	R/W	Delay timer start control at non-maskable interrupt ECMPE331-ECMPE300 is for error factor 31-0(ecmterrin31-0) 0:Not start 1:Start

4.2.35. ECM delay timer configuration register 4(ECMDTMCFG4)

ECMDTMCFG4 is read/write register. The value of this register controls whether delay timer starts or not when non-maskable error occurs.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECMTE431	ECMTE430	ECMTE429	ECMTE428	ECMTE427	ECMTE426	ECMTE425	ECMTE424	ECMTE423	ECMTE422	ECMTE421	ECMTE420	ECMTE419	ECMTE418	ECMTE417	ECMTE416
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMTE415	ECMTE414	ECMTE413	ECMTE412	ECMTE411	ECMTE410	ECMTE409	ECMTE408	ECMTE407	ECMTE406	ECMTE405	ECMTE404	ECMTE403	ECMTE402	ECMTE401	ECMTE400
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-0	ECMTE431-400	all “0"	R/W	Delay timer start control at non-maskable interrupt ECMPE431-ECMPE400 is for error factor 63-32(ecmterrin63-32) 0:Not start 1:Start

4.2.36. ECM delay timer configuration register 5(ECMDTMCFG5)

ECMDTMCFG5 is read/write register. The value of this register controls whether delay timer starts or not when non-maskable error occurs.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	ECMTE528	ECMTE527	ECMTE526	ECMTE525	ECMTE524	ECMTE523	ECMTE522	ECMTE521	ECMTE520	ECMTE519	ECMTE518	ECMTE517	ECMTE516
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	15	14	13	12	11	10	9	9	7	6	5	4	3	2	1	0
	ECMTE515	ECMTE514	ECMTE513	ECMTE512	ECMTE511	ECMTE510	ECMTE509	ECMTE508	ECMTE507	ECMTE506	ECMTE505	ECMTE504	ECMTE503	ECMTE502	ECMTE501	ECMTE500
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	name	Reset	R/W	Definition
31-29	-	all “0"	R	Reserved
28-0	ECMTE528-500	all “0"	R/W	Delay timer start control at non-maskable interrupt ECMPE528-ECMPE500 is for error factor 92-64(ecmterrin92-64) 0:Not start 1:Start

4.2.37. ECM Error output clear invalidation configuration register (ECMEOCCFG)

This register is readable/writable register. Access by 16-bit units is possible for writing.
When this register's value exceed value of "error output clear invalidation counter (please see section 4.3.6)", it is possible to clear non-safe status of error output by SW.
Configure to this register only when error output status is safe. (error output mask logic consider neither whether the counter is run or not, nor whether error status is disabled)
This register is reset by erroutresz.
[Note1] This register setting need to be passed to cntclk domain. So, CMPW indicates that this setting is on execution. While CMPW bit is “1”, the write to this register is ignored. Please access this register after checking CMPW=0 and start from protection sequence. (CMPW does not suppress the access/ignore the protection sequence before final writing to this register. But, not guaranteed.)

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CMPW
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ECMEOUTCLRT[15:0]															
Reset value	0000h															
R/W	R/W															

bit	name	Reset	R/W	Definition
31-17	RFU	all “0"	R	Reserved
16	CMPW	all “0"	R	Indicates on execution of ECMEOCCFG register setting to cntclk domain 0: Not executed 1: On execution of setting ECMEOCCFG
15-0	ECMEOUTCLRT[15:0]	all “0"	R/W	The number of clock cycle which is possible to clear error output by SW.

4.3. Function description

In this section, detailed functions except error capture itself are described.

4.3.1. Error output mode

Error output such as ecmterroutz is non-dynamic mode (fixed level output) and dynamic mode (timer signal (ecmttin) output) selectable. Mode is defined by ECMSL0 bit of ECMEPCFG register.
[Note] ecmterroz is not affected by this mode setting. It's just only for ecmterroutz pin.

Tab. 4-2 Error output mode

Error Status ECMmSSE031-ECMmSSE000 ECMmSSE131-ECMmSSE100 ECMmSSE230-ECMmSSE200	Mode (ECMEPCFG.ECMSL0)	Error output mode	Error output	Error status
0	0	non-dynamic	H	no error
	1	dynamic	toggle (by ecmttin)	no error
1	0	non-dynamic	L	error
	1	dynamic	L	error

ECMmSSE231, which is used for ECMmESET status, and ECMmSSE232, such as loopback of ecmterroutz, are not considered because they are not error themselves.

To set the dynamic mode, following procedure is needed.
1. Initialize the source of ecmttin (usually timer pulse signal)
2. Set error output to high by writing "1" to ECMmECT bit of ECMmECLR.
3. Set ECMSL0 of ECMEPCFG to "1" in order to select dyamic mode.
4. Start the source of ecmttin.

To stop dynamic mode and set to non-dynamic mode, following procedure is neede.
1. Set ecmterroutz to low by writing "1" to ECMmEST bit of ECMmESET.
2. Stop the source of ecmttin
3. Set ECMSL0 of ECMEPCFG to "0" in order to select non-dynamic mode.

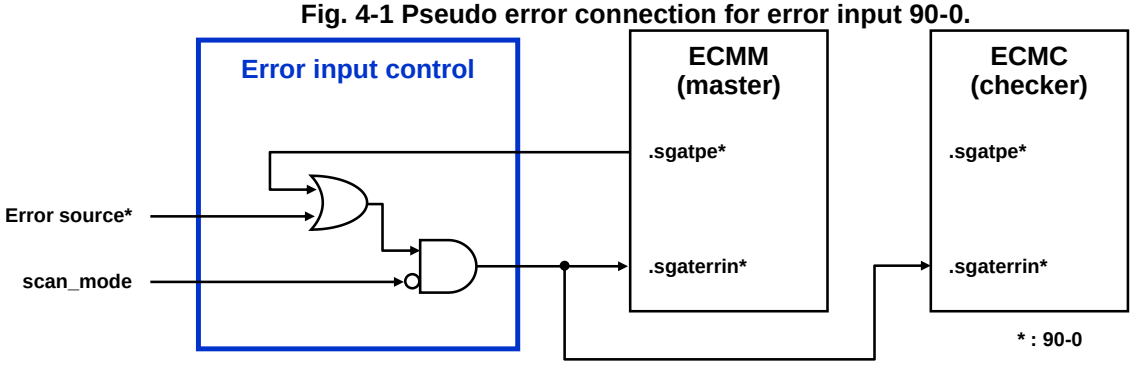
ecmterroutz signal is set to low in reset status. So, please use the ECM after ecmterroutz is cleared in consideration with the note in section 4.2.1.

4.3.2. Pseudo error generation feature

For self-diagnostics and debug purpose, pseudo error generation feature is prepared. The action after pseudo error generation is same as the actual error case because pseudo error function just loop-back the pseudo error signal into error input. The setting of error/interrupt/reset request mask and the setting of delay timer and error output clear mask are all considered as the action to the pseudo errors.

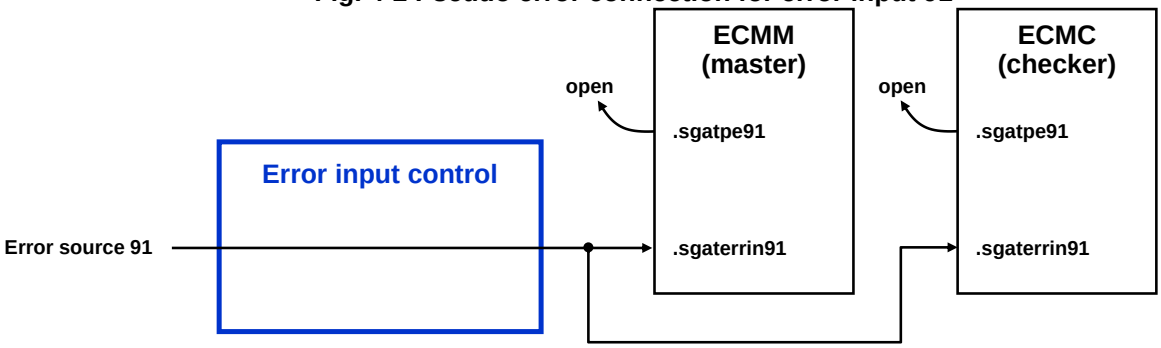
As the pseudo error input, master side of ECM core signal is used.
[note] Following figure use the old pin name for ECMM/ECMC. sgaxxx means that ecmxxx for ECM core module.

Fig. 4-1 Pseudo error connection for error input 90-0.



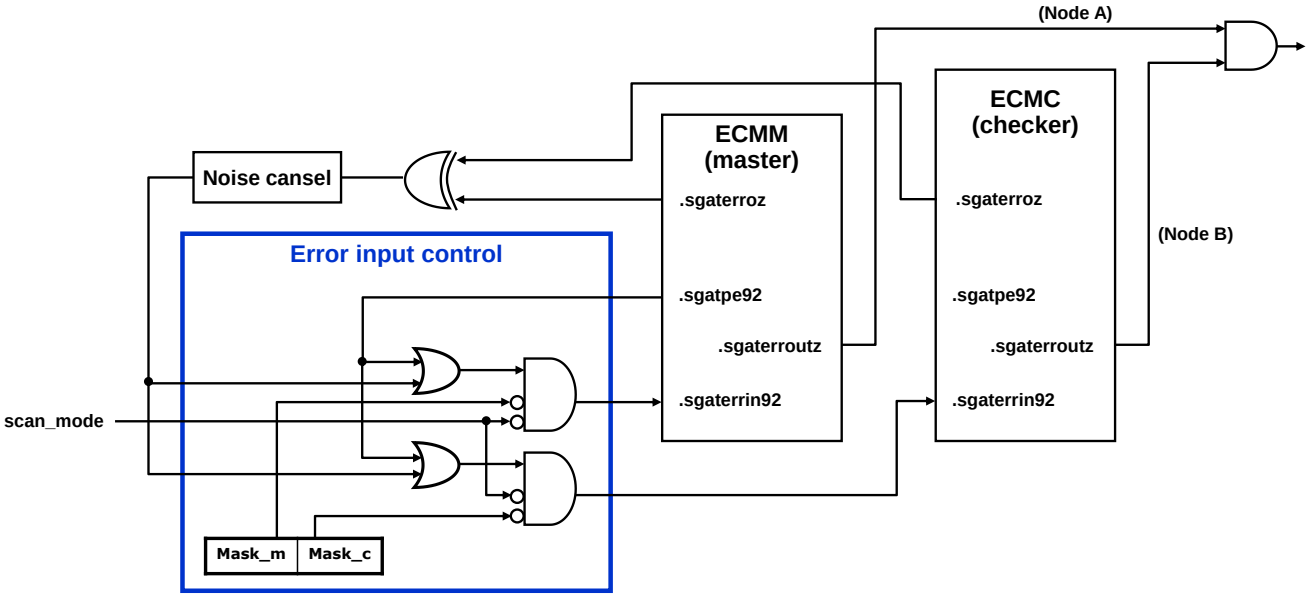
Error source bit 91 (ecmterrin91), which is used for unintended activated BIST, does not have pseudo error injection feature and scan_mode mask.

Fig. 4-2 Pseudo error connection for error input 91



For error input 92 (ECMmESSTR2.ECMmSSE28), such as ECM compare error have a feature to generate the inconsistent error input which cause actual ecmterroz and ecmterroutz.

Fig. 4-3 Pseudo error connection for error input 92



[Note1] Mask_m and Mask_c register is not prepared in uhiapecm0020. uhiapecm0020 prepares the ecmterrin92msk_m pin and ecmterr92msk_c pin.
[Note2] Noise cansel logic is prepared for the asynchronous ecmterroz signal xor. In order to avoid the glitch at the rising edge of this signal, following three signal AND is used.

1. XOR of ecmterroz of master core and checker core : (A)
2. 1cycle PCLK delay of (A) : (B)
3. 1cycle PCLK delay of (B) : (C)

For ECMmESSTR2.ECMmSSE29, which is used for delay timer overflow, pseudo error injection is internal ECM core module.
For ECMmESSTR2.ECMmSSE31-30 does not have the pseudo error input.

4.3.3. ecmterroutz loop back feature

To check the path to error output pin as 1-chip level, ECMmESSTR2.ECMSSE31 is assigned to monitor ecmterrlbz pin. This monitor path considered that ecmterrlbz is stable signal. So, any synchronization logic does not have the path to PRDATA. So, in order to read the correct error, S/W on CPU handling like reading twice is needed.

4.3.4. Error status

Error status is inciated by ECMmESSTR0/1/2. This register can be reset only by external pin reset, such as resstg1z and pclkin_resstg1z. This register can be also cleared by writing “1” to ECMESSTC0/1/2.
Error status is kept when internal reset, such as erroutresz or PRESETn, occurs. After reset is released, user can confirm the reset factor, which cause the internal reset, by reading ECMmESSTR0/1/2.
[Pending item] For PFC1B base macro mask the error input (ecmterrin) by scan_enable. But PCLK for ECMmESSTR01/2 is not masked by scan_mode. After checking the reset and clock activation sequence for CCC, the isolation method of this register is determined.

4.3.5. Delay timer feature

Delay timer is started when interrupt is asserted. If S/W on CPU cannot stop the delay timer and the value of delay timer become the same as the value of ECMDTMCMP register, ECM can assert ecmterroutz and/or ecmtresz (reset request).

Delay timer starts from the count “0”, please set the proper value to ECMDTMCMP and ECMDTMCFG0-5 register.

Delay timer runs with cntclk.
Delay timer is implemented both in ECM core master side and checker side. So, delay timer start trigger of master and checker side is OR-ed outside ECM core module (and synchronized to cntclk clock) and loop back to ECM core master and checker side as the delay timer start trigger.

Delay timer related registers, such as ECDTMCMP and ECMDTMCFG0-5, should not be modified while delay timer is activated. Otherwise this may cause the glitch of deley timer overflow detection signal.

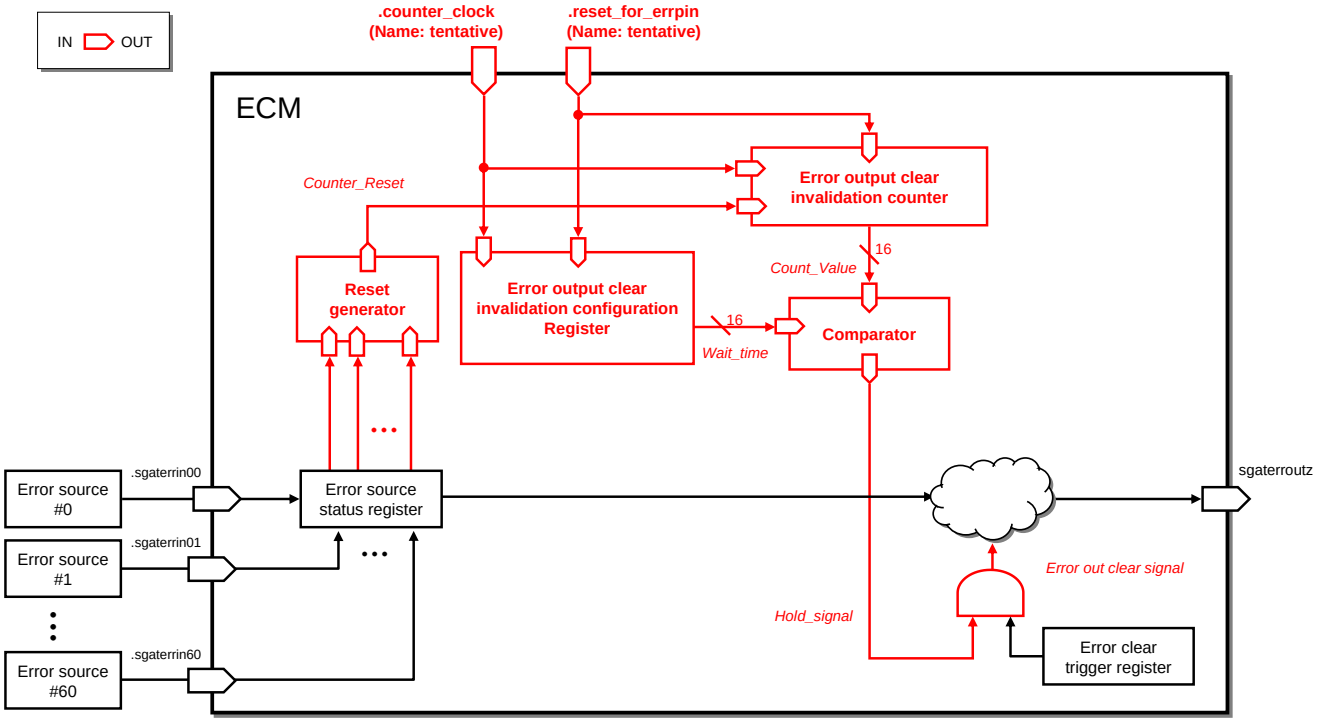
[Note] The timer value is not stopped in debug break (svaccess).

4.3.6. Errorout clear mask feature

Once ecmterroutz is asserted, ECM has the feature to prevent the ecmterroutz clear by writing ECMmECLR register. Once error is inserted, error output clear invalidation counter is cleared and clear of ecmterroutz by writing ECMmECLR register (See the conceptual image below).
This counter runs with cntclk and reset by erroutresz. (Counter initial value by erroutresz is FFFFh and kept until counter reset signal is asserted.)

If an error is set to ECMmESSTR0/1/2 register is set, counter value is reset and start the counter.
If another error source is set before counter value reached to ECMEOCCFG, counter is cleared and count-up again.
[Note] If same error is reported to ECM, counter value is not cleared because ECMmESSTR0/1/2 is the stable status register.

Fig. 4-4 Conceptual image of errorout clear mask feature



Actual implementation, counter reset signal is synchronized outside ECM core module like delay timer and loop-back to ECM core as counter reset trigger signal.

[Note] The timer value is not stopped in debug break (svaccess).

Followings are implmentation image of terroutz logics in ECM core module.
Clear request by writing ECMmECLR register is masked by eclmsk logic.
[Note1] This mask logic does not actived by ECMmESET action
[Note2] clr_ctl request during handshke in clrctlsync (PCLK->cntclk) is ignored.
[Note3] Because of ECM error status is asserted completely asynchronous logic and need to be synchronized to cntclk, which is much slower than CPU clock, in order to make the trigger of error mask timer. So following situation may occur and unavoidable.

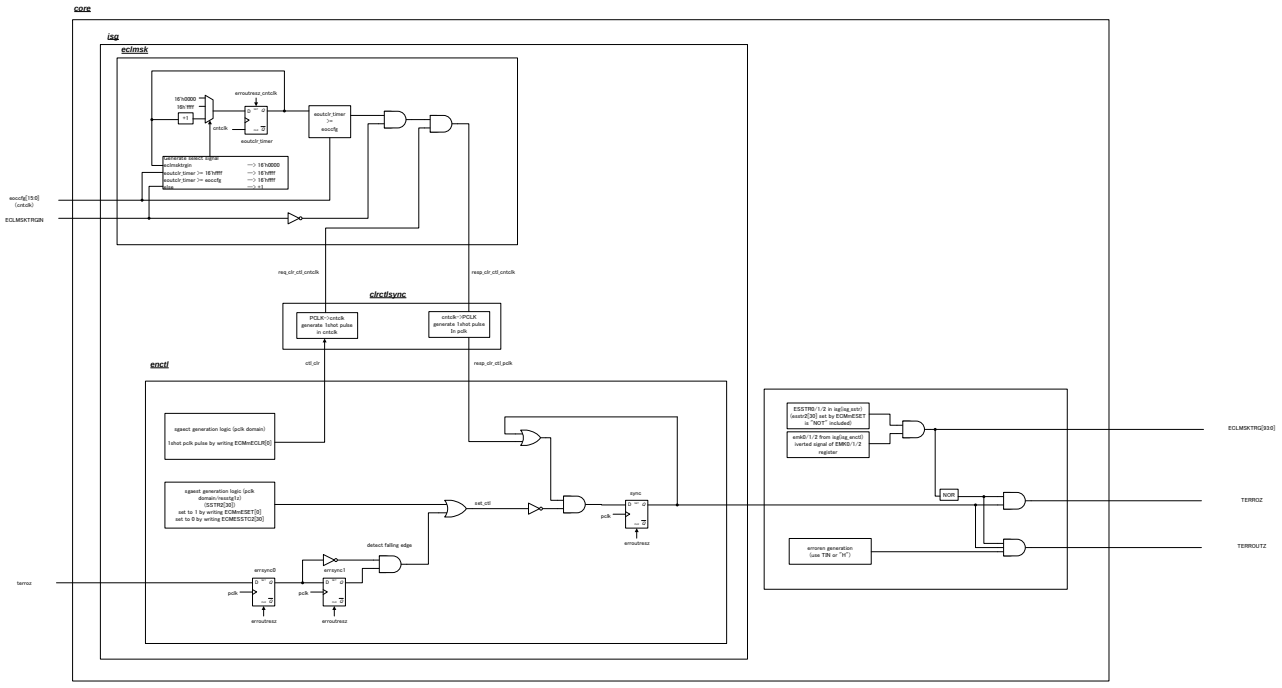
1. CPU clear all status register and write ECMmECLR to make terroutz to high.
2. During item 1, next error occurs
3. Error clear request passes the error clear mask
4. Error mask trigger reach this error mask logic

This situation lead to the result :

1. “sync” signal, which holds the terroutz to low (unsafe state), is released.
2. error clear mask counter is runnning

To avoid this situation, masking error by enabling ECMEMK0/1/2 is needed. In such case, terroutz is re-asserted after ECMEMK is disabled even if the above situation occurs.
If delay timer is activated and reset by delay timer is activated during ECMEMK is enabled, delay timer can assert reset request internal reset and internal reset will clear ECMECMK, which leads to assert terroutz (unsafe state).

Fig. 4-5 errorout logic in core module



4.3.7. Protection by access sequence

Several configuration registers indicated in section 3.3.1 are protected by access sequences.

In order to write sequence protected registers are as following.

1. Write 000000A5h to ECMmPCMD0 or ECMPCMD1 register
2. Write intended value to protected register.
3. Write inverted value to protected register.
4. Write intended value to protected register again.
5. Check ECMPRERR=0 of ECMPS, and check the protected register whether the required value has been written.

If another access is executed by CPU while the sequence from 1 to 4, the action of this module is as following :

・If the accessed register is included in ECM module, the write access to protected register is failed (Set "1" to ECMPRERR of ECMPES register). Please retry from sequence 1.

・If another register is not the ECM register, sequence is not failed.

If break is occured (svaccess is asserted) while the sequence from 1 to 4, the access to sequence protected register is not failed. The access is executed after svaccess is released.

4.3.8. Debug feature (svaccess)

As the feature for 1-chip debug, separated write sequence protection for svaccess is prepared.
While svaccess is asserted,
Access sequence is as following.

1. Write 000000A5h to ECMmPCMD0 or ECMPCMD1 register
2. Dummy write to protected register.
3. Dummy write to protected register.
4. Write intended value to protected register.

For write dummy access, any protected register is ok different from normal sequence described in section 4.3.7.

4.3.9. Write only register in testmode

Several write only register like ECMmESET register etc. can be read in testmode. But, these register read just read the 1shot pclk pulse of these kinds of trigger register. So, this feature has no meaning for the product that cannot execute APB read access after write access without interval.

5. Other design issue.

5.1. False path

ECM has several false paths in order to capture the asynchronous error input even if clock distributed to ECM is stopped

Followings are considered to be false path. for :

- Input path to ESSTR asynchronous set pins
- Input path to asynchronous pulse shaper
- PCLK<->cntclk cross domain path.

```
set_false_path -from SYS_CLK(cntclk) -to PCLK
set_false_path -from PCLK       -to SYS_CLK(cntclk)

set_false_path -through [get_ports ecmterrin91]
set_false_path -through [get_ports ecmterrlbz]
set_false_path -through [get_ports ecmttin]

set_false_path -through [get_pins ecg/terrin*]
set_false_path -through [get_pins ecmm/SGATERROUTZ]
set_false_path -through [get_pins ecmm/SGATERROZ]
set_false_path -through [get_pins ecmm/SGATI]
set_false_path -through [get_pins ecmm/SGATNMI]
set_false_path -through [get_pins ecmm/DTMTRGOUT]
set_false_path -through [get_pins ecmm/ECLMSKTRG[*]]
set_false_path -through [get_pins ecmc/SGATERROUTZ]
set_false_path -through [get_pins ecmc/SGATERROZ]
set_false_path -through [get_pins ecmc/SGATI]
set_false_path -through [get_pins ecmc/SGATNMI]
set_false_path -through [get_pins ecmc/DTMTRGOUT]
set_false_path -through [get_pins ecmc/ECLMSKTRG[*]]

# asynchronous pulse phaper
set_false_path -through [get_pins pshap/pshaps/CLR*]
set_false_path -through [get_pins pshap/pshaps/OUT*]
set_false_path -through [get_pins pshap2/pshaps0/CLR*]
set_false_path -through [get_pins pshap2/pshaps0/OUT*]
set_false_path -through [get_pins pshap2/pshaps1/CLR*]
set_false_path -through [get_pins pshap2/pshaps1/OUT*]
```

5.2. Multi-Cycle Path

There is no multi-cycle path in this module

5.3. Asynchronous constraint

This will be described in the next version.

ECM has several asynchronous logics in order to capture the asynchronous error input even if clock distributed to ECM is stopped.

End of Document