

Chip Layout Design

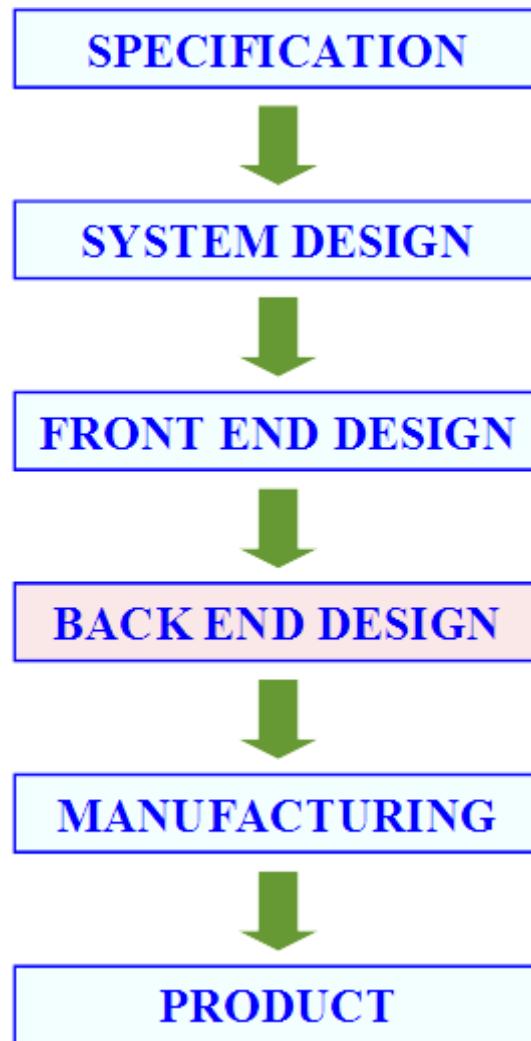
Renesas Design Vietnam Co., Ltd.
Training Center

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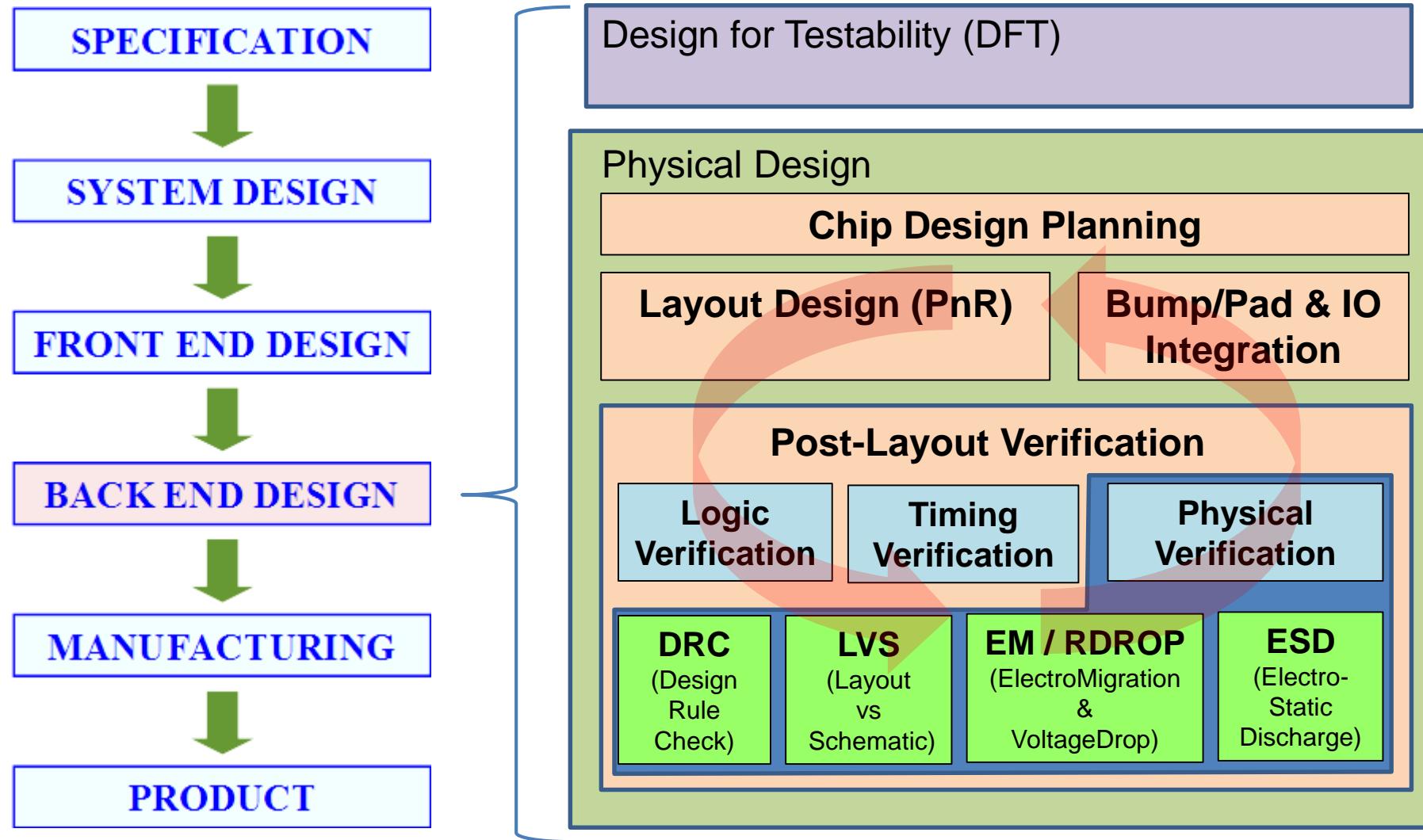
Overview of Chip Layout Design

Position in SoC design flow



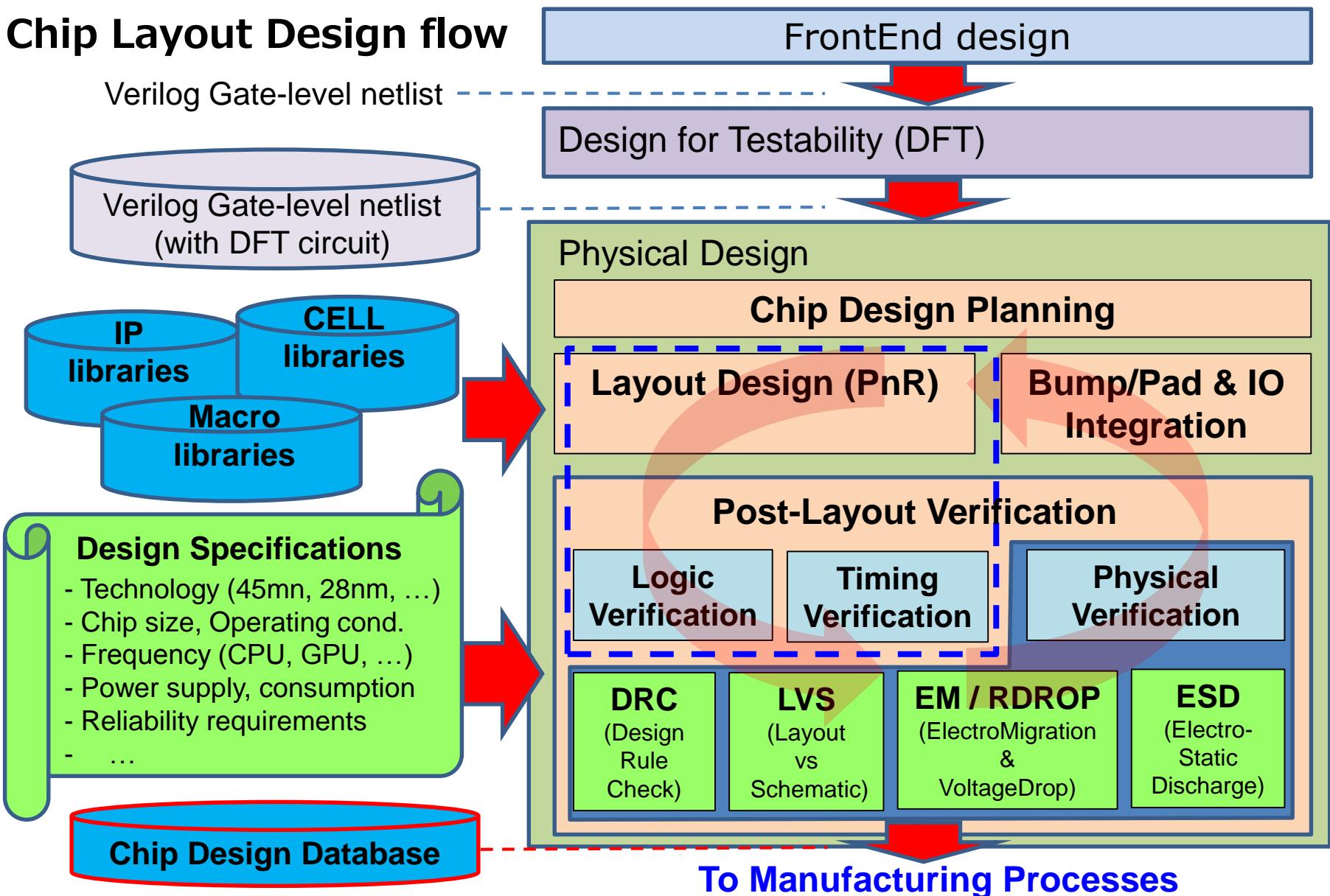
Overview of Chip Layout Design

Chip Layout Design flow



Overview of Chip Layout Design

Chip Layout Design flow



Content

1. Overview of Chip Layout Design
- 2. Cell and Library**
3. Understand about Layout Design
4. Chip design planning
5. Bump/Pad and IO integration
6. Block and TOP level layout design (PnR)
7. Post-Layout verification

Cell and Library

What is a cell ?

A **cell** is **macro** or **functional unit** that performs common operations and is used to build more complex logic blocks.

Examples:

- Standard cells : Inverter, NAND, NOR, Flip-Flop, Latches and Buffers.
- Macro cells : ADC (Analog to Digital converter), DAC, THS (Thermal sensor), USB, PCI
PLL (Clock pulse generator)

Cell and Library

What is a cell library ?

A cell library often refers to a collection of cells.

- Standard cell library (Primitive cell Library)
- I/O cell library
- Memory (Compiled memory, Fixed size memory)
- Analog (ADC, DAC, PLL, USB, THS)

Cell library consists of :

- Schematics (Transistor level circuits.Usually, not released)
- Frontend model (Verilog, VHDL, Liberty(.DB), other support libraries)
- Backend Model (LEF, ASTRO/Milkyway, GDS(Layout), CDL)

LEF and ASTRO are cell information which shows locations of ports, cell size, wiring prohibition area, ... used for Place-and-Route.

LEF is often used for Cadenc P&R tool

ASTRO/MILKYWAY is often used for Synopsys P&R tool

GDS is a design database format for design transfer

CDL is format of design circuit netlist, used in LVS verification (*Layout-versus-Schematic*), or ESD verification, ...

Cell and Library

What is a cell library ? – Example of library model (INVERTER)

Verilog (.v)

```
`ifdef TS_OFF
`else
`timescale 1ps/1ps
`endif
`celldefine
`ifdef verifault
`suppress_faults
`enable_portfaults
`endif

`ifdef FAST_FUNC
`delay_mode_zero
`else
`delay_mode_path
`endif

module TCAINVXC( A,YB );
output YB;
input A;
reg notifier;
not (YB,A);

`ifdef FAST_FUNC
`else
.....

```

Liberty (.lib)

```
cell(TCAINVXC){
area : 3.0;
cell_leakage_power : a;
cell_footprint : INVX_;
pin(YB){
function : "!(A)";
max_fanout : 50;
max_capacitance : b;
capacitance : 0.000000;
direction : output;
internal_power() {
related_pin : "A";
fall_power(pwr_tin_oload_3x3){
index_1 (" , , ");
index_2 (" , , ");
values(" , , ", \
"- , , ", \
" , , ");
}
rise_power(pwr_tin_oload_3x3){
index_1 (" , , ");
index_2 (" , , ");
values(" , , ", \
" , , ", \
" , , ");
}
}
.....

```

LEF (.lef)

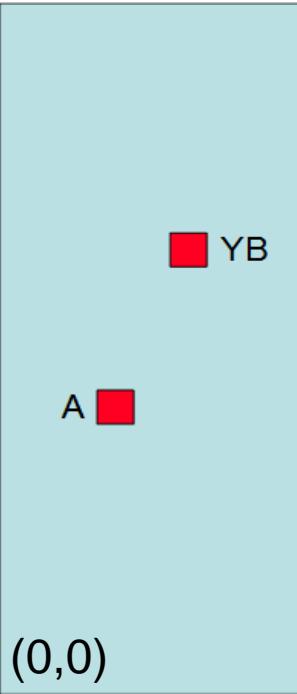
```
MACRO TCAINVXC
CLASS CORE ;
FOREIGN TCAINVXC 0.000 0.000 ;
SIZE 0.840 BY 2.520 ;
SYMMETRY Y X ;
ORIGIN 0.0 0.0 ;
SITE CORE009 ;
PIN A DIRECTION INPUT ;
USE SIGNAL ;
AntennaGateArea 0.14 LAYER M1 ;
AntennaPartialMetalArea 0.104 LAYER M1 ;
PORT
LAYER M1 ;
RECT 0.170 0.970 0.350 1.550 ;
END
END A
PIN YB DIRECTION OUTPUT ;
USE SIGNAL ;
AntennaPartialMetalArea 0.242200 LAYER M1 ;
AntennaDiffArea 0.331200 LAYER M1 ;
PORT
LAYER M1 ;
RECT 0.490 0.380 0.630 2.110 ;
END
END YB
.....
```

Actual numbers are deleted from original .lib

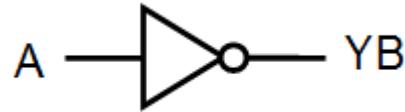
Cell and Library

What is a cell library ? – Example of library model (INVERTER)

PnR Layout view

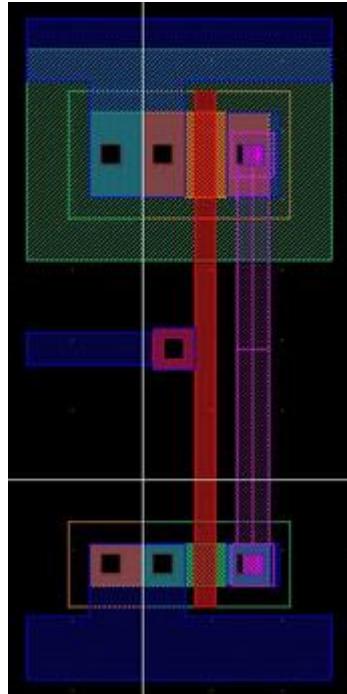


Logic symbol



(0.840, 2.520)

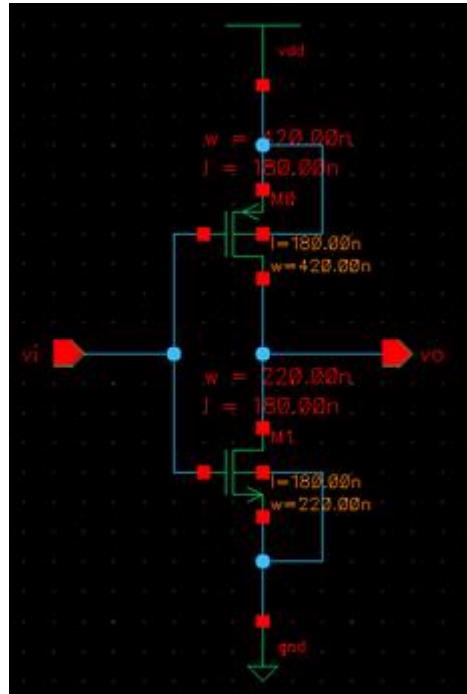
Detailed layout



CDL model (.cdl) (aaa~ddd is MOS size)

```
.SUBCKT TCAINVXC A YB  
XI2 A YB VDD VSS / TCXINV wn=aaa u wp=bbb u  
XI0 A YB VDD VSS / TCXINV wn=ccc u wp=ddd u  
.ENDS
```

Schematic view (Circuit)



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Understand about Layout Design

Layout design Methodology

1) Individual design method

Design with interactive mode EDA tool (interactive design)

Eg: applied in custom layout design, std cell / Analog layout design, ...

2) Master slice method (gate array method) P&R

Common master layout with buried transistors is ready and automatic wiring tool is applied to do layout.

The development cost is small thanks to the buried gate-array.

Since **base wafers are already prepared**, the manufacturing period is short.

3) Cell base method P&R

P&R area of cell/module are changeable.

It is necessary to minimize the chip size.

4) Hierarchical cell base method P&R

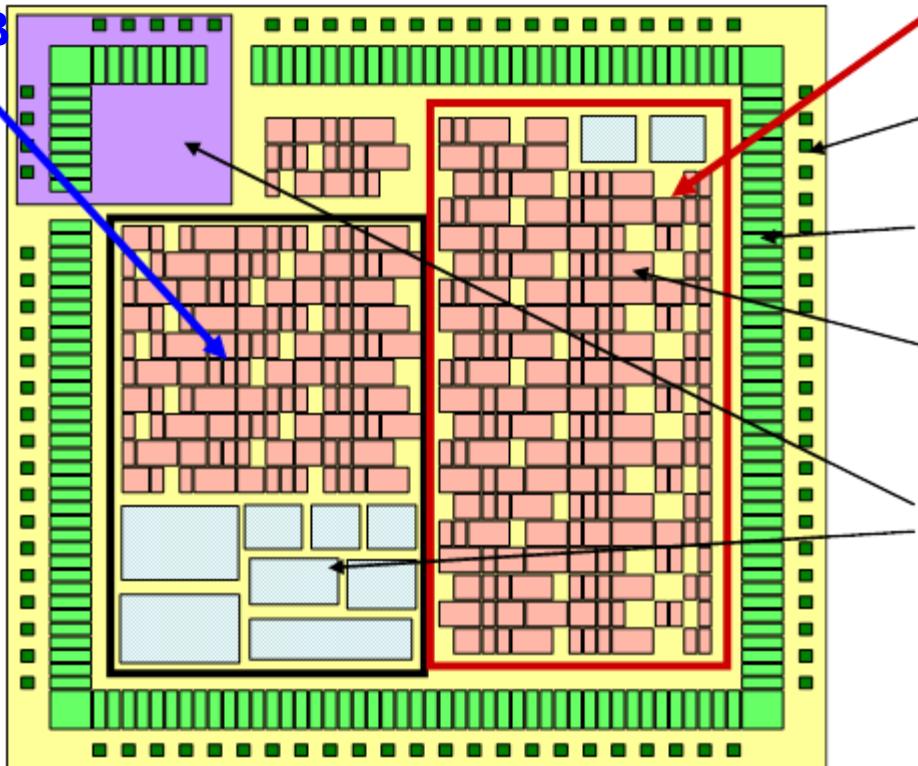
A hierarchical design of method(3) where **logic is split from the top down**, and **layout is done from the bottom-up**.

Understand about Layout Design

Hierarchical cell based method

The standard cell placement area is done layout hierarchically depending on the hierarchical logical structure of the gate level netlist. **Automatic P&R is applied.**

Hierarchical logic B



Hierarchical logic A

Bonding PAD

IO cell (free placement)

Internal cell row
(Standard cell placement area, flat placement)

IP modules areas (memory and analog, etc, free placement)

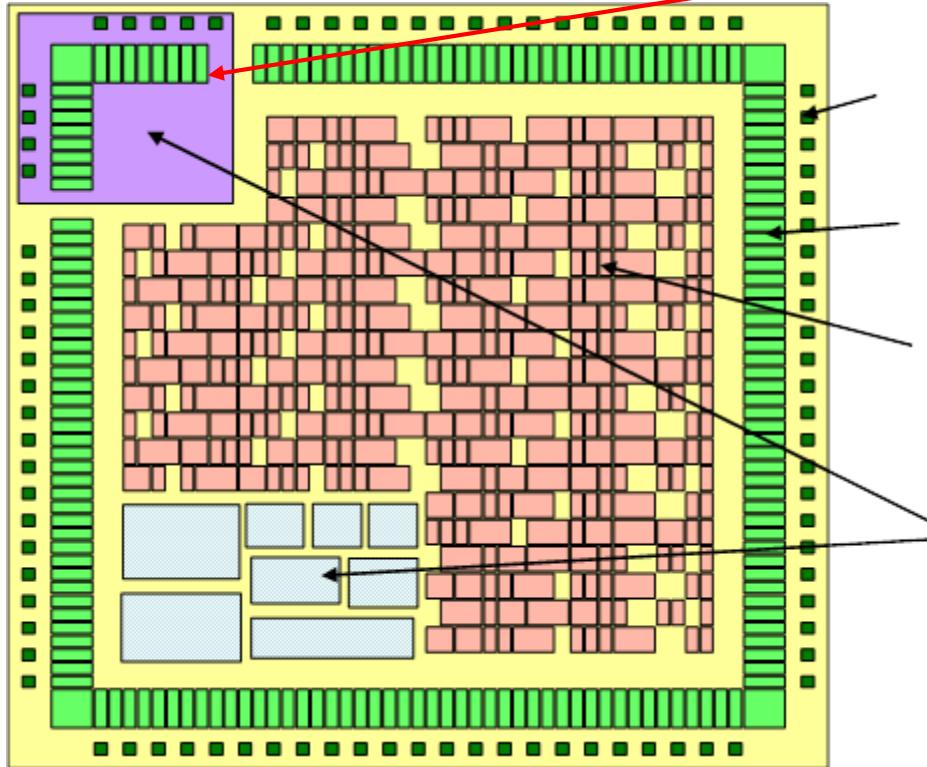
All areas are for the wiring areas.
(wiring can run in free channels and though over cells)

Hierarchy block A and B are done PnR separately and are called into TOP design as a cell (HM, block, design)

Understand about Layout Design

Cell-based method

Because cells can be arbitrarily placed, it is adopted by the layout design for general SoC. Automatic P&R is applied. Multi-layer metals are used.



Analog IOs and digital IOs are separated to avoid the digital noise.

Bonding PAD

IO cell (free placement)

Internal cell row

(Standard cell placement area, flat placement)

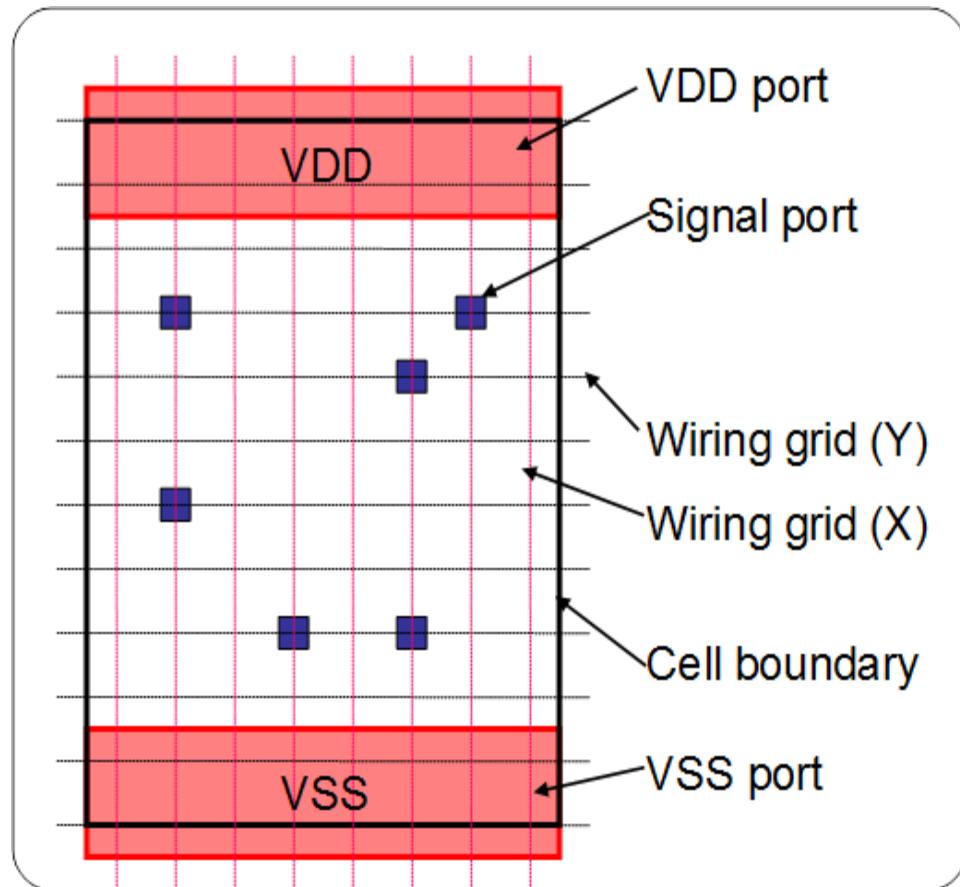
IP modules areas (memory and analog, etc, free placement)

All areas are for the wiring areas.
(wiring can run in free channels and through over cells)

Understand about Layout Design

Cell-based method

◆ Standard cell structure of cell based method



The width of the cell is changeable.
(integral multiples in X wiring grid)

The height of the cell is constant.
(integral multiples in Y wiring grid)

The signal port is “on grid”.
(for routability)

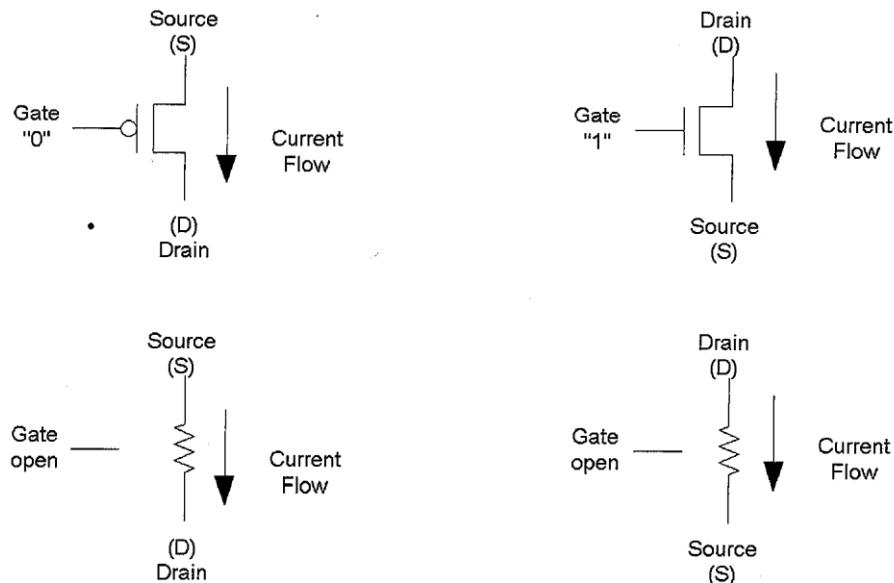
Power supply ports are fixed in the
cell. Y location is same to all cells.

Metal wirings can run over cells.

Understand about Layout Design

Transistor Layout

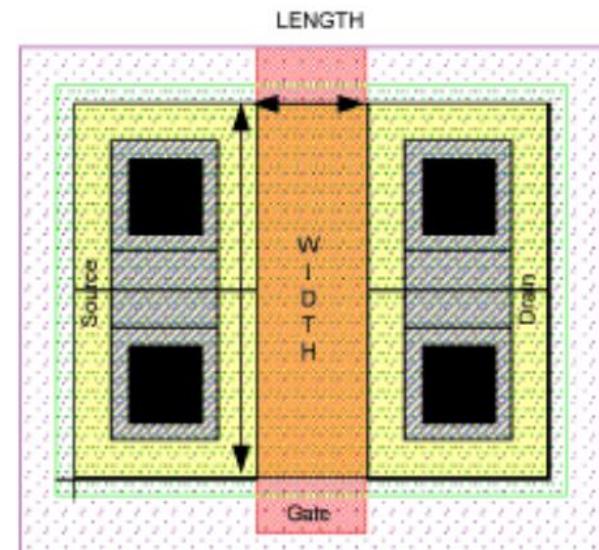
Basic symbol of PMOS and NMOS



PMOS and NMOS Transistors

Gate-size in a technology refers to min.gate-length (the narrowest poly-silicon that can be manufactured reliably) in that technology.

Eg. in T28: Ld35, Ld40

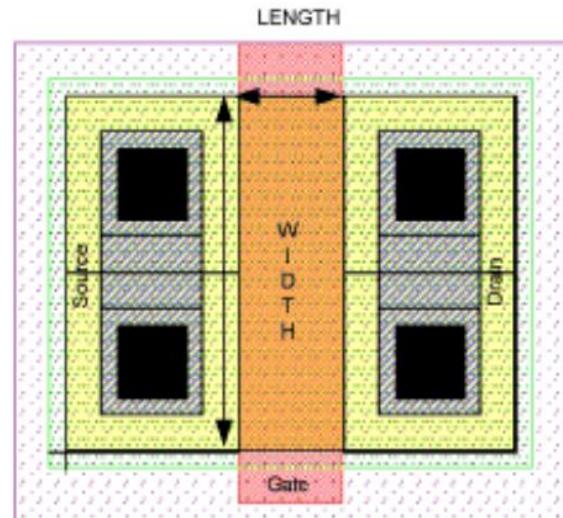
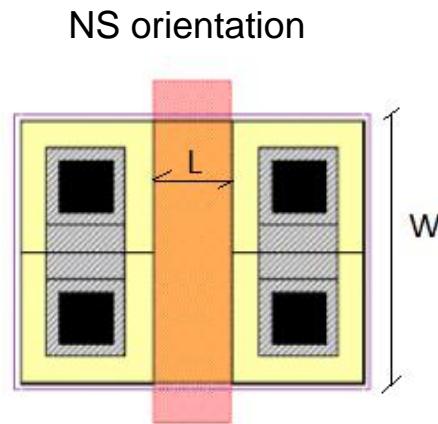
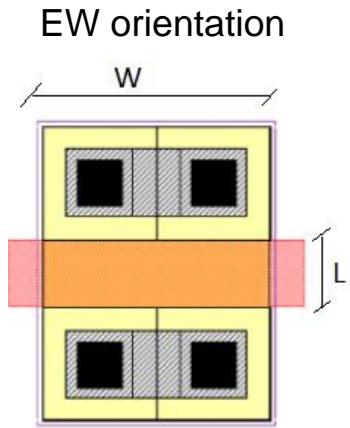


Transistor layout from top view

Understand about Layout Design

Transistor Layout

The **length** and **width** of a transistor are the two most important dimensions of a transistor. When we talk about the **gate size** of a specific technology, they are referring to the minimum **gate length**.



In terms of layout design, the length of a transistor is the distance between source and drain.

In terms of manufacturing capabilities, the length of a transistor is **the narrowest possible piece of polysilicon (poly)** that can be **manufactured reliably**.

Smaller poly dimensions and thus smaller transistors results in smaller ICs (chip), so it is attractive to use the minimum gate length to minimize chip area.

Understand about Layout Design

Transistor Layout

In terms of transistor performance, the length of the transistor is **the distance** electrons have to travel when the gate is "on" or "open", to produce a measurable current flow.
(Effective Channel Length)

Remember, it is the **gate voltage** that **controls the flow of current**.

If the distance between the source and drain is reduced, the gate voltage has a stronger influence in enabling current flow.

The current flow is increased when **W is increased** or **L is decreased**.

$$Id = \frac{W}{2L} \mu Cox (Vg - Vth)^2$$

(equation of saturation current)

Note:

Proportional : W, μ , Cox, $(Vg - Vth)$
inversely proportional : L

$Muy (\mu)$: mobility

Cox = $Epsilon_{ox} / tox$

tox : gate-oxide thickness

$Epsilon_{ox}$: gate permittivity of silicon

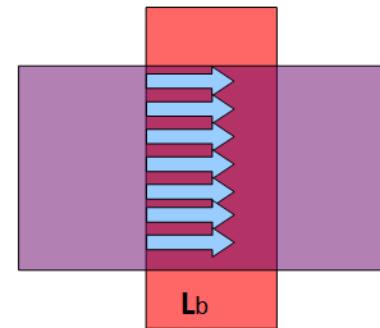
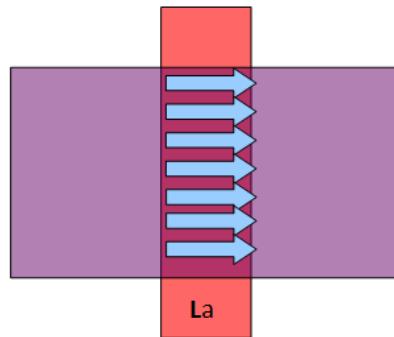
$Epsilon_0$: $8.85e-2 F/m$

Good insulator : $epsilon_{ox} = 3.9 * epsilon_0$

Understand about Layout Design

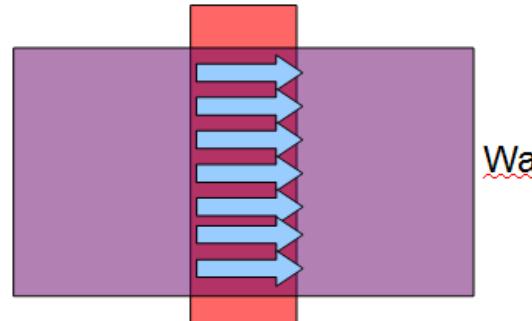
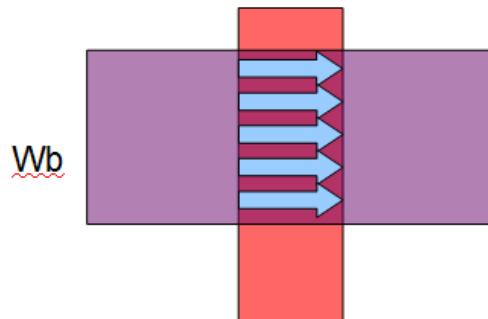
Transistor Layout

In the same process technology, if two transistors have the same **W** but different **L**, the transistor with shorter **L** will produce more current, which means **faster** performance.



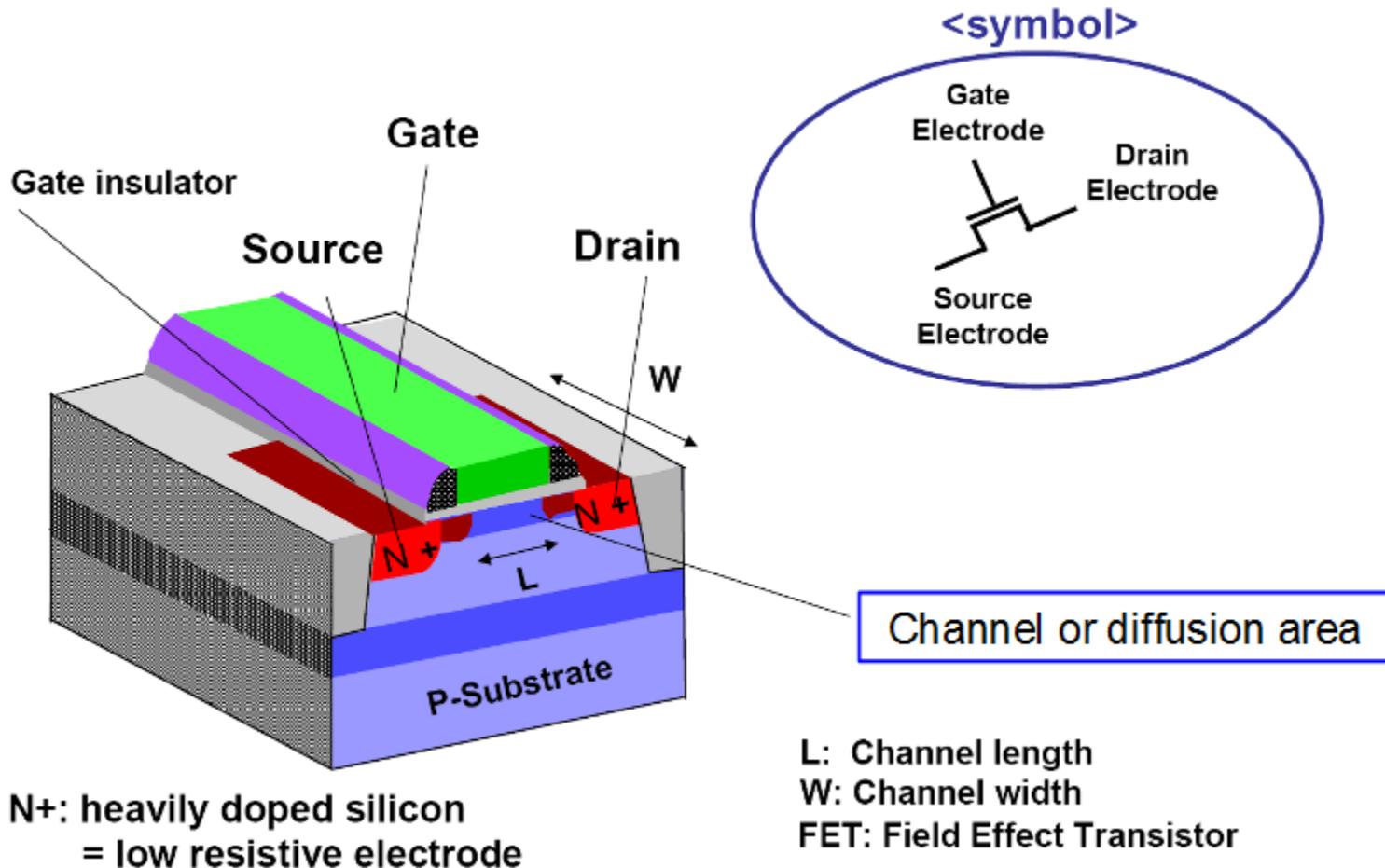
The width of a transistor can be seen as the number of parallel channels available for current to pass from source to drain. Wider transistors allow more current.

So if two transistors have the same **L**, the transistor with wider **W** will produce more current.



Understand about Layout Design

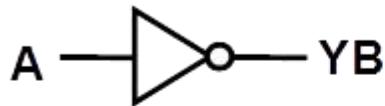
3D-image of a TRANSISTOR



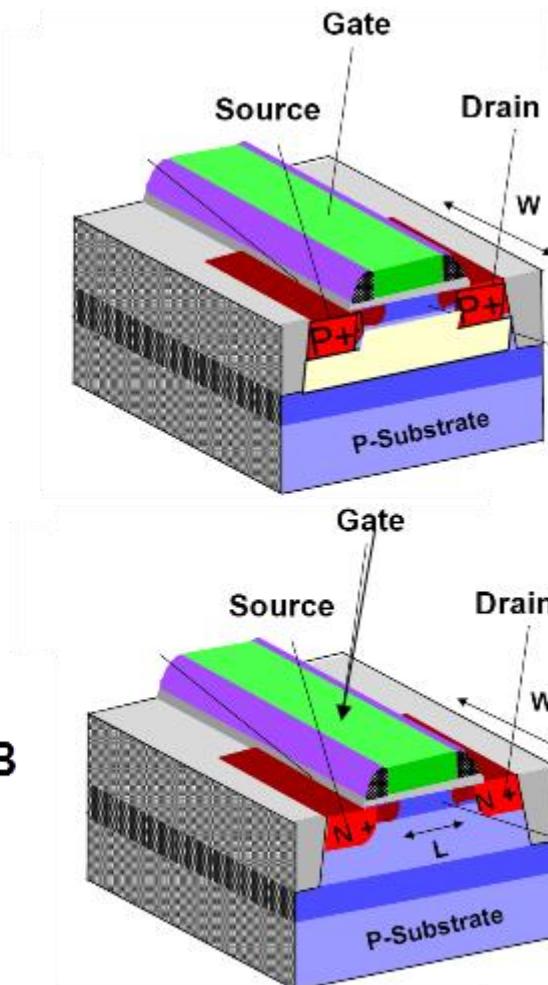
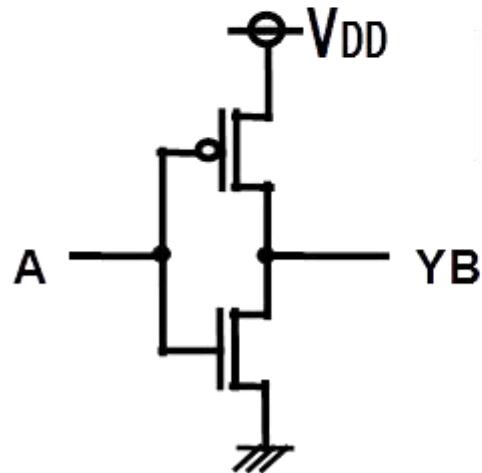
Understand about Layout Design

Cell layout of an INVERTER

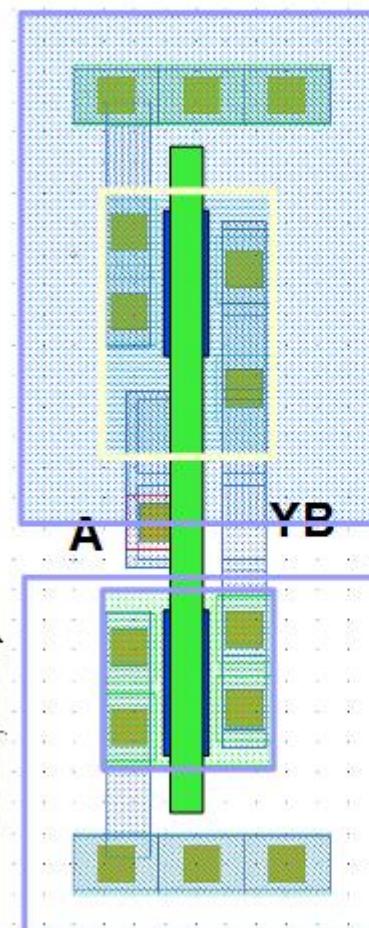
Logic Symbol



Circuit



NWELL-Contact



P-channel

N-WELL

N- channel

P-WELL

PWELL-Contact

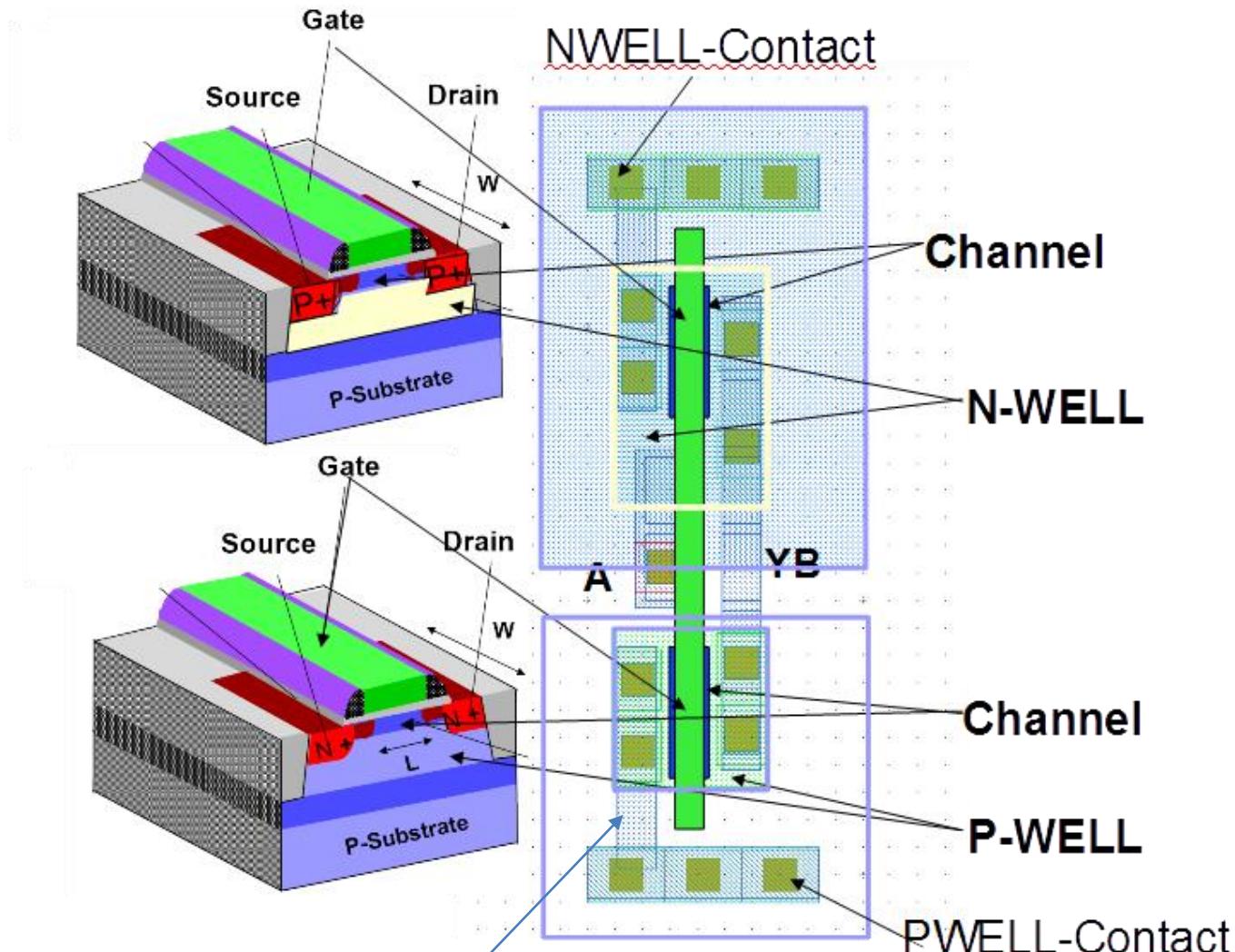
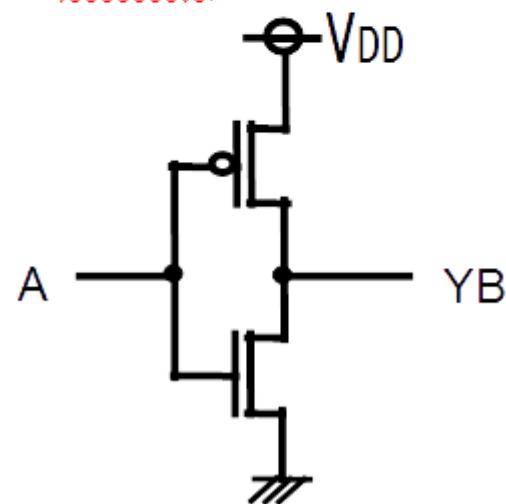
Understand about Layout Design

Cell layout of an INVERTER

Truth Table

Input	Output
A	YB
L	H
H	L

uCircuit

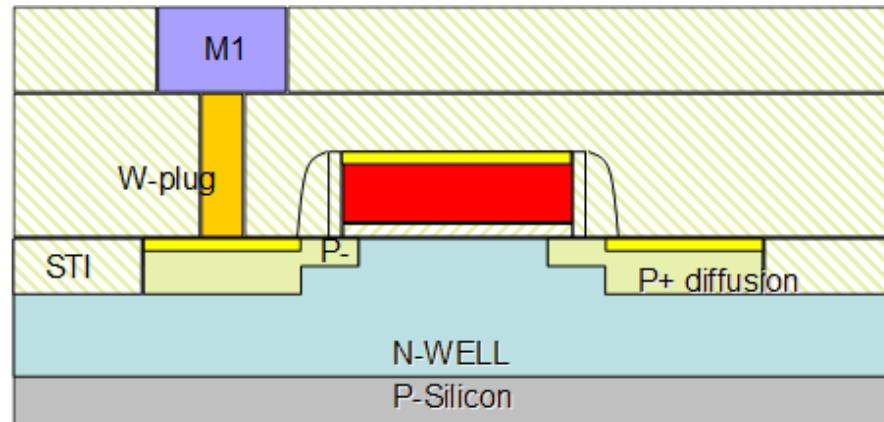
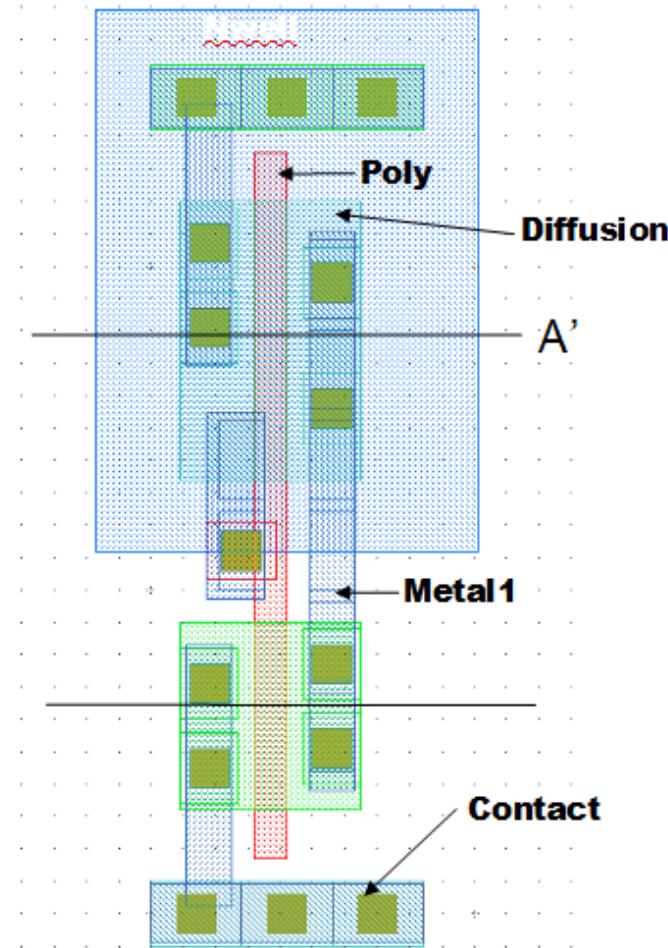


Drain/source pins will be connected upper layer via contacts

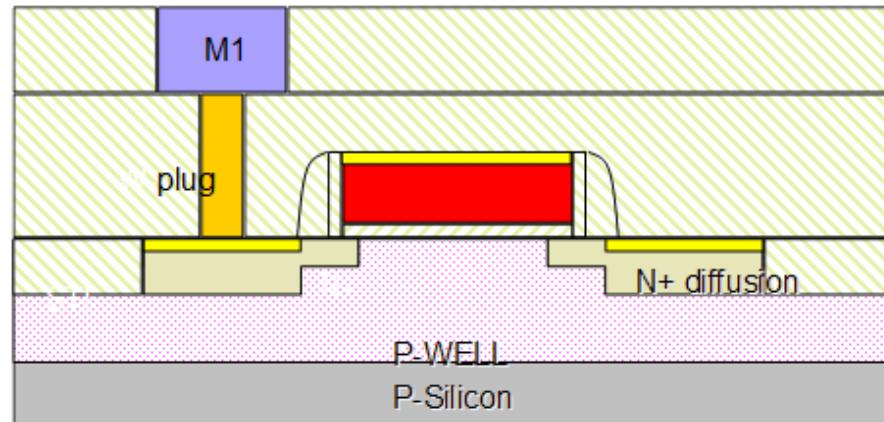
Understand about Layout Design

Cell layout of an INVERTER

Cross Section of Cell



The cross-section at A-A'.



The cross-section at B-B'.

Understand about Layout Design

Layers and Connectivity

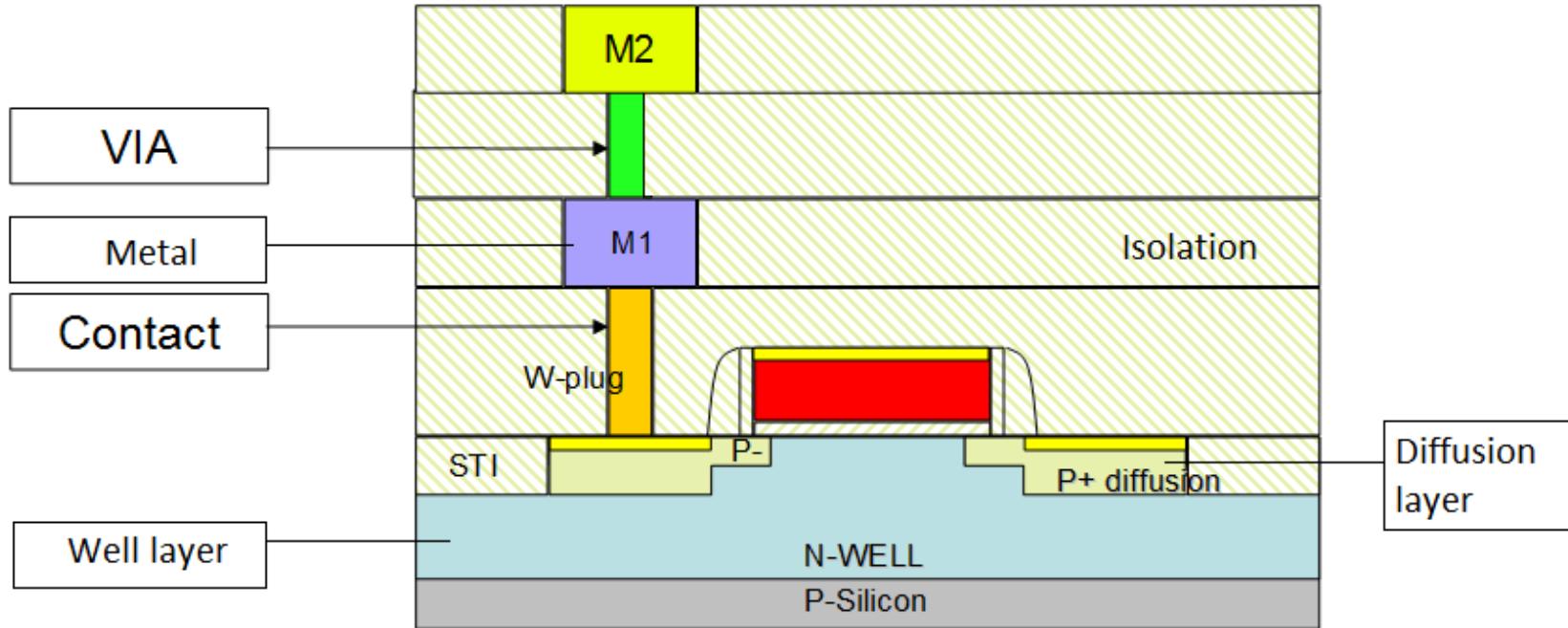
Conductors : metal, polysilicon layers, diffusion layers, well layers

Isolation layers: insulator layers to isolate conducting layers to avoid “short-circuit”
They are never drawn, but are always implied from mask layers.

Contacts, vias : These layers define cuts in the insulation layer.
Vias connect metal layers

Contacts connect lowest metal layer (M1) down to polysilicon or diffusion layers.

Implant layers : Are not physical layers. They are CAD layers used to create other layers



Understand about Layout Design

Example of cell layout design (Transistor layout)

Exercise

Providing that:

Ids of unit width for NMOS is $20\mu A/\mu m$.

One contact can flow $50\mu A$ /piece.

Metal can flow $20\mu A$ per μm width.

When designing 1 MOS transistor which needs current flow of $200\mu A$, how many contact holes are needed for each diffusion region (S, D) ? Also, calculate the width of the metal connected to the diffusion region.

Understand about Layout Design

Example of cell layout design (Transistor layout)

Exercise-Ans

I_{dsmax} = 200uA,

Diffusion Width
then width = Channel width = $I_{dsmax} / 20\mu A$ (per um),
= 10um

The metal and vias must be able to carry a current of I_{dsmax} .

Number of Contact = $I_{dsmax} / 50\mu A$ (per contact) = 200uA / 50uA = 4
So, 4 contacts are needed for each diffusion (S, D)

Metal width
then metal width = $I_{dsmax} / 20\mu A$ (per um width),
= 10um.

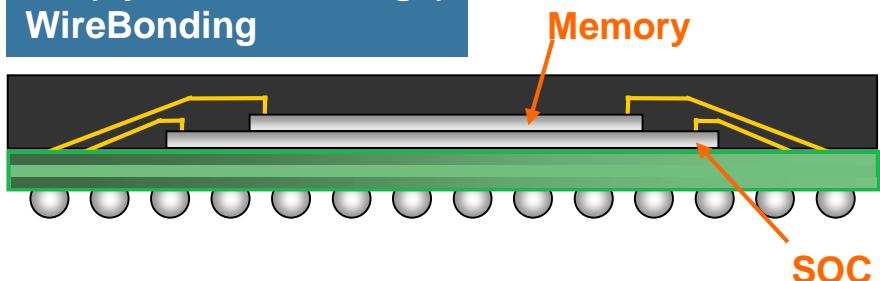
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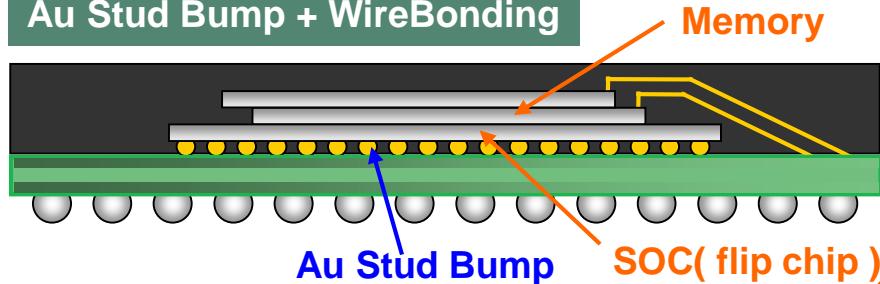
Chip Design Planning

Package types

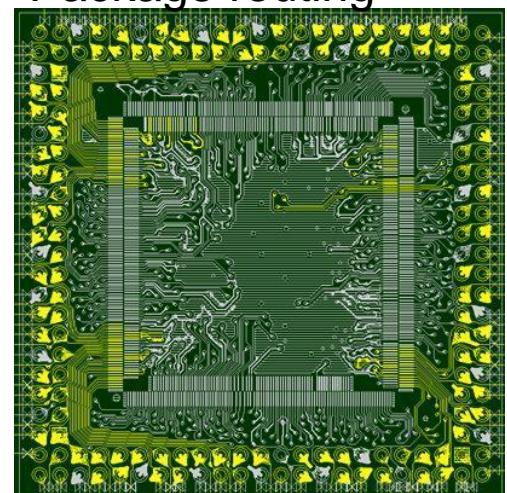
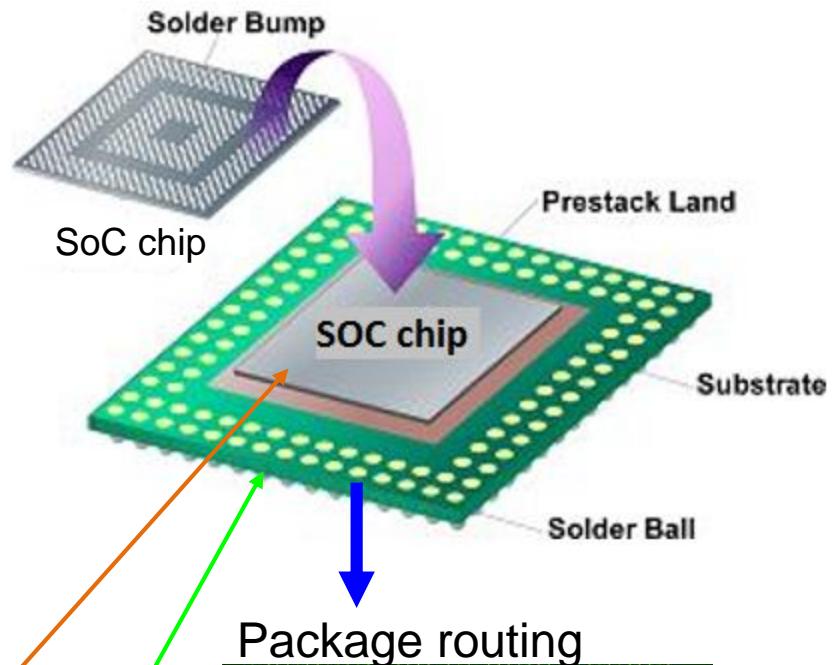
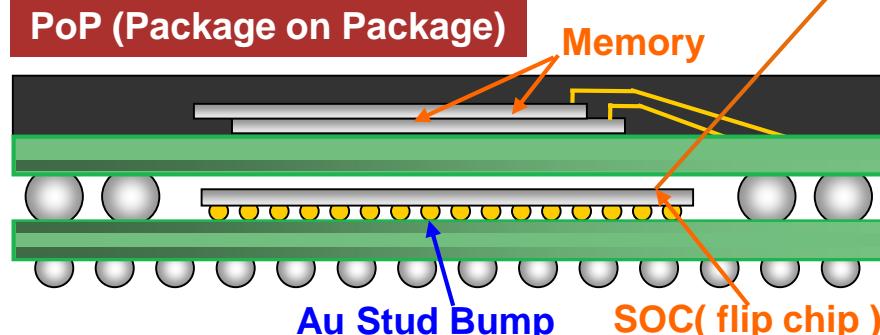
**SiP(System in Package)
WireBonding**



**SiP(System in Package)
Au Stud Bump + WireBonding**



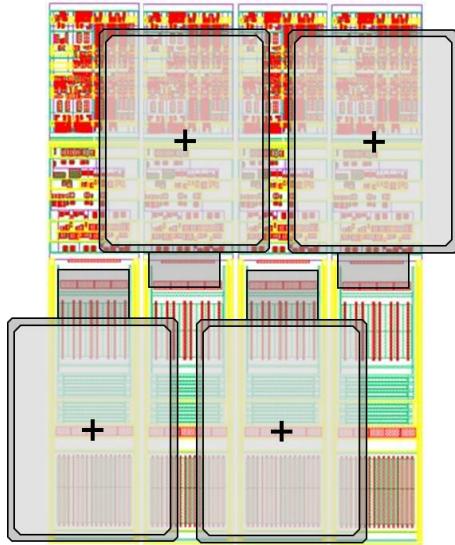
PoP (Package on Package)



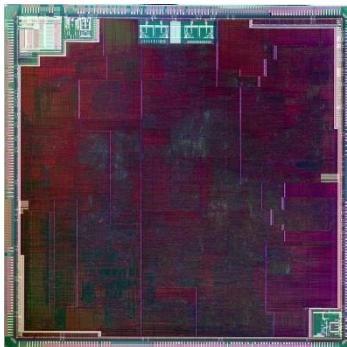
Chip Design Planning

Flipchip PAD design

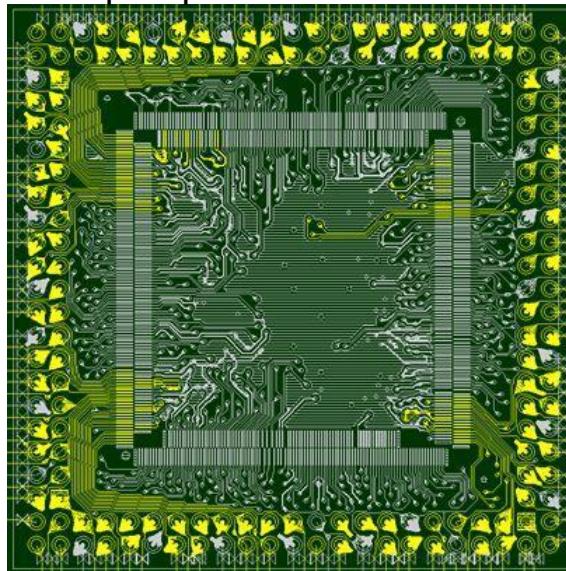
“STAGGER” Pad placement



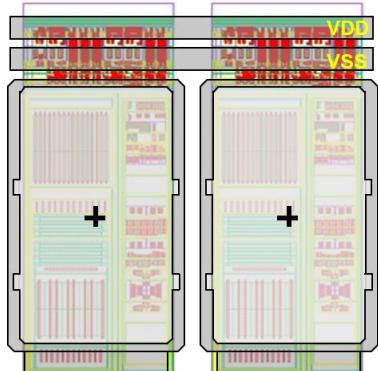
SoC using Stagger PAD



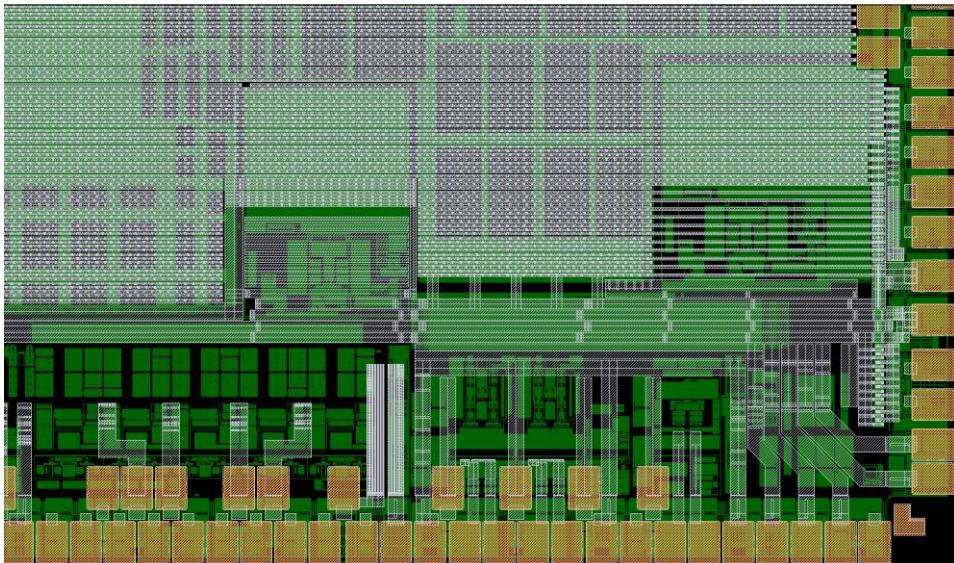
Example of package routing
for FlipChip PAD



“STRAIGHT” Pad placement



(Layout view) PAD arrangement in Chip Layout

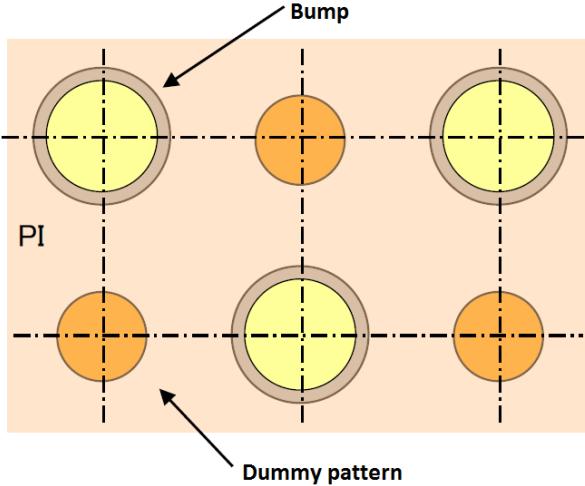


Chip Design Planning

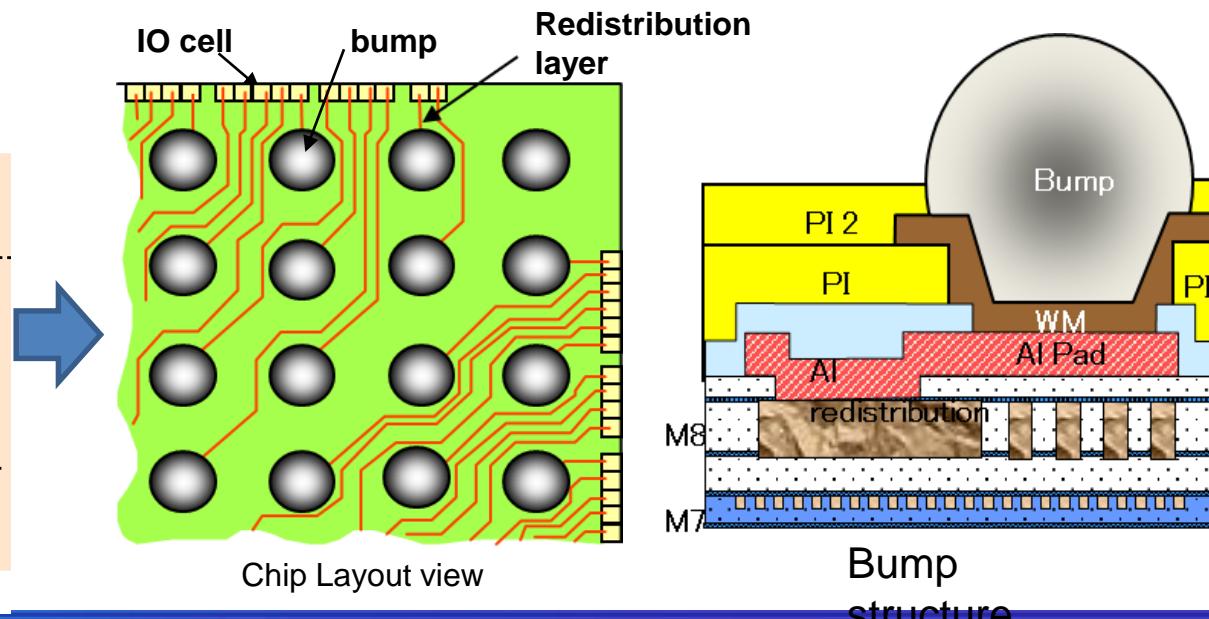
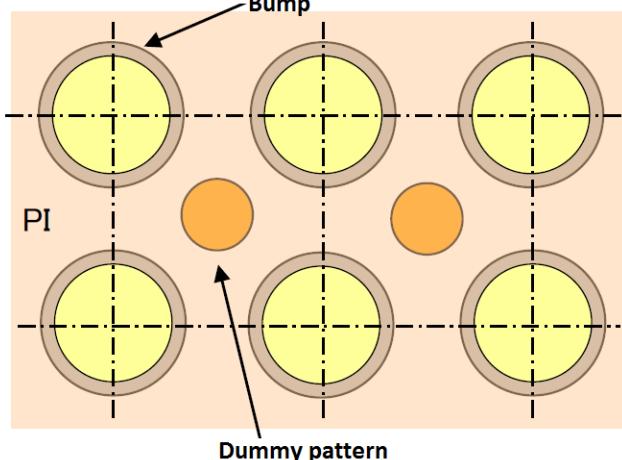
FlipChip BUMP design

Example of Package routing
for FlipChip Bump design

“STAGGER” Bump placement



“STRAIGHT” Bump placement



Chip Design Planning

Chip size and Bump/Pad planning

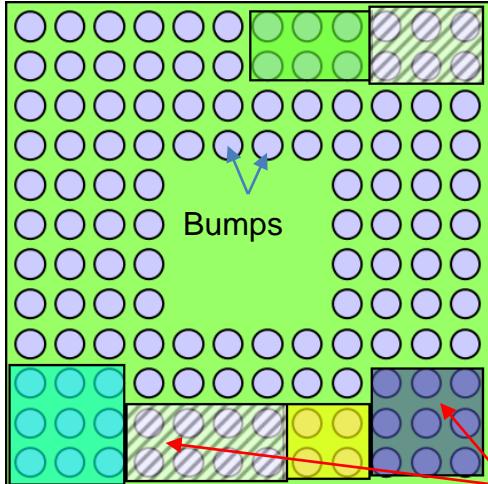
(4)

Block size is estimated to feedback to chip size decision

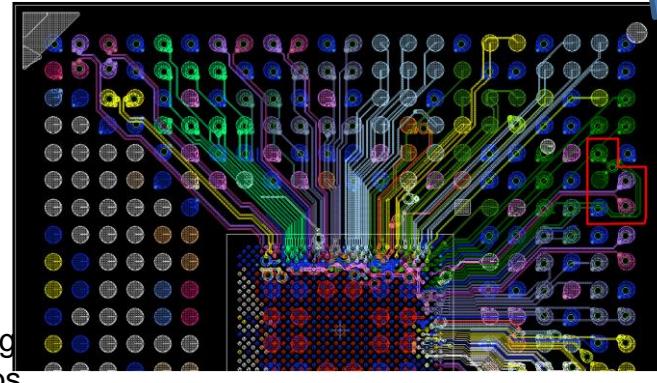


(3)

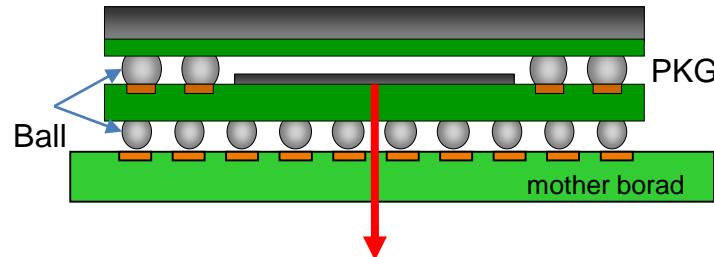
Analog Hard macro is planned.
Bump/Pad is roughly arranged.



(package routing is trialed and feedback to bump/pad arrangement)

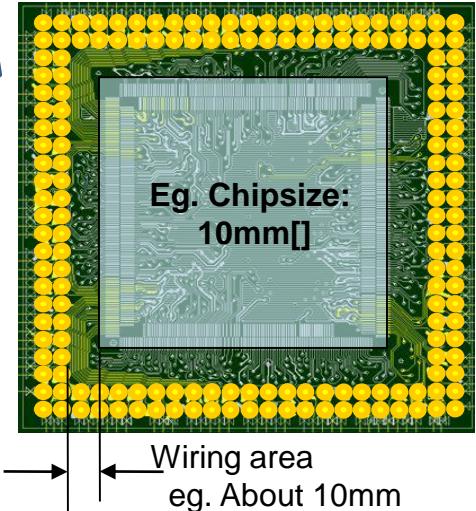


(1) Package type and size is decided



(2)

Chip size is targeted.
Package routing is planned

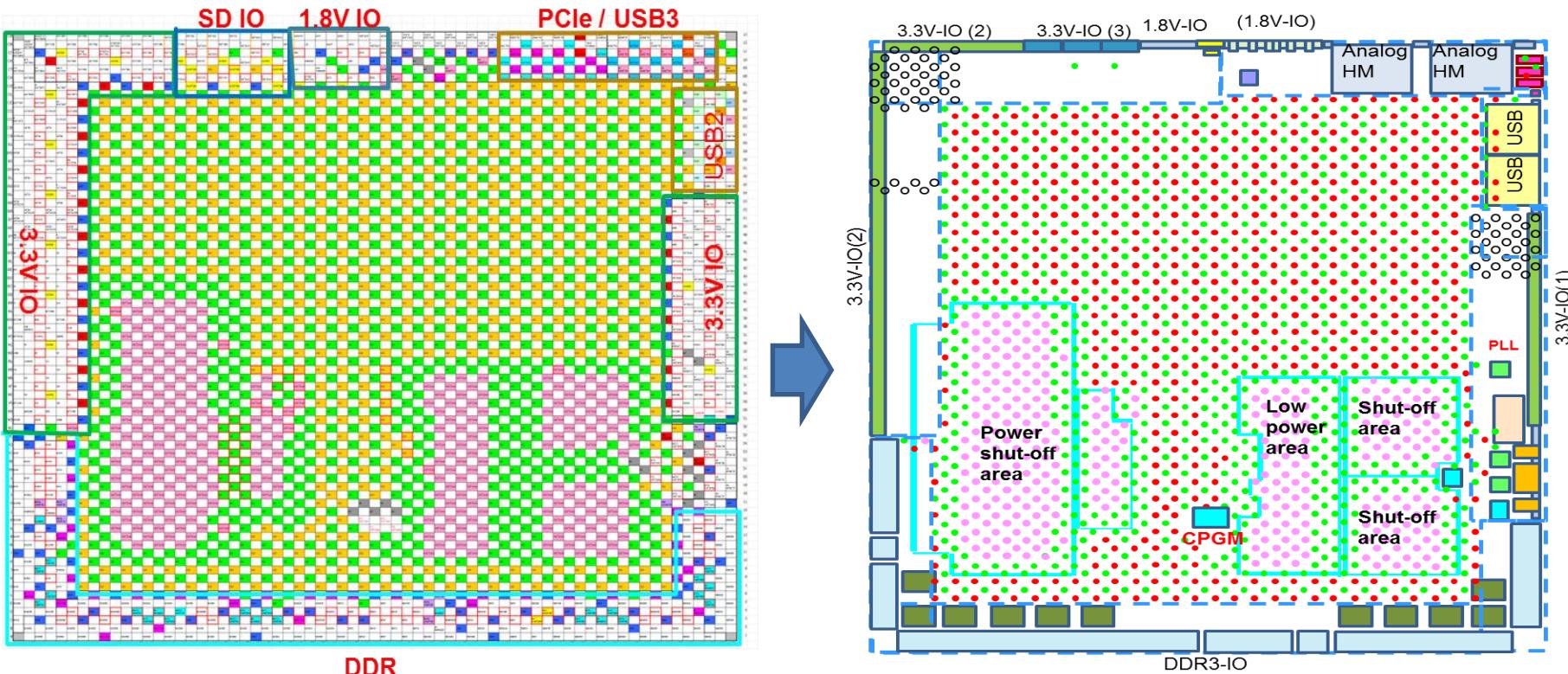


Chip Design Planning

Bump assignment, Block placement, Power arrangement

After chip size is decided and position of Analog macros are planned:

- Make Bump assignment and Block placement
- Arrange Power areas and their position



Chip Design Planning

Early power analysis

Power consumption for each block is estimated.

Rough power analysis (IR drop, power distribution, ...) is executed.

→ Bump assignment may be adjusted

→ Power structure and Power supplying plan are made

- Big voltage drop
- More PG bumps?
 - Block position?
 - PG supply?
 - How to reduce drop?

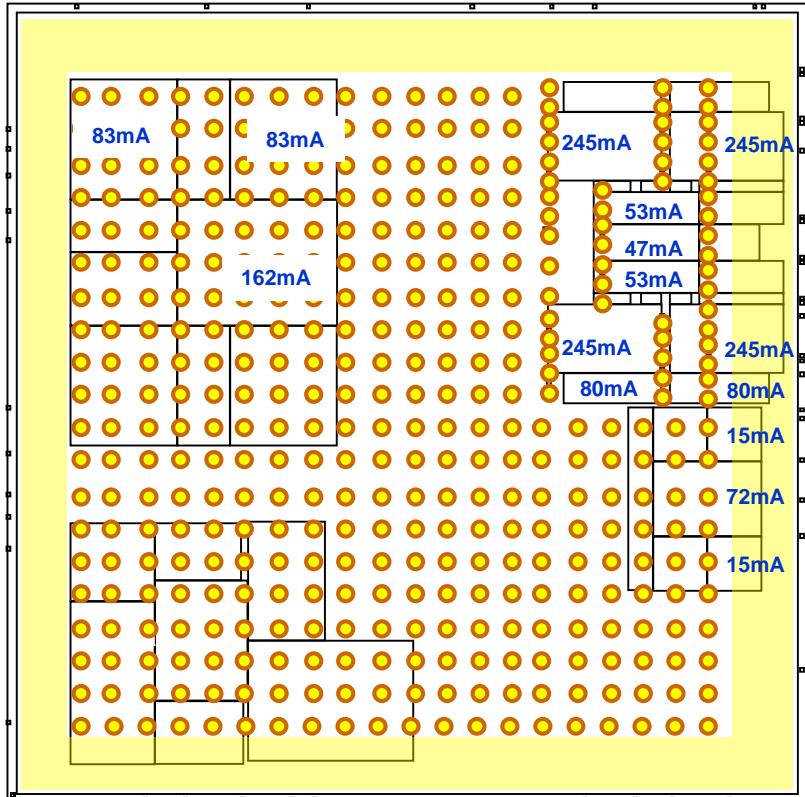


Fig VDD/VSS Core bump Image

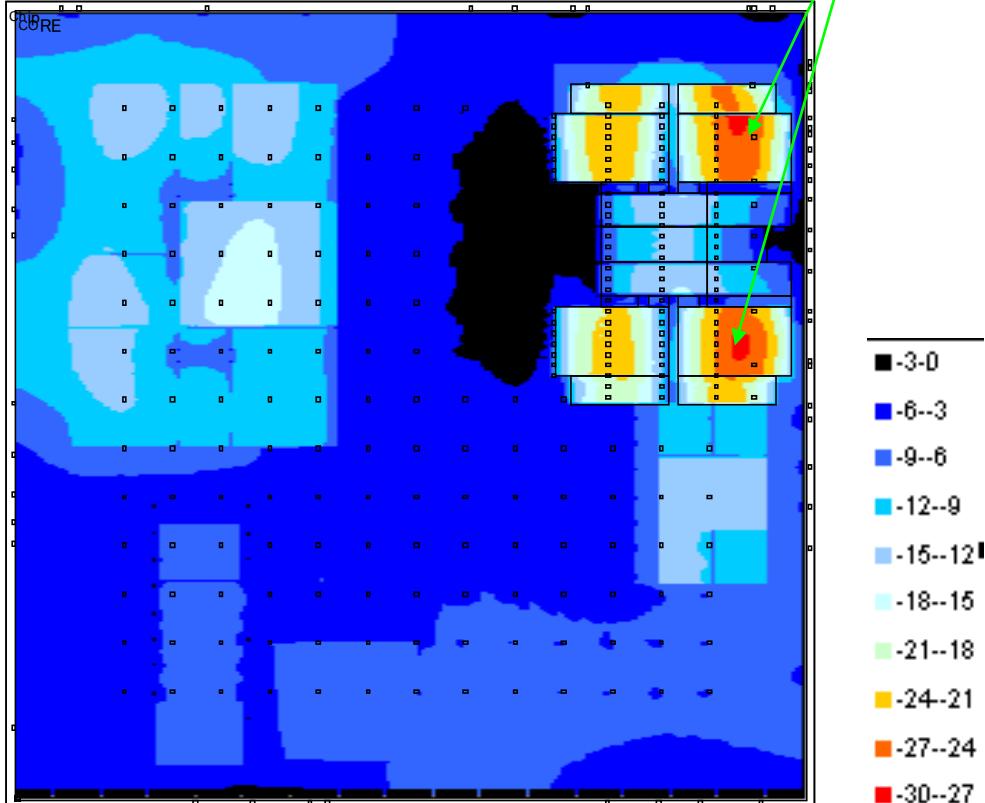


Fig temporary IR-Drop

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Bump/Pad and IO integration

Purpose ?

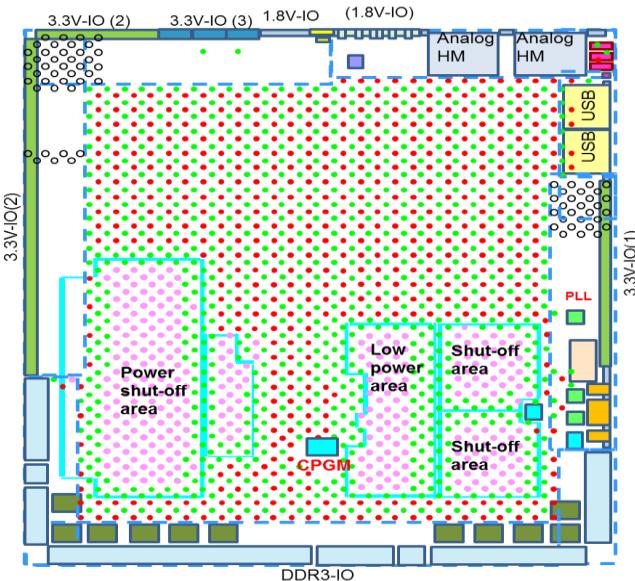
- Detail bump/pad and I/O cells assignment.
- Design ESD protection network and adjust I/O placement
- RDL routing
- Create detail mesh of PG supply (core area, macro area, I/O area)

*ESD: Electrostatic discharge
RDL: Redistribution layer*

Bump/Pad and IO integration

Bump/Pad and I/O cells assignment

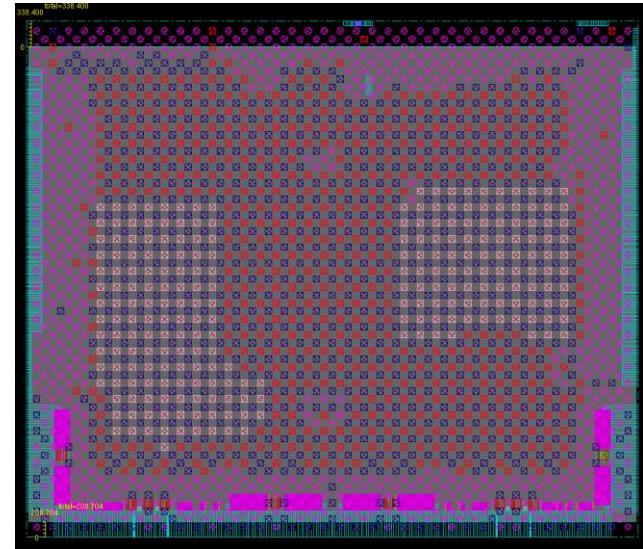
Power area, Analog macros placement (Chip planning)



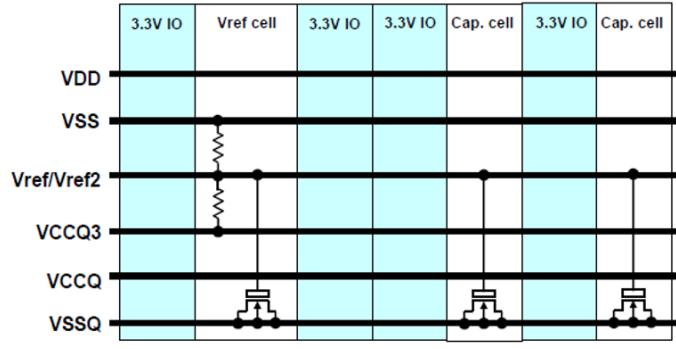
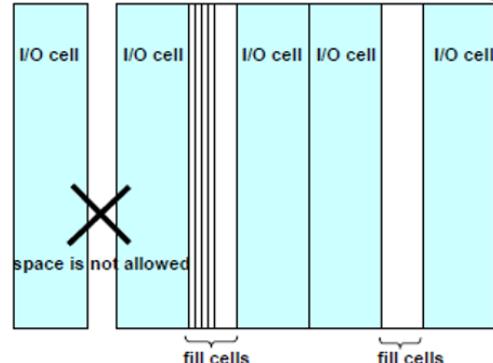
Bumps are assigned for each power area.

I/O cells and Bumps are arranged according to position of Analog macros and peripheral modules

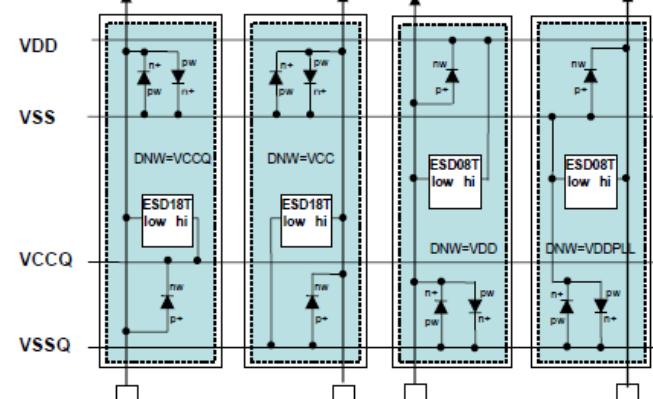
Bumps and I/O cells are arranged



I/O fillers, Vref, and Cap cells are added
(I/O cells include both signal and power cells)



Power I/O cells include ESD protection circuits

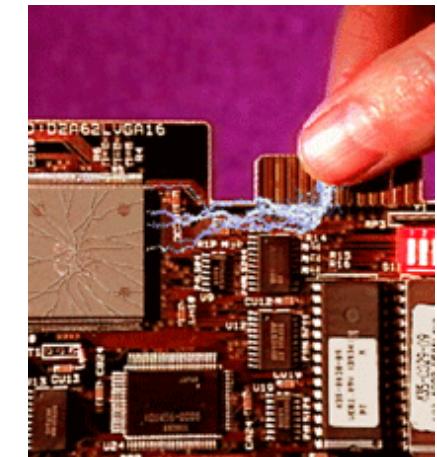


Bump/Pad and IO integration

ESD Protection overview

Electrostatic discharge (ESD) is the transfer of electrostatic charge between two objects of **different potentials** when they come into **contact with each other**.

ESD is one of the main causes of device failures in the semiconductor industry.



- Silicon melting
- Junction breakdown
- Gate oxide breakdown
- Interconnect melting

ESD protection circuit is included in Power I/O cells. The connection from bumps/pads to IO cells needs to be carefully designed to maintain low resistance.

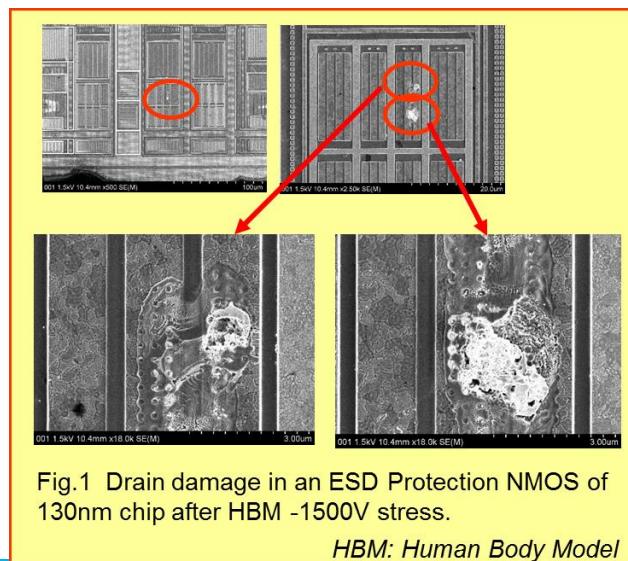
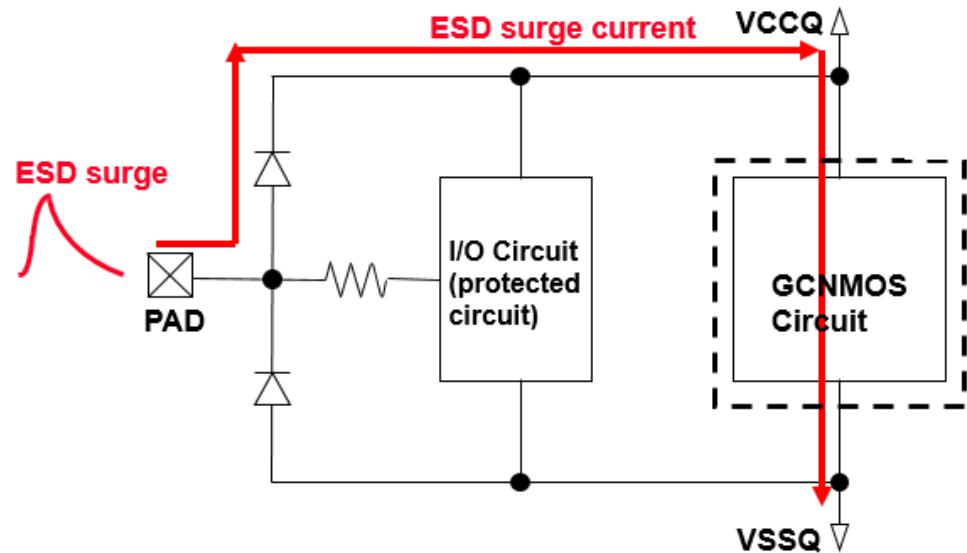


Fig.1 Drain damage in an ESD Protection NMOS of 130nm chip after HBM -1500V stress.

HBM: Human Body Model

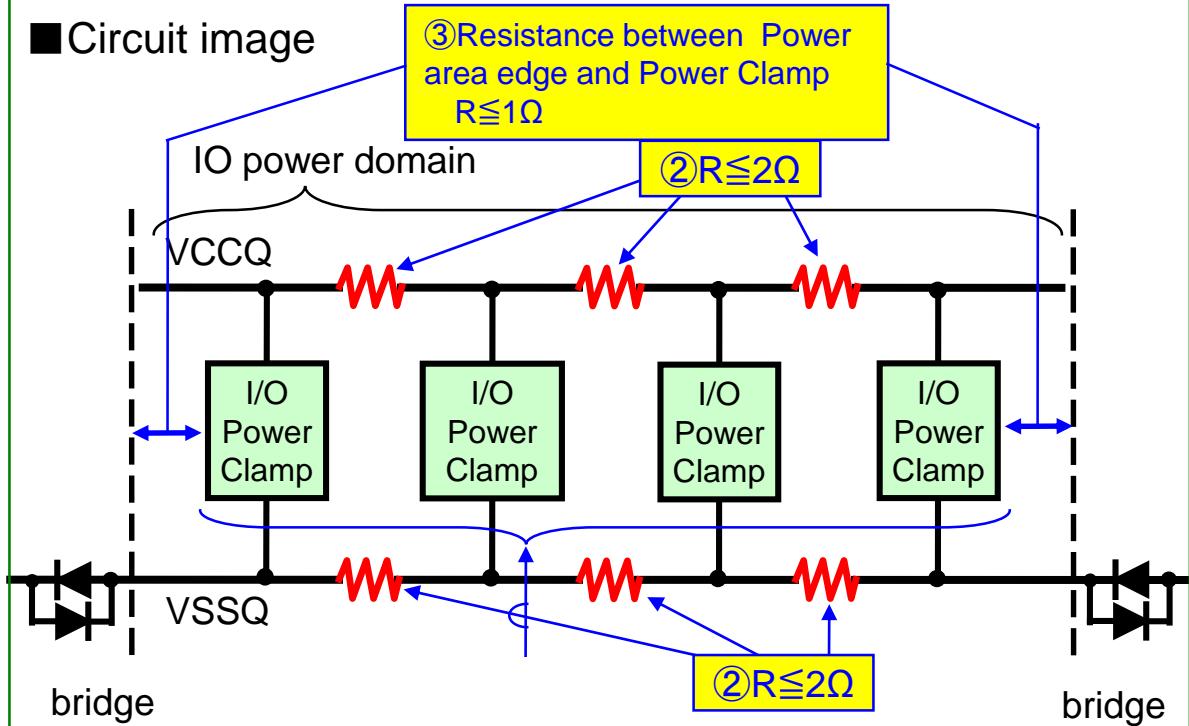


Bump/Pad and IO integration

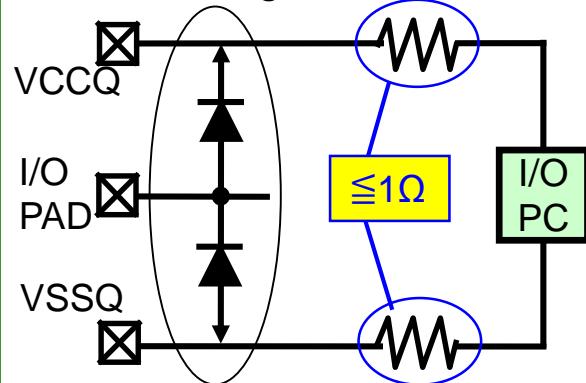
ESD Protection Design

* 28nm ESD constraints for Power I/O cell arrangement

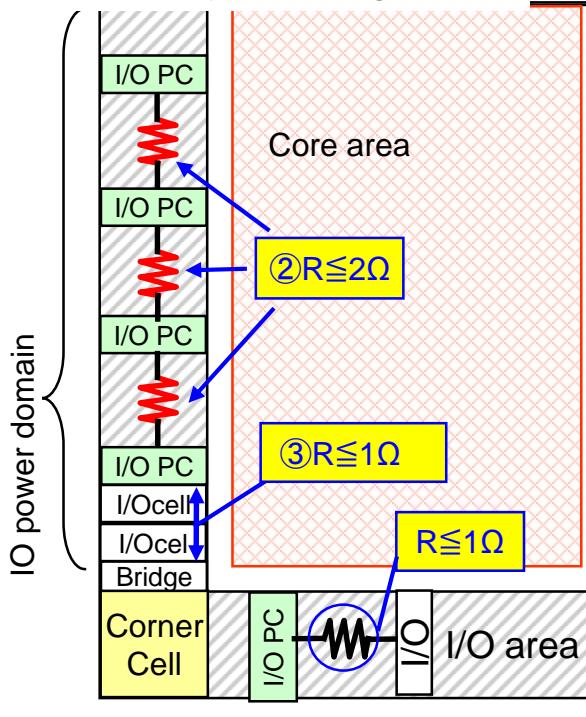
■ Circuit image



■ Circuit image (Signal IO cell)



■ Chip layout image



- ESD protection Circuit consists of Power Clamp and Diode.
- The Power Clamp (PC) is a part of the ESD protection circuit in the Power IO cell.

Bump/Pad and IO integration

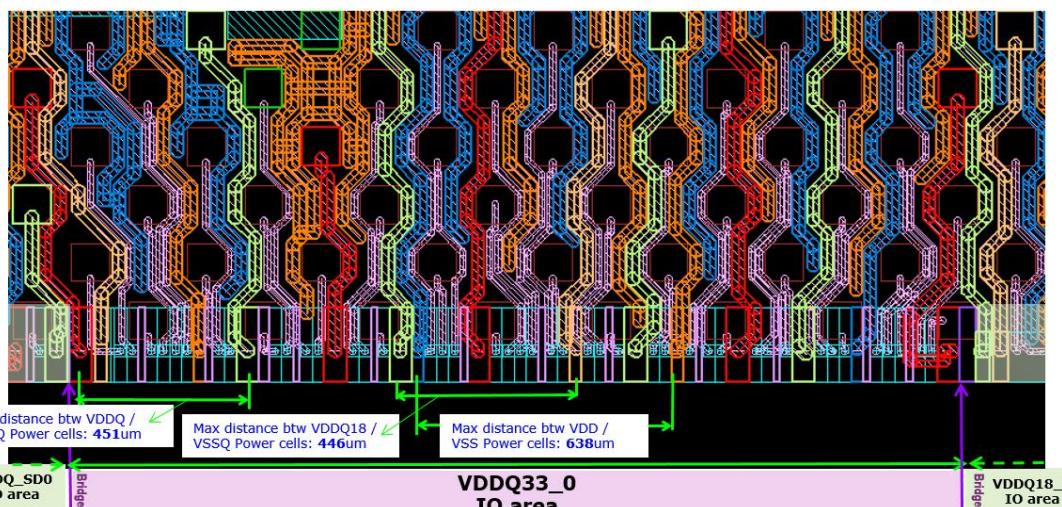
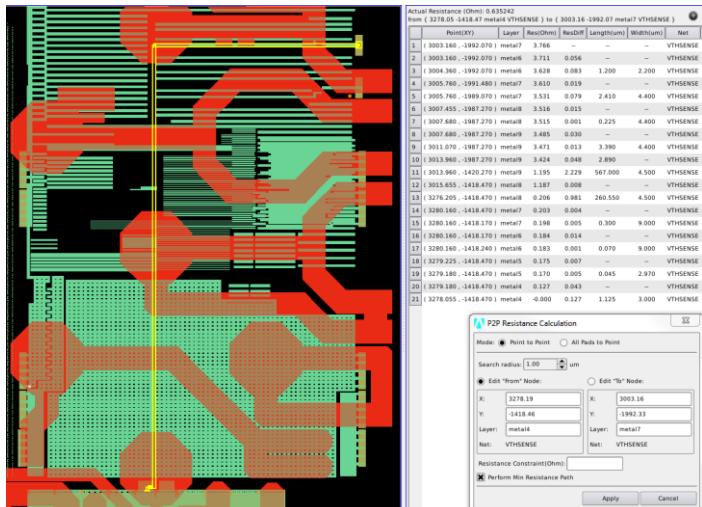
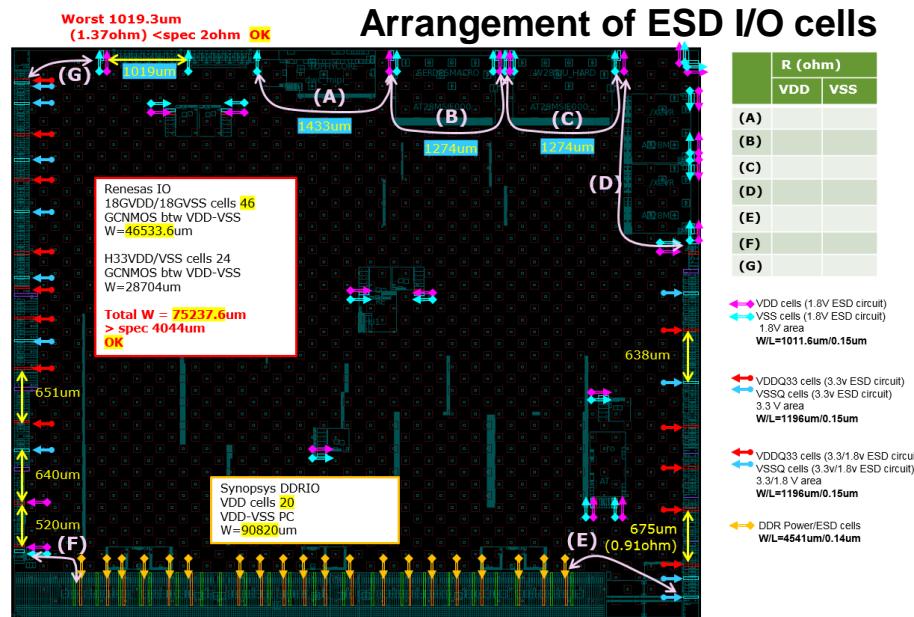
ESD Protection Design

IO cells includes ESD protection circuits.

They are placed around the chip and connected within and between domains for ESD protection. Power domains in IO area are separated by bridge cells.

Connection from Bumps/Pads to ESD cells are routed by Redistribution (RDL) layer to maintain low resistance.

Power/Ground mesh (grid) is enhanced by global routing layers to satisfy resistance target.



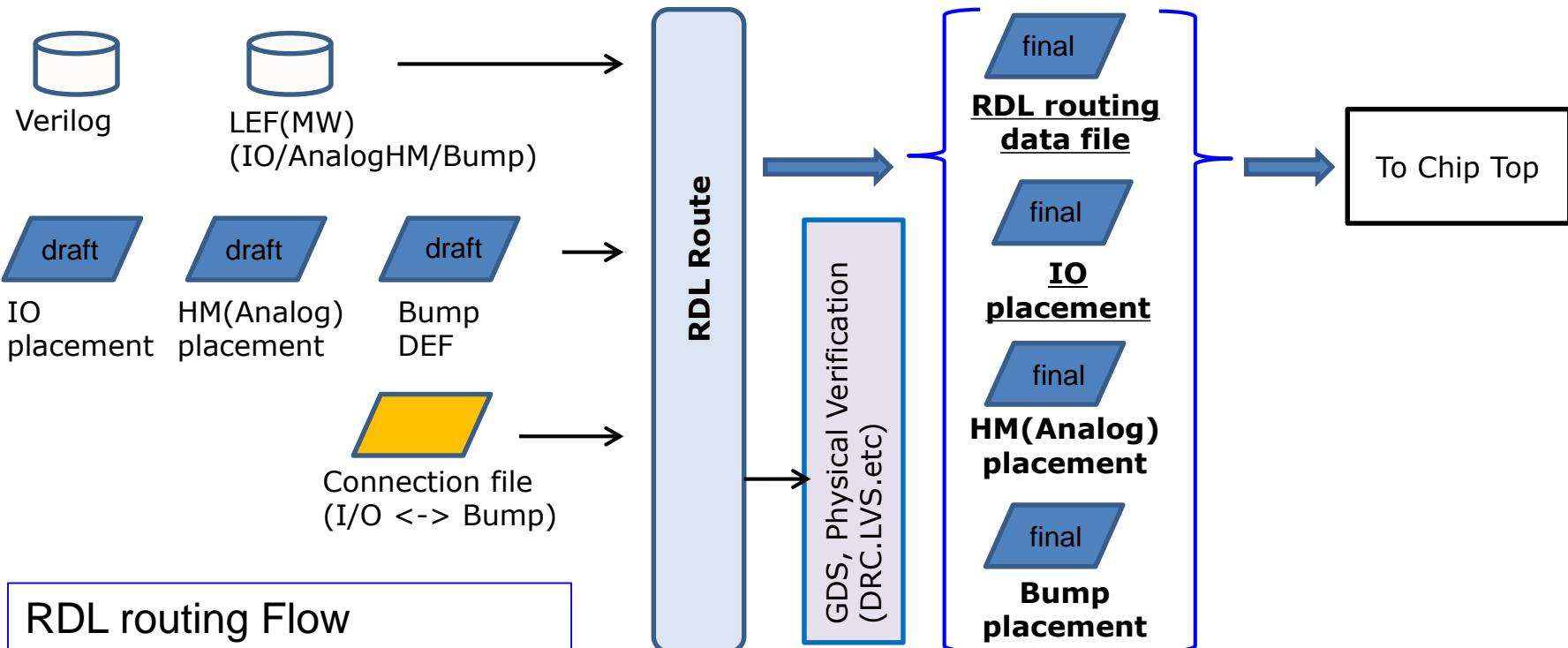
Bump/Pad and IO integration

RDL routing

RDL (Redistribution layer) routing connects :

- Signal Bumps/Pads to signal-IO pads
- PG Bumps/Pads to PG-IO pads (with ESD protection circuits)

RDL is also used to supply power/ground source from bumps/pads to global-metal PG grid (in shut-off areas, Analog macro areas, and other common areas)

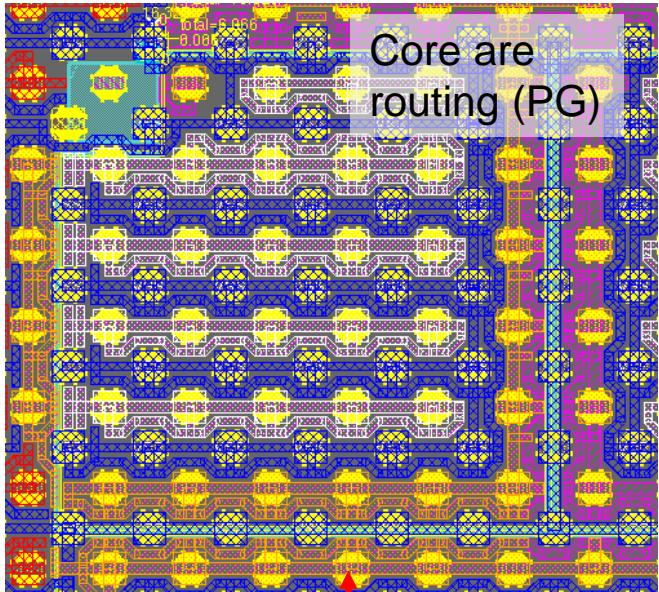
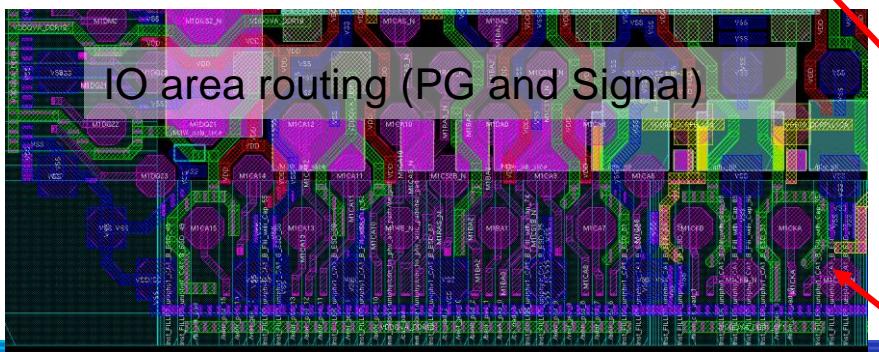
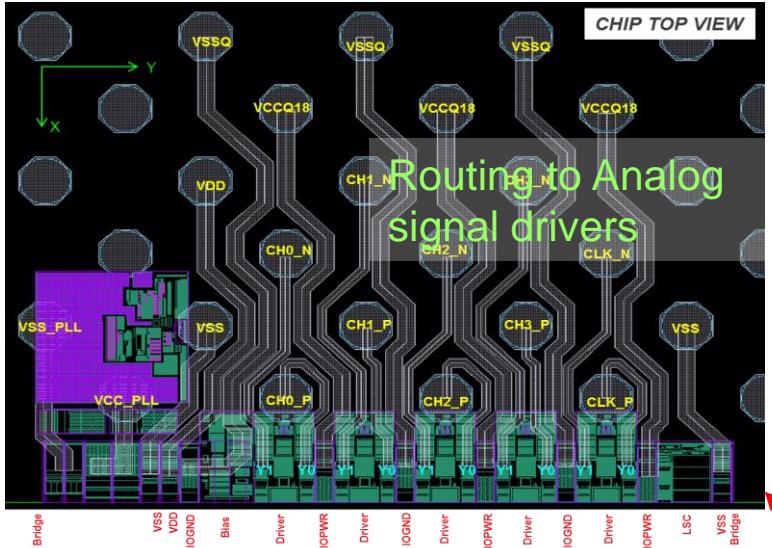


Bump/Pad and IO integration

RDL routing

Routing RDL need to satisfy

- Resistance requirements (for package routing, ESD network design, EM/IRDROP design)
- Special requirements over Analog areas.



Bump/Pad and IO integration

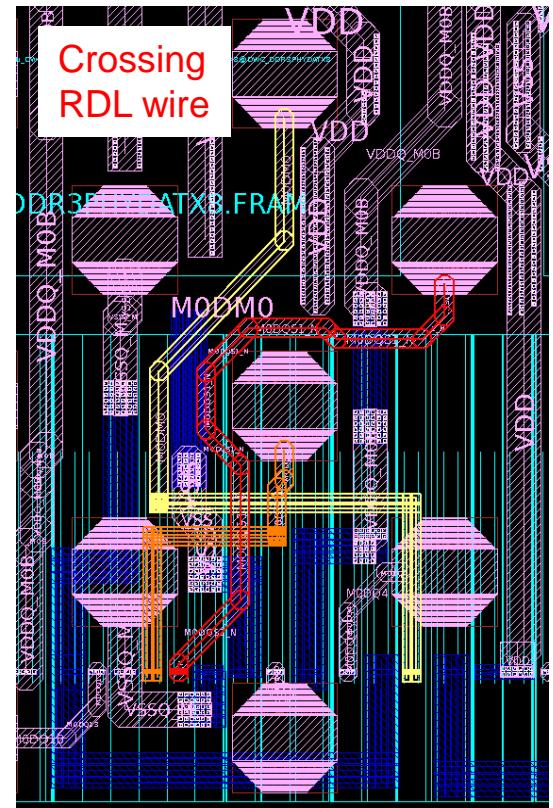
RDL routing

IO and Bump/Pad arrangement may need to change to make routing possible or to reduce cross wiring.

M0BA1	0 B	SNPS_D3F_PDDRIO_NS
VDD	0 B	SNPS_D3F_PVDD_NS
VDD	0 B	SNPS_D3F_PVDD_NS
VSSQ	0 B	SNPS_D3F_PVSSQ
M0A13	0 B	SNPS_D3F_PDDRIO_NS
VSS	0 B	SNPS_D3F_PVSS
VSS	0 B	SNPS_D3F_PVSS
VSSQ	0 B	SNPS_D3F_PVSSQ
M0A6	0 B	SNPS_D3F_PDDRIO_NS
VDDQ_M0A	0 B	SNPS_D3F_PVDDQ
M0A5	0 B	SNPS_D3F_PDDRIO_NS
M0A3	0 B	SNPS_D3F_PDDRIO_NS
M0A10	0 B	SNPS_D3F_PDDRIO_NS
VSSQ	0 B	SNPS_D3F_PVSSQ
M0A11	0 B	SNPS_D3F_PDDRIO_NS
VDDQ_M0A	0 B	SNPS_D3F_PVDDQ
M0CS1#	0 B	SNPS_D3F_PDDRIO_NS
M0A0	0 B	SNPS_D3F_PDDRIO_NS
VSSQ	0 B	SNPS_D3F_PVSSQ
M0A9	0 B	SNPS_D3F_PDDRIO_NS
VDDQ_M0A	0 B	SNPS_D3F_PVDDQ
VSSQ	0 B	SNPS_D3F_PVSSQ
MOCK0#	0 B	SNPS_D3F_PDDRIO_NS
MOCK0	0 B	SNPS_D3F_PDDRIO_NS
VSSQ	0 B	SNPS_D3F_PVSSQ

**differential
Signal pair
Arrangement.**

I/O assignment table



Current Situation

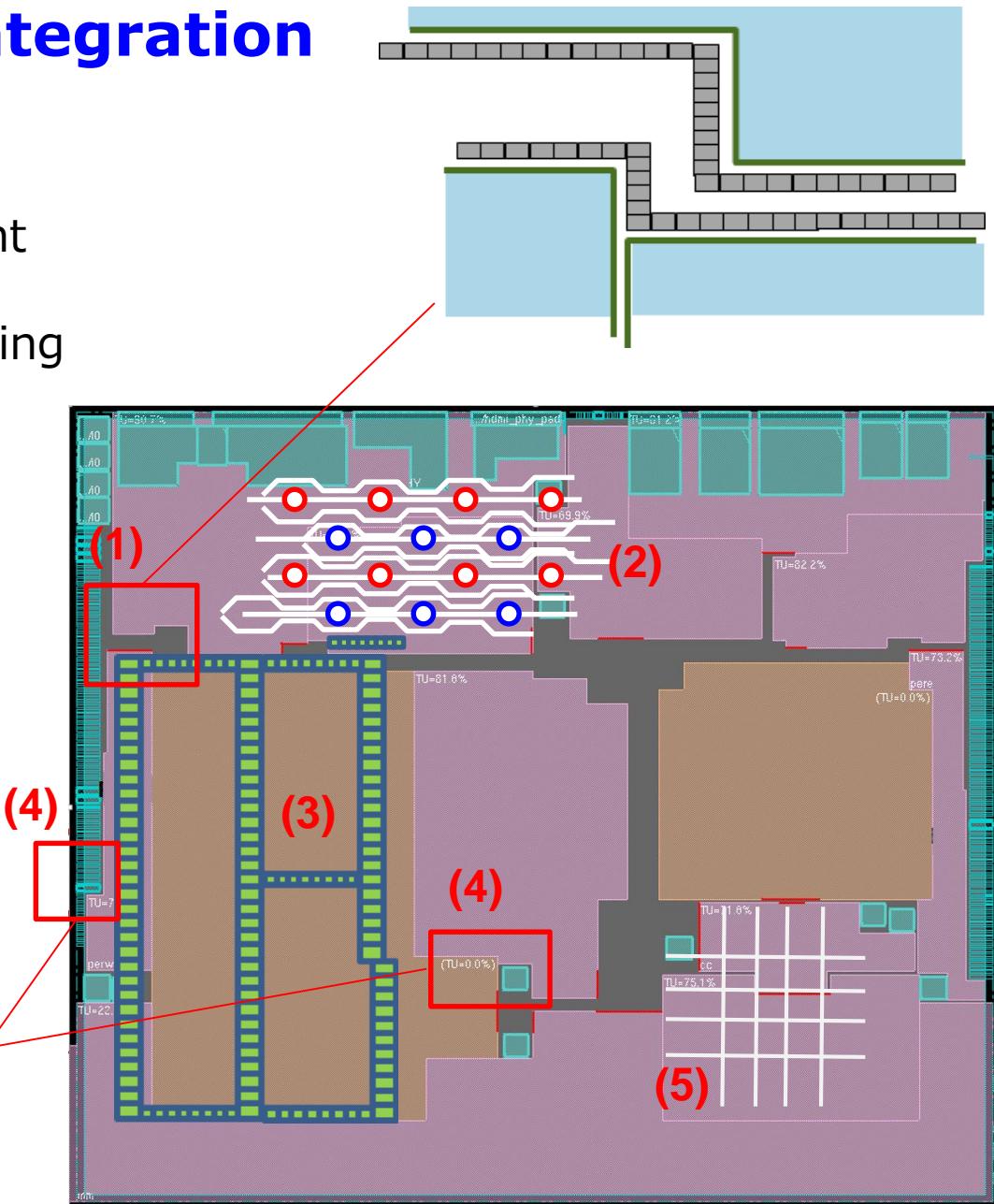
Example of
Changing
better



Bump/Pad and IO integration

Power Rail design

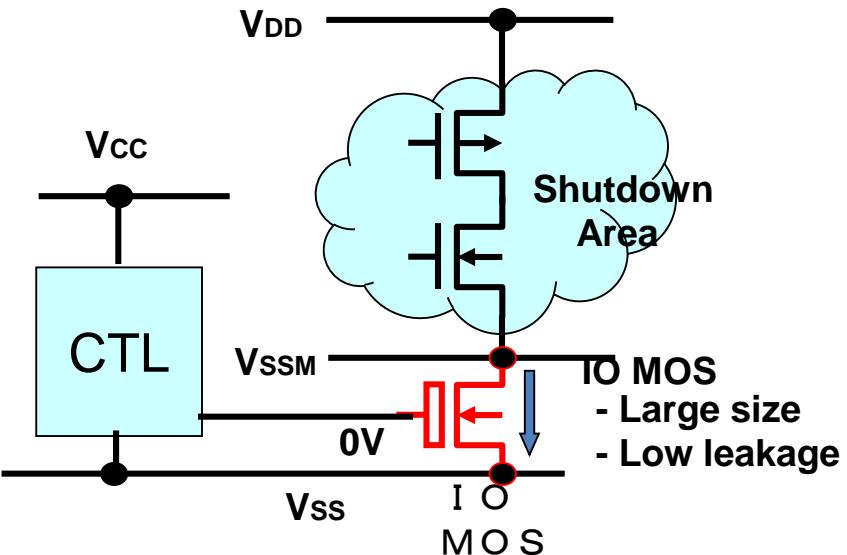
- (1) ENDCAP/WELLTAP placement
(Floor plan)
- (2) BUMP Assign & AP-RDL routing
- (3) Power switch placement
- (4) IO/Analog HM pg routing
- (5) Power/Ground grid routing



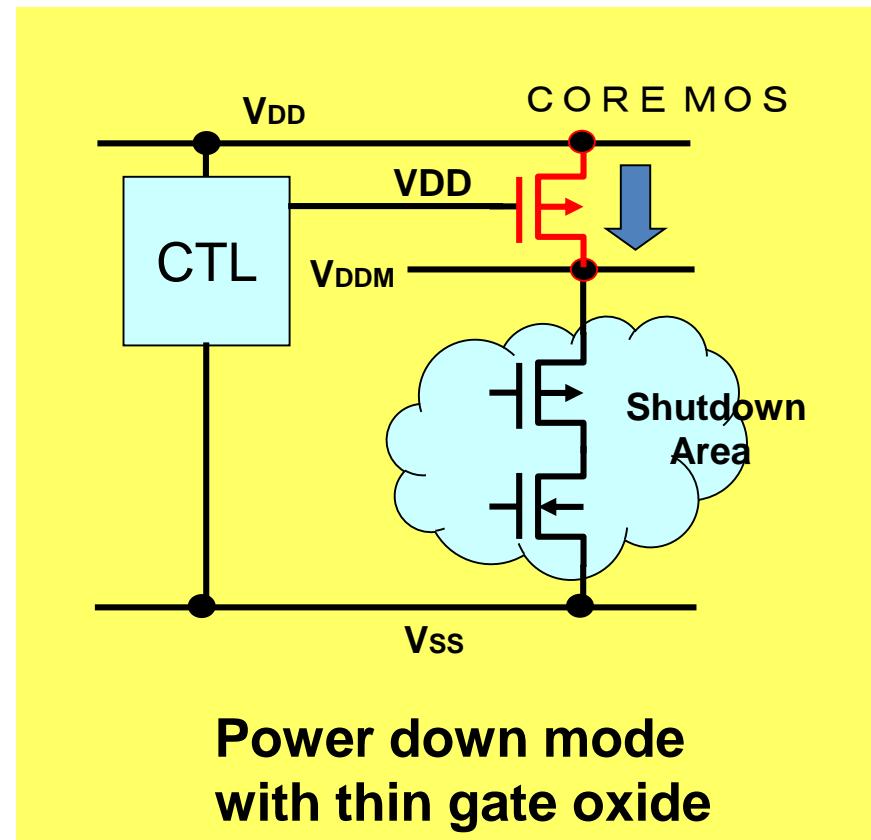
Bump/Pad and IO integration

Power Rail design: Power switch placement

Power switch cells are used to shut-off power supply to a specific block as a method to reduce power consumption, or to separate power supplies between different power domain in a design.



**Power down mode
with thick gate oxide**



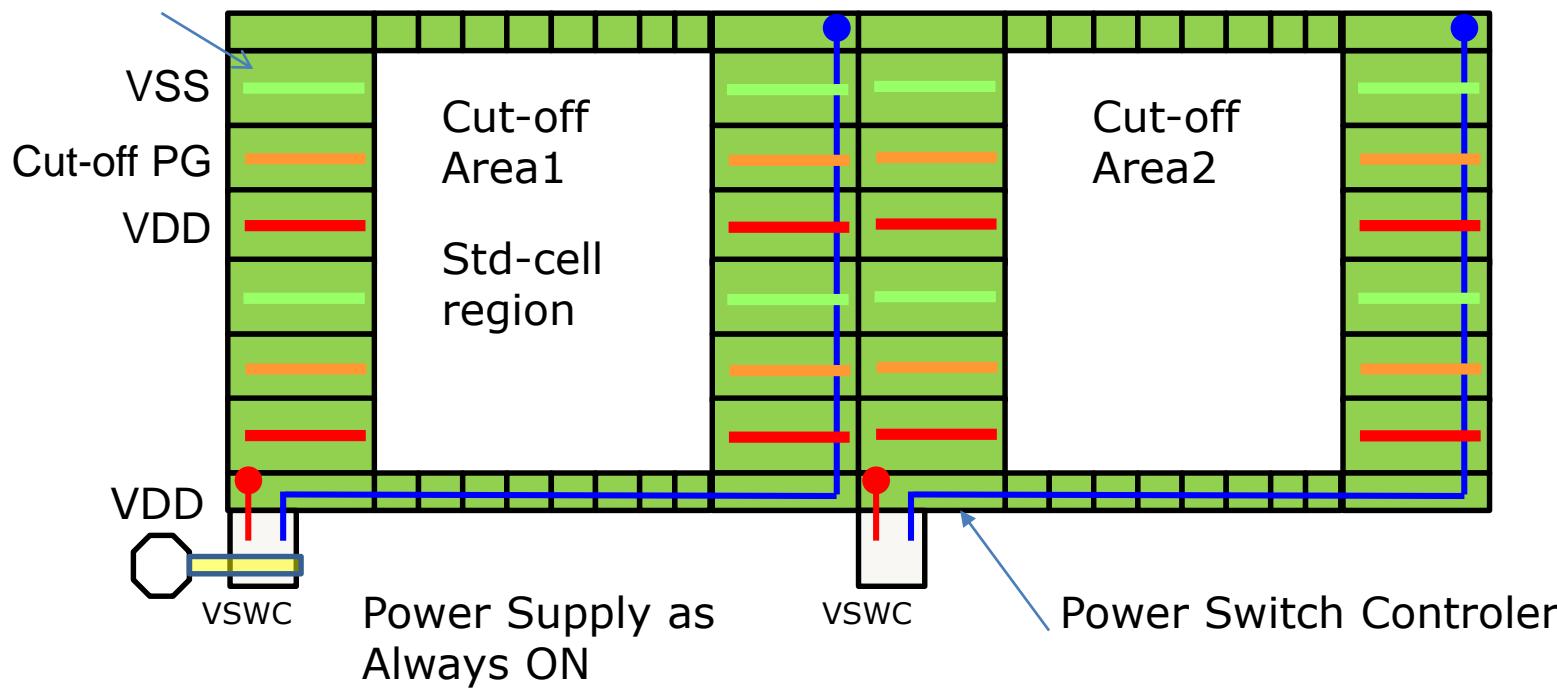
**Power down mode
with thin gate oxide**

Bump/Pad and IO integration

Power Rail design: Power switch placement

Power switch (PSW) cells are put to form a ring around cut-off area and are controlled by PSW controller (VSWC) cells
VSWC cells has only VDD/VSS.
Thus, it should be located adjacent to the ring of PSWs.

Power Switch

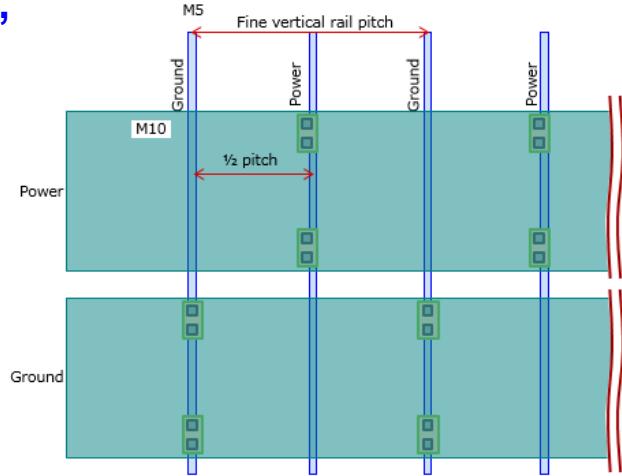
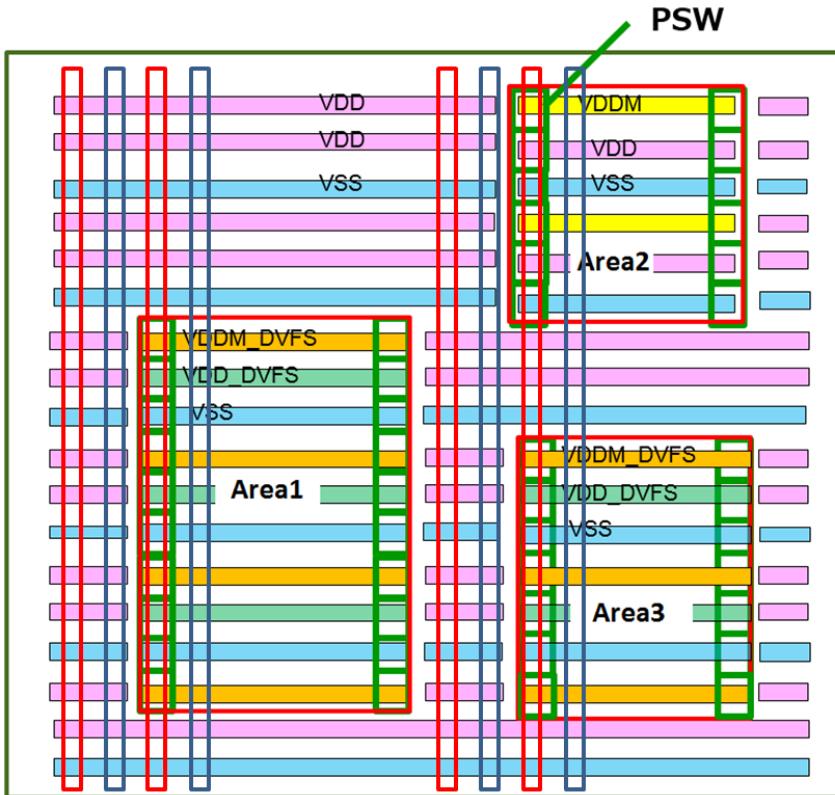


Bump/Pad and IO integration

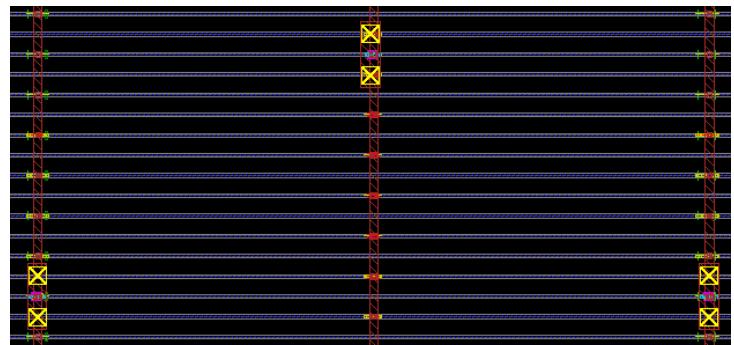
Power Rail design: PG grid routing

Global routing layers are used. Eg, **M10-VIA10-M11** in T16 2XA1XD3XE2Y2R process. This global PG grid connects power and ground source from RDL mesh to lower fine-metal grid (eg. **M1-VIA1~4-M5-VIA5~9**)

PG grid design must satisfy EM/IRDROP requirements, as well as saving routing resource.



M1-Via1~4-M5 fine grid

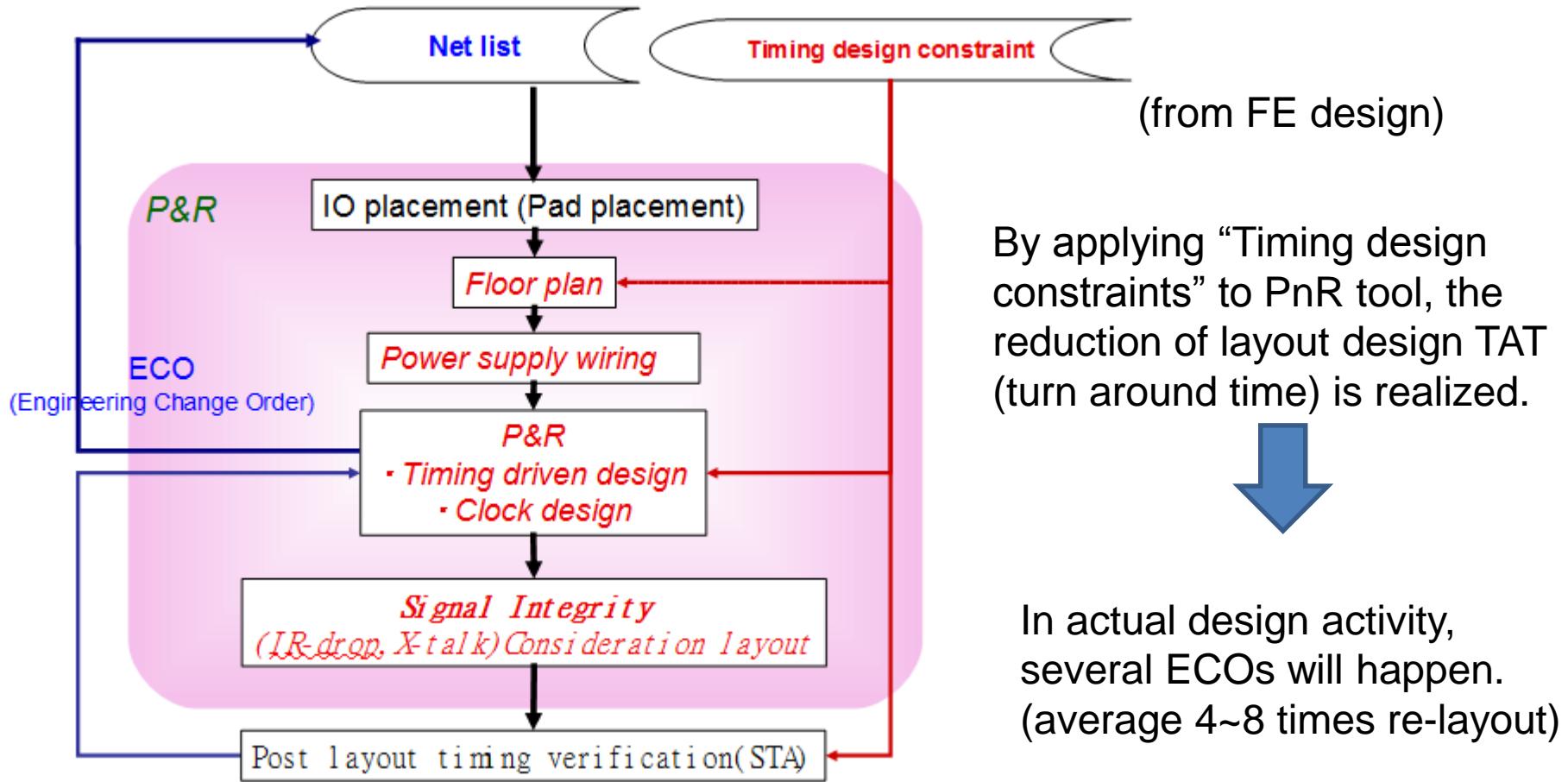


Content

1. Overview of Chip Layout Design
2. Cell and Library
3. Understand about Layout Design
4. Chip design planning
5. Bump/Pad and IO integration
6. **Block and Top level layout design (PnR)**
7. Post-Layout verification

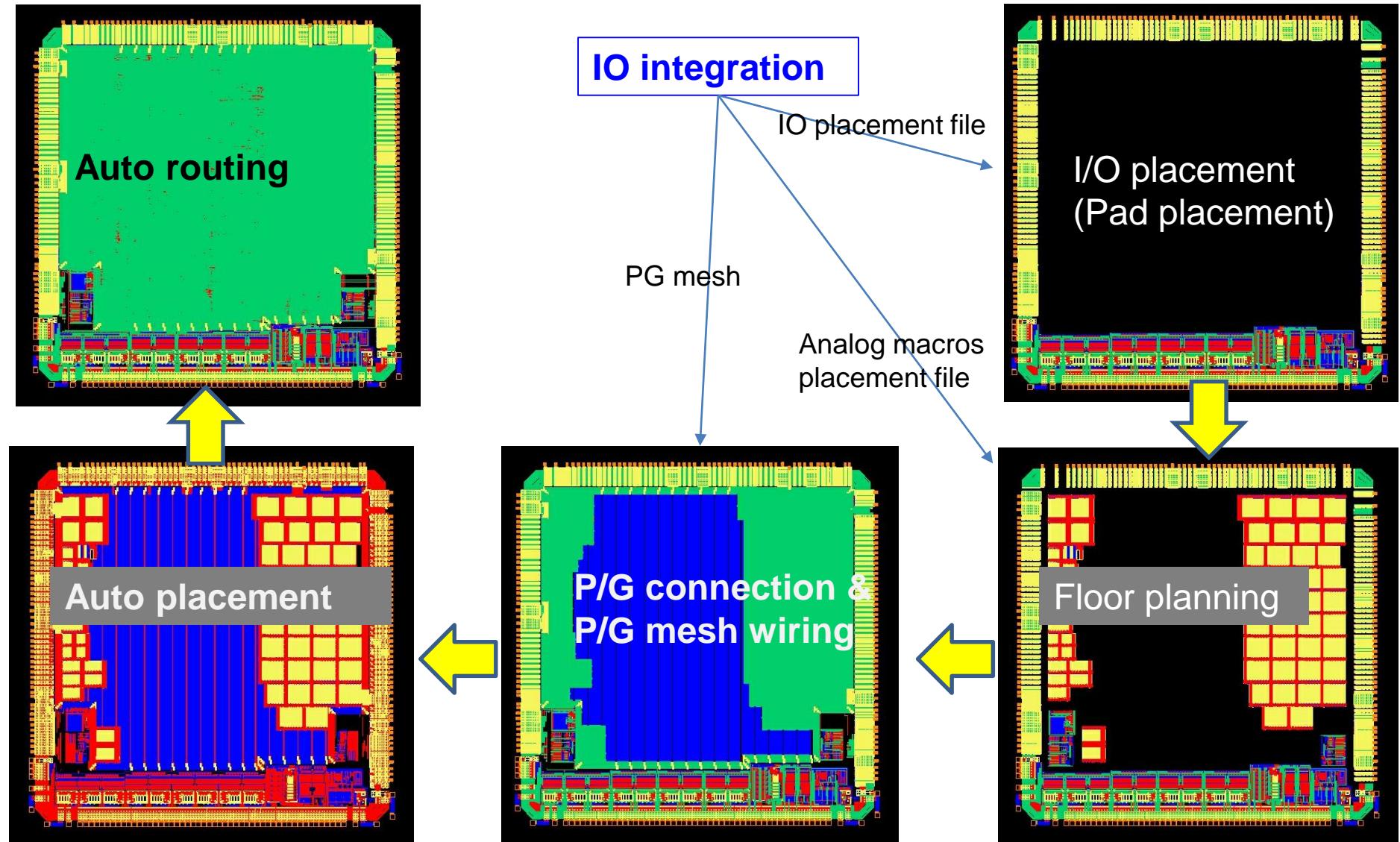
Block and TOP layout design (PnR)

PnR general flow



Block and TOP layout design (PnR)

PnR general flow



Block and TOP layout design (PnR)

PnR general flow

In case of Hierarchical PnR design:

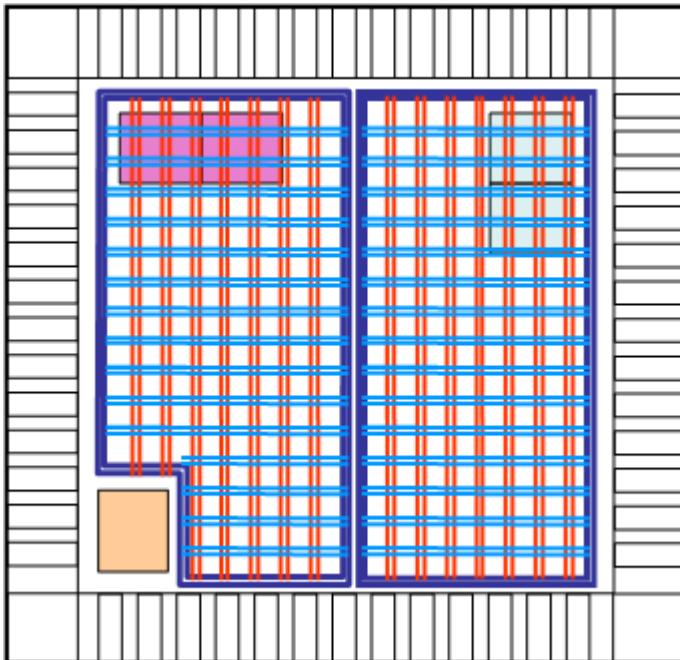
- Chip TOP Floor Planning: decide size (area) and shape for each child block
- Each block is applied the whole design cycle (FP → place → route → timing and signal integrity check)
- **Block interface model** is made for each block. Block size and shape is updated to/from TOP design.
- TOP design will use **block interface model** for its design cycle (FP → Place → Route → Timing and Signal integrity check)



Block and TOP layout design (PnR)

Power supply design

“Power supply design” targets to establish power routing to keep the specifications of design rule, IR-Drop, EM, etc and to supply sufficient current to each cell, considering to minimize the chip size.



<Design approach>

1) Manual design

The designer decides number of wire straps and their width, then uses layout editor and the P&R tool to draw PG mesh manually.

2) Semi-automatic design

Use Angel@Ring (Renesas in-house tool) and pre-determined power routing cells.

3) Automatic power design tool

Developed and implemented to EDA tools
EDA tools will decide PG mesh pattern, number of wire straps, metal width, ... and do the PG routing automatically

Block and TOP layout design (PnR)

Power supply design

In addition, each product needs special care depending on its layout.

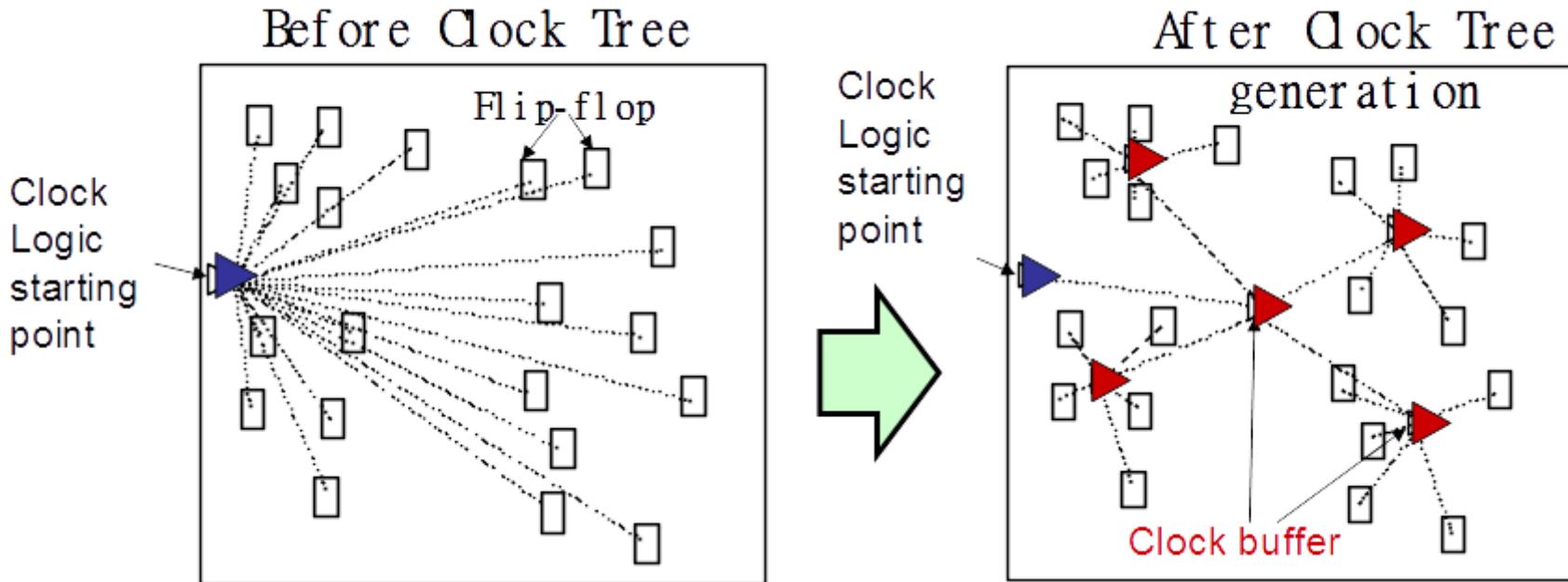
Product usage	Design issues	Power supply design approach
Low power consumption product	- Cell optimization and clock generation in consideration of power consumption reduction.	- Use low-voltage operating cells - Use high Vth (low leak, low speed) cell libraries. - Power-consumption awareness in synthesis phase (clock gating, logic optimization, ...)
Low standby current product	- Systematic power reduction by controlling power supply	- Separate power supply for each block, and control ON/OFF of each domain.
General purpose product	- Modeling power supply trunk to reduce TAT and IR-Drop/EM estimation.	- Select suitable PG supply model to guarantees IR-Drop/EM - Automatic power layout
High speed product	- Strong power supply trunk to support big power consumption	- Apply Bump instead of Pad - Ensure dedicated layers for PG - Consider placement of high speed block for easy PG supply.

Block and TOP layout design (PnR)

Clock design

In the clock design, it is necessary to reduce Skew of the clock.

→**Clock skew** is adjusted by inserting clock dedicated buffers and by dividing net into **tree structure** ([clock tree design](#)).



What is **Clock Skew**:

Maximum value minus minimum value of the delay from starting point of clock to ports of each FF/latch.

Block and TOP layout design (PnR)

Clock design

The excellent clock design means:

Skew of the clock is small.

→ For the operation guarantee of a synchronous circuit

The number of the clock buffer is few.

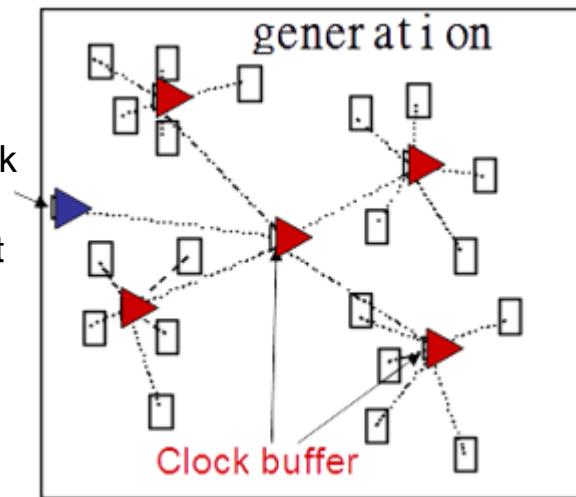
→For the reduction of gate counts and reduction of power consumption

The maximum delay value of the clock path is small.

→For the reduction of dispersion within a wafer and within a chip.

The delay value of the clock path is close to a specified value.

→To adjust delays of different phase between different clocks.



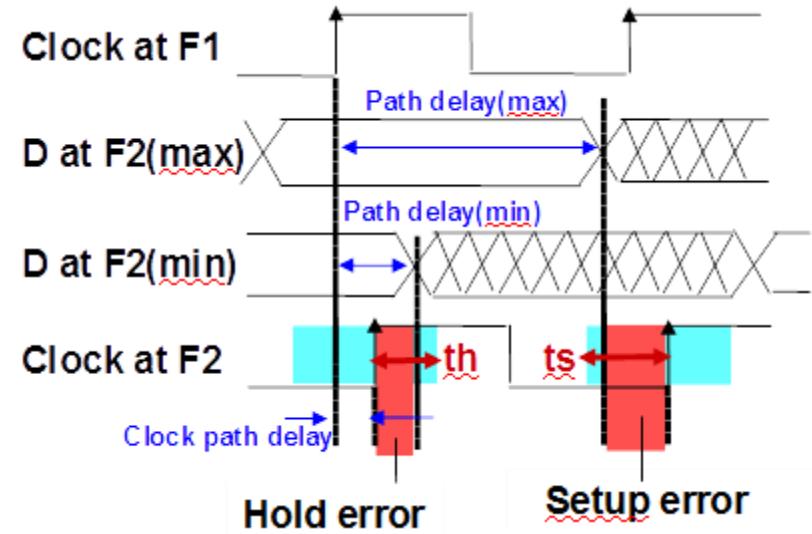
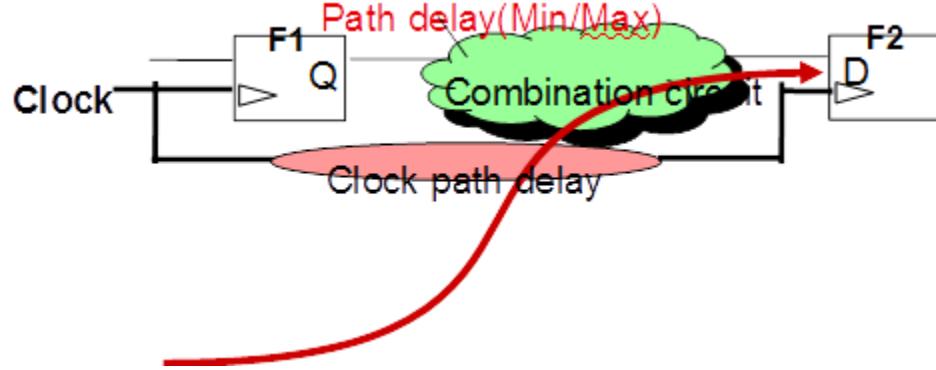
Block and TOP layout design (PnR)

Timing-driven design

- ◆ Timing driven design means that Automatic P&R tool designs layout considering **timing constraints specified at logic design**.
- ◆ **Timing constraint** means that timing (path delay value, setup time, hold time) between clock port and data port of flip-flop.

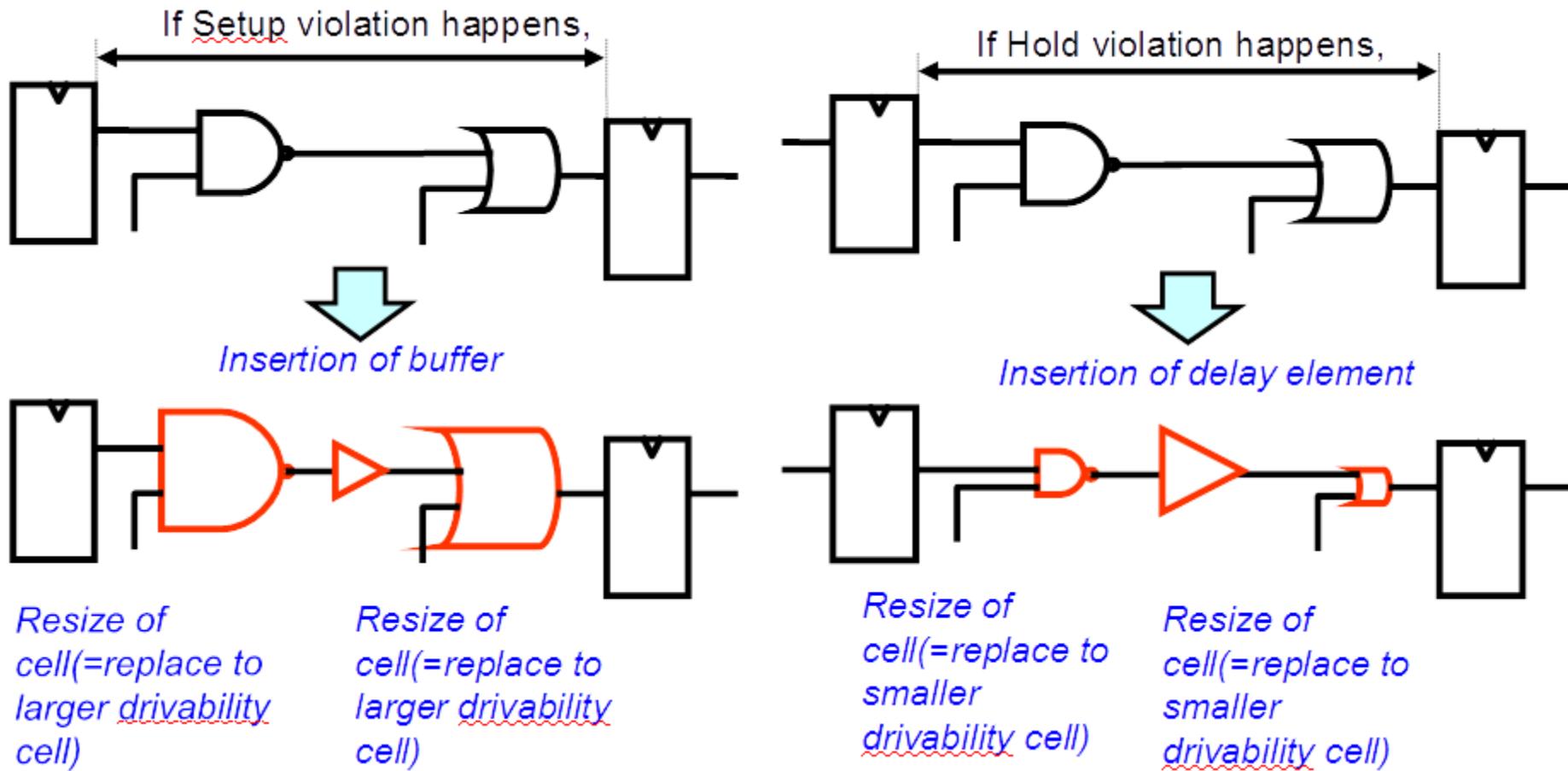
Constraint of Setup time: Data should reach by (the reach time of clock- ts)

Constraint of Hold time: Data should not change by (the reach time of clock + th)



Block and TOP layout design (PnR)

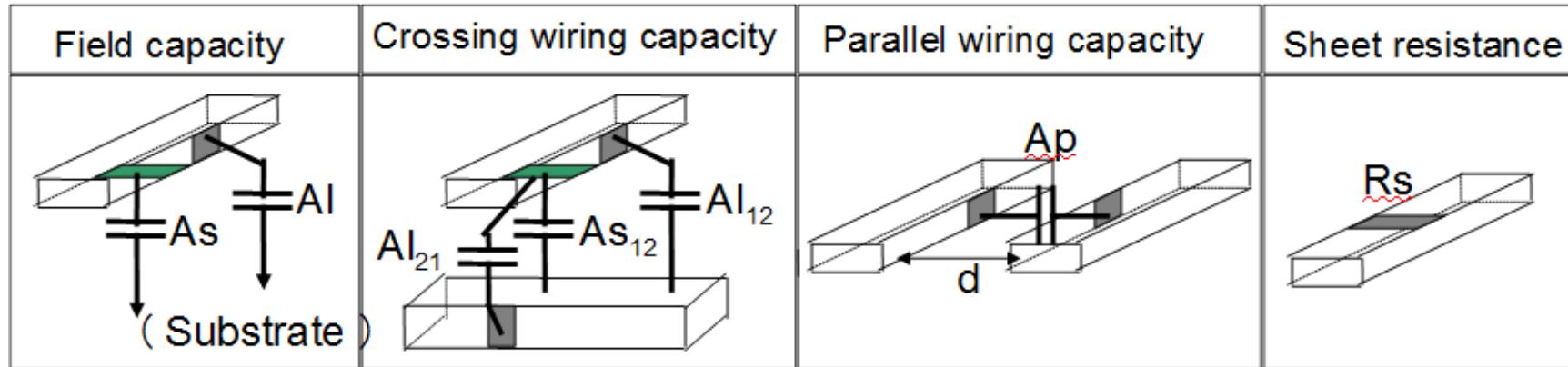
Example of Timing optimization



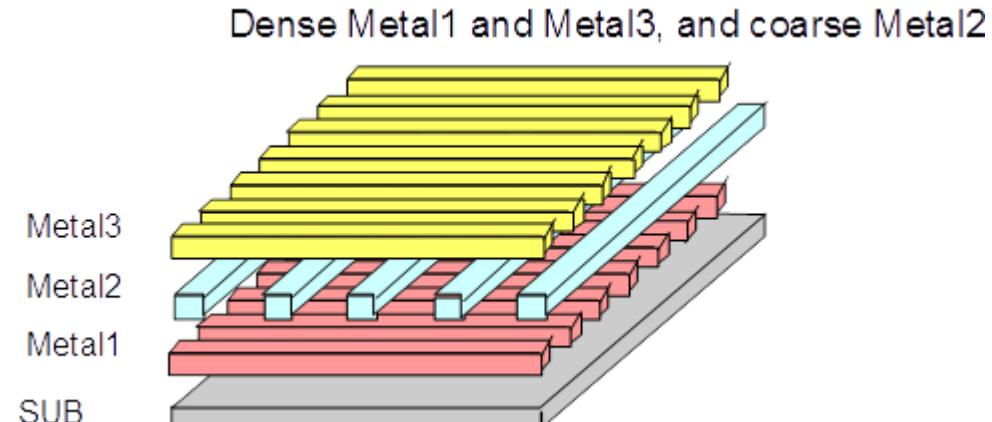
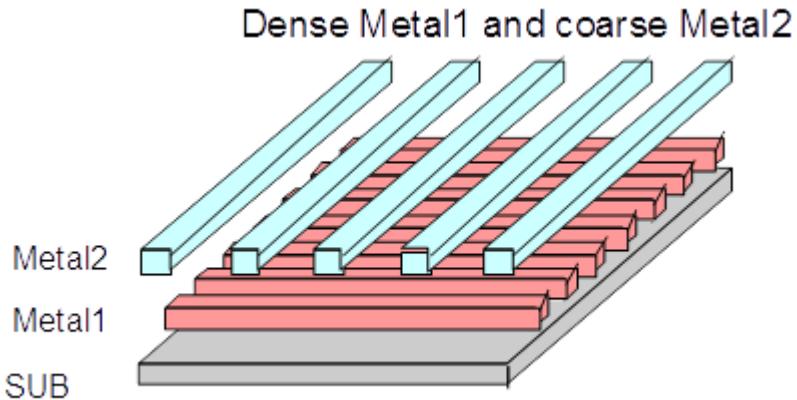
Block and TOP layout design (PnR)

Layout extraction for Signal integrity and Timing check

- ◆ **RC extraction** means that the extraction of wiring loads (stray capacitance and resistance) from layout after P&R.



The parasitic capacitance changes depending on peripheral wiring (with/ without adjacent wire, top and bottom, coarse or dense).



Block and TOP layout design (PnR)

Layout extraction for Signal integrity and Timing check

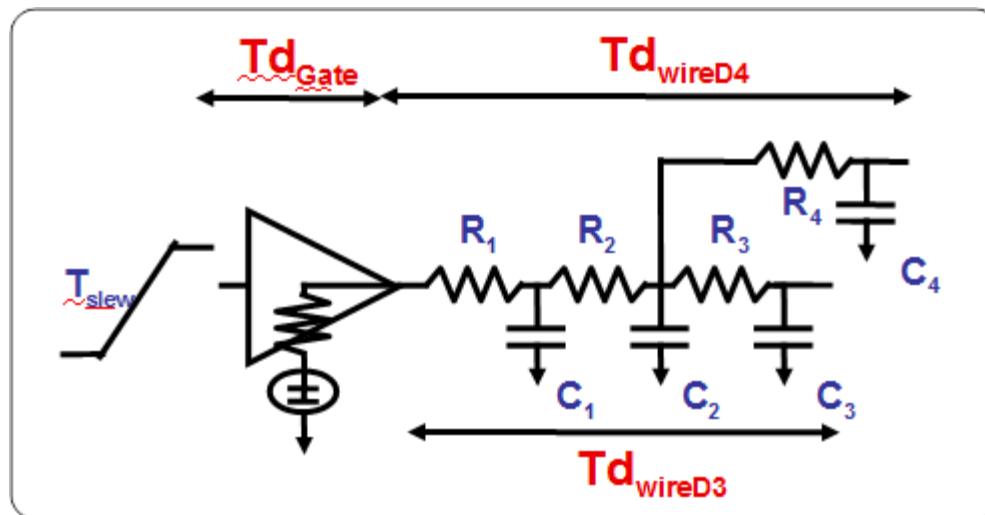
- ◆ WireLoad delay calculation

The wire load delay calculation is done by using the post layout wiring model (stray C/R) and the cell delay model (described in library).

The calculation method for 0.15um-90nm technology:

Gate delay (Td gate) : Input slew/output load capacity dependence model

Wiring delay (Td wire) : AWE and Arnordi method

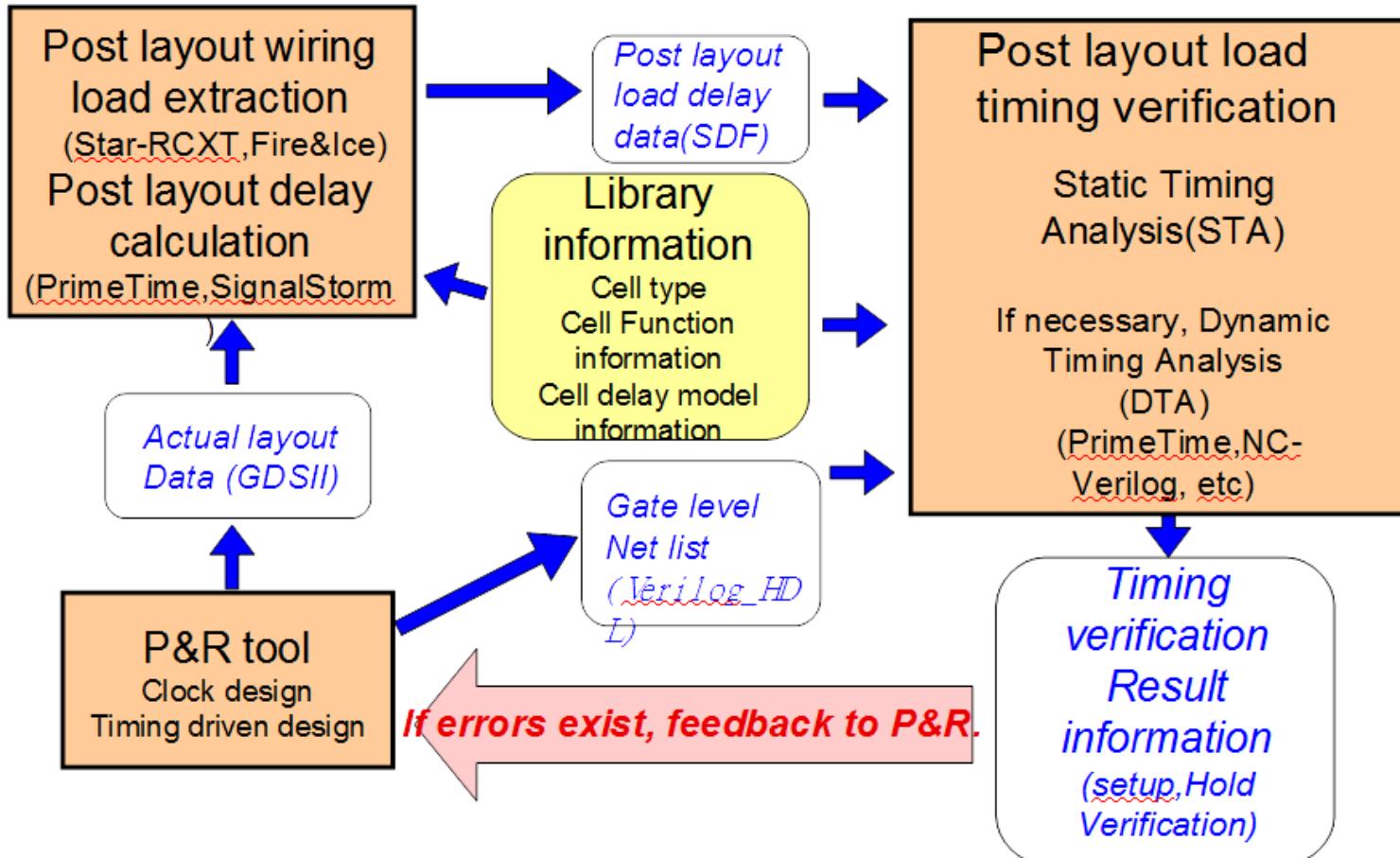


Block and TOP layout design (PnR)

Timing verification

Timing verification is done based on **post layout delay data** extracted from post layout wire load.

Minimum accuracy error to actual LSI(Si) is required.



Block and TOP layout design (PnR)

Space cell insertion for later ECO

As explained in P&R design flow, we need ECO several times before freezing the layout data.

However, It is not practical to re-layout from the beginning.

To make it easy for ECO process (logic modification, timing fixes, ...), we place spare gates (about 2% of logic) to the original design.

When we need to replace cells with big drivability to meet the timing constraints or to fix a logic bug, we use these spare gates and revise the design by modifying only metal wirings.

Content

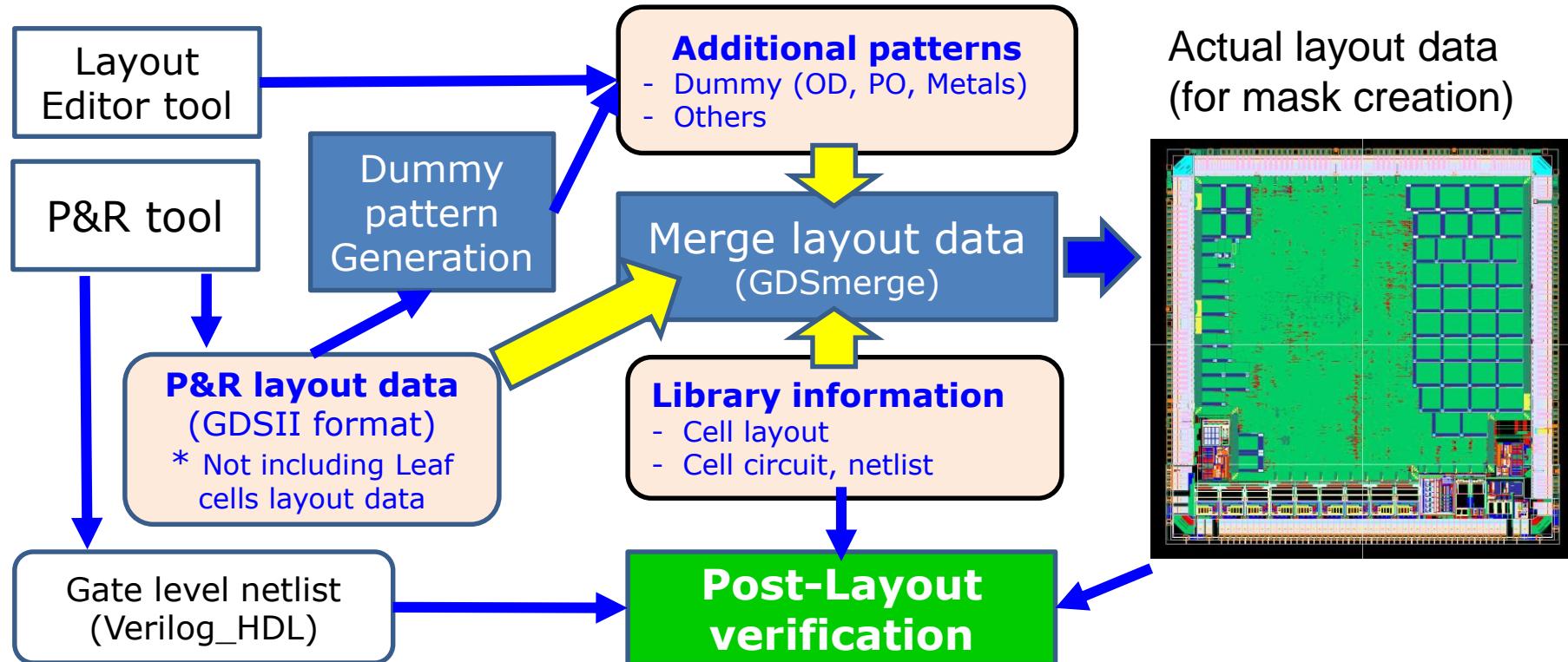
1. Overview of Chip Layout Design
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7. Post-Layout Verification

Post-Layout Verification

Actual data generation

◆ The actual layout data (data for the mask creation) is generated by merging the following data all together:

- (1) P&R layout result (cell placement and wire pattern)
- (2) Cell layout data from libraries
- (3) Additional patterns for manufacturing purpose
(reduce / prevent manufacturing effects).



Post-Layout Verification

Signal Integrity check

- ◆ For LSI of the deep submicron/nano-technology, signal integrity verification is needed.
- ◆ Signal Integrity means following phenomena:
 - (1) Cross-Talk (X-Talk)
Tr/Gate mal-operation and timing change due to noise between signal wirings
 - (2) Power-supply voltage drop / rising of ground voltage. (**IR-Drop**)
Tr/Gate mal-operation and timing change due to power-supply voltage drop
 - (3) Electro Migration (EM)
Disconnection of wiring due to excess current (wiring stress occurs)
 - (4) Hot Carrier (HC)
Tr breakdown due to excessive Tr activation (Tr stress occurs)

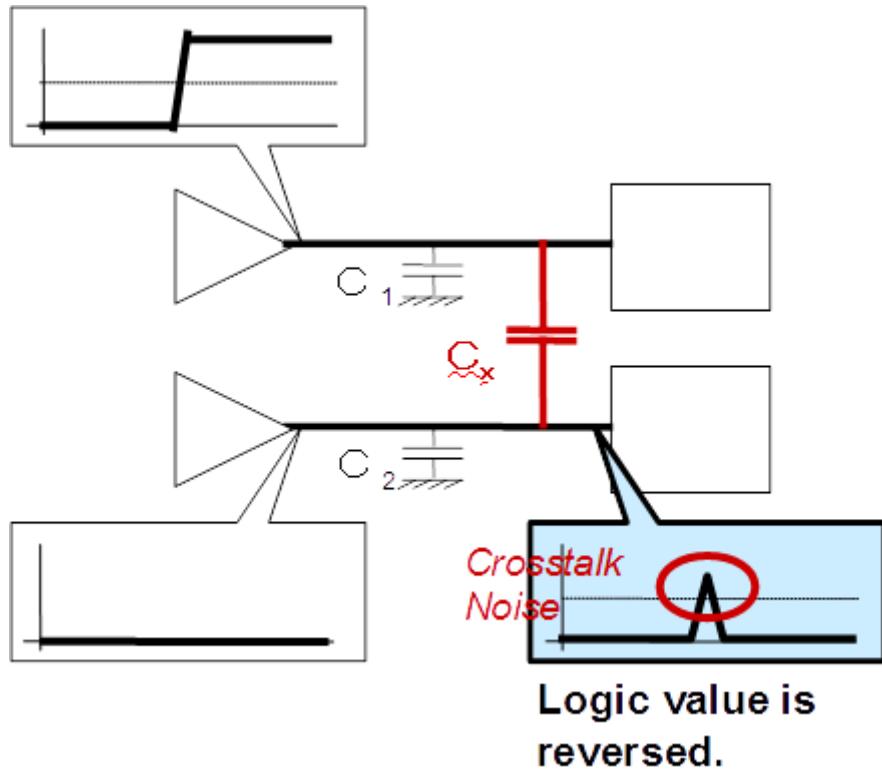
Post-Layout Verification

Signal Integrity check: Cross-talk

◆ **Cross-talk** is that noise generated due to signal operation of adjacent wiring causes mal-function of signal.

- Logic mal-function and timing change make mal-operation of LSI.
 - * Due to finer wiring spacing, the possibility of cross-talk increases.

◆ Logic mal-function due to cross-talk



Asynchronization signal system

The noise is generated in the set and the reset signal.

The logic value of the synchronization signal is reversed..



Logic mal-function

Synchronous signal system

The noise is generated in clock signals.
The logic value (FF output) synchronizing with clock is reversed.

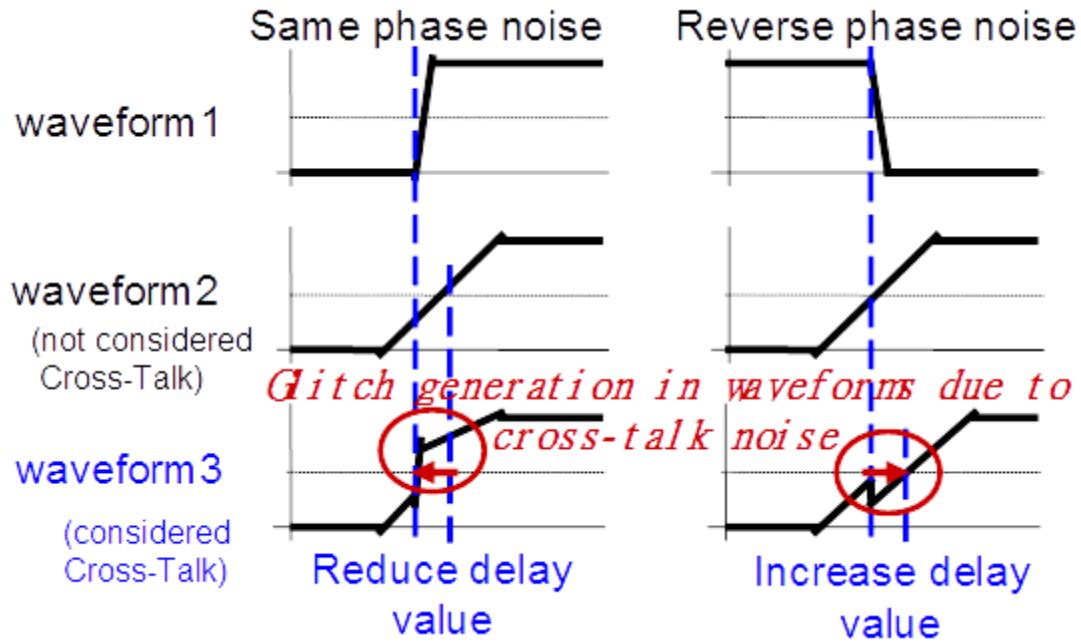
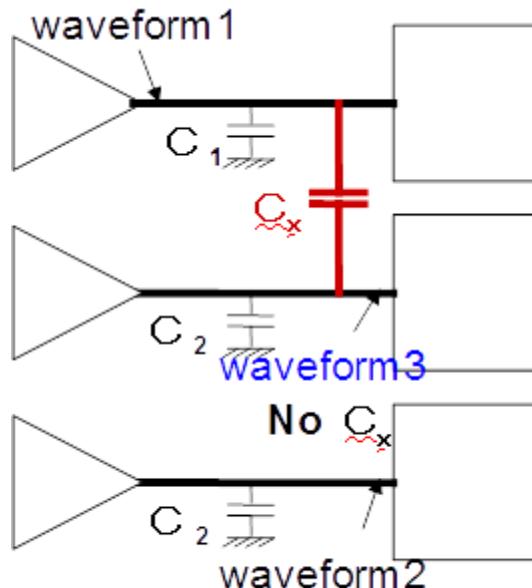


Logic mal-function

Post-Layout Verification

Signal Integrity check: Cross-talk

◆ Timing change due to cross-talk



The delay value is reduced due to same phase noise and increased due to reverse phase noise.

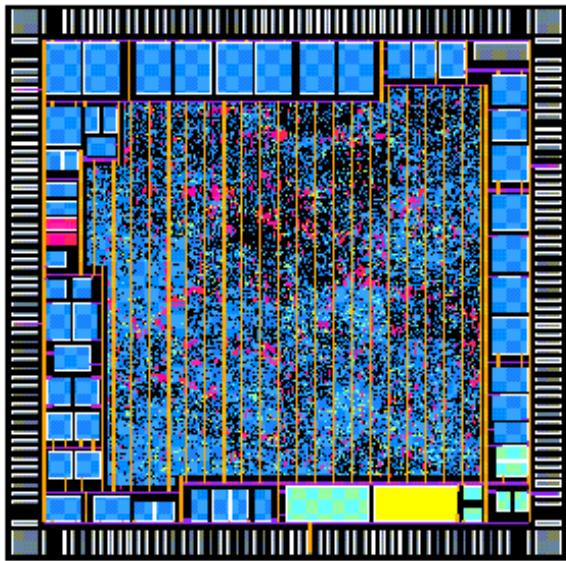


There is a possibility of new timing constraint violation.

Post-Layout Verification

Signal Integrity check: EM/IR-Drop

Analysis of power consumption distribution

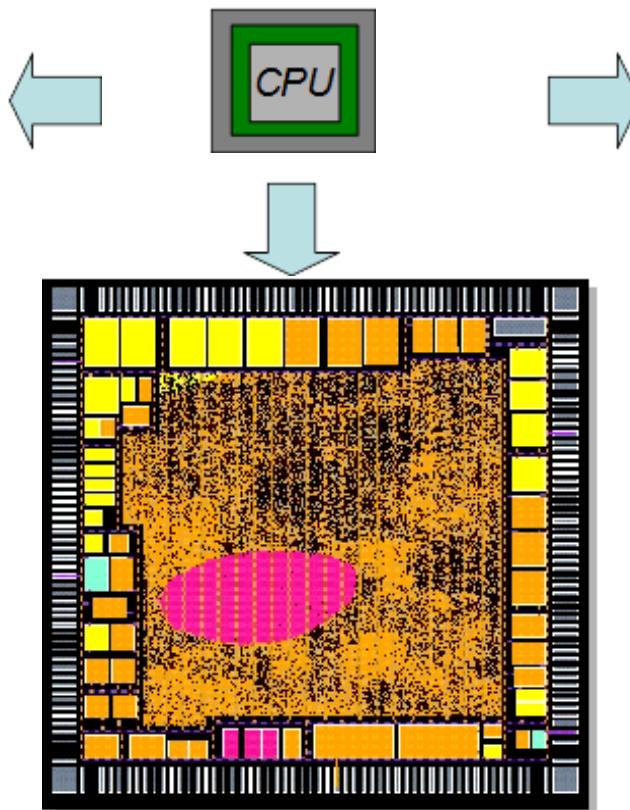


Cells are displayed with several colors based on power consumption.

IR-Drop is displayed based on IR-Drop values.

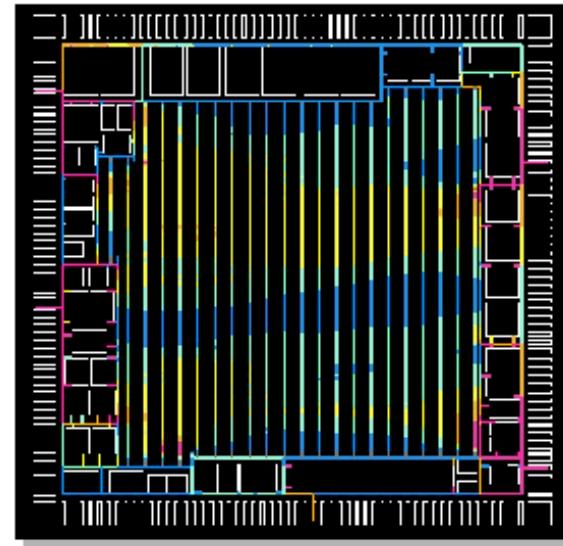
↓
Need to reinforce power supply if reference value is exceeded (manual correction (automatic correction is not applicable)).

Layout data



Analysis of power-supply voltage drop distribution

Analysis of power supply wiring electromigration



Wires are displayed with several colors based on current density.



Need to lower current density if reference value is exceeded (manual correction (automatic correction is not applicable)).

Post-Layout Verification

Physical verification

- ◆ Layout verification is the physical verification of data for mask creation.
Main features are as follows.

Verification item	Input data	Content of Verification
Connection check (LVS)	Logic net data Layout data	Extracts devices and connections topologically from layout data, and compares device connection of logic net data.
Electric rule check (ERC)	Layout data	Electric rule check of power supply, components, etc.
Design rule check (DRC)	Layout data	Geometrical dimension and position check between figures in layout data

LVS(Layout vs Schematic),
DRC(Design Rule Check)

ERC(Electrical Rule Check)

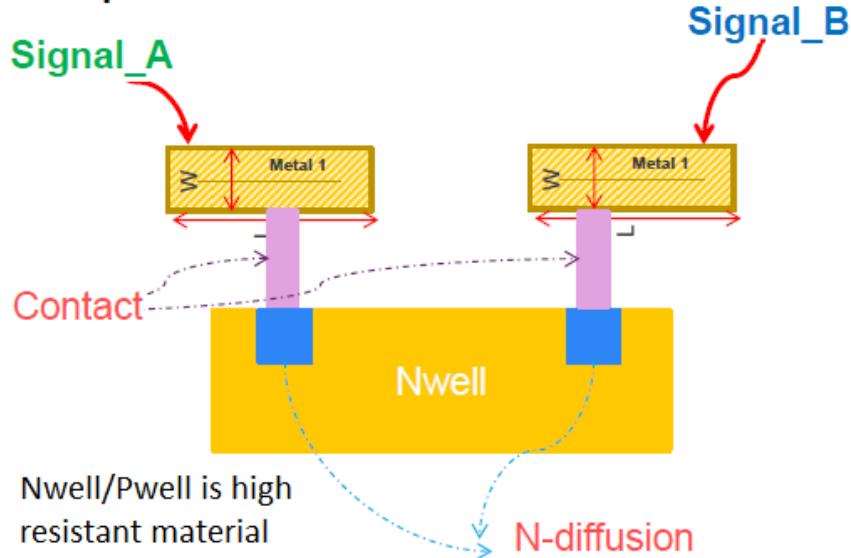
Post-Layout Verification

ERC check

ERC (Electrical Rule Check) involves checking a design for all electrical connections (mainly to PG supply)

- Soft connect checking
- Path checking
- Ptap/ntap checking
- MOS S/D power and ground checking
- Gate directly connecting to power or ground
- Floating well checking

Example of Soft-connect check



Case 01:

- Signal_A connects to Signal_B.
- Signal_A connects to Power & Signal_B connects to IP's Power.
→ IP will get high resistor but IR-Drop is very Serious.

Case 02: (Open)

- Signal_A connects to Power.
- Signal_B connects to Ground.
→ Signal_A and Signal_B will be shorted
➔ Error.

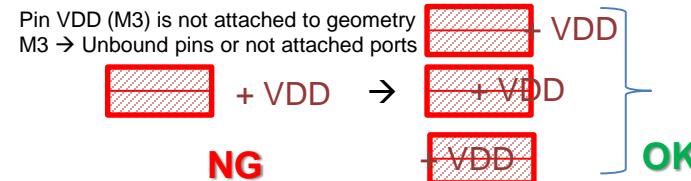
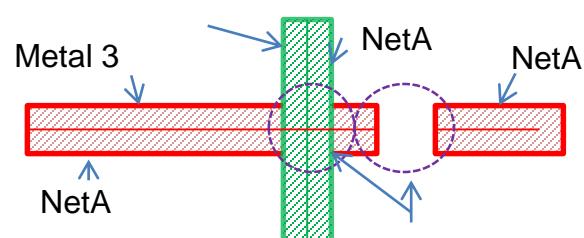
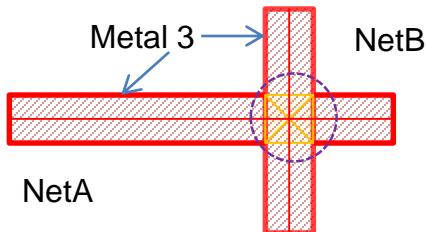
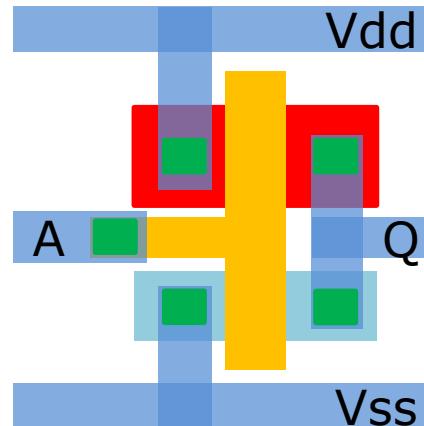
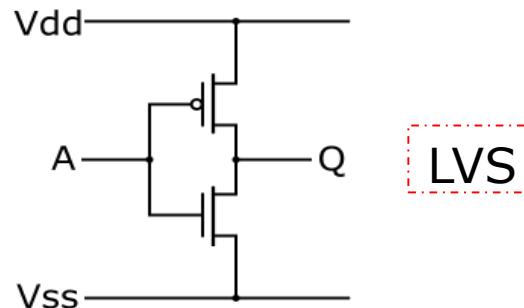
Post-Layout Verification

LVS check

LVS check determines whether Layout data corresponds to the original schematic or circuit diagram of the design.

Layout data, in GDSII format, is a complete data after merging with all library cell layout data)

Schematic data (in .cdl format) is generated from Gate-level netlist (Verilog) of the design and all schematic data (.cdl model) of leaf cells.



Post-Layout Verification

Design Rule check (DRC): Process Design Rule

Design rules are the rules that have to be respected when doing Layout for a design. There are design rules for all of the components, at all physical layers. Fundamentally, these design rules represent the physical limits of the manufacturing process.

There are a lot of Rule in manufacturing phase, now we will investigate 3 basic rule:

- Width Rule
- Space Rule
- Overlap Rule

Post-Layout Verification

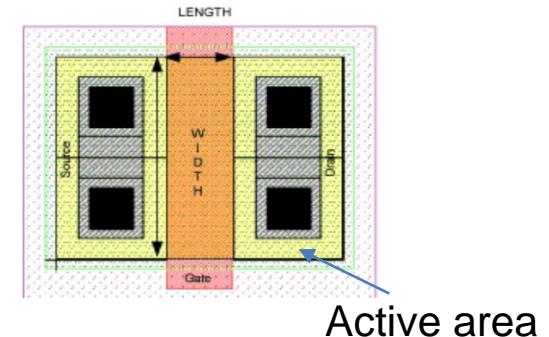
Design Rule check (DRC)

Width Rule:

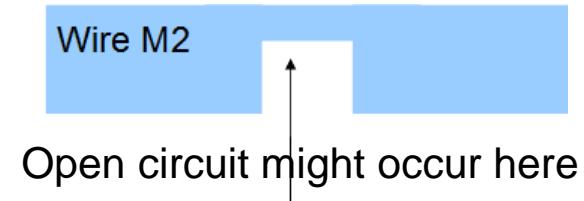
During mask-making, all **shapes and paths are converted to polygons**.

The Width rule refers to the **minimum width of a polygon**, defining the limit of manufacturing process for each layer.

Eg1. The minimum gate length of a transistor is referred to as the minimum width of polysilicon layer over an active area.



Eg2. A violation in a minimum width rule potentially results in an open circuit in the layer.



Eg3. Large currents passing through a narrow metal track can cause the track to act like a fuse. After a long time or during a large current peak, the metal polygon will melt and break. (Electro Migration effect, or EM)



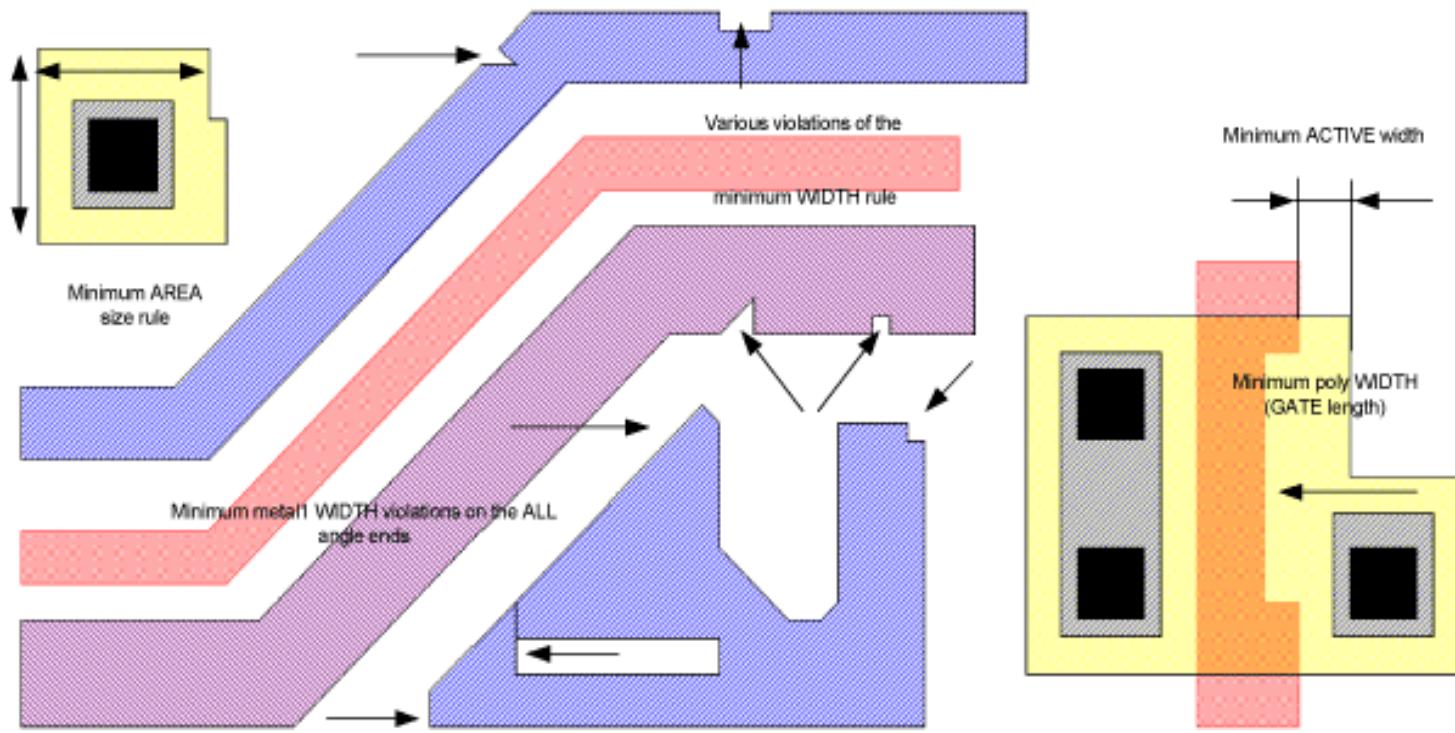
Post-Layout Verification

Design Rule check (DRC)

Width Rule: (Cont'd)

The length of a polygon (or path) is usually unlimited. However, in some processes there may be rules about minimum area of the polygon.

For example in the case of a contact or via, the width and the length rules must be satisfied altogether because of the area constraint.



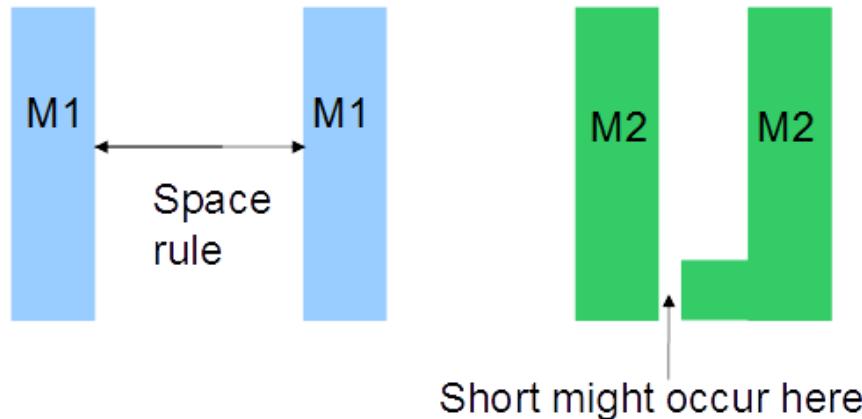
Post-Layout Verification

Design Rule check (DRC)

Space rule:

Space rule refers to the minimum distance between two polygons.

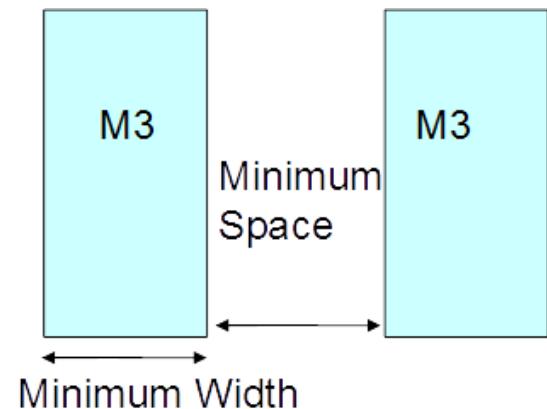
The space rule help avoiding unwanted short circuits between two polygons.



Together, space and width rules define a layer pitch.

Min. Width = Min. Space = Layer pitch

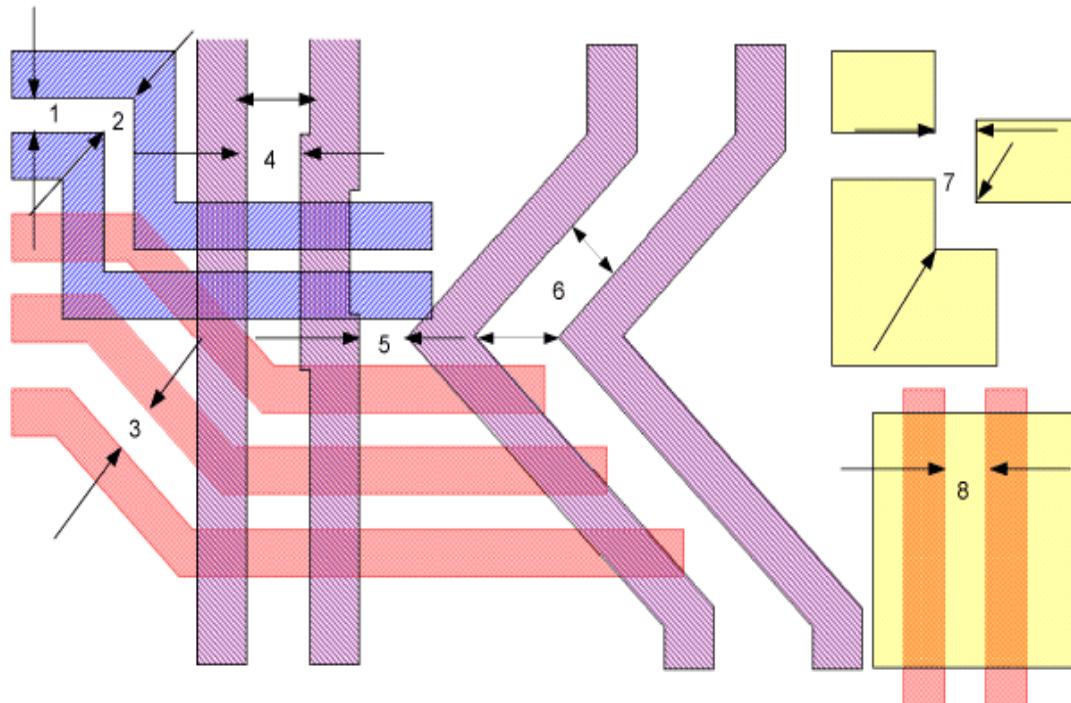
Eg: T28nm layer pitch = 0.05 um



Post-Layout Verification

Design Rule check (DRC)

Space rule: (Cont'd)



Below Figure illustrates some examples of space rules :

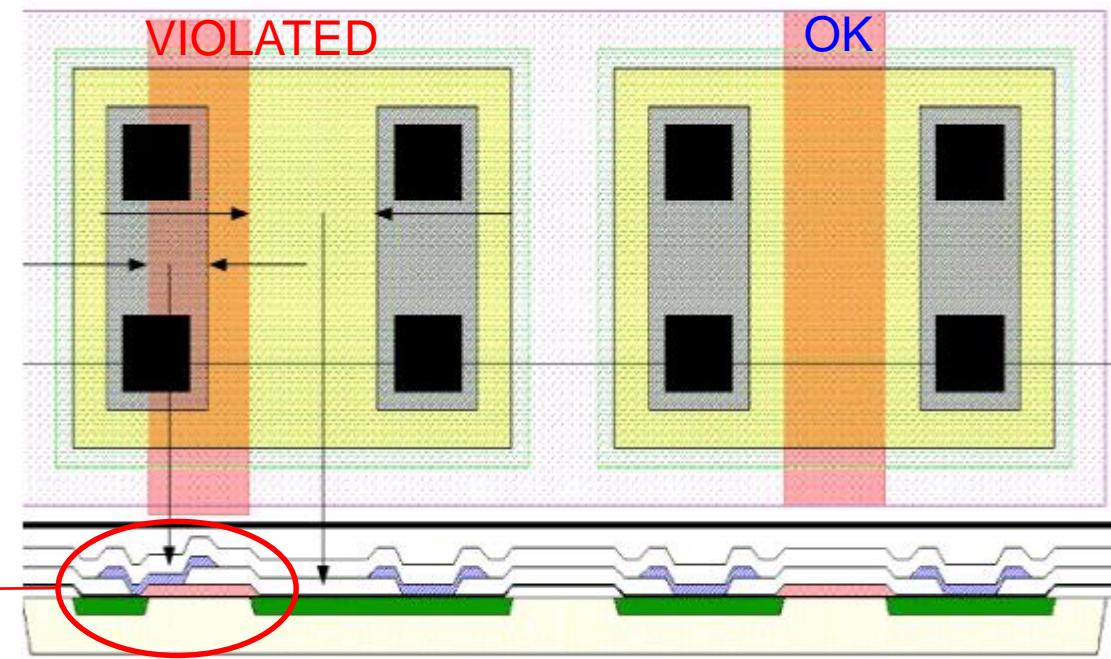
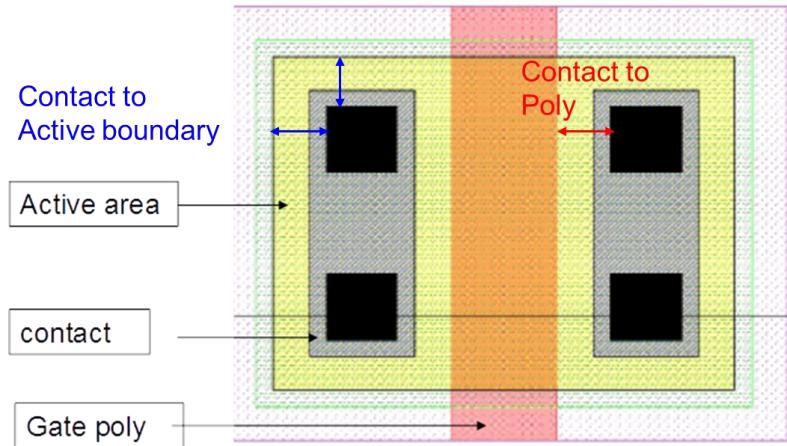
- (1,2) : minimum space between parallel polygons and diagonal corners.
- (3) : minimum space between 45-degree parallel polygons
- (4, 5, 6) : other minimum space between 90 and 45 degree polygons.
- (7) : minimum space between active regions
- (8) : Minimum space between 2 polysilicon. (Eg: abut placement of MOS)

Post-Layout Verification

Design Rule check (DRC)

Space rule: (Cont'd)

Space rules are also applied to **different layers**, for example the space constraint between Contact to Boundary of Active area or to Polysilicon.



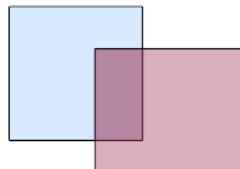
Short circuit between poly (gate)
and metal (Source/Drain)

Post-Layout Verification

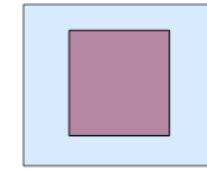
Design Rule check (DRC)

Overlap rule

The overlap rule defines the minimum overlap or surrounding of one polygon by another polygon. This rule always involves polygons existing on different layers.

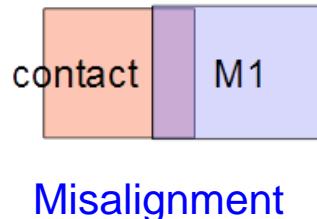


Minimum overlap

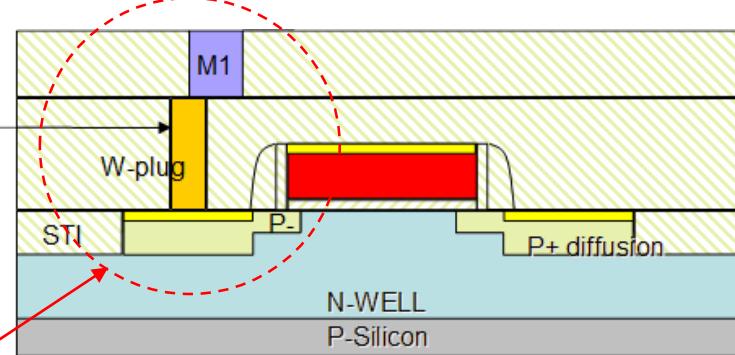


surround

Misalignment between polygons can result in both **undesired open** and **short circuit** connections, depending on the layers involved. Fundamentally, overlap rules reduce the impact of a small misalignment between layers in the manufacturing process



Contact



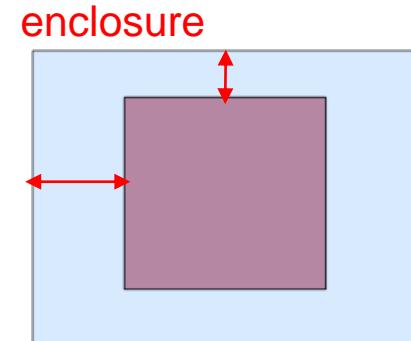
The connectivity between M1 and contact still maintained although there is a misalignment

Post-Layout Verification

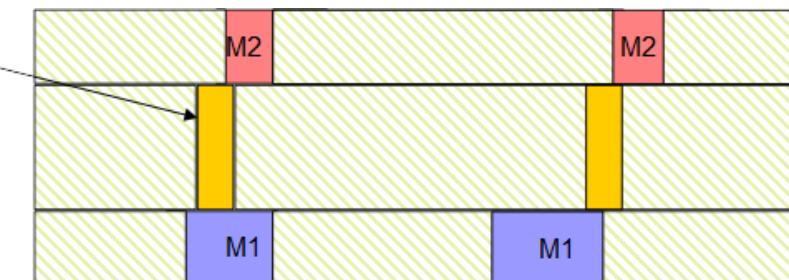
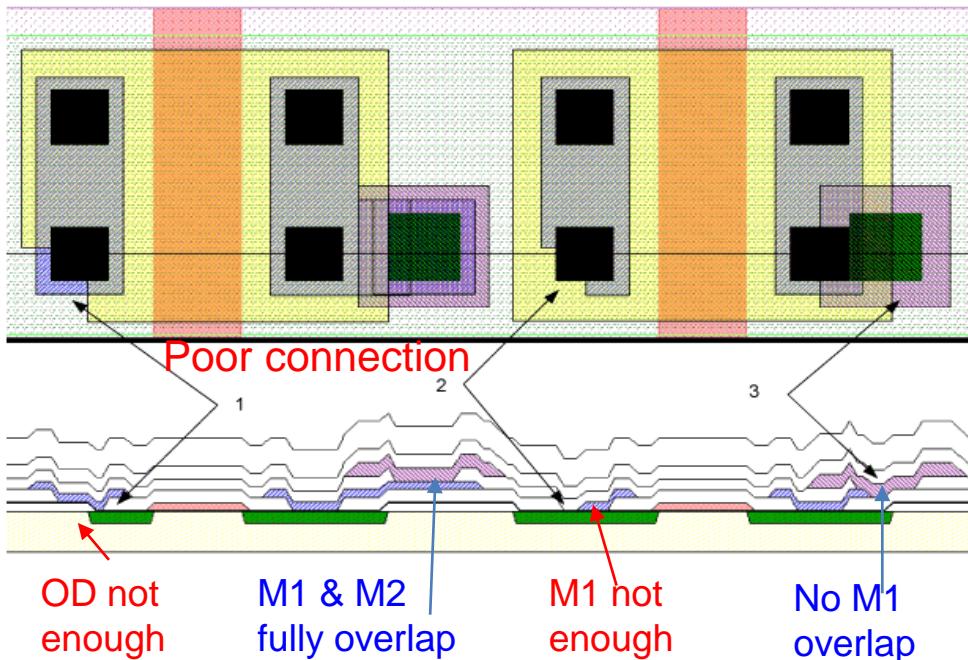
Design Rule check (DRC)

Overlap rule (Cont'd)

Two layers must *not only overlap each other, but also that one layer must surround the other by a certain value* (enclosure).



In the case of a VIA, the **upper and lower layers** must **completely overlap the contact** and surround the contact hole by the overlap rule value.



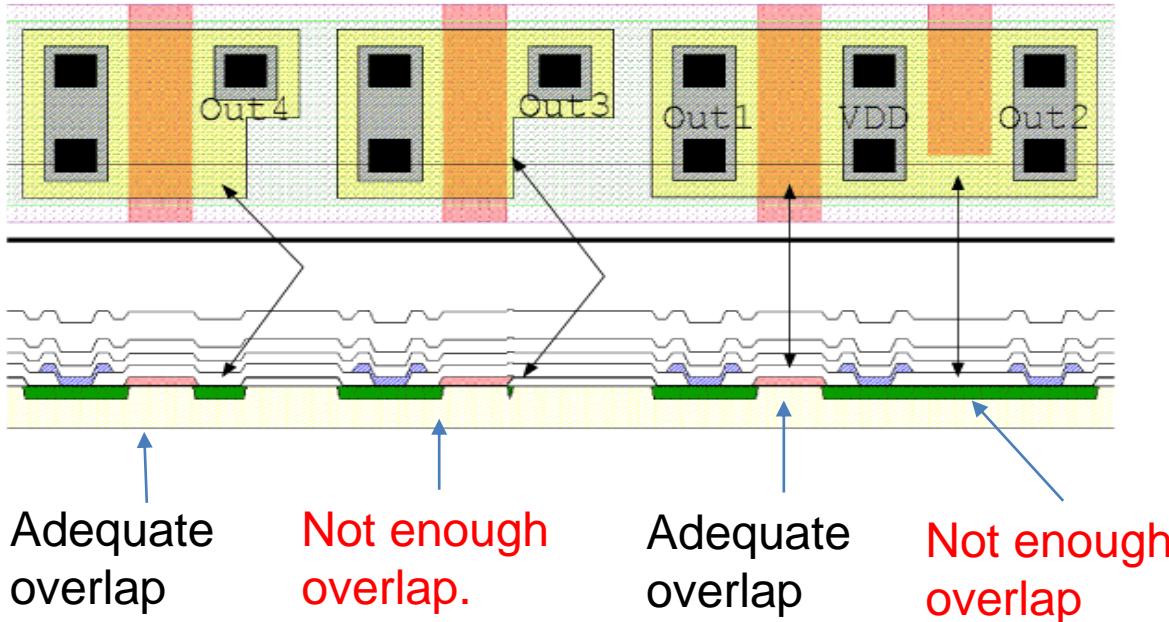
The connectivity between M1 and M2 is weak. Open may occur.

Post-Layout Verification

Design Rule check (DRC)

Overlap rule (Cont'd)

Eg. Overlapping between Poly (Gate) and Active region.



Out3: (Active area does not adequately overlap Poly)

- The thin layer may not be created
- Characteristic of the MOS changes

Out2: (Poly does NOT fully overlap Active area)

- short between Source and Drain (though well)

Post-Layout Verification

Layout verification for advanced technology

- ◆ Beside LVS,ERC and DRC, the following layout verification items are needed for deep sub-micron/nano technology.

(1) Antenna effect verification

Charges are accumulated (on metal or gate surface) during wafer process. These charges can cause damage to normally gate of MOS and sometimes VIA or thin metal.

Antenna effect verification checks the **ratio of Poly (gate) area and metal (or via) area** which are in the **same potential**.

* Layout modification such as pulling up wirings to metal layer, addition of protection diodes, increasing number of vias is needed to the portions where antenna errors are found.

* Antenna effect verification spec is described in **process design manual**.

(2) CMP occupation verification

Chemical Mechanical Polishing(CMP) is adopted to **make plane surface** in wafer process, and to ensure **uniform plane surface** within a chip. So data occupation rule is needed. CMP occupation verification checks this rule.

* If the rule is violated, the dummy patterns are added manually or automatically to the layers which do not satisfy the rule.

* CMP occupation verification spec is described in **process design manual**.

Post-Layout Verification

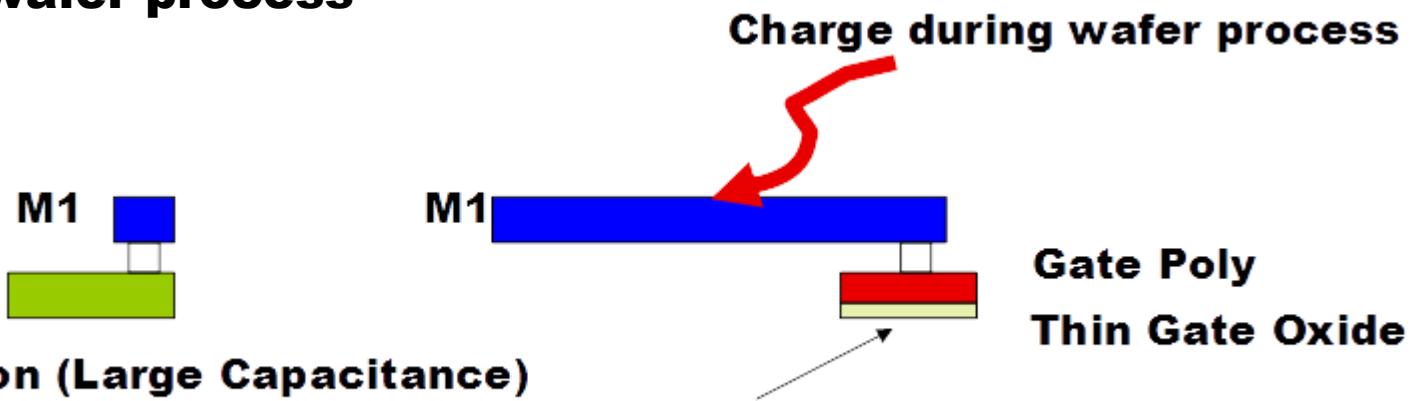
Antenna Effect

Finished structure



Diffusion (Large Capacitance)

During wafer process



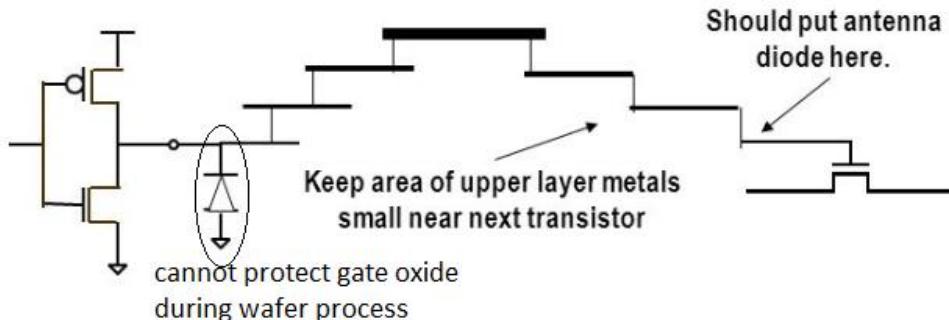
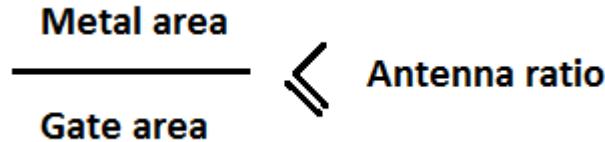
Diffusion (Large Capacitance)

Due to the excess charge, gate oxide breaks down.

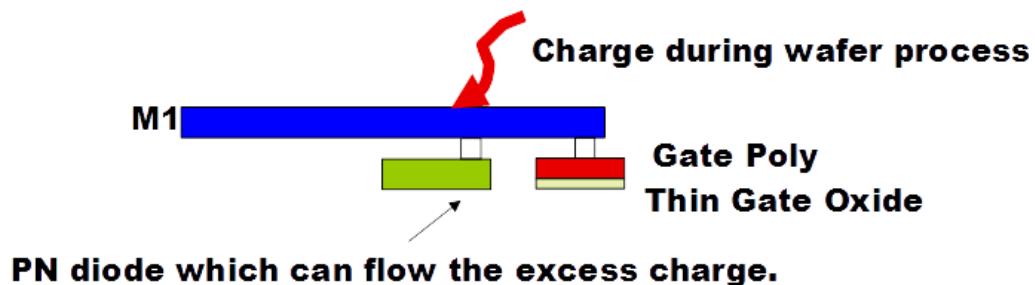
Post-Layout Verification

Antenna Effect: Protection

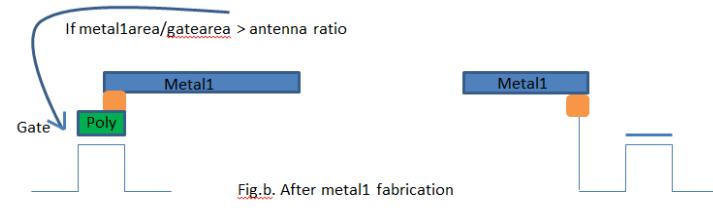
Adding protection diode or bridging routing to higher metal



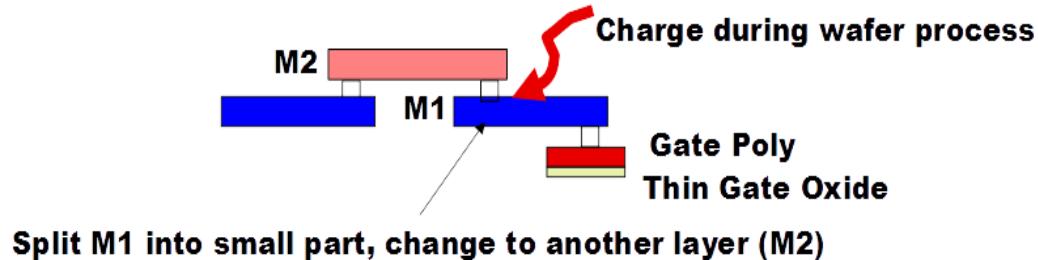
During wafer process



Prevent of Antenna Effect at layout phase



The jumper should be placed near protected gate

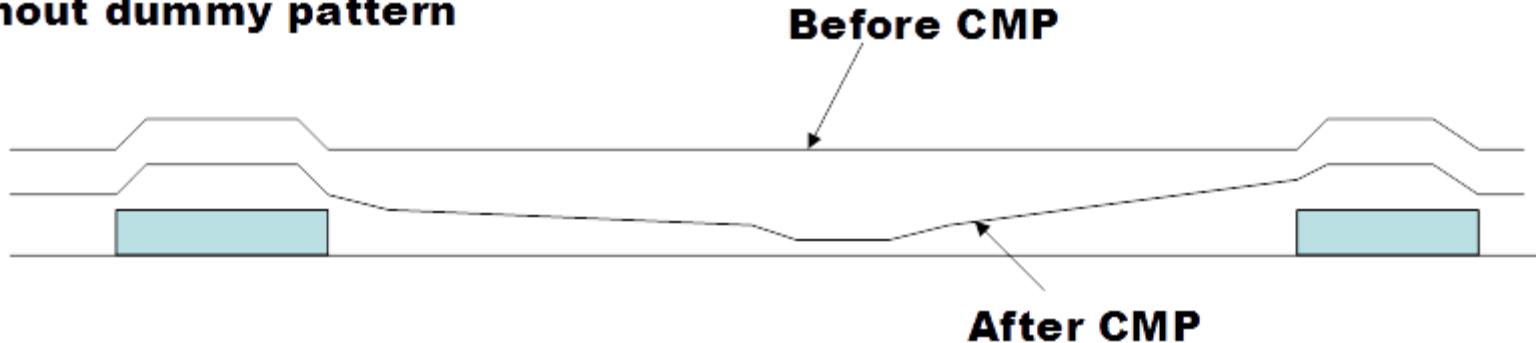


Split M1 into small part, change to another layer (M2)

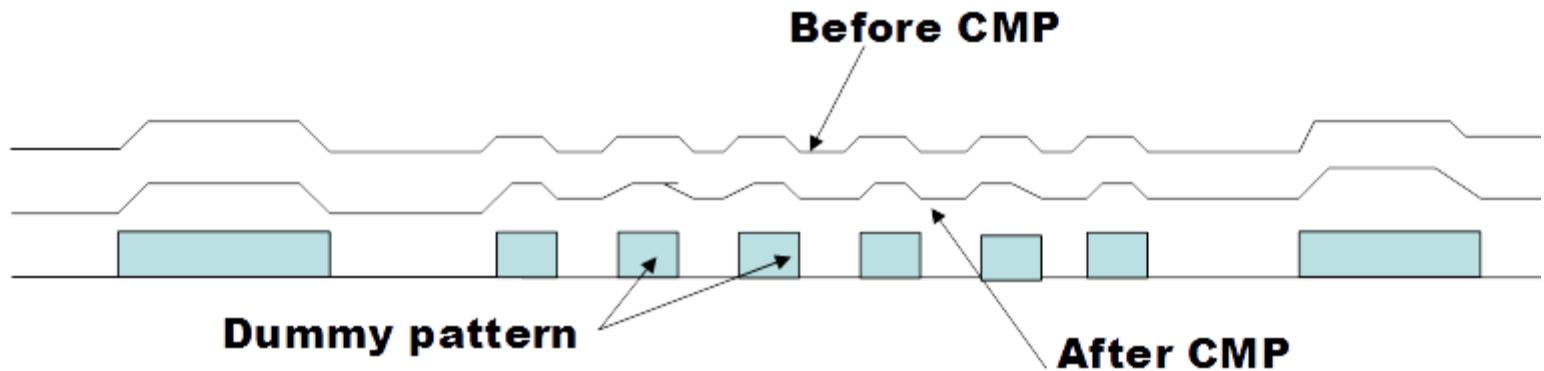
Post-Layout Verification

CMP occupation verification: Dummy pattern insertion

Without dummy pattern



With dummy pattern



Dummy pattern is created and merged to PnR data

The End