# Error Control Module (ECM)

## Features

### Number of Units and Channels

This microcontroller has the following number of ECM unit.

Table 39.1 Number of Units

| Product Name | RH850/E2x-FCC1 | | |
| --- | --- | --- | --- |
| 373pins | 292pins | 176pins |
| Number of Units | 1 | 1 | 1 |
| Name | ECM | ECM | ECM |

Table 39.2 Number of Units

| Product Name | RH850/E2x-FCC1 | | | |
| --- | --- | --- | --- | --- |
| 373pins | 292pins | 176pins | EVA |
| Number of Units | 1 | 1 | 1 | 1 |
| Name | ECM | ECM | ECM | ECM |

Table 39.3 Number of Units

|  |  |  |
| --- | --- | --- |
| Product Name | RH850/E2M | |
| 373 pins | 292 pins |
| Number of Units | 1 | 1 |
| Name | ECM | ECM |

Table 39.4 Number of Units

|  |  |
| --- | --- |
| Product Name | RH850/E2GM |
| 373 pins |
| Number of Units | 1 |
| Name | ECM |

Table 39.5 Number of Units

|  |  |  |
| --- | --- | --- |
| Product Name | RH850/E2L | |
| 292 pins | 176 pins |
| Number of Units | 1 | 1 |
| Name | ECM | ECM |

Table 39.6 Number of Units

| Product Name | RH850/E2x-FCC2 | | |
| --- | --- | --- | --- |
| 468pins | 373pins | EVA |
| Number of Units | 1 | 1 | 1 |
| Name | ECM | ECM | ECM |

Table 39.7 Number of Units

|  |  |  |
| --- | --- | --- |
| Product Name | RH850/E2x-FCC2 | |
| 468 pins | 373 pins |
| Number of Units | 1 | 1 |
| Name | ECM | ECM |

Table 39.8 Number of Units

|  |  |
| --- | --- |
| Product Name | RH850/E2UH |
| 468 pins |
| Number of Units | 1 |
| Name | ECM |

Table 39.9 Number of Units

|  |  |  |
| --- | --- | --- |
| Product Name | RH850/E2x-FCC2 | |
| 468 pins | 373 pins |
| Number of Units | 1 | 1 |
| Name | ECM | ECM |

Table . Index

|  |  |
| --- | --- |
| Index | Meaning |
| m | Throughout this section, the individual ECM Master and ECM Checker are identified by the index “m” (m = M, C). |

### Register Base Address

ECM base addresses are listed in the following table.

ECM register addresses are given as offsets from the base addresses in general.

Table . Register Base Address

|  |  |  |
| --- | --- | --- |
| Base Address Name | Base Address | Bus Group |
| <ECMM\_base> | FFCB 0000H | Peripheral Group 6 |
| <ECMC\_base> | FFCB 1000H | Peripheral Group 6 |
| <ECM\_base> | FFCB 2000H | Peripheral Group 6 |

### Clock Supply

Clock supply by and to ECM is listed in the following table.

Table . Clock Supply

|  |  |  |
| --- | --- | --- |
| Unit Name | Unit Clock Name | Clock Supply Name |
| ECM | PCLK | CLK\_LSB |
| cntclk \*1 | CLK\_WDTICUM |

1. cntclk is used for delay timer and clear mask timer logics

### Interrupt Requests

ECM interrupt requests are listed in the following table. The interrupt request signal is driven to the high level with a pulse width of one cycle of PCLK when error source status that interrupt generation is enable is set.

Table . Interrupt Requests

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Interrupt symbol name | Unit Interrupt Signal | Outline | Interrupt Number | sDMA Trigger Number | DTS Trigger Number |
| INTECMMI | INTECMMI | ECM maskable interrupt (EI level) | EIINT8 | — | — |
| INTECMDCLSMI | INTECMDCLSMI\*1 | DCLS error interrupt (EI level) | EIINT9 | — | — |
| FEINT0 | INTECMNMI | ECM non-maskable interrupt (FE level) | FEINT0 | — | — |

Note1:PE2 and PE3 is unimplemented Checker core.

### Reset Sources

ECMM, ECMC and ECM reset sources are listed in the following table. ECMM, ECMC and ECM are initialized by these reset sources.

Table . Reset Sources (/2)

| Unit Name | Register Name | Reset condition | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Power Up Reset | System Reset1 | System Reset2 | Application Reset | Module Reset | JTAG Reset |
| ECM Master Registers | | | | | | | |
| ECMM | ECM master error set trigger register | √ | √ | √ | √ | — | — |
| ECMM | ECM master error clear trigger register | √ | √ | √ | √ | — | — |
| ECMM | ECM master error source status register n\*1 | √ | √\*2 | — | — | — | — |
| ECM Checker Registers | | | | | | | |
| ECMC | ECM checker error set trigger register | √ | √ | √ | √ | — | — |
| ECMC | ECM checker error clear trigger register | √ | √ | √ | √ | — | — |
| ECMC | ECM checker error source status register n\*1 | √ | √\*2 | — | — | — | — |
| ECM Common Registers | | | | | | | |
| ECM | ECM error pulse configuration register | √ | √ | √ | √ | — | — |
| ECM | ECM maskable interrupt configuration register n\*1 | √ | √ | √ | √ | — | — |
| ECM | ECM non-maskable interrupt configuration register n\*1 | √ | √ | √ | √ | — | — |
| ECM | ECM internal reset configuration register n\*1 | √ | √ | √ | √ | — | — |
| ECM | ECM error mask register n\*1 | √ | √ | √ | √ | — | — |
| ECM | ECM error source status clear register n\*1 | √ | √ | √ | √ | — | — |
| ECM | ECM key-code protection register | √ | √ | √ | √ | — | — |

Table 39.14 Reset Sources (/2)

| Unit Name | Register Name | Reset condition | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Power Up Reset | System Reset1 | System Reset2 | Application Reset | Module Reset | JTAG Reset |
| ECM Common Registers | | | | | | | |
| ECM | ECM pseudo error trigger register n\*1 | √ | √ | √ | √ | — | — |
| ECM | ECM delay timer control register | √ | √ | √ | √ | — | — |
| ECM | ECM delay timer register | √ | √ | √ | √ | — | — |
| ECM | ECM delay timer compare register | √ | √ | √ | √ | — | — |
| ECM | ECM maskable interrupt delay timer configuration register n\*1 | √ | √ | √ | √ | — | — |
| ECM | ECM non-maskable interrupt delay timer configuration register n\*1 | √ | √ | √ | √ | — | — |
| ECM | ECM error output clear invalidation configuration register | √ | √ | √ | — | — | — |
| ECM | ECM pseudo error mask register | √ | √ | √ | √ | — | — |

1. n = 0 to 9
2. It is possible to reset only by “Standby Reset”.

### External Input and Output Signals

External Input/output signals of ECM are listed below.

Table . External Input/Output Signals

|  |  |  |
| --- | --- | --- |
| Unit Signal Name | Description | Alternative Port Pin Signal |
|  | Error output master signal |  |
|  | Error output checker signal |  |
|  | Error input signal |  |

## Overview

### Specification Overview

ECM (Error Control Module) collects error signals coming from different error sources and monitoring circuits. It also outputs error signals from the error pins (,) and generates interrupts and Error Control Module Reset signals. Table 39.16 shows the specification overview of ECM.

Table . Specification Overview

| Item | Description |
| --- | --- |
| Safety processing | ECM can handle the following processing in response to error signal inputs from individual modules.  ● Error flag set  ● EI level interrupt generation  EI level interrupt generation can be controlled (enabled/disabled) for individual errors.  ● DCLS error interrupt generation  DCLS error interrupt generation (EI level) can be controlled (enabled/disabled) for individual errors.   Count the DCLS error and error message based on the DCLS error happen times are reported.   2bit status register for counting the DCLS error, the max count is 3.  ● FE level interrupt generation  FE level interrupt generation can be controlled (enabled/disabled) for individual errors.  ● Internal reset generation  System reset 2 or Application reset generation can be controlled (enabled/disabled) for individual errors.  ● Error pin output  Pin output mask can be controlled (enabled/disabled) for individual errors.  Output can be toggled in response to a timer input or made at a fixed level. |
| Error status | ECM incorporates the error status register, which can be used to confirm the error status from the error flag.  The error flags are only cleared by a power up reset or Standby Reset (System reset 1). In case of External reset (System reset1), System reset2, Application reset, Module reset and JTAG reset, the error flags are kept and the reset generation source can be confirmed by reading the status register after reset. |
| Debug, self-diagnosis | ● Pseudo errors can be generated for debug and self-diagnosis.  The operation during injection of pseudo errors is identical to that for the occurrence of real errors.   All configurations for the mask to the error pin output, interrupt, or Error Control Module Reset   apply in the same way.  ● ECM incorporates a loop-back function of the error pin output that is used to diagnose the path to   the error output pin.  The status of the error output pin is reflected to an internal register and can be confirmed by   reading the register. |
| Timeout function | ECM incorporates a function that generates an error signal output or Error Control Module Reset when the count value of the delay timer matches with the delay timer compare register because the delay timer was not stopped during the interrupt processing after being started simultaneously with the occurrence of an interrupt request. |
| Port safe state | ERROROUTZ connects to port safe state and ECM can control the state of general purpose I/O to safe state according to user configuration. Configuration state is Hi-Z, Low and High output. For details of function, see Section 2, Pin Function. |
| Register protection | A write-protection with a key code is implemented to protect registers from unintended write access. For details of function, see Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register. |
| clear masking | ECM incorporates a function that can mask software clearance for until the time which is counted from error occurrence reaches with the Error Output.  Clear Invalidation Configuration register. If another error occurs during time counting,  then the time count is reset and restarted from the beginning. |
| Others | ECM is duplexed. ECM incorporates the error output pin. |

### Block Diagram

ECM is implemented redundant from ECM Master and ECM Checker. See Figure 39.1 Connection of two ECM and Figure 39.2 Connection among ECM Master, ECM Checker and peripherals.



Figure . Connection of ECM



Figure . Connection among ECM Master, ECM Checker and Peripherals

CAUTION

Pay attention to the difference in output voltage between the and

pins because different power supply systems are used for those pins.

pin: SYSVCC (5 V / 3.3 V)

pin: E0VCC (5 V) for P01\_7, P15\_7, P22\_5 and P32\_3; E1VCC (5 V / 3.3 V) for P11\_2; E2VCC (5 V / 3.3 V) for P12\_8

### Error Input

Table 39.18 shows the error inputs to ECM of E2x-FCC1.

Table 39.19 shows the error inputs to ECM of E2M.

Table 39.20 shows the error inputs to ECM of E2GM.

Table 39.21 shows the error inputs to ECM of E2L.

**Table 39.22** shows the inputs to ECM of E2x-FCC2.

**Table 39.23** shows the inputs to ECM of E2UH.

**Table 39.24** shows the inputs to ECM of E2H.

"—":not covered, "√":covered, gray hatching: its number is reserve bit.

Table 39.17 List of Error Inputs (1/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | Dual Core Lock-step | DCLS compare error (PE0) | √ | √ | √ | √ | √ | √ | √ | √ |
| 1 |  | DCLS compare error (PE1) | √ | √ | √ | √ | √ | √ | √ | √ |
| 2 |  | Reserve | — | — | — | — | — | — | — | — |
| 3 |  | Reserve | — | — | — | — | — | — | — | — |
| 4 |  | Reserve | — | — | — | — | — | — | — | — |
| 5 |  | Reserve | — | — | — | — | — | — | — | — |
| 6 |  | Reserve | — | — | — | — | — | — | — | — |
| 7 |  | Reserve | — | — | — | — | — | — | — | — |
| 8 | Watchdog timer | Watchdog timer ch0 error (PE0) | √ | √ | √ | √[\*](#Note1)[1](#Note1) | √ | √ | — | √ |
| 9 |  | Watchdog timer ch1 error (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 10 |  | Reserve | — | — | — | — | — | — | — | — |
| 11 |  | Reserve | — | — | — | — | — | — | — | — |
| 12 |  | Reserve | — | — | — | — | — | — | — | — |
| 13 |  | Reserve | — | — | — | — | — | — | — | — |
| 14 |  | Reserve | — | — | — | — | — | — | — | — |
| 15 |  | Reserve | — | — | — | — | — | — | — | — |
| 16 | Local RAM  (own core) | Local RAM (PE0)  - Address feedback compare error  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 17 |  | Local RAM (PE1)  - Address feedback compare error  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 18 |  | Reserve | — | — | — | — | — | — | — | — |
| 19 |  | Reserve | — | — | — | — | — | — | — | — |
| 20 |  | Reserve | — | — | — | — | — | — | — | — |
| 21 |  | Reserve | — | — | — | — | — | — | — | — |
| 22 |  | Reserve | — | — | — | — | — | — | — | — |
| 23 |  | Reserve | — | — | — | — | — | — | — | — |
| 24 |  | Local RAM ECC (PE0)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 25 |  | Local RAM ECC (PE1)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 26 |  | Reserve | — | — | — | — | — | — | — | — |
| 27 |  | Reserve | — | — | — | — | — | — | — | — |
| 28 |  | Reserve | — | — | — | — | — | — | — | — |
| 29 |  | Reserve | — | — | — | — | — | — | — | — |
| 30 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.17 List of Error Inputs (2/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | Local RAM  (own core) | Reserve | — | — | — | — | — | — | — | — |
| 32 |  | Local RAM ECC (PE0)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 33 |  | Local RAM ECC (PE1)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 34 |  | Reserve | — | — | — | — | — | — | — | — |
| 35 |  | Reserve | — | — | — | — | — | — | — | — |
| 36 |  | Reserve | — | — | — | — | — | — | — | — |
| 37 |  | Reserve | — | — | — | — | — | — | — | — |
| 38 |  | Reserve | — | — | — | — | — | — | — | — |
| 39 |  | Reserve | — | — | — | — | — | — | — | — |
| 40 |  | Local RAM ECC (PE0)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 41 |  | Local RAM ECC (PE1)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 42 |  | Reserve | — | — | — | — | — | — | — | — |
| 43 |  | Reserve | — | — | — | — | — | — | — | — |
| 44 |  | Reserve | — | — | — | — | — | — | — | — |
| 45 |  | Reserve | — | — | — | — | — | — | — | — |
| 46 |  | Reserve | — | — | — | — | — | — | — | — |
| 47 |  | Reserve | — | — | — | — | — | — | — | — |
| 48 | Instruction Cache RAM | Instruction Cache RAM (PE0)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 49 |  | Instruction Cache RAM (PE1)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 50 |  | Reserve | — | — | — | — | — | — | — | — |
| 51 |  | Reserve | — | — | — | — | — | — | — | — |
| 52 |  | Reserve | — | — | — | — | — | — | — | — |
| 53 |  | Reserve | — | — | — | — | — | — | — | — |
| 54 |  | Reserve | — | — | — | — | — | — | — | — |
| 55 |  | Reserve | — | — | — | — | — | — | — | — |
| 56 |  | Instruction Cache RAM EDC (PE0)  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 57 |  | Instruction Cache RAM EDC (PE1)  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 58 |  | Reserve | — | — | — | — | — | — | — | — |
| 59 |  | Reserve | — | — | — | — | — | — | — | — |
| 60 |  | Reserve | — | — | — | — | — | — | — | — |
| 61 |  | Reserve | — | — | — | — | — | — | — | — |
| 62 |  | Reserve | — | — | — | — | — | — | — | — |
| 63 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.17 List of Error Inputs (3/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 64 | Instruction Cache RAM | Reserve | — | — | — | — | — | — | — | — |
| 65 |  | Reserve | — | — | — | — | — | — | — | — |
| 66 |  | Reserve | — | — | — | — | — | — | — | — |
| 67 |  | Reserve | — | — | — | — | — | — | — | — |
| 68 |  | Reserve | — | — | — | — | — | — | — | — |
| 69 |  | Reserve | — | — | — | — | — | — | — | — |
| 70 |  | Reserve | — | — | — | — | — | — | — | — |
| 71 |  | Reserve | — | — | — | — | — | — | — | — |
| 72 | MPU | MPU guard error (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 73 |  | MPU guard error (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 74 |  | Reserve | — | — | — | — | — | — | — | — |
| 75 |  | Reserve | — | — | — | — | — | — | — | — |
| 76 |  | Reserve | — | — | — | — | — | — | — | — |
| 77 |  | Reserve | — | — | — | — | — | — | — | — |
| 78 |  | Reserve | — | — | — | — | — | — | — | — |
| 79 |  | Reserve | — | — | — | — | — | — | — | — |
| 80 | PE guard function (PEG) | PEG error (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 81 |  | PEG error (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 82 |  | Reserve | — | — | — | — | — | — | — | — |
| 83 |  | Reserve | — | — | — | — | — | — | — | — |
| 84 |  | Reserve | — | — | — | — | — | — | — | — |
| 85 |  | Reserve | — | — | — | — | — | — | — | — |
| 86 |  | Reserve | — | — | — | — | — | — | — | — |
| 87 |  | Reserve | — | — | — | — | — | — | — | — |
| 88 | Clock Monitor | Clock monitor error (CLMA5) (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 89 |  | Clock monitor error (CLMA6) (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 90 |  | Reserve | — | — | — | — | — | — | — | — |
| 91 |  | Reserve | — | — | — | — | — | — | — | — |
| 92 |  | Reserve | — | — | — | — | — | — | — | — |
| 93 |  | Reserve | — | — | — | — | — | — | — | — |
| 94 |  | Reserve | — | — | — | — | — | — | — | — |
| 95 |  | Reserve | — | — | — | — | — | — | — | — |
| 96 | OSTM | OSTM1 Interrupt | √ | √ | √ | √ | √ | √ | — | √ |
| 97 |  | OSTM2 Interrupt | √ | √ | √ | √ | √ | √ | — | √ |
| 98 |  | Reserve | — | — | — | — | — | — | — | — |
| 99 |  | Reserve | — | — | — | — | — | — | — | — |
| 100 |  | Reserve | — | — | — | — | — | — | — | — |
| 101 |  | Reserve | — | — | — | — | — | — | — | — |
| 102 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.17 List of Error Inputs (4/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 103 | Reserve |  | — | — | — | — | — | — | — | — |
| 104 | Reserve |  | — | — | — | — | — | — | — | — |
| 105 | Reserve |  | — | — | — | — | — | — | — | — |
| 106 | Reserve |  | — | — | — | — | — | — | — | — |
| 107 | Reserve |  | — | — | — | — | — | — | — | — |
| 108 | Reserve |  | — | — | — | — | — | — | — | — |
| 109 | Reserve |  | — | — | — | — | — | — | — | — |
| 110 | Reserve |  | — | — | — | — | — | — | — | — |
| 111 | Reserve |  | — | — | — | — | — | — | — | — |
| 112 | Mode Error | Unintended Debug Enable detection (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 113 |  | Unintended Debug Enable detection (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 114 |  | Reserve | — | — | — | — | — | — | — | — |
| 115 |  | Reserve | — | — | — | — | — | — | — | — |
| 116 |  | Reserve | — | — | — | — | — | — | — | — |
| 117 |  | Reserve | — | — | — | — | — | — | — | — |
| 118 |  | Reserve | — | — | — | — | — | — | — | — |
| 119 |  | Reserve | — | — | — | — | — | — | — | — |
| 120 | PEG error | PEG error (PE0) Detected in a read request from PE0 to the others LRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 121 |  | PEG error (PE1) Detected in a read request from PE1 to the others LRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 122 |  | Reserve | — | — | — | — | — | — | — | — |
| 123 |  | Reserve | — | — | — | — | — | — | — | — |
| 124 |  | Reserve | — | — | — | — | — | — | — | — |
| 125 |  | Reserve | — | — | — | — | — | — | — | — |
| 126 |  | Reserve | — | — | — | — | — | — | — | — |
| 127 |  | Reserve | — | — | — | — | — | — | — | — |
| 128 | Reserve |  | — | — | — | — | — | — | — | — |
| 129 | Reserve |  | — | — | — | — | — | — | — | — |
| 130 | Reserve |  | — | — | — | — | — | — | — | — |
| 131 | Reserve |  | — | — | — | — | — | — | — | — |
| 132 | Reserve |  | — | — | — | — | — | — | — | — |
| 133 | Reserve |  | — | — | — | — | — | — | — | — |
| 134 | Reserve |  | — | — | — | — | — | — | — | — |
| 135 | Reserve |  | — | — | — | — | — | — | — | — |
| 136 | Reserve |  | — | — | — | — | — | — | — | — |
| 137 | Reserve |  | — | — | — | — | — | — | — | — |
| 138 | Reserve |  | — | — | — | — | — | — | — | — |
| 139 | Reserve |  | — | — | — | — | — | — | — | — |
| 140 | Reserve |  | — | — | — | — | — | — | — | — |

Table 39.17 List of Error Inputs (5/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 141 | Reserve |  | — | — | — | — | — | — | — | — |
| 142 | Reserve |  | — | — | — | — | — | — | — | — |
| 143 | Reserve |  | — | — | — | — | — | — | — | — |
| 144 | Reserve |  | — | — | — | — | — | — | — | — |
| 145 | Reserve |  | — | — | — | — | — | — | — | — |
| 146 | Reserve |  | — | — | — | — | — | — | — | — |
| 147 | Reserve |  | — | — | — | — | — | — | — | — |
| 148 | Reserve |  | — | — | — | — | — | — | — | — |
| 149 | Reserve |  | — | — | — | — | — | — | — | — |
| 150 | Reserve |  | — | — | — | — | — | — | — | — |
| 151 | Reserve |  | — | — | — | — | — | — | — | — |
| 152 | Cluster RAM | Cluster RAM  - Address feedback compare error  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 153 |  | Cluster RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 154 |  | Cluster RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 155 |  | Cluster RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 156 |  | Reserve | — | — | — | — | — | — | — | — |
| 157 |  | Reserve | — | — | — | — | — | — | — | — |
| 158 |  | Reserve | — | — | — | — | — | — | — | — |
| 159 |  | Reserve | — | — | — | — | — | — | — | — |
| 160 | Local RAM  (other core) | LRAM (error by other core access)  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 161 |  | LRAM (error by other core access)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 162 |  | LRAM (error by other core access)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 163 |  | LRAM (error by other core access)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 164 | sDMA | sDMAC0 RAM  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 165 |  | sDMAC0 RAM  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 166 |  | sDMAC1 RAM  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 167 |  | sDMAC1 RAM  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |

Table 39.17 List of Error Inputs (6/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 168 | Peripheral RAM | Peripheral (DTS) RAM ECC  - ECC 2bit error  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 169 |  | Peripheral (DTS) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 170 |  | Peripheral (DTS) RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 171 |  | Peripheral(except DTS) RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 172 |  | Peripheral(FlexRay) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 173 |  | Peripheral(FlexRay) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 174 |  | Peripheral(CAN) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 175 |  | Peripheral(CAN) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 176 |  | Peripheral(DFE) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 177 |  | Peripheral(DFE) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 178 |  | Peripheral(GTM) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 179 |  | Peripheral(GTM) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 180 |  | Peripheral(Ethernet) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 181 |  | Peripheral(Ethernet) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 182 |  | Reserve | — | — | — | — | — | — | — | — |
| 183 |  | Reserve | — | — | — | — | — | — | — | — |
| 184 |  | Reserve | — | — | — | — | — | — | — | — |
| 185 |  | Reserve | — | — | — | — | — | — | — | — |
| 186 |  | Reserve | — | — | — | — | — | — | — | — |
| 187 |  | Reserve | — | — | — | — | — | — | — | — |
| 188 |  | Reserve | — | — | — | — | — | — | — | — |
| 189 |  | Reserve | — | — | — | — | — | — | — | — |
| 190 |  | Reserve | — | — | — | — | — | — | — | — |
| 191 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.17 List of Error Inputs (7/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 192 | Peripheral RAM | Reserve | — | — | — | — | — | — | — | — |
| 193 |  | Reserve | — | — | — | — | — | — | — | — |
| 194 |  | Reserve | — | — | — | — | — | — | — | — |
| 195 |  | Reserve | — | — | — | — | — | — | — | — |
| 196 |  | Reserve | — | — | — | — | — | — | — | — |
| 197 |  | Reserve | — | — | — | — | — | — | — | — |
| 198 |  | Reserve | — | — | — | — | — | — | — | — |
| 199 |  | Reserve | — | — | — | — | — | — | — | — |
| 200 | Code Flash | Code Flash  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 201 |  | Code Flash ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 202 |  | Code Flash ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 203 |  | Code Flash ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 204 |  | Reserve | — | — | — | — | — | — | — | — |
| 205 |  | Reserve | — | — | — | — | — | — | — | — |
| 206 |  | Reserve | — | — | — | — | — | — | — | — |
| 207 |  | Reserve | — | — | — | — | — | — | — | — |
| 208 | Data Flash | Data Flash ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 209 |  | Data Flash ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 210 |  | Data Flash ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 211 |  | Reserve | — | — | — | — | — | — | — | — |
| 212 |  | Reserve | — | — | — | — | — | — | — | — |
| 213 |  | Reserve | — | — | — | — | — | — | — | — |
| 214 |  | Reserve | — | — | — | — | — | — | — | — |
| 215 |  | Reserve | — | — | — | — | — | — | — | — |
| 216 | Bus ECC | Data Bus ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 217 |  | Data Bus ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 218 |  | Address Bus ECC  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 219 |  | Reserve | — | — | — | — | — | — | — | — |
| 220 |  | Reserve | — | — | — | — | — | — | — | — |
| 221 |  | Reserve | — | — | — | — | — | — | — | — |
| 222 |  | Reserve | — | — | — | — | — | — | — | — |
| 223 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.17 List of Error Inputs (8/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 224 | Cluster RAM Guard (CRG) | CRAM Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 225 | P-Bus Guard (PBG) | P-Bus Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 226 | H-Bus Guard (HBG) | H-Bus Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 227 | I-Bus Guard (IBG) | I-Bus Guard error  (IPIR MEV Barrier TPTM) | √ | √ | √ | √ | √ | √ | — | √ |
| 228 | Reserve |  | — | — | — | — | — | — | — | — |
| 229 | Reserve |  | — | — | — | — | — | — | — | — |
| 230 | Reserve |  | — | — | — | — | — | — | — | — |
| 231 | Reserve |  | — | — | — | — | — | — | — | — |
| 232 | Clock Monitor | Clock monitor error (CLMA0) | √ | √ | √ | √ | √ | √ | — | √ |
| 233 |  | Clock monitor error (CLMA1) | √ | √ | √ | √ | √ | √ | — | √ |
| 234 |  | Clock monitor error (CLMA2) | √ | √ | √ | √ | √ | √ | — | √ |
| 235 |  | Clock monitor error (CLMA3) | √ | √ | √ | √ | √ | √ | — | √ |
| 236 |  | Clock monitor error (CLMA4) | √ | √ | √ | √ | √ | √ | — | √ |
| 237 | Reserve |  | — | — | — | — | — | — | — | — |
| 238 | Reserve |  | — | — | — | — | — | — | — | — |
| 239 | Reserve |  | — | — | — | — | — | — | — | — |
| 240 | DSADC  ADC  Cyclic ADC | AD parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 241 | MISG | MISG compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 242 | DTS | DTS compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 243 | External Error Input | ERRORIN | √ | √ | √ | √ | √ | √ | — | √ |
| 244 | Flash | Flash access error | √ | √ | √ | √ | √ | √ | — | √ |
| 245 |  | FACI reset transfer error | √ | — | — | — | √ | — | — | — |
| 246 |  | FBIST parameter transfer error | √ | — | — | — | √ | — | — | — |
| 247 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.17 List of Error Inputs (9/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 248 | SEG | PE0 Code flash, Cache | √ | √ | √ | √ | √ | √ | — | √ |
| 249 |  | PE0 LRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 250 |  | PE0 CRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 251 |  | PE0 Other Slave | √ | √ | √ | √ | √ | √ | — | √ |
| 252 |  | PE1 Code flash, Cache | √ | √ | √ | √ | √ | √ | — | √ |
| 253 |  | PE1 LRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 254 |  | PE1 CRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 255 |  | PE1 Other Slave | √ | √ | √ | √ | √ | √ | — | √ |
| 256 |  | Reserve | — | — | — | — | — | — | — | — |
| 257 |  | Reserve | — | — | — | — | — | — | — | — |
| 258 |  | Reserve | — | — | — | — | — | — | — | — |
| 259 |  | Reserve | — | — | — | — | — | — | — | — |
| 260 |  | Reserve | — | — | — | — | — | — | — | — |
| 261 |  | Reserve | — | — | — | — | — | — | — | — |
| 262 |  | Reserve | — | — | — | — | — | — | — | — |
| 263 |  | Reserve | — | — | — | — | — | — | — | — |
| 264 |  | Reserve | — | — | — | — | — | — | — | — |
| 265 |  | Reserve | — | — | — | — | — | — | — | — |
| 266 |  | Reserve | — | — | — | — | — | — | — | — |
| 267 |  | Reserve | — | — | — | — | — | — | — | — |
| 268 |  | Reserve | — | — | — | — | — | — | — | — |
| 269 |  | Reserve | — | — | — | — | — | — | — | — |
| 270 |  | Reserve | — | — | — | — | — | — | — | — |
| 271 |  | Reserve | — | — | — | — | — | — | — | — |
| 272 |  | Reserve | — | — | — | — | — | — | — | — |
| 273 |  | Reserve | — | — | — | — | — | — | — | — |
| 274 |  | Reserve | — | — | — | — | — | — | — | — |
| 275 |  | Reserve | — | — | — | — | — | — | — | — |
| 276 |  | Reserve | — | — | — | — | — | — | — | — |
| 277 |  | Reserve | — | — | — | — | — | — | — | — |
| 278 |  | Reserve | — | — | — | — | — | — | — | — |
| 279 |  | Reserve | — | — | — | — | — | — | — | — |
| 280 | Data Path Redundancy | DMA Comp error | √ | √ | √ | √ | √ | √ | — | √ |
| 281 |  | BUS Bridge Comp error | √ | √ | √ | √ | √ | √ | — | √ |

Table 39.17 List of Error Inputs (10/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 282 | BUS Routing checker | Inter-processor element Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 283 |  | Inter-cluster Bus (I-Bus) | √ | √ | √ | √ | √ | √ | — | √ |
| 284 |  | Peripheral Bus (P-Bus) | √ | √ | √ | √ | √ | √ | — | √ |
| 285 |  | CRAM Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 286 |  | System Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 287 |  | Global FLASH Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 288 |  | Local FLASH Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 289 |  | Reserve | — | — | — | — | — | — | — | — |
| 290 |  | Reserve | — | — | — | — | — | — | — | — |
| 291 |  | Reserve | — | — | — | — | — | — | — | — |
| 292 | Voltage Monitor | EVCC Secondary HDET | √ | √ | √ | √ | √ | √ | — | √ |
| 293 |  | EVCC Secondary LDET | √ | √ | √ | √ | √ | √ | — | √ |
| 294 |  | VCC Secondary HDET | √ | √ | √ | √ | √ | √ | — | √ |
| 295 |  | VCC Secondary LDET | √ | √ | √ | √ | √ | √ | — | √ |
| 296 |  | VDD Secondary HDET | √ | √ | √ | √ | √ | √ | — | √ |
| 297 |  | VDD Secondary LDET | √ | √ | √ | √ | √ | √ | — | √ |
| 298 |  | Reserve | — | — | — | — | — | — | — | — |
| 299 | Mode Error | Mode error  - Unintended activation of Production Test Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 300 |  | Mode error  - Unintended activation of Normal Operation Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 301 |  | Mode error  - Unintended deactivation of Normal Operation Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 302 |  | Mode error  - Unintended activation of Serial Programming Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 303 |  | Mode error  - Unintended activation of User Boot Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 304 |  | Mode error  - Unintended deactivation of User Boot Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 305 |  | Mode error  - Mode latch error | √ | √ | √ | √ | √ | √ | — | √ |
| 306 | Reserve |  | — | — | — | — | — | — | — | — |
| 307 | Reserve |  | — | — | — | — | — | — | — | — |
| 308 | ECM | ECM compare error | √ | √ | √ | √ | √ | √ | — | √ |

1. The internal reset generation is enabled in the initial state.

Table 39.18 List of Error Inputs of E2x-FCC1 (1/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | Dual Core Lock-step | DCLS compare error (PE0) | √ | √ | √ | √ | √ | √ | √ | √ |
| 1 |  | DCLS compare error (PE1) | √ | √ | √ | √ | √ | √ | √ | √ |
| 2 |  | Reserve | — | — | — | — | — | — | — | — |
| 3 |  | Reserve | — | — | — | — | — | — | — | — |
| 4 |  | Reserve | — | — | — | — | — | — | — | — |
| 5 |  | Reserve | — | — | — | — | — | — | — | — |
| 6 |  | Reserve | — | — | — | — | — | — | — | — |
| 7 |  | Reserve | — | — | — | — | — | — | — | — |
| 8 | Watchdog timer | Watchdog timer ch0 error (PE0) | √ | √ | √ | √[\*](#Note1_FCC1)[1](#Note1_FCC1) | √ | √ | — | √ |
| 9 |  | Watchdog timer ch1 error (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 10 |  | Reserve | — | — | — | — | — | — | — | — |
| 11 |  | Reserve | — | — | — | — | — | — | — | — |
| 12 |  | Reserve | — | — | — | — | — | — | — | — |
| 13 |  | Reserve | — | — | — | — | — | — | — | — |
| 14 |  | Reserve | — | — | — | — | — | — | — | — |
| 15 |  | Reserve | — | — | — | — | — | — | — | — |
| 16 | Local RAM  (own core) | Local RAM (PE0)  - Address feedback compare error  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 17 |  | Local RAM (PE1)  - Address feedback compare error  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 18 |  | Reserve | — | — | — | — | — | — | — | — |
| 19 |  | Reserve | — | — | — | — | — | — | — | — |
| 20 |  | Reserve | — | — | — | — | — | — | — | — |
| 21 |  | Reserve | — | — | — | — | — | — | — | — |
| 22 |  | Reserve | — | — | — | — | — | — | — | — |
| 23 |  | Reserve | — | — | — | — | — | — | — | — |
| 24 |  | Local RAM ECC (PE0)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 25 |  | Local RAM ECC (PE1)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 26 |  | Reserve | — | — | — | — | — | — | — | — |
| 27 |  | Reserve | — | — | — | — | — | — | — | — |
| 28 |  | Reserve | — | — | — | — | — | — | — | — |
| 29 |  | Reserve | — | — | — | — | — | — | — | — |
| 30 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.18 List of Error Inputs of E2x-FCC1 (2/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | Local RAM  (own core) | Reserve | — | — | — | — | — | — | — | — |
| 32 |  | Local RAM ECC (PE0)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 33 |  | Local RAM ECC (PE1)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 34 |  | Reserve | — | — | — | — | — | — | — | — |
| 35 |  | Reserve | — | — | — | — | — | — | — | — |
| 36 |  | Reserve | — | — | — | — | — | — | — | — |
| 37 |  | Reserve | — | — | — | — | — | — | — | — |
| 38 |  | Reserve | — | — | — | — | — | — | — | — |
| 39 |  | Reserve | — | — | — | — | — | — | — | — |
| 40 |  | Local RAM ECC (PE0)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 41 |  | Local RAM ECC (PE1)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 42 |  | Reserve | — | — | — | — | — | — | — | — |
| 43 |  | Reserve | — | — | — | — | — | — | — | — |
| 44 |  | Reserve | — | — | — | — | — | — | — | — |
| 45 |  | Reserve | — | — | — | — | — | — | — | — |
| 46 |  | Reserve | — | — | — | — | — | — | — | — |
| 47 |  | Reserve | — | — | — | — | — | — | — | — |
| 48 | Instruction Cache RAM | Instruction Cache RAM (PE0)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 49 |  | Instruction Cache RAM (PE1)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 50 |  | Reserve | — | — | — | — | — | — | — | — |
| 51 |  | Reserve | — | — | — | — | — | — | — | — |
| 52 |  | Reserve | — | — | — | — | — | — | — | — |
| 53 |  | Reserve | — | — | — | — | — | — | — | — |
| 54 |  | Reserve | — | — | — | — | — | — | — | — |
| 55 |  | Reserve | — | — | — | — | — | — | — | — |
| 56 |  | Instruction Cache RAM EDC (PE0)  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 57 |  | Instruction Cache RAM EDC (PE1)  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 58 |  | Reserve | — | — | — | — | — | — | — | — |
| 59 |  | Reserve | — | — | — | — | — | — | — | — |
| 60 |  | Reserve | — | — | — | — | — | — | — | — |
| 61 |  | Reserve | — | — | — | — | — | — | — | — |
| 62 |  | Reserve | — | — | — | — | — | — | — | — |
| 63 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.18 List of Error Inputs of E2x-FCC1 (3/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 64 | Instruction Cache RAM | Reserve | — | — | — | — | — | — | — | — |
| 65 |  | Reserve | — | — | — | — | — | — | — | — |
| 66 |  | Reserve | — | — | — | — | — | — | — | — |
| 67 |  | Reserve | — | — | — | — | — | — | — | — |
| 68 |  | Reserve | — | — | — | — | — | — | — | — |
| 69 |  | Reserve | — | — | — | — | — | — | — | — |
| 70 |  | Reserve | — | — | — | — | — | — | — | — |
| 71 |  | Reserve | — | — | — | — | — | — | — | — |
| 72 | Reserve |  | — | — | — | — | — | — | — | — |
| 73 | Reserve |  | — | — | — | — | — | — | — | — |
| 74 | Reserve |  | — | — | — | — | — | — | — | — |
| 75 | Reserve |  | — | — | — | — | — | — | — | — |
| 76 | Reserve |  | — | — | — | — | — | — | — | — |
| 77 | Reserve |  | — | — | — | — | — | — | — | — |
| 78 | Reserve |  | — | — | — | — | — | — | — | — |
| 79 | Reserve |  | — | — | — | — | — | — | — | — |
| 80 | PE guard function (PEG) | PEG error (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 81 |  | PEG error (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 82 |  | Reserve | — | — | — | — | — | — | — | — |
| 83 |  | Reserve | — | — | — | — | — | — | — | — |
| 84 |  | Reserve | — | — | — | — | — | — | — | — |
| 85 |  | Reserve | — | — | — | — | — | — | — | — |
| 86 |  | Reserve | — | — | — | — | — | — | — | — |
| 87 |  | Reserve | — | — | — | — | — | — | — | — |
| 88 | Clock Monitor | Clock monitor error (CLMA5) (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 89 |  | Clock monitor error (CLMA6) (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 90 |  | Reserve | — | — | — | — | — | — | — | — |
| 91 |  | Reserve | — | — | — | — | — | — | — | — |
| 92 |  | Reserve | — | — | — | — | — | — | — | — |
| 93 |  | Reserve | — | — | — | — | — | — | — | — |
| 94 |  | Reserve | — | — | — | — | — | — | — | — |
| 95 |  | Reserve | — | — | — | — | — | — | — | — |
| 96 | OSTM | OSTM1 Interrupt | √ | √ | √ | √ | √ | √ | — | √ |
| 97 |  | OSTM2 Interrupt | √ | √ | √ | √ | √ | √ | — | √ |
| 98 |  | Reserve | — | — | — | — | — | — | — | — |
| 99 |  | Reserve | — | — | — | — | — | — | — | — |
| 100 |  | Reserve | — | — | — | — | — | — | — | — |
| 101 |  | Reserve | — | — | — | — | — | — | — | — |
| 102 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.18 List of Error Inputs of E2x-FCC1 (4/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 103 | Reserve |  | — | — | — | — | — | — | — | — |
| 104 | Reserve |  | — | — | — | — | — | — | — | — |
| 105 | Reserve |  | — | — | — | — | — | — | — | — |
| 106 | Reserve |  | — | — | — | — | — | — | — | — |
| 107 | Reserve |  | — | — | — | — | — | — | — | — |
| 108 | Reserve |  | — | — | — | — | — | — | — | — |
| 109 | Reserve |  | — | — | — | — | — | — | — | — |
| 110 | Reserve |  | — | — | — | — | — | — | — | — |
| 111 | Reserve |  | — | — | — | — | — | — | — | — |
| 112 | Mode Error | Unintended Debug Enable detection (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 113 |  | Unintended Debug Enable detection (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 114 |  | Reserve | — | — | — | — | — | — | — | — |
| 115 |  | Reserve | — | — | — | — | — | — | — | — |
| 116 |  | Reserve | — | — | — | — | — | — | — | — |
| 117 |  | Reserve | — | — | — | — | — | — | — | — |
| 118 |  | Reserve | — | — | — | — | — | — | — | — |
| 119 |  | Reserve | — | — | — | — | — | — | — | — |
| 120 | PEG error | PEG error (PE0) Detected in a read request from PE0 to the others LRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 121 |  | PEG error (PE1) Detected in a read request from PE1 to the others LRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 122 |  | Reserve | — | — | — | — | — | — | — | — |
| 123 |  | Reserve | — | — | — | — | — | — | — | — |
| 124 |  | Reserve | — | — | — | — | — | — | — | — |
| 125 |  | Reserve | — | — | — | — | — | — | — | — |
| 126 |  | Reserve | — | — | — | — | — | — | — | — |
| 127 |  | Reserve | — | — | — | — | — | — | — | — |
| 128 | Reserve |  | — | — | — | — | — | — | — | — |
| 129 | Reserve |  | — | — | — | — | — | — | — | — |
| 130 | Reserve |  | — | — | — | — | — | — | — | — |
| 131 | Reserve |  | — | — | — | — | — | — | — | — |
| 132 | Reserve |  | — | — | — | — | — | — | — | — |
| 133 | Reserve |  | — | — | — | — | — | — | — | — |
| 134 | Reserve |  | — | — | — | — | — | — | — | — |
| 135 | Reserve |  | — | — | — | — | — | — | — | — |
| 136 | Reserve |  | — | — | — | — | — | — | — | — |
| 137 | Reserve |  | — | — | — | — | — | — | — | — |
| 138 | Reserve |  | — | — | — | — | — | — | — | — |
| 139 | Reserve |  | — | — | — | — | — | — | — | — |
| 140 | Reserve |  | — | — | — | — | — | — | — | — |

Table 39.18 List of Error Inputs of E2x-FCC1 (5/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 141 | Reserve |  | — | — | — | — | — | — | — | — |
| 142 | Reserve |  | — | — | — | — | — | — | — | — |
| 143 | Reserve |  | — | — | — | — | — | — | — | — |
| 144 | Reserve |  | — | — | — | — | — | — | — | — |
| 145 | Reserve |  | — | — | — | — | — | — | — | — |
| 146 | Reserve |  | — | — | — | — | — | — | — | — |
| 147 | Reserve |  | — | — | — | — | — | — | — | — |
| 148 | Reserve |  | — | — | — | — | — | — | — | — |
| 149 | Reserve |  | — | — | — | — | — | — | — | — |
| 150 | Reserve |  | — | — | — | — | — | — | — | — |
| 151 | Reserve |  | — | — | — | — | — | — | — | — |
| 152 | Cluster RAM | Cluster RAM  - Address feedback compare error  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 153 |  | Cluster RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 154 |  | Cluster RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 155 |  | Cluster RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 156 |  | Reserve | — | — | — | — | — | — | — | — |
| 157 |  | Reserve | — | — | — | — | — | — | — | — |
| 158 |  | Reserve | — | — | — | — | — | — | — | — |
| 159 |  | Reserve | — | — | — | — | — | — | — | — |
| 160 | Local RAM  (other core) | LRAM (error by other core access)  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 161 |  | LRAM (error by other core access)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 162 |  | LRAM (error by other core access)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 163 |  | LRAM (error by other core access)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 164 | sDMA | sDMAC0 RAM  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 165 |  | sDMAC0 RAM  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 166 |  | sDMAC1 RAM  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 167 |  | sDMAC1 RAM  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |

Table 39.18 List of Error Inputs of E2x-FCC1 (6/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 168 | Peripheral RAM | Peripheral (DTS) RAM ECC  - ECC 2bit error  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 169 |  | Peripheral (DTS) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 170 |  | Peripheral (DTS) RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 171 |  | Peripheral(except DTS) RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 172 |  | Peripheral(FlexRay) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 173 |  | Peripheral(FlexRay) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 174 |  | Peripheral(CAN) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 175 |  | Peripheral(CAN) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 176 |  | Peripheral(DFE) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 177 |  | Peripheral(DFE) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 178 |  | Peripheral(GTM) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 179 |  | Peripheral(GTM) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 180 |  | Peripheral(Ethernet) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 181 |  | Peripheral(Ethernet) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 182 |  | Reserve | — | — | — | — | — | — | — | — |
| 183 |  | Reserve | — | — | — | — | — | — | — | — |
| 184 |  | Reserve | — | — | — | — | — | — | — | — |
| 185 |  | Reserve | — | — | — | — | — | — | — | — |
| 186 |  | Reserve | — | — | — | — | — | — | — | — |
| 187 |  | Reserve | — | — | — | — | — | — | — | — |
| 188 |  | Reserve | — | — | — | — | — | — | — | — |
| 189 |  | Reserve | — | — | — | — | — | — | — | — |
| 190 |  | Reserve | — | — | — | — | — | — | — | — |
| 191 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.18 List of Error Inputs of E2x-FCC1 (7/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 192 | Peripheral RAM | Reserve | — | — | — | — | — | — | — | — |
| 193 |  | Reserve | — | — | — | — | — | — | — | — |
| 194 |  | Reserve | — | — | — | — | — | — | — | — |
| 195 |  | Reserve | — | — | — | — | — | — | — | — |
| 196 |  | Reserve | — | — | — | — | — | — | — | — |
| 197 |  | Reserve | — | — | — | — | — | — | — | — |
| 198 |  | Reserve | — | — | — | — | — | — | — | — |
| 199 |  | Reserve | — | — | — | — | — | — | — | — |
| 200 | Code Flash | Code Flash  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 201 |  | Code Flash ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 202 |  | Code Flash ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 203 |  | Code Flash ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 204 |  | Reserve | — | — | — | — | — | — | — | — |
| 205 |  | Reserve | — | — | — | — | — | — | — | — |
| 206 |  | Reserve | — | — | — | — | — | — | — | — |
| 207 |  | Reserve | — | — | — | — | — | — | — | — |
| 208 | Data Flash | Data Flash ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 209 |  | Data Flash ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 210 |  | Data Flash ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 211 |  | Reserve | — | — | — | — | — | — | — | — |
| 212 |  | Reserve | — | — | — | — | — | — | — | — |
| 213 |  | Reserve | — | — | — | — | — | — | — | — |
| 214 |  | Reserve | — | — | — | — | — | — | — | — |
| 215 |  | Reserve | — | — | — | — | — | — | — | — |
| 216 | Bus ECC | Data Bus ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 217 |  | Data Bus ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 218 |  | Address Bus ECC  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 219 |  | Reserve | — | — | — | — | — | — | — | — |
| 220 |  | Reserve | — | — | — | — | — | — | — | — |
| 221 |  | Reserve | — | — | — | — | — | — | — | — |
| 222 |  | Reserve | — | — | — | — | — | — | — | — |
| 223 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.18 List of Error Inputs of E2x-FCC1 (8/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 224 | Cluster RAM Guard (CRG) | CRAM Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 225 | P-Bus Guard (PBG) | P-Bus Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 226 | H-Bus Guard (HBG) | H-Bus Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 227 | I-Bus Guard (IBG) | I-Bus Guard error  (IPIR MEV Barrier TPTM) | √ | √ | √ | √ | √ | √ | — | √ |
| 228 | Reserve |  | — | — | — | — | — | — | — | — |
| 229 | Reserve |  | — | — | — | — | — | — | — | — |
| 230 | Reserve |  | — | — | — | — | — | — | — | — |
| 231 | Reserve |  | — | — | — | — | — | — | — | — |
| 232 | Clock Monitor | Clock monitor error (CLMA0) | √ | √ | √ | √ | √ | √ | — | √ |
| 233 |  | Clock monitor error (CLMA1) | √ | √ | √ | √ | √ | √ | — | √ |
| 234 |  | Clock monitor error (CLMA2) | √ | √ | √ | √ | √ | √ | — | √ |
| 235 |  | Clock monitor error (CLMA3) | √ | √ | √ | √ | √ | √ | — | √ |
| 236 |  | Clock monitor error (CLMA4) | √ | √ | √ | √ | √ | √ | — | √ |
| 237 | Reserve |  | — | — | — | — | — | — | — | — |
| 238 | Reserve |  | — | — | — | — | — | — | — | — |
| 239 | Reserve |  | — | — | — | — | — | — | — | — |
| 240 | DSADC  ADC  Cyclic ADC | AD parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 241 | MISG | MISG compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 242 | DTS | DTS compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 243 | External Error Input | ERRORIN | √ | √ | √ | √ | √ | √ | — | √ |
| 244 | Flash | Flash access error | √ | √ | √ | √ | √ | √ | — | √ |
| 245 |  | FACI reset transfer error | √ | — | — | — | √ | — | — | — |
| 246 |  | FBIST parameter transfer error | √ | — | — | — | √ | — | — | — |
| 247 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.18 List of Error Inputs of E2x-FCC1 (9/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 248 | Reserve |  | — | — | — | — | — | — | — | — |
| 249 | Reserve |  | — | — | — | — | — | — | — | — |
| 250 | Reserve |  | — | — | — | — | — | — | — | — |
| 251 | Reserve |  | — | — | — | — | — | — | — | — |
| 252 | Reserve |  | — | — | — | — | — | — | — | — |
| 253 | Reserve |  | — | — | — | — | — | — | — | — |
| 254 | Reserve |  | — | — | — | — | — | — | — | — |
| 255 | Reserve |  | — | — | — | — | — | — | — | — |
| 256 | Reserve |  | — | — | — | — | — | — | — | — |
| 257 | Reserve |  | — | — | — | — | — | — | — | — |
| 258 | Reserve |  | — | — | — | — | — | — | — | — |
| 259 | Reserve |  | — | — | — | — | — | — | — | — |
| 260 | Reserve |  | — | — | — | — | — | — | — | — |
| 261 | Reserve |  | — | — | — | — | — | — | — | — |
| 262 | Reserve |  | — | — | — | — | — | — | — | — |
| 263 | Reserve |  | — | — | — | — | — | — | — | — |
| 264 | Reserve |  | — | — | — | — | — | — | — | — |
| 265 | Reserve |  | — | — | — | — | — | — | — | — |
| 266 | Reserve |  | — | — | — | — | — | — | — | — |
| 267 | Reserve |  | — | — | — | — | — | — | — | — |
| 268 | Reserve |  | — | — | — | — | — | — | — | — |
| 269 | Reserve |  | — | — | — | — | — | — | — | — |
| 270 | Reserve |  | — | — | — | — | — | — | — | — |
| 271 | Reserve |  | — | — | — | — | — | — | — | — |
| 272 | Reserve |  | — | — | — | — | — | — | — | — |
| 273 | Reserve |  | — | — | — | — | — | — | — | — |
| 274 | Reserve |  | — | — | — | — | — | — | — | — |
| 275 | Reserve |  | — | — | — | — | — | — | — | — |
| 276 | Reserve |  | — | — | — | — | — | — | — | — |
| 277 | Reserve |  | — | — | — | — | — | — | — | — |
| 278 | Reserve |  | — | — | — | — | — | — | — | — |
| 279 | Reserve |  | — | — | — | — | — | — | — | — |
| 280 | Data Path Redundancy | DMA Comp error | √ | √ | √ | √ | √ | √ | — | √ |
| 281 |  | BUS Bridge Comp error | √ | √ | √ | √ | √ | √ | — | √ |

Table 39.18 List of Error Inputs of E2x-FCC1 (10/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 282 | BUS Routing checker | Inter-processor element Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 283 |  | Inter-cluster Bus (I-Bus) | √ | √ | √ | √ | √ | √ | — | √ |
| 284 |  | Peripheral Bus (P-Bus) | √ | √ | √ | √ | √ | √ | — | √ |
| 285 |  | CRAM Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 286 |  | System Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 287 |  | Global FLASH Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 288 |  | Local FLASH Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 289 |  | Reserve | — | — | — | — | — | — | — | — |
| 290 |  | Reserve | — | — | — | — | — | — | — | — |
| 291 |  | Reserve | — | — | — | — | — | — | — | — |
| 292 | Voltage Monitor | EVCC Secondary HDET | √ | √ | √ | √ | √ | √ | — | √ |
| 293 |  | EVCC Secondary LDET | √ | √ | √ | √ | √ | √ | — | √ |
| 294 |  | VCC Secondary HDET | √ | √ | √ | √ | √ | √ | — | √ |
| 295 |  | VCC Secondary LDET | √ | √ | √ | √ | √ | √ | — | √ |
| 296 |  | VDD Secondary HDET | √ | √ | √ | √ | √ | √ | — | √ |
| 297 |  | VDD Secondary LDET | √ | √ | √ | √ | √ | √ | — | √ |
| 298 |  | Reserve | — | — | — | — | — | — | — | — |
| 299 | Mode Error | Mode error  - Unintended activation of Production Test Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 300 |  | Mode error  - Unintended activation of Normal Operation Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 301 |  | Mode error  - Unintended deactivation of Normal Operation Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 302 |  | Mode error  - Unintended activation of Serial Programming Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 303 |  | Mode error  - Unintended activation of User Boot Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 304 |  | Mode error  - Unintended deactivation of User Boot Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 305 |  | Mode error  - Mode latch error | √ | √ | √ | √ | √ | √ | — | √ |
| 306 | Reserve |  | — | — | — | — | — | — | — | — |
| 307 | Reserve |  | — | — | — | — | — | — | — | — |
| 308 | ECM | ECM compare error | √ | √ | √ | √ | √ | √ | — | √ |

1. The internal reset generation is enabled in the initial state.

Table 39.19 List of Error Inputs of E2M (1/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | Dual Core Lock-step | DCLS compare error (PE0) | √ | √ | √ | √ | √ | √ | √ | √ |
| 1 |  | DCLS compare error (PE1) | √ | √ | √ | √ | √ | √ | √ | √ |
| 2 |  | Reserve | — | — | — | — | — | — | — | — |
| 3 |  | Reserve | — | — | — | — | — | — | — | — |
| 4 |  | Reserve | — | — | — | — | — | — | — | — |
| 5 |  | Reserve | — | — | — | — | — | — | — | — |
| 6 |  | Reserve | — | — | — | — | — | — | — | — |
| 7 |  | Reserve | — | — | — | — | — | — | — | — |
| 8 | Watchdog timer | Watchdog timer ch0 error (PE0) | √ | √ | √ | √[\*](#Note1_E2M)[1](#Note1_E2M) | √ | √ | — | √ |
| 9 |  | Watchdog timer ch1 error (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 10 |  | Reserve | — | — | — | — | — | — | — | — |
| 11 |  | Reserve | — | — | — | — | — | — | — | — |
| 12 |  | Reserve | — | — | — | — | — | — | — | — |
| 13 |  | Reserve | — | — | — | — | — | — | — | — |
| 14 |  | Reserve | — | — | — | — | — | — | — | — |
| 15 |  | Reserve | — | — | — | — | — | — | — | — |
| 16 | Local RAM  (own core) | Local RAM (PE0)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 17 |  | Local RAM (PE1)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 18 |  | Reserve | — | — | — | — | — | — | — | — |
| 19 |  | Reserve | — | — | — | — | — | — | — | — |
| 20 |  | Reserve | — | — | — | — | — | — | — | — |
| 21 |  | Reserve | — | — | — | — | — | — | — | — |
| 22 |  | Reserve | — | — | — | — | — | — | — | — |
| 23 |  | Reserve | — | — | — | — | — | — | — | — |
| 24 |  | Local RAM ECC (PE0)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 25 |  | Local RAM ECC (PE1)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 26 |  | Reserve | — | — | — | — | — | — | — | — |
| 27 |  | Reserve | — | — | — | — | — | — | — | — |
| 28 |  | Reserve | — | — | — | — | — | — | — | — |
| 29 |  | Reserve | — | — | — | — | — | — | — | — |
| 30 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.19 List of Error Inputs of E2M (2/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | Local RAM  (own core) | Reserve | — | — | — | — | — | — | — | — |
| 32 |  | Local RAM ECC (PE0)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 33 |  | Local RAM ECC (PE1)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 34 |  | Reserve | — | — | — | — | — | — | — | — |
| 35 |  | Reserve | — | — | — | — | — | — | — | — |
| 36 |  | Reserve | — | — | — | — | — | — | — | — |
| 37 |  | Reserve | — | — | — | — | — | — | — | — |
| 38 |  | Reserve | — | — | — | — | — | — | — | — |
| 39 |  | Reserve | — | — | — | — | — | — | — | — |
| 40 |  | Local RAM ECC (PE0)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 41 |  | Local RAM ECC (PE1)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 42 |  | Reserve | — | — | — | — | — | — | — | — |
| 43 |  | Reserve | — | — | — | — | — | — | — | — |
| 44 |  | Reserve | — | — | — | — | — | — | — | — |
| 45 |  | Reserve | — | — | — | — | — | — | — | — |
| 46 |  | Reserve | — | — | — | — | — | — | — | — |
| 47 |  | Reserve | — | — | — | — | — | — | — | — |
| 48 | Instruction Cache RAM | Instruction Cache RAM (PE0)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 49 |  | Instruction Cache RAM (PE1)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 50 |  | Reserve | — | — | — | — | — | — | — | — |
| 51 |  | Reserve | — | — | — | — | — | — | — | — |
| 52 |  | Reserve | — | — | — | — | — | — | — | — |
| 53 |  | Reserve | — | — | — | — | — | — | — | — |
| 54 |  | Reserve | — | — | — | — | — | — | — | — |
| 55 |  | Reserve | — | — | — | — | — | — | — | — |
| 56 |  | Instruction Cache RAM EDC (PE0)  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 57 |  | Instruction Cache RAM EDC (PE1)  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 58 |  | Reserve | — | — | — | — | — | — | — | — |
| 59 |  | Reserve | — | — | — | — | — | — | — | — |
| 60 |  | Reserve | — | — | — | — | — | — | — | — |
| 61 |  | Reserve | — | — | — | — | — | — | — | — |
| 62 |  | Reserve | — | — | — | — | — | — | — | — |
| 63 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.19 List of Error Inputs of E2M (3/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 64 | Instruction Cache RAM | Reserve | — | — | — | — | — | — | — | — |
| 65 |  | Reserve | — | — | — | — | — | — | — | — |
| 66 |  | Reserve | — | — | — | — | — | — | — | — |
| 67 |  | Reserve | — | — | — | — | — | — | — | — |
| 68 |  | Reserve | — | — | — | — | — | — | — | — |
| 69 |  | Reserve | — | — | — | — | — | — | — | — |
| 70 |  | Reserve | — | — | — | — | — | — | — | — |
| 71 |  | Reserve | — | — | — | — | — | — | — | — |
| 72 | Reserve |  | — | — | — | — | — | — | — | — |
| 73 | Reserve |  | — | — | — | — | — | — | — | — |
| 74 | Reserve |  | — | — | — | — | — | — | — | — |
| 75 | Reserve |  | — | — | — | — | — | — | — | — |
| 76 | Reserve |  | — | — | — | — | — | — | — | — |
| 77 | Reserve |  | — | — | — | — | — | — | — | — |
| 78 | Reserve |  | — | — | — | — | — | — | — | — |
| 79 | Reserve |  | — | — | — | — | — | — | — | — |
| 80 | PE guard function (PEG) | PEG error (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 81 |  | PEG error (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 82 |  | Reserve | — | — | — | — | — | — | — | — |
| 83 |  | Reserve | — | — | — | — | — | — | — | — |
| 84 |  | Reserve | — | — | — | — | — | — | — | — |
| 85 |  | Reserve | — | — | — | — | — | — | — | — |
| 86 |  | Reserve | — | — | — | — | — | — | — | — |
| 87 |  | Reserve | — | — | — | — | — | — | — | — |
| 88 | Clock Monitor | Clock monitor error (CLMA5) (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 89 |  | Clock monitor error (CLMA6) (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 90 |  | Reserve | — | — | — | — | — | — | — | — |
| 91 |  | Reserve | — | — | — | — | — | — | — | — |
| 92 |  | Reserve | — | — | — | — | — | — | — | — |
| 93 |  | Reserve | — | — | — | — | — | — | — | — |
| 94 |  | Reserve | — | — | — | — | — | — | — | — |
| 95 |  | Reserve | — | — | — | — | — | — | — | — |
| 96 | OSTM | OSTM1 Interrupt | √ | √ | √ | √ | √ | √ | — | √ |
| 97 |  | OSTM2 Interrupt | √ | √ | √ | √ | √ | √ | — | √ |
| 98 |  | Reserve | — | — | — | — | — | — | — | — |
| 99 |  | Reserve | — | — | — | — | — | — | — | — |
| 100 |  | Reserve | — | — | — | — | — | — | — | — |
| 101 |  | Reserve | — | — | — | — | — | — | — | — |
| 102 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.19 List of Error Inputs of E2M (4/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 103 | Reserve |  | — | — | — | — | — | — | — | — |
| 104 | Reserve |  | — | — | — | — | — | — | — | — |
| 105 | Reserve |  | — | — | — | — | — | — | — | — |
| 106 | Reserve |  | — | — | — | — | — | — | — | — |
| 107 | Reserve |  | — | — | — | — | — | — | — | — |
| 108 | Reserve |  | — | — | — | — | — | — | — | — |
| 109 | Reserve |  | — | — | — | — | — | — | — | — |
| 110 | Reserve |  | — | — | — | — | — | — | — | — |
| 111 | Reserve |  | — | — | — | — | — | — | — | — |
| 112 | Mode Error | Unintended Debug Enable detection (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 113 |  | Unintended Debug Enable detection (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 114 |  | Reserve | — | — | — | — | — | — | — | — |
| 115 |  | Reserve | — | — | — | — | — | — | — | — |
| 116 |  | Reserve | — | — | — | — | — | — | — | — |
| 117 |  | Reserve | — | — | — | — | — | — | — | — |
| 118 |  | Reserve | — | — | — | — | — | — | — | — |
| 119 |  | Reserve | — | — | — | — | — | — | — | — |
| 120 | PEG error | PEG error (PE0) Detected in a read request from PE0 to the others LRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 121 |  | PEG error (PE1) Detected in a read request from PE1 to the others LRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 122 |  | Reserve | — | — | — | — | — | — | — | — |
| 123 |  | Reserve | — | — | — | — | — | — | — | — |
| 124 |  | Reserve | — | — | — | — | — | — | — | — |
| 125 |  | Reserve | — | — | — | — | — | — | — | — |
| 126 |  | Reserve | — | — | — | — | — | — | — | — |
| 127 |  | Reserve | — | — | — | — | — | — | — | — |
| 128 | Reserve |  | — | — | — | — | — | — | — | — |
| 129 | Reserve |  | — | — | — | — | — | — | — | — |
| 130 | Reserve |  | — | — | — | — | — | — | — | — |
| 131 | Reserve |  | — | — | — | — | — | — | — | — |
| 132 | Reserve |  | — | — | — | — | — | — | — | — |
| 133 | Reserve |  | — | — | — | — | — | — | — | — |
| 134 | Reserve |  | — | — | — | — | — | — | — | — |
| 135 | Reserve |  | — | — | — | — | — | — | — | — |
| 136 | Reserve |  | — | — | — | — | — | — | — | — |
| 137 | Reserve |  | — | — | — | — | — | — | — | — |
| 138 | Reserve |  | — | — | — | — | — | — | — | — |
| 139 | Reserve |  | — | — | — | — | — | — | — | — |
| 140 | Reserve |  | — | — | — | — | — | — | — | — |

Table 39.19 List of Error Inputs of E2M (5/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 141 | Reserve |  | — | — | — | — | — | — | — | — |
| 142 | Reserve |  | — | — | — | — | — | — | — | — |
| 143 | Reserve |  | — | — | — | — | — | — | — | — |
| 144 | Reserve |  | — | — | — | — | — | — | — | — |
| 145 | Reserve |  | — | — | — | — | — | — | — | — |
| 146 | Reserve |  | — | — | — | — | — | — | — | — |
| 147 | Reserve |  | — | — | — | — | — | — | — | — |
| 148 | Reserve |  | — | — | — | — | — | — | — | — |
| 149 | Reserve |  | — | — | — | — | — | — | — | — |
| 150 | Reserve |  | — | — | — | — | — | — | — | — |
| 151 | Reserve |  | — | — | — | — | — | — | — | — |
| 152 | Cluster RAM | Cluster RAM  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 153 |  | Cluster RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 154 |  | Cluster RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 155 |  | Cluster RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 156 |  | Reserve | — | — | — | — | — | — | — | — |
| 157 |  | Reserve | — | — | — | — | — | — | — | — |
| 158 |  | Reserve | — | — | — | — | — | — | — | — |
| 159 |  | Reserve | — | — | — | — | — | — | — | — |
| 160 | Local RAM  (other core) | Reserve | — | — | — | — | — | — | — | — |
| 161 |  | LRAM (error by other core access)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 162 |  | LRAM (error by other core access)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 163 |  | LRAM (error by other core access)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 164 | sDMA | sDMAC0 RAM  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 165 |  | sDMAC0 RAM  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 166 |  | sDMAC1 RAM  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 167 |  | sDMAC1 RAM  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |

Table 39.19 List of Error Inputs of E2M (6/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 168 | Peripheral RAM | Peripheral (DTS) RAM ECC  - ECC 2bit error  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 169 |  | Peripheral (DTS) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 170 |  | Peripheral (DTS) RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 171 |  | Peripheral(except DTS) RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 172 |  | Peripheral(FlexRay) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 173 |  | Peripheral(FlexRay) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 174 |  | Peripheral(CAN) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 175 |  | Peripheral(CAN) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 176 |  | Peripheral(DFE) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 177 |  | Peripheral(DFE) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 178 |  | Peripheral(GTM) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 179 |  | Peripheral(GTM) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 180 |  | Peripheral(Ethernet) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 181 |  | Peripheral(Ethernet) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 182 |  | Reserve | — | — | — | — | — | — | — | — |
| 183 |  | Reserve | — | — | — | — | — | — | — | — |
| 184 |  | Reserve | — | — | — | — | — | — | — | — |
| 185 |  | Reserve | — | — | — | — | — | — | — | — |
| 186 |  | Reserve | — | — | — | — | — | — | — | — |
| 187 |  | Reserve | — | — | — | — | — | — | — | — |
| 188 |  | Reserve | — | — | — | — | — | — | — | — |
| 189 |  | Reserve | — | — | — | — | — | — | — | — |
| 190 |  | Reserve | — | — | — | — | — | — | — | — |
| 191 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.19 List of Error Inputs of E2M (7/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 192 | Peripheral RAM | Reserve | — | — | — | — | — | — | — | — |
| 193 |  | Reserve | — | — | — | — | — | — | — | — |
| 194 |  | Reserve | — | — | — | — | — | — | — | — |
| 195 |  | Reserve | — | — | — | — | — | — | — | — |
| 196 |  | Reserve | — | — | — | — | — | — | — | — |
| 197 |  | Reserve | — | — | — | — | — | — | — | — |
| 198 |  | Reserve | — | — | — | — | — | — | — | — |
| 199 |  | Reserve | — | — | — | — | — | — | — | — |
| 200 | Code Flash | Code Flash  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 201 |  | Code Flash ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 202 |  | Code Flash ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 203 |  | Code Flash ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 204 |  | Reserve | — | — | — | — | — | — | — | — |
| 205 |  | Reserve | — | — | — | — | — | — | — | — |
| 206 |  | Reserve | — | — | — | — | — | — | — | — |
| 207 |  | Reserve | — | — | — | — | — | — | — | — |
| 208 | Data Flash | Data Flash ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 209 |  | Data Flash ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 210 |  | Data Flash ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 211 |  | Reserve | — | — | — | — | — | — | — | — |
| 212 |  | Reserve | — | — | — | — | — | — | — | — |
| 213 |  | Reserve | — | — | — | — | — | — | — | — |
| 214 |  | Reserve | — | — | — | — | — | — | — | — |
| 215 |  | Reserve | — | — | — | — | — | — | — | — |
| 216 | Bus ECC | Data Bus ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 217 |  | Data Bus ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 218 |  | Address Bus ECC  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 219 |  | Reserve | — | — | — | — | — | — | — | — |
| 220 |  | Reserve | — | — | — | — | — | — | — | — |
| 221 |  | Reserve | — | — | — | — | — | — | — | — |
| 222 |  | Reserve | — | — | — | — | — | — | — | — |
| 223 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.19 List of Error Inputs of E2M (8/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 224 | Cluster RAM Guard (CRG) | CRAM Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 225 | P-Bus Guard (PBG) | P-Bus Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 226 | H-Bus Guard (HBG) | H-Bus Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 227 | I-Bus Guard (IBG) | I-Bus Guard error  (IPIR MEV Barrier TPTM) | √ | √ | √ | √ | √ | √ | — | √ |
| 228 | Reserve |  | — | — | — | — | — | — | — | — |
| 229 | Reserve |  | — | — | — | — | — | — | — | — |
| 230 | Reserve |  | — | — | — | — | — | — | — | — |
| 231 | Reserve |  | — | — | — | — | — | — | — | — |
| 232 | Clock Monitor | Clock monitor error (CLMA0) | √ | √ | √ | √ | √ | √ | — | √ |
| 233 |  | Clock monitor error (CLMA1) | √ | √ | √ | √ | √ | √ | — | √ |
| 234 |  | Clock monitor error (CLMA2) | √ | √ | √ | √ | √ | √ | — | √ |
| 235 |  | Clock monitor error (CLMA3) | √ | √ | √ | √ | √ | √ | — | √ |
| 236 |  | Clock monitor error (CLMA4) | √ | √ | √ | √ | √ | √ | — | √ |
| 237 | Reserve |  | — | — | — | — | — | — | — | — |
| 238 | Reserve |  | — | — | — | — | — | — | — | — |
| 239 | Reserve |  | — | — | — | — | — | — | — | — |
| 240 | DSADC  ADC  Cyclic ADC | AD parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 241 | MISG | MISG compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 242 | DTS | DTS compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 243 | External Error Input | ERRORIN | √ | √ | √ | √ | √ | √ | — | √ |
| 244 | Flash | Flash access error | √ | √ | √ | √ | √ | √ | — | √ |
| 245 |  | FACI reset transfer error | √ | — | — | — | √ | — | — | — |
| 246 |  | FBIST parameter transfer error | √ | — | — | — | √ | — | — | — |
| 247 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.19 List of Error Inputs of E2M (9/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 248 | Reserve |  | — | — | — | — | — | — | — | — |
| 249 | Reserve |  | — | — | — | — | — | — | — | — |
| 250 | Reserve |  | — | — | — | — | — | — | — | — |
| 251 | Reserve |  | — | — | — | — | — | — | — | — |
| 252 | Reserve |  | — | — | — | — | — | — | — | — |
| 253 | Reserve |  | — | — | — | — | — | — | — | — |
| 254 | Reserve |  | — | — | — | — | — | — | — | — |
| 255 | Reserve |  | — | — | — | — | — | — | — | — |
| 256 | Reserve |  | — | — | — | — | — | — | — | — |
| 257 | Reserve |  | — | — | — | — | — | — | — | — |
| 258 | Reserve |  | — | — | — | — | — | — | — | — |
| 259 | Reserve |  | — | — | — | — | — | — | — | — |
| 260 | Reserve |  | — | — | — | — | — | — | — | — |
| 261 | Reserve |  | — | — | — | — | — | — | — | — |
| 262 | Reserve |  | — | — | — | — | — | — | — | — |
| 263 | Reserve |  | — | — | — | — | — | — | — | — |
| 264 | Reserve |  | — | — | — | — | — | — | — | — |
| 265 | Reserve |  | — | — | — | — | — | — | — | — |
| 266 | Reserve |  | — | — | — | — | — | — | — | — |
| 267 | Reserve |  | — | — | — | — | — | — | — | — |
| 268 | Reserve |  | — | — | — | — | — | — | — | — |
| 269 | Reserve |  | — | — | — | — | — | — | — | — |
| 270 | Reserve |  | — | — | — | — | — | — | — | — |
| 271 | Reserve |  | — | — | — | — | — | — | — | — |
| 272 | Reserve |  | — | — | — | — | — | — | — | — |
| 273 | Reserve |  | — | — | — | — | — | — | — | — |
| 274 | Reserve |  | — | — | — | — | — | — | — | — |
| 275 | Reserve |  | — | — | — | — | — | — | — | — |
| 276 | Reserve |  | — | — | — | — | — | — | — | — |
| 277 | Reserve |  | — | — | — | — | — | — | — | — |
| 278 | Reserve |  | — | — | — | — | — | — | — | — |
| 279 | Reserve |  | — | — | — | — | — | — | — | — |
| 280 | Data Path Redundancy | DMA Comp error | √ | √ | √ | √ | √ | √ | — | √ |
| 281 |  | BUS Bridge Comp error | √ | √ | √ | √ | √ | √ | — | √ |

Table 39.19 List of Error Inputs of E2M (10/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 282 | BUS Routing checker | Inter-processor element Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 283 |  | Inter-cluster Bus (I-Bus) | √ | √ | √ | √ | √ | √ | — | √ |
| 284 |  | Peripheral Bus (P-Bus) | √ | √ | √ | √ | √ | √ | — | √ |
| 285 |  | CRAM Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 286 |  | System Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 287 |  | Global FLASH Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 288 |  | Local FLASH Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 289 |  | Reserve | — | — | — | — | — | — | — | — |
| 290 |  | Reserve | — | — | — | — | — | — | — | — |
| 291 |  | Reserve | — | — | — | — | — | — | — | — |
| 292 | Voltage Monitor | EVCC Secondary HDET | √ | √ | √ | √ | √ | √ | — | √ |
| 293 |  | EVCC Secondary LDET | √ | √ | √ | √ | √ | √ | — | √ |
| 294 |  | VCC Secondary HDET | √ | √ | √ | √ | √ | √ | — | √ |
| 295 |  | VCC Secondary LDET | √ | √ | √ | √ | √ | √ | — | √ |
| 296 |  | VDD Secondary HDET | √ | √ | √ | √ | √ | √ | — | √ |
| 297 |  | VDD Secondary LDET | √ | √ | √ | √ | √ | √ | — | √ |
| 298 |  | Reserve | — | — | — | — | — | — | — | — |
| 299 | Mode Error | Mode error  - Unintended activation of Production Test Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 300 |  | Mode error  - Unintended activation of Normal Operation Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 301 |  | Mode error  - Unintended deactivation of Normal Operation Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 302 |  | Mode error  - Unintended activation of Serial Programming Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 303 |  | Mode error  - Unintended activation of User Boot Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 304 |  | Mode error  - Unintended deactivation of User Boot Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 305 |  | Mode error  - Mode latch error | √ | √ | √ | √ | √ | √ | — | √ |
| 306 | Reserve |  | — | — | — | — | — | — | — | — |
| 307 | Reserve |  | — | — | — | — | — | — | — | — |
| 308 | ECM | ECM compare error | √ | √ | √ | √ | √ | √ | — | √ |

1. The internal reset generation is enabled in the initial state.

Table 39.20 List of Error Inputs of E2GM (1/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | Dual Core Lock-step | DCLS compare error (PE0) | √ | √ | √ | √ | √ | √ | √ | √ |
| 1 |  | DCLS compare error (PE1) | √ | √ | √ | √ | √ | √ | √ | √ |
| 2 |  | Reserve | — | — | — | — | — | — | — | — |
| 3 |  | Reserve | — | — | — | — | — | — | — | — |
| 4 |  | Reserve | — | — | — | — | — | — | — | — |
| 5 |  | Reserve | — | — | — | — | — | — | — | — |
| 6 |  | Reserve | — | — | — | — | — | — | — | — |
| 7 |  | Reserve | — | — | — | — | — | — | — | — |
| 8 | Watchdog timer | Watchdog timer ch0 error (PE0) | √ | √ | √ | √[\*](#Note1_E2GM)[1](#Note1_E2GM) | √ | √ | — | √ |
| 9 |  | Watchdog timer ch1 error (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 10 |  | Reserve | — | — | — | — | — | — | — | — |
| 11 |  | Reserve | — | — | — | — | — | — | — | — |
| 12 |  | Reserve | — | — | — | — | — | — | — | — |
| 13 |  | Reserve | — | — | — | — | — | — | — | — |
| 14 |  | Reserve | — | — | — | — | — | — | — | — |
| 15 |  | Reserve | — | — | — | — | — | — | — | — |
| 16 | Local RAM  (own core) | Local RAM (PE0)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 17 |  | Local RAM (PE1)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 18 |  | Reserve | — | — | — | — | — | — | — | — |
| 19 |  | Reserve | — | — | — | — | — | — | — | — |
| 20 |  | Reserve | — | — | — | — | — | — | — | — |
| 21 |  | Reserve | — | — | — | — | — | — | — | — |
| 22 |  | Reserve | — | — | — | — | — | — | — | — |
| 23 |  | Reserve | — | — | — | — | — | — | — | — |
| 24 |  | Local RAM ECC (PE0)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 25 |  | Local RAM ECC (PE1)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 26 |  | Reserve | — | — | — | — | — | — | — | — |
| 27 |  | Reserve | — | — | — | — | — | — | — | — |
| 28 |  | Reserve | — | — | — | — | — | — | — | — |
| 29 |  | Reserve | — | — | — | — | — | — | — | — |
| 30 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.20 List of Error Inputs of E2GM (2/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | Local RAM  (own core) | Reserve | — | — | — | — | — | — | — | — |
| 32 |  | Local RAM ECC (PE0)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 33 |  | Local RAM ECC (PE1)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 34 |  | Reserve | — | — | — | — | — | — | — | — |
| 35 |  | Reserve | — | — | — | — | — | — | — | — |
| 36 |  | Reserve | — | — | — | — | — | — | — | — |
| 37 |  | Reserve | — | — | — | — | — | — | — | — |
| 38 |  | Reserve | — | — | — | — | — | — | — | — |
| 39 |  | Reserve | — | — | — | — | — | — | — | — |
| 40 |  | Local RAM ECC (PE0)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 41 |  | Local RAM ECC (PE1)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 42 |  | Reserve | — | — | — | — | — | — | — | — |
| 43 |  | Reserve | — | — | — | — | — | — | — | — |
| 44 |  | Reserve | — | — | — | — | — | — | — | — |
| 45 |  | Reserve | — | — | — | — | — | — | — | — |
| 46 |  | Reserve | — | — | — | — | — | — | — | — |
| 47 |  | Reserve | — | — | — | — | — | — | — | — |
| 48 | Instruction Cache RAM | Instruction Cache RAM (PE0)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 49 |  | Instruction Cache RAM (PE1)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 50 |  | Reserve | — | — | — | — | — | — | — | — |
| 51 |  | Reserve | — | — | — | — | — | — | — | — |
| 52 |  | Reserve | — | — | — | — | — | — | — | — |
| 53 |  | Reserve | — | — | — | — | — | — | — | — |
| 54 |  | Reserve | — | — | — | — | — | — | — | — |
| 55 |  | Reserve | — | — | — | — | — | — | — | — |
| 56 |  | Instruction Cache RAM EDC (PE0)  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 57 |  | Instruction Cache RAM EDC (PE1)  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 58 |  | Reserve | — | — | — | — | — | — | — | — |
| 59 |  | Reserve | — | — | — | — | — | — | — | — |
| 60 |  | Reserve | — | — | — | — | — | — | — | — |
| 61 |  | Reserve | — | — | — | — | — | — | — | — |
| 62 |  | Reserve | — | — | — | — | — | — | — | — |
| 63 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.20 List of Error Inputs of E2GM (3/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 64 | Instruction Cache RAM | Reserve | — | — | — | — | — | — | — | — |
| 65 |  | Reserve | — | — | — | — | — | — | — | — |
| 66 |  | Reserve | — | — | — | — | — | — | — | — |
| 67 |  | Reserve | — | — | — | — | — | — | — | — |
| 68 |  | Reserve | — | — | — | — | — | — | — | — |
| 69 |  | Reserve | — | — | — | — | — | — | — | — |
| 70 |  | Reserve | — | — | — | — | — | — | — | — |
| 71 |  | Reserve | — | — | — | — | — | — | — | — |
| 72 | Reserve |  | — | — | — | — | — | — | — | — |
| 73 | Reserve |  | — | — | — | — | — | — | — | — |
| 74 | Reserve |  | — | — | — | — | — | — | — | — |
| 75 | Reserve |  | — | — | — | — | — | — | — | — |
| 76 | Reserve |  | — | — | — | — | — | — | — | — |
| 77 | Reserve |  | — | — | — | — | — | — | — | — |
| 78 | Reserve |  | — | — | — | — | — | — | — | — |
| 79 | Reserve |  | — | — | — | — | — | — | — | — |
| 80 | PE guard function (PEG) | PEG error (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 81 |  | PEG error (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 82 |  | Reserve | — | — | — | — | — | — | — | — |
| 83 |  | Reserve | — | — | — | — | — | — | — | — |
| 84 |  | Reserve | — | — | — | — | — | — | — | — |
| 85 |  | Reserve | — | — | — | — | — | — | — | — |
| 86 |  | Reserve | — | — | — | — | — | — | — | — |
| 87 |  | Reserve | — | — | — | — | — | — | — | — |
| 88 | Clock Monitor | Clock monitor error (CLMA5) (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 89 |  | Clock monitor error (CLMA6) (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 90 |  | Reserve | — | — | — | — | — | — | — | — |
| 91 |  | Reserve | — | — | — | — | — | — | — | — |
| 92 |  | Reserve | — | — | — | — | — | — | — | — |
| 93 |  | Reserve | — | — | — | — | — | — | — | — |
| 94 |  | Reserve | — | — | — | — | — | — | — | — |
| 95 |  | Reserve | — | — | — | — | — | — | — | — |
| 96 | OSTM | OSTM1 Interrupt | √ | √ | √ | √ | √ | √ | — | √ |
| 97 |  | OSTM2 Interrupt | √ | √ | √ | √ | √ | √ | — | √ |
| 98 |  | Reserve | — | — | — | — | — | — | — | — |
| 99 |  | Reserve | — | — | — | — | — | — | — | — |
| 100 |  | Reserve | — | — | — | — | — | — | — | — |
| 101 |  | Reserve | — | — | — | — | — | — | — | — |
| 102 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.20 List of Error Inputs of E2GM (4/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 103 | Reserve |  | — | — | — | — | — | — | — | — |
| 104 | Reserve |  | — | — | — | — | — | — | — | — |
| 105 | Reserve |  | — | — | — | — | — | — | — | — |
| 106 | Reserve |  | — | — | — | — | — | — | — | — |
| 107 | Reserve |  | — | — | — | — | — | — | — | — |
| 108 | Reserve |  | — | — | — | — | — | — | — | — |
| 109 | Reserve |  | — | — | — | — | — | — | — | — |
| 110 | Reserve |  | — | — | — | — | — | — | — | — |
| 111 | Reserve |  | — | — | — | — | — | — | — | — |
| 112 | Mode Error | Unintended Debug Enable detection (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 113 |  | Unintended Debug Enable detection (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 114 |  | Reserve | — | — | — | — | — | — | — | — |
| 115 |  | Reserve | — | — | — | — | — | — | — | — |
| 116 |  | Reserve | — | — | — | — | — | — | — | — |
| 117 |  | Reserve | — | — | — | — | — | — | — | — |
| 118 |  | Reserve | — | — | — | — | — | — | — | — |
| 119 |  | Reserve | — | — | — | — | — | — | — | — |
| 120 | PEG error | PEG error (PE0) Detected in a read request from PE0 to the others LRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 121 |  | PEG error (PE1) Detected in a read request from PE1 to the others LRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 122 |  | Reserve | — | — | — | — | — | — | — | — |
| 123 |  | Reserve | — | — | — | — | — | — | — | — |
| 124 |  | Reserve | — | — | — | — | — | — | — | — |
| 125 |  | Reserve | — | — | — | — | — | — | — | — |
| 126 |  | Reserve | — | — | — | — | — | — | — | — |
| 127 |  | Reserve | — | — | — | — | — | — | — | — |
| 128 | Reserve |  | — | — | — | — | — | — | — | — |
| 129 | Reserve |  | — | — | — | — | — | — | — | — |
| 130 | Reserve |  | — | — | — | — | — | — | — | — |
| 131 | Reserve |  | — | — | — | — | — | — | — | — |
| 132 | Reserve |  | — | — | — | — | — | — | — | — |
| 133 | Reserve |  | — | — | — | — | — | — | — | — |
| 134 | Reserve |  | — | — | — | — | — | — | — | — |
| 135 | Reserve |  | — | — | — | — | — | — | — | — |
| 136 | Reserve |  | — | — | — | — | — | — | — | — |
| 137 | Reserve |  | — | — | — | — | — | — | — | — |
| 138 | Reserve |  | — | — | — | — | — | — | — | — |
| 139 | Reserve |  | — | — | — | — | — | — | — | — |
| 140 | Reserve |  | — | — | — | — | — | — | — | — |

Table 39.20 List of Error Inputs of E2GM (5/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 141 | Reserve |  | — | — | — | — | — | — | — | — |
| 142 | Reserve |  | — | — | — | — | — | — | — | — |
| 143 | Reserve |  | — | — | — | — | — | — | — | — |
| 144 | Reserve |  | — | — | — | — | — | — | — | — |
| 145 | Reserve |  | — | — | — | — | — | — | — | — |
| 146 | Reserve |  | — | — | — | — | — | — | — | — |
| 147 | Reserve |  | — | — | — | — | — | — | — | — |
| 148 | Reserve |  | — | — | — | — | — | — | — | — |
| 149 | Reserve |  | — | — | — | — | — | — | — | — |
| 150 | Reserve |  | — | — | — | — | — | — | — | — |
| 151 | Reserve |  | — | — | — | — | — | — | — | — |
| 152 | Cluster RAM | Cluster RAM  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 153 |  | Cluster RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 154 |  | Cluster RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 155 |  | Cluster RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 156 |  | Reserve | — | — | — | — | — | — | — | — |
| 157 |  | Reserve | — | — | — | — | — | — | — | — |
| 158 |  | Reserve | — | — | — | — | — | — | — | — |
| 159 |  | Reserve | — | — | — | — | — | — | — | — |
| 160 | Local RAM  (other core) | Reserve | — | — | — | — | — | — | — | — |
| 161 |  | LRAM (error by other core access)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 162 |  | LRAM (error by other core access)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 163 |  | LRAM (error by other core access)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 164 | sDMA | sDMAC0 RAM  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 165 |  | sDMAC0 RAM  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 166 |  | sDMAC1 RAM  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 167 |  | sDMAC1 RAM  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |

Table 39.20 List of Error Inputs of E2GM (6/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 168 | Peripheral RAM | Peripheral (DTS) RAM ECC  - ECC 2bit error  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 169 |  | Peripheral (DTS) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 170 |  | Peripheral (DTS) RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 171 |  | Peripheral(except DTS) RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 172 |  | Reserve | — | — | — | — | — | — | — | — |
| 173 |  | Reserve | — | — | — | — | — | — | — | — |
| 174 |  | Peripheral(CAN) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 175 |  | Peripheral(CAN) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 176 |  | Peripheral(DFE) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 177 |  | Peripheral(DFE) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 178 |  | Peripheral(GTM) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 179 |  | Peripheral(GTM) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 180 |  | Reserve | — | — | — | — | — | — | — | — |
| 181 |  | Reserve | — | — | — | — | — | — | — | — |
| 182 |  | Reserve | — | — | — | — | — | — | — | — |
| 183 |  | Reserve | — | — | — | — | — | — | — | — |
| 184 |  | Reserve | — | — | — | — | — | — | — | — |
| 185 |  | Reserve | — | — | — | — | — | — | — | — |
| 186 |  | Reserve | — | — | — | — | — | — | — | — |
| 187 |  | Reserve | — | — | — | — | — | — | — | — |
| 188 |  | Reserve | — | — | — | — | — | — | — | — |
| 189 |  | Reserve | — | — | — | — | — | — | — | — |
| 190 |  | Reserve | — | — | — | — | — | — | — | — |
| 191 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.20 List of Error Inputs of E2GM (7/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 192 | Peripheral RAM | Reserve | — | — | — | — | — | — | — | — |
| 193 |  | Reserve | — | — | — | — | — | — | — | — |
| 194 |  | Reserve | — | — | — | — | — | — | — | — |
| 195 |  | Reserve | — | — | — | — | — | — | — | — |
| 196 |  | Reserve | — | — | — | — | — | — | — | — |
| 197 |  | Reserve | — | — | — | — | — | — | — | — |
| 198 |  | Reserve | — | — | — | — | — | — | — | — |
| 199 |  | Reserve | — | — | — | — | — | — | — | — |
| 200 | Code Flash | Code Flash  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 201 |  | Code Flash ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 202 |  | Code Flash ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 203 |  | Code Flash ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 204 |  | Reserve | — | — | — | — | — | — | — | — |
| 205 |  | Reserve | — | — | — | — | — | — | — | — |
| 206 |  | Reserve | — | — | — | — | — | — | — | — |
| 207 |  | Reserve | — | — | — | — | — | — | — | — |
| 208 | Data Flash | Data Flash ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 209 |  | Data Flash ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 210 |  | Data Flash ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 211 |  | Reserve | — | — | — | — | — | — | — | — |
| 212 |  | Reserve | — | — | — | — | — | — | — | — |
| 213 |  | Reserve | — | — | — | — | — | — | — | — |
| 214 |  | Reserve | — | — | — | — | — | — | — | — |
| 215 |  | Reserve | — | — | — | — | — | — | — | — |
| 216 | Bus ECC | Data Bus ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 217 |  | Data Bus ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 218 |  | Address Bus ECC  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 219 |  | Reserve | — | — | — | — | — | — | — | — |
| 220 |  | Reserve | — | — | — | — | — | — | — | — |
| 221 |  | Reserve | — | — | — | — | — | — | — | — |
| 222 |  | Reserve | — | — | — | — | — | — | — | — |
| 223 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.20 List of Error Inputs of E2GM (8/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 224 | Cluster RAM Guard (CRG) | CRAM Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 225 | P-Bus Guard (PBG) | P-Bus Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 226 | Reserve |  | — | — | — | — | — | — | — | — |
| 227 | I-Bus Guard (IBG) | I-Bus Guard error  (IPIR MEV Barrier TPTM) | √ | √ | √ | √ | √ | √ | — | √ |
| 228 | Reserve |  | — | — | — | — | — | — | — | — |
| 229 | Reserve |  | — | — | — | — | — | — | — | — |
| 230 | Reserve |  | — | — | — | — | — | — | — | — |
| 231 | Reserve |  | — | — | — | — | — | — | — | — |
| 232 | Clock Monitor | Clock monitor error (CLMA0) | √ | √ | √ | √ | √ | √ | — | √ |
| 233 |  | Clock monitor error (CLMA1) | √ | √ | √ | √ | √ | √ | — | √ |
| 234 |  | Clock monitor error (CLMA2) | √ | √ | √ | √ | √ | √ | — | √ |
| 235 |  | Clock monitor error (CLMA3) | √ | √ | √ | √ | √ | √ | — | √ |
| 236 |  | Clock monitor error (CLMA4) | √ | √ | √ | √ | √ | √ | — | √ |
| 237 | Reserve |  | — | — | — | — | — | — | — | — |
| 238 | Reserve |  | — | — | — | — | — | — | — | — |
| 239 | Reserve |  | — | — | — | — | — | — | — | — |
| 240 | DSADC  ADC  Cyclic ADC | AD parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 241 | MISG | MISG compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 242 | DTS | DTS compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 243 | External Error Input | ERRORIN | √ | √ | √ | √ | √ | √ | — | √ |
| 244 | Flash | Flash access error | √ | √ | √ | √ | √ | √ | — | √ |
| 245 |  | FACI reset transfer error | √ | — | — | — | √ | — | — | — |
| 246 |  | FBIST parameter transfer error | √ | — | — | — | √ | — | — | — |
| 247 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.20 List of Error Inputs of E2GM (9/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 248 | Reserve |  | — | — | — | — | — | — | — | — |
| 249 | Reserve |  | — | — | — | — | — | — | — | — |
| 250 | Reserve |  | — | — | — | — | — | — | — | — |
| 251 | Reserve |  | — | — | — | — | — | — | — | — |
| 252 | Reserve |  | — | — | — | — | — | — | — | — |
| 253 | Reserve |  | — | — | — | — | — | — | — | — |
| 254 | Reserve |  | — | — | — | — | — | — | — | — |
| 255 | Reserve |  | — | — | — | — | — | — | — | — |
| 256 | Reserve |  | — | — | — | — | — | — | — | — |
| 257 | Reserve |  | — | — | — | — | — | — | — | — |
| 258 | Reserve |  | — | — | — | — | — | — | — | — |
| 259 | Reserve |  | — | — | — | — | — | — | — | — |
| 260 | Reserve |  | — | — | — | — | — | — | — | — |
| 261 | Reserve |  | — | — | — | — | — | — | — | — |
| 262 | Reserve |  | — | — | — | — | — | — | — | — |
| 263 | Reserve |  | — | — | — | — | — | — | — | — |
| 264 | Reserve |  | — | — | — | — | — | — | — | — |
| 265 | Reserve |  | — | — | — | — | — | — | — | — |
| 266 | Reserve |  | — | — | — | — | — | — | — | — |
| 267 | Reserve |  | — | — | — | — | — | — | — | — |
| 268 | Reserve |  | — | — | — | — | — | — | — | — |
| 269 | Reserve |  | — | — | — | — | — | — | — | — |
| 270 | Reserve |  | — | — | — | — | — | — | — | — |
| 271 | Reserve |  | — | — | — | — | — | — | — | — |
| 272 | Reserve |  | — | — | — | — | — | — | — | — |
| 273 | Reserve |  | — | — | — | — | — | — | — | — |
| 274 | Reserve |  | — | — | — | — | — | — | — | — |
| 275 | Reserve |  | — | — | — | — | — | — | — | — |
| 276 | Reserve |  | — | — | — | — | — | — | — | — |
| 277 | Reserve |  | — | — | — | — | — | — | — | — |
| 278 | Reserve |  | — | — | — | — | — | — | — | — |
| 279 | Reserve |  | — | — | — | — | — | — | — | — |
| 280 | Data Path Redundancy | DMA Comp error | √ | √ | √ | √ | √ | √ | — | √ |
| 281 |  | BUS Bridge Comp error | √ | √ | √ | √ | √ | √ | — | √ |

Table 39.20 List of Error Inputs of E2GM (10/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 282 | BUS Routing checker | Inter-processor element Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 283 |  | Inter-cluster Bus (I-Bus) | √ | √ | √ | √ | √ | √ | — | √ |
| 284 |  | Peripheral Bus (P-Bus) | √ | √ | √ | √ | √ | √ | — | √ |
| 285 |  | CRAM Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 286 |  | System Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 287 |  | Global FLASH Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 288 |  | Local FLASH Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 289 |  | Reserve | — | — | — | — | — | — | — | — |
| 290 |  | Reserve | — | — | — | — | — | — | — | — |
| 291 |  | Reserve | — | — | — | — | — | — | — | — |
| 292 | Reserve |  | — | — | — | — | — | — | — | — |
| 293 | Reserve |  | — | — | — | — | — | — | — | — |
| 294 | Reserve |  | — | — | — | — | — | — | — | — |
| 295 | Reserve |  | — | — | — | — | — | — | — | — |
| 296 | Reserve |  | — | — | — | — | — | — | — | — |
| 297 | Reserve |  | — | — | — | — | — | — | — | — |
| 298 | Reserve |  | — | — | — | — | — | — | — | — |
| 299 | Mode Error | Mode error  - Unintended activation of Production Test Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 300 |  | Mode error  - Unintended activation of Normal Operation Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 301 |  | Mode error  - Unintended deactivation of Normal Operation Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 302 |  | Mode error  - Unintended activation of Serial Programming Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 303 |  | Mode error  - Unintended activation of User Boot Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 304 |  | Mode error  - Unintended deactivation of User Boot Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 305 |  | Mode error  - Mode latch error | √ | √ | √ | √ | √ | √ | — | √ |
| 306 | Reserve |  | — | — | — | — | — | — | — | — |
| 307 | Reserve |  | — | — | — | — | — | — | — | — |
| 308 | ECM | ECM compare error | √ | √ | √ | √ | √ | √ | — | √ |

1. The internal reset generation is enabled in the initial state.

Table 39.21 List of Error Inputs of E2L (1/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | Dual Core Lock-step | DCLS compare error (PE0) | √ | √ | √ | √ | √ | √ | √ | √ |
| 1 |  | DCLS compare error (PE1) | √ | √ | √ | √ | √ | √ | √ | √ |
| 2 |  | Reserve | — | — | — | — | — | — | — | — |
| 3 |  | Reserve | — | — | — | — | — | — | — | — |
| 4 |  | Reserve | — | — | — | — | — | — | — | — |
| 5 |  | Reserve | — | — | — | — | — | — | — | — |
| 6 |  | Reserve | — | — | — | — | — | — | — | — |
| 7 |  | Reserve | — | — | — | — | — | — | — | — |
| 8 | Watchdog timer | Watchdog timer ch0 error (PE0) | √ | √ | √ | √[\*](#Note1_E2L)[1](#Note1_E2L) | √ | √ | — | √ |
| 9 |  | Watchdog timer ch1 error (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 10 |  | Reserve | — | — | — | — | — | — | — | — |
| 11 |  | Reserve | — | — | — | — | — | — | — | — |
| 12 |  | Reserve | — | — | — | — | — | — | — | — |
| 13 |  | Reserve | — | — | — | — | — | — | — | — |
| 14 |  | Reserve | — | — | — | — | — | — | — | — |
| 15 |  | Reserve | — | — | — | — | — | — | — | — |
| 16 | Local RAM  (own core) | Local RAM (PE0)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 17 |  | Local RAM (PE1)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 18 |  | Reserve | — | — | — | — | — | — | — | — |
| 19 |  | Reserve | — | — | — | — | — | — | — | — |
| 20 |  | Reserve | — | — | — | — | — | — | — | — |
| 21 |  | Reserve | — | — | — | — | — | — | — | — |
| 22 |  | Reserve | — | — | — | — | — | — | — | — |
| 23 |  | Reserve | — | — | — | — | — | — | — | — |
| 24 |  | Local RAM ECC (PE0)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 25 |  | Local RAM ECC (PE1)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 26 |  | Reserve | — | — | — | — | — | — | — | — |
| 27 |  | Reserve | — | — | — | — | — | — | — | — |
| 28 |  | Reserve | — | — | — | — | — | — | — | — |
| 29 |  | Reserve | — | — | — | — | — | — | — | — |
| 30 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.21 List of Error Inputs of E2L (2/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | Local RAM  (own core) | Reserve | — | — | — | — | — | — | — | — |
| 32 |  | Local RAM ECC (PE0)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 33 |  | Local RAM ECC (PE1)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 34 |  | Reserve | — | — | — | — | — | — | — | — |
| 35 |  | Reserve | — | — | — | — | — | — | — | — |
| 36 |  | Reserve | — | — | — | — | — | — | — | — |
| 37 |  | Reserve | — | — | — | — | — | — | — | — |
| 38 |  | Reserve | — | — | — | — | — | — | — | — |
| 39 |  | Reserve | — | — | — | — | — | — | — | — |
| 40 |  | Local RAM ECC (PE0)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 41 |  | Local RAM ECC (PE1)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 42 |  | Reserve | — | — | — | — | — | — | — | — |
| 43 |  | Reserve | — | — | — | — | — | — | — | — |
| 44 |  | Reserve | — | — | — | — | — | — | — | — |
| 45 |  | Reserve | — | — | — | — | — | — | — | — |
| 46 |  | Reserve | — | — | — | — | — | — | — | — |
| 47 |  | Reserve | — | — | — | — | — | — | — | — |
| 48 | Instruction Cache RAM | Instruction Cache RAM (PE0)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 49 |  | Instruction Cache RAM (PE1)  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 50 |  | Reserve | — | — | — | — | — | — | — | — |
| 51 |  | Reserve | — | — | — | — | — | — | — | — |
| 52 |  | Reserve | — | — | — | — | — | — | — | — |
| 53 |  | Reserve | — | — | — | — | — | — | — | — |
| 54 |  | Reserve | — | — | — | — | — | — | — | — |
| 55 |  | Reserve | — | — | — | — | — | — | — | — |
| 56 |  | Instruction Cache RAM EDC (PE0)  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 57 |  | Instruction Cache RAM EDC (PE1)  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 58 |  | Reserve | — | — | — | — | — | — | — | — |
| 59 |  | Reserve | — | — | — | — | — | — | — | — |
| 60 |  | Reserve | — | — | — | — | — | — | — | — |
| 61 |  | Reserve | — | — | — | — | — | — | — | — |
| 62 |  | Reserve | — | — | — | — | — | — | — | — |
| 63 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.21 List of Error Inputs of E2L (3/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 64 | Instruction Cache RAM | Reserve | — | — | — | — | — | — | — | — |
| 65 |  | Reserve | — | — | — | — | — | — | — | — |
| 66 |  | Reserve | — | — | — | — | — | — | — | — |
| 67 |  | Reserve | — | — | — | — | — | — | — | — |
| 68 |  | Reserve | — | — | — | — | — | — | — | — |
| 69 |  | Reserve | — | — | — | — | — | — | — | — |
| 70 |  | Reserve | — | — | — | — | — | — | — | — |
| 71 |  | Reserve | — | — | — | — | — | — | — | — |
| 72 | Reserve |  | — | — | — | — | — | — | — | — |
| 73 | Reserve |  | — | — | — | — | — | — | — | — |
| 74 | Reserve |  | — | — | — | — | — | — | — | — |
| 75 | Reserve |  | — | — | — | — | — | — | — | — |
| 76 | Reserve |  | — | — | — | — | — | — | — | — |
| 77 | Reserve |  | — | — | — | — | — | — | — | — |
| 78 | Reserve |  | — | — | — | — | — | — | — | — |
| 79 | Reserve |  | — | — | — | — | — | — | — | — |
| 80 | PE guard function (PEG) | PEG error (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 81 |  | PEG error (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 82 |  | Reserve | — | — | — | — | — | — | — | — |
| 83 |  | Reserve | — | — | — | — | — | — | — | — |
| 84 |  | Reserve | — | — | — | — | — | — | — | — |
| 85 |  | Reserve | — | — | — | — | — | — | — | — |
| 86 |  | Reserve | — | — | — | — | — | — | — | — |
| 87 |  | Reserve | — | — | — | — | — | — | — | — |
| 88 | Clock Monitor | Clock monitor error (CLMA5) (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 89 |  | Clock monitor error (CLMA6) (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 90 |  | Reserve | — | — | — | — | — | — | — | — |
| 91 |  | Reserve | — | — | — | — | — | — | — | — |
| 92 |  | Reserve | — | — | — | — | — | — | — | — |
| 93 |  | Reserve | — | — | — | — | — | — | — | — |
| 94 |  | Reserve | — | — | — | — | — | — | — | — |
| 95 |  | Reserve | — | — | — | — | — | — | — | — |
| 96 | OSTM | OSTM1 Interrupt | √ | √ | √ | √ | √ | √ | — | √ |
| 97 |  | OSTM2 Interrupt | √ | √ | √ | √ | √ | √ | — | √ |
| 98 |  | Reserve | — | — | — | — | — | — | — | — |
| 99 |  | Reserve | — | — | — | — | — | — | — | — |
| 100 |  | Reserve | — | — | — | — | — | — | — | — |
| 101 |  | Reserve | — | — | — | — | — | — | — | — |
| 102 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.21 List of Error Inputs of E2L (4/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 103 | Reserve |  | — | — | — | — | — | — | — | — |
| 104 | Reserve |  | — | — | — | — | — | — | — | — |
| 105 | Reserve |  | — | — | — | — | — | — | — | — |
| 106 | Reserve |  | — | — | — | — | — | — | — | — |
| 107 | Reserve |  | — | — | — | — | — | — | — | — |
| 108 | Reserve |  | — | — | — | — | — | — | — | — |
| 109 | Reserve |  | — | — | — | — | — | — | — | — |
| 110 | Reserve |  | — | — | — | — | — | — | — | — |
| 111 | Reserve |  | — | — | — | — | — | — | — | — |
| 112 | Mode Error | Unintended Debug Enable detection (PE0) | √ | √ | √ | √ | √ | √ | — | √ |
| 113 |  | Unintended Debug Enable detection (PE1) | √ | √ | √ | √ | √ | √ | — | √ |
| 114 |  | Reserve | — | — | — | — | — | — | — | — |
| 115 |  | Reserve | — | — | — | — | — | — | — | — |
| 116 |  | Reserve | — | — | — | — | — | — | — | — |
| 117 |  | Reserve | — | — | — | — | — | — | — | — |
| 118 |  | Reserve | — | — | — | — | — | — | — | — |
| 119 |  | Reserve | — | — | — | — | — | — | — | — |
| 120 | PEG error | PEG error (PE0) Detected in a read request from PE0 to the others LRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 121 |  | PEG error (PE1) Detected in a read request from PE1 to the others LRAM | √ | √ | √ | √ | √ | √ | — | √ |
| 122 |  | Reserve | — | — | — | — | — | — | — | — |
| 123 |  | Reserve | — | — | — | — | — | — | — | — |
| 124 |  | Reserve | — | — | — | — | — | — | — | — |
| 125 |  | Reserve | — | — | — | — | — | — | — | — |
| 126 |  | Reserve | — | — | — | — | — | — | — | — |
| 127 |  | Reserve | — | — | — | — | — | — | — | — |
| 128 | Reserve |  | — | — | — | — | — | — | — | — |
| 129 | Reserve |  | — | — | — | — | — | — | — | — |
| 130 | Reserve |  | — | — | — | — | — | — | — | — |
| 131 | Reserve |  | — | — | — | — | — | — | — | — |
| 132 | Reserve |  | — | — | — | — | — | — | — | — |
| 133 | Reserve |  | — | — | — | — | — | — | — | — |
| 134 | Reserve |  | — | — | — | — | — | — | — | — |
| 135 | Reserve |  | — | — | — | — | — | — | — | — |
| 136 | Reserve |  | — | — | — | — | — | — | — | — |
| 137 | Reserve |  | — | — | — | — | — | — | — | — |
| 138 | Reserve |  | — | — | — | — | — | — | — | — |
| 139 | Reserve |  | — | — | — | — | — | — | — | — |
| 140 | Reserve |  | — | — | — | — | — | — | — | — |

Table 39.21 List of Error Inputs of E2L (5/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 141 | Reserve |  | — | — | — | — | — | — | — | — |
| 142 | Reserve |  | — | — | — | — | — | — | — | — |
| 143 | Reserve |  | — | — | — | — | — | — | — | — |
| 144 | Reserve |  | — | — | — | — | — | — | — | — |
| 145 | Reserve |  | — | — | — | — | — | — | — | — |
| 146 | Reserve |  | — | — | — | — | — | — | — | — |
| 147 | Reserve |  | — | — | — | — | — | — | — | — |
| 148 | Reserve |  | — | — | — | — | — | — | — | — |
| 149 | Reserve |  | — | — | — | — | — | — | — | — |
| 150 | Reserve |  | — | — | — | — | — | — | — | — |
| 151 | Reserve |  | — | — | — | — | — | — | — | — |
| 152 | Cluster RAM | Cluster RAM  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 153 |  | Cluster RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 154 |  | Cluster RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 155 |  | Cluster RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 156 |  | Reserve | — | — | — | — | — | — | — | — |
| 157 |  | Reserve | — | — | — | — | — | — | — | — |
| 158 |  | Reserve | — | — | — | — | — | — | — | — |
| 159 |  | Reserve | — | — | — | — | — | — | — | — |
| 160 | Local RAM  (other core) | Reserve | — | — | — | — | — | — | — | — |
| 161 |  | LRAM (error by other core access)  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 162 |  | LRAM (error by other core access)  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 163 |  | LRAM (error by other core access)  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 164 | sDMA | sDMAC0 RAM  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 165 |  | sDMAC0 RAM  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 166 |  | Reserve | — | — | — | — | — | — | — | — |
| 167 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.21 List of Error Inputs of E2L (6/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 168 | Peripheral RAM | Peripheral (DTS) RAM ECC  - ECC 2bit error  - Address feedback compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 169 |  | Peripheral (DTS) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 170 |  | Peripheral (DTS) RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 171 |  | Peripheral(except DTS) RAM ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 172 |  | Reserve | — | — | — | — | — | — | — | — |
| 173 |  | Reserve | — | — | — | — | — | — | — | — |
| 174 |  | Peripheral(CAN) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 175 |  | Peripheral(CAN) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 176 |  | Peripheral(DFE) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 177 |  | Peripheral(DFE) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 178 |  | Peripheral(GTM) RAM ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 179 |  | Peripheral(GTM) RAM ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 180 |  | Reserve | — | — | — | — | — | — | — | — |
| 181 |  | Reserve | — | — | — | — | — | — | — | — |
| 182 |  | Reserve | — | — | — | — | — | — | — | — |
| 183 |  | Reserve | — | — | — | — | — | — | — | — |
| 184 |  | Reserve | — | — | — | — | — | — | — | — |
| 185 |  | Reserve | — | — | — | — | — | — | — | — |
| 186 |  | Reserve | — | — | — | — | — | — | — | — |
| 187 |  | Reserve | — | — | — | — | — | — | — | — |
| 188 |  | Reserve | — | — | — | — | — | — | — | — |
| 189 |  | Reserve | — | — | — | — | — | — | — | — |
| 190 |  | Reserve | — | — | — | — | — | — | — | — |
| 191 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.21 List of Error Inputs of E2L (7/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 192 | Peripheral RAM | Reserve | — | — | — | — | — | — | — | — |
| 193 |  | Reserve | — | — | — | — | — | — | — | — |
| 194 |  | Reserve | — | — | — | — | — | — | — | — |
| 195 |  | Reserve | — | — | — | — | — | — | — | — |
| 196 |  | Reserve | — | — | — | — | — | — | — | — |
| 197 |  | Reserve | — | — | — | — | — | — | — | — |
| 198 |  | Reserve | — | — | — | — | — | — | — | — |
| 199 |  | Reserve | — | — | — | — | — | — | — | — |
| 200 | Code Flash | Code Flash  - Address parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 201 |  | Code Flash ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 202 |  | Code Flash ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 203 |  | Code Flash ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 204 |  | Reserve | — | — | — | — | — | — | — | — |
| 205 |  | Reserve | — | — | — | — | — | — | — | — |
| 206 |  | Reserve | — | — | — | — | — | — | — | — |
| 207 |  | Reserve | — | — | — | — | — | — | — | — |
| 208 | Data Flash | Data Flash ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 209 |  | Data Flash ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 210 |  | Data Flash ECC  - Error address overflow | √ | √ | √ | √ | √ | √ | — | √ |
| 211 |  | Reserve | — | — | — | — | — | — | — | — |
| 212 |  | Reserve | — | — | — | — | — | — | — | — |
| 213 |  | Reserve | — | — | — | — | — | — | — | — |
| 214 |  | Reserve | — | — | — | — | — | — | — | — |
| 215 |  | Reserve | — | — | — | — | — | — | — | — |
| 216 | Bus ECC | Data Bus ECC  - ECC 2bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 217 |  | Data Bus ECC  - ECC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 218 |  | Address Bus ECC  - EDC 2bit error  - EDC 1bit error | √ | √ | √ | √ | √ | √ | — | √ |
| 219 |  | Reserve | — | — | — | — | — | — | — | — |
| 220 |  | Reserve | — | — | — | — | — | — | — | — |
| 221 |  | Reserve | — | — | — | — | — | — | — | — |
| 222 |  | Reserve | — | — | — | — | — | — | — | — |
| 223 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.21 List of Error Inputs of E2L (8/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 224 | Cluster RAM Guard (CRG) | CRAM Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 225 | P-Bus Guard (PBG) | P-Bus Guard error | √ | √ | √ | √ | √ | √ | — | √ |
| 226 | Reserve |  | — | — | — | — | — | — | — | — |
| 227 | I-Bus Guard (IBG) | I-Bus Guard error  (IPIR MEV Barrier TPTM) | √ | √ | √ | √ | √ | √ | — | √ |
| 228 | Reserve |  | — | — | — | — | — | — | — | — |
| 229 | Reserve |  | — | — | — | — | — | — | — | — |
| 230 | Reserve |  | — | — | — | — | — | — | — | — |
| 231 | Reserve |  | — | — | — | — | — | — | — | — |
| 232 | Clock Monitor | Clock monitor error (CLMA0) | √ | √ | √ | √ | √ | √ | — | √ |
| 233 |  | Clock monitor error (CLMA1) | √ | √ | √ | √ | √ | √ | — | √ |
| 234 |  | Clock monitor error (CLMA2) | √ | √ | √ | √ | √ | √ | — | √ |
| 235 |  | Clock monitor error (CLMA3) | √ | √ | √ | √ | √ | √ | — | √ |
| 236 |  | Clock monitor error (CLMA4) | √ | √ | √ | √ | √ | √ | — | √ |
| 237 | Reserve |  | — | — | — | — | — | — | — | — |
| 238 | Reserve |  | — | — | — | — | — | — | — | — |
| 239 | Reserve |  | — | — | — | — | — | — | — | — |
| 240 | DSADC  ADC  Cyclic ADC | AD parity error | √ | √ | √ | √ | √ | √ | — | √ |
| 241 | MISG | MISG compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 242 | DTS | DTS compare error | √ | √ | √ | √ | √ | √ | — | √ |
| 243 | External Error Input | ERRORIN | √ | √ | √ | √ | √ | √ | — | √ |
| 244 | Flash | Flash access error | √ | √ | √ | √ | √ | √ | — | √ |
| 245 |  | FACI reset transfer error | √ | — | — | — | √ | — | — | — |
| 246 |  | FBIST parameter transfer error | √ | — | — | — | √ | — | — | — |
| 247 |  | Reserve | — | — | — | — | — | — | — | — |

Table 39.21 List of Error Inputs of E2L (9/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 248 | Reserve |  | — | — | — | — | — | — | — | — |
| 249 | Reserve |  | — | — | — | — | — | — | — | — |
| 250 | Reserve |  | — | — | — | — | — | — | — | — |
| 251 | Reserve |  | — | — | — | — | — | — | — | — |
| 252 | Reserve |  | — | — | — | — | — | — | — | — |
| 253 | Reserve |  | — | — | — | — | — | — | — | — |
| 254 | Reserve |  | — | — | — | — | — | — | — | — |
| 255 | Reserve |  | — | — | — | — | — | — | — | — |
| 256 | Reserve |  | — | — | — | — | — | — | — | — |
| 257 | Reserve |  | — | — | — | — | — | — | — | — |
| 258 | Reserve |  | — | — | — | — | — | — | — | — |
| 259 | Reserve |  | — | — | — | — | — | — | — | — |
| 260 | Reserve |  | — | — | — | — | — | — | — | — |
| 261 | Reserve |  | — | — | — | — | — | — | — | — |
| 262 | Reserve |  | — | — | — | — | — | — | — | — |
| 263 | Reserve |  | — | — | — | — | — | — | — | — |
| 264 | Reserve |  | — | — | — | — | — | — | — | — |
| 265 | Reserve |  | — | — | — | — | — | — | — | — |
| 266 | Reserve |  | — | — | — | — | — | — | — | — |
| 267 | Reserve |  | — | — | — | — | — | — | — | — |
| 268 | Reserve |  | — | — | — | — | — | — | — | — |
| 269 | Reserve |  | — | — | — | — | — | — | — | — |
| 270 | Reserve |  | — | — | — | — | — | — | — | — |
| 271 | Reserve |  | — | — | — | — | — | — | — | — |
| 272 | Reserve |  | — | — | — | — | — | — | — | — |
| 273 | Reserve |  | — | — | — | — | — | — | — | — |
| 274 | Reserve |  | — | — | — | — | — | — | — | — |
| 275 | Reserve |  | — | — | — | — | — | — | — | — |
| 276 | Reserve |  | — | — | — | — | — | — | — | — |
| 277 | Reserve |  | — | — | — | — | — | — | — | — |
| 278 | Reserve |  | — | — | — | — | — | — | — | — |
| 279 | Reserve |  | — | — | — | — | — | — | — | — |
| 280 | Data Path Redundancy | DMA Comp error | √ | √ | √ | √ | √ | √ | — | √ |
| 281 |  | BUS Bridge Comp error | √ | √ | √ | √ | √ | √ | — | √ |

Table 39.21 List of Error Inputs of E2L (10/10)

| No. | Module | Error sources | Error Flag  Set | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 282 | BUS Routing checker | Inter-processor element Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 283 |  | Inter-cluster Bus (I-Bus) | √ | √ | √ | √ | √ | √ | — | √ |
| 284 |  | Peripheral Bus (P-Bus) | √ | √ | √ | √ | √ | √ | — | √ |
| 285 |  | CRAM Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 286 |  | System Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 287 |  | Global FLASH Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 288 |  | Local FLASH Bus | √ | √ | √ | √ | √ | √ | — | √ |
| 289 |  | Reserve | — | — | — | — | — | — | — | — |
| 290 |  | Reserve | — | — | — | — | — | — | — | — |
| 291 |  | Reserve | — | — | — | — | — | — | — | — |
| 292 | Voltage Monitor | EVCC Secondary HDET | √ | √ | √ | √ | √ | √ | — | √ |
| 293 |  | EVCC Secondary LDET | √ | √ | √ | √ | √ | √ | — | √ |
| 294 |  | VCC Secondary HDET | √ | √ | √ | √ | √ | √ | — | √ |
| 295 |  | VCC Secondary LDET | √ | √ | √ | √ | √ | √ | — | √ |
| 296 |  | VDD Secondary HDET | √ | √ | √ | √ | √ | √ | — | √ |
| 297 |  | VDD Secondary LDET | √ | √ | √ | √ | √ | √ | — | √ |
| 298 |  | Reserve | — | — | — | — | — | — | — | — |
| 299 | Mode Error | Mode error  - Unintended activation of Production Test Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 300 |  | Mode error  - Unintended activation of Normal Operation Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 301 |  | Mode error  - Unintended deactivation of Normal Operation Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 302 |  | Mode error  - Unintended activation of Serial Programming Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 303 |  | Mode error  - Unintended activation of User Boot Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 304 |  | Mode error  - Unintended deactivation of User Boot Mode | √ | √ | √ | √ | √ | √ | — | √ |
| 305 |  | Mode error  - Mode latch error | √ | √ | √ | √ | √ | √ | — | √ |
| 306 | Reserve |  | — | — | — | — | — | — | — | — |
| 307 | Reserve |  | — | — | — | — | — | — | — | — |
| 308 | ECM | ECM compare error | √ | √ | √ | √ | √ | √ | — | √ |

1. The internal reset generation is enabled in the initial state.

Table 39.22 List of Error Inputs of E2x-FCC2

| No. | Module | Error sources | Error Flag  Set | | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | Dual Core Lock-step | DCLS compare error (PE0) | √ | | √ | √ | √ | √ | √ | √ | √ |
| 1 |  | DCLS compare error (PE1) | √ | | √ | √ | √ | √ | √ | √ | √ |
| 2 |  | Reserve | — | | — | — | — | — | — | — | — |
| 3 |  | Reserve | — | | — | — | — | — | — | — | — |
| 4 |  | DCLS compare error (PE4) | √ | | √ | √ | √ | √ | √ | √ | √ |
| 5 |  | DCLS compare error (PE5) | √ | | √ | √ | √ | √ | √ | √ | √ |
| 6 |  | Reserve | — | | — | — | — | — | — | — | — |
| 7 |  | Reserve | — | | — | — | — | — | — | — | — |
| 8 | Watchdog timer | Watchdog timer ch0 error (PE0) | √ | | √ | √ | √[\*](#Note1_FCC1)[1](#Note1_FCC1) | √ | √ | — | √ |
| 9 |  | Watchdog timer ch1 error (PE1) | √ | | √ | √ | √ | √ | √ | — | √ |
| 10 |  | Watchdog timer ch1 error (PE2) | √ | | √ | √ | √ | √ | √ | — | √ |
| 11 |  | Watchdog timer ch1 error (PE3) | √ | | √ | √ | √ | √ | √ | — | √ |
| 12 |  | Watchdog timer ch1 error (PE4) | √ | | √ | √ | √ | √ | √ | — | √ |
| 13 |  | Watchdog timer ch1 error (PE5) | √ | | √ | √ | √ | √ | √ | — | √ |
| 14 |  | Reserve | — | | — | — | — | — | — | — | — |
| 15 |  | Reserve | — | | — | — | — | — | — | — | — |
| 16 | Local RAM  (own core) | Local RAM (PE0)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 17 |  | Local RAM (PE1)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 18 |  | Local RAM (PE2)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 19 |  | Local RAM (PE3)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 20 |  | Local RAM (PE4)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 21 |  | Local RAM (PE5)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 22 |  | Reserve | — | | — | — | — | — | — | — | — |
| 23 |  | Reserve | — | | — | — | — | — | — | — | — |
| 24 |  | Local RAM ECC (PE0)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 25 |  | Local RAM ECC (PE1)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 26 |  | Local RAM ECC (PE2)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 27 |  | Local RAM ECC (PE3)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 28 |  | Local RAM ECC (PE4)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 29 |  | Local RAM ECC (PE5)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 30 |  | Reserve | — | | — | — | — | — | — | — | — |
| 31 | Local RAM  (own core) | Reserve | — | — | | — | — | — | — | — | — |
| 32 |  | Local RAM ECC (PE0)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 33 |  | Local RAM ECC (PE1)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 34 |  | Local RAM ECC (PE2)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 35 |  | Local RAM ECC (PE3)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 36 |  | Local RAM ECC (PE4)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 37 |  | Local RAM ECC (PE5)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 38 |  | Reserve | — | — | | — | — | — | — | — | — |
| 39 |  | Reserve | — | — | | — | — | — | — | — | — |
| 40 |  | Local RAM ECC (PE0)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 41 |  | Local RAM ECC (PE1)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 42 |  | Local RAM ECC (PE2)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 43 |  | Local RAM ECC (PE3)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 44 |  | Local RAM ECC (PE4)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 45 |  | Local RAM ECC (PE5)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 46 |  | Reserve | — | — | | — | — | — | — | — | — |
| 47 |  | Reserve | — | — | | — | — | — | — | — | — |
| 48 | Instruction Cache RAM | Instruction Cache RAM (PE0)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 49 |  | Instruction Cache RAM (PE1)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 50 |  | Instruction Cache RAM (PE2)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 51 |  | Instruction Cache RAM (PE3)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 52 |  | Instruction Cache RAM (PE4)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 53 |  | Instruction Cache RAM (PE5)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 54 |  | Reserve | — | — | | — | — | — | — | — | — |
| 55 |  | Reserve | — | — | | — | — | — | — | — | — |
| 56 |  | Instruction Cache RAM EDC (PE0)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 57 |  | Instruction Cache RAM EDC (PE1)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 58 |  | Instruction Cache RAM EDC (PE2)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 59 |  | Instruction Cache RAM EDC (PE3)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 60 |  | Instruction Cache RAM EDC (PE4)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 61 |  | Instruction Cache RAM EDC (PE5)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 62 |  | Reserve | — | — | | — | — | — | — | — | — |
| 63 |  | Reserve | — | — | | — | — | — | — | — | — |
| 64 |  | Reserve | — | — | | — | — | — | — | — | — |
| 65 |  | Reserve | — | — | | — | — | — | — | — | — |
| 66 |  | Reserve | — | — | | — | — | — | — | — | — |
| 67 |  | Reserve | — | — | | — | — | — | — | — | — |
| 68 |  | Reserve | — | — | | — | — | — | — | — | — |
| 69 |  | Reserve | — | — | | — | — | — | — | — | — |
| 70 |  | Reserve | — | — | | — | — | — | — | — | — |
| 71 |  | Reserve | — | — | | — | — | — | — | — | — |
| 72 | Reserve |  | — | — | | — | — | — | — | — | — |
| 73 | Reserve |  | — | — | | — | — | — | — | — | — |
| 74 | Reserve |  | — | — | | — | — | — | — | — | — |
| 75 | Reserve |  | — | — | | — | — | — | — | — | — |
| 76 | Reserve |  | — | — | | — | — | — | — | — | — |
| 77 | Reserve |  | — | — | | — | — | — | — | — | — |
| 78 | Reserve |  | — | — | | — | — | — | — | — | — |
| 79 | Reserve |  | — | — | | — | — | — | — | — | — |
| 80 | PE guard function (PEG) | PEG error (PE0) | √ | √ | | √ | √ | √ | √ | — | √ |
| 81 |  | PEG error (PE1) | √ | √ | | √ | √ | √ | √ | — | √ |
| 82 |  | PEG error (PE2) | √ | √ | | √ | √ | √ | √ | — | √ |
| 83 |  | PEG error (PE3) | √ | √ | | √ | √ | √ | √ | — | √ |
| 84 |  | PEG error (PE4) | √ | √ | | √ | √ | √ | √ | — | √ |
| 85 |  | PEG error (PE5) | √ | √ | | √ | √ | √ | √ | — | √ |
| 86 |  | Reserve | — | — | | — | — | — | — | — | — |
| 87 |  | Reserve | — | — | | — | — | — | — | — | — |
| 88 | Clock Monitor | Clock monitor error (CLMA5) (PE0) | √ | √ | | √ | √ | √ | √ | — | √ |
| 89 |  | Clock monitor error (CLMA6) (PE1) | √ | √ | | √ | √ | √ | √ | — | √ |
| 90 |  | Clock monitor error (CLMA7) (PE2) | √ | √ | | √ | √ | √ | √ | — | √ |
| 91 |  | Clock monitor error (CLMA8) (PE3) | √ | √ | | √ | √ | √ | √ | — | √ |
| 92 |  | Clock monitor error (CLMA9) (PE4) | √ | √ | | √ | √ | √ | √ | — | √ |
| 93 |  | Clock monitor error (CLMA10) (PE5) | √ | √ | | √ | √ | √ | √ | — | √ |
| 94 |  | Reserve | — | — | | — | — | — | — | — | — |
| 95 |  | Reserve | — | — | | — | — | — | — | — | — |
| 96 | OSTM | OSTM1 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 97 |  | OSTM2 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 98 |  | OSTM3 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 99 |  | OSTM4 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 100 |  | OSTM5 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 101 |  | OSTM6 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 102 |  | Reserve | — | — | | — | — | — | — | — | — |
| 103 |  | Reserve | — | — | | — | — | — | — | — | — |
| 104 | Reserve |  | — | — | | — | — | — | — | — | — |
| 105 | Reserve |  | — | — | | — | — | — | — | — | — |
| 106 | Reserve |  | — | — | | — | — | — | — | — | — |
| 107 | Reserve |  | — | — | | — | — | — | — | — | — |
| 108 | Reserve |  | — | — | | — | — | — | — | — | — |
| 109 | Reserve |  | — | — | | — | — | — | — | — | — |
| 110 | Reserve |  | — | — | | — | — | — | — | — | — |
| 111 | Reserve |  | — | — | | — | — | — | — | — | — |
| 112 | Mode Error | Unintended Debug Enable detection (PE0) | √ | √ | | √ | √ | √ | √ | — | √ |
| 113 |  | Unintended Debug Enable detection (PE1) | √ | √ | | √ | √ | √ | √ | — | √ |
| 114 |  | Unintended Debug Enable detection (PE2) | √ | √ | | √ | √ | √ | √ | — | √ |
| 115 |  | Unintended Debug Enable detection (PE3) | √ | √ | | √ | √ | √ | √ | — | √ |
| 116 |  | Unintended Debug Enable detection (PE4) | √ | √ | | √ | √ | √ | √ | — | √ |
| 117 |  | Unintended Debug Enable detection (PE5) | √ | √ | | √ | √ | √ | √ | — | √ |
| 118 |  | Reserve | — | — | | — | — | — | — | — | — |
| 119 |  | Reserve | — | — | | — | — | — | — | — | — |
| 120 | PEG error | PEG error (PE0) Detected in a read request from PE0 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 121 |  | PEG error (PE1) Detected in a read request from PE1 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 122 |  | PEG error (PE2) Detected in a read request from PE2 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 123 |  | PEG error (PE3) Detected in a read request from PE3 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 124 |  | PEG error (PE4) Detected in a read request from PE4 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 125 |  | PEG error (PE5) Detected in a read request from PE5 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 126 |  | Reserve | — | — | | — | — | — | — | — | — |
| 127 |  | Reserve | — | — | | — | — | — | — | — | — |
| 128 | Reserve |  | — | — | | — | — | — | — | — | — |
| 129 | Reserve |  | — | — | | — | — | — | — | — | — |
| 130 | Reserve |  | — | — | | — | — | — | — | — | — |
| 131 | Reserve |  | — | — | | — | — | — | — | — | — |
| 132 | Reserve |  | — | — | | — | — | — | — | — | — |
| 133 | Reserve |  | — | — | | — | — | — | — | — | — |
| 134 | Reserve |  | — | — | | — | — | — | — | — | — |
| 135 | Reserve |  | — | — | | — | — | — | — | — | — |
| 136 | Reserve |  | — | — | | — | — | — | — | — | — |
| 137 | Reserve |  | — | — | | — | — | — | — | — | — |
| 138 | Reserve |  | — | — | | — | — | — | — | — | — |
| 139 | Reserve |  | — | — | | — | — | — | — | — | — |
| 140 | Reserve |  | — | — | | — | — | — | — | — | — |
| 141 | Reserve |  | — | — | | — | — | — | — | — | — |
| 142 | Reserve |  | — | — | | — | — | — | — | — | — |
| 143 | Reserve |  | — | — | | — | — | — | — | — | — |
| 144 | Reserve |  | — | — | | — | — | — | — | — | — |
| 145 | Reserve |  | — | — | | — | — | — | — | — | — |
| 146 | Reserve |  | — | — | | — | — | — | — | — | — |
| 147 | Reserve |  | — | — | | — | — | — | — | — | — |
| 148 | Reserve |  | — | — | | — | — | — | — | — | — |
| 149 | Reserve |  | — | — | | — | — | — | — | — | — |
| 150 | Reserve |  | — | — | | — | — | — | — | — | — |
| 151 | Reserve |  | — | — | | — | — | — | — | — | — |
| 152 | Cluster RAM | Cluster RAM  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 153 |  | Cluster RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 154 |  | Cluster RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 155 |  | Cluster RAM ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 156 |  | Reserve | — | — | | — | — | — | — | — | — |
| 157 |  | Reserve | — | — | | — | — | — | — | — | — |
| 158 |  | Reserve | — | — | | — | — | — | — | — | — |
| 159 |  | Reserve | — | — | | — | — | — | — | — | — |
| 160 | Local RAM  (other core) | Reserve | — | — | | — | — | — | — | — | — |
| 161 |  | LRAM (error by other core access)  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 162 |  | LRAM (error by other core access)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 163 |  | LRAM (error by other core access)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 164 | sDMA | sDMAC0 RAM  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 165 |  | sDMAC0 RAM  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 166 |  | sDMAC1 RAM  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 167 |  | sDMAC1 RAM  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 168 | Peripheral RAM | Peripheral (DTS) RAM ECC  - ECC 2bit error  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 169 |  | Peripheral (DTS) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 170 |  | Peripheral (DTS) RAM ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 171 |  | Peripheral(except DTS) RAM ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 172 |  | Peripheral(FlexRay) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 173 |  | Peripheral(FlexRay) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 174 |  | Peripheral(CAN) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 175 |  | Peripheral(CAN) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 176 |  | Peripheral(DFE) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 177 |  | Peripheral(DFE) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 178 |  | Peripheral(GTM) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 179 |  | Peripheral(GTM) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 180 |  | Peripheral(Ethernet) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 181 |  | Peripheral(Ethernet) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 182 |  | Reserve | — | — | | — | — | — | — | — | — |
| 183 |  | Reserve | — | — | | — | — | — | — | — | — |
| 184 |  | Reserve | — | — | | — | — | — | — | — | — |
| 185 |  | Reserve | — | — | | — | — | — | — | — | — |
| 186 |  | Reserve | — | — | | — | — | — | — | — | — |
| 187 |  | Reserve | — | — | | — | — | — | — | — | — |
| 188 |  | Reserve | — | — | | — | — | — | — | — | — |
| 189 |  | Reserve | — | — | | — | — | — | — | — | — |
| 190 |  | Reserve | — | — | | — | — | — | — | — | — |
| 191 |  | Reserve | — | — | | — | — | — | — | — | — |
| 192 |  | Reserve | — | — | | — | — | — | — | — | — |
| 193 |  | Reserve | — | — | | — | — | — | — | — | — |
| 194 |  | Reserve | — | — | | — | — | — | — | — | — |
| 195 |  | Reserve | — | — | | — | — | — | — | — | — |
| 196 |  | Reserve | — | — | | — | — | — | — | — | — |
| 197 |  | Reserve | — | — | | — | — | — | — | — | — |
| 198 |  | Reserve | — | — | | — | — | — | — | — | — |
| 199 |  | Reserve | — | — | | — | — | — | — | — | — |
| 200 | Code Flash | Code Flash  - Address parity error | √ | √ | | √ | √ | √ | √ | — | √ |
| 201 |  | Code Flash ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 202 |  | Code Flash ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 203 |  | Code Flash ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 204 |  | Reserve | — | — | | — | — | — | — | — | — |
| 205 |  | Reserve | — | — | | — | — | — | — | — | — |
| 206 |  | Reserve | — | — | | — | — | — | — | — | — |
| 207 |  | Reserve | — | — | | — | — | — | — | — | — |
| 208 | Data Flash | Data Flash ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 209 |  | Data Flash ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 210 |  | Data Flash ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 211 |  | Reserve | — | — | | — | — | — | — | — | — |
| 212 |  | Reserve | — | — | | — | — | — | — | — | — |
| 213 |  | Reserve | — | — | | — | — | — | — | — | — |
| 214 |  | Reserve | — | — | | — | — | — | — | — | — |
| 215 |  | Reserve | — | — | | — | — | — | — | — | — |
| 216 | Bus ECC | Data Bus ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 217 |  | Data Bus ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 218 |  | Address Bus ECC  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 219 |  | Reserve | — | — | | — | — | — | — | — | — |
| 220 |  | Reserve | — | — | | — | — | — | — | — | — |
| 221 |  | Reserve | — | — | | — | — | — | — | — | — |
| 222 |  | Reserve | — | — | | — | — | — | — | — | — |
| 223 |  | Reserve | — | — | | — | — | — | — | — | — |
| 224 | Cluster RAM Guard (CRG) | CRAM Guard error | √ | √ | | √ | √ | √ | √ | — | √ |
| 225 | P-Bus Guard (PBG) | P-Bus Guard error | √ | √ | | √ | √ | √ | √ | — | √ |
| 226 | H-Bus Guard (HBG) | H-Bus Guard error | √ | √ | | √ | √ | √ | √ | — | √ |
| 227 | I-Bus Guard (IBG) | I-Bus Guard error  (IPIR MEV Barrier TPTM) | √ | √ | | √ | √ | √ | √ | — | √ |
| 228 | Reserve |  | — | — | | — | — | — | — | — | — |
| 229 | Reserve |  | — | — | | — | — | — | — | — | — |
| 230 | Reserve |  | — | — | | — | — | — | — | — | — |
| 231 | Reserve |  | — | — | | — | — | — | — | — | — |
| 232 | Clock Monitor | Clock monitor error (CLMA0) | √ | √ | | √ | √ | √ | √ | — | √ |
| 233 |  | Clock monitor error (CLMA1) | √ | √ | | √ | √ | √ | √ | — | √ |
| 234 |  | Clock monitor error (CLMA2) | √ | √ | | √ | √ | √ | √ | — | √ |
| 235 |  | Clock monitor error (CLMA3) | √ | √ | | √ | √ | √ | √ | — | √ |
| 236 |  | Clock monitor error (CLMA4) | √ | √ | | √ | √ | √ | √ | — | √ |
| 237 | Reserve |  | — | — | | — | — | — | — | — | — |
| 238 | Reserve |  | — | — | | — | — | — | — | — | — |
| 239 | Reserve |  | — | — | | — | — | — | — | — | — |
| 240 | DSADC  ADC  Cyclic ADC | AD parity error | √ | √ | | √ | √ | √ | √ | — | √ |
| 241 | MISG | MISG compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 242 | DTS | DTS compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 243 | External Error Input | ERRORIN | √ | √ | | √ | √ | √ | √ | — | √ |
| 244 | Flash | Flash access error | √ | √ | | √ | √ | √ | √ | — | √ |
| 245 |  | FACI reset transfer error | √ | — | | — | — | √ | — | — | — |
| 246 |  | FBIST parameter transfer error | √ | — | | — | — | √ | — | — | — |
| 247 |  | Reserve | — | — | | — | — | — | — | — | — |
| 248 | Reserve |  | — | — | | — | — | — | — | — | — |
| 249 | Reserve |  | — | — | | — | — | — | — | — | — |
| 250 | Reserve |  | — | — | | — | — | — | — | — | — |
| 251 | Reserve |  | — | — | | — | — | — | — | — | — |
| 252 | Reserve |  | — | — | | — | — | — | — | — | — |
| 253 | Reserve |  | — | — | | — | — | — | — | — | — |
| 254 | Reserve |  | — | — | | — | — | — | — | — | — |
| 255 | Reserve |  | — | — | | — | — | — | — | — | — |
| 256 | Reserve |  | — | — | | — | — | — | — | — | — |
| 257 | Reserve |  | — | — | | — | — | — | — | — | — |
| 258 | Reserve |  | — | — | | — | — | — | — | — | — |
| 259 | Reserve |  | — | — | | — | — | — | — | — | — |
| 260 | Reserve |  | — | — | | — | — | — | — | — | — |
| 261 | Reserve |  | — | — | | — | — | — | — | — | — |
| 262 | Reserve |  | — | — | | — | — | — | — | — | — |
| 263 | Reserve |  | — | — | | — | — | — | — | — | — |
| 264 | Reserve |  | — | — | | — | — | — | — | — | — |
| 265 | Reserve |  | — | — | | — | — | — | — | — | — |
| 266 | Reserve |  | — | — | | — | — | — | — | — | — |
| 267 | Reserve |  | — | — | | — | — | — | — | — | — |
| 268 | Reserve |  | — | — | | — | — | — | — | — | — |
| 269 | Reserve |  | — | — | | — | — | — | — | — | — |
| 270 | Reserve |  | — | — | | — | — | — | — | — | — |
| 271 | Reserve |  | — | — | | — | — | — | — | — | — |
| 272 | Reserve |  | — | — | | — | — | — | — | — | — |
| 273 | Reserve |  | — | — | | — | — | — | — | — | — |
| 274 | Reserve |  | — | — | | — | — | — | — | — | — |
| 275 | Reserve |  | — | — | | — | — | — | — | — | — |
| 276 | Reserve |  | — | — | | — | — | — | — | — | — |
| 277 | Reserve |  | — | — | | — | — | — | — | — | — |
| 278 | Reserve |  | — | — | | — | — | — | — | — | — |
| 279 | Reserve |  | — | — | | — | — | — | — | — | — |
| 280 | Data Path Redundancy | DMA Comp error | √ | √ | | √ | √ | √ | √ | — | √ |
| 281 |  | BUS Bridge Comp error | √ | √ | | √ | √ | √ | √ | — | √ |
| 282 | BUS Routing checker | Inter-processor element Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 283 |  | Inter-cluster Bus (I-Bus) | √ | √ | | √ | √ | √ | √ | — | √ |
| 284 |  | Peripheral Bus (P-Bus) | √ | √ | | √ | √ | √ | √ | — | √ |
| 285 |  | CRAM Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 286 |  | System Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 287 |  | Global FLASH Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 288 |  | Local FLASH Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 289 |  | Reserve | — | — | | — | — | — | — | — | — |
| 290 |  | Reserve | — | — | | — | — | — | — | — | — |
| 291 |  | Reserve | — | — | | — | — | — | — | — | — |
| 292 | Voltage Monitor | EVCC Secondary HDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 293 |  | EVCC Secondary LDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 294 |  | VCC Secondary HDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 295 |  | VCC Secondary LDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 296 |  | VDD Secondary HDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 297 |  | VDD Secondary LDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 298 |  | Reserve | — | — | | — | — | — | — | — | — |
| 299 | Mode Error | Mode error  - Unintended activation of Production Test Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 300 |  | Mode error  - Unintended activation of Normal Operation Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 301 |  | Mode error  - Unintended deactivation of Normal Operation Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 302 |  | Mode error  - Unintended activation of Serial Programming Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 303 |  | Mode error  - Unintended activation of User Boot Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 304 |  | Mode error  - Unintended deactivation of User Boot Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 305 |  | Mode error  - Mode latch error | √ | √ | | √ | √ | √ | √ | — | √ |
| 306 | Reserve |  | — | — | | — | — | — | — | — | — |
| 307 | Reserve |  | — | — | | — | — | — | — | — | — |
| 308 | ECM | ECM compare error | √ | √ | | √ | √ | √ | √ | — | √ |
|  |  |  |  |  | |  |  |  |  |  |  |

1. The internal reset generation is enabled in the initial state.

Table 39.23 List of Error Inputs of E2UH

| No. | Module | Error sources | Error Flag  Set | | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | Dual Core Lock-step | DCLS compare error (PE0) | √ | | √ | √ | √ | √ | √ | √ | √ |
| 1 |  | DCLS compare error (PE1) | √ | | √ | √ | √ | √ | √ | √ | √ |
| 2 |  | Reserve | — | | — | — | — | — | — | — | — |
| 3 |  | Reserve | — | | — | — | — | — | — | — | — |
| 4 |  | DCLS compare error (PE4) | √ | | √ | √ | √ | √ | √ | √ | √ |
| 5 |  | DCLS compare error (PE5) | √ | | √ | √ | √ | √ | √ | √ | √ |
| 6 |  | Reserve | — | | — | — | — | — | — | — | — |
| 7 |  | Reserve | — | | — | — | — | — | — | — | — |
| 8 | Watchdog timer | Watchdog timer ch0 error (PE0) | √ | | √ | √ | √[\*](#Note1_FCC1)[1](#Note1_FCC1) | √ | √ | — | √ |
| 9 |  | Watchdog timer ch1 error (PE1) | √ | | √ | √ | √ | √ | √ | — | √ |
| 10 |  | Watchdog timer ch1 error (PE2) | √ | | √ | √ | √ | √ | √ | — | √ |
| 11 |  | Watchdog timer ch1 error (PE3) | √ | | √ | √ | √ | √ | √ | — | √ |
| 12 |  | Watchdog timer ch1 error (PE4) | √ | | √ | √ | √ | √ | √ | — | √ |
| 13 |  | Watchdog timer ch1 error (PE5) | √ | | √ | √ | √ | √ | √ | — | √ |
| 14 |  | Reserve | — | | — | — | — | — | — | — | — |
| 15 |  | Reserve | — | | — | — | — | — | — | — | — |
| 16 | Local RAM  (own core) | Local RAM (PE0)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 17 |  | Local RAM (PE1)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 18 |  | Local RAM (PE2)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 19 |  | Local RAM (PE3)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 20 |  | Local RAM (PE4)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 21 |  | Local RAM (PE5)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 22 |  | Reserve | — | | — | — | — | — | — | — | — |
| 23 |  | Reserve | — | | — | — | — | — | — | — | — |
| 24 |  | Local RAM ECC (PE0)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 25 |  | Local RAM ECC (PE1)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 26 |  | Local RAM ECC (PE2)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 27 |  | Local RAM ECC (PE3)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 28 |  | Local RAM ECC (PE4)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 29 |  | Local RAM ECC (PE5)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 30 |  | Reserve | — | | — | — | — | — | — | — | — |
| 31 | Local RAM  (own core) | Reserve | — | — | | — | — | — | — | — | — |
| 32 |  | Local RAM ECC (PE0)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 33 |  | Local RAM ECC (PE1)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 34 |  | Local RAM ECC (PE2)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 35 |  | Local RAM ECC (PE3)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 36 |  | Local RAM ECC (PE4)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 37 |  | Local RAM ECC (PE5)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 38 |  | Reserve | — | — | | — | — | — | — | — | — |
| 39 |  | Reserve | — | — | | — | — | — | — | — | — |
| 40 |  | Local RAM ECC (PE0)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 41 |  | Local RAM ECC (PE1)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 42 |  | Local RAM ECC (PE2)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 43 |  | Local RAM ECC (PE3)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 44 |  | Local RAM ECC (PE4)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 45 |  | Local RAM ECC (PE5)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 46 |  | Reserve | — | — | | — | — | — | — | — | — |
| 47 |  | Reserve | — | — | | — | — | — | — | — | — |
| 48 | Instruction Cache RAM | Instruction Cache RAM (PE0)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 49 |  | Instruction Cache RAM (PE1)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 50 |  | Instruction Cache RAM (PE2)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 51 |  | Instruction Cache RAM (PE3)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 52 |  | Instruction Cache RAM (PE4)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 53 |  | Instruction Cache RAM (PE5)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 54 |  | Reserve | — | — | | — | — | — | — | — | — |
| 55 |  | Reserve | — | — | | — | — | — | — | — | — |
| 56 |  | Instruction Cache RAM EDC (PE0)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 57 |  | Instruction Cache RAM EDC (PE1)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 58 |  | Instruction Cache RAM EDC (PE2)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 59 |  | Instruction Cache RAM EDC (PE3)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 60 |  | Instruction Cache RAM EDC (PE4)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 61 |  | Instruction Cache RAM EDC (PE5)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 62 |  | Reserve | — | — | | — | — | — | — | — | — |
| 63 |  | Reserve | — | — | | — | — | — | — | — | — |
| 64 |  | Reserve | — | — | | — | — | — | — | — | — |
| 65 |  | Reserve | — | — | | — | — | — | — | — | — |
| 66 |  | Reserve | — | — | | — | — | — | — | — | — |
| 67 |  | Reserve | — | — | | — | — | — | — | — | — |
| 68 |  | Reserve | — | — | | — | — | — | — | — | — |
| 69 |  | Reserve | — | — | | — | — | — | — | — | — |
| 70 |  | Reserve | — | — | | — | — | — | — | — | — |
| 71 |  | Reserve | — | — | | — | — | — | — | — | — |
| 72 | Reserve |  | — | — | | — | — | — | — | — | — |
| 73 | Reserve |  | — | — | | — | — | — | — | — | — |
| 74 | Reserve |  | — | — | | — | — | — | — | — | — |
| 75 | Reserve |  | — | — | | — | — | — | — | — | — |
| 76 | Reserve |  | — | — | | — | — | — | — | — | — |
| 77 | Reserve |  | — | — | | — | — | — | — | — | — |
| 78 | Reserve |  | — | — | | — | — | — | — | — | — |
| 79 | Reserve |  | — | — | | — | — | — | — | — | — |
| 80 | PE guard function (PEG) | PEG error (PE0) | √ | √ | | √ | √ | √ | √ | — | √ |
| 81 |  | PEG error (PE1) | √ | √ | | √ | √ | √ | √ | — | √ |
| 82 |  | PEG error (PE2) | √ | √ | | √ | √ | √ | √ | — | √ |
| 83 |  | PEG error (PE3) | √ | √ | | √ | √ | √ | √ | — | √ |
| 84 |  | PEG error (PE4) | √ | √ | | √ | √ | √ | √ | — | √ |
| 85 |  | PEG error (PE5) | √ | √ | | √ | √ | √ | √ | — | √ |
| 86 |  | Reserve | — | — | | — | — | — | — | — | — |
| 87 |  | Reserve | — | — | | — | — | — | — | — | — |
| 88 | Clock Monitor | Clock monitor error (CLMA5) (PE0) | √ | √ | | √ | √ | √ | √ | — | √ |
| 89 |  | Clock monitor error (CLMA6) (PE1) | √ | √ | | √ | √ | √ | √ | — | √ |
| 90 |  | Clock monitor error (CLMA7) (PE2) | √ | √ | | √ | √ | √ | √ | — | √ |
| 91 |  | Clock monitor error (CLMA8) (PE3) | √ | √ | | √ | √ | √ | √ | — | √ |
| 92 |  | Clock monitor error (CLMA9) (PE4) | √ | √ | | √ | √ | √ | √ | — | √ |
| 93 |  | Clock monitor error (CLMA10) (PE5) | √ | √ | | √ | √ | √ | √ | — | √ |
| 94 |  | Reserve | — | — | | — | — | — | — | — | — |
| 95 |  | Reserve | — | — | | — | — | — | — | — | — |
| 96 | OSTM | OSTM1 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 97 |  | OSTM2 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 98 |  | OSTM3 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 99 |  | OSTM4 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 100 |  | OSTM5 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 101 |  | OSTM6 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 102 |  | Reserve | — | — | | — | — | — | — | — | — |
| 103 |  | Reserve | — | — | | — | — | — | — | — | — |
| 104 | Reserve |  | — | — | | — | — | — | — | — | — |
| 105 | Reserve |  | — | — | | — | — | — | — | — | — |
| 106 | Reserve |  | — | — | | — | — | — | — | — | — |
| 107 | Reserve |  | — | — | | — | — | — | — | — | — |
| 108 | Reserve |  | — | — | | — | — | — | — | — | — |
| 109 | Reserve |  | — | — | | — | — | — | — | — | — |
| 110 | Reserve |  | — | — | | — | — | — | — | — | — |
| 111 | Reserve |  | — | — | | — | — | — | — | — | — |
| 112 | Mode Error | Unintended Debug Enable detection (PE0) | √ | √ | | √ | √ | √ | √ | — | √ |
| 113 |  | Unintended Debug Enable detection (PE1) | √ | √ | | √ | √ | √ | √ | — | √ |
| 114 |  | Unintended Debug Enable detection (PE2) | √ | √ | | √ | √ | √ | √ | — | √ |
| 115 |  | Unintended Debug Enable detection (PE3) | √ | √ | | √ | √ | √ | √ | — | √ |
| 116 |  | Unintended Debug Enable detection (PE4) | √ | √ | | √ | √ | √ | √ | — | √ |
| 117 |  | Unintended Debug Enable detection (PE5) | √ | √ | | √ | √ | √ | √ | — | √ |
| 118 |  | Reserve | — | — | | — | — | — | — | — | — |
| 119 |  | Reserve | — | — | | — | — | — | — | — | — |
| 120 | PEG error | PEG error (PE0) Detected in a read request from PE0 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 121 |  | PEG error (PE1) Detected in a read request from PE1 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 122 |  | PEG error (PE2) Detected in a read request from PE2 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 123 |  | PEG error (PE3) Detected in a read request from PE3 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 124 |  | PEG error (PE4) Detected in a read request from PE4 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 125 |  | PEG error (PE5) Detected in a read request from PE5 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 126 |  | Reserve | — | — | | — | — | — | — | — | — |
| 127 |  | Reserve | — | — | | — | — | — | — | — | — |
| 128 | Reserve |  | — | — | | — | — | — | — | — | — |
| 129 | Reserve |  | — | — | | — | — | — | — | — | — |
| 130 | Reserve |  | — | — | | — | — | — | — | — | — |
| 131 | Reserve |  | — | — | | — | — | — | — | — | — |
| 132 | Reserve |  | — | — | | — | — | — | — | — | — |
| 133 | Reserve |  | — | — | | — | — | — | — | — | — |
| 134 | Reserve |  | — | — | | — | — | — | — | — | — |
| 135 | Reserve |  | — | — | | — | — | — | — | — | — |
| 136 | Reserve |  | — | — | | — | — | — | — | — | — |
| 137 | Reserve |  | — | — | | — | — | — | — | — | — |
| 138 | Reserve |  | — | — | | — | — | — | — | — | — |
| 139 | Reserve |  | — | — | | — | — | — | — | — | — |
| 140 | Reserve |  | — | — | | — | — | — | — | — | — |
| 141 | Reserve |  | — | — | | — | — | — | — | — | — |
| 142 | Reserve |  | — | — | | — | — | — | — | — | — |
| 143 | Reserve |  | — | — | | — | — | — | — | — | — |
| 144 | Reserve |  | — | — | | — | — | — | — | — | — |
| 145 | Reserve |  | — | — | | — | — | — | — | — | — |
| 146 | Reserve |  | — | — | | — | — | — | — | — | — |
| 147 | Reserve |  | — | — | | — | — | — | — | — | — |
| 148 | Reserve |  | — | — | | — | — | — | — | — | — |
| 149 | Reserve |  | — | — | | — | — | — | — | — | — |
| 150 | Reserve |  | — | — | | — | — | — | — | — | — |
| 151 | Reserve |  | — | — | | — | — | — | — | — | — |
| 152 | Cluster RAM | Cluster RAM  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 153 |  | Cluster RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 154 |  | Cluster RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 155 |  | Cluster RAM ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 156 |  | Reserve | — | — | | — | — | — | — | — | — |
| 157 |  | Reserve | — | — | | — | — | — | — | — | — |
| 158 |  | Reserve | — | — | | — | — | — | — | — | — |
| 159 |  | Reserve | — | — | | — | — | — | — | — | — |
| 160 | Local RAM  (other core) | Reserve | — | — | | — | — | — | — | — | — |
| 161 |  | LRAM (error by other core access)  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 162 |  | LRAM (error by other core access)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 163 |  | LRAM (error by other core access)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 164 | sDMA | sDMAC0 RAM  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 165 |  | sDMAC0 RAM  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 166 |  | sDMAC1 RAM  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 167 |  | sDMAC1 RAM  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 168 | Peripheral RAM | Peripheral (DTS) RAM ECC  - ECC 2bit error  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 169 |  | Peripheral (DTS) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 170 |  | Peripheral (DTS) RAM ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 171 |  | Peripheral(except DTS) RAM ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 172 |  | Peripheral(FlexRay) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 173 |  | Peripheral(FlexRay) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 174 |  | Peripheral(CAN) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 175 |  | Peripheral(CAN) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 176 |  | Peripheral(DFE) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 177 |  | Peripheral(DFE) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 178 |  | Peripheral(GTM) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 179 |  | Peripheral(GTM) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 180 |  | Peripheral(Ethernet) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 181 |  | Peripheral(Ethernet) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 182 |  | Reserve | — | — | | — | — | — | — | — | — |
| 183 |  | Reserve | — | — | | — | — | — | — | — | — |
| 184 |  | Reserve | — | — | | — | — | — | — | — | — |
| 185 |  | Reserve | — | — | | — | — | — | — | — | — |
| 186 |  | Reserve | — | — | | — | — | — | — | — | — |
| 187 |  | Reserve | — | — | | — | — | — | — | — | — |
| 188 |  | Reserve | — | — | | — | — | — | — | — | — |
| 189 |  | Reserve | — | — | | — | — | — | — | — | — |
| 190 |  | Reserve | — | — | | — | — | — | — | — | — |
| 191 |  | Reserve | — | — | | — | — | — | — | — | — |
| 192 |  | Reserve | — | — | | — | — | — | — | — | — |
| 193 |  | Reserve | — | — | | — | — | — | — | — | — |
| 194 |  | Reserve | — | — | | — | — | — | — | — | — |
| 195 |  | Reserve | — | — | | — | — | — | — | — | — |
| 196 |  | Reserve | — | — | | — | — | — | — | — | — |
| 197 |  | Reserve | — | — | | — | — | — | — | — | — |
| 198 |  | Reserve | — | — | | — | — | — | — | — | — |
| 199 |  | Reserve | — | — | | — | — | — | — | — | — |
| 200 | Code Flash | Code Flash  - Address parity error | √ | √ | | √ | √ | √ | √ | — | √ |
| 201 |  | Code Flash ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 202 |  | Code Flash ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 203 |  | Code Flash ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 204 |  | Reserve | — | — | | — | — | — | — | — | — |
| 205 |  | Reserve | — | — | | — | — | — | — | — | — |
| 206 |  | Reserve | — | — | | — | — | — | — | — | — |
| 207 |  | Reserve | — | — | | — | — | — | — | — | — |
| 208 | Data Flash | Data Flash ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 209 |  | Data Flash ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 210 |  | Data Flash ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 211 |  | Reserve | — | — | | — | — | — | — | — | — |
| 212 |  | Reserve | — | — | | — | — | — | — | — | — |
| 213 |  | Reserve | — | — | | — | — | — | — | — | — |
| 214 |  | Reserve | — | — | | — | — | — | — | — | — |
| 215 |  | Reserve | — | — | | — | — | — | — | — | — |
| 216 | Bus ECC | Data Bus ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 217 |  | Data Bus ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 218 |  | Address Bus ECC  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 219 |  | Reserve | — | — | | — | — | — | — | — | — |
| 220 |  | Reserve | — | — | | — | — | — | — | — | — |
| 221 |  | Reserve | — | — | | — | — | — | — | — | — |
| 222 |  | Reserve | — | — | | — | — | — | — | — | — |
| 223 |  | Reserve | — | — | | — | — | — | — | — | — |
| 224 | Cluster RAM Guard (CRG) | CRAM Guard error | √ | √ | | √ | √ | √ | √ | — | √ |
| 225 | P-Bus Guard (PBG) | P-Bus Guard error | √ | √ | | √ | √ | √ | √ | — | √ |
| 226 | H-Bus Guard (HBG) | H-Bus Guard error | √ | √ | | √ | √ | √ | √ | — | √ |
| 227 | I-Bus Guard (IBG) | I-Bus Guard error  (IPIR MEV Barrier TPTM) | √ | √ | | √ | √ | √ | √ | — | √ |
| 228 | Reserve |  | — | — | | — | — | — | — | — | — |
| 229 | Reserve |  | — | — | | — | — | — | — | — | — |
| 230 | Reserve |  | — | — | | — | — | — | — | — | — |
| 231 | Reserve |  | — | — | | — | — | — | — | — | — |
| 232 | Clock Monitor | Clock monitor error (CLMA0) | √ | √ | | √ | √ | √ | √ | — | √ |
| 233 |  | Clock monitor error (CLMA1) | √ | √ | | √ | √ | √ | √ | — | √ |
| 234 |  | Clock monitor error (CLMA2) | √ | √ | | √ | √ | √ | √ | — | √ |
| 235 |  | Clock monitor error (CLMA3) | √ | √ | | √ | √ | √ | √ | — | √ |
| 236 |  | Clock monitor error (CLMA4) | √ | √ | | √ | √ | √ | √ | — | √ |
| 237 | Reserve |  | — | — | | — | — | — | — | — | — |
| 238 | Reserve |  | — | — | | — | — | — | — | — | — |
| 239 | Reserve |  | — | — | | — | — | — | — | — | — |
| 240 | DSADC  ADC  Cyclic ADC | AD parity error | √ | √ | | √ | √ | √ | √ | — | √ |
| 241 | MISG | MISG compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 242 | DTS | DTS compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 243 | External Error Input | ERRORIN | √ | √ | | √ | √ | √ | √ | — | √ |
| 244 | Flash | Flash access error | √ | √ | | √ | √ | √ | √ | — | √ |
| 245 |  | FACI reset transfer error | √ | — | | — | — | √ | — | — | — |
| 246 |  | FBIST parameter transfer error | √ | — | | — | — | √ | — | — | — |
| 247 |  | Reserve | — | — | | — | — | — | — | — | — |
| 248 | Reserve |  | — | — | | — | — | — | — | — | — |
| 249 | Reserve |  | — | — | | — | — | — | — | — | — |
| 250 | Reserve |  | — | — | | — | — | — | — | — | — |
| 251 | Reserve |  | — | — | | — | — | — | — | — | — |
| 252 | Reserve |  | — | — | | — | — | — | — | — | — |
| 253 | Reserve |  | — | — | | — | — | — | — | — | — |
| 254 | Reserve |  | — | — | | — | — | — | — | — | — |
| 255 | Reserve |  | — | — | | — | — | — | — | — | — |
| 256 | Reserve |  | — | — | | — | — | — | — | — | — |
| 257 | Reserve |  | — | — | | — | — | — | — | — | — |
| 258 | Reserve |  | — | — | | — | — | — | — | — | — |
| 259 | Reserve |  | — | — | | — | — | — | — | — | — |
| 260 | Reserve |  | — | — | | — | — | — | — | — | — |
| 261 | Reserve |  | — | — | | — | — | — | — | — | — |
| 262 | Reserve |  | — | — | | — | — | — | — | — | — |
| 263 | Reserve |  | — | — | | — | — | — | — | — | — |
| 264 | Reserve |  | — | — | | — | — | — | — | — | — |
| 265 | Reserve |  | — | — | | — | — | — | — | — | — |
| 266 | Reserve |  | — | — | | — | — | — | — | — | — |
| 267 | Reserve |  | — | — | | — | — | — | — | — | — |
| 268 | Reserve |  | — | — | | — | — | — | — | — | — |
| 269 | Reserve |  | — | — | | — | — | — | — | — | — |
| 270 | Reserve |  | — | — | | — | — | — | — | — | — |
| 271 | Reserve |  | — | — | | — | — | — | — | — | — |
| 272 | Reserve |  | — | — | | — | — | — | — | — | — |
| 273 | Reserve |  | — | — | | — | — | — | — | — | — |
| 274 | Reserve |  | — | — | | — | — | — | — | — | — |
| 275 | Reserve |  | — | — | | — | — | — | — | — | — |
| 276 | Reserve |  | — | — | | — | — | — | — | — | — |
| 277 | Reserve |  | — | — | | — | — | — | — | — | — |
| 278 | Reserve |  | — | — | | — | — | — | — | — | — |
| 279 | Reserve |  | — | — | | — | — | — | — | — | — |
| 280 | Data Path Redundancy | DMA Comp error | √ | √ | | √ | √ | √ | √ | — | √ |
| 281 |  | BUS Bridge Comp error | √ | √ | | √ | √ | √ | √ | — | √ |
| 282 | BUS Routing checker | Inter-processor element Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 283 |  | Inter-cluster Bus (I-Bus) | √ | √ | | √ | √ | √ | √ | — | √ |
| 284 |  | Peripheral Bus (P-Bus) | √ | √ | | √ | √ | √ | √ | — | √ |
| 285 |  | CRAM Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 286 |  | System Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 287 |  | Global FLASH Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 288 |  | Local FLASH Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 289 |  | Reserve | — | — | | — | — | — | — | — | — |
| 290 |  | Reserve | — | — | | — | — | — | — | — | — |
| 291 |  | Reserve | — | — | | — | — | — | — | — | — |
| 292 | Voltage Monitor | EVCC Secondary HDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 293 |  | EVCC Secondary LDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 294 |  | VCC Secondary HDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 295 |  | VCC Secondary LDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 296 |  | VDD Secondary HDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 297 |  | VDD Secondary LDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 298 |  | Reserve | — | — | | — | — | — | — | — | — |
| 299 | Mode Error | Mode error  - Unintended activation of Production Test Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 300 |  | Mode error  - Unintended activation of Normal Operation Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 301 |  | Mode error  - Unintended deactivation of Normal Operation Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 302 |  | Mode error  - Unintended activation of Serial Programming Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 303 |  | Mode error  - Unintended activation of User Boot Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 304 |  | Mode error  - Unintended deactivation of User Boot Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 305 |  | Mode error  - Mode latch error | √ | √ | | √ | √ | √ | √ | — | √ |
| 306 | Reserve |  | — | — | | — | — | — | — | — | — |
| 307 | Reserve |  | — | — | | — | — | — | — | — | — |
| 308 | ECM | ECM compare error | √ | √ | | √ | √ | √ | √ | — | √ |

1. The internal reset generation is enabled in the initial state.

Table 39.24 List of Error Inputs of E2H

| No. | Module | Error sources | Error Flag  Set | | Maskable Interrupt | FE level Interrupt | Internal  Reset | ERROROUT Output | Delay Timer Start | DCLS Error Interrupt | Port Safe State |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | Dual Core Lock-step | DCLS compare error (PE0) | √ | | √ | √ | √ | √ | √ | √ | √ |
| 1 |  | DCLS compare error (PE1) | √ | | √ | √ | √ | √ | √ | √ | √ |
| 2 |  | Reserve | — | | — | — | — | — | — | — | — |
| 3 |  | Reserve | — | | — | — | — | — | — | — | — |
| 4 |  | Reserve | — | | — | — | — | — | — | — | — |
| 5 |  | Reserve | — | | — | — | — | — | — | — | — |
| 6 |  | Reserve | — | | — | — | — | — | — | — | — |
| 7 |  | Reserve | — | | — | — | — | — | — | — | — |
| 8 | Watchdog timer | Watchdog timer ch0 error (PE0) | √ | | √ | √ | √[\*](#Note1_FCC1)[1](#Note1_FCC1) | √ | √ | — | √ |
| 9 |  | Watchdog timer ch1 error (PE1) | √ | | √ | √ | √ | √ | √ | — | √ |
| 10 |  | Watchdog timer ch1 error (PE2) | √ | | √ | √ | √ | √ | √ | — | √ |
| 11 |  | Watchdog timer ch1 error (PE3) | √ | | √ | √ | √ | √ | √ | — | √ |
| 12 |  | Reserve | — | | — | — | — | — | — | — | — |
| 13 |  | Reserve | — | | — | — | — | — | — | — | — |
| 14 |  | Reserve | — | | — | — | — | — | — | — | — |
| 15 |  | Reserve | — | | — | — | — | — | — | — | — |
| 16 | Local RAM  (own core) | Local RAM (PE0)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 17 |  | Local RAM (PE1)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 18 |  | Local RAM (PE2)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 19 |  | Local RAM (PE3)  - Address feedback compare error | √ | | √ | √ | √ | √ | √ | — | √ |
| 20 |  | Reserve | — | | — | — | — | — | — | — | — |
| 21 |  | Reserve | — | | — | — | — | — | — | — | — |
| 22 |  | Reserve | — | | — | — | — | — | — | — | — |
| 23 |  | Reserve | — | | — | — | — | — | — | — | — |
| 24 |  | Local RAM ECC (PE0)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 25 |  | Local RAM ECC (PE1)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 26 |  | Local RAM ECC (PE2)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 27 |  | Local RAM ECC (PE3)  - ECC 2bit error | √ | | √ | √ | √ | √ | √ | — | √ |
| 28 |  | Reserve | — | | — | — | — | — | — | — | — |
| 29 |  | Reserve | — | | — | — | — | — | — | — | — |
| 30 |  | Reserve | — | | — | — | — | — | — | — | — |
| 31 | Local RAM  (own core) | Reserve | — | — | | — | — | — | — | — | — |
| 32 |  | Local RAM ECC (PE0)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 33 |  | Local RAM ECC (PE1)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 34 |  | Local RAM ECC (PE2)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 35 |  | Local RAM ECC (PE3)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 36 |  | Reserve | — | — | | — | — | — | — | — | — |
| 37 |  | Reserve | — | — | | — | — | — | — | — | — |
| 38 |  | Reserve | — | — | | — | — | — | — | — | — |
| 39 |  | Reserve | — | — | | — | — | — | — | — | — |
| 40 |  | Local RAM ECC (PE0)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 41 |  | Local RAM ECC (PE1)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 42 |  | Local RAM ECC (PE2)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 43 |  | Local RAM ECC (PE3)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 44 |  | Reserve | — | — | | — | — | — | — | — | — |
| 45 |  | Reserve | — | — | | — | — | — | — | — | — |
| 46 |  | Reserve | — | — | | — | — | — | — | — | — |
| 47 |  | Reserve | — | — | | — | — | — | — | — | — |
| 48 | Instruction Cache RAM | Instruction Cache RAM (PE0)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 49 |  | Instruction Cache RAM (PE1)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 50 |  | Instruction Cache RAM (PE2)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 51 |  | Instruction Cache RAM (PE3)  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 52 |  | Reserve | — | — | | — | — | — | — | — | — |
| 53 |  | Reserve | — | — | | — | — | — | — | — | — |
| 54 |  | Reserve | — | — | | — | — | — | — | — | — |
| 55 |  | Reserve | — | — | | — | — | — | — | — | — |
| 56 |  | Instruction Cache RAM EDC (PE0)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 57 |  | Instruction Cache RAM EDC (PE1)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 58 |  | Instruction Cache RAM EDC (PE2)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 59 |  | Instruction Cache RAM EDC (PE3)  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 60 |  | Reserve | — | — | | — | — | — | — | — | — |
| 61 |  | Reserve | — | — | | — | — | — | — | — | — |
| 62 |  | Reserve | — | — | | — | — | — | — | — | — |
| 63 |  | Reserve | — | — | | — | — | — | — | — | — |
| 64 |  | Reserve | — | — | | — | — | — | — | — | — |
| 65 |  | Reserve | — | — | | — | — | — | — | — | — |
| 66 |  | Reserve | — | — | | — | — | — | — | — | — |
| 67 |  | Reserve | — | — | | — | — | — | — | — | — |
| 68 |  | Reserve | — | — | | — | — | — | — | — | — |
| 69 |  | Reserve | — | — | | — | — | — | — | — | — |
| 70 |  | Reserve | — | — | | — | — | — | — | — | — |
| 71 |  | Reserve | — | — | | — | — | — | — | — | — |
| 72 | Reserve |  | — | — | | — | — | — | — | — | — |
| 73 | Reserve |  | — | — | | — | — | — | — | — | — |
| 74 | Reserve |  | — | — | | — | — | — | — | — | — |
| 75 | Reserve |  | — | — | | — | — | — | — | — | — |
| 76 | Reserve |  | — | — | | — | — | — | — | — | — |
| 77 | Reserve |  | — | — | | — | — | — | — | — | — |
| 78 | Reserve |  | — | — | | — | — | — | — | — | — |
| 79 | Reserve |  | — | — | | — | — | — | — | — | — |
| 80 | PE guard function (PEG) | PEG error (PE0) | √ | √ | | √ | √ | √ | √ | — | √ |
| 81 |  | PEG error (PE1) | √ | √ | | √ | √ | √ | √ | — | √ |
| 82 |  | PEG error (PE2) | √ | √ | | √ | √ | √ | √ | — | √ |
| 83 |  | PEG error (PE3) | √ | √ | | √ | √ | √ | √ | — | √ |
| 84 |  | Reserve | — | — | | — | — | — | — | — | — |
| 85 |  | Reserve | — | — | | — | — | — | — | — | — |
| 86 |  | Reserve | — | — | | — | — | — | — | — | — |
| 87 |  | Reserve | — | — | | — | — | — | — | — | — |
| 88 | Clock Monitor | Clock monitor error (CLMA5) (PE0) | √ | √ | | √ | √ | √ | √ | — | √ |
| 89 |  | Clock monitor error (CLMA6) (PE1) | √ | √ | | √ | √ | √ | √ | — | √ |
| 90 |  | Clock monitor error (CLMA7) (PE2) | √ | √ | | √ | √ | √ | √ | — | √ |
| 91 |  | Clock monitor error (CLMA8) (PE3) | √ | √ | | √ | √ | √ | √ | — | √ |
| 92 |  | Reserve | — | — | | — | — | — | — | — | — |
| 93 |  | Reserve | — | — | | — | — | — | — | — | — |
| 94 |  | Reserve | — | — | | — | — | — | — | — | — |
| 95 |  | Reserve | — | — | | — | — | — | — | — | — |
| 96 | OSTM | OSTM1 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 97 |  | OSTM2 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 98 |  | OSTM3 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 99 |  | OSTM4 Interrupt | √ | √ | | √ | √ | √ | √ | — | √ |
| 100 |  | Reserve | — | — | | — | — | — | — | — | — |
| 101 |  | Reserve | — | — | | — | — | — | — | — | — |
| 102 |  | Reserve | — | — | | — | — | — | — | — | — |
| 103 |  | Reserve | — | — | | — | — | — | — | — | — |
| 104 | Reserve |  | — | — | | — | — | — | — | — | — |
| 105 | Reserve |  | — | — | | — | — | — | — | — | — |
| 106 | Reserve |  | — | — | | — | — | — | — | — | — |
| 107 | Reserve |  | — | — | | — | — | — | — | — | — |
| 108 | Reserve |  | — | — | | — | — | — | — | — | — |
| 109 | Reserve |  | — | — | | — | — | — | — | — | — |
| 110 | Reserve |  | — | — | | — | — | — | — | — | — |
| 111 | Reserve |  | — | — | | — | — | — | — | — | — |
| 112 | Mode Error | Unintended Debug Enable detection (PE0) | √ | √ | | √ | √ | √ | √ | — | √ |
| 113 |  | Unintended Debug Enable detection (PE1) | √ | √ | | √ | √ | √ | √ | — | √ |
| 114 |  | Unintended Debug Enable detection (PE2) | √ | √ | | √ | √ | √ | √ | — | √ |
| 115 |  | Unintended Debug Enable detection (PE3) | √ | √ | | √ | √ | √ | √ | — | √ |
| 116 |  | Reserve | — | — | | — | — | — | — | — | — |
| 117 |  | Reserve | — | — | | — | — | — | — | — | — |
| 118 |  | Reserve | — | — | | — | — | — | — | — | — |
| 119 |  | Reserve | — | — | | — | — | — | — | — | — |
| 120 | PEG error | PEG error (PE0) Detected in a read request from PE0 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 121 |  | PEG error (PE1) Detected in a read request from PE1 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 122 |  | PEG error (PE2) Detected in a read request from PE2 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 123 |  | PEG error (PE3) Detected in a read request from PE3 to the others LRAM | √ | √ | | √ | √ | √ | √ | — | √ |
| 124 |  | Reserve | — | — | | — | — | — | — | — | — |
| 125 |  | Reserve | — | — | | — | — | — | — | — | — |
| 126 |  | Reserve | — | — | | — | — | — | — | — | — |
| 127 |  | Reserve | — | — | | — | — | — | — | — | — |
| 128 | Reserve |  | — | — | | — | — | — | — | — | — |
| 129 | Reserve |  | — | — | | — | — | — | — | — | — |
| 130 | Reserve |  | — | — | | — | — | — | — | — | — |
| 131 | Reserve |  | — | — | | — | — | — | — | — | — |
| 132 | Reserve |  | — | — | | — | — | — | — | — | — |
| 133 | Reserve |  | — | — | | — | — | — | — | — | — |
| 134 | Reserve |  | — | — | | — | — | — | — | — | — |
| 135 | Reserve |  | — | — | | — | — | — | — | — | — |
| 136 | Reserve |  | — | — | | — | — | — | — | — | — |
| 137 | Reserve |  | — | — | | — | — | — | — | — | — |
| 138 | Reserve |  | — | — | | — | — | — | — | — | — |
| 139 | Reserve |  | — | — | | — | — | — | — | — | — |
| 140 | Reserve |  | — | — | | — | — | — | — | — | — |
| 141 | Reserve |  | — | — | | — | — | — | — | — | — |
| 142 | Reserve |  | — | — | | — | — | — | — | — | — |
| 143 | Reserve |  | — | — | | — | — | — | — | — | — |
| 144 | Reserve |  | — | — | | — | — | — | — | — | — |
| 145 | Reserve |  | — | — | | — | — | — | — | — | — |
| 146 | Reserve |  | — | — | | — | — | — | — | — | — |
| 147 | Reserve |  | — | — | | — | — | — | — | — | — |
| 148 | Reserve |  | — | — | | — | — | — | — | — | — |
| 149 | Reserve |  | — | — | | — | — | — | — | — | — |
| 150 | Reserve |  | — | — | | — | — | — | — | — | — |
| 151 | Reserve |  | — | — | | — | — | — | — | — | — |
| 152 | Cluster RAM | Cluster RAM  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 153 |  | Cluster RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 154 |  | Cluster RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 155 |  | Cluster RAM ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 156 |  | Reserve | — | — | | — | — | — | — | — | — |
| 157 |  | Reserve | — | — | | — | — | — | — | — | — |
| 158 |  | Reserve | — | — | | — | — | — | — | — | — |
| 159 |  | Reserve | — | — | | — | — | — | — | — | — |
| 160 | Local RAM  (other core) | Reserve | — | — | | — | — | — | — | — | — |
| 161 |  | LRAM (error by other core access)  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 162 |  | LRAM (error by other core access)  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 163 |  | LRAM (error by other core access)  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 164 | sDMA | sDMAC0 RAM  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 165 |  | sDMAC0 RAM  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 166 |  | sDMAC1 RAM  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 167 |  | sDMAC1 RAM  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 168 | Peripheral RAM | Peripheral (DTS) RAM ECC  - ECC 2bit error  - Address feedback compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 169 |  | Peripheral (DTS) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 170 |  | Peripheral (DTS) RAM ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 171 |  | Peripheral(except DTS) RAM ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 172 |  | Peripheral(FlexRay) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 173 |  | Peripheral(FlexRay) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 174 |  | Peripheral(CAN) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 175 |  | Peripheral(CAN) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 176 |  | Peripheral(DFE) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 177 |  | Peripheral(DFE) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 178 |  | Peripheral(GTM) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 179 |  | Peripheral(GTM) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 180 |  | Peripheral(Ethernet) RAM ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 181 |  | Peripheral(Ethernet) RAM ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 182 |  | Reserve | — | — | | — | — | — | — | — | — |
| 183 |  | Reserve | — | — | | — | — | — | — | — | — |
| 184 |  | Reserve | — | — | | — | — | — | — | — | — |
| 185 |  | Reserve | — | — | | — | — | — | — | — | — |
| 186 |  | Reserve | — | — | | — | — | — | — | — | — |
| 187 |  | Reserve | — | — | | — | — | — | — | — | — |
| 188 |  | Reserve | — | — | | — | — | — | — | — | — |
| 189 |  | Reserve | — | — | | — | — | — | — | — | — |
| 190 |  | Reserve | — | — | | — | — | — | — | — | — |
| 191 |  | Reserve | — | — | | — | — | — | — | — | — |
| 192 |  | Reserve | — | — | | — | — | — | — | — | — |
| 193 |  | Reserve | — | — | | — | — | — | — | — | — |
| 194 |  | Reserve | — | — | | — | — | — | — | — | — |
| 195 |  | Reserve | — | — | | — | — | — | — | — | — |
| 196 |  | Reserve | — | — | | — | — | — | — | — | — |
| 197 |  | Reserve | — | — | | — | — | — | — | — | — |
| 198 |  | Reserve | — | — | | — | — | — | — | — | — |
| 199 |  | Reserve | — | — | | — | — | — | — | — | — |
| 200 | Code Flash | Code Flash  - Address parity error | √ | √ | | √ | √ | √ | √ | — | √ |
| 201 |  | Code Flash ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 202 |  | Code Flash ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 203 |  | Code Flash ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 204 |  | Reserve | — | — | | — | — | — | — | — | — |
| 205 |  | Reserve | — | — | | — | — | — | — | — | — |
| 206 |  | Reserve | — | — | | — | — | — | — | — | — |
| 207 |  | Reserve | — | — | | — | — | — | — | — | — |
| 208 | Data Flash | Data Flash ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 209 |  | Data Flash ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 210 |  | Data Flash ECC  - Error address overflow | √ | √ | | √ | √ | √ | √ | — | √ |
| 211 |  | Reserve | — | — | | — | — | — | — | — | — |
| 212 |  | Reserve | — | — | | — | — | — | — | — | — |
| 213 |  | Reserve | — | — | | — | — | — | — | — | — |
| 214 |  | Reserve | — | — | | — | — | — | — | — | — |
| 215 |  | Reserve | — | — | | — | — | — | — | — | — |
| 216 | Bus ECC | Data Bus ECC  - ECC 2bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 217 |  | Data Bus ECC  - ECC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 218 |  | Address Bus ECC  - EDC 2bit error  - EDC 1bit error | √ | √ | | √ | √ | √ | √ | — | √ |
| 219 |  | Reserve | — | — | | — | — | — | — | — | — |
| 220 |  | Reserve | — | — | | — | — | — | — | — | — |
| 221 |  | Reserve | — | — | | — | — | — | — | — | — |
| 222 |  | Reserve | — | — | | — | — | — | — | — | — |
| 223 |  | Reserve | — | — | | — | — | — | — | — | — |
| 224 | Cluster RAM Guard (CRG) | CRAM Guard error | √ | √ | | √ | √ | √ | √ | — | √ |
| 225 | P-Bus Guard (PBG) | P-Bus Guard error | √ | √ | | √ | √ | √ | √ | — | √ |
| 226 | H-Bus Guard (HBG) | H-Bus Guard error | √ | √ | | √ | √ | √ | √ | — | √ |
| 227 | I-Bus Guard (IBG) | I-Bus Guard error  (IPIR MEV Barrier TPTM) | √ | √ | | √ | √ | √ | √ | — | √ |
| 228 | Reserve |  | — | — | | — | — | — | — | — | — |
| 229 | Reserve |  | — | — | | — | — | — | — | — | — |
| 230 | Reserve |  | — | — | | — | — | — | — | — | — |
| 231 | Reserve |  | — | — | | — | — | — | — | — | — |
| 232 | Clock Monitor | Clock monitor error (CLMA0) | √ | √ | | √ | √ | √ | √ | — | √ |
| 233 |  | Clock monitor error (CLMA1) | √ | √ | | √ | √ | √ | √ | — | √ |
| 234 |  | Clock monitor error (CLMA2) | √ | √ | | √ | √ | √ | √ | — | √ |
| 235 |  | Clock monitor error (CLMA3) | √ | √ | | √ | √ | √ | √ | — | √ |
| 236 |  | Clock monitor error (CLMA4) | √ | √ | | √ | √ | √ | √ | — | √ |
| 237 | Reserve |  | — | — | | — | — | — | — | — | — |
| 238 | Reserve |  | — | — | | — | — | — | — | — | — |
| 239 | Reserve |  | — | — | | — | — | — | — | — | — |
| 240 | DSADC  ADC  Cyclic ADC | AD parity error | √ | √ | | √ | √ | √ | √ | — | √ |
| 241 | MISG | MISG compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 242 | DTS | DTS compare error | √ | √ | | √ | √ | √ | √ | — | √ |
| 243 | External Error Input | ERRORIN | √ | √ | | √ | √ | √ | √ | — | √ |
| 244 | Flash | Flash access error | √ | √ | | √ | √ | √ | √ | — | √ |
| 245 |  | FACI reset transfer error | √ | — | | — | — | √ | — | — | — |
| 246 |  | FBIST parameter transfer error | √ | — | | — | — | √ | — | — | — |
| 247 |  | Reserve | — | — | | — | — | — | — | — | — |
| 248 | Reserve |  | — | — | | — | — | — | — | — | — |
| 249 | Reserve |  | — | — | | — | — | — | — | — | — |
| 250 | Reserve |  | — | — | | — | — | — | — | — | — |
| 251 | Reserve |  | — | — | | — | — | — | — | — | — |
| 252 | Reserve |  | — | — | | — | — | — | — | — | — |
| 253 | Reserve |  | — | — | | — | — | — | — | — | — |
| 254 | Reserve |  | — | — | | — | — | — | — | — | — |
| 255 | Reserve |  | — | — | | — | — | — | — | — | — |
| 256 | Reserve |  | — | — | | — | — | — | — | — | — |
| 257 | Reserve |  | — | — | | — | — | — | — | — | — |
| 258 | Reserve |  | — | — | | — | — | — | — | — | — |
| 259 | Reserve |  | — | — | | — | — | — | — | — | — |
| 260 | Reserve |  | — | — | | — | — | — | — | — | — |
| 261 | Reserve |  | — | — | | — | — | — | — | — | — |
| 262 | Reserve |  | — | — | | — | — | — | — | — | — |
| 263 | Reserve |  | — | — | | — | — | — | — | — | — |
| 264 | Reserve |  | — | — | | — | — | — | — | — | — |
| 265 | Reserve |  | — | — | | — | — | — | — | — | — |
| 266 | Reserve |  | — | — | | — | — | — | — | — | — |
| 267 | Reserve |  | — | — | | — | — | — | — | — | — |
| 268 | Reserve |  | — | — | | — | — | — | — | — | — |
| 269 | Reserve |  | — | — | | — | — | — | — | — | — |
| 270 | Reserve |  | — | — | | — | — | — | — | — | — |
| 271 | Reserve |  | — | — | | — | — | — | — | — | — |
| 272 | Reserve |  | — | — | | — | — | — | — | — | — |
| 273 | Reserve |  | — | — | | — | — | — | — | — | — |
| 274 | Reserve |  | — | — | | — | — | — | — | — | — |
| 275 | Reserve |  | — | — | | — | — | — | — | — | — |
| 276 | Reserve |  | — | — | | — | — | — | — | — | — |
| 277 | Reserve |  | — | — | | — | — | — | — | — | — |
| 278 | Reserve |  | — | — | | — | — | — | — | — | — |
| 279 | Reserve |  | — | — | | — | — | — | — | — | — |
| 280 | Data Path Redundancy | DMA Comp error | √ | √ | | √ | √ | √ | √ | — | √ |
| 281 |  | BUS Bridge Comp error | √ | √ | | √ | √ | √ | √ | — | √ |
| 282 | BUS Routing checker | Inter-processor element Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 283 |  | Inter-cluster Bus (I-Bus) | √ | √ | | √ | √ | √ | √ | — | √ |
| 284 |  | Peripheral Bus (P-Bus) | √ | √ | | √ | √ | √ | √ | — | √ |
| 285 |  | CRAM Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 286 |  | System Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 287 |  | Global FLASH Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 288 |  | Local FLASH Bus | √ | √ | | √ | √ | √ | √ | — | √ |
| 289 |  | Reserve | — | — | | — | — | — | — | — | — |
| 290 |  | Reserve | — | — | | — | — | — | — | — | — |
| 291 |  | Reserve | — | — | | — | — | — | — | — | — |
| 292 | Voltage Monitor | EVCC Secondary HDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 293 |  | EVCC Secondary LDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 294 |  | VCC Secondary HDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 295 |  | VCC Secondary LDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 296 |  | VDD Secondary HDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 297 |  | VDD Secondary LDET | √ | √ | | √ | √ | √ | √ | — | √ |
| 298 |  | Reserve | — | — | | — | — | — | — | — | — |
| 299 | Mode Error | Mode error  - Unintended activation of Production Test Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 300 |  | Mode error  - Unintended activation of Normal Operation Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 301 |  | Mode error  - Unintended deactivation of Normal Operation Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 302 |  | Mode error  - Unintended activation of Serial Programming Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 303 |  | Mode error  - Unintended activation of User Boot Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 304 |  | Mode error  - Unintended deactivation of User Boot Mode | √ | √ | | √ | √ | √ | √ | — | √ |
| 305 |  | Mode error  - Mode latch error | √ | √ | | √ | √ | √ | √ | — | √ |
| 306 | Reserve |  | — | — | | — | — | — | — | — | — |
| 307 | Reserve |  | — | — | | — | — | — | — | — | — |
| 308 | ECM | ECM compare error | √ | √ | | √ | √ | √ | √ | — | √ |

1. The internal reset generation is enabled in the initial state.

### Operations for Error Output

After reset release, the pin outputs the low (error) level. Follow the procedure described in Section 39.3.3, ECMmECLR ― ECM Master/Checker Error Clear Trigger Register (m = M/C) , to clear the error before using ECM. As the pin is multiplexed with a general-purpose port and other functions, select the function before use. For settings, see Section 2, Pin Function.

The error output can be configured for two different modes of operation, non-dynamic or dynamic.

The error output is in synchronization with the occurrence of error source conditions and the error level is output as the pin state regardless of the dynamic mode pulse cycle.

ERROROUTZ connects to port safe state and ECM can control the state of general purpose I/O to safe state according to user configuration. For details of function, see Section 2, Pin Function. ERROROUTZ can be used as only non-dynamic mode.

Table . Operation for Error Output

| Error Status  ECMmSSE | Operating Mode  ECMEPCFG.ECMSL0 Bit | Error Output  Operating Mode | Error Output Level\*1 | ERROROUTZ\*1 | Error Status |
| --- | --- | --- | --- | --- | --- |
| 0 | 0 | Non-dynamic | H | H | No error |
| 1 | Dynamic | Toggles  (according to timer input) | H | No error |
| 1 | 0 | Non-dynamic | L | L | Error |
| 1 | Dynamic | L | L | Error |

1. The level of the error output (and) and ERROROUTZ can be masked by ECMEMKn registers value.

### and Behavior at Reset

Below table explains the behavior of the error output logic and theandpins at reset. Also the level of theandsignals during and after reset is explained.

Table . Behavior at Reset

| Category | Reset Condition | | | | | |
| --- | --- | --- | --- | --- | --- | --- |
| Power Up Reset | System Reset 1 | System Reset 2 | Application Reset | Module Reset | JTAG Reset |
| pin level during reset | Low level | Low level | Level according to error status before reset\*1 | Level according to error status before reset\*1 | Level according to error status before reset | Level according to error status before reset |
| pin level after reset | Low level | Low level | Level according to error status before reset\*1 | Level according to error status before reset\*1 | Level according to error status before reset | Level according to error status before reset |

1. The level of the can be changed by clearing ECMEMKn registers at reset. To keep the level, it is necessary to clear the ECMMESSTRn bit which corresponds to ECMEMKn bit of setting which masked error signal output before reset.

Table . Behavior at Reset

| Category | Reset Condition | | | | | |
| --- | --- | --- | --- | --- | --- | --- |
| Power Up Reset | System Reset 1 | System Reset 2 | Application Reset | Module Reset | JTAG Reset |
| pin level during reset | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Level according to error status before reset | Level according to error status before reset |
| pin level after reset | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Level according to error status before reset | Level according to error status before reset |

#### Dynamic Mode Enable

1. Initialize the related timer OSTM0.
2. Set the error output to high level by setting the ECMmECT (m = M/C) bit in the ECM master/checker error clear trigger register to 1.
3. Set the ECMEPCFG.ECMSL0 bit to 1 for dynamic mode.
4. Start the timer OSTM0.

#### Dynamic Mode Disable

1. Set the error output to low level by setting the ECMmEST bit (m = M/C) in the ECM master/checker error set trigger register to 1.
2. Stop the timer OSTM0.
3. Clear the ECMSL0 bit in the ECM error pulse configuration register to 0 to specify non-dynamic mode.

### Loop-Back Function

ECM incorporates a loop-back function that is used to check the path to the error output pin. The output level of the error output pin can be checked with the ECMmSSE311 bit (m = M/C) in the ECM master/checker error source status register 9.

#### Example of a Loop-Back Test after Reset

1. After Power up reset or System reset 1, the error output has a “low level”.
2. Read the ECMMESSTR9.ECMMSSE311 and ECMCESSTR9.ECMCSSE311 bits and check for “0”.
3. Clear all internal error sources by the ECMESSTC registers.
4. Mask “ECM compare error” by setting the ECMEMK9.ECMEMK308 bit.
5. Set error output to “high level” by the ECMMECLR and ECMCECLR registers.
6. Read the ECMMESSTR9.ECMMSSE311 and ECMCESSTR9.ECMCSSE311 bits and check for “1”.
7. Set error output to “low level” by the ECMMESET register.
8. Read the ECMMESSTR9.ECMMSSE311 and ECMCESSTR9.ECMCSSE311 bits and check for “0”
9. Clear the error by the ECMESSTC9.ECMCLSSE310 bit.
10. Set error output to “high level” by the ECMmECLR register.
11. Read the ECMmESSTR9.ECMMSSE311 and ECMCESSTR9.ECMCSSE311 bits and check for “1”.
12. Set error output to “low level” by the ECMCESET register.
13. Read the ECMMESSTR9.ECMMSSE311 and ECMCESSTR9.ECMCSSE311 bits and check for "0".
14. Set error output to "low level" by the ECMMESET and ECMCESET registers.
15. Clear the error by the ECMESSTC9.ECMCLSSE308 bit.
16. Unmask "ECM compare error" by clearing the ECMEMK9.ECMEMK308 bit.

### Pseudo Error Generation

ECM incorporates a function that can generate pseudo errors for test or debug purposes. The operation of the ECM during injection of pseudo errors is identical to that for the occurrence of real errors. All configurations for error masks, interrupt, internal reset, or delay timer apply in the same way.

### Pseudo Error Generation for Errorout binder

Error signals from ECM Master and Checker instance can be controlled individually. This enables full testing of the Errorout binder function. All possible input patter (01/10/11) can be stimulated. Error injection input for Errorout binder is assigned to “ECM compare error”.

****

Figure 39.3 Pseudo Error Generation for Errorout Binder Test

NOTE

This Section is listed in Safety Application note.

### Error Status

The error status is indicated by ECM master/checker error source status registers. The error status is only cleared by software, power up reset or standby reset. In case of reset except for power up reset and standby reset, the error status is kept and the error of the reset source can be confirmed by reading the ECM master/checker error source status registers after reset release.

### Register Protection

Write protected registers are protected from inadvertent write access due to erroneous program execution, etc.

By releasing the protection of ECMKCPROT, it can be written. For details, see Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register.

### Timeout Function for Interrupt Processing

The delay timer incorporated to ECM can be started simultaneously with the occurrence of an interrupt request. ECM incorporates a function that generates an error signal output or Error Control Module Reset when the count value of the delay timer matches with the value of the delay timer compare register because the delay timer was not stopped during the interrupt processing. The timer counting is not stopped when a break occurs.

The counting of the delay timer always starts from 0. Configure the duration until an Error Control Module Reset or error output is generated with the settings of the delay timer compare register.

### Masking of “Error Clear Trigger Register”

The active error output status must be cleared by software via the Error clear trigger register (ECMMECLR/ECMCECLR). A minimum activation time of the error output is achieved by the Error output clear invalidation counter. This counter is (re)started each time a new error event is triggered at the ECM. It counts up from 0000H to FFFFH. Error output clear by software is not possible unless this counter reaches the compare value configured in the ECMEOCCFG register. If Error output clear invalidation counter is still running, Error output clear is masked and Error output clear request by software is not memorized.

### DCLS Error Interrupt (EI Level) and EI Level Interrupt

This module can generate specific interrupts of DCLS error for each CPU. When DCLS error is occurred in the state of setting the ECMMICFG0, DCLS error interrupt and EI level interrupt are generated. The following figure shows the generation logic of DCLS error interrupt and EI level interrupt from ECM. For each PEn (n = 0, 1), EI level interrupt of CPUn is generated by EI level interrupt from ECM master, ECM checker and other DCLS error interrupt except self’s DCLS error interrupt being OR-ed.



Figure 39.4 DCLS Error Interrupt (EI Level) and EI Level Interrupt



Figure 39.5 DCLS Error Interrupt (EI Level) and EI Level Interrupt



Figure 39.6 DCLS Error Interrupt (EI Level) and EI Level Interrupt for RH850/E2x-FCC2 and E2UH



Figure 39.7 DCLS Error Interrupt (EI Level) and EI Level Interrupt for RH850/E2H

## Register Specification

### List of Registers

ECM consists of three address areas: ECM master, ECM checker, ECM common.

The following shows the register map of the ECM master and checker registers.

Table . Address List of ECM Master and Checker Registers

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Module Name | Register Name | Symbol | Address | Access | Access Protection |
| ECM Master Registers <ECMM\_base: FFCB 0000H> | | | | | |
| ECMM | ECM master error set trigger register | ECMMESET | <ECMM\_base> + 00H | 8 | ECMKCPROT |
| ECMM | ECM master error clear trigger register | ECMMECLR | <ECMM\_base> + 04H | 8 | ECMKCPROT |
| ECMM | ECM master error source status register n\*1 | ECMMESSTRn\*1 | <ECMM\_base> + 08H to 2CH | 32 | ― |
| ECM Checker Registers <ECMC\_base: FFCB 1000H> | | | | | |
| ECMC | ECM checker error set trigger register | ECMCESET | <ECMC\_base> + 00H | 8 | ECMKCPROT |
| ECMC | ECM checker error clear trigger register | ECMCECLR | <ECMC\_base> + 04H | 8 | ECMKCPROT |
| ECMC | ECM checker error source status register n\*1 | ECMCESSTRn\*1 | <ECMC\_base> + 08H to 2CH | 32 | ― |

1. n = 0 to 9

The following shows the register map of the ECM common registers.

Table . Address List of ECM Common Registers

| Module Name | Register Name | Symbol Name | Address | Access | Access Protection |
| --- | --- | --- | --- | --- | --- |
| ECM Common Registers <ECM\_base: FFCB 2000H> | | | | | |
| ECM | ECM error pulse configuration register | ECMEPCFG | <ECM\_base> + 00H | 8 | ECMKCPROT |
| ECM | ECM maskable interrupt configuration register n\*1 | ECMMICFGn\*1 | <ECM\_base> + 04H~28H | 32 | ECMKCPROT |
| ECM | ECM non-maskable interrupt configuration register n\*1 | ECMNMICFGn\*1 | <ECM\_base> + 2CH~50H | 32 | ECMKCPROT |
| ECM | ECM internal reset configuration register n\*1 | ECMIRCFGn\*1 | <ECM\_base> + 54H~78H | 32 | ECMKCPROT |
| ECM | ECM error mask register n\*1 | ECMEMKn\*1 | <ECM\_base> + 7CH~A0H | 32 | ECMKCPROT |
| ECM | ECM error source status clear trigger register n\*1 | ECMESSTCn\*1 | <ECM\_base> + A4H~C8H | 32 | ECMKCPROT |
| ECM | ECM key code protection register | ECMKCPROT | <ECM\_base> + CCH | 32 | ― |
| ECM | ECM pseudo error trigger register n\*1 | ECMPEn\*1 | <ECM\_base> + D0H to F4H | 32 | ECMKCPROT |
| ECM | ECM delay timer control register | ECMDTMCTL | <ECM\_base> + F8H | 8 | ECMKCPROT |
| ECM | ECM delay timer register | ECMDTMR | <ECM\_base> + FCH | 16 | ECMKCPROT |
| ECM | ECM delay timer compare register | ECMDTMCMP | <ECM\_base> + 100H | 32 | ECMKCPROT |
| ECM | ECM maskable interrupt delay timer configuration register n\*1 | ECMMIDTMCFGn\*1 | <ECM\_base> + 104H to 128H | 32 | ECMKCPROT |
| ECM | ECM non-maskable interrupt delay timer configuration register n\*1 | ECMNMIDTMCFGn\*1 | <ECM\_base> + 12CH to 150H | 32 | ECMKCPROT |
| ECM | ECM error output clear invalidation configuration register | ECMEOCCFG | <ECM\_base> + 154H | 32 | ECMKCPROT |
| ECM | ECM pseudo error mask register | ECMPEM | <ECM\_base> + 158H | 32 | ― |

1. n = 0 to 9

The ECM registers are the register areas common to the redundancy area to be implemented. Writes to the common register areas are conducted simultaneously. The common area for ECM master is read by reading access to the common area. The ECM master register and the ECM checker register represent the address areas which can be written separately.

### ECMmESET ― ECM Master/Checker Error Set Trigger Register (m = M/C)

The ECM master/checker error set trigger register is for setting the error signal from the error pin to the low level. When the ECMmEST bit is set to 1, the error pin immediately outputs the low level. The output cannot be masked. This registers is also the trigger for the port safe state function. When Error signal output is set, each port state will be changed to safe state according to user’s setting. Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register for the details of key code protection. This register is always read as 00H.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 00H |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | — | — | — | — | — | — | — | ECMm EST |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | W |

Table . ECMmESET Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 7 to 1 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 0 | ECMmEST | Error set trigger bit  0: Writing 0 is invalid  1: Set the output level from the error pin to the active (low) level. |

CAUTIONS

Setting or clearing the error output from the error pin via the ECMmESET or ECMmECLR register will set the ECMmSSE308 bit of the ECMmESSTR9 register (ECM compare error). Therefore, the ECMmESET register has to be set following the sequence below.

1. Set the MSKM bit and MSKC bit of the ECMPEM register to “masked”.
2. Set the ECMmEST bit in the ECMmESET register.
3. Wait until and become low by checking that the ECMmSSE311 bit of the ECMmESSTR9 register is "0”.
4. Set the MSKM bit and MSKC bit of the ECMPEM register to “not masked”.

### ECMmECLR ― ECM Master/Checker Error Clear Trigger Register (m = M/C)

The ECM master/checker error clear trigger register is for setting the error signal from the error pin to the high level (toggle). When the ECMmECT bit is set to 1, the error pin outputs the high level (toggle) as long as there are no other sources that set the error pin to the low level. This registers is also the trigger for the port safe state function. When Error signal output is cleared, each port state will be changed to safe state according to user’s setting. Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register for the details of key code protection. This register is always read as 00H.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 00H |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | — | — | — | — | — | — | — | ECMm ECT |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | W |

Table . ECMmECLR Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 7 to 1 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 0 | ECMmECT | Error clear trigger bit  0: Writing 0 is invalid  1: Set the output level from the error pin to the inactive (high) level. |

CAUTIONS

Clearing of the error pin is only possible if all errors, not masked by ECMEMK registers, are cleared beforehand.

Setting or clearing the error output via the ECMmECLR register will generate the error. Therefore, the following has to be set in advance. The sequence below shall be executed by either CPU.

1. Set the MSKM bit and MSKC bit of the ECMPEM register to “masked”.
2. Set the ECMmECT bit in the ECMmECLR registers.
3. Wait until and become high by reading ECMmSSE311 bit of ECMmESSTR9 register 5 times. After that, check that the ECMmSSE311 bit of the ECMmESSTR9 register is "1". If the ECMmSSE311 bit of the ECMmESSTR9 register is not “1", a new error may occur.
4. Set the MSKM bit and MSKC bit of the ECMPEM register to “not masked”.

Note: This procedure is in case of not setting ECMEOCCFG register.

NOTE

If the Error Pin Low Time counter is still running, the Error Output clear function is masked.

The Error Output clear request will not be memorized. Error Output clear function is executed, if the Error Pin Low Time Counter is expired and the Error Output clear register is written.

The configuration flow of port safe state mode must be set after error signal is cleared by the ECMmECLR register. For the configuration flow of port safe state mode setting, see Section 2.6.2.4, Configuration Flow.

### ECMmESSTR0 to ECMmESSTR9 ― ECM Master/Checker Error Source Status Register 0 to 9 (m = M/C)

The ECM master/checker error source status registers 0 to 9 are read-only registers.

This register represents the status of individual internal error sources, which is irrelevant to the setting of the error mask.

ECMmSSEs are provided for the each status of individual internal error sources.

ECMmSSE001-ECMmSSE000 are status bits for counting DCLS error from PE1-PE0. To each DCLS error from each CPU, 2bit expanded status register is prepared for counting the DCLS error. If DCLS error occurs when these bits are “11B”, these bits keep the values.

ECMmSSE001-ECMmSSE000 are status bits for counting DCLS error from PE1-PE0. To each DCLS error from each CPU, 2bit expanded status register is prepared for counting the DCLS error. If DCLS error occurs when these bits are “11B”, these bits keep the values.

ECMmSSE005-ECMmSSE000 are status bits for counting DCLS error from PE5-PE0(except PE2/3)\*1. To each DCLS error from each CPU, 2bit expanded status register is prepared for counting the DCLS error. If DCLS error occurs when these bits are “11B”, these bits keep the values.

Note1:E2H is unimplemented PE4 and PE5.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

ECMmESSTR0

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECMm  SSE  023 | ECMm  SSE  022 | ECMm  SSE  021 | ECMm  SSE  020 | ECMm  SSE  019 | ECMm  SSE  018 | ECMm  SSE  017 | ECMm  SSE  016 | ECMm  SSE  015 | ECMm  SSE  014 | ECMm  SSE  013 | ECMm  SSE  012 | ECMm  SSE  011 | ECMm  SSE  010 | ECMm  SSE  009 | ECMm  SSE  008 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECMm  SSE  007[1:0] | | ECMm  SSE  006[1:0] | | ECMm  SSE  005[1:0] | | ECMm  SSE  004[1:0] | | ECMm  SSE  003[1:0] | | ECMm  SSE  002[1:0] | | ECMm  SSE  001[1:0] | | ECMm  SSE  000[1:0] | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

Table . ECMmESSTR0 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 16 | ECMmSSE023 to  ECMmSSE008 | Error source status bit  ECMmSSE023 to ECMmSSE008 correspond to error sources 23 to 8.  0: Error not occurred  1: Error occurred |
| 15 to 0 | ECMmSSE007[1:0] to  ECMmSSE000[1:0] | Error source status bit  ECMmSSE007 to ECMmSSE000 count error sources 7 to 0 (DCLS error).  00: Error doesn’t happen  01: Error happened once  10: Error happened twice  11: Error happened 3 times or more |

ECMmESSTRn (n = 1 to 8, x = (n–1) × 32)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECMm SSE [x+55] | ECMm SSE [x+54] | ECMm SSE [x+53] | ECMm SSE [x+52] | ECMm SSE [x+51] | ECMm SSE [x+50] | ECMm SSE [x+49] | ECMm SSE [x+48] | ECMm SSE [x+47] | ECMm SSE [x+46] | ECMm SSE [x+45] | ECMm SSE [x+44] | ECMm SSE [x+43] | ECMm SSE [x+42] | ECMm SSE [x+41] | ECMm SSE [x+40] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECMm SSE [x+39] | ECMm SSE [x+38] | ECMm SSE [x+37] | ECMm SSE [x+36] | ECMm SSE [x+35] | ECMm SSE [x+34] | ECMm SSE [x+33] | ECMm SSE [x+32] | ECMm SSE [x+31] | ECMm SSE [x+30] | ECMm SSE [x+29] | ECMm SSE [x+28] | ECMm SSE [x+27] | ECMm SSE [x+26] | ECMm SSE [x+25] | ECMm SSE [x+24] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

Table . ECMmESSTRn Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 0 | ECMmSSE[x+55] to  ECMmSSE[x+24] | Error source status bit  ECMmSSE[x+55] to ECMmSSE[x+24] correspond to error sources [x+55] to [x+24].  0: Error not occurred  1: Error occurred |

ECMmESSTR9

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECMm  SSE  311 | ECMm  SSE  310 | ECMm  SSE  309 | ECMm  SSE  308 | ECMm  SSE  307 | ECMm  SSE  306 | ECMm  SSE  305 | ECMm  SSE  304 | ECMm  SSE  303 | ECMm  SSE  302 | ECMm  SSE  301 | ECMm  SSE  300 | ECMm  SSE  299 | ECMm  SSE  298 | ECMm  SSE  297 | ECMm  SSE  296 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECMm  SSE  295 | ECMm  SSE  294 | ECMm  SSE  293 | ECMm  SSE  292 | ECMm  SSE  291 | ECMm  SSE  290 | ECMm  SSE  289 | ECMm  SSE  288 | ECMm  SSE  287 | ECMm  SSE  286 | ECMm  SSE  285 | ECMm  SSE  284 | ECMm  SSE  283 | ECMm  SSE  282 | ECMm  SSE  281 | ECMm  SSE  280 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

Table . ECMmESSTR9 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 | ECMmSSE311 | The status of the pin  0: is low level  1: is high level  In ECMMESSTR9 register, pin is pin.  In ECMCESSTR9 register, pin is pin. |
| 30 | ECMmSSE310 | The status of the ECMmEST writing  0: No Error  1: Error is set by ECMmEST |
| 29 | ECMmSSE309 | The status of the delay timer overflow  0: No overflow  1: Overflow |
| 28 to 0 | ECMmSSE308 to  ECMmSSE280 | Error source status bit  ECMmSSE308 to ECMmSSE280 count error sources 308 to 280.  0: Error not occurred  1: Error occurred |

NOTE

Reserved bit

The read value of ECMmSSE bit listed as reserved in Table 39.18, Table 39.19 and Table 39.20 and Table 39.21 **Table 39.22**, **Table 39.23** and **Table 39.24** is undefined. Please mask these values of reserve bit when user confirms ECMmESSTRn.

### ECMEPCFG ― ECM Error Pulse Configuration Register

The ECM error pulse configuration register is a read/write register. Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 00H |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | — | — | — | — | — | — | — | ECMSL0 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R/W |

Table . ECMEPCFG Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 7 to 1 | — | Reserved |
| 0 | ECMSL0 | Error pin operation configuration bit  Error output operation setting for the error pin  0: Non-dynamic mode  1: Dynamic mode |

In Dynamic mode the timer output OSTM0 determines the output wave of the error terminal in case of no error.

CAUTION

After setting the dynamic mode, it is recommended not to change to non-dynamic mode again, because there is a possibility of a glitch at the error output.

### ECMMICFG0 to ECMMICFG9 ― ECM Maskable Interrupt Configuration Register 0 to 9

The ECM maskable interrupt configuration registers 0 to 9 are used to set the generation of the INTECMMI interrupts (EI level interrupts) and the INTECMDCLSMI interrupts (EI level interrupts) when DCLS error occurs. The generation of EI level interrupts in response to errors is selectable. Writing to these registers are protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

ECMMICFG0

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECMM  IE023 | ECMM  IE022 | ECMM  IE021 | ECMM  IE020 | ECMM  IE019 | ECMM  IE018 | ECMM  IE017 | ECMM  IE016 | ECMM  IE015 | ECMM  IE014 | ECMM  IE013 | ECMM  IE012 | ECMM  IE011 | ECMM  IE010 | ECMM  IE009 | ECMM  IE008 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECMM  IE007[1:0] | | ECMM  IE006[1:0] | | ECMM  IE005[1:0] | | ECMM  IE004[1:0] | | ECMM  IE003[1:0] | | ECMM  IE002[1:0] | | ECMM  IE001[1:0] | | ECMM  IE000[1:0] | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMMICFG0 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 16 | ECMMIE023 to ECMMIE008 | ECM maskable interrupt generation control bit  ECMMIE023 to ECMMIE008 correspond to error sources 23 to 8.  0: Interrupt generation disabled  1: Interrupt generation enabled |
| 15 to 0 | ECMMIE007[1:0] to ECMMIE000[1:0] | ECM maskable interrupt generation control bit  ECMMIE007 to ECMMIE000 correspond error sources 7 to 0 (DCLS error).  00: Interrupt generation disabled  01: Interrupt generation enabled when error counting once  Interrupt generation enabled when error counting twice  Interrupt generation enabled when error counting 3 times  10\*1: Interrupt generation disabled when error counting once  Interrupt generation enabled when error counting twice  Interrupt generation enabled when error counting 3 times  11\*1: Interrupt generation disabled when error counting once  Interrupt generation disabled when error counting twice  Interrupt generation enabled when error counting 3 times |

1. Interrupt is not generated when error counting over 4 times.

ECMMICFGn (n = 1 to 8, x = (n–1) × 32)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM MIE [x+55] | ECM MIE [x+54] | ECM MIE [x+53] | ECM MIE [x+52] | ECM MIE [x+51] | ECM MIE [x+50] | ECM MIE [x+49] | ECM MIE [x+48] | ECM MIE [x+47] | ECM MIE [x+46] | ECM MIE [x+45] | ECM MIE [x+44] | ECM MIE [x+43] | ECM MIE [x+42] | ECM MIE [x+41] | ECM MIE [x+40] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM MIE [x+39] | ECM MIE [x+38] | ECM MIE [x+37] | ECM MIE [x+36] | ECM MIE [x+35] | ECM MIE [x+34] | ECM MIE [x+33] | ECM MIE [x+32] | ECM MIE [x+31] | ECM MIE [x+30] | ECM MIE [x+29] | ECM MIE [x+28] | ECM MIE [x+27] | ECM MIE [x+26] | ECM MIE [x+25] | ECM MIE [x+24] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMMICFGn Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 0 | ECMMIE[x+55] to ECMMIE[x+24] | ECM maskable interrupt generation control bit  ECMMIE[x+55] to ECMMIE[x+24] correspond to error sources [x+55] to [x+24].  0: Interrupt generation disabled  1: Interrupt generation enabled |

ECMMICFG9

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | — | — | — | ECMM IE308 | ECMM IE307 | — | ECMM IE305 | ECMM IE304 | ECMM IE303 | ECMM IE302 | ECMM IE301 | ECMM IE300 | ECMM IE299 | ECMM IE298 | ECMM IE297 | ECMM IE296 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECMM IE295 | ECMM IE294 | ECMM IE293 | ECMM IE292 | ECMM IE291 | ECMM IE290 | ECMM IE289 | ECMM IE288 | ECMM IE287 | ECMM IE286 | ECMM IE285 | ECMM IE284 | ECMM IE283 | ECMM IE282 | ECMM IE281 | ECMM IE280 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMMICFG9 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 29 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 28 to 27 | ECMMIE308 to ECMMIE307 | ECM maskable interrupt generation control bit  ECMMIE308 to ECMMIE307 correspond to error sources 308 to 307.  0: Interrupt generation disabled  1: Interrupt generation enabled |
| 26 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 25 to 0 | ECMMIE305 to ECMMIE280 | ECM maskable interrupt generation control bit  ECMMIE305 to ECMMIE280 correspond to error sources 305 to 280.  0: Interrupt generation disabled  1: Interrupt generation enabled |

NOTE

Reserved bit

The value of ECMMIE bit listed as reserved for the given error input numbers in Table 39.18, Table 39.19 and Table 39.20 and Table 39.21 **Table 39.22**, **Table 39.23** and **Table 39.24**. When read, the value after reset is returned. When writing, write the value after reset.

### ECMNMICFG0 to ECMNMICFG9 ― ECM Non-maskable Interrupt Configuration Register 0 to 9

The ECM Non-maskable interrupt configuration registers 0 to 9 are used to set the generation of INTECMNMI interrupts (FE level interrupt). Writing to these registers are protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

ECMNMICFG0

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM NMI E023 | ECM NMI E022 | ECM NMI E021 | ECM NMI E020 | ECM NMI E019 | ECM NMI E018 | ECM NMI E017 | ECM NMI E016 | ECM NMI E015 | ECM NMI E014 | ECM NMI E013 | ECM NMI E012 | ECM NMI E011 | ECM NMI E010 | ECM NMI E009 | ECM NMI E008 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM NMI E007[1:0] | | ECM NMI E006[1:0] | | ECM NMI E005[1:0] | | ECM NMI E004[1:0] | | ECM NMI E003[1:0] | | ECM NMI E002[1:0] | | ECM NMI E001[1:0] | | ECM NMI E000[1:0] | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMNMICFG0 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 16 | ECMNMIE023 to ECMNMIE008 | ECM Non-maskable interrupt generation control bit  ECMNMIE023 to ECMNMIE008 correspond to error sources 23 to 8.  0: Interrupt generation disabled  1: Interrupt generation enabled |
| 15 to 0 | ECMNMIE007[1:0] to ECMNMIE000[1:0] | ECM Non-maskable interrupt generation control bit  ECMNMIE007 to ECMNMIE000 correspond error source 7 to 0 (DCLS error).  00: Interrupt generation disabled  01: Interrupt generation enabled when error counting once  Interrupt generation enabled when error counting twice  Interrupt generation enabled when error counting 3 times  10\*1: Interrupt generation disabled when error counting once  Interrupt generation enabled when error counting twice  Interrupt generation enabled when error counting 3 times  11\*1: Interrupt generation disabled when error counting once  Interrupt generation disabled when error counting twice  Interrupt generation enabled when error counting 3 times |

1. Interrupt is not generated when error counting over 4 times.

ECMNMICFGn (n = 1 to 8, x = (n–1) × 32)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM NMIE [x+55] | ECM NMIE [x+54] | ECM NMIE [x+53] | ECM NMIE [x+52] | ECM NMIE [x+51] | ECM NMIE [x+50] | ECM NMIE [x+49] | ECM NMIE [x+48] | ECM NMIE [x+47] | ECM NMIE [x+46] | ECM NMIE [x+45] | ECM NMIE [x+44] | ECM NMIE [x+43] | ECM NMIE [x+42] | ECM NMIE [x+41] | ECM NMIE [x+40] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM NMIE [x+39] | ECM NMIE [x+38] | ECM NMIE [x+37] | ECM NMIE [x+36] | ECM NMIE [x+35] | ECM NMIE [x+34] | ECM NMIE [x+33] | ECM NMIE [x+32] | ECM NMIE [x+31] | ECM NMIE [x+30] | ECM NMIE [x+29] | ECM NMIE [x+28] | ECM NMIE [x+27] | ECM NMIE [x+26] | ECM NMIE [x+25] | ECM NMIE [x+24] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMNMICFGn Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 0 | ECMNMIE[x+55] to ECMNMIE[x+24] | ECM Non-maskable interrupt generation control bit  ECMNMIE[x+55] to ECMNMIE[x+24] correspond to error sources [x+55] to [x+24].  0: Interrupt generation disabled  1: Interrupt generation enabled |

ECMNMICFG9

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | — | — | — | ECM NMI E308 | ECM NMI E307 | — | ECM NMI E305 | ECM NMI E304 | ECM NMI E303 | ECM NMI E302 | ECM NMI E301 | ECM NMI E300 | ECM NMI E299 | ECM NMI E298 | ECM NMI E297 | ECM NMI E296 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM NMI E295 | ECM NMI E294 | ECM NMI E293 | ECM NMI E292 | ECM NMI E291 | ECM NMI E290 | ECM NMI E289 | ECM NMI E288 | ECM NMI E287 | ECM NMI E286 | ECM NMI E285 | ECM NMI E284 | ECM NMI E283 | ECM NMI E282 | ECM NMI E281 | ECM NMI E280 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMNMICFG9 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 29 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 28 to 27 | ECMNMIE308 to ECMNMIE307 | ECM Non-maskable interrupt generation control bit  ECMNMIE308 to ECMNMIE307 correspond to error sources 308 to 307.  0: Interrupt generation disabled  1: Interrupt generation enabled |
| 26 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 25 to 0 | ECMNMIE305 to ECMNMIE280 | ECM Non-maskable interrupt generation control bit  ECMNMIE305 to ECMNMIE280 correspond to error sources 305 to 280.  0: Interrupt generation disabled  1: Interrupt generation enabled |

NOTE

Reserved bit

The value of ECMNMIE bit listed as reserved for the given error input numbers in Table 39.18, Table 39.19 and Table 39.20 and Table 39.21 **Table 39.22**, **Table 39.23** and **Table 39.24**. When read, the value after reset is returned. When writing, write the value after reset.

### ECMIRCFG0 to ECMIRCFG9 ― ECM Internal Reset Configuration Register 0 to 9

The ECM internal reset configuration registers 0 to 9 are used to set the generation of Error Control Module Reset in response to internal errors. Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0001 0000H (ECMIRCFG0), 0000 0000H (ECMIRCFG1 to ECMIRCFG9) |

ECMIRCFG0

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM IRE023 | ECM IRE022 | ECM IRE021 | ECM IRE020 | ECM IRE019 | ECM IRE018 | ECM IRE017 | ECM IRE016 | ECM IRE015 | ECM IRE014 | ECM IRE013 | ECM IRE012 | ECM IRE011 | ECM IRE010 | ECM IRE009 | ECM IRE008 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM IRE007[1:0] | | ECM IRE006[1:0] | | ECM IRE005[1:0] | | ECM IRE004[1:0] | | ECM IRE003[1:0] | | ECM IRE002[1:0] | | ECM IRE001[1:0] | | ECM IRE000[1:0] | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMIRCFG0 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 16 | ECMIRE023 to ECMIRE008 | ECM internal reset generation control bit  ECMIRE023 to ECMIRE008 correspond to error sources 23 to 8.  0: ECM internal reset generation disabled  1: ECM internal reset generation enabled |
| 15 to 0 | ECMIRE007[1:0] to ECMIRE000[1:0] | ECM internal reset generation control bit  ECMIRE007 to ECMIRE000 correspond error sources 7 to 0 (DCLS error).  00: ECM internal reset disabled  01: ECM internal reset enabled when error counting once  ECM internal reset enabled when error counting twice  ECM internal reset enabled when error counting 3 times  10\*1: ECM internal reset disabled when error counting once  ECM internal reset enabled when error counting twice  ECM internal reset enabled when error counting 3 times  11\*1: ECM internal reset disabled when error counting once  ECM internal reset disabled when error counting twice  ECM internal reset enabled when error counting 3 times |

1. ECM internal reset is not generated when error counting over 4 times.

ECMIRCFGn (n = 1 to 8, x = (n–1) × 32)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM IRE [x+55] | ECM IRE [x+54] | ECM IRE [x+53] | ECM IRE [x+52] | ECM IRE [x+51] | ECM IRE [x+50] | ECM IRE [x+49] | ECM IRE [x+48] | ECM IRE [x+47] | ECM IRE [x+46] | ECM IRE [x+45] | ECM IRE [x+44] | ECM IRE [x+43] | ECM IRE [x+42] | ECM IRE [x+41] | ECM IRE [x+40] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM IRE [x+39] | ECM IRE [x+38] | ECM IRE [x+37] | ECM IRE [x+36] | ECM IRE [x+35] | ECM IRE [x+34] | ECM IRE [x+33] | ECM IRE [x+32] | ECM IRE [x+31] | ECM IRE [x+30] | ECM IRE [x+29] | ECM IRE [x+28] | ECM IRE [x+27] | ECM IRE [x+26] | ECM IRE [x+25] | ECM IRE [x+24] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMIRCFGn Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 0 | ECMIRE[x+55] to ECMIRE[x+24] | ECM internal reset generation control bit  ECMIRE[x+55] to ECMIRE[x+24] correspond to error sources [x+55] to [x+24].  0: ECM internal reset generation disabled  1: ECM internal reset generation enabled |

ECMIRCFG9

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | — | — | ECM IRE309 | ECM IRE308 | ECM IRE307 | — | ECM IRE305 | ECM IRE304 | ECM IRE303 | ECM IRE302 | ECM IRE301 | ECM IRE300 | ECM IRE299 | ECM IRE298 | ECM IRE297 | ECM IRE296 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R/W | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM IRE295 | ECM IRE294 | ECM IRE293 | ECM IRE292 | ECM IRE291 | ECM IRE290 | ECM IRE289 | ECM IRE288 | ECM IRE287 | ECM IRE286 | ECM IRE285 | ECM IRE284 | ECM IRE283 | ECM IRE282 | ECM IRE281 | ECM IRE280 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMIRCFG9 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31, 30 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 29 | ECMIRE309 | ECM internal reset generation control bit  ECMIRE309 corresponds to delay timer overflow.  0: ECM internal reset generation disabled  1: ECM internal reset generation enabled |
| 28 to 27 | ECMIRE308 to ECMIRE307 | ECM internal reset generation control bit  ECMIRE308 to ECMIRE307 correspond to error sources 308 to 307.  0: ECM internal reset generation disabled  1: ECM internal reset generation enabled |
| 26 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 25 to 0 | ECMIRE305 to ECMIRE280 | ECM internal reset generation control bit  ECMIRE305 to ECMIRE280 correspond to error sources 305 to 280.  0: ECM internal reset generation disabled  1: ECM internal reset generation enabled |

NOTE

Reserved bit

The value of ECMIRE bit listed as reserved for the given error input numbers in Table 39.18, Table 39.19 and Table 39.20 and Table 39.21 **Table 39.22**, **Table 39.23** and **Table 39.24**. When read, the value after reset is returned. When writing, write the value after reset.

### ECMEMK0 to ECMEMK9 ― ECM Error Mask Register 0 to 9

The ECM error mask registers 0 to 9 are used to mask the individual error sources of the error pin output. This registers is also the trigger for the port safe state function. When Error signal output is not masked, each port state will be changed to safe state according to user’s setting. Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

ECMEMK0

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM EMK 023 | ECM EMK 022 | ECM EMK 021 | ECM EMK 020 | ECM EMK 019 | ECM EMK 018 | ECM EMK 017 | ECM EMK 016 | ECM EMK 015 | ECM EMK 014 | ECM EMK 013 | ECM EMK 012 | ECM EMK 011 | ECM EMK 010 | ECM EMK 009 | ECM EMK 008 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM EMK 007[1:0] | | ECM EMK 006[1:0] | | ECM EMK 005[1:0] | | ECM EMK 004[1:0] | | ECM EMK 003[1:0] | | ECM EMK 002[1:0] | | ECM EMK 001[1:0] | | ECM EMK 000[1:0] | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 39.45 ECMEMK0 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 16 | ECMEMK023 to ECMEMK008 | ECM error output signal mask control bit  ECMEMK023 to ECMEMK008 correspond to error sources 23 to 8.  0: Error signal output is not masked  1: Error signal output is masked |
| 15 to 0 | ECMEMK007[1:0] to ECMEMK000[1:0] | ECM error output signal mask control bit  ECMEMK007 to ECMEMK000 correspond error sources 7 to 0 (DCLS error).  00: Error output signal is not masked.  01: Error output signal is masked when error counting once  Error output signal is not masked when error counting twice  Error output signal is not masked when error counting 3 times  10: Error output signal is masked when error counting once  Error output signal is masked when error counting twice  Error output signal is not masked when error counting 3 times  11: Error output signal is masked |

ECMEMKn (n = 1 to 8, x = (n–1) × 32)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM EMK [x+55] | ECM EMK [x+54] | ECM EMK [x+53] | ECM EMK [x+52] | ECM EMK [x+51] | ECM EMK [x+50] | ECM EMK [x+49] | ECM EMK [x+48] | ECM EMK [x+47] | ECM EMK [x+46] | ECM EMK [x+45] | ECM EMK [x+44] | ECM EMK [x+43] | ECM EMK [x+42] | ECM EMK [x+41] | ECM EMK [x+40] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM EMK [x+39] | ECM EMK [x+38] | ECM EMK [x+37] | ECM EMK [x+36] | ECM EMK [x+35] | ECM EMK [x+34] | ECM EMK [x+33] | ECM EMK [x+32] | ECM EMK [x+31] | ECM EMK [x+30] | ECM EMK [x+29] | ECM EMK [x+28] | ECM EMK [x+27] | ECM EMK [x+26] | ECM EMK [x+25] | ECM EMK [x+24] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 39.46 ECMEMKn Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 0 | ECMEMK[x+55] to ECMEMK[x+24] | ECM error output signal mask control bit  ECMEMK[x+55] to ECMEMK[x+24] correspond to error sources [x+55] to [x+24].  0: Error signal output is not masked  1: Error signal output is masked |

ECMEMK9

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | — | — | ECM EMK 309 | ECM EMK 308 | ECM EMK 307 | — | ECM EMK 305 | ECM EMK 304 | ECM EMK 303 | ECM EMK 302 | ECM EMK 301 | ECM EMK 300 | ECM EMK 299 | ECM EMK 298 | ECM EMK 297 | ECM EMK 296 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R/W | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM EMK 295 | ECM EMK 294 | ECM EMK 293 | ECM EMK 292 | ECM EMK 291 | ECM EMK 290 | ECM EMK 289 | ECM EMK 288 | ECM EMK 287 | ECM EMK 286 | ECM EMK 285 | ECM EMK 284 | ECM EMK 283 | ECM EMK 282 | ECM EMK 281 | ECM EMK 280 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 39.47 ECMEMK9 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31, 30 | — | Reserved  When read, the value after reset is returned. When writing, write the value to “1”. |
| 29 | ECMEMK309 | ECM error output signal mask control bit  ECMEMK309 corresponds to delay timer overflow.  0: Error signal output is not masked  1: Error signal output is masked |
| 28 to 27 | ECMEMK308 to ECMEMK307 | ECM error output signal mask control bit  ECMEMK308 to ECMEMK307 correspond to error sources 308 to 307.  0: Error signal output is not masked  1: Error signal output is masked |
| 26 | — | Reserved  When read, the value after reset is returned. When writing, write the value to "1". |
| 25 to 0 | ECMEMK305 to ECMEMK280 | ECM error output signal mask control bit  ECMEMK305 to ECMEMK280 correspond to error sources 305 to 280.  0: Error signal output is not masked  1: Error signal output is masked |

NOTES

1. Error mask specification  
   If an error flag is set but masked, clearing the mask will set the , and ERROROUTZ to active level. This happens independently from the time of the error occurrence. In other words, the flag is evaluated statically.
2. Reserved bit  
   Please set the value of ECMEMK bit listed as reserved in Table 39.18, Table 39.19 and Table 39.20 and Table 39.21 **Table 39.22**, **Table 39.23** and **Table 39.24** to “1”.

### ECMEMK0 to ECMEMK9 ― ECM Error Mask Register 0 to 9

The ECM error mask registers 0 to 9 are used to mask the individual error sources of the error pin output. This registers is also the trigger for the port safe state function. When Error signal output is not masked, each port state will be changed to safe state according to user’s setting. Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

ECMEMK0

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM EMK 023 | ECM EMK 022 | ECM EMK 021 | ECM EMK 020 | ECM EMK 019 | ECM EMK 018 | ECM EMK 017 | ECM EMK 016 | ECM EMK 015 | ECM EMK 014 | ECM EMK 013 | ECM EMK 012 | ECM EMK 011 | ECM EMK 010 | ECM EMK 009 | ECM EMK 008 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM EMK 007[1:0] | | ECM EMK 006[1:0] | | ECM EMK 005[1:0] | | ECM EMK 004[1:0] | | ECM EMK 003[1:0] | | ECM EMK 002[1:0] | | ECM EMK 001[1:0] | | ECM EMK 000[1:0] | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 39.48 ECMEMK0 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 16 | ECMEMK023 to ECMEMK008 | ECM error output signal mask control bit  ECMEMK023 to ECMEMK008 correspond to error sources 23 to 8.  0: Error signal output is not masked  1: Error signal output is masked |
| 15 to 0 | ECMEMK007[1:0] to ECMEMK000[1:0] | ECM error output signal mask control bit  ECMEMK007 to ECMEMK000 correspond error sources 7 to 0 (DCLS error).  00: Error output signal is not masked.  01: Error output signal is masked when error counting once  Error output signal is not masked when error counting twice  Error output signal is not masked when error counting 3 times  10: Error output signal is masked when error counting once  Error output signal is masked when error counting twice  Error output signal is not masked when error counting 3 times  11: Error output signal is masked |

ECMEMKn (n = 1 to 8, x = (n–1) × 32)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM EMK [x+55] | ECM EMK [x+54] | ECM EMK [x+53] | ECM EMK [x+52] | ECM EMK [x+51] | ECM EMK [x+50] | ECM EMK [x+49] | ECM EMK [x+48] | ECM EMK [x+47] | ECM EMK [x+46] | ECM EMK [x+45] | ECM EMK [x+44] | ECM EMK [x+43] | ECM EMK [x+42] | ECM EMK [x+41] | ECM EMK [x+40] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM EMK [x+39] | ECM EMK [x+38] | ECM EMK [x+37] | ECM EMK [x+36] | ECM EMK [x+35] | ECM EMK [x+34] | ECM EMK [x+33] | ECM EMK [x+32] | ECM EMK [x+31] | ECM EMK [x+30] | ECM EMK [x+29] | ECM EMK [x+28] | ECM EMK [x+27] | ECM EMK [x+26] | ECM EMK [x+25] | ECM EMK [x+24] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 39.49 ECMEMKn Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 0 | ECMEMK[x+55] to ECMEMK[x+24] | ECM error output signal mask control bit  ECMEMK[x+55] to ECMEMK[x+24] correspond to error sources [x+55] to [x+24].  0: Error signal output is not masked  1: Error signal output is masked |

ECMEMK9

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | — | — | ECM EMK 309 | ECM EMK 308 | ECM EMK 307 | — | ECM EMK 305 | ECM EMK 304 | ECM EMK 303 | ECM EMK 302 | ECM EMK 301 | ECM EMK 300 | ECM EMK 299 | ECM EMK 298 | ECM EMK 297 | ECM EMK 296 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R/W | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM EMK 295 | ECM EMK 294 | ECM EMK 293 | ECM EMK 292 | ECM EMK 291 | ECM EMK 290 | ECM EMK 289 | ECM EMK 288 | ECM EMK 287 | ECM EMK 286 | ECM EMK 285 | ECM EMK 284 | ECM EMK 283 | ECM EMK 282 | ECM EMK 281 | ECM EMK 280 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 39.50 ECMEMK9 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31, 30 | — | Reserved  When read, the value after reset is returned. When writing, write the value to “1”. |
| 29 | ECMEMK309 | ECM error output signal mask control bit  ECMEMK309 corresponds to delay timer overflow.  0: Error signal output is not masked  1: Error signal output is masked |
| 28 to 27 | ECMEMK308 to ECMEMK307 | ECM error output signal mask control bit  ECMEMK308 to ECMEMK307 correspond to error sources 308 to 307.  0: Error signal output is not masked  1: Error signal output is masked |
| 26 | — | Reserved  When read, the value after reset is returned. When writing, write the value to "1". |
| 25 to 0 | ECMEMK305 to ECMEMK280 | ECM error output signal mask control bit  ECMEMK305 to ECMEMK280 correspond to error sources 305 to 280.  0: Error signal output is not masked  1: Error signal output is masked |

NOTES

1. Error mask specification  
   If an error flag is set but masked, clearing the mask will set the , and ERROROUTZ to active level. This happens independently from the time of the error occurrence. In other words, the flag is evaluated statically.
2. Reserved bit  
   Please set the value of ECMEMK bit listed as reserved in Table 39.20 to “1”.

### ECMEMK0 to ECMEMK9 ― ECM Error Mask Register 0 to 9

The ECM error mask registers 0 to 9 are used to mask the individual error sources of the error pin output. This registers is also the trigger for the port safe state function. When Error signal output is not masked, each port state will be changed to safe state according to user’s setting. Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

ECMEMK0

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM EMK 023 | ECM EMK 022 | ECM EMK 021 | ECM EMK 020 | ECM EMK 019 | ECM EMK 018 | ECM EMK 017 | ECM EMK 016 | ECM EMK 015 | ECM EMK 014 | ECM EMK 013 | ECM EMK 012 | ECM EMK 011 | ECM EMK 010 | ECM EMK 009 | ECM EMK 008 |
| Value after reset | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM EMK 007[1:0] | | ECM EMK 006[1:0] | | ECM EMK 005[1:0] | | ECM EMK 004[1:0] | | ECM EMK 003[1:0] | | ECM EMK 002[1:0] | | ECM EMK 001[1:0] | | ECM EMK 000[1:0] | |
| Value after reset | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Note1: The initial value of ECMEMK bit listed as reserved in**Table 39.23** and **Table 39.24** to “1”.

The initial value of ECMEMK bit which exist error factor is “0”.

Table 39.51 ECMEMK0 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 16 | ECMEMK023 to ECMEMK008 | ECM error output signal mask control bit  ECMEMK023 to ECMEMK008 correspond to error sources 23 to 8.  0: Error signal output is not masked  1: Error signal output is masked |
| 15 to 0 | ECMEMK007[1:0] to ECMEMK000[1:0] | ECM error output signal mask control bit  ECMEMK007 to ECMEMK000 correspond error sources 7 to 0 (DCLS error).  00: Error output signal is not masked.  01: Error output signal is masked when error counting once  Error output signal is not masked when error counting twice  Error output signal is not masked when error counting 3 times  10: Error output signal is masked when error counting once  Error output signal is masked when error counting twice  Error output signal is not masked when error counting 3 times  11: Error output signal is masked |

ECMEMKn (n = 1 to 8, x = (n–1) × 32)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM EMK [x+55] | ECM EMK [x+54] | ECM EMK [x+53] | ECM EMK [x+52] | ECM EMK [x+51] | ECM EMK [x+50] | ECM EMK [x+49] | ECM EMK [x+48] | ECM EMK [x+47] | ECM EMK [x+46] | ECM EMK [x+45] | ECM EMK [x+44] | ECM EMK [x+43] | ECM EMK [x+42] | ECM EMK [x+41] | ECM EMK [x+40] |
| Value after reset | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM EMK [x+39] | ECM EMK [x+38] | ECM EMK [x+37] | ECM EMK [x+36] | ECM EMK [x+35] | ECM EMK [x+34] | ECM EMK [x+33] | ECM EMK [x+32] | ECM EMK [x+31] | ECM EMK [x+30] | ECM EMK [x+29] | ECM EMK [x+28] | ECM EMK [x+27] | ECM EMK [x+26] | ECM EMK [x+25] | ECM EMK [x+24] |
| Value after reset | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Note1: The initial value of ECMEMK bit listed as reserved in**Table 39.23** and **Table 39.24** to “1”.

The initial value of ECMEMK bit which exist error factor is “0”.

Table 39.52 ECMEMKn Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 0 | ECMEMK[x+55] to ECMEMK[x+24] | ECM error output signal mask control bit  ECMEMK[x+55] to ECMEMK[x+24] correspond to error sources [x+55] to [x+24].  0: Error signal output is not masked  1: Error signal output is masked |

ECMEMK9

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | — | — | ECM EMK 309 | ECM EMK 308 | ECM EMK 307 | — | ECM EMK 305 | ECM EMK 304 | ECM EMK 303 | ECM EMK 302 | ECM EMK 301 | ECM EMK 300 | ECM EMK 299 | ECM EMK 298 | ECM EMK 297 | ECM EMK 296 |
| Value after reset | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 |
| R/W | R | R | R/W | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM EMK 295 | ECM EMK 294 | ECM EMK 293 | ECM EMK 292 | ECM EMK 291 | ECM EMK 290 | ECM EMK 289 | ECM EMK 288 | ECM EMK 287 | ECM EMK 286 | ECM EMK 285 | ECM EMK 284 | ECM EMK 283 | ECM EMK 282 | ECM EMK 281 | ECM EMK 280 |
| Value after reset | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 | \*1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Note1: The initial value of ECMEMK bit listed as reserved in**Table 39.23** and **Table 39.24** to “1”.

The initial value of ECMEMK bit which exist error factor is “0”.

Table 39.53 ECMEMK9 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31, 30 | — | Reserved  When read, the value after reset is returned. When writing, write the value to “1”. |
| 29 | ECMEMK309 | ECM error output signal mask control bit  ECMEMK309 corresponds to delay timer overflow.  0: Error signal output is not masked  1: Error signal output is masked |
| 28 to 27 | ECMEMK308 to ECMEMK307 | ECM error output signal mask control bit  ECMEMK308 to ECMEMK307 correspond to error sources 308 to 307.  0: Error signal output is not masked  1: Error signal output is masked |
| 26 | — | Reserved  When read, the value after reset is returned. When writing, write the value to "1". |
| 25 to 0 | ECMEMK305 to ECMEMK280 | ECM error output signal mask control bit  ECMEMK305 to ECMEMK280 correspond to error sources 305 to 280.  0: Error signal output is not masked  1: Error signal output is masked |

NOTES

1. Error mask specification  
   If an error flag is set but masked, clearing the mask will set the , and ERROROUTZ to active level. This happens independently from the time of the error occurrence. In other words, the flag is evaluated statically.
2. PE3 and PE4 is unimplemented in RH850/E2x-FCC2 for E2H and E2H.But the initial value of ECMEMK bit related PE3 and PE4 function is “0”.

### ECMESSTC0 to ECMESSTC9 ― ECM Error Source Status Clear Trigger Register 0 to 9

The ECM error source status clear trigger registers 0 to 9 are a write-only register and can be written in 32-bit units. These registers are used to clear the individual error source status of the ECM master/checker error source status registers 0 to 9. Both the error status of the ECM master and the ECM checker are cleared simultaneously.

Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

ECMESSTC0

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM CLSSE 023 | ECM CLSSE 022 | ECM CLSSE 021 | ECM CLSSE 020 | ECM CLSSE 019 | ECM CLSSE 018 | ECM CLSSE 017 | ECM CLSSE 016 | ECM CLSSE 015 | ECM CLSSE 014 | ECM CLSSE 013 | ECM CLSSE 012 | ECM CLSSE 011 | ECM CLSSE 010 | ECM CLSSE 009 | ECM CLSSE 008 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM CLSSE 007[1:0] | | ECM CLSSE 006[1:0] | | ECM CLSSE 005[1:0] | | ECM CLSSE 004[1:0] | | ECM CLSSE 003[1:0] | | ECM CLSSE 002[1:0] | | ECM CLSSE 001[1:0] | | ECM CLSSE 000[1:0] | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |

Table . ECMESSTC0 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 16 | ECMCLSSE023 to ECMCLSSE008 | ECM error status clear bit  ECMCLSSE023 to ECMCLSSE008 correspond to ECMmSSE023 to ECMmSSE008.  0: Corresponding error status unchanged  1: Corresponding error status cleared |
| 15 to 0 | ECMCLSSE007[1:0] to ECMCLSSE000[1:0] | ECM error status clear bit  ECMCLSSE007 to ECMCLSSE000 correspond to ECMmSSE007 to ECMmSSE000.  00: Corresponding error status unchanged  01: (Same with 11B setting) Error status cleared  10: (Same with 11B setting) Error status cleared  11: Corresponding error status cleared |

ECMESSTCn (n = 1 to 8, x = (n–1) × 32)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM CLSSE [x+55] | ECM CLSSE [x+54] | ECM CLSSE [x+53] | ECM CLSSE [x+52] | ECM CLSSE [x+51] | ECM CLSSE [x+50] | ECM CLSSE [x+49] | ECM CLSSE [x+48] | ECM CLSSE [x+47] | ECM CLSSE [x+46] | ECM CLSSE [x+45] | ECM CLSSE [x+44] | ECM CLSSE [x+43] | ECM CLSSE [x+42] | ECM CLSSE [x+41] | ECM CLSSE [x+40] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM CLSSE [x+39] | ECM CLSSE [x+38] | ECM CLSSE [x+37] | ECM CLSSE [x+36] | ECM CLSSE [x+35] | ECM CLSSE [x+34] | ECM CLSSE [x+33] | ECM CLSSE [x+32] | ECM CLSSE [x+31] | ECM CLSSE [x+30] | ECM CLSSE [x+29] | ECM CLSSE [x+28] | ECM CLSSE [x+27] | ECM CLSSE [x+26] | ECM CLSSE [x+25] | ECM CLSSE [x+24] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |

Table . ECMESSTCn Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 0 | ECMCLSSE[x+55] to ECMCLSSE[x+24] | ECM error status clear bit  ECMCLSSE[x+55] to ECMCLSSE[x+24] correspond to ECMmSSE[x+55] to ECMmSSE[x+24].  0: Corresponding error status unchanged  1: Corresponding error status cleared |

ECMESSTC9

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | — | ECM CLSSE 310 | ECM CLSSE 309 | ECM CLSSE 308 | ECM CLSSE 307 | ECM CLSSE 306 | ECM CLSSE 305 | ECM CLSSE 304 | ECM CLSSE 303 | ECM CLSSE 302 | ECM CLSSE 301 | ECM CLSSE 300 | ECM CLSSE 299 | ECM CLSSE 298 | ECM CLSSE 297 | ECM CLSSE 296 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM CLSSE 295 | ECM CLSSE 294 | ECM CLSSE 293 | ECM CLSSE 292 | ECM CLSSE 291 | ECM CLSSE 290 | ECM CLSSE 289 | ECM CLSSE 288 | ECM CLSSE 287 | ECM CLSSE 286 | ECM CLSSE 285 | ECM CLSSE 284 | ECM CLSSE 283 | ECM CLSSE 282 | ECM CLSSE 281 | ECM CLSSE 280 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |

Table . ECMESSTC9 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 | — | Reserved  When writing, write the value after reset. |
| 30 | ECMCLSSE310 | ECM error status clear bit  ECMCLSSE310 corresponds to ECMmSSE310.  0: Corresponding error status unchanged  1: Corresponding error status cleared |
| 29 | ECMCLSSE309 | ECM error status clear bit  ECMCLSSE309 corresponds to ECMmSSE309.  0: Corresponding error status unchanged  1: Corresponding error status cleared |
| 28 to 0 | ECMCLSSE308 to ECMCLSSE280 | ECM error status clear bit  ECMCLSSE308 to ECMCLSSE280 correspond to ECMmSSE308 to ECMmSSE280.  0: Corresponding error status unchanged  1: Corresponding error status cleared |

NOTE

Reserved bit

The value of ECMCLSSE bit listed as reserved for the given error input numbers in Table 39.18, Table 39.19 and Table 39.20 and Table 39.21 **Table 39.22**, **Table 39.23** and **Table 39.24**. When writing, write the value after reset.

### ECMKCPROT ― ECM Key Code Protection Register

The ECM key code protection register is used for protection against writing operation to the configuration registers.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | KCPROT[31:16] | | | | | | | | | | | | | | | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | KCPROT[15:1] | | | | | | | | | | | | | | | KCE |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | R/W |

Table . ECMKCPROT Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 1 | KCPROT[31:1] | Enable or disable modification of the KCE bit.  The value written is not retained. These bits are always read as 0. \*1 |
| 0 | KCE | Key Code Enable bit  0: Disables write access of protected registers  1: Enables write access of protected registers |

1. Set A5A5A500H with {KCPROT[31:1],KCE} to disable to write key code protection register.  
   Set A5A5A501H with {KCPROT[31:1],KCE} to enable to write key code protection register.

### ECMPE0 to ECMPE9 ― ECM Pseudo Error Trigger Register 0 to 9

The ECM pseudo error trigger registers 0 to 9 are write-only registers. These registers are used to generate a pseudo error for test purposes. The ECM operation in response to the generation of a pseudo error is identical to that in response to a real error source. Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

ECMPE0

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM PE023 | ECM PE022 | ECM PE021 | ECM PE020 | ECM PE019 | ECM PE018 | ECM PE017 | ECM PE016 | ECM PE015 | ECM PE014 | ECM PE013 | ECM PE012 | ECM PE011 | ECM PE010 | ECM PE009 | ECM PE008 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM PE007[1:0] | | ECM PE006[1:0] | | ECM PE005[1:0] | | ECM PE004[1:0] | | ECM PE003[1:0] | | ECM PE002[1:0] | | ECM PE001[1:0] | | ECM PE000[1:0] | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |

Table . ECMPE0 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 16 | ECMPE023 to ECMPE008 | ECM pseudo error trigger bit  ECMPE023 to ECMPE008 correspond to error sources 23 to 8.  0: Pseudo error is not generated.  1: Pseudo error is generated. |
| 15 to 0 | ECMPE007[1:0] to ECMPE000[1:0] | ECM pseudo error trigger bit  ECMPE007 to ECMPE000 correspond to error sources 7 to 0 (DCLS error).  00: Pseudo error is not generated  01: Pseudo error is generated as same as error counting once  10: Pseudo error is generated as same as error counting once  11: Pseudo error is generated as same as error counting once |

ECMPEn (n = 1 to 8, (n–1) × 32)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM PE [x+55] | ECM PE [x+54] | ECM PE [x+53] | ECM PE [x+52] | ECM PE [x+51] | ECM PE [x+50] | ECM PE [x+49] | ECM PE [x+48] | ECM PE [x+47] | ECM PE [x+46] | ECM PE [x+45] | ECM PE [x+44] | ECM PE [x+43] | ECM PE [x+42] | ECM PE [x+41] | ECM PE [x+40] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM PE [x+39] | ECM PE [x+38] | ECM PE [x+37] | ECM PE [x+36] | ECM PE [x+35] | ECM PE [x+34] | ECM PE [x+33] | ECM PE [x+32] | ECM PE [x+31] | ECM PE [x+30] | ECM PE [x+29] | ECM PE [x+28] | ECM PE [x+27] | ECM PE [x+26] | ECM PE [x+25] | ECM PE [x+24] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |

Table . ECMPEn Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 0 | ECMPE[x+55] to ECMPE[x+24] | ECM pseudo error trigger bit  ECMPE[x+55] to ECMPE[x+24] correspond to error sources [x+55] to [x+24].  0: Pseudo error is not generated.  1: Pseudo error is generated. |

ECMPE9

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | — | — | ECM PE309 | ECM PE308 | — | — | ECM PE305 | ECM PE304 | ECM PE303 | ECM PE302 | ECM PE301 | ECM PE300 | ECM PE299 | ECM PE298 | ECM PE297 | ECM PE296 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | W | W | R | R | W | W | W | W | W | W | W | W | W | W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM PE295 | ECM PE294 | ECM PE293 | ECM PE292 | ECM PE291 | ECM PE290 | ECM PE289 | ECM PE288 | ECM PE287 | ECM PE286 | ECM PE285 | ECM PE284 | ECM PE283 | ECM PE282 | ECM PE281 | ECM PE280 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |

Table . ECMPE9 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31, 30 | — | Reserved  When writing, write the value after reset. |
| 29 | ECMPE309 | ECM pseudo error trigger bit  ECMPE309 corresponds to delay timer overflow.  0: Pseudo error is not generated.  1: Pseudo error is generated. |
| 28 | ECMPE308 | ECM pseudo error trigger bit  ECMPE308 corresponds to error source 308.  0: Pseudo error is not generated.  1: Pseudo error is generated. |
| 27, 26 | — | Reserved  When writing, write the value after reset. |
| 25 to 0 | ECMPE305 to ECMPE280 | ECM pseudo error trigger bit  ECMPE305 to ECMPE280 correspond to error sources 305 to 280.  0: Pseudo error is not generated.  1: Pseudo error is generated. |

NOTE

Reserved bit

The value of ECMPE bit listed as reserved for the given error input numbers in Table 39.18, Table 39.19 and Table 39.20 and Table 39.21 **Table 39.22**, **Table 39.23** and **Table 39.24**. When writing, write the value after reset.

### ECMDTMCTL ― ECM Delay Timer Control Register

The ECM delay timer control register is a read/write register. This register is used to control the delay timer. Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 00H |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | — | — | — | DTMSTACNTCLK | — | — | DTMSTP | DTMSTA |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | W | R/W |

Table . ECMDTMCTL Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 7 to 5 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 4 | DTMSTACNTCLK | Delay timer start confirmation status.  0: Delay timer does not start  1: Delay timer starts. |
| 3, 2 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 1 | DTMSTP | Delay timer stop bit  By writing “1” to this bit, delay timer is stopped (0 write is ignored). Simultaneously, DTMSTA bit will be 0.  0: Delay timer is completed or not executed.  1: Stop request for delay timer is on execution. |
| 0 | DTMSTA | Delay timer start bit  Specifies the operation of the delay timer when any error event is occurred.  0: Delay timer does not start  1: Delay timer starts |

NOTES

1. ECMDTMCTL register can be accessed via P-Bus but delay timer runs with not P-Bus clock but dedicated counter clock.  
   Therefore, time rag exists between writing of ECMDTMCTL and running of delay timer.  
   DTMSTACNTCLK can be used to confirm whether delay timer is enabled or not. Please confirm again whether DTMSTA is updated or not after your write action.
2. ECMDTMCTL register can be written only when (DTMSTA, DTMSTACNTCLK) = (0, 0) or (1, 1).  
   Please confirm the combination of DTMSTA and DTMSTACNTCLK before your write action.
3. The delay timer needs 3 clocks of cntclk until it stops an overflow certainly.  
   Please consider to set the sufficient value to ECMDTMCMP[15:0].

### ECMDTMR ― ECM Delay Timer Register

The ECM delay timer register is a read-only register. The ECM delay timer register is initialized by setting the ECMSTA bit of the ECM delay timer control register from 1 (timer in operation) to 0 (timer stops).

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000H |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECMDTMR[15:0] | | | | | | | | | | | | | | | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

Table . ECMDTMR Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 15 to 0 | ECMDTMR[15:0] | Delay timer counter value. |

### ECMDTMCMP ― ECM Delay Timer Compare Register

The ECM delay timer compare register is a read/write register. The ECMmESSTR9.ECMmSSE309 bit is set when this register matches with the value of the ECM delay timer register. Writing data to this register has to be conducted while the delay timer is stopped. Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CMPW |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECMDTMCMP[15:0] | | | | | | | | | | | | | | | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMDTMCMP Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 17 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 16 | CMPW | Indicates on execution of ECMDTMCMP register setting to counter clock  domain  0: Not executed  1: On execution of setting ECMDTMCMP |
| 15 to 0 | ECMDTMCMP[15:0] | Delay timer compare value |

NOTES

1. ECMDTMCMP can be accessible via P-Bus. But delay timer is run with not P-Bus clock but dedicated counter clock. When ECMDTMCMP is configured, this value is moved to dedicate counter clock domain to be able to be used by delay timer. CMPW indicates the current status of ECMDTMCMP setting on dedicated counter clock domain.
2. While CMPW is “1”, writing of ECMDTMCMP is ignored. Please confirm CMPW = 0 before writing of ECMDTMCMP.

### ECMMIDTMCFG0 to ECMMIDTMCFG9― ECM Maskable Interrupt Delay Timer Configuration Register 0 to 9

The ECM maskable interrupt delay timer configuration registers 0 to 9 are used to set enable/disable of the delay timer start caused by EI level interrupts in response to errors. Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

ECMMIDTMCFG0

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM MITE 023 | ECM MITE 022 | ECM MITE 021 | ECM MITE 020 | ECM MITE 019 | ECM MITE 018 | ECM MITE 017 | ECM MITE 016 | ECM MITE 015 | ECM MITE 014 | ECM MITE 013 | ECM MITE 012 | ECM MITE 011 | ECM MITE 010 | ECM MITE 009 | ECM MITE 008 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM MITE 007[1:0] | | ECM MITE 006[1:0] | | ECM MITE 005[1:0] | | ECM MITE 004[1:0] | | ECM MITE 003[1:0] | | ECM MITE 002[1:0] | | ECM MITE 001[1:0] | | ECM MITE 000[1:0] | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMMIDTMCFG0 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 16 | ECMMITE023 to ECMMITE008 | ECM delay timer start control bit  ECMMITE023 to ECMMITE008 correspond to maskable interrupts generated by error sources 23 to 8.  0: Delay timer start disabled  1: Delay timer start enabled |
| 15 to 0 | ECMMITE007[1:0] to ECMMITE000[1:0]\*1 | ECM delay timer start control bit  ECMMITE007 to ECMMITE000 correspond to error sources 7 to 0 (DCLS error).  00: Delay timer start disabled  01: Delay timer start enabled  10\*2: Delay timer start disabled when error counting once  Delay timer start enabled when error counting twice  Delay timer start enabled when error counting 3 times  11\*2: Delay timer start disabled when error counting once  Delay timer start disabled when error counting twice  Delay timer start enabled when error counting 3 times |

1. It is necessary that ECMMITE007[1:0] to ECMMITE000[1:0] bit corresponding to ECMMIE007[1:0] to ECMMIE000[1:0] bit is set to a value same as ECMMIE007[1:0] to ECMMIE000[1:0] when ECM delay timer is enabled.
2. Delay timer is not started when error counting over 4 times.

ECMMIDTMCFGn (n = 1 to 8, x = (n–1) × 32)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM MITE [x+55] | ECM MITE [x+54] | ECM MITE [x+53] | ECM MITE [x+52] | ECM MITE [x+51] | ECM MITE [x+50] | ECM MITE [x+49] | ECM MITE [x+48] | ECM MITE [x+47] | ECM MITE [x+46] | ECM MITE [x+45] | ECM MITE [x+44] | ECM MITE [x+43] | ECM MITE [x+42] | ECM MITE [x+41] | ECM MITE [x+40] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM MITE [x+39] | ECM MITE [x+38] | ECM MITE [x+37] | ECM MITE [x+36] | ECM MITE [x+35] | ECM MITE [x+34] | ECM MITE [x+33] | ECM MITE [x+32] | ECM MITE [x+31] | ECM MITE [x+30] | ECM MITE [x+29] | ECM MITE [x+28] | ECM MITE [x+27] | ECM MITE [x+26] | ECM MITE [x+25] | ECM MITE [x+24] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMMIDTMCFGn Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 0 | ECMMITE[x+55] to ECMMITE[x+24] | ECM delay timer start control bit  ECMMITE[x+55] to ECMMITE[x+24] correspond to maskable interrupts generated by error sources [x+55] to [x+24].  0: Delay timer start disabled  1: Delay timer start enabled |

ECMMIDTMCFG9

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | — | — | — | ECM MITE 308 | ECM MITE 307 | — | ECM MITE 305 | ECM MITE 304 | ECM MITE 303 | ECM MITE 302 | ECM MITE 301 | ECM MITE 300 | ECM MITE 299 | ECM MITE 298 | ECM MITE 297 | ECM MITE 296 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM MITE 295 | ECM MITE 294 | ECM MITE 293 | ECM MITE 292 | ECM MITE 291 | ECM MITE 290 | ECM MITE 289 | ECM MITE 288 | ECM MITE 287 | ECM MITE 286 | ECM MITE 285 | ECM MITE 284 | ECM MITE 283 | ECM MITE 282 | ECM MITE 281 | ECM MITE 280 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMMIDTMCFG9 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 29 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 28 to 27 | ECMMITE308 to ECMMITE307 | ECM delay timer start control bit  ECMMITE308 to ECMMITE307 correspond to maskable interrupts generated by error sources 308 to 307.  0: Delay timer start disabled  1: Delay timer start enabled |
| 26 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 25 to 0 | ECMMITE305 to ECMMITE280 | ECM delay timer start control bit  ECMMITE305 to ECMMITE280 correspond to maskable interrupts generated by error sources 305 to 280.  0: Delay timer start disabled  1: Delay timer start enabled |

NOTE

Reserved bit

The value of ECMMITE bit listed as reserved for the given error input numbers in Table 39.18, Table 39.19 and Table 39.20 and Table 39.21 **Table 39.22**, **Table 39.23** and **Table 39.24**. When read, the value after reset is returned. When writing, write the value after reset.

### ECMNMIDTMCFG0 to ECMNMIDTMCFG9 ― ECM Non-maskable Interrupt Delay Timer Configuration Register 0 to 9

The ECM non-maskable interrupt delay timer registers 0 to 9 are used to set enable/disable of the delay timer start caused by FE level interrupts in response to errors. Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

ECMNMIDTMCFG0

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM NMITE 023 | ECM NMITE 022 | ECM NMITE 021 | ECM NMITE 020 | ECM NMITE 019 | ECM NMITE 018 | ECM NMITE 017 | ECM NMITE 016 | ECM NMITE 015 | ECM NMITE 014 | ECM NMITE 013 | ECM NMITE 012 | ECM NMITE 011 | ECM NMITE 010 | ECM NMITE 009 | ECM NMITE 008 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM NMITE 007[1:0] | | ECM NMITE 006[1:0] | | ECM NMITE 005[1:0] | | ECM NMITE 004[1:0] | | ECM NMITE 003[1:0] | | ECM NMITE 002[1:0] | | ECM NMITE 001[1:0] | | ECM NMITE 000[1:0] | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMNMIDTMCFG0 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 16 | ECMNMITE023 to ECMNMITE008 | ECM delay timer start control bit  ECMNMITE023 to ECMNMITE008 correspond to non-maskable interrupts generated by error sources 23 to 8.  0: Delay timer start disabled  1: Delay timer start enabled |
| 15 to 0 | ECMNMITE007[1:0] to ECMNMITE000[1:0] \*1 | ECM delay timer start control bit  ECMNMITE007 to ECMNMITE000 correspond to error sources 7 to 0 (DCLS error).  00: Delay timer start disabled  01: Delay timer start enabled  10\*2: Delay timer start disabled when error counting once  Delay timer start enabled when error counting twice  Delay timer start enabled when error counting 3 times  11\*2: Delay timer start disabled when error counting once  Delay timer start disabled when error counting twice  Delay timer start enabled when error counting 3 times |

1. It is necessary that ECMNMITE007[1:0] to ECMNMITE000[1:0] bit corresponding to ECMNMIE007[1:0] to ECMNMIE000[1:0] bit is set to a value same as ECMNMIE007[1:0] to ECMNMIE000[1:0] when ECM delay timer is enabled.
2. Delay timer is not started when error counting over 4 times.

ECMNMIDTMCFGn (n = 1 to 8, x = (n–1) × 32)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | ECM NMITE [x+55] | ECM NMITE [x+54] | ECM NMITE [x+53] | ECM NMITE [x+52] | ECM NMITE [x+51] | ECM NMITE [x+50] | ECM NMITE [x+49] | ECM NMITE [x+48] | ECM NMITE [x+47] | ECM NMITE [x+46] | ECM NMITE [x+45] | ECM NMITE [x+44] | ECM NMITE [x+43] | ECM NMITE [x+42] | ECM NMITE [x+41] | ECM NMITE [x+40] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM NMITE [x+39] | ECM NMITE [x+38] | ECM NMITE [x+37] | ECM NMITE [x+36] | ECM NMITE [x+35] | ECM NMITE [x+34] | ECM NMITE [x+33] | ECM NMITE [x+32] | ECM NMITE [x+31] | ECM NMITE [x+30] | ECM NMITE [x+29] | ECM NMITE [x+28] | ECM NMITE [x+27] | ECM NMITE [x+26] | ECM NMITE [x+25] | ECM NMITE [x+24] |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMNMIDTMCFGn Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 0 | ECMNMITE[x+55] to ECMNMITE[x+24] | ECM delay timer start control bit  ECMNMITE[x+55] to ECMNMITE[x+24] correspond to non-maskable interrupts generated by error sources [x+55] to [x+24].  0: Delay timer start disabled  1: Delay timer start enabled |

ECMNMIDTMCFG9

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | — | — | — | ECM NMITE 308 | ECM NMITE 307 | — | ECM NMITE 305 | ECM NMITE 304 | ECM NMITE 303 | ECM NMITE 302 | ECM NMITE 301 | ECM NMITE 300 | ECM NMITE 299 | ECM NMITE 298 | ECM NMITE 297 | ECM NMITE 296 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECM NMITE 295 | ECM NMITE 294 | ECM NMITE 293 | ECM NMITE 292 | ECM NMITE 291 | ECM NMITE 290 | ECM NMITE 289 | ECM NMITE 288 | ECM NMITE 287 | ECM NMITE 286 | ECM NMITE 285 | ECM NMITE 284 | ECM NMITE 283 | ECM NMITE 282 | ECM NMITE 281 | ECM NMITE 280 |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMNMIDTMCFG9 Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 29 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 28 to 27 | ECMNMITE308 to ECMNMITE307 | ECM delay timer start control bit  ECMNMITE308 to ECMNMITE307 correspond to non-maskable interrupts generated by error sources 308 to 307.  0: Delay timer start disabled  1: Delay timer start enabled |
| 26 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 25 to 0 | ECMNMITE305 to ECMNMITE280 | ECM delay timer start control bit  ECMNMITE305 to ECMNMITE280 correspond to non-maskable interrupts generated by error sources 305 to 280.  0: Delay timer start disabled  1: Delay timer start enabled |

NOTE

Reserved bit

The value of ECMNMITE bit listed as reserved for the given error input numbers in Table 39.18, Table 39.19 and Table 39.20 and Table 39.21 **Table 39.22**, **Table 39.23** and **Table 39.24**. When read, the value after reset is returned. When writing, write the value after reset.

### ECMEOCCFG ― ECM Error Output Clear Invalidation Configuration Register

This register is readable/writable register. Access by 32-bit units is possible.

After counter for Error Output clear invalidation exceed the value which is configured to this register, it is possible to clear non-safe status of error output by SW.

Configure to this register only if error output status is safe.

Writing to this register is protected by ECMKCPROT. Refer to Section 39.3.13, ECMKCPROT ― ECM Key Code Protection Register, for the details of key code protection.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H. |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | EOCI EN | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CMPW |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | ECMEOUTCLRT[15:0] | | | | | | | | | | | | | | | |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table . ECMEOCCFG Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 | EOCIEN | ERROROUT Clear Invalidation Function Enabled  0: Disabled  1: Enabled |
| 30 to 17 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 16 | CMPW | Indicates on execution of ECMEOUTCLRT[15:0] register setting to counter clock  domain  0: Not executed  1: On execution of setting ECMEOUTCLRT[15:0] |
| 15 to 0 | ECMEOUTCLRT [15:0] | The number of clock cycles after which it is possible to clear error output by SW. |

NOTES

1. ECMEOCCFG can be accessible via P-Bus. But Errorout release timer is run with not P-Bus clock but dedicated counter clock. When ECMEOCCFG is configured, this value is moved to dedicate counter clock domain to be able to be used by Errorout release timer. CMPW indicates the current status of ECMEOCCFG setting on dedicated counter clock domain.
2. While CMPW is “1”, writing of ECMEOUTCLRT[15:0] is ignored. Please confirm CMPW = 0 before writing of ECMEOUTCLRT[15:0].

### ECMPEM ― ECM Pseudo Error Mask Register

This register can mask the pseudo error of "ECM compare error" to support self-diagnosis of Errorout binder.

|  |  |  |
| --- | --- | --- |
| Value after reset: |  | 0000 0000H |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | — | — | — | — | — | — | — | — | — | — | — | — | — | — | MSKM | MSKC |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R/W | R/W |

Table . ECMPEM Register Contents

|  |  |  |
| --- | --- | --- |
| Bit Position | Bit Name | Function |
| 31 to 2 | — | Reserved  When read, the value after reset is returned. When writing, write the value after reset. |
| 1 | MSKM | 0: Pseudo error of "ECM compare error" for ECM master is NOT masked.  1: Pseudo error of "ECM compare error" for ECM master is masked. |
| 0 | MSKC | 0: Pseudo error of "ECM compare error" for ECM checker is NOT masked.  1: Pseudo error of "ECM compare error" for ECM checker is masked. |

## Related RFQ Items

Refer to ECM\_RFQ\_list.xlsx.