
Notes:

- Students are requested to submit the MIPS program(s)/source code and report (in pdf) to the elearning no later than 10-June-2019. All files need to be compressed into one .zip file before submitting.
 - Students have to execute program(s) on MARS MIPS as well as the Verilog-based processor on an FPGA board on Tuesday, 11-June-2019 at Room 511A4.
 - **Similarity less than 20% in both MIPS code and Verilog code is allowed. In other words, you will get 0 if your answers are similar to an another student more than 20%.**
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This question is used for both Computer Science and Computer Engineering students

Question 1. Given the following MIPS declaration in the data section of a MIPS program

```
.data
nums .word <an integer number>
elems .word <array elements>
```

Where <an integer number> will store the number of elements in the array elems. elems is an array that stores integer elements whose size is equal to value <an integer number>. You are required to choose those values when developing and testing your program.

1. Write a MIPS program that sort the the array elems in **descending order** using the **buble sort** algorithm. (*3 points*)
2. Calculate the execution time of your program if one instruction requires 1 ns for processing. (*1 point*)

Students must choose one of the following questions according to your major

Question 2. (For Computer Science) Given the following MIPS declaration in the data section of a MIPS program

```
.data
nums .word <an integer number>
elems .word <array elements>
```

Where <an integer number> will store the number of elements in the array elems. elems is an array that stores integer elements whose size is equal to value <an integer number>. You are required to choose those values when developing and testing your program.

1. Write a MIPS program that sort the the array elems in **ascending order** using the **quick sort** algorithm. (*5 points*)
2. Calculate the execution time of your program if one instruction requires 1 ns for processing. (*1 point*)

Question 3. (For Computer Engineering) (*6 point*) Design and implement a simple MIPS-based processor using the Verilog-HDL. The processor should be able to execute the following instructions:

add
sub
and
or
addi
beq
slt

The processor must be synthesized and implemented on an FPGA board (e.g., DE2i, DE2nano, or Zedboard). More hints can be found in this document: <http://bit.ly/2UA0J9J>

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