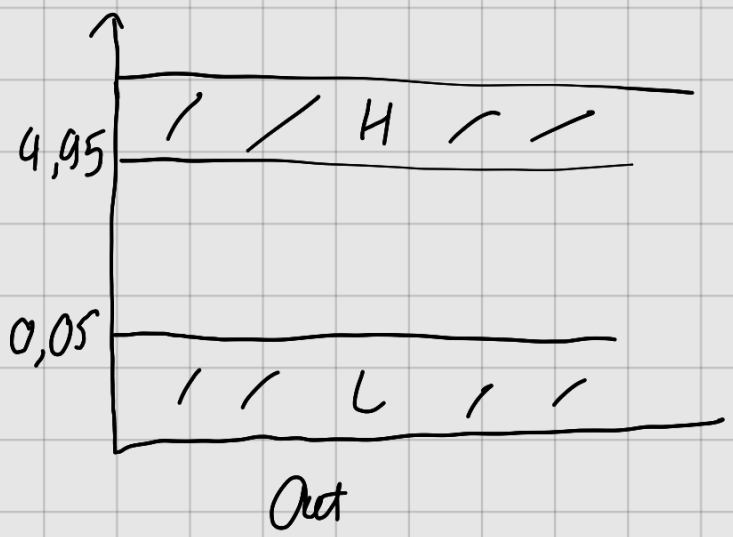
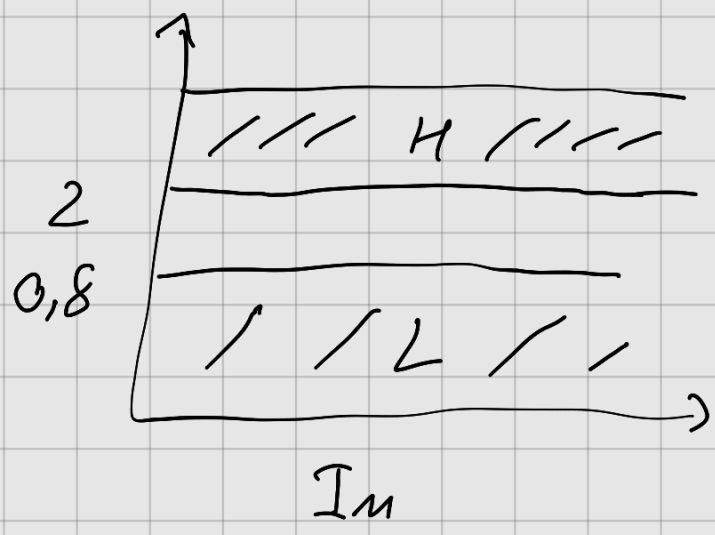
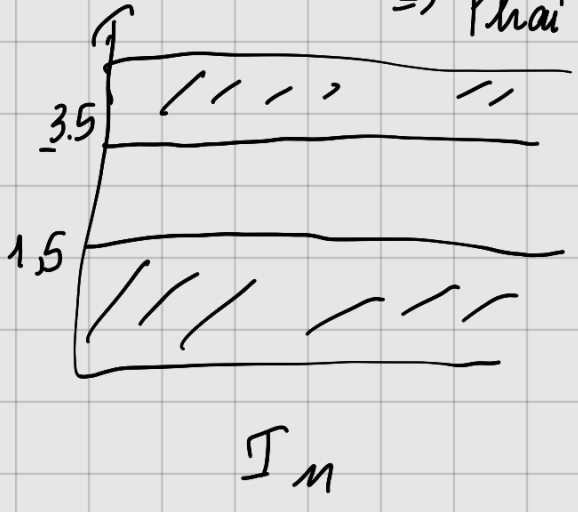
(I) { ① CMOS (4000) ; ② TTL (N) } ⇒ OK





(II) { TTL (N) ; CMOS (4000) } ⇒ NOT OK

⇒ Phải có mạch trung gian ① và ②



$$\underline{\text{Fan-Out}} = \min\left\{ \frac{|I_{OL\,gh}|}{|I_{IL\,gh}|}, \frac{|I_{OH\,gh}|}{|I_{IH\,gh}|} \right\}$$

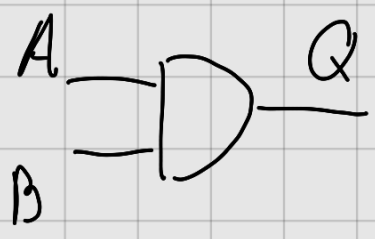
ALS (TTL)

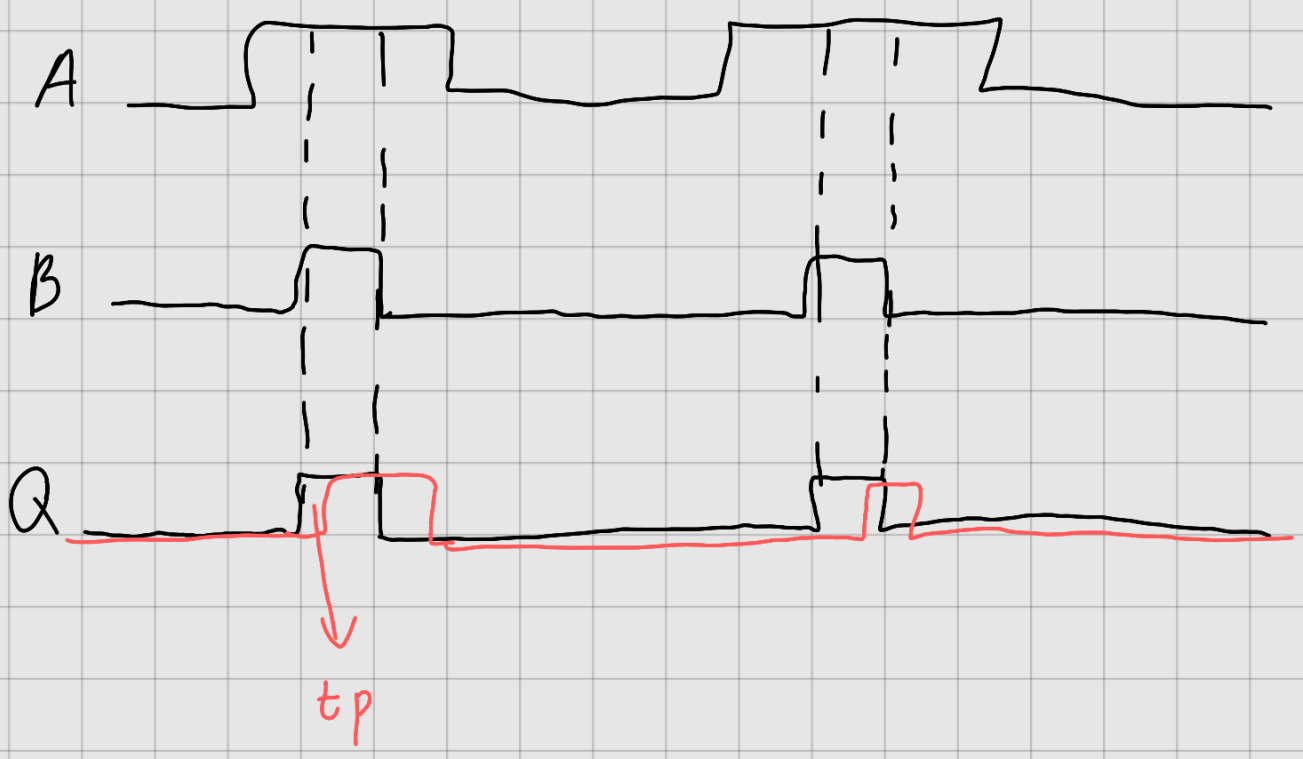
$$\text{Fan-Out} = \min\left\{ \frac{8}{0,2}, \frac{0,4}{0,02} \right\}$$

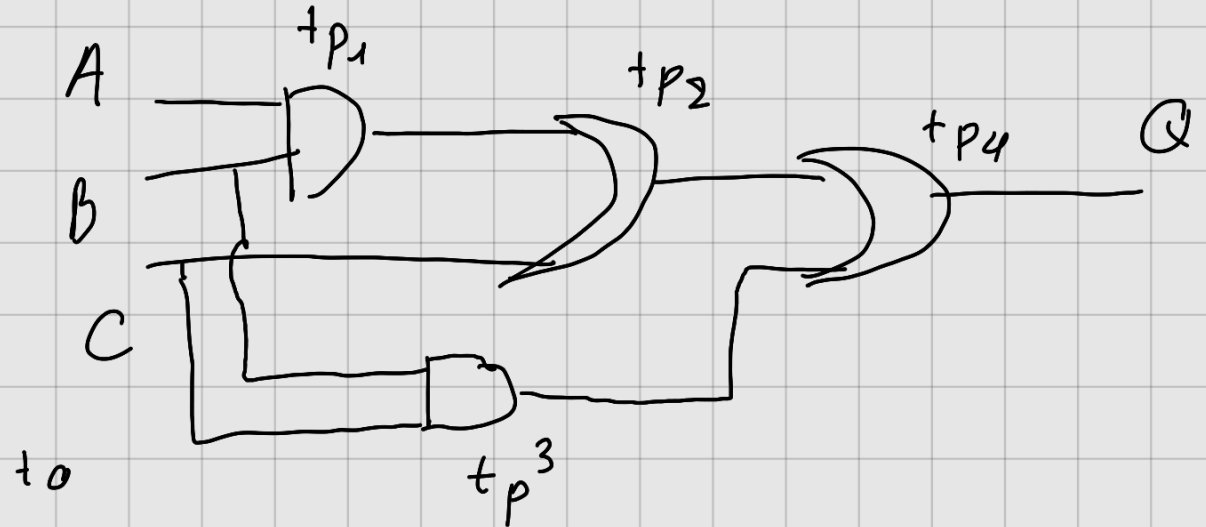
$= \min \{ 40, 20 \}$

$= 20$

* TP



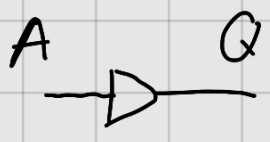




$\Rightarrow \quad t = \max \left(t_{p_1} + t_{p_2} , t_{p_3} \right) + t_{p_4}$

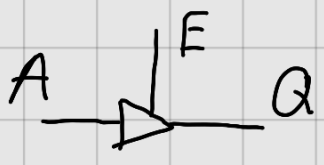
3 output logic circuit
- totempole (đẩy - kéo)
- open collector (cực góp để hở)
- tri-state → tri-state buffer

⊛ Buffer

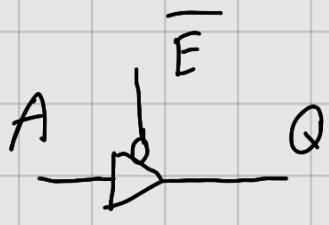


A	Q
0	0
1	1

⊛ Tri-state buffer



E	A	Q
active	0	0
	1	1
not active	X	Hi-Z



$\overline{E}$	A	Q
0	0	0
0	1	1
1	X	Hi-Z

E	A	Q
1	0	0
1	1	1
0	X	Hi-Z