Analysis and ringing suppressing method in 13.56MHz resonant inverter for wireless power transfer systems

NGUYEN KIEN TRUNG *KAN AKATSU* ***Shibaura Institute of Technology***

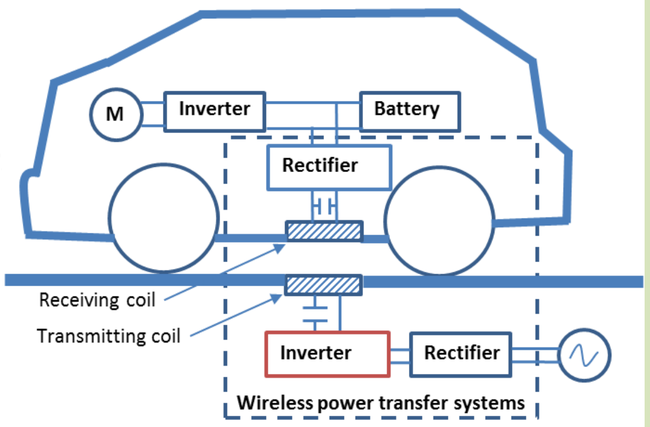
Target of this research

Design 1.5 kW class D resonant inverter for wireless power transfer systems operating at 13.56MHz.

Introduction

Design Parameter

- Operating frequency: 13.56 MHz
- Transfer distance: 1m
- Rate power: up to 10kW
- Step 1: Design 1.5kW
- Step 2: Design 3kW
- Step 3: Design 10kW



Electric vehicle running charging system

Research challenges

- Effect of parasitic elements
- Switching power loss
- High power and high efficiency.

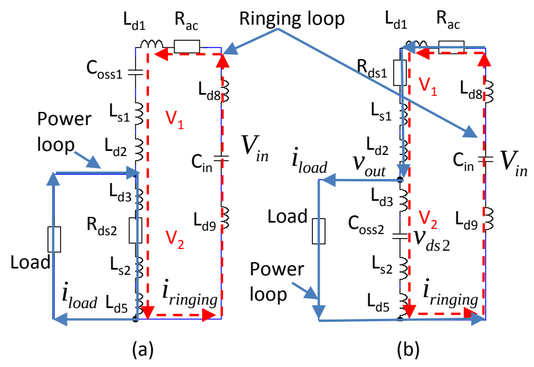
Problems

- Unstable
- High power loss
- Damage power switches

Solution

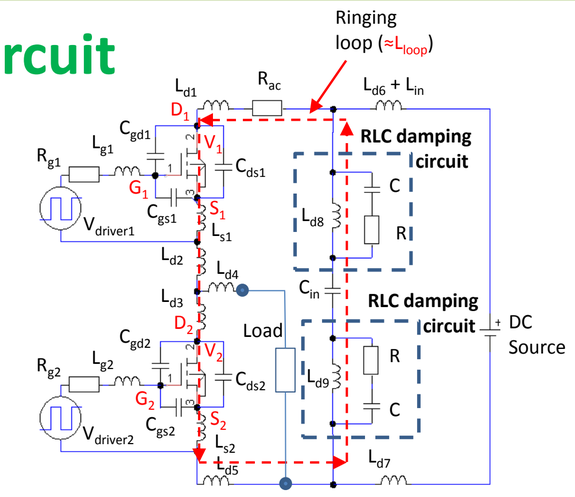
- Analysis effect of parasitic elements
- Optimize PCB design to minimize parasitic elements
- Ringing suppressing

❶ Proposed damping circuit



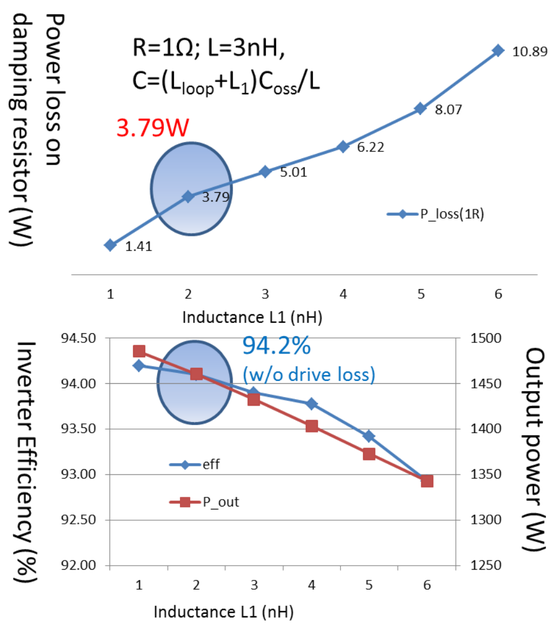
Equivalent circuit of ringing loop

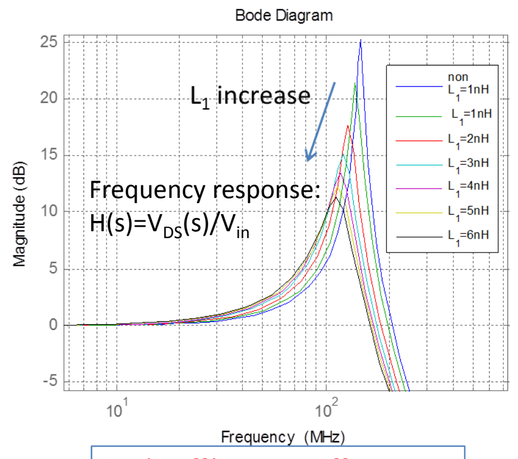
(a) V_1 :OFF and V_2: ON (b) V_1 :ON and V_2: OFF



RLC damping circuit

Damping circuit design

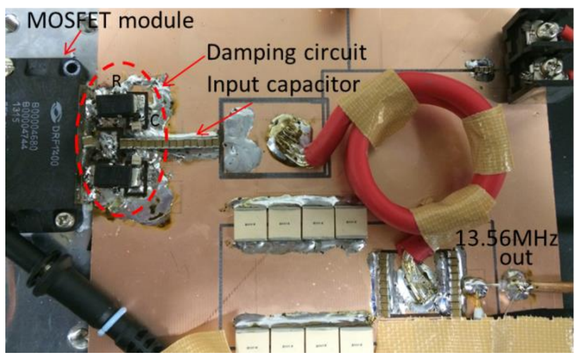




Trade-off between efficiency and damping coefficient

$L_{d8}=L_{d9}=L_1$

L: parasitic inductance of damping resistor

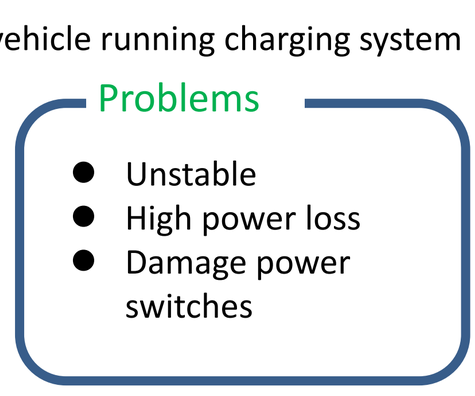


Prototype of proposed damping circuit

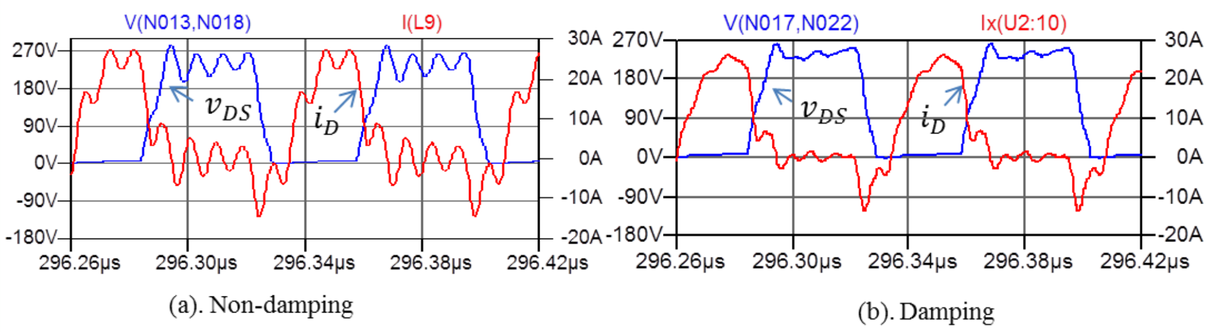
❷ Simulation results

Simulation and experiment parameters

Parameters	Non-damping	Proposed method
Input voltage	250V	
Resonant load	L5=228nH; C3=1µF;C4=800pF;R=50Ω	
MOSFET	DRF1400	
L_{loop}	$L_{d1}+L_{s1}+L_{d2}+L_{d3}+L_{s2}+L_{d5}$=4.8nH	
$L_{d8}=L_{d9}$	1nH	2nH
R		1Ω + 3nH
C		470pF

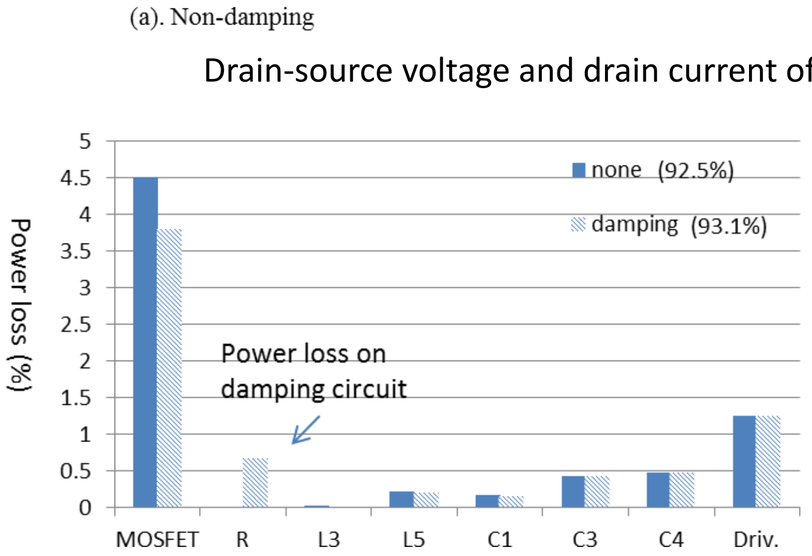


Resonant load in simulation and experiment



(a). Non-damping (b). Damping

Drain-source voltage and drain current of MOSFETs

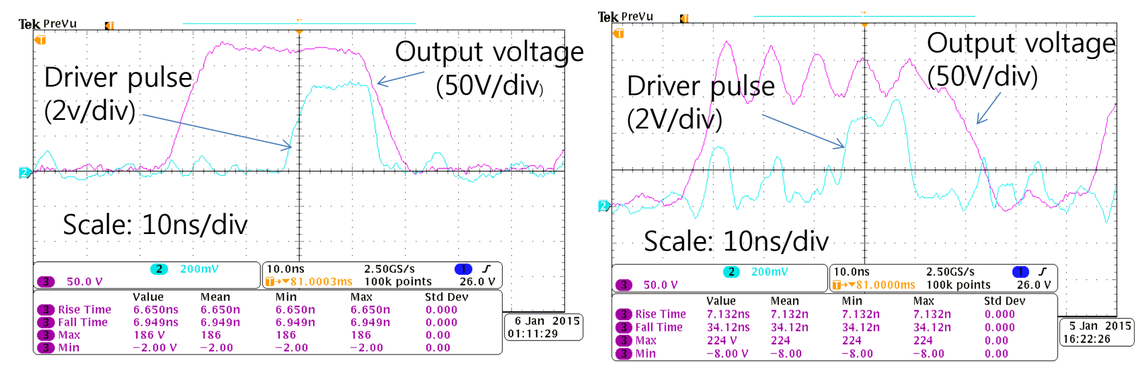


Power loss on 13.6MHz resonant inverter at 1.5kW

Result

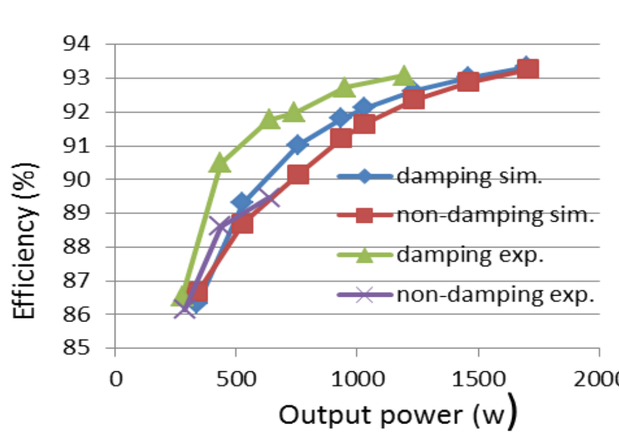
- The ringing is damped by proposed damping circuit
- Power loss on MOSFETs is reduced
- Efficiency is slightly increase

❸ Experiment result

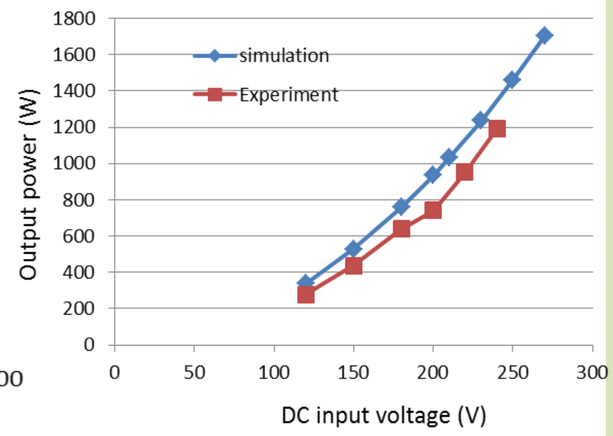


(a) damping (b) non-damping

Output voltage and driver pulse waveform (input voltage Vdc=180V)



Output power and efficiency



Input voltage and output power

Summary

- Without damping circuit, the inverter was unstable at 180Vdc
- With damping circuit, output voltage waveform and driver pulse waveform are clear. The inverter is stable. The peak efficiency obtain 93.1% at 1.2kW output power.
- Proposed damping circuit using parasitic inductance can control the parasitic inductance in the power loop. The circuit board become more compact and stable.