ESP32-S3

Hardware Design Guidelines

Release master
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Table of contents

Table of contents i

1 About This Document 3
- 1.1 Introduction . . . 3
- 1.2 Latest Version of This Document . . . 3

2 Product Overview 5

3 Schematic Checklist 7
- 3.1 Power Supply . . . 9
  - 3.1.1 Digital Power Supply . . . 9
  - 3.1.2 Analog Power Supply . . . 9
  - 3.1.3 RTC Power Supply . . . 11
- 3.2 Chip Power-up and Reset Timing . . . 11
- 3.3 Flash and PSRAM . . . 13
  - 3.3.1 In-Package Flash and PSRAM . . . 13
  - 3.3.2 Off-Package Flash and PSRAM . . . 14
- 3.4 Clock Source . . . 14
  - 3.4.1 External Crystal Clock Source (Compulsory) . . . 14
  - 3.4.2 RTC Clock Source (Optional) . . . 15
- 3.5 RF . . . 16
  - 3.5.1 RF Circuit . . . 16
  - 3.5.2 RF Tuning . . . 16
- 3.6 UART . . . 18
- 3.7 Strapping Pins . . . 18
- 3.8 GPIO . . . 19
- 3.9 ADC . . . 22
- 3.10 SDIO . . . 22
- 3.11 USB . . . 22
- 3.12 Touch Sensor . . . 23

4 PCB Layout Design 25
- 4.1 General Principles of PCB Layout . . . 25
- 4.2 Positioning a Module on a Base Board . . . 26
- 4.3 Power Supply . . . 28
  - 4.3.1 General Guidelines . . . 28
  - 4.3.2 3.3 V Power Layout . . . 28
  - 4.3.3 Analog Power Layout . . . 29
- 4.4 Crystal . . . 29
- 4.5 RF . . . 31
- 4.6 Flash and PSRAM . . . 31
- 4.7 UART . . . 33
- 4.8 USB . . . 34
- 4.9 SDIO . . . 34
- 4.10 Touch Sensor . . . 34
  - 4.10.1 Electrode Pattern . . . 35
  - 4.10.2 PCB Layout . . . 35

4.10.3 Waterproof and Proximity Sensing Design . . . 36
4.11 Typical Layout Problems and Solutions . . . 36
4.11.1 1. The voltage ripple is not large, but the TX performance of RF is rather poor. . . . 36
4.11.2 2. When ESP32-S3 sends data packages, the voltage ripple is small, but RF TX performance is poor. . . . 37
4.11.3 3. When ESP32-S3 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor. . . . 37
4.11.4 4. TX performance is not bad, but the RX sensitivity is low. . . . 38

5 Hardware Development **39**
5.1 ESP32-S3 Modules . . . 39
5.2 ESP32-S3 Development Boards . . . 39
5.3 Download Guidelines . . . 39

6 Related Documentation and Resources **41**

7 Glossary **43**

8 Revision History **45**
8.1 ESP Hardware Design Guidelines v1.0 . . . 45

9 Disclaimer and Copyright Notice **47**

This document provides guidelines for the ESP32-S3 SoC.

		
Schematic Checklist	PCB Layout Design	Hardware Development

Chapter 1

About This Document

1.1 Introduction

The hardware design guidelines advise on how to integrate ESP32-S3 into a product. These guidelines will help to achieve optimal performance of your product, ensuring technical accuracy and adherence to Espressif's standards. The guidelines are intended for hardware and application engineers.

The document assumes that you possess a certain level of familiarity with the ESP32-S3 SoC. In case you lack prior knowledge, we recommend utilizing this document in conjunction with the ESP32-S3 Series Datasheet.

1.2 Latest Version of This Document

Check the link to make sure that you use the latest version of this document: https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/index.html

Chapter 2

Product Overview

ESP32-S3 is a system on a chip that integrates the following features:

- Wi-Fi (2.4 GHz band)
- Bluetooth® 5 (LE)
- Dual high-performance Xtensa® 32-bit LX7 CPU cores
- Ultra Low Power coprocessor running either RISC-V or FSM core
- Multiple peripherals
- Built-in security hardware
- USB OTG interface
- USB Serial/JTAG Controller

Powered by 40 nm technology, ESP32-S3 provides a robust, highly-integrated platform, which helps meet the continuous demands for efficient power usage, compact design, security, high performance, and reliability. Typical application scenarios for ESP32-S3 include:

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- USB Devices
- Speech Recognition
- Image Recognition
- Wi-Fi + Bluetooth Networking Card
- Touch and Proximity Sensing

For more information about ESP32-S3, please refer to ESP32-S3 Series Datasheet.

Note: Unless otherwise specified, "ESP32-S3" used in this document refers to the series of chips, instead of a specific chip variant.

Chapter 3

Schematic Checklist

The integrated circuitry of ESP32-S3 requires only 20 electrical components (resistors, capacitors, and inductors) and a crystal, as well as an SPI flash. The high integration of ESP32-S3 allows for simple peripheral circuit design. This chapter details the schematic design of ESP32-S3.

The following figure shows a reference schematic design of ESP32-S3. It can be used as the basis of your schematic design.

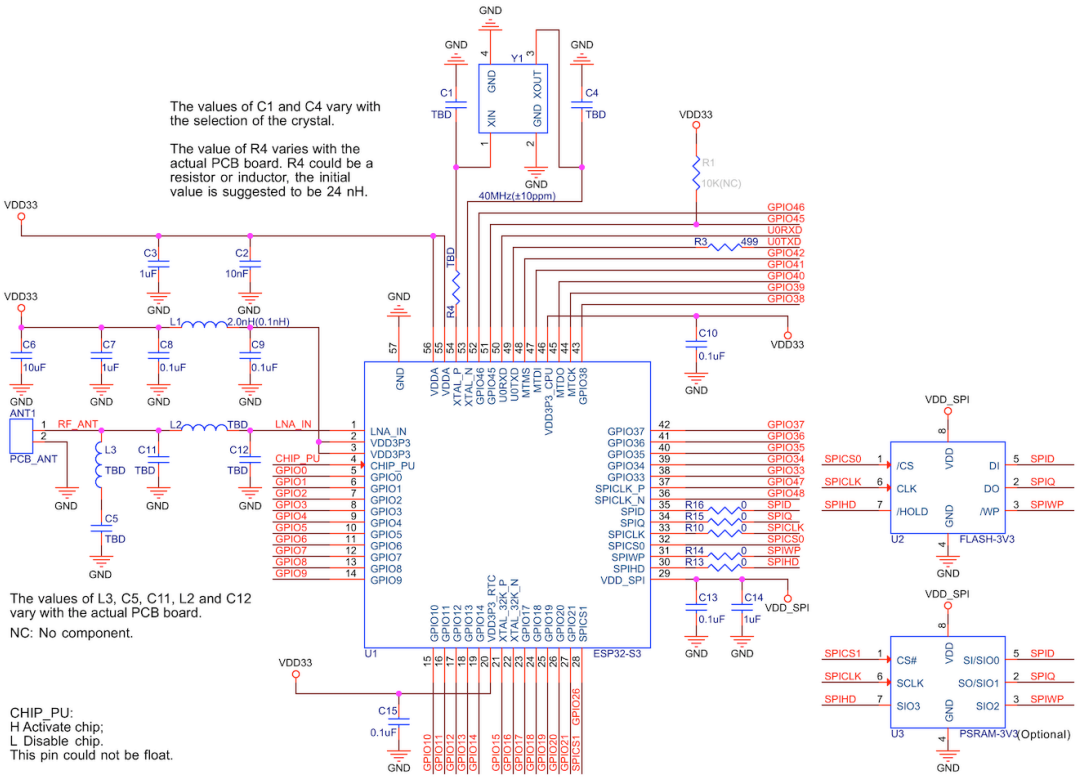

Fig. 1: ESP32-S3 Reference Schematic

Note that Figure *ESP32-S3 Reference Schematic* shows the connection for 3.3 V, quad, off-package SPI flash/PSRAM.

- In cases where 1.8 V or 3.3 V, octal, in-package or off-package SPI flash/PSRAM is used, GPIO33 ~ GPIO37 are occupied and cannot be used for other functions.
- If an in-package SPI flash/PSRAM is utilized, where VDD_SPI is set at either 1.8 V or 3.3 V, GPIO45 will no longer have any impact. In these scenarios, the presence of R1 is optional. However, in all other cases, refer to

Table *IO Pad Status After Chip Initialization in the USB-OTG Download Boot Mode* to determine whether R1 should be populated or not.

- The connection for 1.8 V, octal, off-package flash/PSRAM is as shown in Figure *ESP32-S3 Schematic for Off-Package 1.8 V Octal Flash/PSRAM*.
- When only in-package flash/PSRAM is used, there is no need to populate the resistor on the SPI traces or to care the SPI traces.

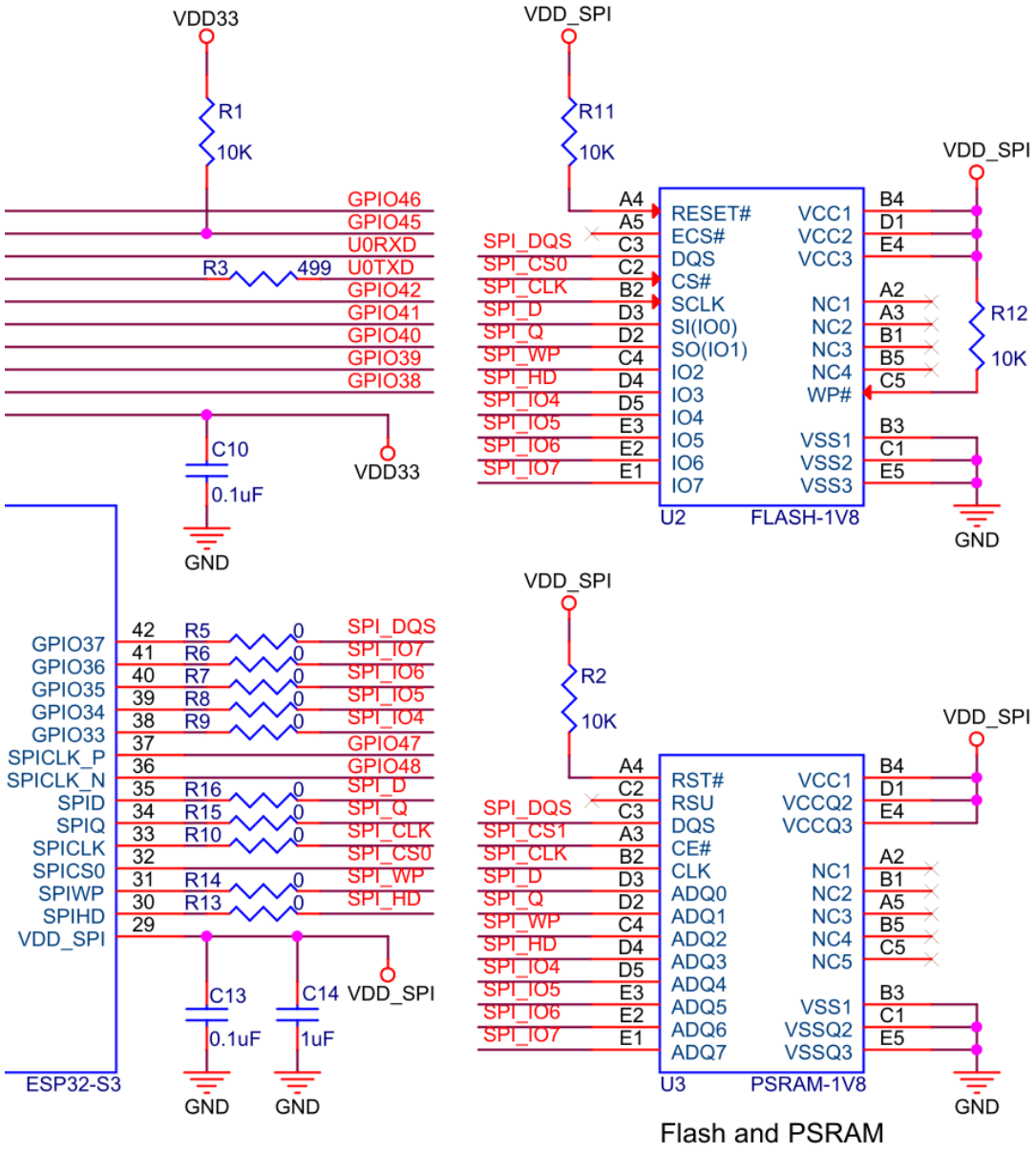

Fig. 2: ESP32-S3 Schematic for Off-Package 1.8 V Octal Flash/PSRAM

Any basic ESP32-S3 circuit design may be broken down into the following major building blocks:

- *Power supply*
- *Chip power-up and reset timing*
- *Flash and PSRAM*
- *Clock source*
- *RF*
- *UART*
- *Strapping pins*

- *GPIO*
- *ADC*
- *SDIO*
- *USB*
- *Touch sensor*

The rest of this chapter details the specifics of circuit design for each of these sections.

3.1 Power Supply

The general recommendations for power supply design are:

- When using a single power supply, the recommended power supply voltage is 3.3 V and the output current is no less than 500 mA.
- It is suggested to add an ESD protection diode at the power entrance.

More information about power supply pins can be found in ESP32-S3 Series Datasheet > Section *Power Supply*.

3.1.1 Digital Power Supply

ESP32-S3 has pin46 VDD3P3_CPU as the digital power supply pin(s) working in a voltage range of 3.0 V ~ 3.6 V. It is recommended to add an extra 0.1 µF decoupling capacitor close to the pin(s).

Pin VDD_SPI can serve as the power supply for the external device at either 1.8 V or 3.3 V (default). It is recommended to add extra 0.1 µF and 1 µF decoupling capacitors close to VDD_SPI.

- When VDD_SPI operates at 1.8 V, it is powered by ESP32-S3's internal LDO. The typical current this LDO can offer is 40 mA.
- When VDD_SPI operates at 3.3 V, it is driven directly by VDD3P3_RTC through a 14 Ω resistor, therefore, there will be some voltage drop from VDD3P3_RTC.

Attention: When using VDD_SPI as the power supply pin for in-package or off-package 3.3 V flash/PSRAM, the supply voltage should be 3.0 V or above, so as to meet the requirements of flash/PSRAM's working voltage.

Depending on the value of EFUSE_VDD_SPI_FORCE, the VDD_SPI voltage can be controlled in two ways, as Table *VDD_SPI Voltage Control* shows.

Table 1: VDD_SPI Voltage Control

EFUSE_VDD_SPI_FORC	EGPIO45	EFUSE_VDD_SPI_FORC	EVolt-age	VDD_SPI Power Source
0	0	Ignored	3.3 V	VDD3P3_RTC via R_{SPI} (default)
0	1	Ignored	1.8 V	Flash Voltage Regulator
1	Ignored	0	1.8 V	Flash Voltage Regulator
1	Ignored	1	3.3 V	VDD3P3_RTC via R_{SPI}

VDD_SPI can also be driven by an external power supply.

The schematic for the digital power supply pins is shown in Figure *ESP32-S3 Schematic for Digital Power Supply Pins*.

3.1.2 Analog Power Supply

ESP32-S3's VDDA and VDD3P3 pins are the analog power supply pins, working at 3.0 V ~ 3.6 V.

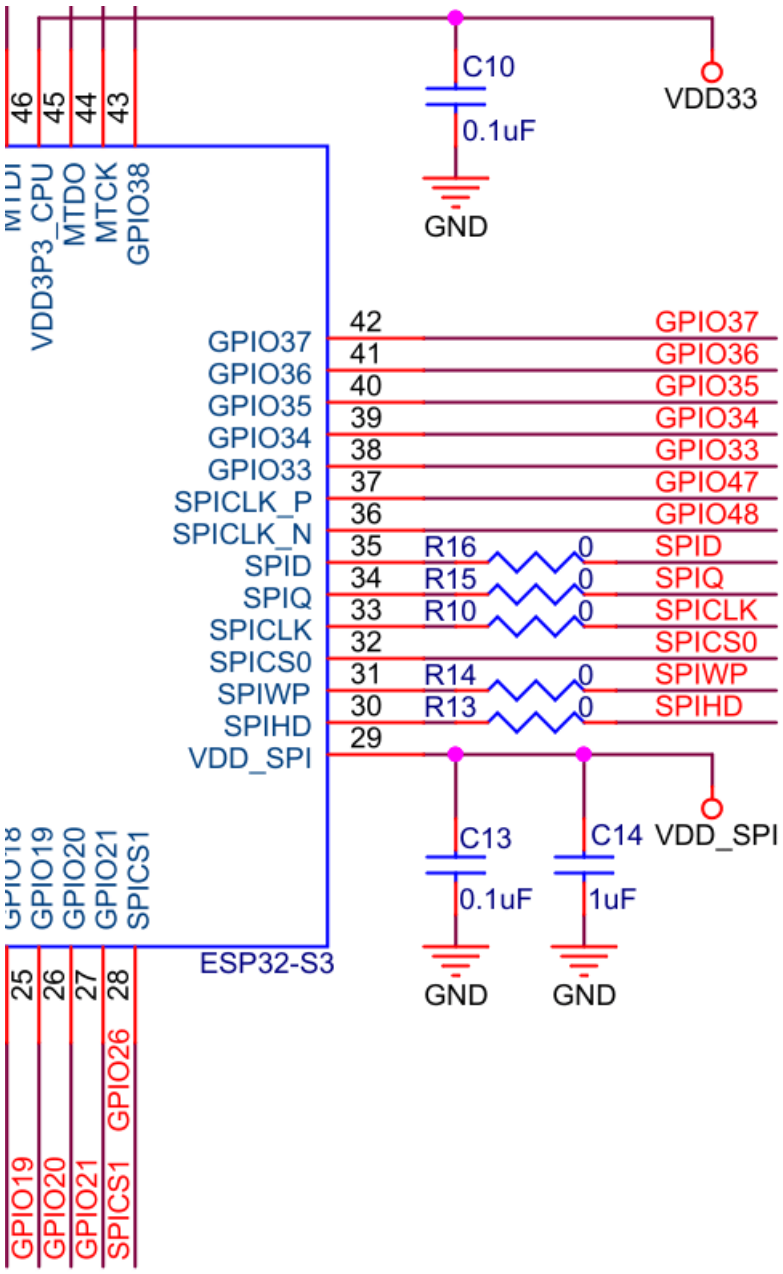

Fig. 3: ESP32-S3 Schematic for Digital Power Supply Pins

For VDD3P3, when ESP32-S3 is transmitting signals, there may be a sudden increase in the current draw, causing power rail collapse. Therefore, it is highly recommended to add a 10 µF capacitor to the power rail, which can work in conjunction with the 1 µF capacitor(s).

It is suggested to add an extra 10 µF capacitor at the power entrance. If the power entrance is close to VDD3P3, then two 10 µF capacitors can be merged into one.

Add a LC circuit on the VDD3P3 power rail to suppress high-frequency harmonics. The inductor's rated current is preferably 500 mA and above.

Place appropriate decoupling capacitors near the other analog power pins according to Figure *ESP32-S3 Schematic for Analog Power Supply Pins*.

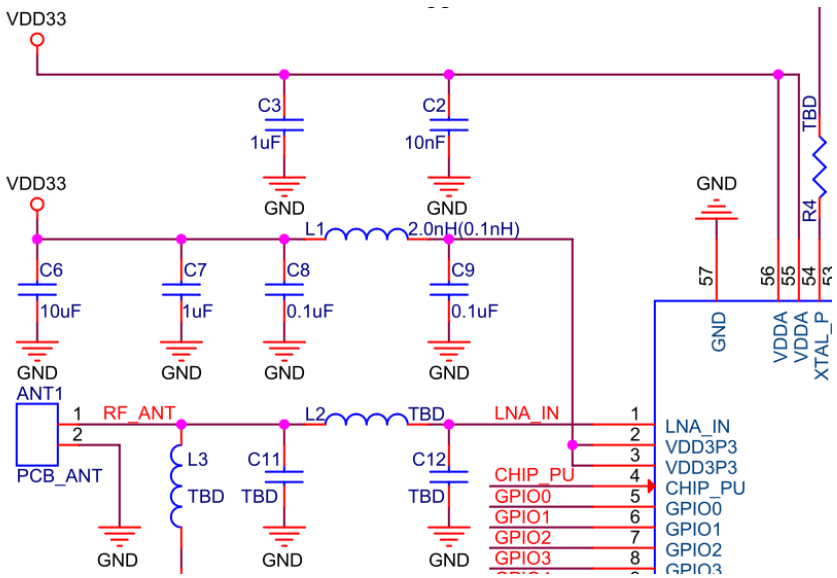

Fig. 4: ESP32-S3 Schematic for Analog Power Supply Pins

3.1.3 RTC Power Supply

ESP32-S3's VDD3P3_RTC pin is the RTC and analog power pin. It is recommended to place a 0.1 µF decoupling capacitor near this power pin in the circuit.

Note that this power supply cannot be used as a single backup power supply.

The schematic for the RTC power supply pin is shown in Figure *ESP32-S3 Schematic for RTC Power Supply Pin*.

3.2 Chip Power-up and Reset Timing

ESP32-S3's CHIP_PU pin can enable the chip when it is high and reset the chip when it is low.

When ESP32-S3 uses a 3.3 V system power supply, the power rails need some time to stabilize before CHIP_PU is pulled up and the chip is enabled. Therefore, CHIP_PU needs to be asserted high after the 3.3 V rails have been brought up.

To reset the chip, keep the reset voltage V_{IL_nRST} in the range of (–0.3 ~ 0.25 × VDD) V. To avoid reboots caused by external interferences, make the CHIP_PU trace as short as possible.

Figure *ESP32-S3 Power-up and Reset Timing* shows the power-up and reset timing of ESP32-S3.

Table *Description of Timing Parameters for Power-up and Reset* provides the specific timing requirements.

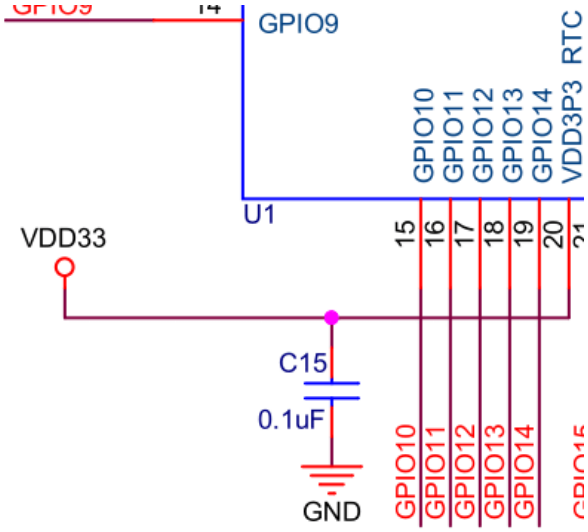

Fig. 5: ESP32-S3 Schematic for RTC Power Supply Pin

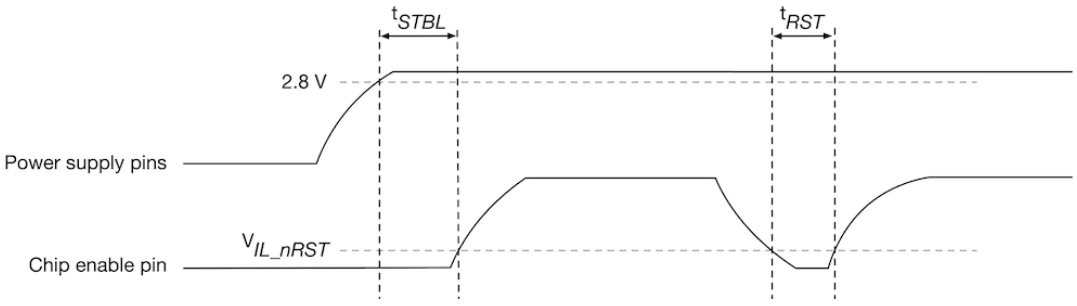

Fig. 6: ESP32-S3 Power-up and Reset Timing

Table 2: Description of Timing Parameters for Power-up and Reset

Parameter	Description	Minimum (µs)
t_{STBL}	Time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip	50
t_{RST}	Time reserved for CHIP_PU to stay below V_{IL_nRST} to reset the chip	50

Attention:

- CHIP_PU must not be left floating.
- To ensure the correct power-up and reset timing, it is advised to add an RC delay circuit at the CHIP_PU pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 µF. However, specific parameters should be adjusted based on the characteristics of the actual power supply and the power-up and reset timing of the chip.
- If the user application has one of the following scenarios:
  - Slow power rise or fall, such as during battery charging.
  - Frequent power on/off operations.
  - Unstable power supply, such as in photovoltaic power generation.

  Then, the RC circuit itself may not meet the timing requirements, resulting in the chip being unable to boot correctly. In this case, additional designs need to be added, such as:
  - Adding an external reset chip or a watchdog chip, typically with a threshold of around 3.0 V.
  - Implementing reset functionality through a button or the main controller.

3.3 Flash and PSRAM

ESP32-S3 requires in-package or off-package flash to store application firmware and data. In-package PSRAM or off-package RAM is optional.

3.3.1 In-Package Flash and PSRAM

The tables list the pin-to-pin mapping between the chip and in-package flash/PSRAM. Please note that the following chip pins can connect at most one flash and one PSRAM. That is to say, when there is only flash in the package, the pin occupied by flash can only connect PSRAM and cannot be used for other functions; when there is only PSRAM, the pin occupied by PSRAM can only connect flash; when there are both flash and PSRAM, the pin occupied cannot connect any more flash or PSRAM.

Table 3: Pin-to-Pin Mapping Between Chip and In-Package Quad SPI Flash

ESP32-S3FN8/ESP32-S3FH4R2	In-Package Flash (Quad SPI)
SPICLK	CLK
SPICS0	CS#
SPID	DI
SPIQ	DO
SPIWP	WP#
SPIHD	HOLD#

Table 4: Pin-to-Pin Mapping Between Chip and In-Package Quad SPI PSRAM

ESP32-S3R2/ESP32-S3FH4R2	In-Package PSRAM (2 MB, Quad SPI)
SPICLK	CLK
SPICS1	CE#
SPID	SI/SIO0
SPIQ	SO/SIO1
SPIWP	SIO2
SPIHD	SIO3

Table 5: Pin-to-Pin Mapping Between Chip and In-Package Octal SPI PSRAM

ESP32-S3R8/ESP32-S3R8V	In-Package PSRAM (8 MB, Octal SPI)
SPICLK	CLK
SPICS1	CE#
SPID	DQ0
SPIQ	DQ1
SPIWP	DQ2
SPIHD	DQ3
GPIO33	DQ4
GPIO34	DQ5
GPIO35	DQ6
GPIO36	DQ7
GPIO37	DQS/DM

3.3.2 Off-Package Flash and PSRAM

ESP32-S3 supports up to 1 GB off-package flash and 1 GB off-package RAM. If VDD_SPI is used to supply power, make sure to select the appropriate off-package flash and RAM according to the power voltage on VDD_SPI (1.8 V/3.3 V). It is recommended to add a zero-ohm series resistor on the SPI communication lines to lower the driving current, reduce interference to RF, adjust timing, and better shield from interference.

3.4 Clock Source

ESP32-S3 supports two external clock sources:

- *External crystal clock source (Compulsory)*
- *RTC clock source (Optional)*

3.4.1 External Crystal Clock Source (Compulsory)

The ESP32-S3 firmware only supports 40 MHz crystal.

The circuit for the crystal is shown in Figure *ESP32-S3 Schematic for External Crystal*. Note that the accuracy of the selected crystal should be within ±10 ppm.

Please add a series component (resistor or inductor) on the XTAL_P clock trace. Initially, it is suggested to use an inductor of 24 nH to reduce the impact of high-frequency crystal harmonics on RF performance, and the value should be adjusted after an overall test.

The initial values of external capacitors C1 and C4 can be determined according to the formula:

$$C_L = \frac{C1 \times C4}{C1 + C4} + C_{stray}$$

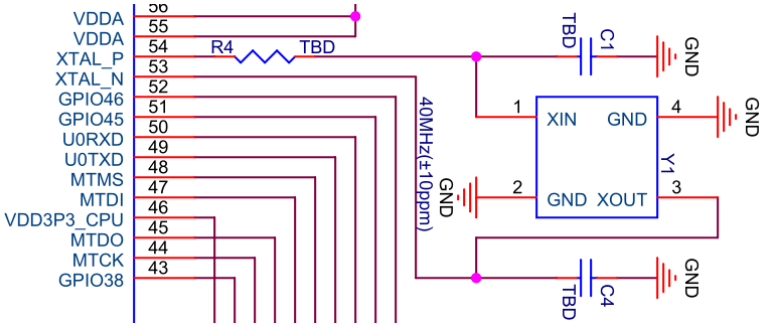

Fig. 7: ESP32-S3 Schematic for External Crystal

where the value of C_L (load capacitance) can be found in the crystal's datasheet, and the value of C_{stray} refers to the PCB's stray capacitance. The values of C1 and C4 need to be further adjusted after an overall test as below:

1. Select TX tone mode using the Certification and Test Tool.
2. Observe the 2.4 GHz signal with a radio communication analyzer or a spectrum analyzer and demodulate it to obtain the actual frequency offset.
3. Adjust the frequency offset to be within ±10 ppm (recommended) by adjusting the external load capacitance.

- When the center frequency offset is positive, it means that the equivalent load capacitance is small, and the external load capacitance needs to be increased.
- When the center frequency offset is negative, it means the equivalent load capacitance is large, and the external load capacitance needs to be reduced.
- External load capacitance at the two sides are usually equal, but in special cases, they may have slightly different values.

Note:

- Defects in the manufacturing of crystal (for example, large frequency deviation of more than ±10 ppm, unstable performance within the operating temperature range, etc) may lead to the malfunction of ESP32-S3, resulting in a decrease of the RF performance.
- It is recommended that the amplitude of the crystal is greater than 500 mV.
- When Wi-Fi or Bluetooth connection fails, after ruling out software problems, you may follow the steps mentioned above to ensure that the frequency offset meets the requirements by adjusting capacitors at the two sides of the crystal.

3.4.2 RTC Clock Source (Optional)

ESP32-S3 supports an external 32.768 kHz crystal or an external signal (e.g., an oscillator) to act as the RTC clock. The external RTC clock source enhances timing accuracy and consequently decreases average power consumption, without impacting functionality.

Figure *ESP32-S3 Schematic for 32.768 kHz Crystal* shows the schematic for the external 32.768 kHz crystal.

Please note the requirements for the 32.768 kHz crystal:

- Equivalent series resistance (ESR) ≤ 70 kΩ.
- Load capacitance at both ends should be configured according to the crystal's specification.

The parallel resistor R is used for biasing the crystal circuit (5 MΩ < R ≤ 10 MΩ). In general, you do not need to populate the resistor.

If the RTC clock source is not required, then the pins for the 32.768 kHz crystal can be used as GPIOs.

The external signal can be input to the XTAL's P end through a DC blocking capacitor (about 20 pF). The XTAL's N end can be floating. Figure *ESP32-S3 Schematic for External Oscillator* shows the schematic of the external signal.

The signal should meet the following requirements:

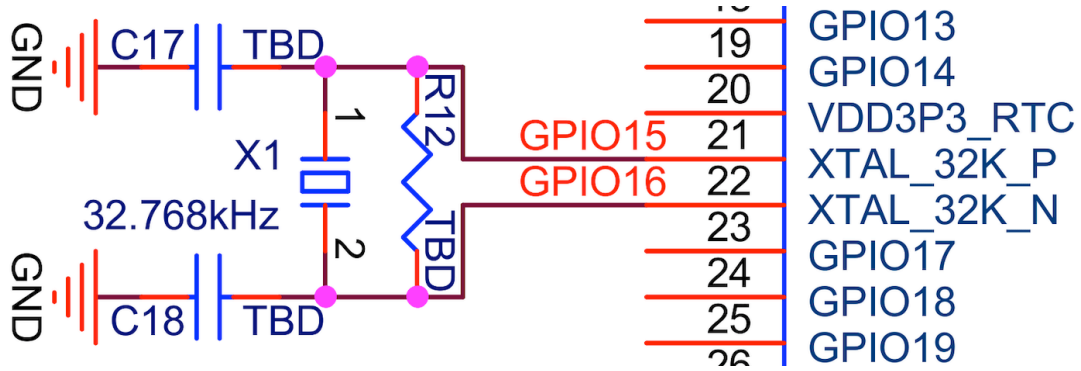

Fig. 8: ESP32-S3 Schematic for 32.768 kHz Crystal

Fig. 9: ESP32-S3 Schematic for External Oscillator

External signal	Amplitude (Vpp, unit: V)
Sine wave or square wave	0.6 < Vpp < VDD

3.5 RF

3.5.1 RF Circuit

ESP32-S3 ' s RF circuit is mainly composed of three parts, the RF traces on the PCB board, the chip matching circuit, the antenna and the antenna matching circuit. Each part should meet the following requirements:

- For the RF traces on the PCB board, 50 Ω impedance control is required.
- For the chip matching circuit, it must be placed close to the chip. A CLC structure is preferred.
  - The CLC structure is mainly used to adjust the impedance point and suppress harmonics, and a set of LC can be added if space permits.
  - The RF matching circuit is shown in Figure *ESP32-S3 Schematic for RF Matching*.
- For the antenna and the antenna matching circuit, to ensure radiation performance, the antenna ' s characteristic impedance must be around 50 Ω. Adding a CLC matching circuit near the antenna is recommended to adjust the antenna. However, if the available space is limited and the antenna impedance point can be guaranteed to be 50 Ω by simulation, then there is no need to add a matching circuit near the antenna.

3.5.2 RF Tuning

The RF matching parameters vary with the board, so the ones used in Espressif modules could not be applied directly. Follow the instructions below to do RF tuning.

Figure *ESP32-S3 RF Tuning Diagram* shows the general process of RF tuning.

In the matching circuit, define the port near the chip as Port 1 and the port near the antenna as Port 2. S11 describes the ratio of the signal power reflected back from Port 1 to the input signal power, the transmission performance is best if the matching impedance is conjugate to the chip impedance. S21 is used to describe the transmission loss of signal from Port 1 to Port 2. If S11 is close to the chip conjugate point (35+j0) and S21 is less than -35 dB at 4.8 GHz and 7.2 GHz, the matching circuit can satisfy transmission requirements.

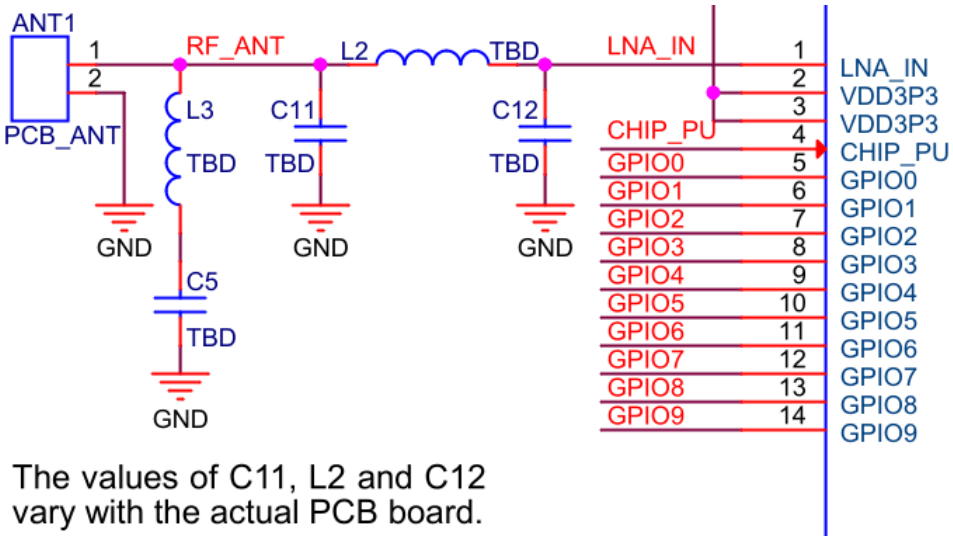

Fig. 10: ESP32-S3 Schematic for RF Matching

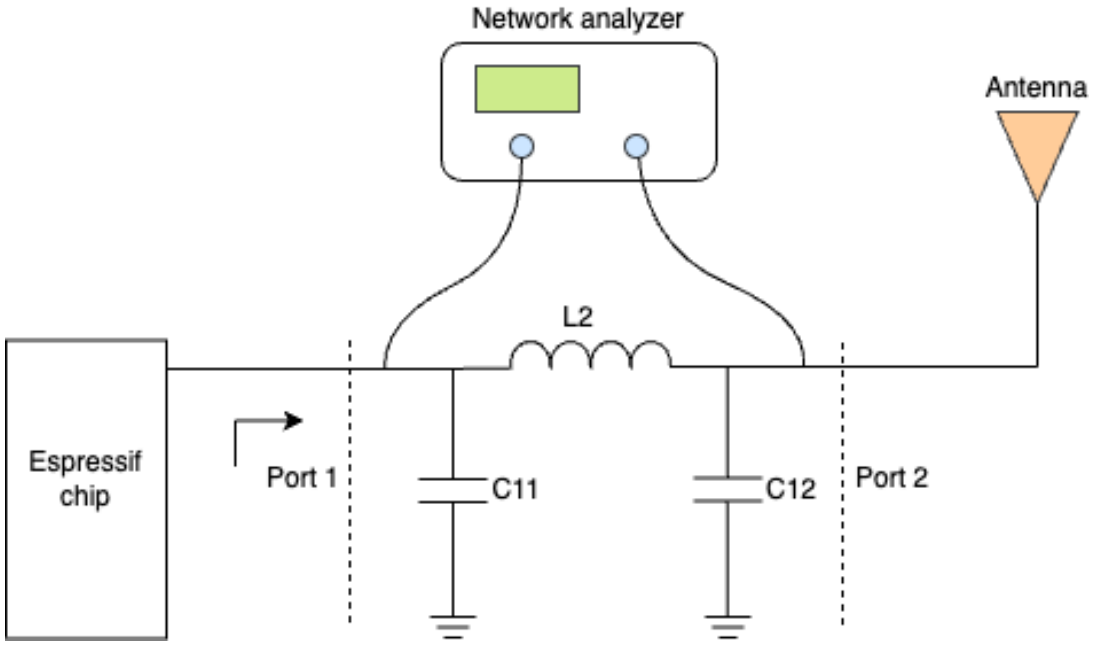

Fig. 11: ESP32-S3 RF Tuning Diagram

Connect the two ends of the matching circuit to the network analyzer, and test its signal reflection parameter S11 and transmission parameter S21. Adjust the values of the components in the circuit until S11 and S21 meet the requirements. If your PCB design of the chip strictly follows the PCB design stated in Chapter *PCB Layout Design*, you can refer to the value ranges in Table *Recommended Value Ranges for Components* to debug the matching circuit.

Table 6: Recommended Value Ranges for Components

Reference Designator	Recommended Value Range	Serial No.
C11	1.2 ~ 1.8 pF	GRM0335C1H1RXBA01D
L2	2.4 ~ 3.0 nH	LQP03TN2NXB02D
C12	1.8 ~ 1.2 pF	GRM0335C1H1RXBA01D

If the components are in the 0201 SMD package size, please use a stub in the PCB design of the RF matching circuit near the chip. If the antenna input impedance is not 50 ohm, an additional set of RF matching is recommended for antenna tuning.

If the usage or production environment is sensitive to electrostatic discharge, it is recommended to reserve ESD protection devices near the antenna.

Note: If RF function is not required, then the RF pin can be left floating.

3.6 UART

It is recommended to connect a 499 Ω series resistor to the U0TXD line to suppress the 80 MHz harmonics.

Usually, UART0 is used as the serial port for download and log printing. For instructions on download over UART0, please refer to Section *Download Guidelines*.

Other UART interfaces can be used as serial ports for communication, which could be mapped to any available GPIO by software configurations. For these interfaces, it is also recommended to add a series resistor to the TX line to suppress harmonics.

When using the AT firmware, please note that the UART GPIO is already configured (refer to AT Firmware Download). It is recommended to use the default configuration.

3.7 Strapping Pins

At each startup or reset, a chip requires some initial configuration parameters, such as in which boot mode to load the chip, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins work as normal function pins.

All the information about strapping pins is covered in ESP32-S3 Series Datasheet > Section *Strapping Pins*. In this document, we will mainly cover the strapping pins related to boot mode.

After chip reset is released, the combination of GPIO0 and GPIO46 controls the boot mode. See Table *Boot Mode Control*.

Table 7: Boot Mode Control

Boot Mode	GPIO0	GPIO46
Default Config	1 (Pull-up)	0 (Pull-down)
SPI Boot (default)	1	Any value
Joint Download Boot[1]	0	0
Invalid combination[2]	0	1

[1] Joint Download Boot mode supports the following download methods:

Signals applied to the strapping pins should have specific *setup time* and *hold time*. For more information, see Figure *Setup and Hold Times for Strapping Pins* and Table *Description of Timing Parameters for Strapping Pins*.

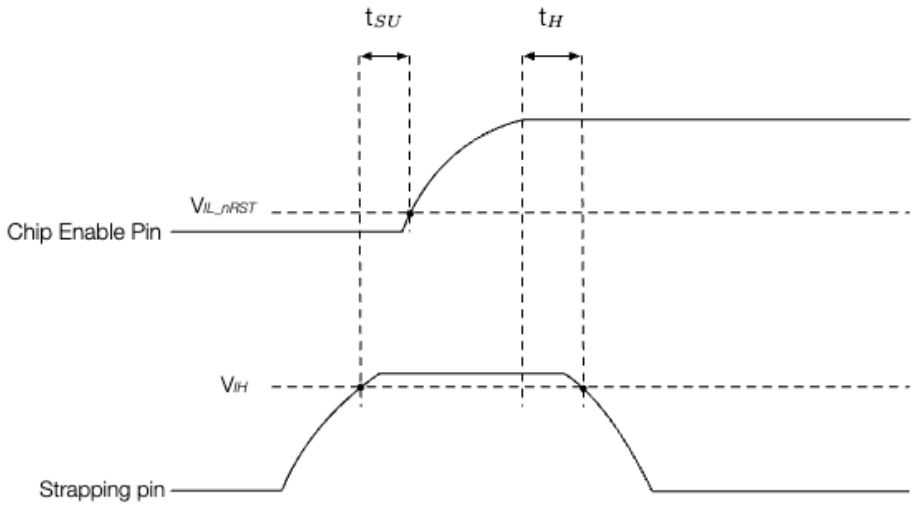

Fig. 12: Setup and Hold Times for Strapping Pins

Table 8: Description of Timing Parameters for Strapping Pins

Parameter	Description	Minimum (ms)
t_{SU}	Time reserved for the power rails to stabilize before the chip enable pin (CHIP_PU) is pulled high to activate the chip.	0
t_{H}	Time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

Attention: Do not add high-value capacitors at GPIO0, otherwise, the chip may not boot successfully.

3.8 GPIO

The pins of ESP32-S3 can be configured via IO MUX or GPIO matrix. IO MUX provides the default pin configurations, whereas the GPIO matrix is used to route signals from peripherals to GPIO pins. For more information about IO MUX and GPIO matrix, please refer to ESP32-S3 Technical Reference Manual > Chapter *IO MUX and GPIO Matrix*.

Some peripheral signals have already been routed to certain GPIO pins, while some can be routed to any available GPIO pins. For details, please refer to ESP32-S3 Series Datasheet > Section *Peripheral Pin Configurations*.

When using GPIOs, please:

- Pay attention to the states of strapping pins during power-up.

- USB Download Boot:
  - USB-Serial-JTAG Download Boot
  - USB-OTG Download Boot
- UART Download Boot

[2] This combination triggers unexpected behavior and should be avoided.

- Pay attention to the default configurations of the GPIOs after reset. The default configurations can be found in Table *IO MUX Pin Functions*. It is recommended to add a pull-up or pull-down resistor to pins in the high-impedance state or enable the pull-up and pull-down during software initialization to avoid extra power consumption.
- Avoid using the pins already occupied by flash/PSRAM.
- Some pins will have glitches during power-up. Refer to Table *Power-Up Glitches on Pins* for details.
- When USB-OTG Download Boot mode is enabled, some pins will have level output. Refer to Table *IO Pad Status After Chip Initialization in the USB-OTG Download Boot Mode* for details.
- SPICLK_N, SPICLK_P, and GPIO33 ~ GPIO37 work in the same power domain, so if octal 1.8 V flash/PSRAM is used, then SPICLK_P and SPICLK_N also work in the 1.8 V power domain.
- Only GPIOs in the VDD3P3_RTC power domain can be controlled in Deep-sleep mode.

Table 9: IO MUX Pin Functions

No.	Name	Type	Power	At Reset	After Reset	IO MUX	RTC	Analog
1	LNA_IN	Analog						
2	VDD3P3	Power						
3	VDD3P3	Power						
4	CHIP_PU	Analog	VDD3P3_RTC					
5	GPIO0	IO	VDD3P3_RTC	IE, WPU	IE, WPU	IO MUX	RTC	
6	GPIO1	IO	VDD3P3_RTC	IE	IE	IO MUX	RTC	Analog
7	GPIO2	IO	VDD3P3_RTC	IE	IE	IO MUX	RTC	Analog
8	GPIO3	IO	VDD3P3_RTC	IE	IE	IO MUX	RTC	Analog
9	GPIO4	IO	VDD3P3_RTC			IO MUX	RTC	Analog
10	GPIO5	IO	VDD3P3_RTC			IO MUX	RTC	Analog
11	GPIO6	IO	VDD3P3_RTC			IO MUX	RTC	Analog
12	GPIO7	IO	VDD3P3_RTC			IO MUX	RTC	Analog
13	GPIO8	IO	VDD3P3_RTC			IO MUX	RTC	Analog
14	GPIO9	IO	VDD3P3_RTC		IE	IO MUX	RTC	Analog
15	GPIO10	IO	VDD3P3_RTC		IE	IO MUX	RTC	Analog
16	GPIO11	IO	VDD3P3_RTC		IE	IO MUX	RTC	Analog
17	GPIO12	IO	VDD3P3_RTC		IE	IO MUX	RTC	Analog
18	GPIO13	IO	VDD3P3_RTC		IE	IO MUX	RTC	Analog
19	GPIO14	IO	VDD3P3_RTC		IE	IO MUX	RTC	Analog
20	VDD3P3_RTC	Power						
21	XTAL_32K_P	IO	VDD3P3_RTC			IO MUX	RTC	Analog
22	XTAL_32K_N	IO	VDD3P3_RTC			IO MUX	RTC	Analog
23	GPIO17	IO	VDD3P3_RTC		IE	IO MUX	RTC	Analog
24	GPIO18	IO	VDD3P3_RTC		IE	IO MUX	RTC	Analog
25	GPIO19	IO	VDD3P3_RTC			IO MUX	RTC	Analog
26	GPIO20	IO	VDD3P3_RTC	USB_PU	USB_PU	IO MUX	RTC	Analog
27	GPIO21	IO	VDD3P3_RTC			IO MUX	RTC	
28	SPICS1	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
29	VDD_SPI	Power						
30	SPIHD	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
31	SPIWP	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
32	SPICS0	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
33	SPICLK	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
34	SPIQ	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
35	SPID	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
36	SPICLK_N	IO	VDD_SPI / VDD3P3_CPU	IE	IE	IO MUX		
37	SPICLK_P	IO	VDD_SPI / VDD3P3_CPU	IE	IE	IO MUX		
38	GPIO33	IO	VDD_SPI / VDD3P3_CPU		IE	IO MUX		
39	GPIO34	IO	VDD_SPI / VDD3P3_CPU		IE	IO MUX		
40	GPIO35	IO	VDD_SPI / VDD3P3_CPU		IE	IO MUX		
41	GPIO36	IO	VDD_SPI / VDD3P3_CPU		IE	IO MUX		

continues on next page

Table 9 – continued from previous page

No.	Name	Type	Power	At Reset	After Reset	IO MUX	RTC	Analog
42	GPIO37	IO	VDD_SPI / VDD3P3_CPU		IE	IO MUX		
43	GPIO38	IO	VDD3P3_CPU		IE	IO MUX		
44	MTCK	IO	VDD3P3_CPU		IE	IO MUX		
45	MTDO	IO	VDD3P3_CPU		IE	IO MUX		
46	VDD3P3_CPU	Power						
47	MTDI	IO	VDD3P3_CPU		IE	IO MUX		
48	MTMS	IO	VDD3P3_CPU		IE	IO MUX		
49	U0TXD	IO	VDD3P3_CPU	IE, WPU	IE, WPU	IO MUX		
50	U0RXD	IO	VDD3P3_CPU	IE, WPU	IE, WPU	IO MUX		
51	GPIO45	IO	VDD3P3_CPU	IE, WPD	IE, WPD	IO MUX		
52	GPIO46	IO	VDD3P3_CPU	IE, WPD	IE, WPD	IO MUX		
53	XTAL_N	Analog						
54	XTAL_P	Analog						
55	VDDA	Power						
56	VDDA	Power						
57	GND	Power						

- IE –input enabled
- WPU –internal weak pull-up resistor enabled
- WPD –internal weak pull-down resistor enabled
- USB_PU –USB pull-up resistor enabled
  - By default, the USB function is enabled for USB pins (i.e., GPIO19 and GPIO20), and the pin pull-up is decided by the USB pull-up resistor. The USB pull-up resistor is controlled by USB_SERIAL_JTAG_DP/DM_PULLUP and the pull-up value is controlled by USB_SERIAL_JTAG_PULLUP_VALUE. For details, see ESP32-S3 Technical Reference Manual > Chapter *USB Serial/JTAG Controller*.
  - When the USB function is disabled, USB pins are used as regular GPIOs and the pin's internal weak pull-up and pull-down resistors are disabled by default (configurable by IO_MUX_FUN_WPU/WPD)

Table 10: Power-Up Glitches on Pins

Pin	Glitch[3]	Typical Time (µs)
GPIO1	Low-level glitch	60
GPIO2	Low-level glitch	60
GPIO3	Low-level glitch	60
GPIO4	Low-level glitch	60
GPIO5	Low-level glitch	60
GPIO6	Low-level glitch	60
GPIO7	Low-level glitch	60
GPIO8	Low-level glitch	60
GPIO9	Low-level glitch	60
GPIO10	Low-level glitch	60
GPIO11	Low-level glitch	60
GPIO12	Low-level glitch	60
GPIO13	Low-level glitch	60
GPIO14	Low-level glitch	60
XTAL_32K_P	Low-level glitch	60
XTAL_32K_N	Low-level glitch	60
GPIO17	Low-level glitch	60
GPIO18	Low-level/High-level glitch	60
GPIO19	Low-level glitch/High-level glitch[4]	60
GPIO20	Pull-down glitch/High-level glitch[Page 22, 4]	60

[3]
- Low-level glitch: the pin is at a low level output status during the time period;
- High-level glitch: the pin is at a high level output status during the time period;

3.9 ADC

Please add a 0.1 µF filter capacitor between ESP pins and ground when using the ADC function to improve accuracy.

ADC1 is recommended for use.

The calibrated ADC results after hardware calibration and software calibration are shown in the list below. For higher accuracy, you may implement your own calibration methods.

- When ATTEN=0 and the effective measurement range is 0 ~ 850 mV, the total error is ±5 mV.
- When ATTEN=1 and the effective measurement range is 0 ~ 1100 mV, esp32c6=, the total error is ±6 mV.
- When ATTEN=2 and the effective measurement range is 0 ~ 1600 mV, the total error is ±10 mV.
- When ATTEN=3 and the effective measurement range is 0 ~ 2900 mV, the total error is ±50 mV.

3.10 SDIO

ESP32-S3 only has one SD/MMC Host controller, which cannot be used as a slave device.

The SDIO interface can be configured to any free GPIO by software. Please add pull-up resistors to the SDIO GPIO pins, and it is recommended to reserve a series resistor on each trace.

3.11 USB

ESP32-S3 has a full-speed USB On-The-Go (OTG) peripheral with integrated transceivers. The USB peripheral is compliant with the USB 2.0 specification.

ESP32-S3 integrates a USB Serial/JTAG controller that supports USB 2.0 full-speed device.

GPIO19 and GPIO20 can be used as D- and D + of USB respectively. It is recommended to populate zero-ohm series resistors between the mentioned pins and the USB connector. Also, reserve a footprint for a capacitor to ground on each trace. Note that both components should be placed close to the chip.

Note that USB_D+ will have level output, so please add a pull-up resistor to determine the initial high-level output voltage.

ESP32-S3 also supports download functions and log message printing via USB. For details please refer to Section *Download Guidelines*.

When USB-OTG Download Boot mode is enabled, the chip initializes the IO pad connected to the external PHY in ROM when starts up. The status of each IO pad after initialization is as follows.

Table 11: IO Pad Status After Chip Initialization in the USB-OTG Download Boot Mode

IO Pad	Input/Output Mode	Level Status
VP (MTMS)	INPUT	–
VM (MTDI)	INPUT	–
RCV (GPIO21)	INPUT	–
OEN (MTDO)	OUTPUT	HIGH
VPO (MTCK)	OUTPUT	LOW
VMO(GPIO38)	OUTPUT	LOW

- Pull-down glitch: the pin is at an internal weak pulled-down status during the time period;
- Pull-up glitch: the pin is at an internal weak pulled-up status during the time period.

[4] GPIO19 and GPIO20 pins both have two high-level glitches during chip power-up, each lasting for about 60 µs. The total duration for the glitches and the delay are 3.2 ms and 2 ms respectively for GPIO19 and GPIO20.

If the USB-OTG Download Boot mode is not needed, it is suggested to disable the USB-OTG Download Boot mode by setting the eFuse bit EFUSE_DIS_USB_OTG_DOWNLOAD_MODE to avoid IO pad state change.

3.12 Touch Sensor

When using the touch function, it is recommended to populate a zero-ohm series resistor at the chip side to reduce the coupling noise and interference on the line, and to strengthen the ESD protection. The recommended resistance is from 470 Ω to 2 kΩ, preferably 510 Ω. The specific value depends on the actual test results of the product.

The ESP32-S3 touch sensor has a waterproof design and digital filtering function. Note that only GPIO14 (TOUCH14) can drive the shield electrode.

Chapter 4

PCB Layout Design

This chapter introduces the key points of how to design an ESP32-S3 PCB layout using an ESP32-S3 module (see Figure *ESP32-S3 Reference PCB Layout*) as an example.

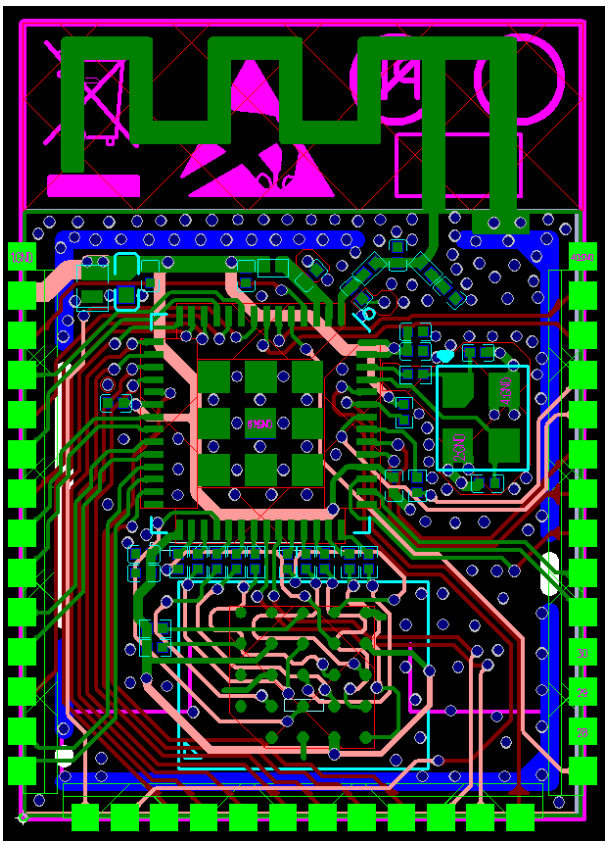

Fig. 1: ESP32-S3 Reference PCB Layout

4.1 General Principles of PCB Layout

It is recommended to use a four-layer PCB design:

- Layer 1 (TOP): Signal traces and components.
- Layer 2 (GND): No signal traces here to ensure a complete GND plane.

- Layer 3 (POWER): GND plane should be applied to better isolate the RF and crystal. Route power traces and a few signal traces on this layer, provided that there is a complete GND plane under the RF and crystal.
- Layer 4 (BOTTOM): Route a few signal traces here. It is not recommended to place any components on this layer.

A two-layer PCB design can also be used:

- Layer 1 (TOP): Signal traces and components.
- Layer 2 (BOTTOM): Do not place any components on this layer and keep traces to a minimum. Please make sure there is a complete GND plane for the chip, RF, and crystal.

4.2 Positioning a Module on a Base Board

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the baseboard on the module's antenna performance should be minimized.

It is suggested to place the module's on-board PCB antenna outside the base board, and the feed point of the antenna closest to the board. In the following example figures, positions with mark ✓ are strongly recommended, while positions without a mark are not recommended.

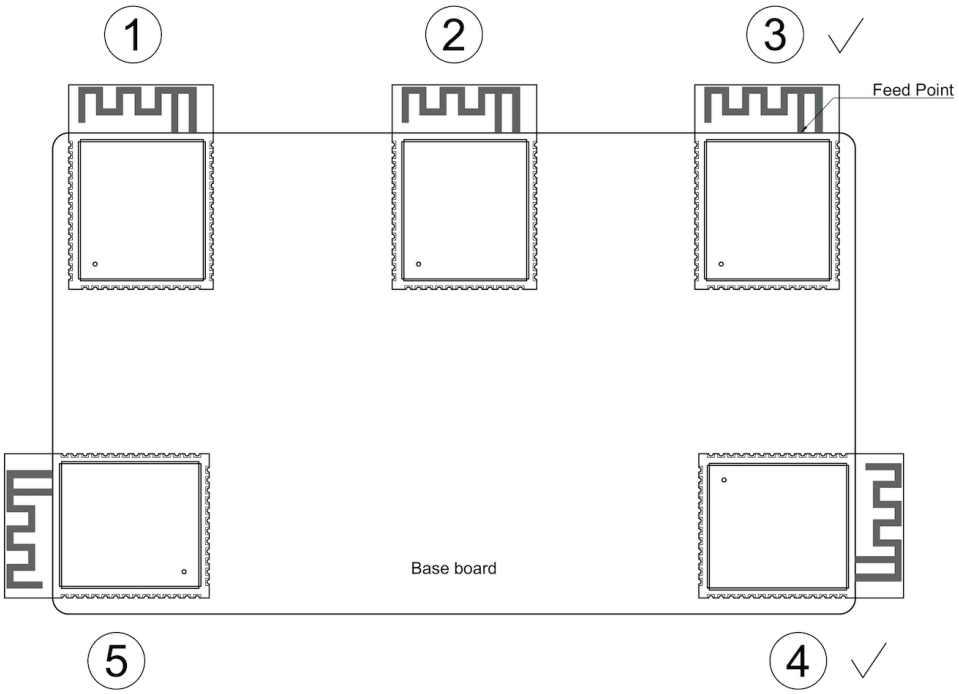

Fig. 2: Placement of ESP32-S3 Modules on Base Board (antenna feed point on the right)

If the PCB antenna cannot be placed outside the board, please ensure a clearance of at least 15 mm around the antenna area (no copper, routing, or components on it), and place the feed point of the antenna closest to the board. If there is a base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna. Figure *Keepout Zone for ESP32-S3 Module's Antenna on the Base Board* shows the suggested clearance for modules whose antenna feed point is on the right.

When designing an end product, attention should be paid to the interference caused by the housing of the antenna and it is recommended to carry out RF verification. It is necessary to test the throughput and communication signal range of the whole product to ensure the product's actual RF performance.

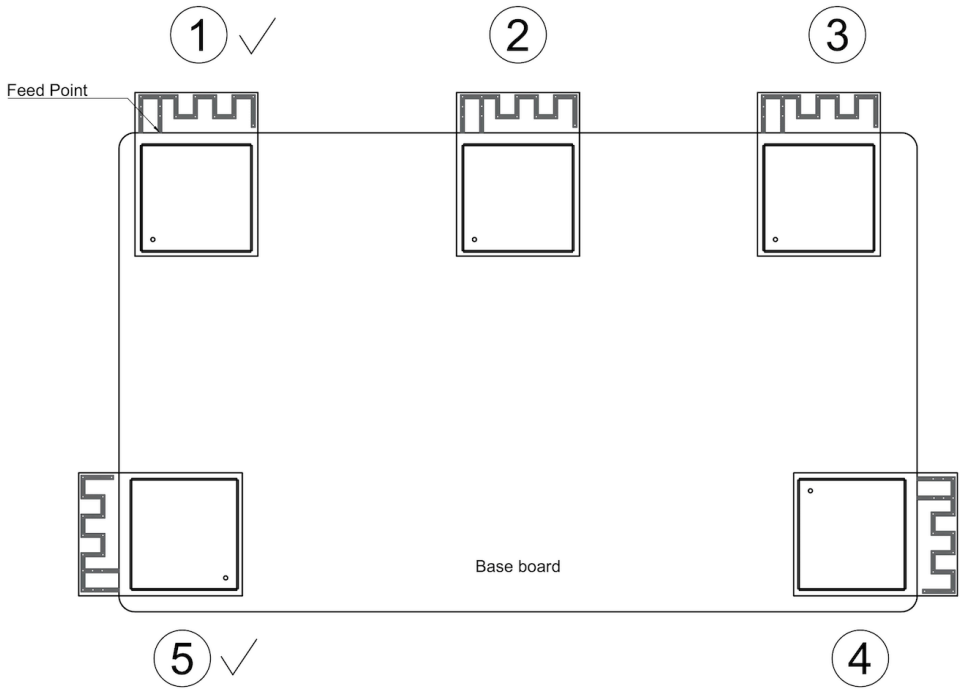

Fig. 3: Placement of ESP32-S3 Modules on Base Board (antenna feed point on the left)

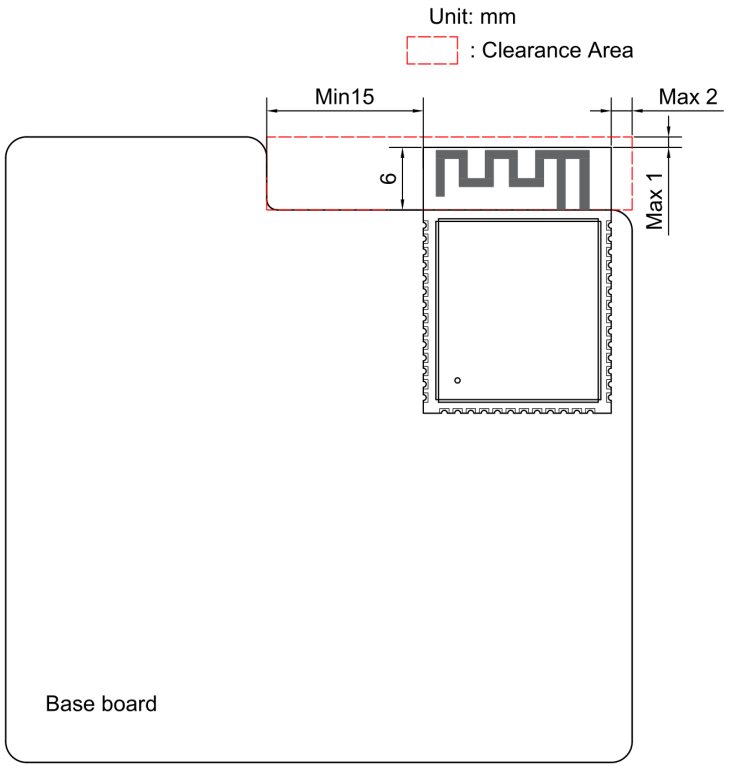

Fig. 4: Keepout Zone for ESP32-S3 Module ' s Antenna on the Base Board

4.3 Power Supply

Figure *ESP32-S3 Power Traces in a Four-layer PCB Design* shows the overview of the power traces in a four-layer PCB design.

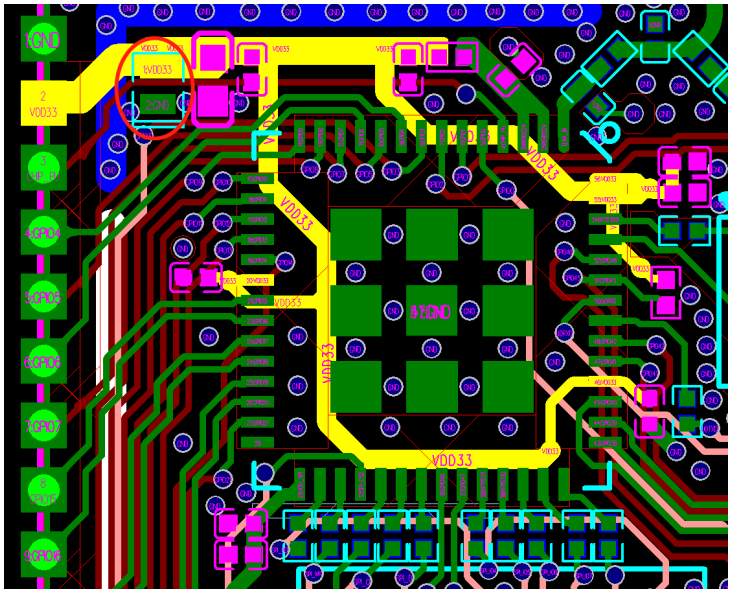

Fig. 5: ESP32-S3 Power Traces in a Four-layer PCB Design

4.3.1 General Guidelines

- Four-layer PCB design is preferred.
- The power traces should be routed on the inner third layer whenever possible.
- Vias are required for the power traces to go through the layers and get connected to the pins on the top layer. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.
- The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias.
- If you need to add a thermal pad EPAD under the chip on the bottom of the module, it is recommended to employ a square grid on the EPAD, cover the gaps with solder paste, and place ground vias in the gaps, as shown in Figure *ESP32-S3 Power Traces in a Four-layer PCB Design*. This can avoid chip displacement caused by tin leakage and bubbles when soldering the module EPAD to the substrate.

4.3.2 3.3 V Power Layout

The 3.3 V power traces, highlighted in yellow, are routed as shown in Figure *ESP32-S3 Power Traces in a Four-layer PCB Design*.

The 3.3 V power layout should meet the following guidelines:

- The ESD protection diode is placed next to the power port (circled in red in Figure *ESP32-S3 Power Traces in a Four-layer PCB Design*). The power trace should have a 10 µF capacitor on its way before entering into the chip, and a 0.1 or 1 µF capacitor could also be used in conjunction. After that, the power traces are divided into several branches using a star-shaped topology, which reduces the coupling between different power pins. Note that all decoupling capacitors should be placed close to the corresponding power pin, and ground vias should be added close to the capacitor's ground pad to ensure a short return path.
- In Figure *ESP32-S3 Power Traces in a Four-layer PCB Design*, the 10 µF capacitor is shared by the analog power supply VDD3P3, and the power entrance since the analog power is close to the chip power entrance.

If the chip power entrance is not near VDD3P3, it is recommended to add a 10 µF capacitor to both the chip power entrance and VDD3P3. Also, reserve two 1 µF capacitors if space permits.

- The width of the main power traces should be no less than 25 mil. The width of VDD3P3 power traces should be no less than 20 mil. The recommended width of other power traces is 10 mil.

4.3.3 Analog Power Layout

Figure *ESP32-S3 Analog Power Traces in a Four-layer PCB Design* shows the analog power layout in a four-layer PCB design.

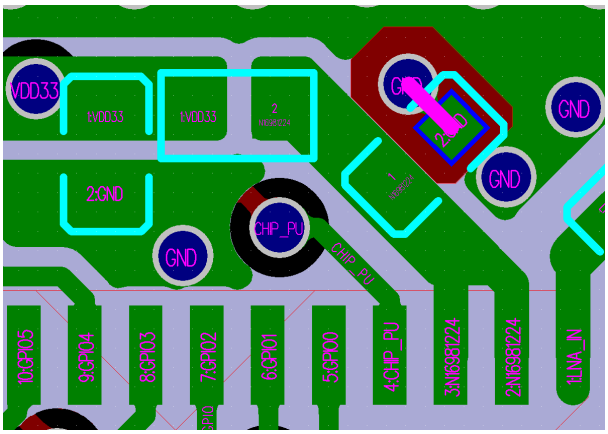

Fig. 6: ESP32-S3 Analog Power Traces in a Four-layer PCB Design

The analog power layout should meet the following guidelines:

- As shown in Figure *ESP32-S3 Analog Power Traces in a Four-layer PCB Design*, it is recommended to connect the capacitor to ground in the CLC filter circuit near VDD3P3 to the fourth layer through a via, and maintain a keep-out area on other layers. The purpose is to further reduce harmonic interference.
- VDD3P3 analog power supply should be surrounded by ground copper. It is required to add GND isolation between VDD3P3, power trace and the surrounding GPIO and RF traces, and place vias whenever possible.

4.4 Crystal

Figure *ESP32-S3 Crystal Layout (with Keep-out Area on Top Layer)* shows a reference PCB layout where the crystal is connected to the ground through vias and a keep-out area is maintained around the crystal on the top layer for ground isolation.

Figure *ESP32-S3 Crystal Layout (without Keep-out Area on Top Layer)* shows the layout for the crystal that is connected to the ground through vias but there is no keep-out area on the top layer for ground isolation.

If there is sufficient ground on the top layer, it is recommended to maintain a keep-out area around the crystal for ground isolation. This helps to reduce the value of parasitic capacitance and suppress temperature conduction, which can otherwise affect the frequency offset.

The layout of the crystal should follow the guidelines below:

- Ensure a complete GND plane for the RF, crystal, and chip.
- The crystal should be placed far from the clock pin to avoid interference on the chip. The gap should be at least 2.0 mm. It is good practice to add high-density ground vias stitching around the clock trace for better isolation.
- There should be no vias for the clock input and output traces, which means the traces cannot cross layers. The clock traces should not intersect with each other.
- Components in series to the crystal trace should be placed close to the chip side.

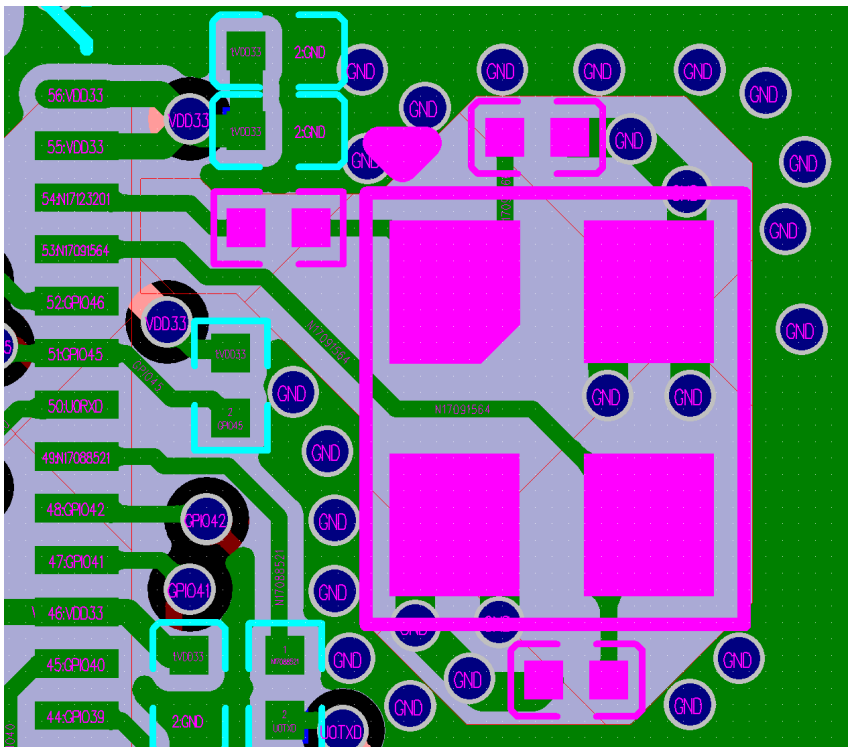

Fig. 7: ESP32-S3 Crystal Layout (with Keep-out Area on Top Layer)

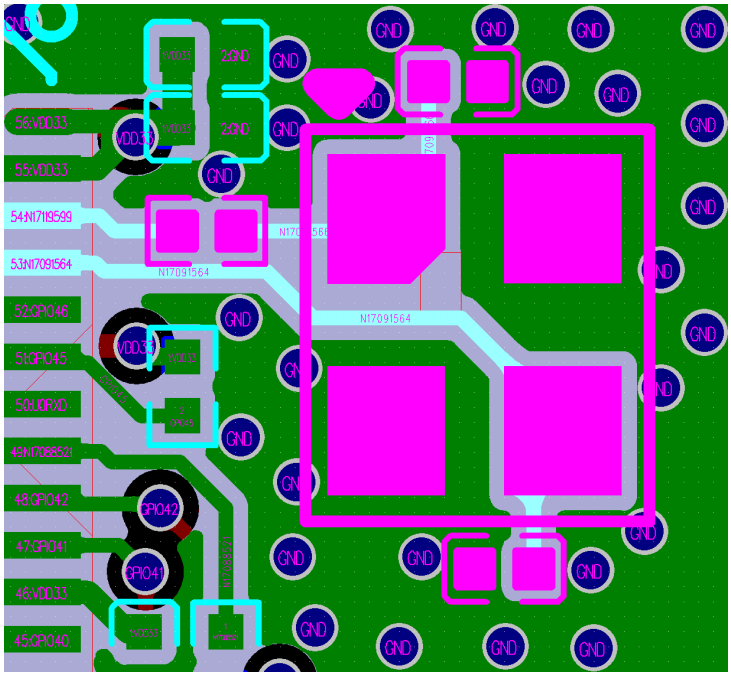

Fig. 8: ESP32-S3 Crystal Layout (without Keep-out Area on Top Layer)

- The external matching capacitors should be placed on the two sides of the crystal, preferably at the end of the clock trace, but not connected directly to the series components. This is to make sure the ground pad of the capacitor is close to that of the crystal.
- Do not route high-frequency digital signal traces under the crystal. It is best not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by grounding copper.
- As the crystal is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal.

4.5 RF

The RF trace is routed as shown highlighted in pink in Figure *ESP32-S3 RF Layout in a Four-layer PCB Design*.

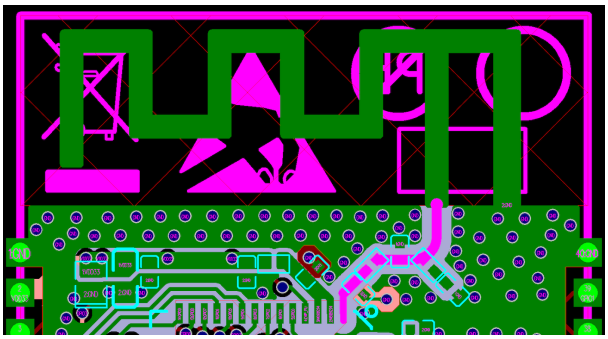

Fig. 9: ESP32-S3 RF Layout in a Four-layer PCB Design

The RF layout should meet the following guidelines:

- A π-type matching circuit should be added to the RF trace and placed close to the chip, in a zigzag.
- The RF trace should have a 50 Ω characteristic impedance. The reference plane is the second layer. For designing the RF trace at 50 Ω impedance, you could refer to the PCB stack-up design shown below.
- Add a stub to the ground at the ground pad of the first matching capacitor to suppress the second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the PCB stack-up so that the characteristic impedance of the stub is 100 Ω ± 10%. In addition, please connect the stub via to the third layer, and maintain a keep-out area on the first and second layers. The trace highlighted in Figure *ESP32-S3 Stub in a Four-layer PCB Design* is the stub. Note that a stub is not required for package types above 0201.
- The RF trace should have a consistent width and not branch out. It should be as short as possible with dense ground vias around for interference shielding.
- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.
- There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR SDRAM, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias.

4.6 Flash and PSRAM

The layout for flash and PSRAM should follow the guidelines below:

Thickness (mm)	Impedance (Ohm)	Gap (mil)	Width (mil)	Gap (mil)
-	50	12.2	12.6	12.2

Stack up	Material	Base copper (oz)	Finished Layer Thickness (mil)	DK
SM			0.4	4
L1_Top	Finished Copper 1 oz	0.33	0.8 (Min)	
PP	7628 TG150 RC50%		8	4.39
L2_Gnd		1	1.2	
Core	Core		Adjustable	4.43
L3_Power		1	1.2	
PP	7628 TG150 RC50%		8	4.39
L4_Bottom	Finished Copper 1 oz	0.33	0.8 (Min)	
SM			0.4	4

Fig. 10: ESP32-S3 PCB Stack-up Design

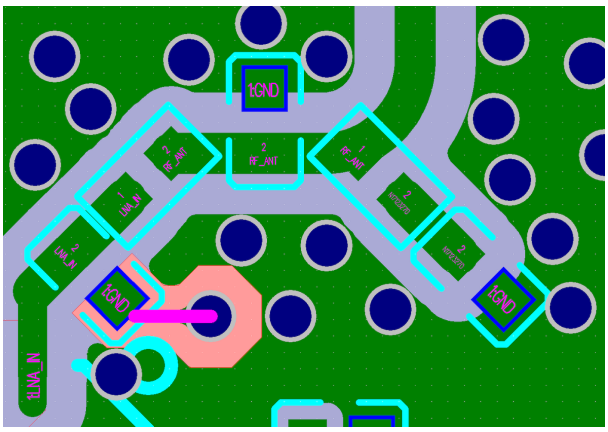

Fig. 11: ESP32-S3 Stub in a Four-layer PCB Design

- Place the zero-ohm series resistors on the SPI lines close to the chip.
- Route the SPI traces on the inner layer (e.g., the third layer) whenever possible, and add ground copper and ground vias around the clock and data traces of SPI separately.
- Place the 0.1 µF capacitor to ground at the VDD_SPI close to corresponding flash and PSRAM power pins.
- Octal SPI traces should have matching lengths.

Figure *ESP32-S3 Quad SPI Flash Layout* shows the quad SPI flash layout.

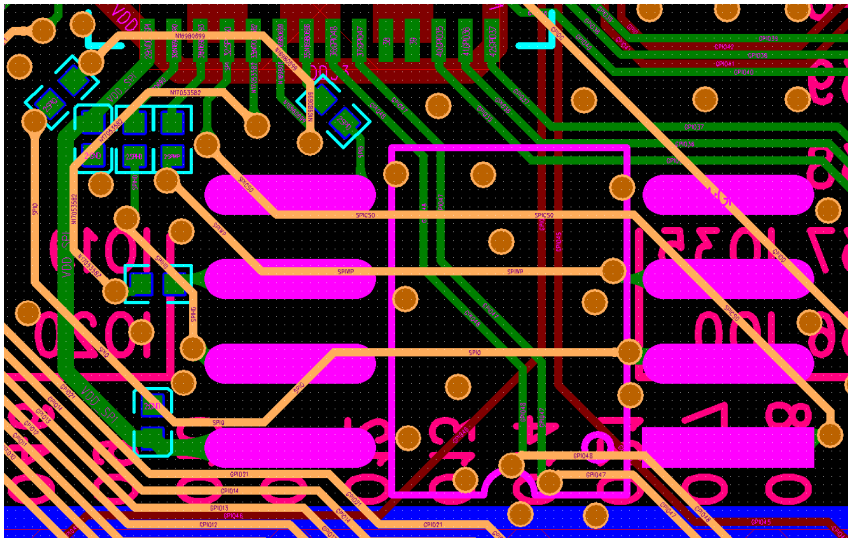

Fig. 12: ESP32-S3 Quad SPI Flash Layout

Figure *ESP32-S3 Octal SPI Flash Layout* shows the octal SPI flash layout.

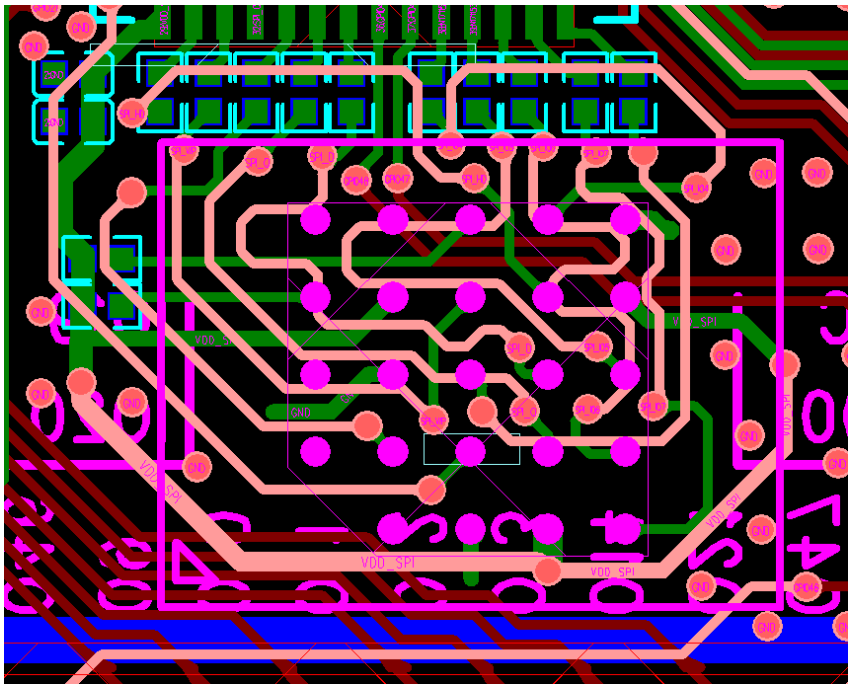

Fig. 13: ESP32-S3 Octal SPI Flash Layout

4.7 UART

Figure *ESP32-S3 UART Layout* shows the UART layout.

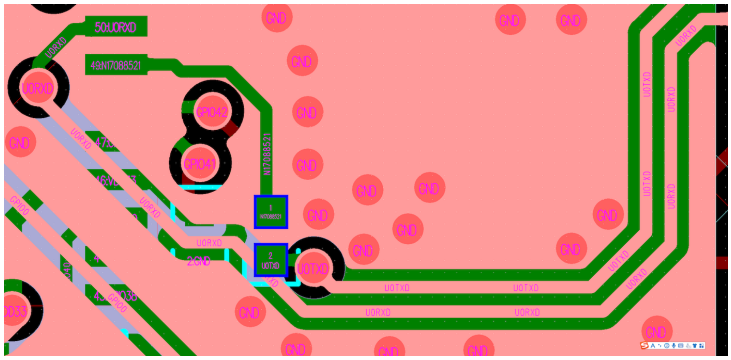

Fig. 14: ESP32-S3 UART Layout

The UART layout should meet the following guidelines:

- The series resistor on the U0TXD trace needs to be placed close to the chip side and away from the crystal.
- The U0TXD and U0RXD traces on the top layer should be as short as possible.
- The UART trace should be surrounded by ground copper and ground vias stitching.

4.8 USB

The USB layout should meet the following guidelines:

- Place the RC circuit on the USB traces close to the chip side.
- Use differential pairs and route them in parallel at equal lengths.
- Make sure there is a complete reference ground plane and surround the USB traces with ground copper.

4.9 SDIO

The SDIO layout should follow the guidelines below:

- Since SDIO traces have a high speed, it is necessary to control the parasitic capacitance.
- The trace length for SDIO_CMD and SDIO_DATA0 ~ SDIO_DATA3 should be 3 mil longer or shorter than the trace length for SDIO_CLK. If necessary, use serpentine routing.
- It is better to surround the SDIO_CLK trace with ground copper. The path from SDIO GPIOs to the master SDIO interface should be as short as possible and no more than 2500 mil or even 2000 mil.
- Do not place SDIO traces across planes.

4.10 Touch Sensor

ESP32-S3 offers up to 14 capacitive IOs that detect changes in capacitance on touch sensors due to finger contact or proximity. The chip's internal capacitance detection circuit features low noise and high sensitivity. It allows to use touch pads with smaller area to implement the touch detection function. You can also use the touch panel array to detect a larger area or more test points.

Figure *ESP32-S3 Typical Touch Sensor Application* depicts a typical touch sensor application.

To prevent capacitive coupling and other electrical interference to the sensitivity of the touch sensor system, the following factors should be taken into account.

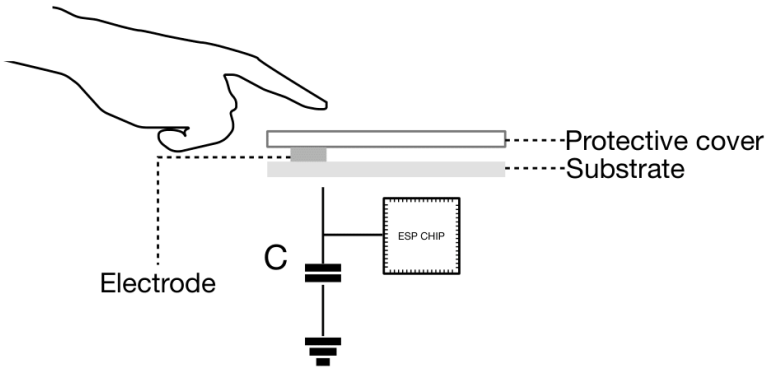

Fig. 15: ESP32-S3 Typical Touch Sensor Application

4.10.1 Electrode Pattern

The proper size and shape of an electrode improves system sensitivity. Round, oval, or shapes similar to a human fingertip are commonly applied. Large size or irregular shape might lead to incorrect responses from nearby electrodes.

Figure *ESP32-S3 Electrode Pattern Requirements* shows the proper and improper size or shape of electrode. Please note that the examples illustrated in the figure are not of actual scale. It is suggested to use a human fingertip as reference.

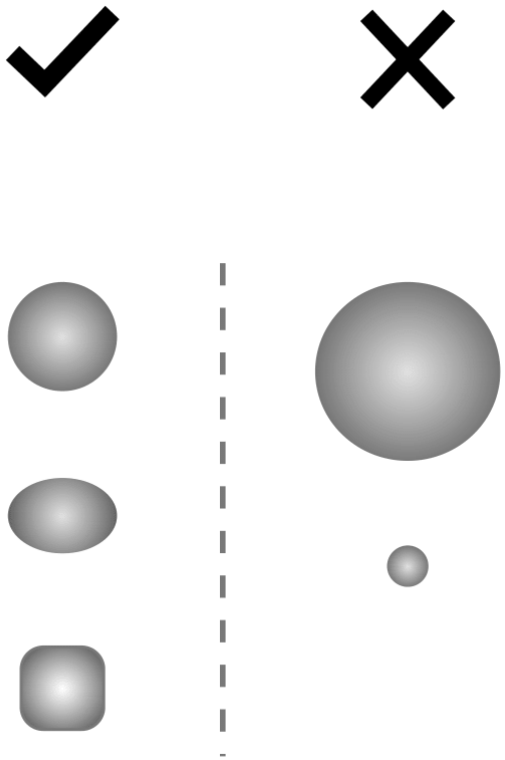

Fig. 16: ESP32-S3 Electrode Pattern Requirements

4.10.2 PCB Layout

Figure *ESP32-S3 Sensor Track Routing Requirements* illustrates the general guidelines to routing traces. Specifically,

- The trace should be as short as possible and no longer than 300 mm.
- The trace width (W) can not be larger than 0.18 mm (7 mil).
- The alignment angle (R) should not be less than 90°.
- The trace-to-ground gap (S) should be in the range of 0.5 mm to 1 mm.
- The electrode diameter (D) should be in the range of 8 mm to 15 mm.
- Hatched ground should be added around the electrodes and traces.
- The traces should be isolated well and routed away from that of the antenna.

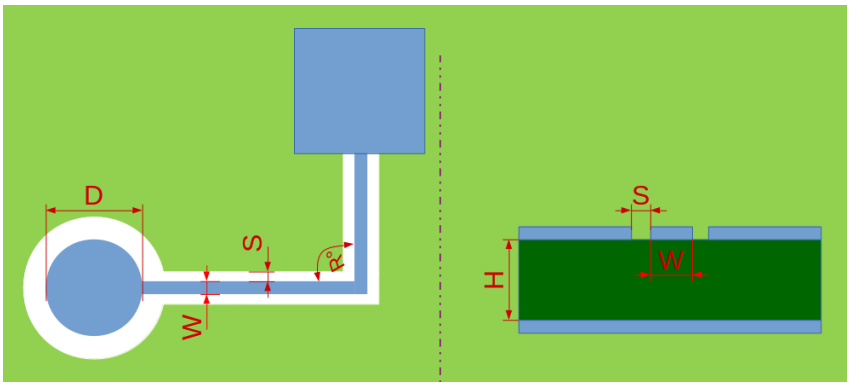

Fig. 17: ESP32-S3 Sensor Track Routing Requirements

Note: For more details on the hardware design of the touch sensor, please refer to Touch Sensor Application Note.

4.10.3 Waterproof and Proximity Sensing Design

ESP32-S3 touch sensor has a waterproof design and features proximity sensor function. Figure *ESP32-S3 Waterproof and Proximity Sensing Design* shows an example layout of a waterproof and proximity sensing design.

Note the following guidelines to better implement the waterproof and proximity sensing design:

- The recommended width of the shield electrode width is 2 cm.
- Employ a grid on the top layer with a trace width of 7 mil and a grid width of 45 mil (25% fill). The filled grid is connected to the driver shield signal.
- Employ a grid on the bottom layer with a trace width of 7 mil and a grid width of 70 mil (17% fill). The filled grid is connected to the driver shield signal.
- The protective sensor should be in a rectangle shape with curved edges and surround all other sensors.
- The recommended width of the protective sensor is 2 mm.
- The recommended gap between the protective sensor and shield sensor is 1 mm.
- The sensing distance of the proximity sensor is directly proportional to the area of the proximity sensor. However, increasing the sensing area will introduce more noise. Actual testing is needed for optimized performance.
- It is recommended that the shape of the proximity sensor is a closed loop. The recommended width is 1.5 mm.

4.11 Typical Layout Problems and Solutions

4.11.1 1. The voltage ripple is not large, but the TX performance of RF is rather poor.

Analysis: The voltage ripple has a strong impact on the RF TX performance. It should be noted that the ripple must be tested when ESP32-S3 is in the normal working mode. The ripple increases when the power gets high in a different mode.

Generally, the peak-to-peak value of the ripple should be <80 mV when ESP32-S3 sends MCS7@11n packets, and <120 mV when ESP32-S3 sends 11 MHz@11b packets.

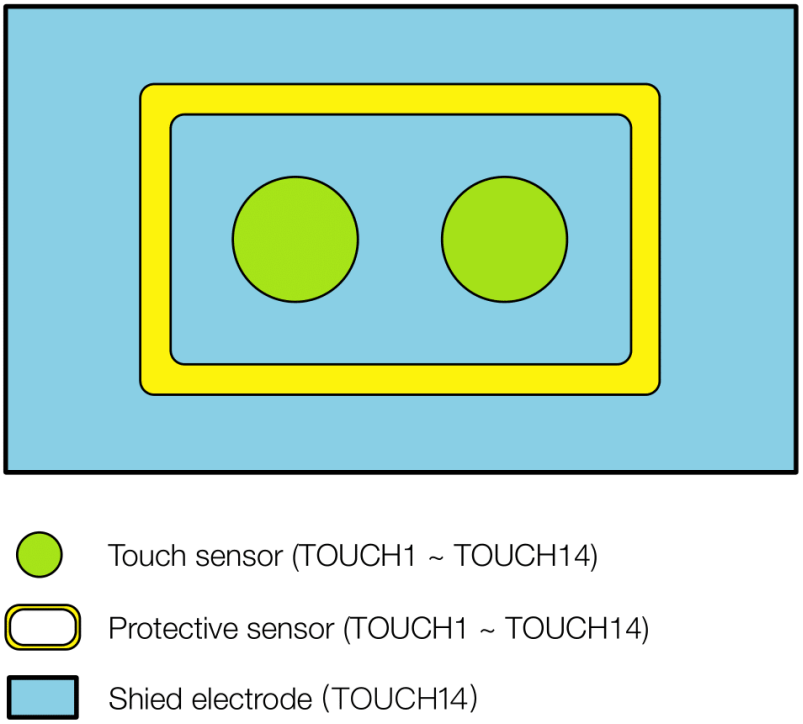

Fig. 18: ESP32-S3 Waterproof and Proximity Sensing Design

Solution: Add a 10 µF filter capacitor to the branch of the power trace (the branch powering the chip's analog power pin). The 10 µF capacitor should be as close to the analog power pin as possible for small and stable voltage ripples.

4.11.2 2. When ESP32-S3 sends data packages, the voltage ripple is small, but RF TX performance is poor.

Analysis: The RF TX performance can be affected not only by voltage ripples, but also by the crystal itself. Poor quality and big frequency offsets of the crystal decrease the RF TX performance. The crystal clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces, such as the SDIO traces and UART traces under the crystal, could also result in the malfunction of the crystal. Besides, sensitive components or radiating components, such as inductors and antennas, may also decrease the RF performance.

Solution: This problem is caused by improper layout for the crystal and can be solved by re-layout. Please refer to Section *Crystal* for details.

4.11.3 3. When ESP32-S3 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis: The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution: Match the antenna's impedance with the π-type circuit on the RF trace, so that the impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.

4.11.4 4. TX performance is not bad, but the RX sensitivity is low.

Analysis: Good TX performance indicates proper RF impedance matching. Poor RX sensitivity may result from external coupling to the antenna. For instance, the crystal signal harmonics could couple to the antenna. If the TX and RX traces of UART cross over with RF trace, they will affect the RX performance, as well. If there are many high-frequency interference sources on the board, signal integrity should be considered.

Solution: Keep the antenna away from crystals. Do not route high-frequency signal traces close to the RF trace. Please refer to Section *RF* for details.

Chapter 5

Hardware Development

5.1 ESP32-S3 Modules

For a list of ESP32-S3 modules please check the Modules section on Espressif's official website.

To review module reference designs please check the Documentation section on Espressif's official website.

5.2 ESP32-S3 Development Boards

For a list of the latest designs of ESP32-S3 boards please check the Development Boards section on Espressif's official website.

5.3 Download Guidelines

You can download firmware to ESP32-S3 via UART and USB.

To download via UART:

1. Before the download, make sure to set the chip or module to Joint Download Boot mode, according to Table *Boot Mode Control*.
2. Power up the chip or module and check the log via the UART0 serial port. If the log shows "waiting for download", the chip or module has entered Joint Download Boot mode.
3. Download your firmware into flash via UART using the Flash Download Tool.
4. After the firmware has been downloaded, pull GPIO0 high or leave it floating to make sure that the chip or module enters SPI Boot mode.
5. Power up the chip or module again. The chip will read and execute the new firmware during initialization.

To download via USB:

1. If the flash is empty, set the chip or module to Joint Download Boot mode, according to Table *Boot Mode Control*.
2. Power up the chip or module and check the log via USB serial port. If the log shows "waiting for download", the chip or module has entered Joint Download Boot mode.
3. Download your firmware into flash via USB using Flash Download Tool.
4. After the firmware has been downloaded, pull GPIO0 high or leave it floating to make sure that the chip or module enters SPI Boot mode.
5. Power up the chip or module again. The chip will read and execute the new firmware during initialization.
6. If the flash is not empty, start directly from Step 3.

Note:

- It is advised to download the firmware only after the "waiting for download" log shows via serial ports.
- Serial tools cannot be used simultaneously with the Flash Download Tool on one com port.
- The USB auto-download will be disabled if the following conditions occur in the application, where it will be necessary to set the chip or module to Joint Download Boot mode first by configuring the strapping pin.
  - USB PHY is disabled by the application;
  - USB is secondary developed for other USB functions, e.g., USB host, USB standard device;
  - USB IOs are configured to other peripherals, such as UART and LEDC.
- It is recommended that the user retains control of the strapping pins to avoid the USB download function not being available in case of the above scenario.

Chapter 6

Related Documentation and Resources

- Chip Datasheet (PDF)
- Technical Reference Manual (PDF)
- Chip Errata (PDF)
- Chip Variants
- Modules
- Development Boards
- Espressif KiCad Library
- ESP Product Selector
- Regulatory Certificates
- User Forum (Hardware)
- Technical Support

Chapter 7

Glossary

The glossary contains terms and acronyms that are used in this document.

Term	Description
CLC	Capacitor-Inductor-Capacitor
DDR SDRAM	Double Data Rate Synchronous Dynamic Random-Access Memory
ESD	Electrostatic Discharge
LC	Inductor-Capacitor
PA	Power Amplifier
RC	Resistor-Capacitor
RTC	Real-Time Clock
Zero-ohm resistor	A zero-ohm resistor is a placeholder on the circuit so that another higher ohm resistor can replace it, depending on design cases.

Chapter 8

Revision History

8.1 ESP Hardware Design Guidelines v1.0

This is the first version of the ESP Hardware Design Guidelines in HTML format. During the migration from PDF to HTML format, minor updates, improvements, and clarifications were made throughout the documentation.

If you would like to check previous versions of the document, please submit documentation feedback.

Chapter 9

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