IC TRAINING CENTER VIETNAM

FINAL PROJECT

TIMER 64 BIT

Prepared by:

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CHAPTER 1: DESIGN SPECIFICATION

1. Timer Features

- 64 bit count-up.
- Address space: 4KB (0x4000_1000 – 0x4000_1FFF).
- Register set is configured via APB bus (IP is APB slave).
- APB 32 bit transfer:
    - Support wait state (1 cycle) and error handling.
    - Support byte access.
    - Support halt (stop) in debug mode.
- System clock frequency is 200 MHz. Timer uses active low async reset.
- Counters can be counted based on the system clock or divided up to 256.
- Support timer interrupt (can be enabled or disabled).

2. Detail Functional Description

a. Counter

- 64 bit count-up.
- Counting mode:
    - Default mode: Counter's speed is the same as the system clock.
    - Control mode: When enabled by writing 1 to TCR.div_en bit, the counter's speed is determined by the divisor value set in TCR.div_val
- Counter continues counting when interrupts occur.
- Counter continues counting when overflow occurs.
- [Standard only]: When timer_en is H->L, the counter needs to be initialized by software. When timer_en is L->H again, the timer can work normally.
- [Advanced] Support halted mode described in next page.
- [Advanced] When timer_en changes from High to Low, the counter is cleared to its initial value. When timer_en is L->H again, the timer can work normally.
- Note: The div_en and div_val are not related to frequency divisor (clock divider). Those settings only control the counter when to count.

b. Halted

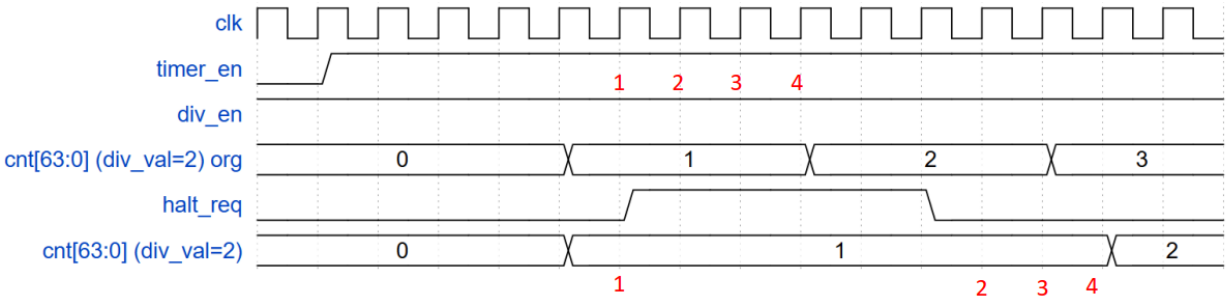
- Counter can be halted (stopped) in debug mode when both below conditions occur:

- Input debug_mode signal is High.
- THCR.halt_req is 1.

– THCSR.halt_ack is 1 after a halt request indicates that the request is accepted.

– After halted, the counter can be resumed to count normally when clearing the halt request to 0.

– The period of each counting number needs to be the same when halt and not halt as described in the below waveform example (div_val=2).



c. Timer Interrupt

– Timer interrupt (tim_int) is asserted (set) when interrupt is enabled and the counter's value matches (equal) the compare value.

– Once asserted, the timer interrupt (tim_int) remains unchanged until it is cleared by writing 1 to TISR.int_st bit or the interrupt is disabled.

d. Counting mode

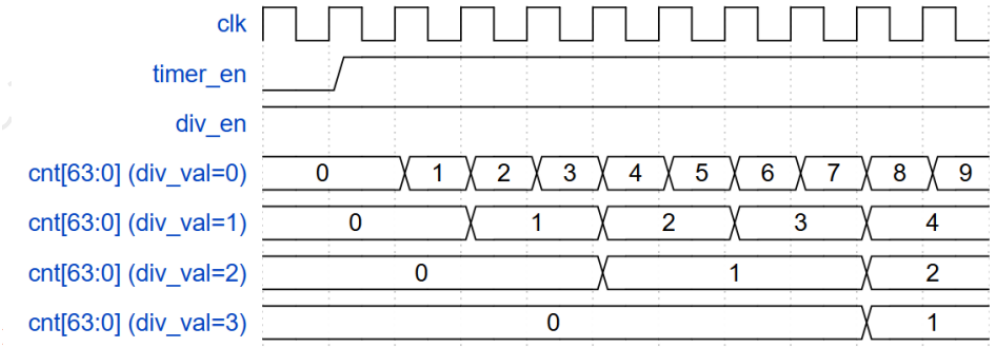
– In default mode, counting speed depends on the system clock (same as div_val=0 case as below waveform).

– The counting's speed can be controlled by register settings by setting into TCR.div_en and TCR.div_val[3:0] as the register specification.

– div_en and div_val can not be changed while timer_en is High.

- Standard level: Testbench should not change div_en and div_val.
- Advanced level: Not allowed to change div_en and div_val while timer_en is High by an error response when user mistakenly accesses.

Example waveform of counter if control mode



e. APB Slave/ Register

- Address space: 4KB (0x4000_1000 – 0x4000_1FFF)
- Read/Write to reserved area is RAZ/WI (read as zero, write ignored)
- System clock frequency is 200 MHz.
- Standard level:
  - Only support APB 32-bit transfer
  - No wait states and no error handling
- Advanced level:
  - Support byte access: Bus can access individual bytes in the register.
  - Support wait state (1 cycle) to improve the timing.
  - Support error handling for some prohibited access:
    - write prohibited value to TCR.div_val
    - div_en or div_val changes during timer is operating
- When error occurs, data is not written into register bit/fields

3. Register Specification

a. Register summary

Base address: 0x4000_1000

Offset	Abbreviation	Register name
0x00	TCR	Timer Control Register
0x04	TDR0	Timer Data Register 0
0x08	TDR1	Timer Data Register 1
0x0C	TCMP0	Timer Compare Register 0
0x10	TCMP1	Timer Compare Register 1
0x14	TIER	Timer Interrupt Enable Register
0x18	TISR	Timer Interrupt Status Register
0x1C	THCSR	Timer Halt Control Status Register

Others	Reserved	

b. Timer Control Register (TCR)

Bit	Name	Type	Default value	Description
31:12	Reserved	-	20'h0	Reserved
11:8	div_val	RW	4'b0001	Counter control mode setting: • 4'b0000: Counting speed is not divided • 4'b0001: Counting speed is divided by 2 (default) • 4'b0010: Counting speed is divided by 4 • 4'b0011: Counting speed is divided by 8 • 4'b0100: Counting speed is divided by 16 • 4'b0101: Counting speed is divided by 32 • 4'b0110: Counting speed is divided by 64 • 4'b0111: Counting speed is divided by 128 • 4'b1000: Counting speed is divided by 256 • Others: Reserved, (*) prohibit settings. When setting the prohibit value, div_val is not changed. Note: User must not change div_en while timer_en is High (*): Add hardware logic to ensure div_val is prohibited to change when timer_en is High. Access is error response in this case. (*) Access is "error response" when setting prohibit value to div_val
7:2	Reserved	RO	6'b0	Reserved
1	div_en	RW	1'b0	Counter control mode enable. • 0: Disabled. Counter counts with normal speed based on system clock • 1: Enabled. The counting speed of counter is controlled based on div_val Note: User must not change div_en while timer_en is High (*): Add hardware logic to ensure div_en is prohibited to change when timer_en is High. Access is error response in this case.
0	timer_en	RW	1'b0	Timer enable • 0: Disabled. Counter does not count. • 1: Enabled. Counter starts counting. (*) timer_en changes from H->L will initialize the TDR0/1 to their initial value

c. Timer Data Register 0 (TDR0)

Bit	Name	Type	Default value	Description
31:0	TDR0	RW	32'h0000_0000	Lower 32-bit of 64-bit counter. Value of this register is cleared to initial value when timer_en changes from H->L.

d. Timer Data Register 1 (TDR1)

Bit	Name	Type	Default value	Description
31:0	TDR1	RW	32'h0000_0000	Upper 32-bit of 64-bit counter. Value of this register is cleared to initial value when timer_en changes from H->L.

e. Timer Compare Register 0 (TCMP0)

Bit	Name	Type	Default value	Description
31:0	TCMP0	RW	32'hFFFF_FFFF	Lower 32-bit of 64-bit compare value. Interrupt is asserted when counter value is equal to compare value

f. Timer Compare Register 1 (TCMP1)

Bit	Name	Type	Default value	Description
31:0	TCMP1	RW	32'hFFFF_FFFF	Upper 32-bit of 64-bit compare value. Interrupt is asserted when counter value is equal to compare value

g. Timer Interrupt Enable Register (TIER)

Bit	Name	Type	Default value	Description
31:1	Reserved	RO	31'h0	Reserved
0	int_en	R/W	1'b0	Timer interrupt enable 0: Timer interrupt is disabled. 1: Timer interrupt is enabled. When this bit is 0, no timer interrupt is output. When this bit is 1, timer interrupt can be output when reaching trigger condition. Clearing this bit to 0 while interrupt is asserting will mask the interrupt to 0 but

				does not affect the interrupt pending bit TISR.int_st bit

h. Timer Interrupt Status Register (TISR)

Bit	Name	Type	Default value	Description
31:1	Reserved	RO	31'h0	Reserved
0	int_st	RW1C	1'b0	Timer interrupt trigger condition status bit (interrupt pending bit) 0: The interrupt trigger condition does not occur. 1: The interrupt trigger condition occurred. Write 1 when this bit is 1 to clear it Write 0 when this bit is 1 has no effect Write to this bit when it is 0 has no effect. Note: When interrupt trigger condition occurred (counter reached compare value), counter continues to count normally

i. Timer Halt Control Status Register (THCSR)

Bit	Name	Type	Default value	Description
31:2	Reserved	RO	30'h0	Reserved
1	halt_ack	RO	1'b0	Timer halt acknowledge 0: Timer is NOT halted 1: Timer is halted Timer accepts the halt request only in debug mode, indicates by debug_mode input signal
0	halt_req	RW	1'b0	Timer halt request 0: No halt req. 1: Timer is requested to halt.

CHAPTER 2: RTL DESIGN

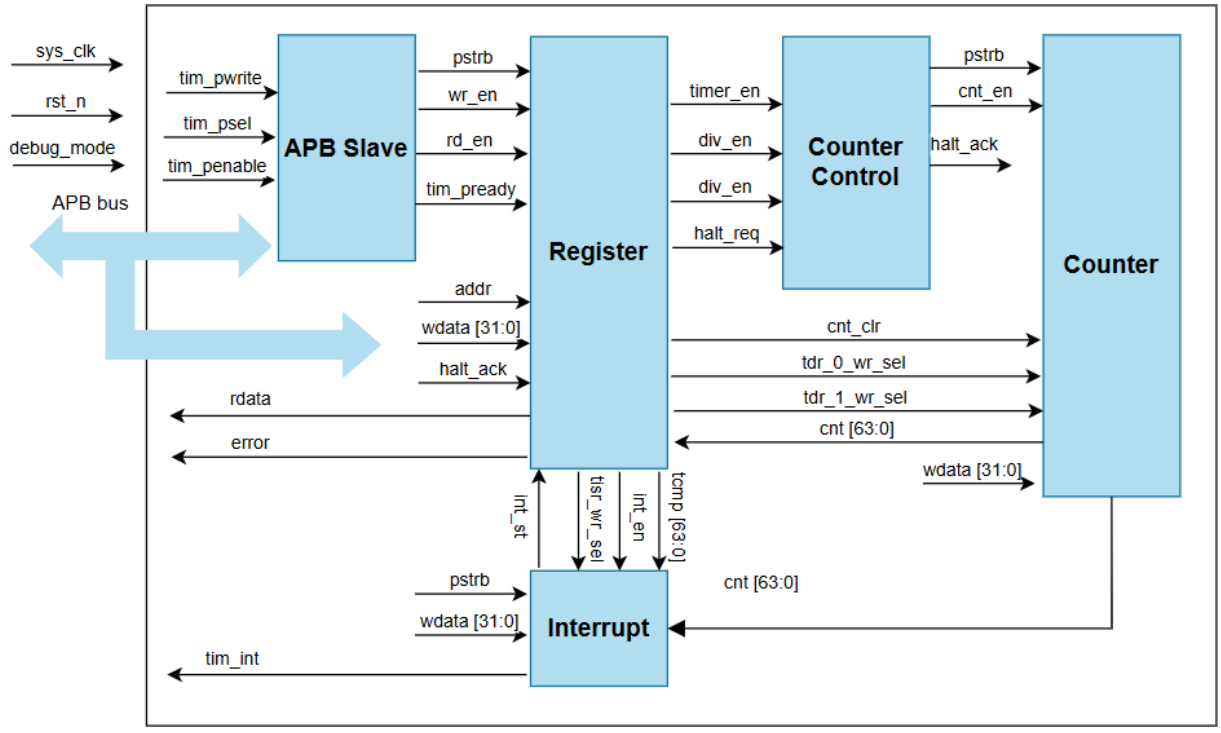
1. IO Port List

Top module name: master_apb

Signal name	Width	Direction	Description
sys_clk	1	Input	Input clock
sys_rst_n	1	Input	Active low asynchronous reset 0: Counter is in reset state 1: Counter is in non_reset state
tim_psel	1	Input	Select signal 0: Not selected 1: Selected
tim_pwrite	1	Input	Write/Read request 1: Write request 0: Read request
tim_penable	1	Input	Enable signal 0: Disabled 1: Enabled
tim_paddr[11:0]	12	Input	Address signal 12 bit address of register for read/write access
tim_pwdata[31:0]	32	Input	32 bit write data
tim_prdata[31:0]	32	Output	32 bit read data
tim_pstrb[3:0]	4	Input	Byte select signal for write operations. 0: Data not valid 1: Data valid
tim_pready	1	Output	Ready signal 0: Timer is not ready, transaction still in progress 1: Timer is ready, transaction can be completed
tim_pslverr	1	Output	Error signal for the transfer 0: No error, transaction successful 1: Error occurred during the transaction
tim_int	1	Output	Interrupt signal

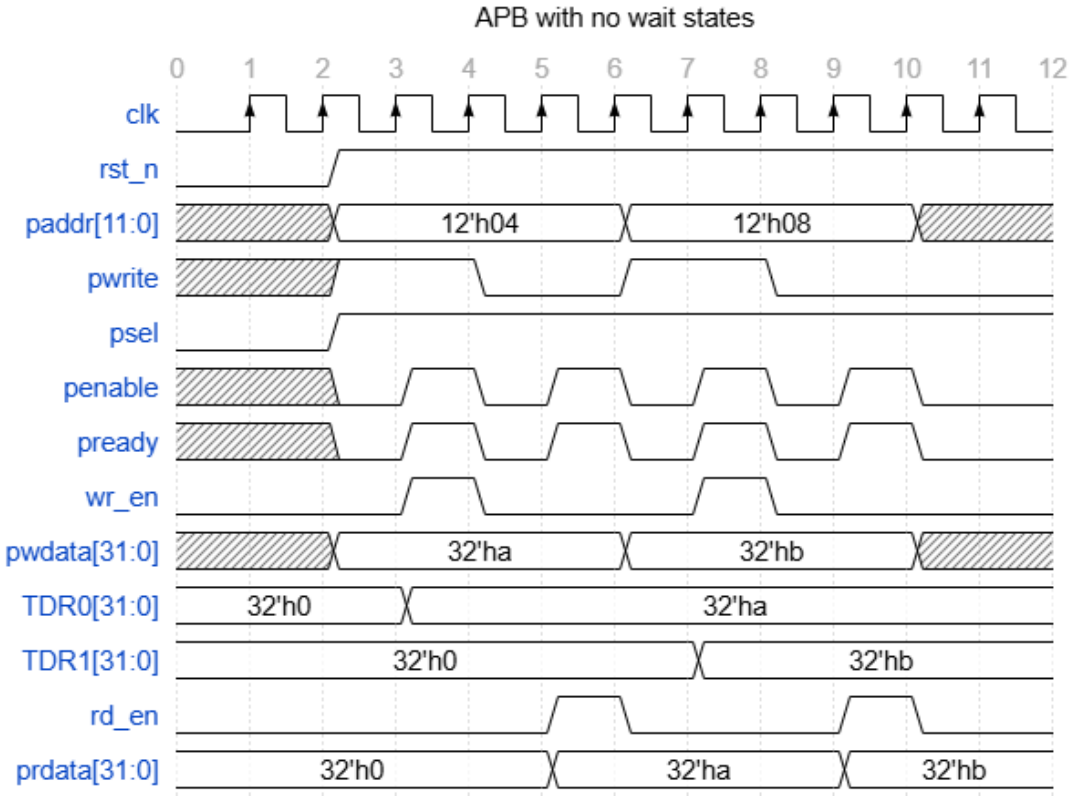
			• 0: Interrupt is disabled or counter value doesn't match the compare value • 1: Interrupt is enabled, counter value matches the compare value
dbg_mode	1	Input	For simple, dbg_mode does not change after timer_en is High

2. Block Diagram

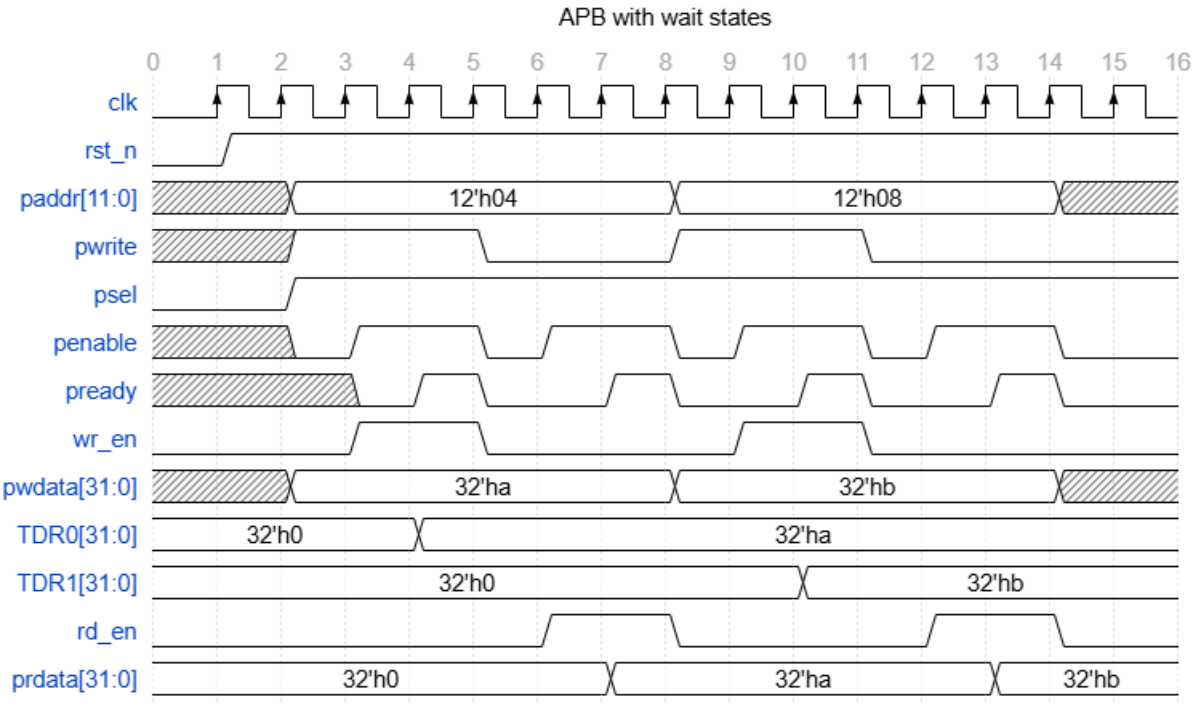


3. Timing Diagram

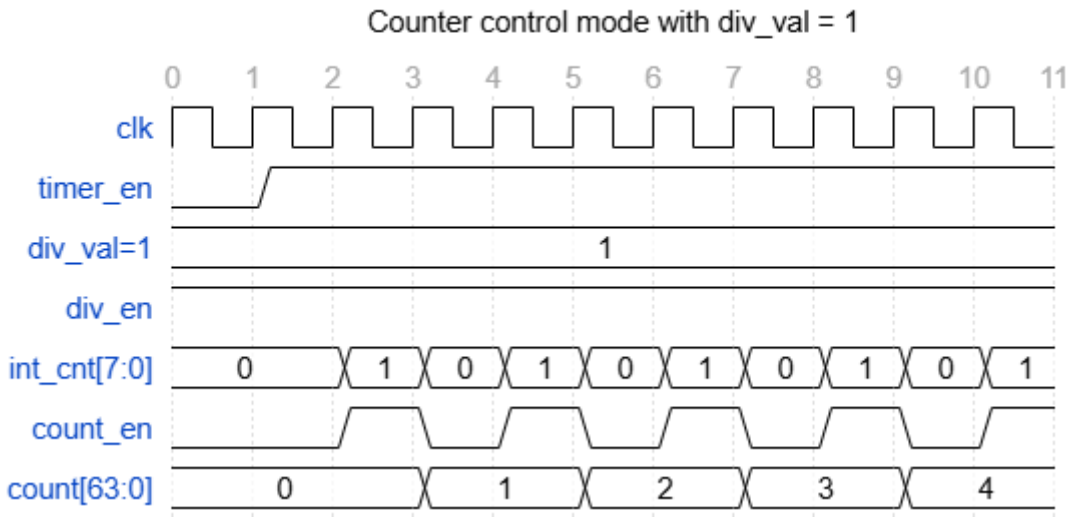
APB transfer with no wait states



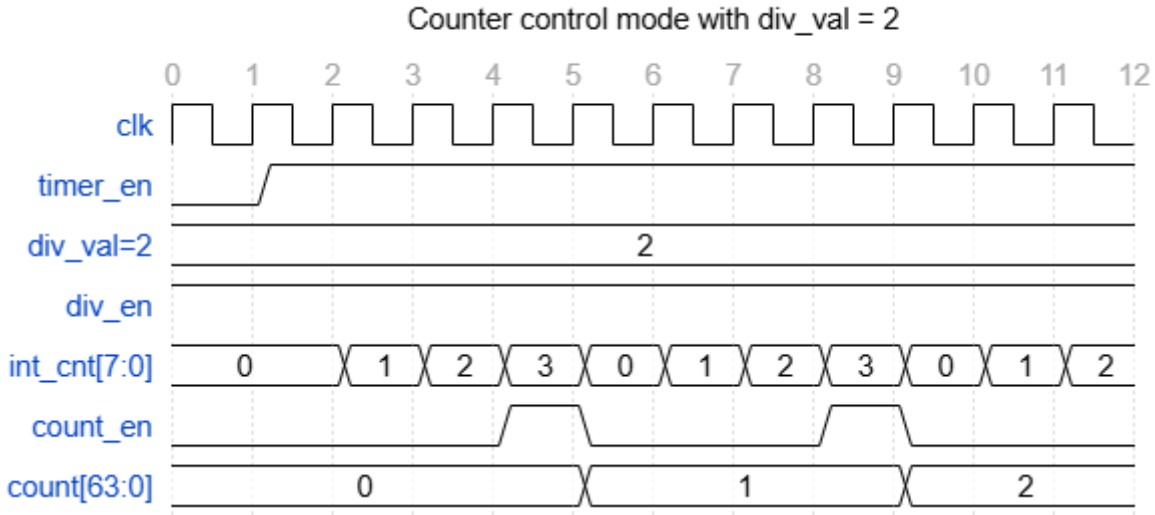
APB transfer with wait states



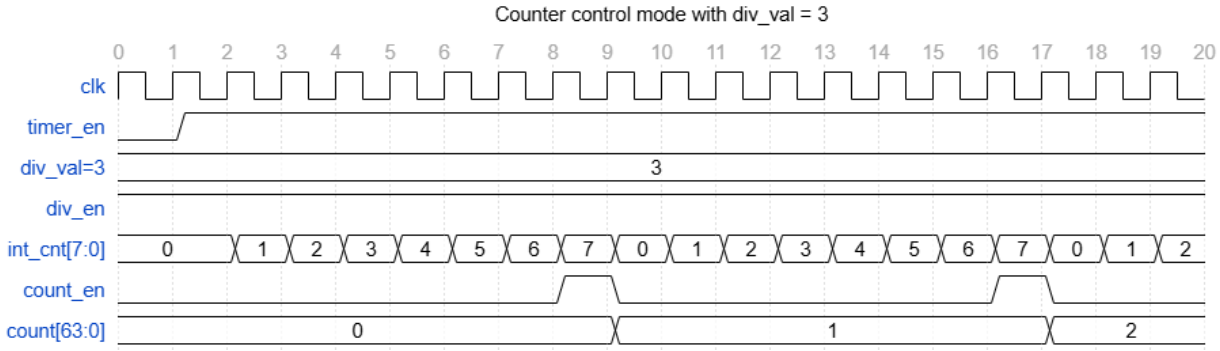
Counter control mode with div_val = 1



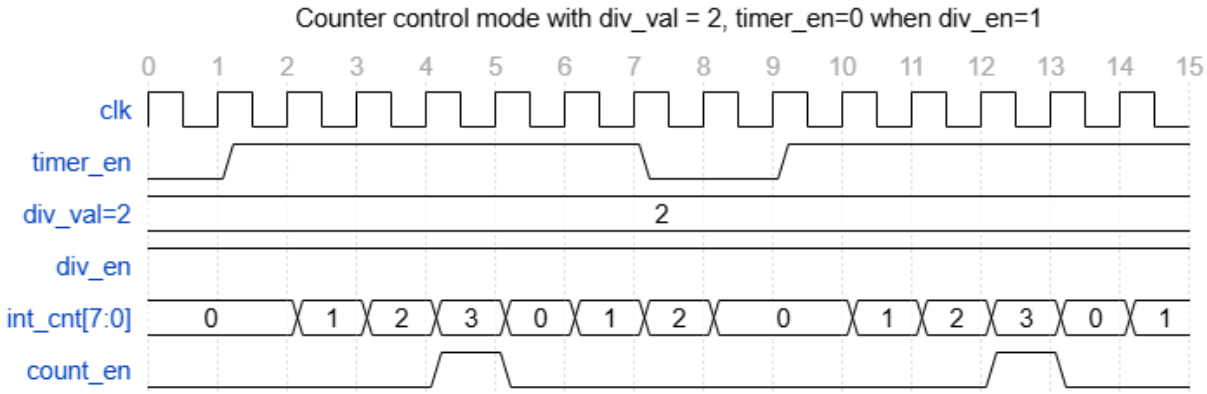
Counter control mode with div_val = 2



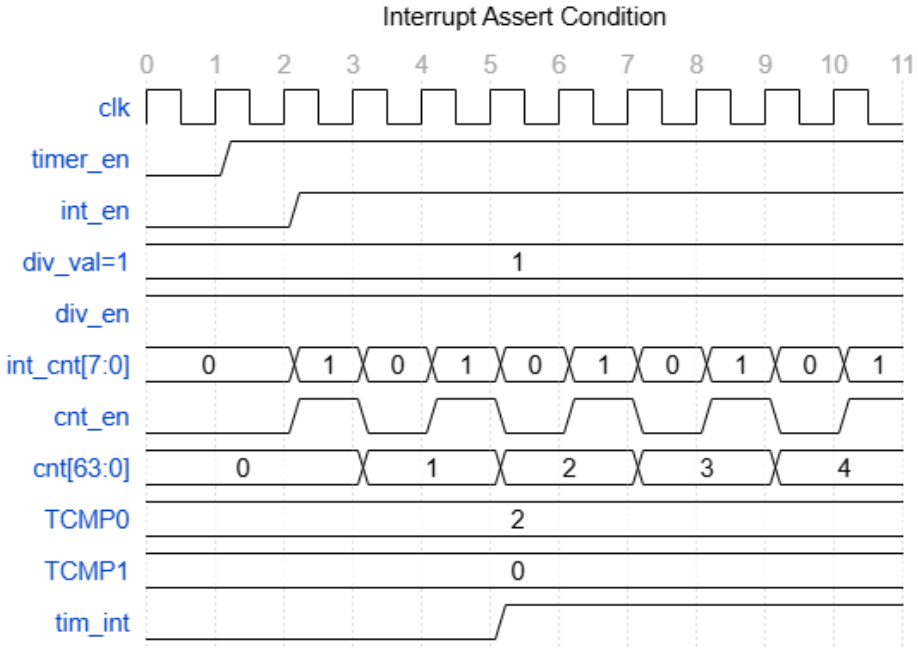
Counter control mode with div_val = 3



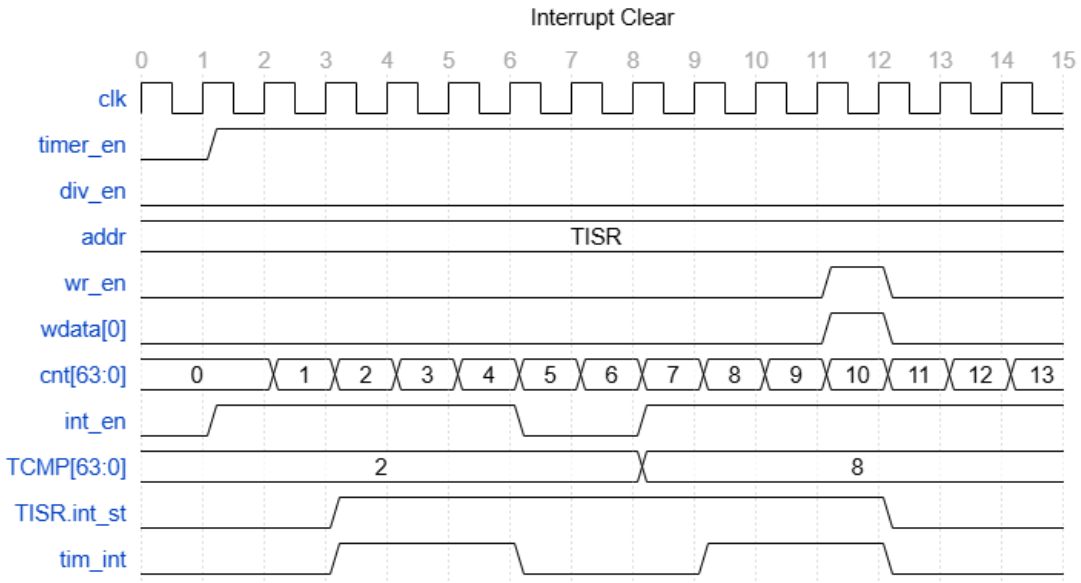
Counter control mode with div_val = 2, timer_en=0 when div_en=1



Interrupt Assert Condition

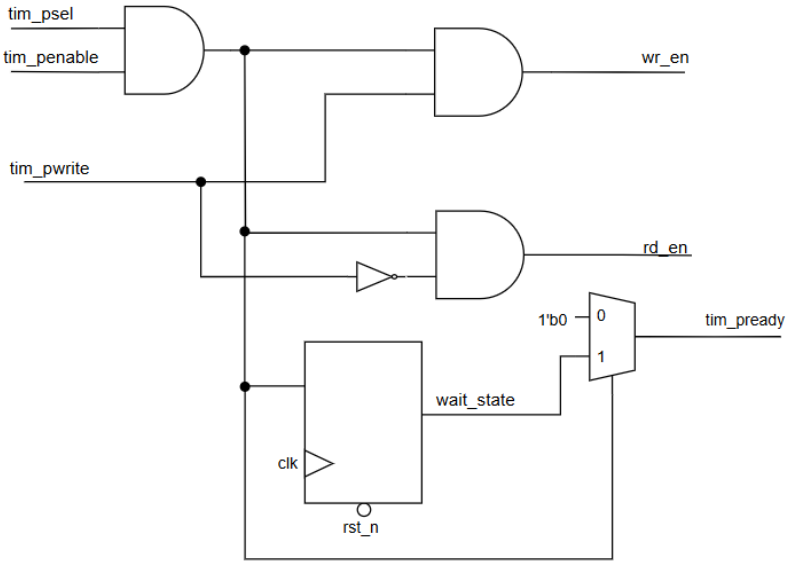


Interrupt Clear

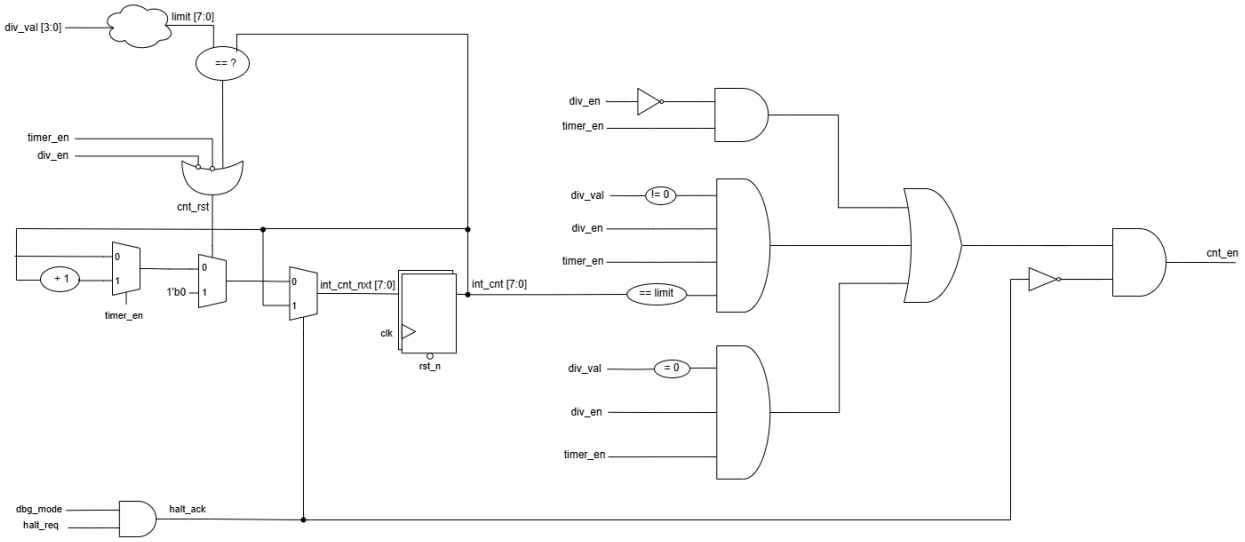


4. Logic Diagram

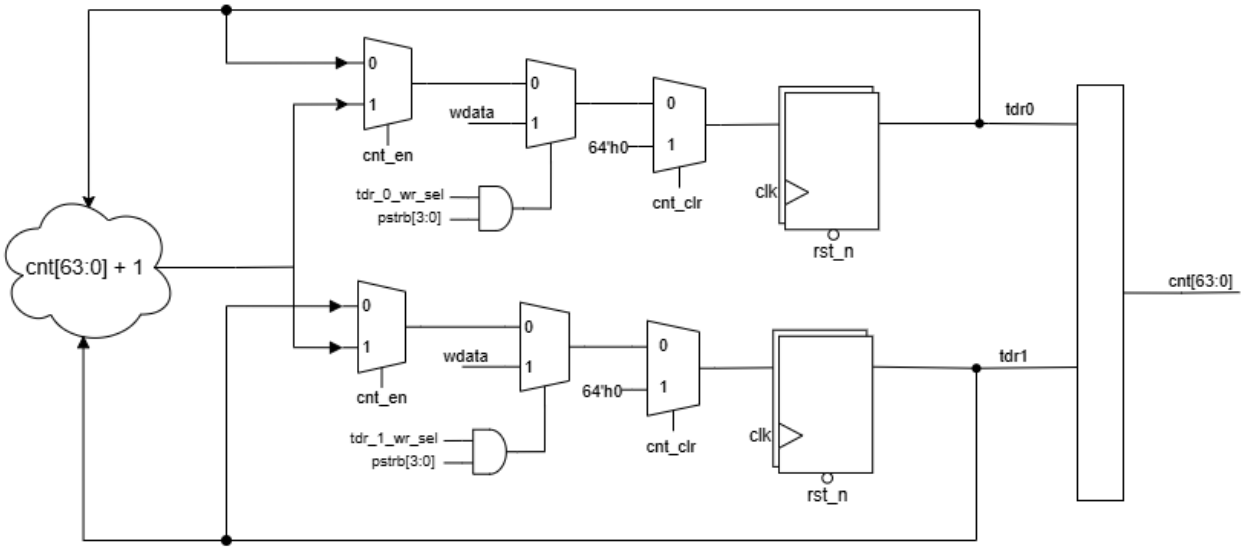
APB Slave



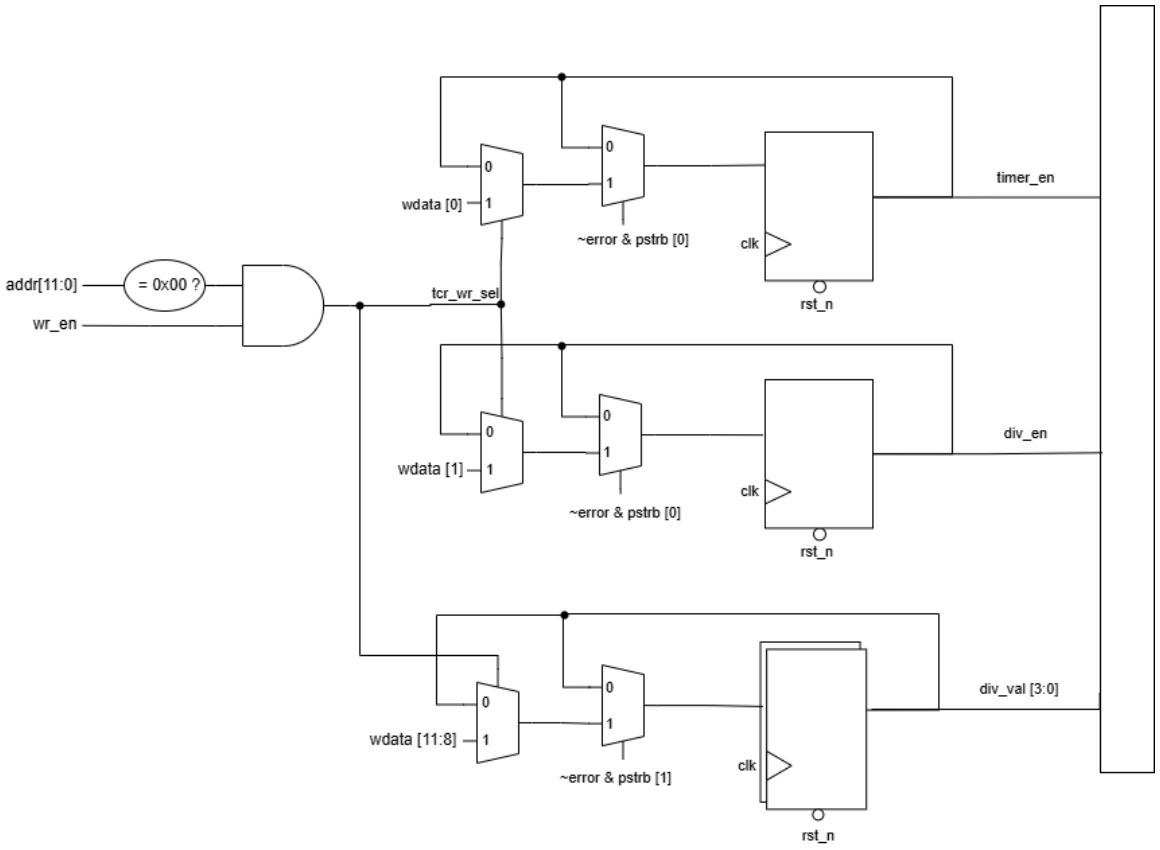
Counter control



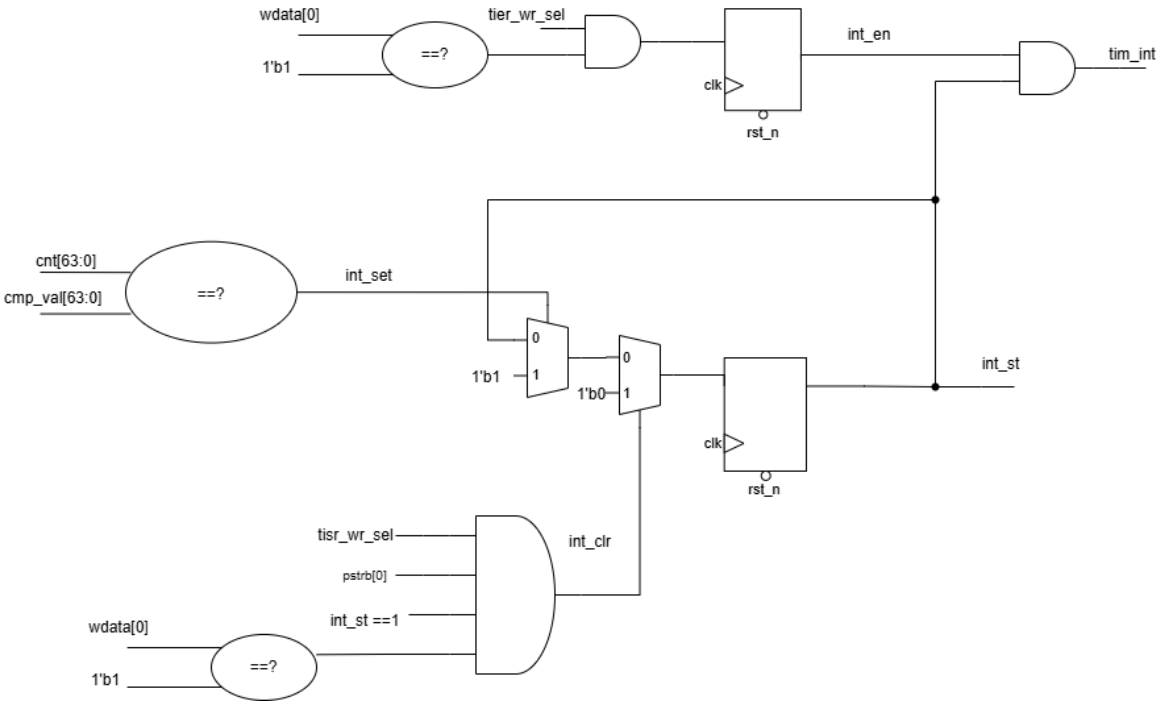
Counter



TCR

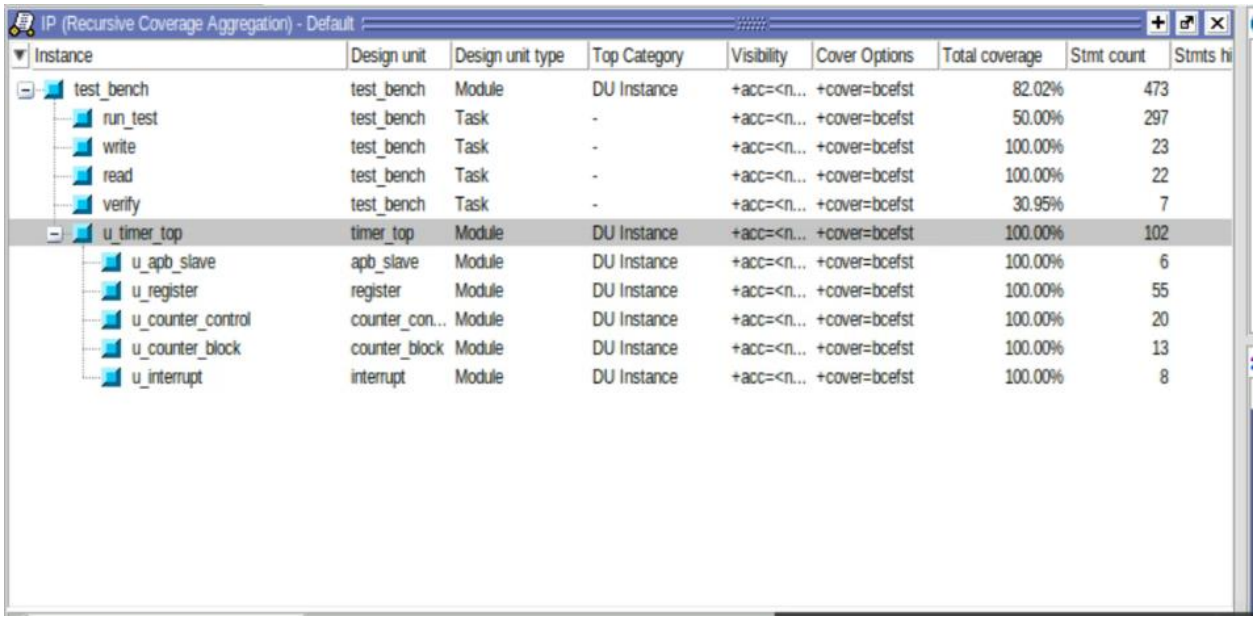


Interrupt



CHAPTER 3: SIMULATION RESULT

1. Coverage



IP (Recursive Coverage Aggregation) - Default

Instance	Design unit	Design unit type	Top Category	Visibility	Cover Options	Total coverage	Stmt count	Stmts hi
test_bench	test_bench	Module	DU Instance	+acc=<n...	+cover=bcefst	82.02%	473	
run_test	test_bench	Task	-	+acc=<n...	+cover=bcefst	50.00%	297	
write	test_bench	Task	-	+acc=<n...	+cover=bcefst	100.00%	23	
read	test_bench	Task	-	+acc=<n...	+cover=bcefst	100.00%	22	
verify	test_bench	Task	-	+acc=<n...	+cover=bcefst	30.95%	7	
u_timer_top	timer_top	Module	DU Instance	+acc=<n...	+cover=bcefst	100.00%	102	
u_apb_slave	apb_slave	Module	DU Instance	+acc=<n...	+cover=bcefst	100.00%	6	
u_register	register	Module	DU Instance	+acc=<n...	+cover=bcefst	100.00%	55	
u_counter_control	counter_con...	Module	DU Instance	+acc=<n...	+cover=bcefst	100.00%	20	
u_counter_block	counter_block	Module	DU Instance	+acc=<n...	+cover=bcefst	100.00%	13	
u_interrupt	interrupt	Module	DU Instance	+acc=<n...	+cover=bcefst	100.00%	8	

PAT_NAME	RUN_DATE	RESULT
onehot	18:04:21 Apr 23 2025	PASSED
reserved_reg	18:04:23 Apr 23 2025	PASSED
tcr_check	18:04:25 Apr 23 2025	PASSED
tdr_check	18:04:26 Apr 23 2025	PASSED
tcmp_check	18:04:28 Apr 23 2025	PASSED
tier_check	18:04:29 Apr 23 2025	PASSED
tisr_check	18:04:31 Apr 23 2025	PASSED
thcsr_check	18:04:33 Apr 23 2025	PASSED
timer_en_fallingedge	18:04:34 Apr 23 2025	PASSED
pstrb_check	18:04:36 Apr 23 2025	PASSED
counter_check	18:04:37 Apr 23 2025	PASSED
counter_control_check	18:04:39 Apr 23 2025	PASSED

pstrb_check	18:04:36 Apr 23 2025	PASSED
counter_check	18:04:37 Apr 23 2025	PASSED
counter_control_check	18:04:39 Apr 23 2025	PASSED
apb_check	18:04:41 Apr 23 2025	PASSED
interrupt_check	18:04:43 Apr 23 2025	PASSED
timer_reset_check	18:04:44 Apr 23 2025	PASSED
halt_check	18:04:46 Apr 23 2025	PASSED

TOTAL/PASSES/REMAIN:16/16/0

2. **Golden model**

PAT_NAME	RUN_DATE	RESULT
reg_init_chk	18:08:28 Apr 23 2025	PASSED
reg_rw_chk	18:08:29 Apr 23 2025	PASSED
reg_reserved_chk	18:08:31 Apr 23 2025	PASSED
reg_1hot_chk	18:08:33 Apr 23 2025	PASSED
reg_byte_access	18:08:34 Apr 23 2025	PASSED
cnt_ctrl_chk	18:08:52 Apr 23 2025	PASSED
apb_protocol_chk	18:08:54 Apr 23 2025	PASSED
apb_multiple_access	18:08:56 Apr 23 2025	PASSED
apb_unaligned_chk	18:08:57 Apr 23 2025	PASSED
cnt_counting_chk	18:08:59 Apr 23 2025	PASSED
interrupt_chk	18:09:01 Apr 23 2025	PASSED
cnt_halt_chk	18:09:11 Apr 23 2025	PASSED
apb_pslverr_chk	18:09:13 Apr 23 2025	PASSED

TOTAL/PASSED/REMAIN:13/13/0

phannhi@ictc-eda-ldap-2:~/final_project/golden_adv/sim$

3. **RTL code and Verification**

/ictc/student_data/phannhi/final_project