National Semiconductor

March 1993

74ACQ574 • 54ACTQ/74ACTQ574 Quiet Series Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ574 is a high-speed, low-power octal D-type flip-flop with a buffered Common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH clock (CP) transition.

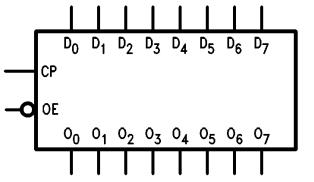
'ACQ/'ACTQ574 utilizes Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

The 'ACQ/'ACTQ574 is functionally identical to the 'ACTQ374 but with different pin-out.

Features

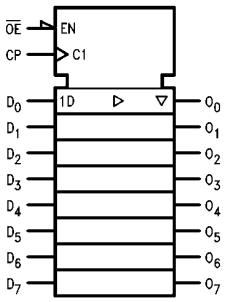
- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on opposite sides of the package allowing easy interface with microprocessors
- Functionally identical to the 'ACQ/ACTQ374
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT574
- 4 kV minimum ESD immunity
- Standard Military Drawing (SMD)
  — 'ACTQ574: 5962-8960102

Logic Symbols



TL/F/10634–1

IEEE/IEC

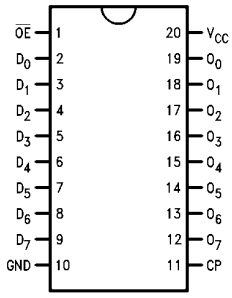


TL/F/10634–2

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

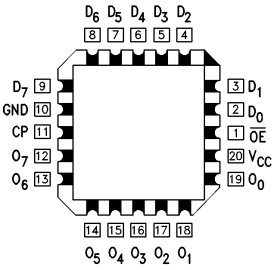
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10634–3

Pin Assignment for LCC



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Functional Description

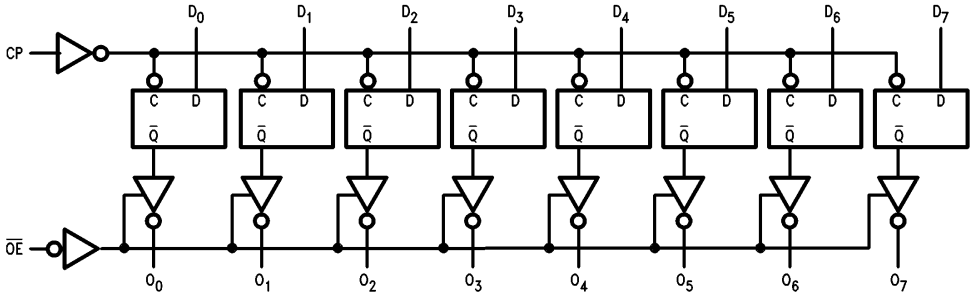
The 'ACQ/'ACTQ574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_N	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⌐	L	L	Z	Load
H	⌐	H	H	Z	Load
L	⌐	L	L	L	Data Available
L	⌐	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



TL/F/10634–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACTQ	−55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$ 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$ 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Electrical Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50\ \mu A$
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.76		I_{OH} −24 mA
		5.5		4.86	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} 12 mA
		4.5		0.36	0.44		I_{OL} 24 mA
		5.5		0.36	0.44		24 mA

*All outputs loaded; thresholds on input associated with output under test.

DC Electrical Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ		74ACQ	Units	Conditions
			$T_A = +25°C$		$T_A = -40°C$ to $+85°C$		
			Typ	Guaranteed Limits			
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND (Note 1)
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.25	±2.5	μA	V_I(OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5		V	*Figures 2-12*, *13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2		V	*Figures 2-12*, *13* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 4: Maximum number of data inputs (n) switching. (n−1) inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). f = 1 MHz.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ		54ACTQ	74ACTQ	Units	Conditions
			$T_A = +25°C$		$T_A = -55°C$ to $+125°C$	$T_A = -40°C$ to $+85°C$		
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.85	3.70	3.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} -24 mA
		5.5		4.86	4.70	4.76		I_{OH} -24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	± 1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		± 0.25	± 5.0	± 2.5	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			-50	-75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 2-12*, *13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	-0.6	-1.2			V	*Figures 2-12*, 13 (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n−1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF			74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3.3 5.0	75 90			70 85		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5	3.0 2.0	13.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable Time	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5	3.0 2.0	13.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	9.5 8.0	14.5 9.5	1.0 1.0	15.0 10.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to $\overline{O}_n$	3.3 5.0		1.0 0.5	1.5 1.0		1.5 1.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V
Voltage Range 3.3 is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF		74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	0 0	3.0 3.0	3.0 3.0	ns
t_H	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0	1.5 1.5	1.5 1.5	ns
t_W	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0	4.0 4.0	4.0 4.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V
Voltage Range 3.3 is 3.3V ±0.3V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	5.0	85			95		80		MHz
t_{PLH}, t_{PHL}	Propagation Delay CP to $\overline{O}_n$	5.0	2.0	7.0	9.0	1.0	11.0	2.0	9.5	ns
t_{PZH}, t_{PZL}	Output Enable Time	5.0	2.0	7.0	9.0	1.0	11.0	2.0	9.5	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0	1.0	11.0	1.0	10.5	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to $\overline{O}_n$	5.0		0.5	1.0				1.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum			
t_S	Setup Time, HIGH or LOW D_n to CP	5.0	0	3.0	3.5	3.0	ns
t_H	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.5	2.0	1.5	ns
t_W	CP Pulse Width, HIGH or LOW	5.0	2.0	4.0	5.0	4.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

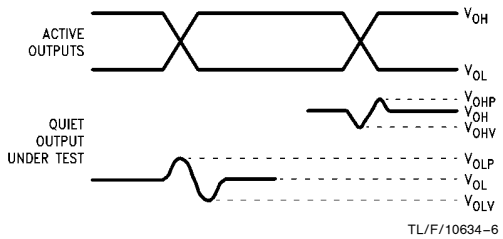
1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{CC} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.



TL/F/10634–6

FIGURE 1. Quiet Output Noise Voltage Waveforms

Note A. V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B. Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

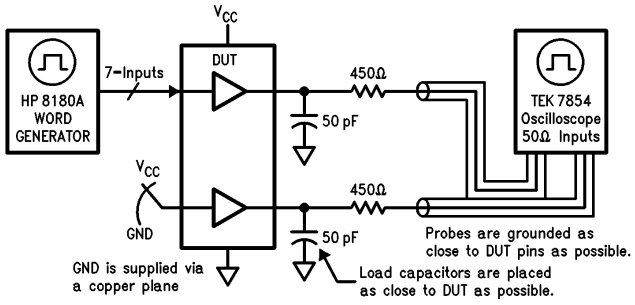


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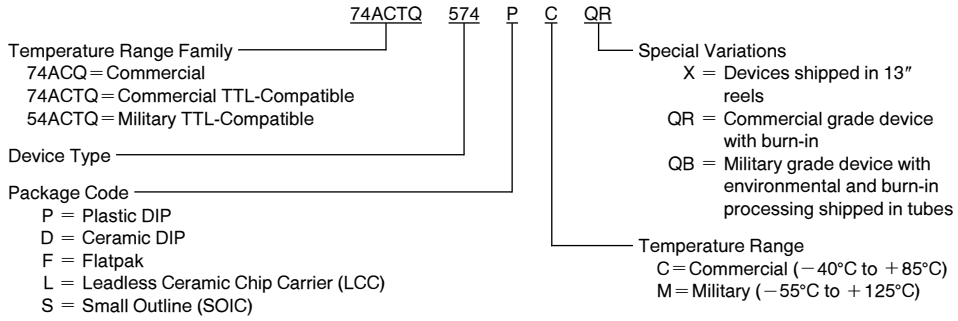
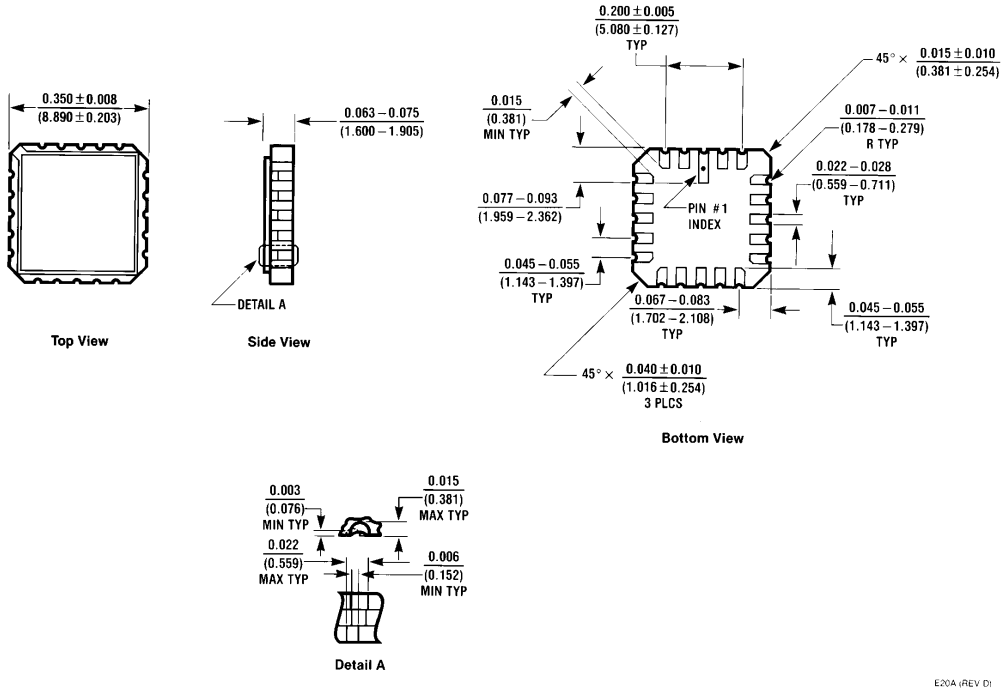
FIGURE 2. Simultaneous Switching Test Circuit

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

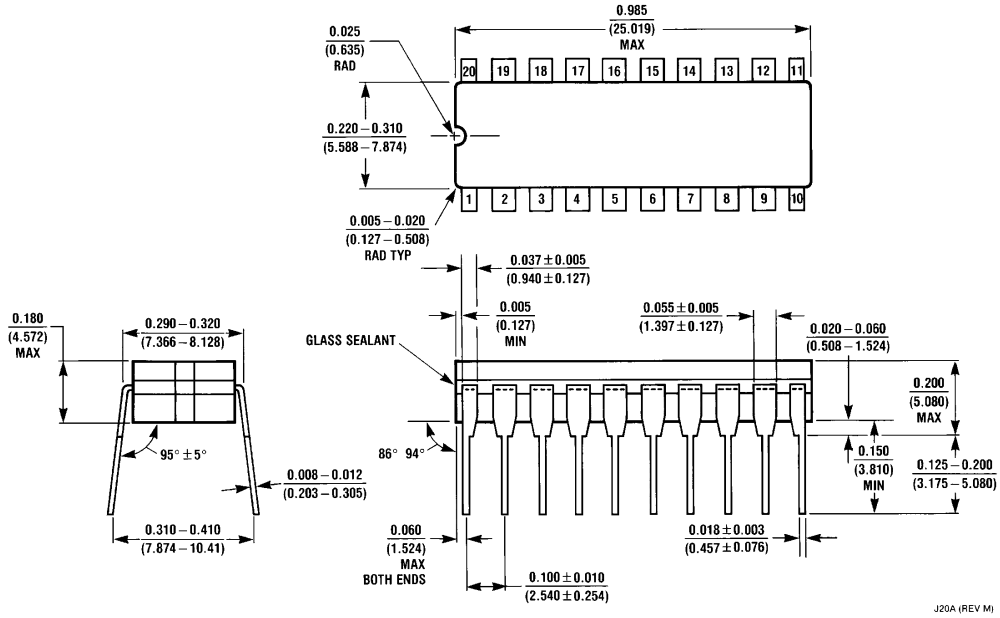


Physical Dimensions inches (millimeters)



E20A (REV D)

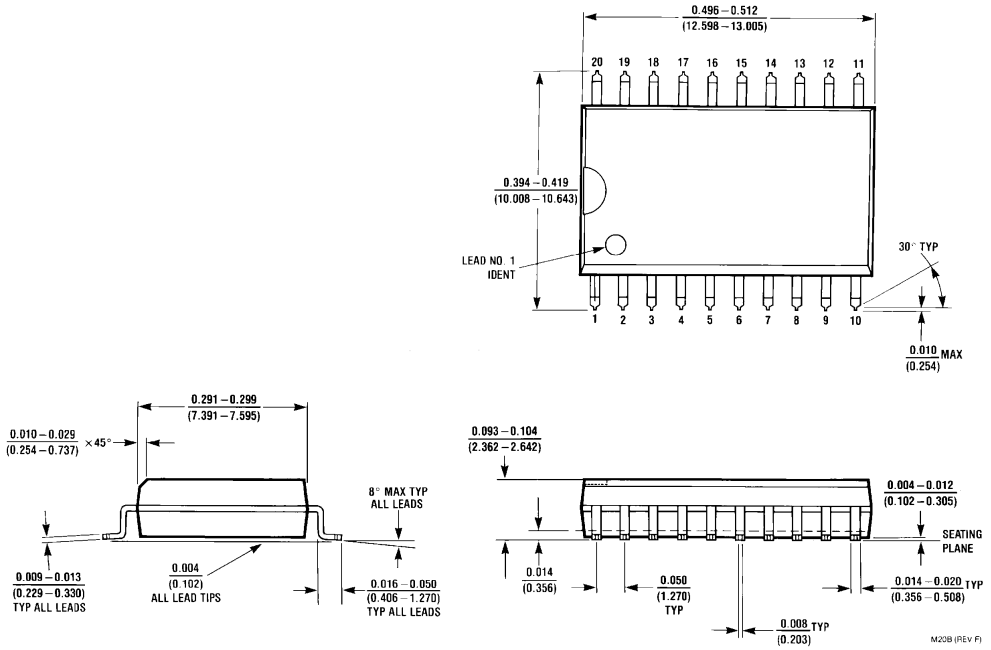
20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



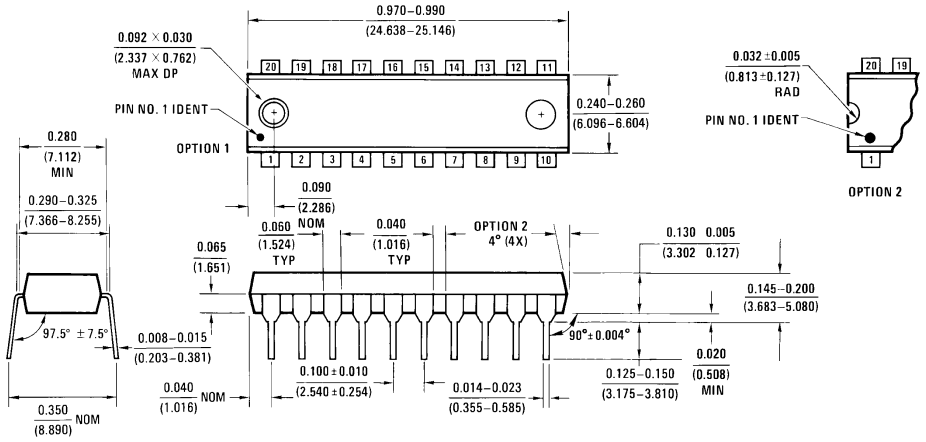
J20A (REV M)

20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) (Continued)



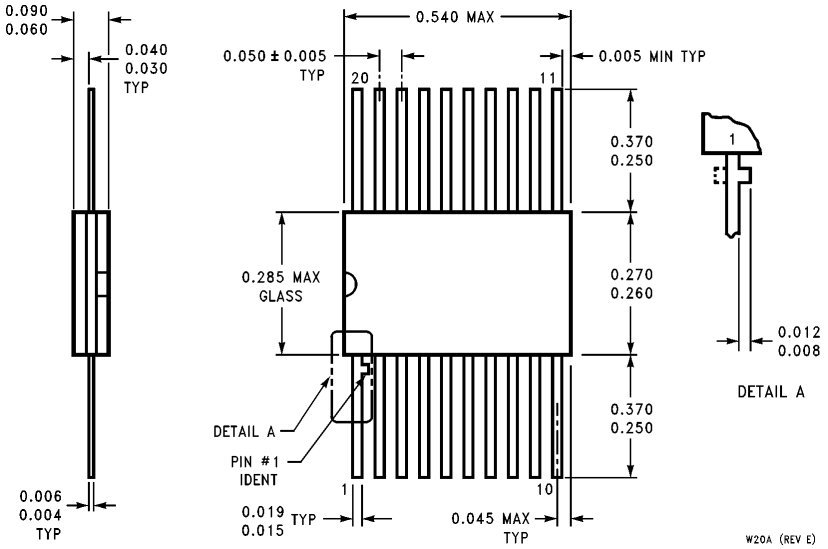
20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B



20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

Physical Dimensions inches (millimeters) (Continued)

Lit. # 115000



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998