

# TRIBHUVAN UNIVERSITY



Institute of Engineering  
**Pulchowk Campus**

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## **LAB REPORT ON**

**Combinational Logic Design Using VHDL**

**[ EMBEDDED SYSTEM]**

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Lab No.: 04

Experiment Date: 2081/11/12

Submission Date: 2081/11/12

**Submitted By:**

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Group : A

**Submitted To:**

Department of Electronics and  
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