TMS320x280x Enhanced Capture (eCAP) Module Reference Guide

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Preface

Read This First

About This Manual

The enhanced capture (eCAP) module is used in systems where accurate timing of external events is important. This guide describes the module and how to use it.

Related Documentation From Texas Instruments

The following books describe the TMS320C28x and related support tools. These documents can be downloaded from the TI website (www.ti.com).

TMS320C28x DSP CPU and Instruction Set Reference Guide (literature number SPRU430) describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x™ fixed-point digital signal processors (DSPs). It also describes emulation features available on these DSPs.

TMS320F2801, TMS320F2806, TMS320F2808 Digital Signal Processors (literature number SPRS230) data sheet contains the pinout, signal descriptions, as well as electrical and timing specifications for the F280x devices.

TMS320x280x Analog-to-Digital Converter (ADC) Reference Guide (literature number SPRU716) describes the ADC module. The module is a 12−bit pipelined ADC. The analog circuits of this converter, referred to as the core in this document, include the front-end analog multiplexers (MUXs), sample−and−hold (S/H) circuits, the conversion core, voltage regulators, and other analog supporting circuits. Digital circuits, referred to as the wrapper in this document, include programmable conversion sequencer, result registers, interface to analog circuits, interface to device peripheral bus, and interface to other on-chip modules.

TMS320x280x Boot ROM Reference Guide (literature number SPRU722) describes the purpose and features of the bootloader (factory-programmed boot-loading software). It also describes other contents of the device on-chip boot ROM and identifies where all of the information is located within that memory.

TMS320x281x, 280x Enhanced Controller Area Network (eCAN) Reference Guide (literature number SPRU074) describes the eCAN that uses established protocol to communicate serially with other controllers in electrically noisy environments. With 32 fully configurable mailboxes and time-stamping feature, the eCAN module provides a versatile and robust serial communication interface. The eCAN module implemented in the C28x DSP is compatible with the CAN 2.0B standard (active).

TMS320x281x, 280x Peripheral Reference Guide (literature number SPRU566) describes the peripheral reference guides of the 28x digital signal processors (DSPs).

TMS320x281x, 280x Serial Communication Interface (SCI) Reference Guide (literature number SPRU051) describes the SCI that is a two-wire asynchronous serial port, commonly known as a UART. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format.

TMS320x281x, 280x Serial Peripheral Interface (SPI) Reference Guide (literature number SPRU059) describes the SPI − a high-speed synchronous serial input/output (I/O) port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmed bit−transfer rate. The SPI is used for communications between the DSP controller and external peripherals or another controller.

TMS320x280x System Control and Interrupts Reference Guide (literature number SPRU712) describes the various interrupts and system control features of the 280x digital signal processors (DSPs).

The TMS320C28x Instruction Set Simulator Technical Overview (literature number SPRU608) describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x core.

TMS320x280x Enhanced Quadrature Encoder Pulse (eQEP) Reference Guide (literature number SPRU790) describes the eQEP module, which is used for interfacing with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine in high performance motion and position control systems. It includes the module description and registers.

TMS320x280x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide (literature number SPRU791). The PWM peripheral is an

essential part of controlling many of the power related systems found in both commercial and industrial equipments. This guide describes the main areas that include digital motor control, switch mode power supply control, UPS (uninterruptable power supplies), and other forms of power conversion. The PWM peripheral can be considered as performing a DAC function, where the duty cycle is equivalent to a DAC analog value, it is sometimes referred to as a Power DAC.

TMS320C28x DSP/BIOS Application Programming Interface (API) Reference Guide (literature number SPRU625) describes development using DSP/BIOS.

3.3 V DSP for Digital Motor Control Application Report (literature number SPRA550). New generations of motor control digital signal processors (DSPs) lower their supply voltages from 5 V to 3.3 V to offer higher performance at lower cost. Replacing traditional 5-V digital control circuitry by 3.3-V designs introduce no additional system cost and no significant complication in interfacing with TTL and CMOS compatible components, as well as with mixed voltage ICs such as power transistor gate drivers. Just like 5-V based designs, good engineering practice should be exercised to minimize noise and EMI effects by proper component layout and PCB design when 3.3-V DSP, ADC, and digital circuitry are used in a mixed signal environment, with high and low voltage analog and switching signals, such as a motor control system. In addition, software techniques such as Random PWM method can be used by special features of the Texas Instruments (TI) TMS320x24xx DSP controllers to significantly reduce noise effects caused by EMI radiation.

This application report reviews designs of 3.3-V DSP versus 5-V DSP for low HP motor control applications.The application report first describes a scenario of a 3.3-V-only motor controller indicating that for most applications, no significant issue of interfacing between 3.3 V and 5 V exists. Cost-effective 3.3-V − 5-V interfacing techniques are then discussed for the situations where such interfacing is needed. On-chip 3.3-V ADC versus 5-V ADC is also discussed. Sensitivity and noise effects in 3.3-V and 5-V ADC conversions are addressed. Guidelines for component layout and printed circuit board (PCB) design that can reduce system's noise and EMI effects are summarized in the last section.

IC Package Thermal Metrics Application Report (literature number SPRA953). Many thermal metrics exist for IC packages ranging from Theta-ja to Psi-jt. Often, these thermal metrics are misapplied by cus-

tomers who try to use them to estimate junction temperatures in their systems. This document will describe the traditional and new thermal metrics and will put their application in perspective with respect to system level junction temperature estimation.

Simulation Fulfills its Promise for Enhancing Debug and Analysis − A White Paper (literature number SPRA991). In the past, simulators did not prove realistic or feasible for debug and performance analysis in the early stages of development. Now, however, advancements in fast simulation technology and analysis tools have enabled developers to speed up the development cycle by allowing them to evaluate system alternatives more effectively. This article will discuss the simulation enhancements that make this possible.

Trademarks

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Enhanced Capture (eCAP) Module

The enhanced Capture (eCAP) module is essential in systems where accurate timing of external events is important.

This reference guide is applicable for the eCAP found on the TMS320x280x family of processors. This includes all Flash-based, ROM-based, and RAM-based devices within the 280x family.

Uses for eCAP include:

- ❑ Speed measurements of rotating machinery (e.g., toothed sprockets sensed via Hall sensors)
- ❑ Elapsed time measurements between position sensor pulses
- ❑ Period and duty cycle measurements of pulse train signals
- ❑ Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module described in this guide includes the following features:

- ❑ 32-bit time base with 10-nS time resolution with a 100-MHz system clock
- ❑ 4-event time-stamp registers (each 32 bits)
- ❑ Edge polarity selection for up to four sequenced time-stamp capture events
- ❑ Interrupt on either of the four events
- ❑ Single shot capture of up to four event time-stamps
- ❑ Continuous mode capture of time-stamps in a four-deep circular buffer
- ❑ Absolute time-stamp capture
- ❑ Difference (Delta) mode time-stamp capture
- ❑ All above resources dedicated to a single input pin
- ❑ When not used in capture mode, the ECAP module can be configured as a single channel PWM output

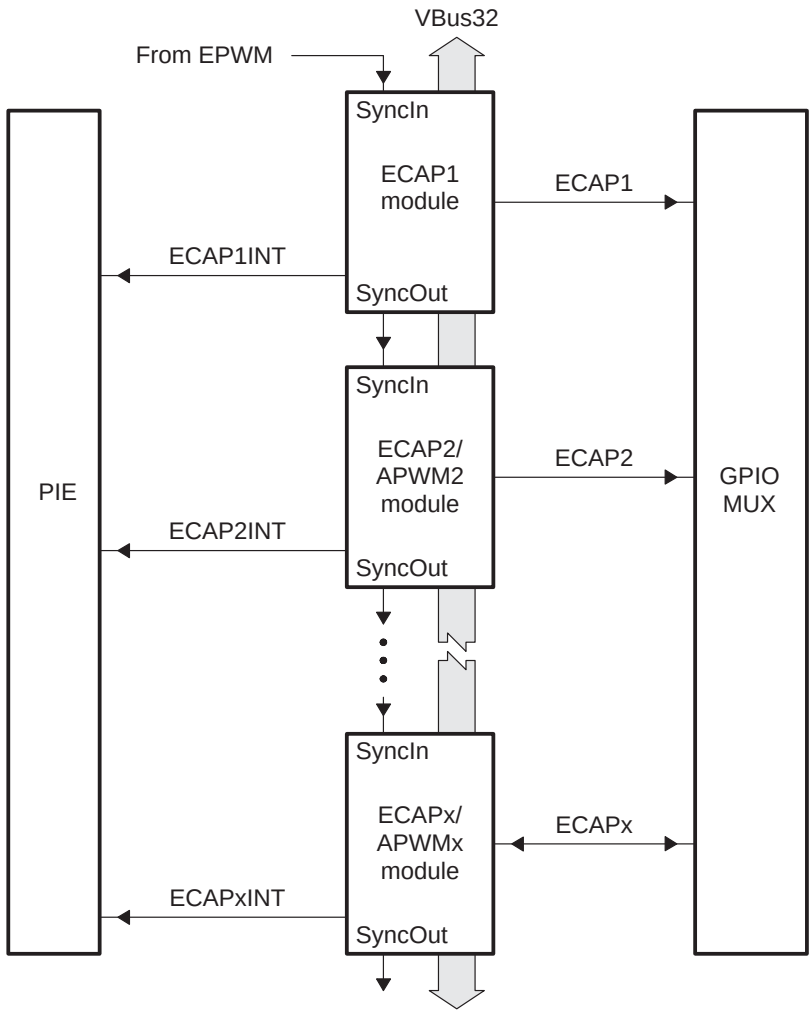
1 Description

The eCAP module represents one complete capture channel that can be instantiated multiple times depending on the target device. In the context of this guide, one eCAP channel has the following independent key resources:

- ❏ Dedicated input capture pin
- ❏ 32-bit time base (counter)
- ❏ 4 x 32-bit time-stamp capture registers (CAP1−CAP4)
- ❏ 4-stage sequencer (Modulo4 counter) that is synchronized to external events, ECAP pin rising/falling edges.
- ❏ Independent edge polarity (rising/falling edge) selection for all 4 events
- ❏ Input capture signal prescaling (from 2−62)
- ❏ One-shot compare register (2 bits) to freeze captures after 1 to 4 time-stamp events
- ❏ Control for continuous time-stamp captures using a 4-deep circular buffer (CAP1−CAP4) scheme
- ❏ Interrupt capabilities on any of the 4 capture events

Multiple identical eCAP modules can be contained in a 280x system as shown in Figure 1. The number of modules is device-dependent and is based on target application needs.

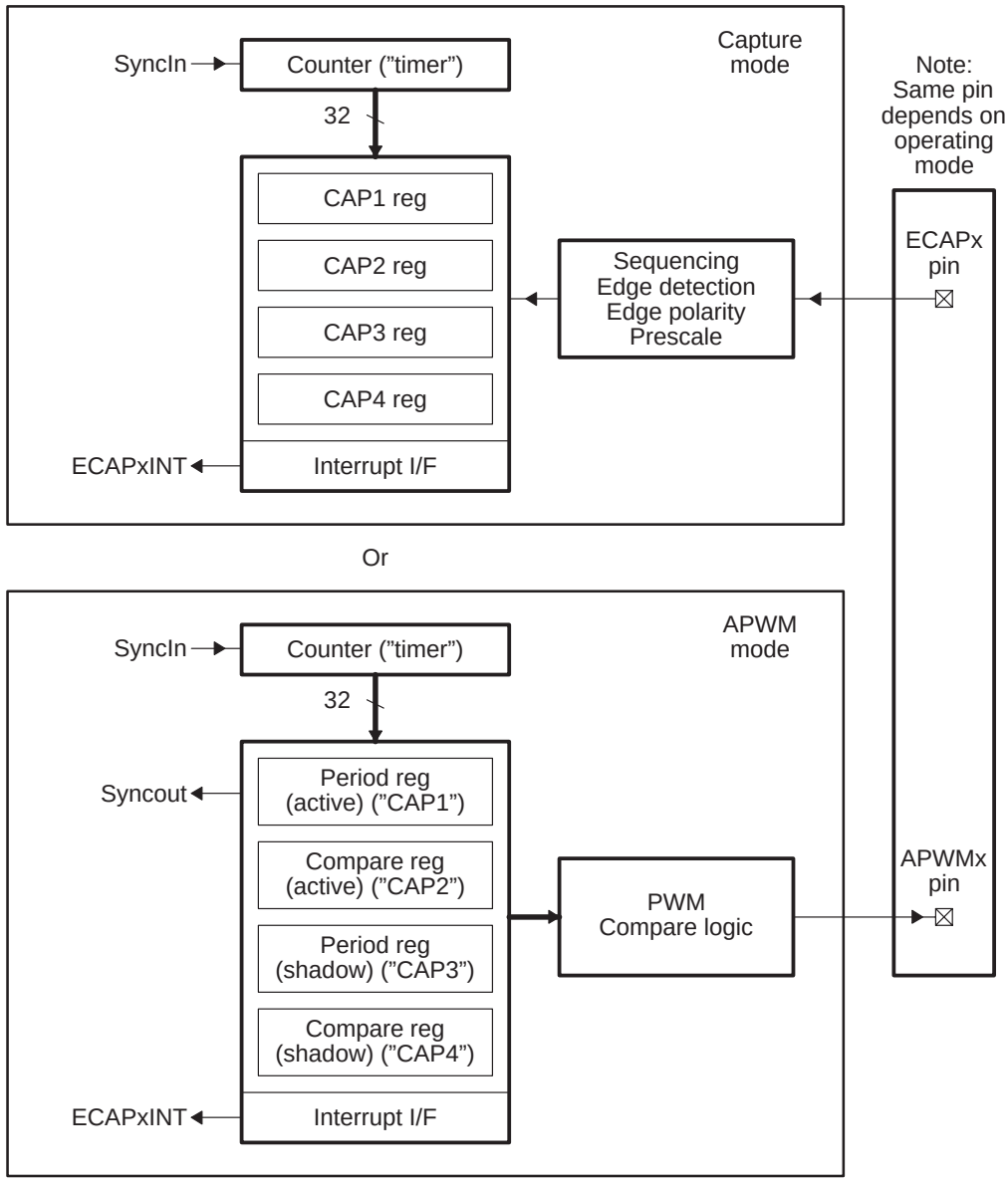
Figure 1. Multiple eCAP Modules In A 28x System



2 Capture and APWM Operating Mode

You can use the eCAP module resources to implement a single-channel PWM generator (with 32 bit capabilities) when it is not being used for input captures. The counter operates in count-up mode, providing a time-base for asymmetrical pulse width modulation (PWM) waveforms. The CAP1 and CAP2 registers become the active period and compare registers, respectively, while CAP3 and CAP4 registers become the period and capture shadow registers, respectively. Figure 2 is a high-level view of both the capture and auxiliary pulse-width modulator (APWM) modes of operation.

Figure 2. Capture and APWM Modes of Operation



1) A single pin is shared between CAP and APWM functions. In capture mode it is an input; in APWM mode, it is an output.

2) In APWM mode, writing any value to CAP1/CAP2 active registers also writes the same value to the corresponding shadow registers CAP3/CAP4. This emulates immediate mode. Writing to the shadow registers CAP3/CAP4 invokes the shadow mode.

3 Capture Mode Description

Figure 3 shows the various components that implement the capture function.

3.1 Event Prescaler

- An input capture signal (pulse train) can be prescaled by N = 2−62 (in multiples of 2) or can by-pass the prescaler.
- Useful when very high frequency signals are used as inputs.

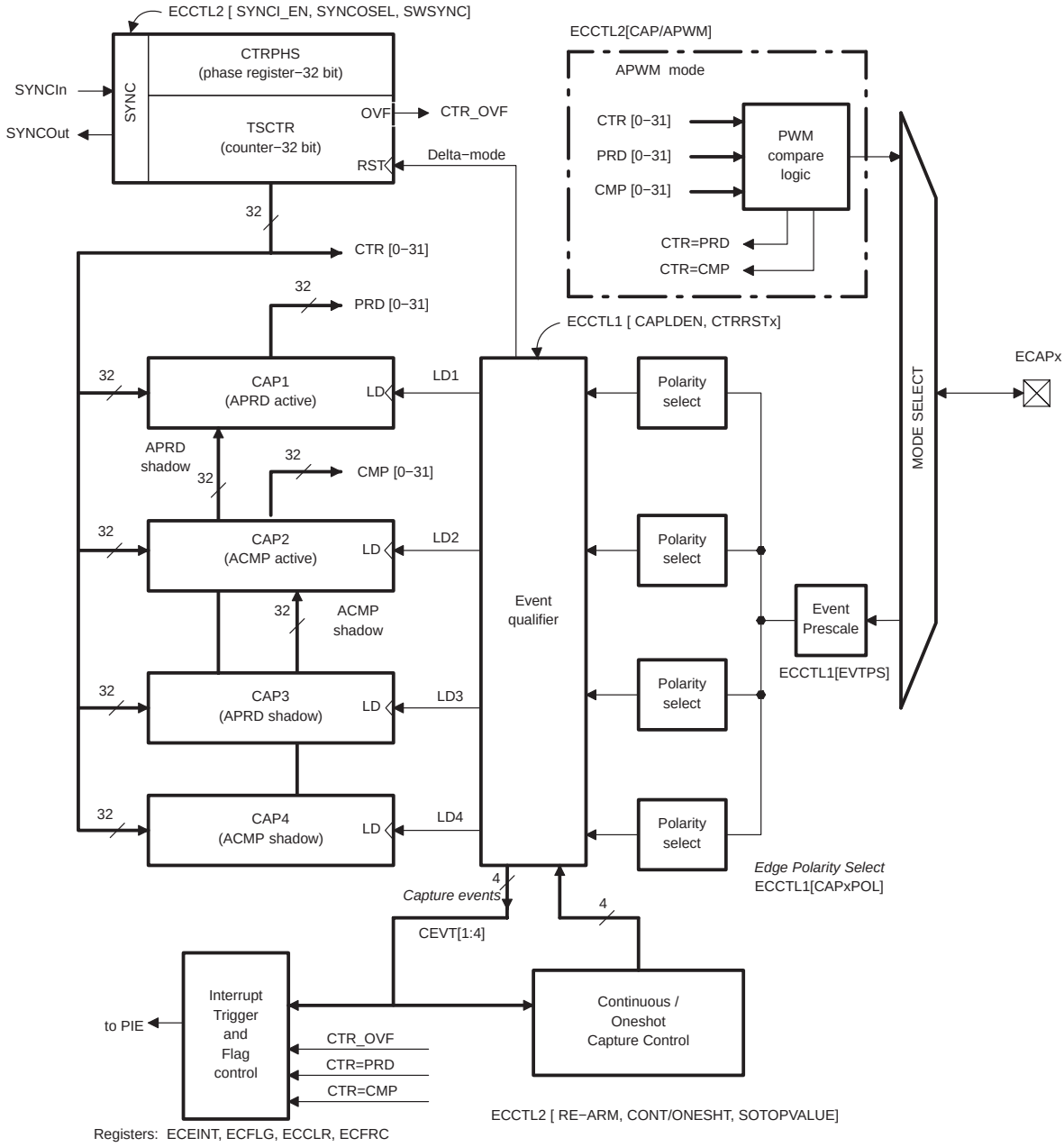
3.2 Edge Polarity Select and Qualifier

- Four independent edge polarity (rising edge/falling edge) selection MUXes are used, one for each capture event.
- Each edge (up to 4) is event qualified by the Modulo4 sequencer.
- The edge event is gated to its respective CAPx register by the Mod4 counter. The CAPx register is loaded on the falling edge.

3.3 Continuous/One-Shot Control

- The Mod4 (2 bit) counter is incremented via edge qualified events (CEVT1−CEVT4).
- The Mod4 counter continues counting (0−>1−>2−>3−>0) and wraps around unless stopped.
- A 2-bit stop register is used to compare the Mod4 counter output, and when equal stops the Mod4 counter and inhibits further loads of the CAP1−CAP4 registers. This occurs during one-shot operation.

Figure 3. Capture Function Diagram



The continuous/one-shot block controls the start/stop and reset (zero) functions of the Mod4 counter via a mono-shot type of action that can be triggered by the stop-value comparator and re-armed via software control.

Once armed, the eCAP module waits for 1−4 (defined by stop-value) capture events before freezing both the Mod4 counter and contents of CAP1−4 registers (i.e., time-stamps).

Re-arming prepares the eCAP module for another capture sequence. Also re-arming clears (to zero) the Mod4 counter and permits loading of CAP1−4 registers again, providing the CAPLDEN bit is set.

In continuous mode, the Mod4 counter continues to run (0−>1−>2−>3−>0, the one-shot action is ignored, and capture values continue to be written to CAP1−4 in a circular buffer sequence.

3.4 32-Bit Counter and Phase Control

This counter provides the time-base for event captures, and is clocked via the system clock.

A phase register is provided to achieve synchronization with other counters, via a hardware and software forced sync. This is useful in APWM mode when a phase offset between modules is needed.

On any of the four event loads, an option to reset the 32-bit counter is given. This is useful for time difference capture. The 32-bit counter value is captured first, then it is reset to 0 by any of the LD1−LD4 signals.

3.5 CAP1−CAP4 Registers

These 32-bit registers are fed by the 32-bit counter timer bus, CTR[0−31] and are loaded (i.e., capture a time-stamp) when their respective LD inputs are strobed.

Loading of the capture registers can be inhibited via control bit CAPLDEN. During one-shot operation, this bit is cleared (loading is inhibited) automatically when a stop condition occurs, i.e. StopValue = Mod4.

CAP1 and CAP2 registers become the active period and compare registers, respectively, in APWM mode.

CAP3 and CAP4 registers become the respective shadow registers (APRD and ACMP) for CAP1 and CAP2 during APWM operation.

3.6 Interrupt Control

An Interrupt can be generated on capture events (CEVT1−CEVT4, CTROVF) or APWM events (CTR=PRD , CTR = CMP).

A counter overflow event (FFFFFFFF−>00000000) is also provided as an interrupt source (CTROVF).

The capture events are edge and sequencer qualified (i.e. ordered in time) by the polarity select and Mod4 gating, respectively.

One of these events can be selected as the interrupt source (from the eCAPx module) going to the PIE.

3.7 Shadow Load and Lockout Control

In capture mode, this logic inhibits (locks out) any shadow loading of CAP1 or CAP2 from APRD and ACMP registers, respectively.

In APWM mode, shadow loading is active and two choices are permitted:

1) Immediate − APRD or ACMP are transferred to CAP1 or CAP2 immediately upon writing a new value.
2) On period equal, i.e., CTR[31:0] = PRD[31:0]

3.8 APWM Mode Operation

Main operating highlights of the APWM section:

- The time-stamp counter bus is made available for comparison via 2 digital (32-bit) comparators.
- When CAP1/2 registers are not used in capture mode, their contents can be used as Period and Compare values in APWM mode.
- Double buffering is achieved via shadow registers APRD and ACMP (CAP3/4). The shadow register contents are transferred over to CAP1/2 registers either immediately upon a write, or on a CTR=PRD trigger.
- In APWM mode, writing to CAP1/CAP2 active registers will also write the same value to the corresponding shadow registers CAP3/CAP4. This emulates immediate mode. Writing to the shadow registers CAP3/CAP4 will invoke the shadow mode.

The behavior of APWM active high mode (APWMPOL == 0) is as follows:

```
CMP = 0x00000000, output low for duration of period (0% duty)
CMP = 0x00000001, output high 1 cycle
CMP = 0x00000002, output high 2 cycles
 .
CMP = PERIOD,     output high except for 1 cycle  (<100% duty)
CMP = PERIOD+1,   output high for complete period (100% duty)
CMP > PERIOD+1,   output high for complete period
```

The behavior of APWM active low mode (APWMPOL == 1) is as follows:

```
CMP = 0x00000000, output high for duration of period (0% duty)
CMP = 0x00000001, output low 1 cycle
CMP = 0x00000002, output low 2 cycles
 .
CMP = PERIOD,     output low except for 1 cycle (<100% duty)
CMP = PERIOD+1,   output low for complete period (100% duty)
CMP > PERIOD+1,   output low for complete period
```

Note: CMP > PERIOD+1 is not normal user operation but may occur if you change the period value to be less than the CMP value.

4 Capture Module − Control and Status Registers

Figure 4. Time-Stamp Counter Register (TSCTR)

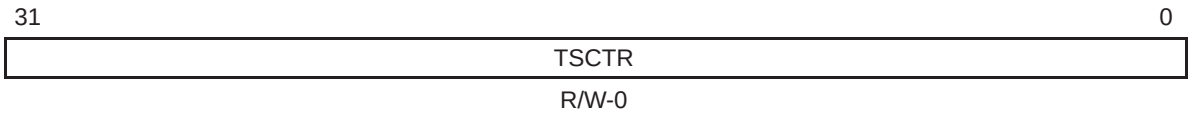


Table 1. Time-Stamp Counter Register (TSCTR) Field Descriptions

Bit(s)	Field	Description
31:0	TSCTR	Active 32-bit counter register, which is used as the capture time-base

Figure 5. Counter Phase Control Register (CTRPHS)

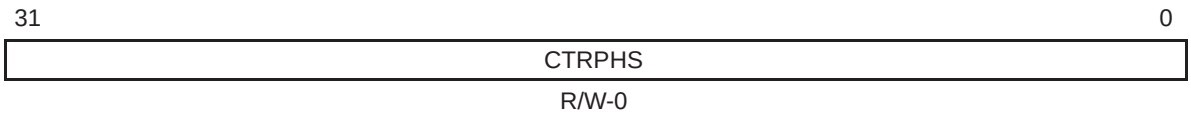


Table 2. Counter Phase Control Register (CTRPHS) Field Descriptions

Bit(s)	Field	Description
31:0	CTRPHS	Counter phase value register that can be programmed for phase lag/lead. This register shadows CTRPHS and is loaded into CTRPHS upon either a SYNCI event or S/W force via a control bit. Used to achieve phase control synchronization with respect to other eCAP and EPWM time-bases.

Figure 6. Capture-1 Register (CAP1)

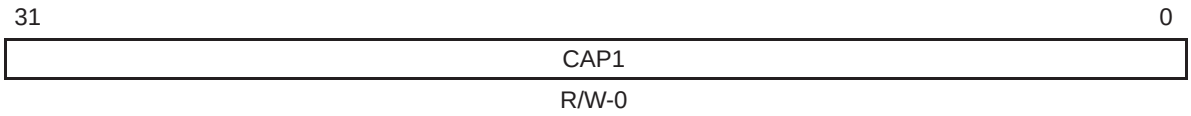


Table 3. Capture-1 Register (CAP1) Field Descriptions

Bit(s)	Field	Description
31:0	CAP1	This register can be loaded (written) by : 1) Time-Stamp (i.e., counter value TSCTR) during a capture event 2) Software − may be useful for test purposes / initialization 3) APRD shadow register (i.e., CAP3) when used in APWM mode

Figure 7. Capture-2 Register (CAP2)

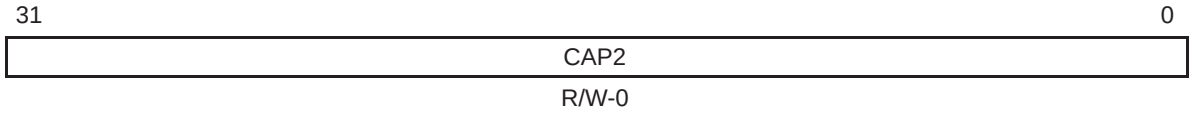


Table 4. Capture-2 Register (CAP2) Field Descriptions

Bit(s)	Field	Description
31:0	CAP2	This register can be loaded (written) by : 1) Time-Stamp (i.e., counter value) during a capture event 2) Software − may be useful for test purposes 3) APRD shadow register (i.e., CAP4) when used in APWM mode

Figure 8. Capture-3 Register (CAP3)

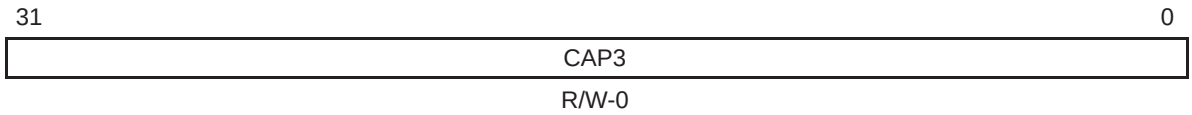


Table 5. Capture-3 Register (CAP3) Field Descriptions

Bit(s)	Field	Description
31:0	CAP3	In CMP mode, this is a time-stamp capture register. In APMW mode, this is the period shadow (APER) register. You update the PWM period value through this register. In this mode, CAP3 (APRD) shadows CAP1.

Figure 9. Capture-4 Register (CAP4)

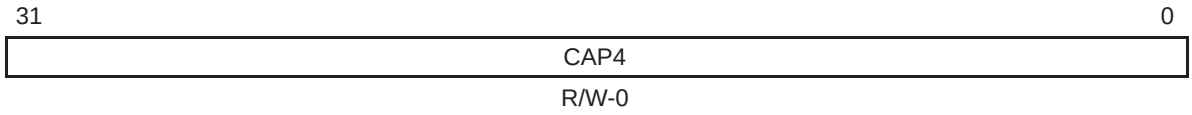
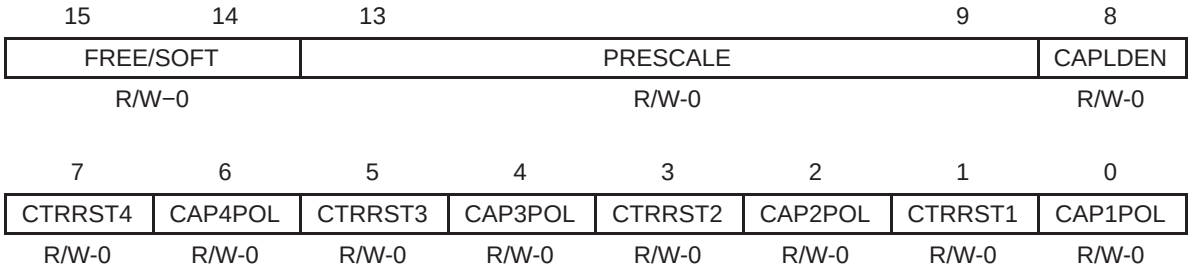


Table 6. Capture-4 Register (CAP4) Field Descriptions

Bit(s)	Field	Description
31:0	CAP4	In CMP mode, this is a time-stamp capture register. In APMW, mode this is the compare shadow (ACMP) register. You update the PWM compare value via this register. In this mode, CAP4 (ACMP) shadows CAP2.

Note: In APWM mode, writing to CAP1/CAP2 active registers also writes the same value to the corresponding shadow registers CAP3/CAP4. This emulates immediate mode. Writing to the shadow registers CAP3/CAP4 will invoke the shadow mode.

Figure 10. ECAP Control Register 1 (ECCTL1)



Note: R − Read, W − Write

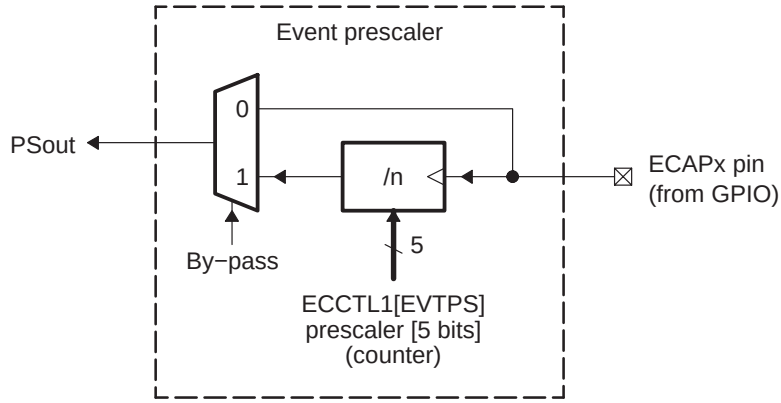
Table 7. ECAP Control Register 1 (ECCTL1) Field Descriptions

Bit(s)	Field	Description
15:14	FREE/SOFT	Emulation Control
		00 TSCTR counter stops immediately on emulation suspend
		01 TSCTR counter runs until = 0
		1x TSCTR counter is unaffected by emulation suspend (Run Free)
13:9	PRESCALE	Event Filter prescale select
		00000 Divide by 1 (i.e,. no prescale, by-pass the prescaler)
		00001 Divide by 2
		00010 Divide by 4
		00011 Divide by 6
		00100 Divide by 8
		00101 Divide by 10
		...
		11110 Divide by 60
		11111 Divide by 62
8	CAPLDEN	Enable Loading of CAP1−4 registers on a capture event
		0 Disable CAP1−4 register loads at capture event time.
		1 Enable CAP1−4 register loads at capture event time.

Table 7. ECAP Control Register 1 (ECCTL1) Field Descriptions (Continued)

Bit(s)	Field	Description
7	CTRRST4	Counter Reset on Capture Event 4
		0 *Do not* reset counter on Capture Event 4 (absolute time stamp operation)
		1 Reset counter after Capture Event 4 time-stamp has been captured (used in difference mode operation)
6	CAP4POL	Capture Event 4 Polarity select
		0 Capture Event 4 triggered on a rising edge (RE)
		1 Capture Event 4 triggered on a falling edge (FE)
5	CTRRST3	Counter Reset on Capture Event 3
		0 *Do not* reset counter on Capture Event 3 (absolute time stamp)
		1 Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	Capture Event 3 Polarity select
		0 Capture Event 3 triggered on a rising edge (RE)
		1 Capture Event 3 triggered on a falling edge (FE)
3	CTRRST2	Counter Reset on Capture Event 2
		0 *Do not* reset counter on Capture Event 2 (absolute time stamp)
		1 Reset counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	Capture Event 2 Polarity select
		0 Capture Event 2 triggered on a rising edge (RE)
		1 Capture Event 2 triggered on a falling edge (FE)
1	CTRRST1	Counter Reset on Capture Event 1
		0 *Do not* reset counter on Capture Event 1 (absolute time stamp)
		1 Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	Capture Event 1 Polarity select
		0 Capture Event 1 triggered on a rising edge (RE)
		1 Capture Event 1 triggered on a falling edge (FE)

Figure 11. Event Prescale Control



Note: When a prescale value of 1 is chosen (i.e. ECCTL1[13:9] = 0,0,0,0,0) the input capture signal by-passes the pre-scale logic completely.

Figure 12 shows the operation of the prescale function.

Figure 12. Prescale Function Waveforms

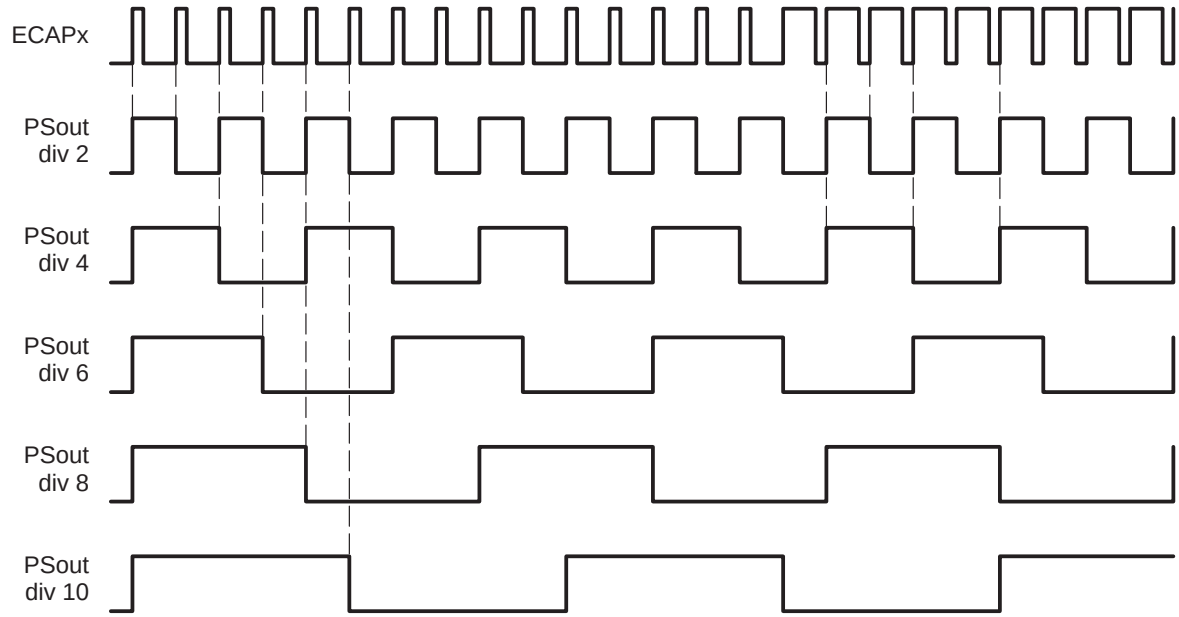


Figure 13. ECAP Control Register 2 (ECCTL2)

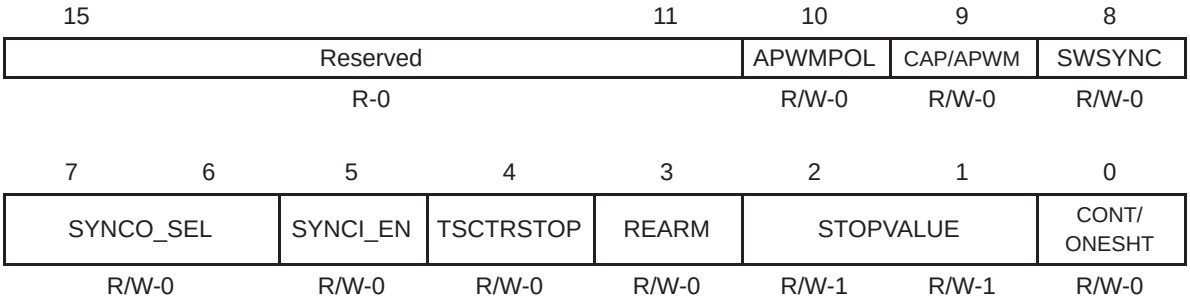


Table 8. ECAP Control Register 2 (ECCTL2) Field Descriptions

Bit(s)	Field	Description
15:11	Reserved	
10	APWMPOL	APWM output polarity select. This is applicable only in APWM operating mode 0 Output is active high (i.e., Compare value defines high time) 1 Output is active low (i.e., Compare value defines low time)
9	CAP/APWM	CAP/APWM operating mode select 0 ECAP module operates in capture mode. This mode forces the following configuration: 1) Inhibits TSCTR resets via CTR=PRD event 2) Inhibits Shadow loads on CAP1 and 2 registers 3) Permits User to enable CAP1−4 register load 4) CAPx/APWMx pin operates as a capture input 1 ECAP module operates in APWM mode. This mode forces the following configuration: 1) Resets TSCTR on CTR=PRD event (period boundary) 2) Permits Shadow loading on CAP1 and 2 registers 3) Disables loading of Time-stamps into CAP1−4 registers 4) CAPx/APWMx pin operates as a APWM output

Table 8. ECAP Control Register 2 (ECCTL2) Field Descriptions (Continued)

Bit(s)	Field	Description
8	SWSYNC	Software-forced Counter (TSCTR) Synchronizing This provides a convenient software method to synchronize some or all ECAP timebases. In APWM mode, the synchronizing can also be done via the CTR=PRD event. 0 Writing a zero has no effect. Reading always returns a zero 1 Writing a one forces a TSCTR shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0,0. After writing a 1, this bit returns to a zero. Note: Selection CTR=PRD is meaningful only in APWM mode, however can still be chosen in CAP mode if you believe it to be useful.
7:6	SYNCO_SEL	Sync-Out Select. 00 Select sync-in event to be the sync-out signal (pass through) 01 Select CTR=PRD event to be the sync-out signal 10 Disable sync out signal 11 Disable sync out signal
5	SYNCI_EN	Counter (TSCTR) Sync-In select mode 0 Disable sync-in option 1 Enable counter (TSCTR) to be loaded from TSCTR register upon either a SYNCI signal or a S/W force event.
4	TSCTRSTOP	Time Stamp (TSCTR) Counter Stop (freeze) Control 0 TSCTR stopped 1 TSCTR free-running
3	RE-ARM	One-Shot Re-Arming Control, i.e. Wait for stop trigger Note: The Re-arm function is valid in ONESHT or continuous mode. 0 Has no effect (reading always returns a 0) 1 Arms the one-shot sequence, i.e.: 1) Resets the Mod4 counter to zero 2) Unfreezes the Mod4 counter 3) Enables capture register loads

Table 8. ECAP Control Register 2 (ECCTL2) Field Descriptions (Continued)

Bit(s)	Field	Description
2:1	STOPVALUE	Stop value for One-Shot mode. This is the number (between 1−4) of captures allowed to occur before the CAP(1−4) registers are frozen, i.e., capture sequence is stopped. 00 Stop after Capture Event 1 01 Stop after Capture Event 2 10 Stop after Capture Event 3 11 Stop after Capture Event 4 Notes: ❑ STOPVALUE is compared to Mod4 counter, when equal, 2 actions occur: 1) Mod4 counter is stopped (frozen) 2) Capture Register Loads are inhibited ❑ In one-shot mode, further interrupt events are blocked until re-armed.
0	CONT/ONESHT	Continuous or one-shot mode control (applicable only in capture mode) 0 Operate in Continuous mode 1 Operate in One-Shot mode

4.1 ECAP Interrupt

Figure 14 shows how the interrupt mechanism works in the eCAP module.

Figure 14. Interrupts in eCAP Module

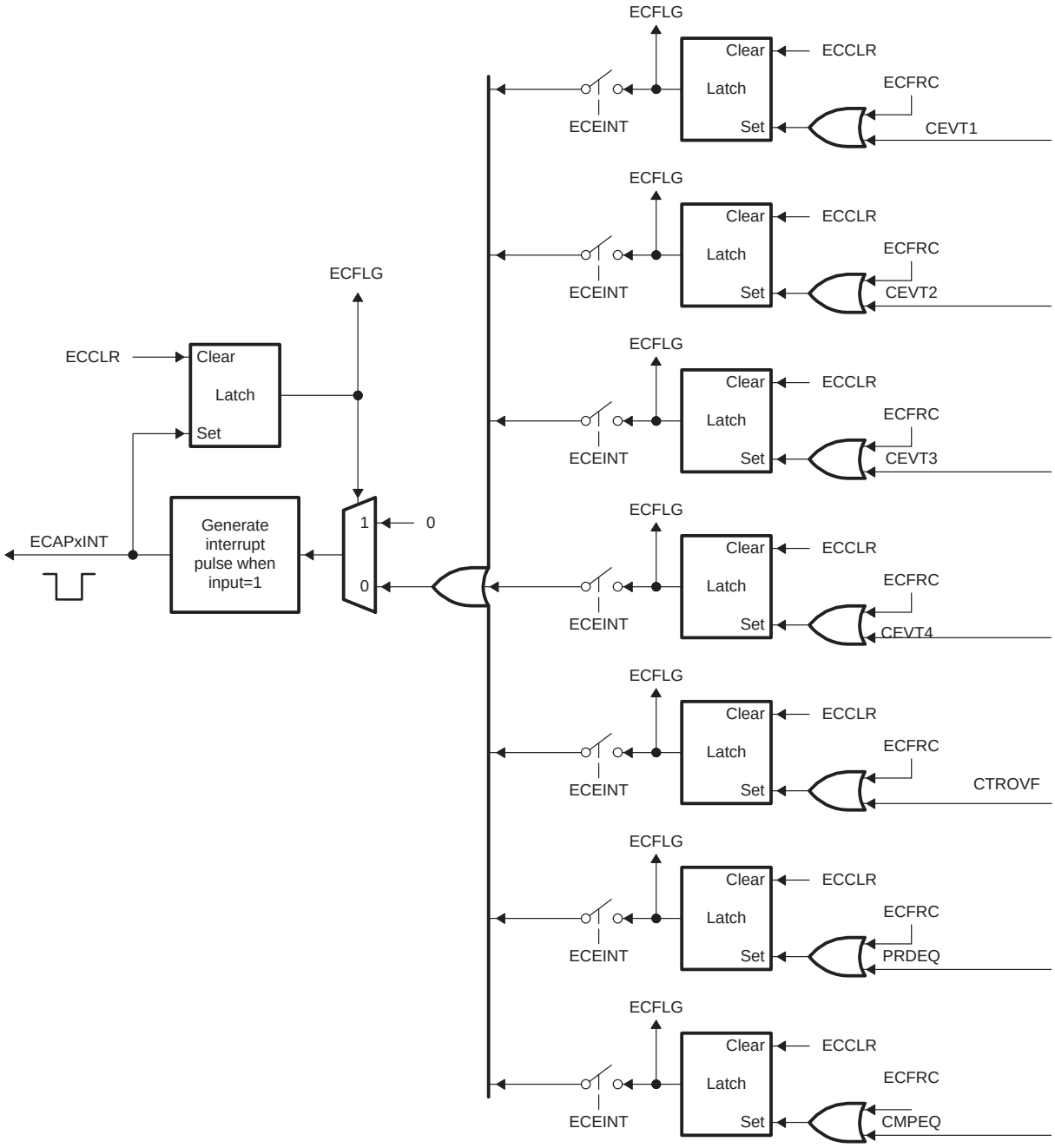


Figure 15. ECAP Interrupt Enable Register (ECEINT)

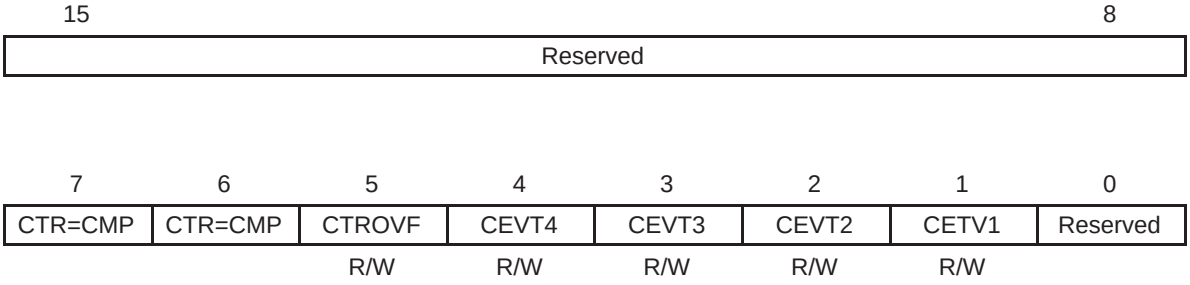


Table 9. ECAP Interrupt Enable Register (ECEINT) Field Descriptions

Bits	Field	Description
15:8	Reserved	
7	CTR=CMP	Counter Equal Compare Interrupt Enable
		0 Disable Compare Equal as an Interrupt source
		1 Enable Compare Equal as an Interrupt source
6	CTR=CMP	Counter Equal Compare Interrupt Enable
		0 Disable Compare Equal as an Interrupt source
		1 Enable Compare Equal as an Interrupt source
5	CTROVF	Counter Overflow Interrupt Enable
		0 Disabled counter Overflow as an Interrupt source
		1 Enable counter Overflow as an Interrupt source
4	CEVT4	Capture Event 4 Interrupt Enable
		0 Disable Capture Event 1 as an Interrupt source
		1 Capture Event 4 Interrupt Enable
3	CEVT3	Capture Event 3 Interrupt Enable
		0 Disable Capture Event 1 as an Interrupt source
		1 Enable Capture Event 1 as an Interrupt source
2	CEVT2	Capture Event 2 Interrupt Enable
		0 Disable Capture Event 1 as an Interrupt source
		1 Enable Capture Event 1 as an Interrupt source

Table 9. ECAP Interrupt Enable Register (ECEINT) Field Descriptions (Continued)

Bits	Field	Description
1	CEVT1	Capture Event 1 Interrupt Enable 0 Disable Capture Event 1 as an Interrupt source 0 Enable Capture Event 1 as an Interrupt source
0	Reserved	

The interrupt enable bits (CEVT1, ...) block any of the selected events from generating an interrupt. Events will still be latched into the flag bit (ECFLG register) and can be forced/cleared via the ECFRC/ECCLR registers.

The proper procedure for configuring peripheral modes and interrupts is as follows:

1) Disable global interrupts
2) Stop eCAP counter
3) Disable eCAP interrupts
4) Configure peripheral registers
5) Clear spurious eCAP interrupt flags
6) Enable eCAP interrupts
7) Start eCAP counter
8) Enable global interrupts

Figure 16. ECAP Interrupt Flag Register (ECFLG)

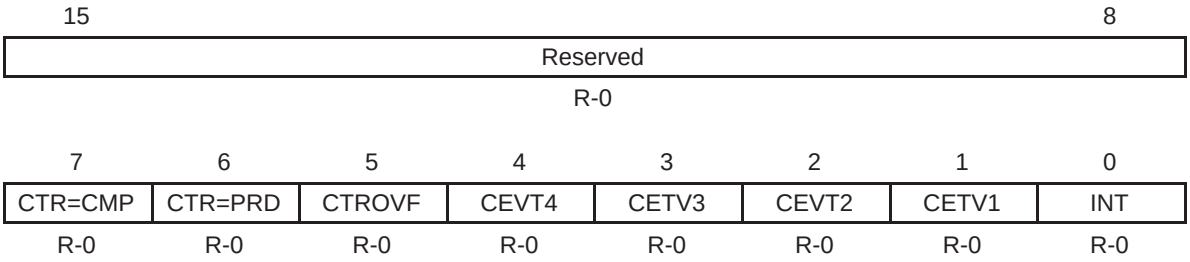


Table 10. ECAP Interrupt Flag Register (ECFLG) Field Descriptions

Bits	Field	Reset	Description
15:8	Reserved		
7	CTR=CMP	Compare Equal Compare Status Flag. This flag is active only in APWM mode.	
		0	Indicates no event occurred
		1	Indicates the counter (TSCTR) reached the compare register value (ACMP)
6	CTR=PRD	Counter Equal Periodl Status Flag. This flag is only active in APWM mode.	
		0	Indicates no event occurred
		1	Indicates the counter (TSCTR) reached the period register value (APER) and was reset.
5	CTROVF	Counter Overflow Status Flag. This flag is active in CAP and APWM mode.	
		0	Indicates no event occurred.
		1	Indicates the counter (TSCTR) has made the transition from FFFFFFFF → 00000000
4	CEVT4	Capture Event 4 Status Flag This flag is only active in CAP mode.	
		0	Indicates no event occurred
		1	Indicates the fourth event occurred at ECAPx pin
3	CEVT3	Capture Event 3 Status Flag. This flag is active only in CAP mode.	
		0	Indicates no event occurred.
		1	Indicates the third event occurred at ECAPx pin.
2	CEVT2	Capture Event 2 Status Flag. This flag is only active in CAP mode.	
		0	Indicates no event occurred.
		1	Indicates the second event occurred at ECAPx pin.

Table 10. ECAP Interrupt Flag Register (ECFLG) Field Descriptions (Continued)

Bits	Field	Reset	Description
1	CEVT1	Capture Event 1 Status Flag. This flag is only active in CAP mode.	
		0	Indicates no event occurred.
		1	Indicates the first event occurred at ECAPx pin.
0	INT	Global Interrupt Status Flag	
		0	Indicates no interrupt generated.
		1	Indicates that an interrupt was generated.

Note: If the event interrupts are enabled (via the ECEINT register) and any one of the above event flags are set to 1 and the INT flag is 0, then an interrupt pulse is generated and the INT flag is set to 1. No further interrupt pulses are generated. Further interrupt pulses are only generated if the INT flag bit is cleared (via the ECCLR register) and one or more event flag bits are set to 1. If all event flag bits are manually cleared, then no further pulses are generated.

Figure 17. ECAP Interrupt Clear Register (ECCLR)

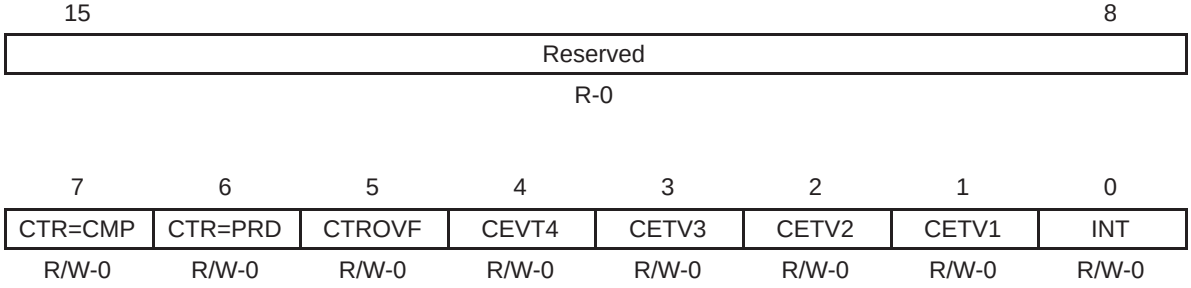


Table 11. ECAP Interrupt Clear Register (ECCLR) Field Descriptions

Bits	Field	Description
15:8	Reserved	
7	CTR=CMP	Counter Equal Compare Status Flag
		0 Writing a 0 has no effect. Always reads back a 0
		1 Writing a 1 clears the CTR=CMP flag condition
6	CTR=PRD	Counter Equal Period Status Flag
		0 Writing a 0 has no effect. Always reads back a 0
		1 Writing a 1 clears the CTR=PRD flag condition

Table 11. ECAP Interrupt Clear Register (ECCLR) Field Descriptions (Continued)

Bits	Field	Description
5	CTROVF	Counter Overflow Status Flag
		0 Writing a 0 has no effect. Always reads back a 0
		1 Writing a 1 clears the CTROVF flag condition
4	CEVT4	Capture Event 4 Status Flag
		0 Writing a 0 has no effect. Always reads back a 0.
		1 Writing a 1 clears the CEVT3 flag condition.
3	CEVT3	Capture Event 3 Status Flag
		0 Writing a 0 hasno effect. Always reads back a 0.
		1 Writing a 1 clears the CEVT3 flag condition.
2	CEVT2	Capture Event 2 Status Flag
		0 Writing a 0 has no effect. Always reads back a 0.
		0 Writing a 1 clears the CEVT2 flag condition.
1	CEVT1	Capture Event 1 Status Flag
		0 Writing a 0 has no effect. Always reads back a 0.
		1 Writing a 1 clears the CEVT1 flag condition.
0	INT	Global Interrupt Clear Flag
		0 Writing a 0 has no effect. Always reads back a 0.
		1 Writing a 1 clears the INT flag and enable further interrupts to be generated if any of the event flags are set to 1.

Figure 18. ECAP Interrupt Forcing Register (ECFRC)

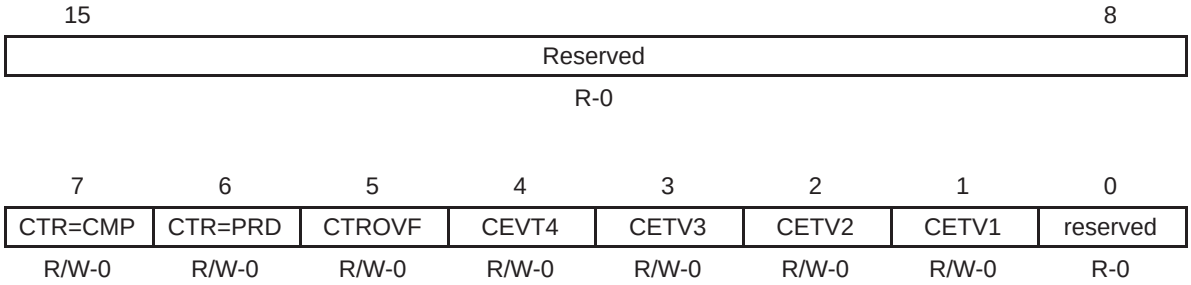


Table 12. ECAP Interrupt Forcing Register (ECFRC) Field Descriptions

Bits	Field	Reset	Description
15:8	Reserved	0:0	
7	CTR−CMP	Force Counter Equal Compare Interrupt	
		0	No effect. Always reads back a 0.
		1	Writing a 1 sets the CTR=CMP flag bit.
6	CTR=PRD	Force Counter Equal Period Interrupt	
		0	No effect. Always reads back a 0.
		1	Writing a 1 sets the CTR=PRD flag bit.
5	CTROVF	Force Counter Overflow	
		0	No effect. Always reads back a 0.
		1	Writing a 1 to this bit sets the CTROVF flag bit.
4	CEVT4	Force Capture Event 4	
		0	No effect. Always reads back a 0.
		1	Writing a 1 sets the CEVT4 flag bit
3	CEVT3	Force Capture Event 3	
		0	No effect. Always reads back a 0.
		1	Writing a 1 sets the CEVT3 flag bit
2	CEVT2	Force Capture Event 2	
		0	No effect. Always reads back a 0.
		1	Writing a 1 sets the CEVT2 flag bit.

Table 12. ECAP Interrupt Forcing Register (ECFRC) Field Descriptions (Continued)

Bits	Field	Reset	Description
1	CEVT1	Force Capture Event 1	
		0	No effect. Always reads back a 0.
		0	Sets the CEVT1 flag bit.
0	reserved	0	

Note: Writing a 1 in any of the above bits causes the respective flag bit to be set to 1. An interrupt pulse is only generated to the PIE if the INT flag bit is 0 before the write. As soon as the interrupt pulse is generated, the INT flag bit is set to 1. If the INT flag bit was already 1 before the operation, then no interrupt pulse is generated. A pulse is generated if the INT flag bit is cleared (via the ECCLR register) and any of the other flag bits are 1.

5 Register Mapping

The eCAP module control and status register set is given in Table 13.

Table 13. Control and Status Register Set

Name	Offset	Size (x16)	Description
Time Base Module Registers			
TSCTR	0x0000	2	Time-Stamp Counter
CTRPHS	0x0002	2	Counter Phase Offset Value Register
CAP1	0x0004	2	Capture 1 Register
CAP2	0x0006	2	Capture 2 Register
CAP3	0x0008	2	Capture 3 Register
CAP4	0x000A	2	Capture 4 Register
reserved	0x000C to 0x0013	8	
ECCTL1	0x0014	1	Capture Control Register 1
ECCTL2	0x0015	1	Capture Control Register 2
ECEINT	0x0016	1	Capture Interrupt Enable Register
ECFLG	0x0017	1	Capture Interrupt Flag Register
ECCLR	0x0018	1	Capture Interrupt Clear Register
ECFRC	0x0019	1	Capture Interrupt Force Register
Reserved	0x001A to 0x001F	6	

Note: All 32-bit registers are aligned on even address boundaries and are organized little-endian mode. Least significant 16 bits of 32-bit register located on lowest address (even address).

6 Application of the ECAP Module

6.1 Absolute Time-Stamp Operation Rising Edge trigger

Figure 19 shows an example of continuous capture operation (Mod4 counter wraps around). In this figure, TSCTR counts-up without resetting and capture events are qualified on the rising edge only, this gives period (and frequency) information.

On an event, the TSCTR contents (i.e., time-dtamp) is first captured, then Mod4 counter is incremented to the next state. When the TSCTR reaches FFFFFFFF (i.e. maximum value), it wraps around to 00000000 (not shown in Figure 19), if this occurs, the CTROVF (counter overflow) flag is set, and an interrupt (if enabled) occurs.

Figure 19. Capture Sequence for Absolute Time-stamp and Rising Edge Detect

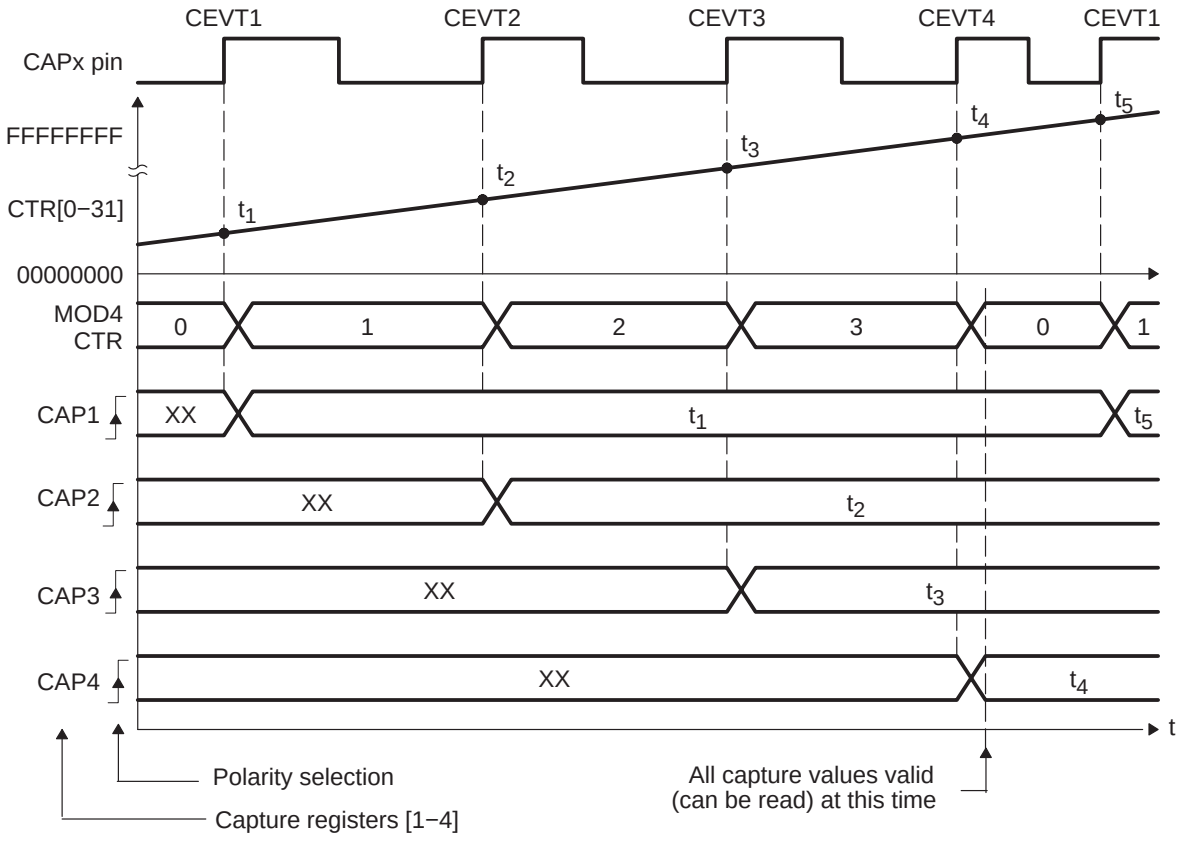
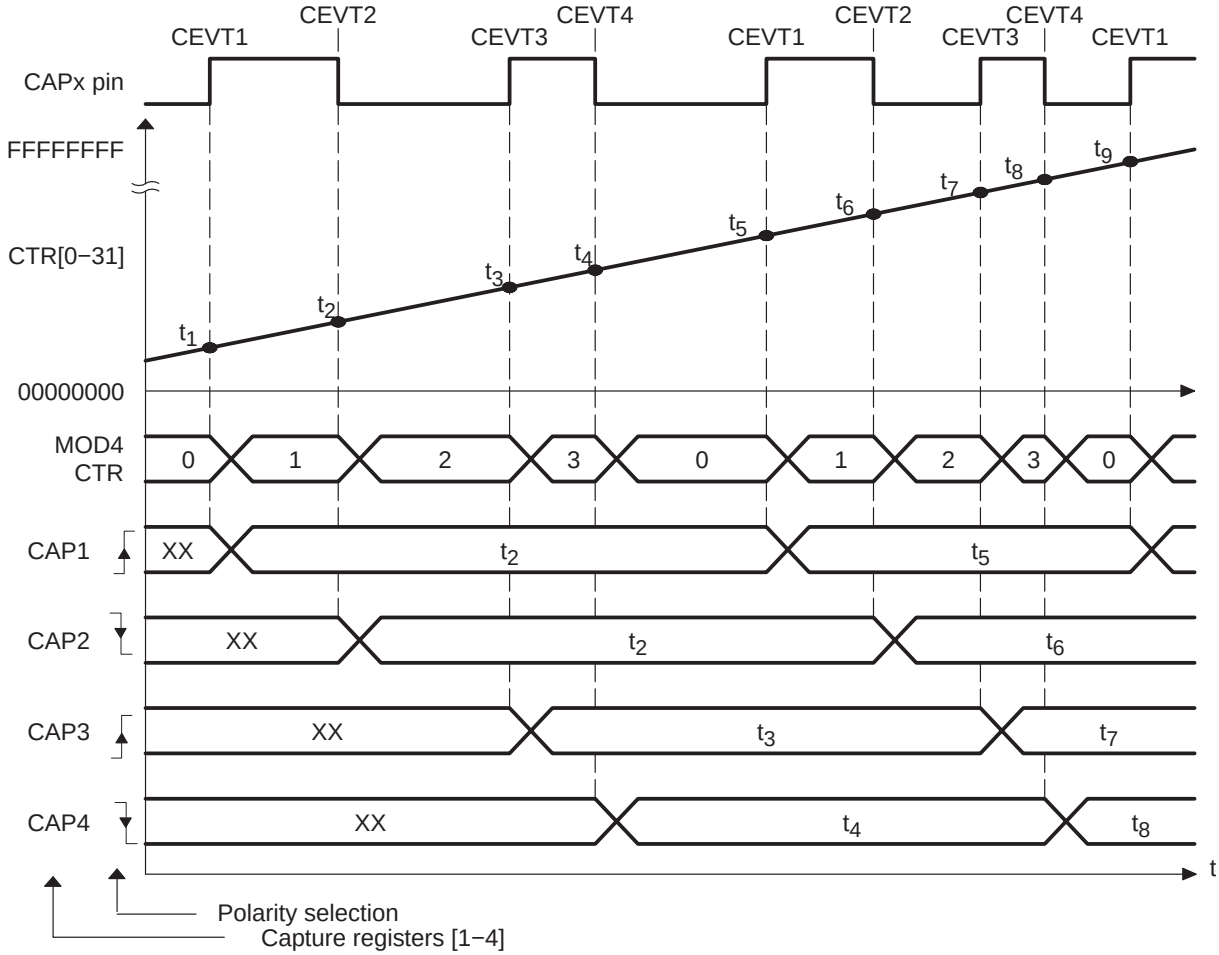


Figure 20. Capture Sequence for Absolute Time-stamp With Rising and Falling Edge Detect



6.2 Time Difference (Delta) Operation

Figure 21. Capture Sequence for Delta Mode Time-stamp and Rising Edge Detect

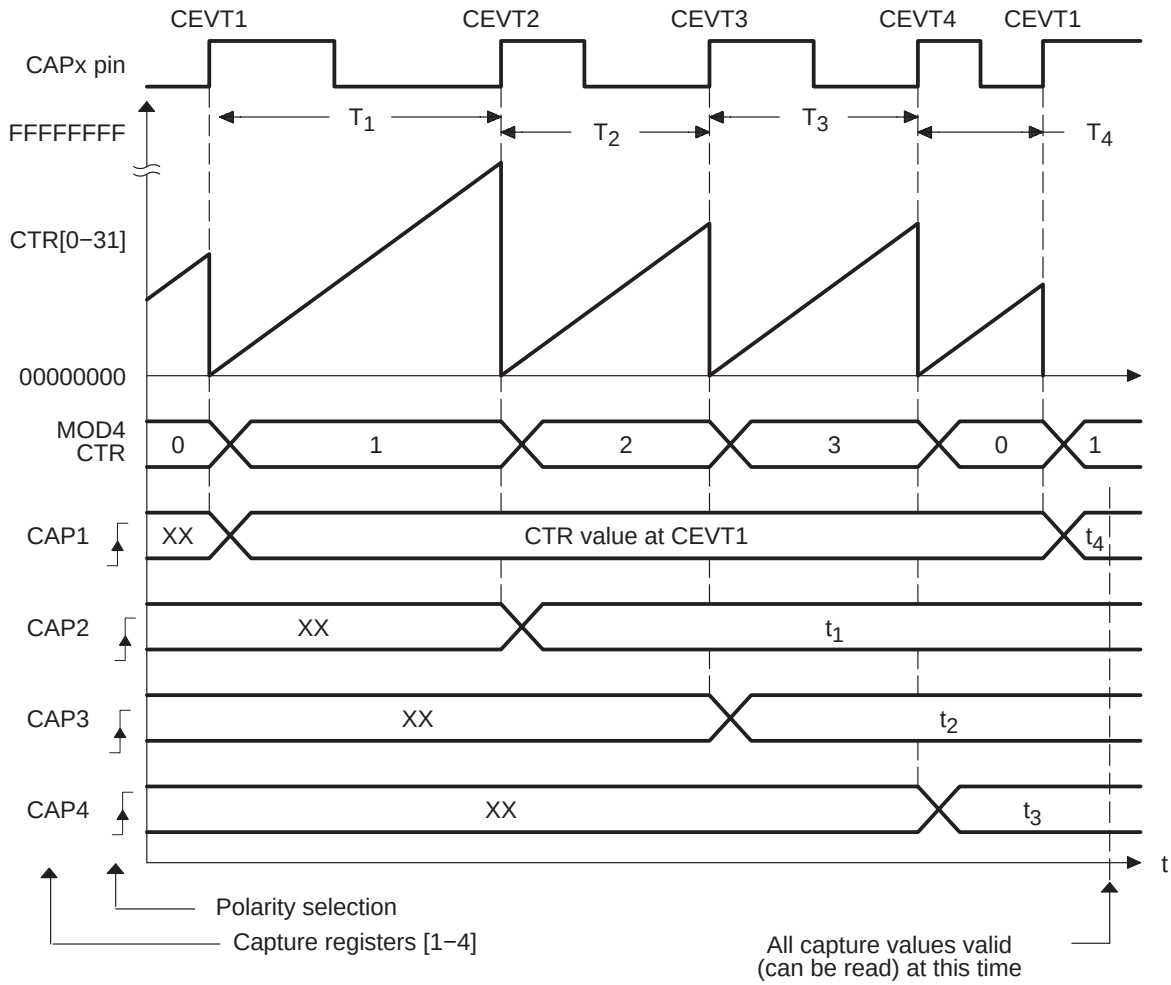


Figure 22. Capture Sequence for Delta Moda Time-stamp With Rising and Falling Edge Detect

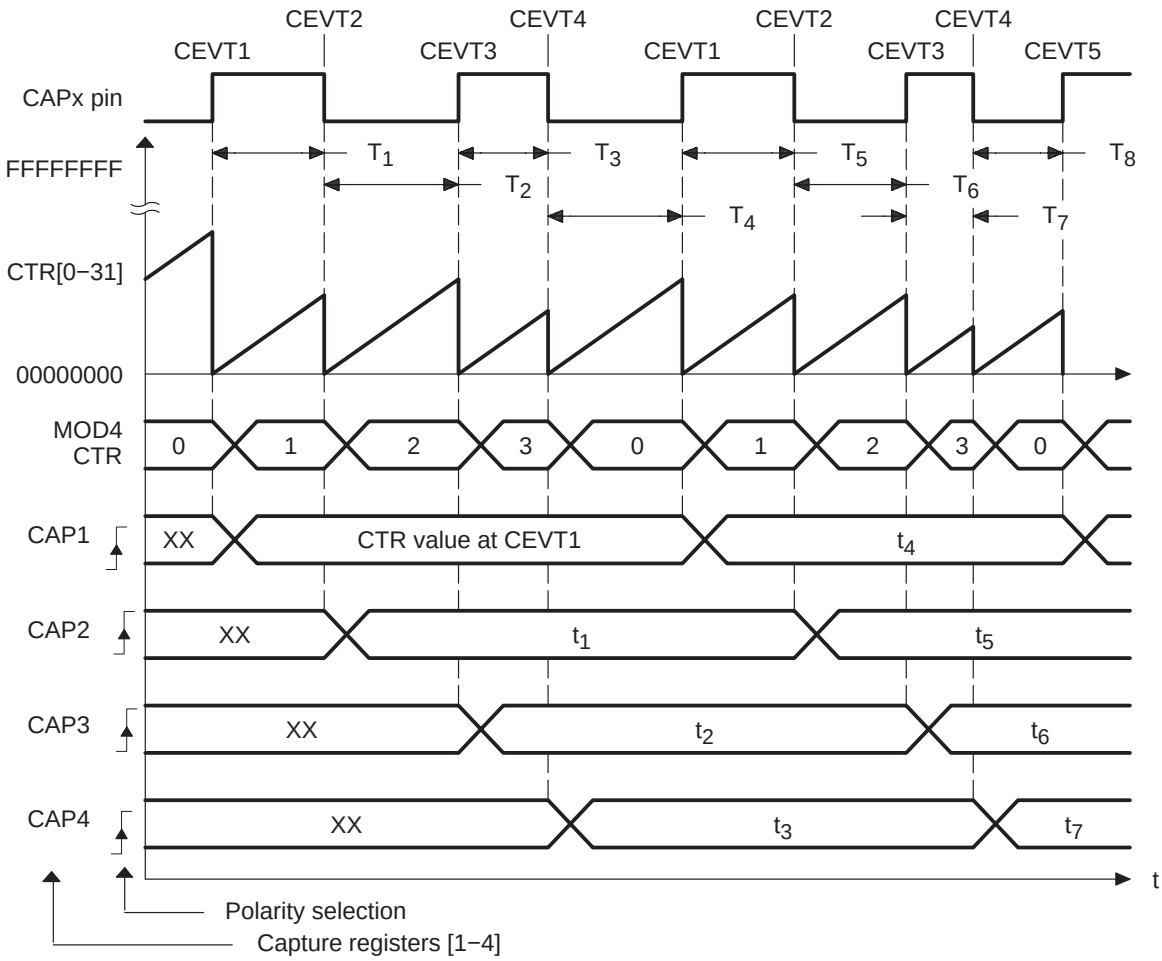
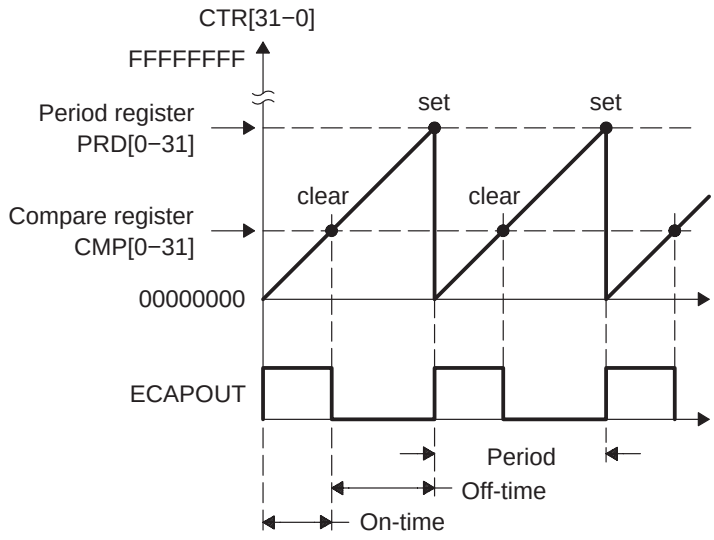


Figure 23. PWM Waveform Details of APWM Mode Operation



During initialization, you must write to the active registers for both period and compare. This will then automatically copy the init values into the shadow values. For subsequent compare updates, i.e. during run-time, only the shadow registers must be used.