TMS320C6000 DSP Power-Down Logic and Modes Reference Guide

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Preface

Read This First

About This Manual

This document describes the power-down logic and modes used by the digital signal processors (DSPs) of the TMS320C6000™ DSP family.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

The following documents describe the C6000™ devices and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

TMS320C6000 CPU and Instruction Set Reference Guide (literature number SPRU189) describes the TMS320C6000™ CPU architecture, instruction set, pipeline, and interrupts for these digital signal processors.

TMS320C6000 DSP Peripherals Overview Reference Guide (literature number SPRU190) describes the peripherals available on the TMS320C6000™ DSPs.

TMS320C6000 Technical Brief (literature number SPRU197) gives an introduction to the TMS320C62x™ and TMS320C67x™ DSPs, development tools, and third-party support.

TMS320C64x Technical Overview (SPRU395) gives an introduction to the TMS320C64x™ DSP and discusses the application areas that are enhanced by the TMS320C64x VelociTI™.

TMS320C6000 Programmer's Guide (literature number SPRU198) describes ways to optimize C and assembly code for the TMS320C6000™ DSPs and includes application program examples.

TMS320C6000 Code Composer Studio Tutorial (literature number SPRU301) introduces the Code Composer Studio™ integrated development environment and software tools.

Code Composer Studio Application Programming Interface Reference Guide (literature number SPRU321) describes the Code Composer Studio™ application programming interface (API), which allows you to program custom plug-ins for Code Composer.

TMS320C6x Peripheral Support Library Programmer's Reference (literature number SPRU273) describes the contents of the TMS320C6000™ peripheral support library of functions and macros. It lists functions and macros both by header file and alphabetically, provides a complete description of each, and gives code examples to show how they are used.

TMS320C6000 Chip Support Library API Reference Guide (literature number SPRU401) describes a set of application programming interfaces (APIs) used to configure and control the on-chip peripherals.

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Power-Down Logic and Modes

This document describes the power-down logic and modes used by the digital signal processors (DSPs) of the TMS320C6000™ DSP family.

1 Overview

Most of the operating power of CMOS logic is dissipated during circuit switching from one logic state to another. By preventing some or all of the device logic from switching, the power-down modes are used to achieve significant power savings without losing any data or operation context. The three power-down modes, PD1, PD2, and PD3, available on the C6000™ DSP perform this function. In addition to PD1, PD2, and PD3, the C6202(B)/C6203(B) DSP also has a peripheral power-down mode, as discussed in section 4. Table 1 summarizes the differences between the power-down modes in the C6000 devices.

Table 1. Differences in C6000 DSP Power-Down Modes

Device	PD pin on device	Power-down control register (PDCTL)	PWRD field in control status register (CSR)
C6201	Yes	No	Yes
C6202/C6202(B)	Yes	Yes	Yes
C6203(B)	Yes	Yes	Yes
C6204	Yes	No	Yes
C6205	Yes	No	Yes
C6211/C6211(B)	No	No	Yes
C6411	No	No	Yes
C6412	No	No	Yes
C6414/15/16	No	No	Yes
DM640/641	No	No	Yes
DM642	No	No	Yes
C6701	Yes	No	Yes
C6711/6711(B)/6711(C)	No	No	Yes
C6712/6712(C)	No	No	Yes
C6713	No	No	Yes

2 Power-Down Mode Descriptions

Figure 1 shows the power-down logic on a C6000 device. Power-down mode PD1 blocks the internal clock inputs at the boundary of the CPU, preventing most of its logic from switching. PD1 effectively shuts down the CPU. During PD1, DMA/EDMA transactions can proceed between peripherals and internal memory.

Additional power savings are accomplished in power-down mode PD2. During PD2, the entire on-chip clock structure (including multiple buffers) is halted at the output of the PLL (see Figure 1). Power-down mode PD3 is like PD2 but also disconnects the external clock source (CLKIN) from reaching the PLL. Wake-up from PD3 takes longer than wake-up from PD2 because the PLL needs to be re-locked, just as it does following power-up.

On the C620x/C670x DSP, both the PD2 and PD3 signals also assert the PD pin for external recognition of these two power-down modes. Although the C621x/C671x/C64x DSP has power-down modes identical to the other devices, there is no PD pin driven externally. In addition to power-down modes described in this document, the IDLE instruction provides lower CPU power consumption by executing continuous NOPs. The IDLE instruction terminates only upon servicing an interrupt. PD2 and PD3 modes are only aborted by device reset. Table 2 summarizes all the power-down modes.

Figure 1. Power-Down Logic

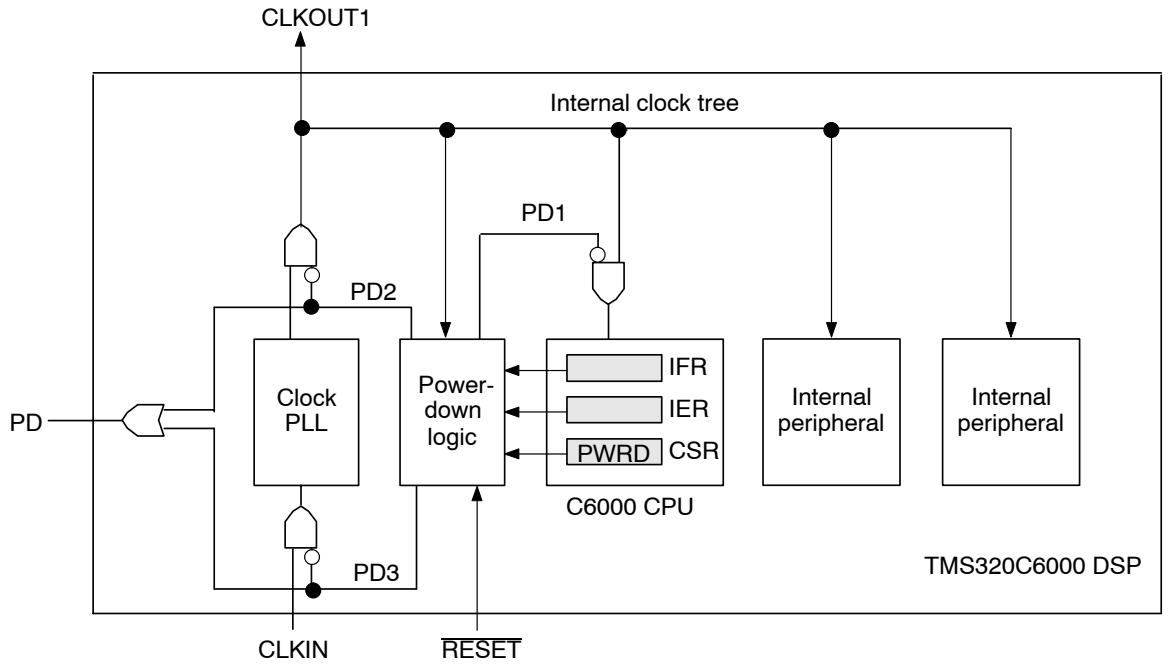


Table 2. Power-Down Modes

Power-down mode	Trigger action	Wake-up method	Effect on device operation
PD1	Write 001001b or 010001b to bits 15–10 of CSR	Internal interrupt, external interrupt, or Reset	CPU halted (except for the interrupt logic)
PD2	Write 011010b to bits 15–10 of CSR	Reset only	Output clock from PLL is halted, stopping the internal clock structure from switching and resulting in the entire device being halted. Signal terminal PD is driven high. All register and internal RAM contents are preserved. All functional I/O “freeze” in the last state when the PLL clock is turned off.†
PD3	Write 11100b to bits 15–10 of CSR	Reset only	Input clock to PLL stops generating clocks. Signal terminal PD is driven high. All register and internal RAM contents are preserved. All functional I/O “freeze” in the last state when the PLL clock is turned off. Following reset, the PLL needs time to re-lock, just as it does following power-up.†

† When entering PD2 and PD3, all functional I/O remains in the previous state. However, for peripherals that are asynchronous in nature (HPI) or peripherals with an external clock source (McBSP, XBUS, timers, C621x/C671x/C64x EMIF, UTOPIA, PCI), output signals may transition in response to stimulus on the inputs. Peripheral operation is not assured under these conditions.

3 Triggering, Wake-Up, and Effects

The power-down modes and their wake-up methods are programmed by the PWRD field (bits 15–10) of the control status register (CSR) in the C6000 CPU, shown in Figure 2. The PWRD field of the CSR is shown in Figure 3 and described in Table 3. When writing to CSR, all bits of the PWRD field should be configured at the same time. A logic 0 should be used when writing to the reserved bit (bit 15) of the PWRD field. The CSR is discussed in detail in the *TMS320C6000 CPU and Instruction Set Reference Guide* (SPRU189).

Figure 2. Control Status Register (CSR)

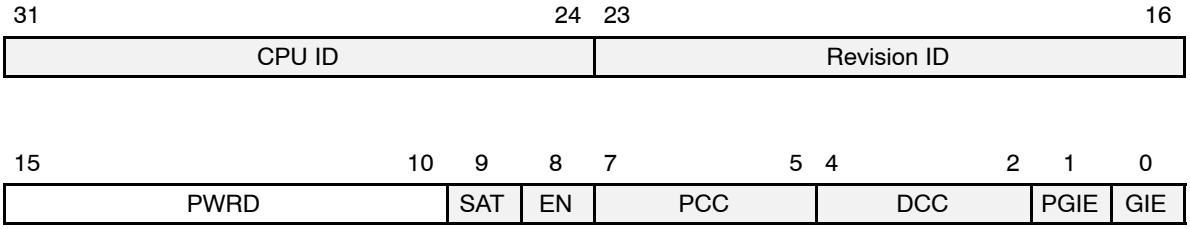


Figure 3. PWRD Field of CSR

15	14	13	12	11	10
Reserved	Enabled or nonenabled interrupt wake	Enabled interrupt wake	PD3	PD2	PD1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R/W = Read/Write; -*n* = value after reset

Note: Refer to the *TMS320C6000 CPU and Instruction Set Reference Guide* (SPRU189) for other bit fields in CSR.

Table 3. Power-Down Mode and Wake-Up Selection

PRWD field	Power-down mode	Wake-up method
00 0000	No power-down	—
00 1001	PD1	Wake by an enabled interrupt.
01 0001	PD1	Wake by an enabled or non-enabled interrupt.
01 1010	PD2	Wake by a device reset.
01 1100	PD3	Wake by a device reset.
other	Reserved	—

Power-down mode PD1 takes effect 8 to 9 clock cycles after the instruction that caused the power down (by setting the PWRD bits in CSR). Use the following code segment to enter power down:

```
                B NextInst          ;branch does not effect program flow, but
                NOP                 ;   hides the move to the CSR in the delay
                                    ;   slots
                MVC Breg, CSR       ;power-down mode is set by this instruction
                NOP
                NOP
                NOP
NextInst:       NOP
                NOP5                ;CPU notifies power-down logic to initiate
                                    ;   power down
                INSTR2              ;normal program execution resumed here
```

The wake-up from PD1 is triggered by either an enabled interrupt or any interrupt (enabled or not enabled). The first case is selected by writing a logic 1 to bit 13 of CSR, and the second case is selected by writing a logic 1 to bit 14 of CSR. If PD1 mode is terminated by a nonenabled interrupt, the program execution returns to the instruction following the NOP 5. Wake-up by an enabled interrupt executes the corresponding interrupt service fetch packet (ISFP) first, prior to returning to the instruction following the NOP 5. The GIE bit in CSR and the NMIE bit in the interrupt enable register (IER) must also be set in order for the ISFP to execute; otherwise, execution returns to the previous point, rather than servicing the interrupt.

4 Peripheral Power-Down Mode for TMS320C6202(B)/C6203(B) DSP

In addition to the power-down modes common to all C6000 devices, the C6202(B)/C6203(B) DSP has the ability to turn off clocks to individual peripherals on the device using the peripheral power-down control register (PDCTL). This feature allows you to selectively turn off peripherals that are not being used for a specific application and save in power consumption for unused peripherals.

This method can have significant savings in power consumption. In a device that is as highly integrated as the C6000 DSP, a significant amount of power is consumed in a reset or no activity state just due to the internal clock distribution. By selectively turning off unused portions of the device, the effects can be minimized.

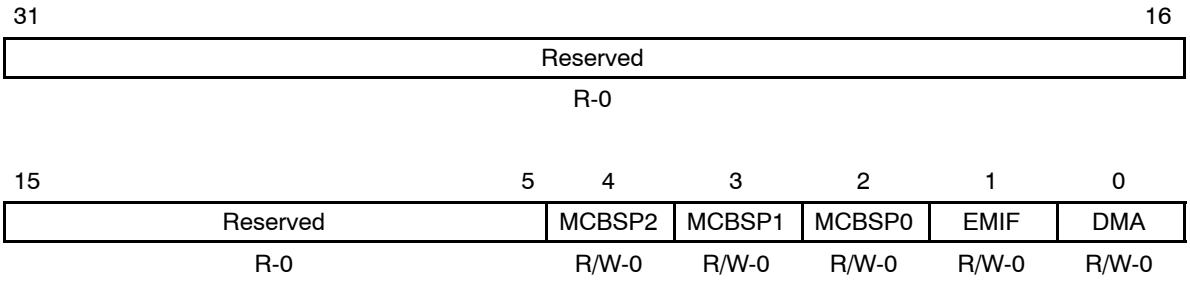
Table 4 shows the PDCTL address location. Figure 4 shows the PDCTL and Table 5 describes the fields.

You must be careful to not disable a portion of the device that is being used, since the peripheral becomes nonoperational once disabled. A clock-off mode can be entered and exited depending on the needs of the application. For example, if an application does not need the serial ports, the ports can be disabled and then reenabled when needed. While a peripheral is in power-down mode, no writes to the peripheral's registers will occur; and reads from the peripheral will produce invalid data.

Table 4. Power-Down Control Register (PDCTL) Address

Byte Address	Abbreviation	Description
019C 0200h	PDCTL	Peripheral power-down control register

Figure 4. Power-Down Control Register (PDCTL) for C6202(B)/C6203(B) DSP



Legend: R = Read only; R/W = Read/Write; -*n* = value after reset

Table 5. Power-Down Control Register (PDCTL) Field Descriptions

Bit	*field*†	*symval*†	Value	Description
31–5	Reserved	–	0	Reserved. The reserved bit location is always read as zero. A value written to this field has no effect.
4	MCBSP2			Internal McBSP2 clock enable bit.
		CLKON	0	Internal McBSP2 clock is enabled.
		CLKOFF	1	Internal McBSP2 clock is disabled. McBSP2 is not functional.
3	MCBSP1			Internal McBSP1 clock enable bit.
		CLKON	0	Internal McBSP1 clock is enabled.
		CLKOFF	1	Internal McBSP1 clock is disabled. McBSP1 is not functional.
2	MCBSP0			Internal McBSP0 clock enable bit.
		CLKON	0	Internal McBSP0 clock is enabled.
		CLKOFF	1	Internal McBSP0 clock is disabled. McBSP1 is not functional.
1	EMIF			Internal EMIF clock enable bit.
		CLKON	0	Internal EMIF clock is enabled.
		CLKOFF	1	Internal EMIF clock is disabled. EMIF is not functional.
0	DMA			Internal DMA clock enable bit.
		CLKON	0	Internal DMA clock is enabled.
		CLKOFF	1	Internal DMA clock is disabled. DMA is not functional.

† For CSL implementation, use the notation PWR_PDCTL_*field_symval*

When reenabling any of the PDCTL bits, the CPU should wait at least 5 additional clock cycles before attempting to access that peripheral. This delay can be accomplished with a NOP 5 instruction after any write to PDCTL, as shown in Example 1.

Example 1. Assemble Code for Initializing Peripheral Power-Down Control Register

```
MVK   0x019C0200, Dest_Ptr_Reg
MVKH  0x019C0200, Dest_Ptr_Reg
STW   SrcReg,   *Dest_Ptr_Reg
NOP   5
```