TMS320x280x DSP System Control and Interrupts Reference Guide

Literature Number: SPRU712
November 2004

Texas Instruments

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Preface

Read This First

About This Manual

This reference guide is applicable for the systems control and interrupts found on the TMS320x280x family of processors. This includes all Flash-based, ROM-based, and RAM-based devices within the 280x family.

This guide describes how various 280x digital signal processor (DSP) system controls and interrupts work with peripherals. It includes information on the:

- ❑ Flash and one-time programmable (OTP) memories
- ❑ Code security module (CSM), which is a security feature incorporated in 28x devices.
- ❑ Clocking mechanisms including the oscillator, PLL, the watchdog function, and the low-power modes.
- ❑ GPIO MUX registers used to select the operation of shared pins on the 280x devices.
- ❑ Peripheral frames and the device emulation registers.
- ❑ Peripheral interrupt expansion (PIE) block that multiplexes numerous interrupt sources into a smaller set of interrupt inputs.

Related Documentation From Texas Instruments

The following books describe the TMS320x280x and related support tools that are available on the TI website:

TMS320F2801, TMS320F2806, TMS320F2808 Digital Signal Processors (literature number SPRS230) data sheet contains the pinout, signal descriptions, as well as electrical and timing specifications for the F280x devices.

TMS320C28x DSP CPU and Instruction Set Reference Guide (literature number SPRU430) describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x™ fixed-point digital signal processors (DSPs). It also describes emulation features available on these DSPs.

TMS320x280x Analog-to-Digital Converter (ADC) Reference Guide (literature number SPRU716) describes the ADC module. The module is a 12−bit pipelined ADC. The analog circuits of this converter, referred to as the core in this document, include the front-end analog multiplexers (MUXs), sample−and−hold (S/H) circuits, the conversion core, voltage regulators, and other analog supporting circuits. Digital circuits, referred to as the wrapper in this document, include programmable conversion sequencer, result registers, interface to analog circuits, interface to device peripheral bus, and interface to other on-chip modules.

TMS320x280x Boot ROM Reference Guide (literature number SPRU722) describes the purpose and features of the bootloader (factory-programmed boot-loading software). It also describes other contents of the device on-chip boot ROM and identifies where all of the information is located within that memory.

TMS320x281x, 280x Enhanced Controller Area Network (eCAN) Reference Guide (literature number SPRU074) describes the eCAN that uses established protocol to communicate serially with other controllers in electrically noisy environments. With 32 fully configurable mailboxes and time-stamping feature, the eCAN module provides a versatile and robust serial communication interface. The eCAN module implemented in the C28x DSP is compatible with the CAN 2.0B standard (active).

TMS320x281x, 280x Peripheral Reference Guide (literature number SPRU566) describes the peripheral reference guides of the 28x digital signal processors (DSPs).

TMS320x281x, 280x Serial Communication Interface (SCI) Reference Guide (literature number SPRU051) describes the SCI that is a two-wire asynchronous serial port, commonly known as a UART. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format.

TMS320x280x Enhanced Quadrature Encoder Pulse (eQEP) Reference Guide (literature number SPRU790) describes the eQEP module, which is used for interfacing with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine in high performance moton and position control systems. It includes the module description and registers.

TMS320x281x, 280x Serial Peripheral Interface (SPI) Reference Guide (literature number SPRU059) describes the SPI − a high-speed synchronous serial input/output (I/O) port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmed bit−transfer rate. The SPI is used for communications between the DSP controller and external peripherals or another controller.

TMS320x280x Inter-Integrated Circuit (I^2C) Reference Guide (literature number SPRU721) describes the features and operation of the inter-integrated circuit (I^2C) module that is available on the TMS320x280x digital signal processor (DSP). The I^2C module provides an interface between one of these DSPs and devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus) specification version 2.1 and connected by way of an I^2C-bus.

TMS320x280x Enhanced Capture (eCAP) Module Reference Guide (literature number SPRU807) describes the enhanced Capture Module. It includes the module description and registers.

TMS320x280x Enhanced Pulse Width Modulation (ePWM) Module Reference Guide (literature number SPRU791). The PWM peripheral is an essential part of controlling many of the power related systems found in both commercial and industrial equipments. This guide describes the main areas that include digital motor control, switch mode power supply control, UPS (uninterruptible power supplies), and other forms of power conversion. The PWM peripheral can be considered as performing a DAC function, where the duty cycle is equivalent to a DAC analog value, it is sometimes referred to as a Power DAC.

TMS320C28x DSP/BIOS Application Programming Interface (API) Reference Guide (literature number SPRU625) describes development using DSP/BIOS.

Trademarks

Code Composer Studio and C28x are trademarks of Texas Instruments.

Contents

1 Memory 1-1
Describes Flash and OTP memory.

1.1 Flash and OTP Memory 1-2
1.1.1 Flash Memory 1-2
1.1.2 OTP Memory 1-2
1.2 Flash and OTP Power Modes 1-3
1.2.1 Flash and OTP Performance 1-5
1.2.2 28x Flash Pipeline Mode 1-6
1.2.3 Procedure to Change the Flash Configuration Registers 1-8
1.3 Flash and OTP Registers 1-9

2 Code Security Module (CSM) 2-1
Describes clocking and system control.

2.1 Functional Description 2-2
2.2 CSM Impact on Other On-Chip Resources 2-4
2.3 Incorporating Code Security in User Applications 2-6
2.3.1 Environments That Require Security Unlocking 2-7
2.3.2 Password Match Flow 2-8
2.3.3 Unsecuring Considerations for Devices With/Without Code Security 2-10
2.3.4 C Code Example to Unsecure 2-11
2.3.5 C Code Example to Resecure 2-12
2.4 Do's and Don'ts to Protect Security Logic 2-13
2.4.1 Do's 2-13
2.4.2 Don'ts 2-13
2.5 CSM Features − Summary 2-14

3 Clocking 3-1
Describes clocking and system control.

3.1 Clocking and System Control 3-2
3.2 OSC and PLL Block 3-13
3.2.1 PLL-Based Clock Module 3-13
3.2.2 Main Oscillator Fail Detection 3-14
3.2.3 XCLKOUT Generation 3-16
3.2.4 PLL Clock-in (PLLCR) Register 3-17
3.2.5 External Reference Oscillator Clock Option 3-17
3.3 Low-Power Modes Block 3-23
3.4 Watchdog Block 3-26
3.4.1 Emulation Considerations 3-29
3.5 32-Bit CPU Timers 0/1/2 3-30

4 General-Purpose Input/Output (GPIO) 4-1
Describes GPIO shared pins and operation selection.

4.1 GPIO Module Overview 4-2
4.2 Input Qualification 4-4
4.3 Configuration Overview 4-6
4.4 GPIO and Peripheral MUXing 4-10
4.5 Register Bit Definitions 4-23

5 Peripheral Frames 5-1
Describes how to configure 28x systems for peripherals.

5.1 Peripheral Frame Registers 5-2
5.2 EALLOW-protected Registers 5-6
5.3 Device Emulation Registers 5-14
5.4 Write-Followed-by-Read Protection 5-16

6 Peripheral Interrupt Expansion (PIE) 6-1
Describes the peripheral interrupt expansion (PIE).

6.1 Overview of the PIE Controller 6-2
6.2 Vector Table Mapping 6-6
6.3 Interrupt Sources 6-9
6.3.1 Procedure for Handling Multiplexed Interrupts 6-10
6.3.2 Procedures for Enabling And Disabling Multiplexed Peripheral Interrupts . . 6-11
6.3.3 Flow of a Multiplexed Interrupt Request From a Peripheral to the CPU 6-13
6.3.4 The PIE Vector Table 6-15
6.4 PIE Configuration Registers 6-24
6.5 PIE Interrupt Registers 6-26
6.5.1 PIE Interrupt Flag Registers 6-27
6.5.2 PIE Interrupt Enable Registers 6-28
6.5.3 CPU Interrupt Flag Register (IFR) 6-29
6.5.4 Interrupt Enable Register (IER) and Debug Interrupt Enable Register (DBGIER) 6-33
6.6 External Interrupt Control Registers 6-39

Figures

1−1 Flash Power Mode State Diagram 1-4
1−2 Flash Pipeline 1-7
1−3 Flash Configuration Access Flow Diagram 1-8
1−4 Flash Options Register (FOPT) 1-10
1−5 Flash Power Register (FPWR) 1-11
1−6 Flash Status Register (FSTATUS) 1-12
1−7 Flash Standby Wait Register (FSTDBYWAIT) 1-13
1−8 Flash Standby to Active Wait Counter Register (FACTIVEWAIT) 1-14
1−9 Flash Waitstate Register (FBANKWAIT) 1-15
1−10 OTP Waitstate Register (FOTPWAIT) 1-16
2−1 CSM Status and Control Register (CSMSCR) 2-7
2−2 Password Match Flow (PMF) 2-9
3−1 Clock and Reset Domains 3-2
3−2 Peripheral Clock Control 0 Register (PCLKCR0) 3-4
3−3 Peripheral Clock Control 1 Register† (PCLKCR1) 3-7
3−4 System Control and Status Register (SCSR) 3-10
3−5 High-Speed Peripheral Clock Prescaler (HISPCP) Register 3-11
3−6 Low-Speed Peripheral Clock Prescaler Register (LOSPCP) 3-12
3−7 OSC and PLL Block 3-13
3−8 Oscillator Fail-Detection Logic Diagram 3-15
3−9 XCLKOUT Generation 3-16
3−10 PLLCR Change Procedure Flow Chart 3-18
3−11 PLLCR Register Layout 3-19
3−12 PLL Status Register (PLLSTS) 3-20
3−13 XCLKOUT Register (XCLK) 3-22
3−14 Low Power Mode Control 0 Register (LPMCR0) 3-25
3−15 Watchdog Module 3-26
3−16 Watchdog Counter Register (WDCNTR) 3-27
3−17 Watchdog Reset Key Register (WDKEY) 3-27
3−18 Watchdog Control Register (WDCR) 3-28
3−19 CPU-Timers 3-30
3−20 CPU-Timer Interrupts Signals and Output Signal 3-30
3−21 TIMERxTIM Register 3-32
3−22 TIMERxTIMH Register 3-32
3−23 TIMERxPRD Register 3-33
3−24 TIMERxPRDH Register 3-33
3−25 TIMERxTCR Register 3-34
3−26 TIMERxTPR Register 3-35
3−27 TIMERxTPRH Register 3-35

4−1 Modes of Operation 4-3
4−2 Input Qualification 4-4
4−3 Input Qualifier Clock Cycles 4-5
5−1 Device Configuration (DEVICECNF) Register 5-14
5−2 DEVICEID Register 5-15
6−1 Overview: Multiplexing of Interrupts Using the PIE Block 6-2
6−2 Typical PIE/CPU Interrupt Response − INTx.y 6-4
6−3 Reset Flow Diagram 6-8
6−4 External and PIE Interrupt Sources 6-9
6−5 Multiplexed Interrupt Request Flow Diagram 6-13
6−6 PIE Interrupt Acknowledge Register (PIEACKx) Register-Address CE1 6-26
6−7 PIEIFRx Register (x = 1 to 12) 6-27
6−8 PIEIERx Register (x = 1 to 12) 6-28
6−9 Interrupt Flag Register (IFR) — CPU Register 6-30
6−10 Interrupt Enable Register (IER) — CPU Register 6-33
6−11 Debug Interrupt Enable Register (DBGIER) — CPU Register 6-36
6−12 External Interrupt 1 Control Register (XINT1CR) — Address 7070h 6-39
6−13 External Interrupt 2 Control Register (XINT2CR) — Address 7071h 6-40
6−14 External NMI Interrupt Control Register (XNMICR) — Address 7077h 6-41
6−15 External Interrupt 1 Counter (XINT1CTR) — Address 7078h 6-42
6−16 External Interrupt 2 Counter (XINT2CTR) — Address 7079h 6-43
6−17 External NMI Interrupt Counter (XNMICTR) — Address 707Fh 6-43

Tables

1−1 Flash/OTP Configuration Registers 1-9
1−2 Flash Options Register (FOPT) Field Descriptions 1-10
1−3 Flash Power Register (FPWR) Field Descriptions 1-11
1−4 Flash Status Register (FSTATUS) Field Descriptions 1-12
1−5 Flash Standby Wait Register (FSTDBYWAIT) Field Descriptions 1-13
1−6 Flash Standby to Active Wait Counter Register (FACTIVEWAIT) Field Descriptions . . . 1-14
1−7 Flash Waitstate Register (FBANKWAIT) Field Descriptions 1-15
1−8 OTP Waitstate Register (FOTPWAIT) Field Descriptions 1-16
2−1 Security Levels 2-2
2−2 280x Resources Affected by the CSM 2-4
2−3 280x Resources Not Affected by the CSM 2-5
2−4 Code Security Module (CSM) Registers 2-6
2−5 CSM Status and Control Register (CSMSCR) Field Descriptions 2-7
3−1 PLL, Clocking, Watchdog, and Low-Power Mode Registers 3-3
3−2 Peripheral Clock Control 0 Register (PCLKCR0) Field Descriptions 3-4
3−3 Peripheral Clock Control 1 Register (PCLKCR1) Field Descriptions 3-7
3−4 System Control and Status Register (SCSR) Field Descriptions 3-10
3−5 High-Speed Peripheral Clock Prescaler (HISPCP) Field Descriptions 3-11
3−6 Low-Speed Peripheral Clock Prescaler Register (LOSPCP) Field Descriptions 3-12
3−7 Possible PLL Configuration Modes 3-14
3−8 PLLCR Bit Descriptions 3-19
3−9 PLL Status Register (PLLSTS) Field Descriptions 3-20
3−10 XCLKOUT Register (XCLK) Field Descriptions 3-22
3−11 280x Low-Power Modes 3-23
3−12 Low Power Modes 3-24
3−13 Low Power Mode Control 0 Register (LPMCR0) Field Descriptions 3-25
3−14 Watchdog Counter Register (WDCNTR) Field Descriptions 3-27
3−15 Watchdog Reset Key Register (WDKEY) Field Descriptions 3-27
3−16 Watchdog Control Register (WDCR) Field Descriptions 3-28
3−17 CPU-Timers 0, 1, 2 Configuration and Control Registers 3-31
3−18 TIMERxTIM Register Field Descriptions 3-32
3−19 TIMERxTIMH Register Field Description 3-32
3−20 TIMERxPRD Register Field Description 3-33
3−21 TIMERxPRDH Register Field Description 3-33
3−22 TIMERxTCR Register Field Descriptions 3-34
3−23 TIMERxTPR Register Field Descriptions 3-35

3−24 TIMERxTPRH Register Field Descriptions 3-35
4−1 GPIO Control Registers 4-8
4−2 GPIO Data Registers 4-9
4−3 GPIO Interrupt and Low Power Mode Select Registers 4-9
4−4 Default State of Peripheral Input 4-11
4−5 2808 GPIO MUX Table 4-12
4−6 2806 GPIO MUX Table 4-14
4−7 2801 GPIO MUX Table 4-16
4−8 Peripheral to GPIO Cross Reference 4-18
4−9 GPIO Port A MUX 1 (GPAMUX1) Register Bit Descriptions 4-23
4−10 GPIO Port A MUX 2 (GPAMUX2) Register Bit Descriptions 4-26
4−11 GPIO Port B MUX 1 (GPBMUX1) Register Bit Descriptions 4-29
4−12 GPIO Port B MUX 2 (GPBMUX2) Register Bit Descriptions 4-30
4−13 GPIO Port A Qualification Control (GPACTRL) Register Bit Descriptions 4-30
4−14 GPIO Port B Input Qualification Control (GPBCTRL) Register Bit Descriptions 4-31
4−15 GPIO Port A Qualification Select 1 (GPAQSEL1) Register Bit Descriptions 4-32
4−16 GPIO Port A Qualification Select 2 (GPAQSEL2) Register Bit Descriptions 4-33
4−17 GPIO Port B Qualification Select 1 (GPBSEL1) Register Bit Descriptions 4-34
4−18 GPIO Port B Qualification Select 2 (GPBSEL2) Register Bit Descriptions 4-34
4−19 GPIO Port A Direction (GPADIR) Register Bit Descriptions 4-35
4−20 GPIO Port B Direction (GPBDIR) Register Bit Descriptions 4-37
4−21 GPIO Port A Internal Pullup Disable (GPAPUD) Register Bit Descriptions 4-38
4−22 GPIO Port B Internal Pullup Disable (GPBPUD) Register Bit Descriptions 4-39
4−23 GPIO Port A Data (GPADAT) Register Bit Descriptions 4-40
4−24 GPIO Port B Data (GPBDAT) Register Bit Descriptions 4-42
4−25 GPIO Port A Set (GPASET) Register Bit Descriptions 4-42
4−26 GPIO Port B Set (GPBSET) Register Bit Descriptions 4-44
4−27 GPIO Port A Clear (GPACLEAR) Register Bit Descriptions 4-44
4−28 GPIO Port B Clear (GPCLEAR) Register Bit Descriptions 4-46
4−29 GPIO Port A Toggle (GPATOGGLE) Register Bit Descriptions 4-46
4−30 GPIO Port B Clear (GPCLEAR) Register Bit Descriptions 4-48
4−31 GPIO XINT1 Interrupt Select (GPIOXINT1SEL) Register Bit Descriptions 4-48
4−32 GPOIO XINT2 Interrupt Select (GPIOXINT2SEL) Register Bit Descriptions 4-49
4−33 GPIO XNMI Interrupt Select (GPIOXNMISEL) Register Bit Descriptions 4-49
4−34 GPIO Low Power Mode Wakeup Select (GPIOLPMSEL) Register Bit Descriptions 4-50
5−1 Peripheral Frame 0 Registers 5-2
5−2 Peripheral Frame 1 Registers 5-3
5−3 Peripheral Frame 2 Registers 5-5
5−4 Access to EALLOW-protected Registers 5-6
5−5 EALLOW-protected Device Emulation Registers 5-6
5−6 EALLOW-protected Flash/OTP Configuration Registers 5-7
5−7 EALLOW-protected Code Security Module (CSM) Registers 5-7
5−8 EALLOW-protected PIE Vector Table 5-8
5−9 EALLOW-protected PLL, Clocking, Watchdog, and Low-Power Mode Registers 5-9

5−10 EALLOW-protected GPIO MUX Registers 5-9
5−11 EALLOW-protected eCAN−A Registers 5-10
5−12 EALLOW-protected eCAN−B Registers 5-11
5−13 EALLOW-protected ePWM−1 Registers 5-11
5−14 EALLOW-protected ePWM−2 Registers 5-12
5−15 EALLOW-Protected ePWM−3 Registers 5-12
5−16 EALLOW-Protected ePWM−4 Registers 5-12
5−17 EALLOW-Protected ePWM−5 Registers 5-13
5−18 EALLOW-Protected ePWM−6 Registers 5-13
5−19 Device Emulation Registers 5-14
5−20 DEVICECNF Register Bit Descriptions 5-15
5−21 DEVICEID Register Bit Description 5-15
5−22 PROTSTART and PROTRANGE Registers 5-16
5−23 PROTSTART Valid Values 5-17
5−24 PROTRANGE Valid Values 5-18
6−1 Enabling Interrupt 6-5
6−2 Interrupt Vector Table Mapping 6-6
6−3 Vector Table Mapping After Reset Operation 6-7
6−4 280x PIE Vector Table 6-16
6−5 280x PIE Peripheral Interrupts 6-23
6−6 PIE Configuration and Control Registers 6-24
6−7 PIECTRL Register-Address CE0 6-26
6−8 PIECTRL Bit Descriptions 6-26
6−9 PIEACKx Bit Descriptions 6-26
6−10 PIEIFRx Bit Descriptions 6-27
6−11 PIEIERx Bit Descriptions 6-28
6−12 IFR Bit Descriptions 6-30
6−13 IER Bit Descriptions 6-34
6−14 DBGIER Bit Descriptions 6-36
6−15 XINT1CR Bit Descriptions 6-39
6−16 XINT2CR Bit Descriptions 6-40
6−17 XNMICR Bit Descriptions 6-41
6−18 XNMICR Register Settings and Interrupt Sources 6-42

Chapter 1

Memory

This chapter describes how Flash and one-time programmable (OTP) memories can be used with the 28x digital signal processor (DSP) device and peripherals. It also includes the registers associated with memory.

Topic **Page**

1.1	Flash and OTP Memory	1-2
1.2	Flash and OTP Power Modes	1-3
1.3	Flash and OTP Registers	1-9

1.1 Flash and OTP Memory

This section describes how to configure two kinds of memory − Flash and one-time programmable (OTP).

1.1.1 Flash Memory

The on-chip Flash in Flash devices is uniformly mapped in both program and data memory space. This Flash memory is always enabled on 28x devices and features:

- Multiple sectors
- Code security
- Low power modes
- Configurable waitstates that can be adjusted based on CPU frequency
- Flash pipeline mode for improved performance of linear code execution

1.1.2 OTP Memory

The 1K × 16 block of one-time programmable (OTP) memory can be used to program data or code. This block can be programmed one time and cannot be erased.

1.2 Flash and OTP Power Modes

The following operating states apply to the Flash and OTP memory:

- Reset or Sleep State: This is the state after a device reset. In this state, the bank and pump are in a sleep state (lowest power). A CPU read or fetch accesses to the Flash/OTP memory map area stalls the CPU. This access automatically initiates a change in power modes to the active or read state.
- Standby State: In this state, the bank and pump are in standby power mode state. A CPU read or fetch accesses to the Flash/OTP memory map area stalls the CPU. This access automatically initiates a change in power modes to the active state.
- Active or Read State: In this state, the bank and pump are in active power mode state (highest power). The CPU read or fetch access wait states to the Flash/OTP memory map area is controlled by the FBANKWAIT and FOTPWAIT registers. A prefetch mechanism called Flash pipeline can also be enabled for improving fetch performance for linear code execution.

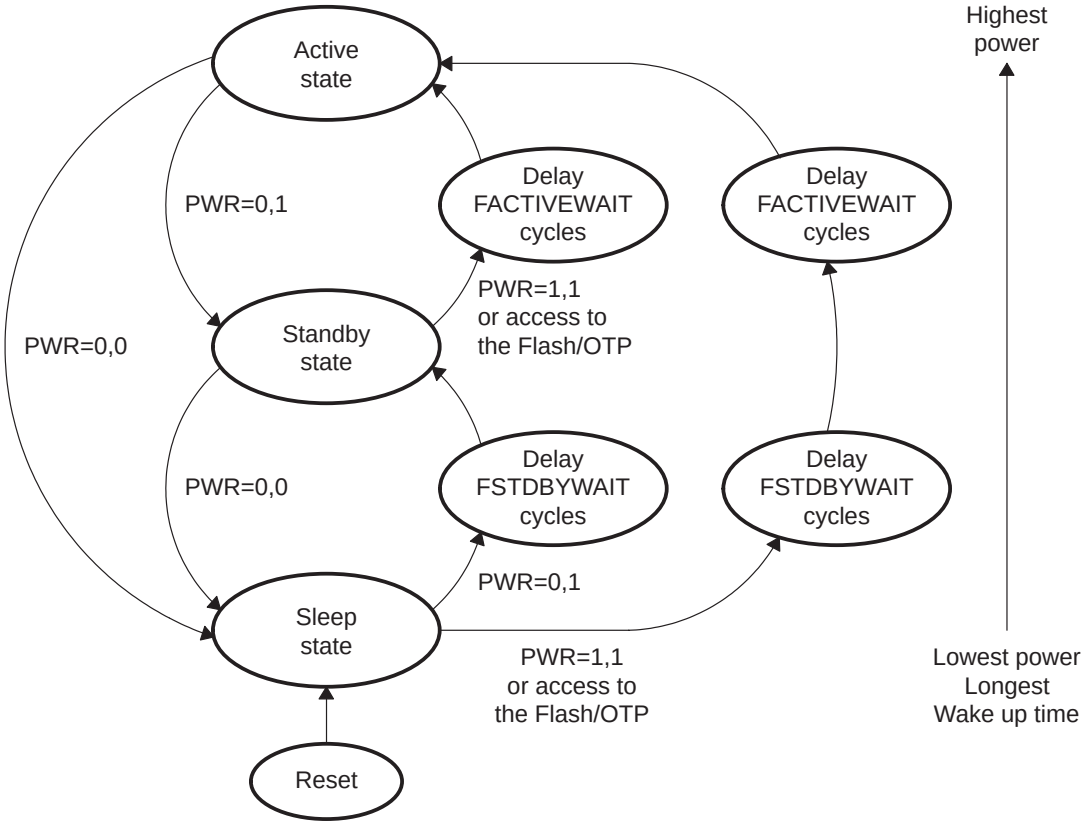
The Flash/OTP bank and pump are always in the same power mode during read or execution operations from the Flash/OTP. See Figure 1−1 for a graphic depiction of the states.

You can change the current Flash/OTP memory power state as follows:

- To move to a lower power state: Change the PWR mode bits from a higher power mode to a lower power mode. This change instantaneously moves the Flash/OTP bank to the lower power state. This register should be accessed only by code running outside the Flash/OTP memory.
- To move from a lower power state to a higher power state, there are two options:
  - Change the FPWR register from a lower state to a higher state. This access brings the Flash/OTP memory to the higher state.
  - Access the Flash or OTP memory by a read access or program fetch access. This access automatically brings the Flash/OTP memory to the active state.

There is a delay when moving from a lower power state to a higher one. See Figure 1−1. This delay is required to allow the Flash to stabilize at the higher power mode. If any access to the Flash/OTP memory occurs during this delay the CPU automatically stalls until the delay is complete.

Figure 1−1. Flash Power Mode State Diagram



The duration of the delay is determined by the FSTDBYWAIT and FACTIVEWAIT registers. Moving from the sleep state to a standby state is delayed by a count determined by the FSTDBYWAIT register. Moving from the standby state to the active state is delayed by a count determined by the FACTIVEWAIT register. Moving from the sleep mode (lowest power) to the active mode (highest power) is delayed by FSTDBYWAIT + FACTIVEWAIT.

1.2.1 Flash and OTP Performance

CPU read or fetch operations to the Flash/OTP can take one of the following forms:

- 32-bit instruction fetch
- 16 or 32-bit data space read
- 16-bit program space read

Once Flash is in the active power state, then a read or fetch access to the bank memory map area can be classified as three types:

- Flash Memory Random Access: The number of wait states, for a random access, is configured by the RANDWAIT bits in the FBANKWAIT register. This register defaults to a worst-case count and the user needs to program the appropriate number of wait states to improve performance based on the CPU clock rate and the access time of the Flash.
- Flash Memory Paged Access: The Flash array is organized into rows and columns. The rows contain 2048 bits of information. The first access to a row is considered a random access. Subsequent accesses within the same row can be made with a faster access time. This is termed a PAGE access.

  The Flash can take advantage of this by the user configuring a lower number of wait states in the PAGEWAIT bits in the FBANKWAIT register. This mode works for data space and program space reads as well as instruction fetches. See the device data sheet for more information on the access time of the Flash.
- OTP Access: Read or fetch accesses to the OTP are controlled by the OTPWAIT register bits in the FOTPWAIT register. Accesses to the OTP take longer than the Flash and there is no paged mode.

Notes:

1) Writes to the Flash/OTP memory map area are ignored. They complete in a single cycle.
2) When the Code Security Module (CSM) is secured, reads to the Flash/OTP memory map area from outside the secure zone take the same number of cycles as a normal access. However, the read operation returns a zero.
3) The Flash supports 0-wait accesses when the PAGEWAIT bits are set to zero. This assumes that the CPU speed is low enough to accommodate the access time.

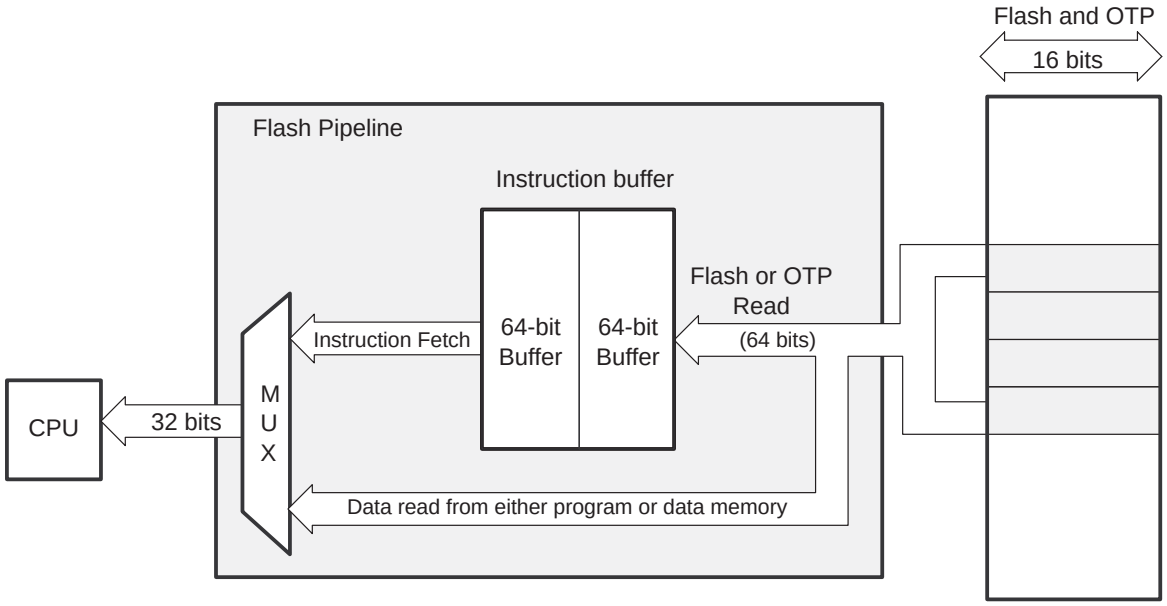
1.2.2 28x Flash Pipeline Mode

Flash memory is typically used to store application code. During code execution, instructions are fetched from sequential memory addresses, except when a discontinuity occurs. Usually the portion of the code that resides in sequential addresses makes up the majority of the application code and is referred to as linear code. To improve the performance of linear code execution, a Flash pipeline mode has been implemented. Setting the ENPIPE bit in the FOPT register enables this mode. The Flash pipeline mode is independent of the CPU pipeline. To allow you to maintain code timing compatibility between Flash and ROM devices, the Flash pipeline mode has also been implemented on ROM devices.

An instruction fetch from the Flash or OTP reads out 64 bits per access. The starting address of the access from Flash is automatically aligned to a 64-bit boundary such that the instruction location is within the 64 bits to be fetched. With Flash pipeline mode enabled (see Figure 1−2), the 64 bits read from the instruction fetch are stored in a 64-bit wide by 2-level deep instruction pre-fetch buffer. The contents of this pre-fetch buffer are then sent to the CPU for processing as required.

Up to two 32-bit instructions or up to four 16-bit instructions can reside within a single 64-bit access. The majority of C28x instructions are 16 bits, so for every 64-bit instruction fetch from the Flash bank it is likely that there are up to four instructions in the pre-fetch buffer ready to process through the CPU. During the time it takes to process these instructions, the Flash pipeline automatically initiates another access to the Flash bank to pre-fetch the next 64 bits. In this manner, the Flash pipeline mode works in the background to keep the instruction pre-fetch buffers as full as possible. Using this technique, the overall efficiency of sequential code execution from Flash or OTP is improved significantly.

Figure 1−2. Flash Pipeline



The Flash pipeline pre-fetch is aborted only on a PC discontinuity caused by executing an instruction such as a branch, BANZ, call, or loop. When this occurs, the pre-fetch is aborted and the contents of the pre-fetch buffer are flushed. There are two possible scenario's when this occurs:

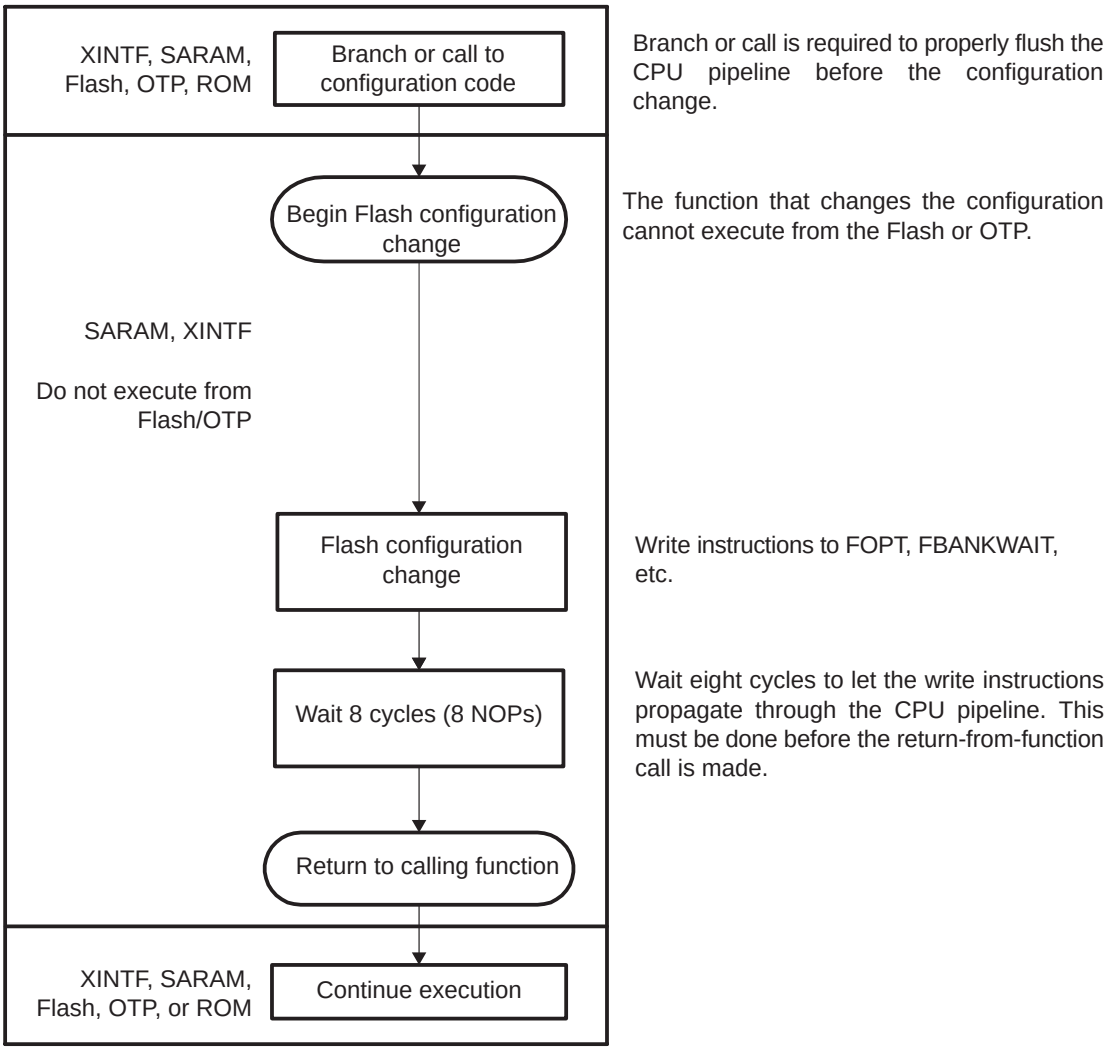
- If the destination address is within the Flash or OTP, the pre-fetch aborts and then resumes at the destination address.
- If the destination address is outside of the Flash and OTP, the pre-fetch is aborted and begins again only when a branch is made back into the Flash or OTP. The Flash pipeline pre-fetch mechanism only applies to instruction fetches from program space. Data reads from data memory and from program memory do not utilize the pre-fetch buffer capability and thus bypass the pre-fetch buffer. For example, instructions such as MAC, DMAC, and PREAD read a data value from program memory. When this read happens, the pre-fetch buffer is bypassed but the buffer is not flushed. If an instruction pre-fetch is already in progress when a data read operation is initiated, then the data read will be stalled until the pre-fetch completes.

1.2.3 Procedure to Change the Flash Configuration Registers

During Flash configuration, no accesses to the Flash or OTP can be in progress. This includes instructions still in the CPU pipeline, data reads, and instruction pre-fetch operations. To be sure that no access takes place during the configuration change, you should follow the procedure shown in Figure 1−3 for any code that modifies the FOPT, FPWR, FBANKWAIT, or FOTPWAIT registers.

This procedure also applies to the ROM on devices where the Flash and OTP have been replaced with ROM.

Figure 1−3. Flash Configuration Access Flow Diagram



1.3 Flash and OTP Registers

The Flash and OTP memory can be configured by the registers shown in Table 1−1. The bit descriptions are in Figure 1−4 through Figure 1−10.

Table 1−1. Flash/OTP Configuration Registers

Name	Address	Size (x16)	Description
			Configuration Registers
FOPT	0x0A80	1	Flash Option Register
Reserved	0x0A81	1	Reserved
FPWR	0x0A82	1	Flash Power Modes Register
FSTATUS	0x0A83	1	Status Register
FSTDBYWAIT	0x0A84	1	Flash Sleep To Standby Wait Register
FACTIVEWAIT	0x0A85	1	Flash Standby To Active Wait Register
FBANKWAIT	0x0A86	1	Flash Read Access Wait State Register
FOTPWAIT	0x0A87	1	OTP Read Access Wait State Register

Note: These registers are EALLOW protected.

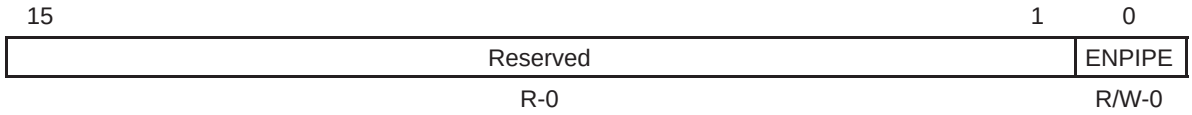
Note: Flash configuration registers should not be accessed while an access is in progress in Flash or OTP memory

The Flash configuration registers should not be accessed from code that is running from OTP or Flash memory or while an access may be in progress. All register accesses to the Flash registers should be made from code executing outside of Flash/OTP memory and an access should not be attempted until all activity on the Flash/OTP has completed. No hardware is included to protect against this.

You can read the Flash registers from code executing in Flash/OTP; however, do not write to the registers.

CPU write access to the registers can be enabled only by executing the EALLOW instruction. Write access is disabled when the EDIS instruction is executed. This protects the registers from spurious accesses. Read access is always available. The registers can be accessed through the JTAG port without the need to execute EALLOW. These registers support both 16-bit and 32-bit accesses.

Figure 1−4. Flash Options Register (FOPT)



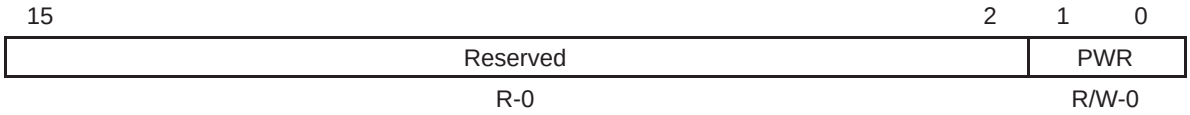
Legend: R = Read access, -0 = value after reset

Note: EALLOW-protected register

Table 1−2. Flash Options Register (FOPT) Field Descriptions

Bit(s)	Field	Description
15−1	Reserved	
0	ENPIPE	Enable Flash Pipeline Mode Bit: Flash pipeline mode is active when this bit is set. The pipeline mode improves performance of instruction fetches by pre-fetching instructions. On Flash devices, ENPIPE affects fetches from Flash and OTP. On ROM devices, this bit affects fetches from the ROM blocks that replaced the Flash and OTP. When pipeline mode is enabled, the Flash waitstates (paged and random) must be greater than zero.

Figure 1−5. Flash Power Register (FPWR)



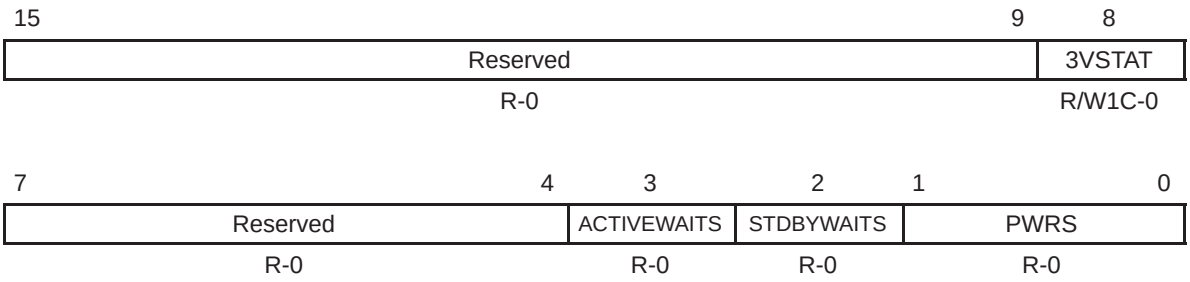
Legend: R = Read access, -0 = value after reset

Note: EALLOW-protected register

Table 1−3. Flash Power Register (FPWR) Field Descriptions

Bit(s)	Field	Value	Description
15−2	Reserved		
1−0	PWR		Flash Power Mode Bits: Writing to these bits changes the current power mode of the Flash bank and pump. See section 1.2 for more information on changing the Flash bank power mode. On ROM devices, changing PWR has no effect on the power consumption of the ROM. Moving to standby or sleep mode causes the next access from the ROM to be delayed just as on Flash devices.
		00	Pump and bank sleep (lowest power)
		01	Pump and bank standby
		10	Reserved (no effect)
		11	Pump and bank active (highest power)

Figure 1−6. Flash Status Register (FSTATUS)



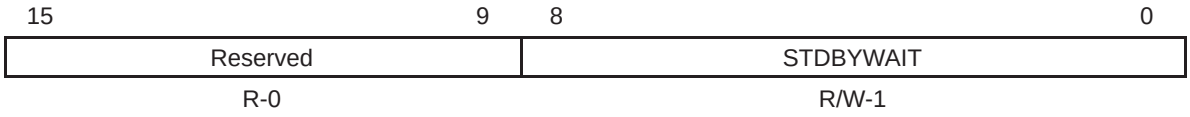
Legend: R = read access, -0 = value after reset, W1C = write 1 to clear

Note: EALLOW-protected register

Table 1−4. Flash Status Register (FSTATUS) Field Descriptions

Bit(s)	Field	Value	Description
15−9	Reserved		
8	3VSTAT		V_{DD3V} Status Latch Bit: When set, this bit indicates that the 3 VSTAT signal from the pump module went to a high level. This signal indicates that the 3 V supply went out of allowable range. This bit is cleared by writing a 1, writes of 0 are ignored.
7−4	Reserved		
3	ACTIVEWAITS		Bank and Pump Standby To Active Wait Counter Status Bit: This bit indicates whether the respective wait counter is currently timing out an access. If the bit is set, then the counter is counting. If the bit is 0, then the counter is not counting.
2	STDBYWAITS		Bank and Pump Sleep To Standby Wait Counter Status Bit: This bit indicates whether the respective wait counter is currently timing out an access. If the bit is set, then the counter is counting. If the bit is 0, then the counter is not counting.
1−0	PWRS		Power Modes Status Bits: These bits indicate the current power mode the Flash/OTP is in:
		00	Pump and bank sleep (lowest power)
		01	Pump and bank standby
		10	Reserved
		11	Pump and bank active (highest power)
			Note: The above bits only get set to the new power mode once the appropriate timing delays have expired.

Figure 1−7. Flash Standby Wait Register (FSTDBYWAIT)



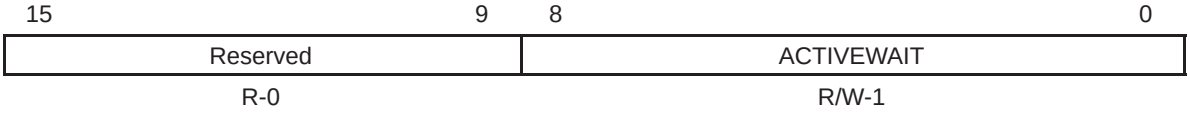
Legend: R = Read access, -0 = value after reset

Note: EALLOW-protected register

Table 1−5. Flash Standby Wait Register (FSTDBYWAIT) Field Descriptions

Bit(s)	Field	Description
15−9	Reserved	
8−0	STDBYWAIT	Bank and Pump Sleep To Standby Wait Count. When the bank and pump modules are in sleep mode and a write is performed to the PWR bits in the FPWR register (to change to a higher default power mode) or a CPU read or fetch access is performed to the Flash bank or OTP, then a counter is initiated with the value specified in these register bits. The power mode for the bank and pump are set for standby mode. The counter then counts down to zero before the PWRS bits are set to standby mode. If a CPU read or fetch access to the Flash bank/OTP initiated the process, the CPU is stalled until the access completes (see ACTIVEWAIT bits). The STDBYWAIT bits specify the number of CPU clock cycles (0..511 SYSCLKOUT cycles) of delay. See the Flash and OTP Power Mode section for more details. This register should be left in its default state.

Figure 1−8. Flash Standby to Active Wait Counter Register (FACTIVEWAIT)



Legend: R = Read access, -0 = value after reset

Note: EALLOW-protected register

Table 1−6. Flash Standby to Active Wait Counter Register (FACTIVEWAIT) Field Descriptions

Bit(s)	Field	Description
15−9	Reserved	
8−0	ACTIVEWAIT	Bank and Pump Standby To Active Wait Count: When the bank and pump modules are in standby mode and a write is performed to the PWR bits in the FPWR register (to change to a higher default power mode) or a CPU read or fetch access is performed to the Flash bank, then a counter is initiated with the value specified in these register bits. The power mode for the bank and pump are set for active mode. The counter then counts down to zero before allowing any CPU access to proceed. If a CPU read or fetch access to the Flash bank initiated the process, the CPU is stalled until the access completes (see PAGEWAIT and RANDWAIT bits). The ACTIVEWAIT bits specify the number of CPU clock cycles (0..511 SYSCLKOUT cycles) of delay. Refer to the Flash and OTP Power Modes section for more details. This register should be left in its default state.

Figure 1−9. Flash Waitstate Register (FBANKWAIT)

15 12	11 8	7 4	3 0
Reserved	PAGEWAIT	Reserved	RANDWAIT
R-0	R/W-1	R-0	R/W-1

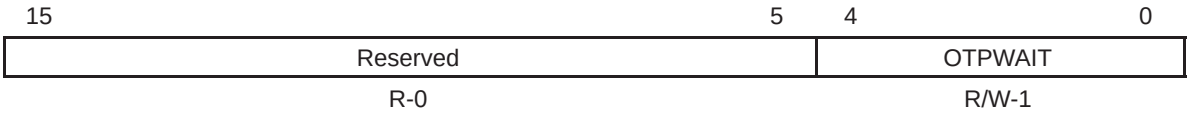
Legend: R = Read access, -0 = value after reset

Note: EALLOW-protected register

Table 1−7. Flash Waitstate Register (FBANKWAIT) Field Descriptions

Bit(s)	Field	Description
15−12	Reserved	
11−8	PAGEWAIT	Flash Paged Read Wait States: These register bits specify the number of wait states for a paged read operation in CPU clock cycles (0..15 SYSCLKOUT cycles) to the banks. See Notes 1 and 2. On ROM devices, these bits affect the wait states of the ROM block that replaced Flash.
7−4	Reserved	
3−0	RANDWAIT	Flash Random Read Wait States: These register bits specify the number of wait states for a random read operation in CPU clock cycles (0..15 SYSCLKOUT cycles) to the banks. See Notes 1 and 2.See the device-specific data sheet for the minimum time required for Flash or ROM access. RANDWAIT must be set greater than 0. That is, at least 1 random waitstate must be used. On ROM devices, these bits affect the wait states of the ROM block that replaced Flash. **Notes:** 1) You must set RANDWAIT to a value greater than or equal to the PAGEWAIT setting. No hardware is provided to detect a PAGEWAIT value that is greater then RANDWAIT. 2) When enabling Flash pipeline mode, you must set PAGEWAIT and RANDWAIT to a value greater than zero.

Figure 1−10. OTP Waitstate Register (FOTPWAIT)



Legend: R = Read access, -0 = value after reset

Note: EALLOW-protected register

Table 1−8. OTP Waitstate Register (FOTPWAIT) Field Descriptions

Bit(s)	Field	Description
15−5	Reserved	
4−0	OTPWAIT	OTP Read Wait States. These register bits specify the number of wait states for a read operation in CPU clock cycles (0..31 SYSCLKOUT cycles) to the OTP. See CPU Read Or Fetch Access From Flash/OTP section for more details. There is no PAGE mode in the OTP. OTPWAIT must be set greater than 0. That is, a minimum of 1 wait-state must be used. See the device-specific datasheet for the minimum time required for an OTP or ROM access. On ROM devices, these bits affect the wait states of the ROM block that replaced Flash.

Chapter 2

Code Security Module (CSM)

The code security module (CSM) is a security feature incorporated in 28x devices. It prevents access/visibility to on-chip memory to unauthorized persons—i.e., it prevents duplication/reverse engineering of proprietary code.

The word secure means access to on-chip memory is protected. The word unsecure means access to on-chip secure memory is not protected — i.e., the contents of the memory could be read by any means (through a debugging tool such as Code Composer Studio™, for example).

Topic **Page**

2.1	Functional Description	2-2
2.2	CSM Impacts on Other On-Chip Resources	2-4
2.3	Incorporating Code Security in User Applications	2-6
2.4	Do’s and Don’ts to Protect Security Logic	2-13
2.5	CSM Features − Summary	2-14

2.1 Functional Description

The security module restricts the CPU access to certain on-chip memory. This, in effect, blocks read and write access to various memories through the JTAG port or external peripherals. Security is defined with respect to the access of on-chip memory and prevents unauthorized copying of proprietary code or data.

The device is secure when CPU access to the on-chip secure memory locations is restricted. When secure, two levels of protection are possible, depending on where the program counter is currently pointing. If code is currently running from inside secure memory, only access through JTAG is blocked (i.e., the emulator). This allows secure code to access secure data. Conversely, if code is running from nonsecure memory, all accesses to secure memories are blocked. User code can dynamically jump in and out of secure memory, thereby allowing secure function calls from nonsecure memory. Similarly, interrupt service routines can be placed in secure memory, even if the main program loop is run from nonsecure memory.

Security is protected by a password of 128-bit data (eight 16-bit words) that is used to secure or unsecure the device.

The device is unsecured by executing the password match flow (PMF), described later in this chapter. Table 2−1 shows the levels of security.

Table 2−1. Security Levels

PMF Executed With Correct Password?	Operating Mode	Program Fetch Location	Security Description
No	Secure	Outside secure memory	Only fetches are allowed to secure memory
No	Secure	Inside secure memory	CPU has full access. JTAG port cannot read the secured memory contents.
Yes	Not Secure	Anywhere	Full access for CPU and JTAG port to secure memory

Passwords are stored in code security password locations (PWL) in flash/ROM memory (0x003F 7FF8−0x003F 7FFF). These locations store the password predetermined by the system designer.

In flash devices, the password can be changed anytime if the old password is known. In ROM devices, the password cannot be changed after the device is manufactured by Texas Instruments (TI).

If the PWL have all 128 bits as ones, the device is labeled unsecure. Since new flash devices have erased flash (all ones), only a read of the PWL is required to bring the device into unsecure mode. If the PWL have all 128 bits as zeros, the device is secure, regardless of the contents of the KEY registers. Do not use all zeros as a password or reset the device after performing a clear routine on the flash. If a device is reset when the PWL is all zeros, the device cannot be debugged or reprogrammed. To summarize, a device with an erased flash array is unsecure. A device with a cleared flash array is secure.

User accessible registers (eight 16-bit words) that are used to secure or unsecure the device are referred to as key registers. These registers are mapped in the memory space at addresses 0x0000 0AE0 − 0x0000 0AE7 and are EALLOW protected.

Note: Security of addresses between 0x3F7F80 and 0x3F7FF5

For code security operation, all addresses between 0x3F7F80 and 0x3F7FF5 cannot be used as program code or data, but must be programmed to 0x0000 when the Code Security Passwords are programmed. If security is not a concern, then these addresses can be used for code or data.

Code Security Module Disclaimer

The Code Security Module (“CSM”) included on this device was designed to password protect the data stored in the associated memory (either ROM or Flash) and is warranted by Texas Instruments (TI), in accordance with its standard terms and conditions, to conform to TI’s published specifications for the warranty period applicable for this device.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

2.2 CSM Impact on Other On-Chip Resources

The CSM has no impact whatsoever on the following on-chip resources:

- Single-access RAM (SARAM) blocks not designated as secure − These memory blocks can be freely accessed and code run from them, whether the device is in secure or unsecure mode.
- Boot ROM contents − Visibility to the boot ROM contents is not impacted by the CSM.
- On-chip peripheral registers − The peripheral registers can be initialized by code running from on-chip or off-chip memory, whether the device is in secure or unsecure mode.
- PIE Vector Table − Vector tables can be read and written regardless of whether the device is in secure or unsecure mode. Table 2−2 and Table 2−3 show which on-chip resources are affected (or are not affected) by the CSM on 280x devices. For other devices, see the device-specific data sheet.

Table 2−2. 280x Resources Affected by the CSM

Address	Block
0x0000 8000−0x0000 8FFF	L0 SARAM (4K X 16)
0x0000 9000−0x0000 9FFF	L1 SARAM (4K X 16)
0x003D 7800− 0x003D 7BFF	One-time programmable (OTP) or ROM (1K X 16)
0x003D 8000−0x003F 7FFF	Flash or ROM (128K X 16 or 64K X 16)
0x003F 8000−0x003F 8FFF	L0 SARAM (4K X 16), mirror
0x003F 9000−0x003F 9FFF	L1 SARAM (4K X 16), mirror

Table 2−3. 280x Resources Not Affected by the CSM

Address	Block
0x0000 0000−0x0000 03FF	M0 SARAM (1K X 16)
0x0000 0400−0x0000 07FF	M1 SARAM (1K X16)
0x0000 0800−0x0000 0CFF	Peripheral Frame 0 (2K X 16)
0x0000 0D00−0x0000 0FFF	PIE Vector RAM (256 X 16)
0x0000 6000−0x0000 6FFF	Peripheral Frame 1 (4K X 16)
0x0000 A0000 − 0x0000 BFFF	H0 SARAM (8K X 16)
0x0000 7000−0x0000 7FFF	Peripheral Frame 2 (4K X 16)
0x003F A000−0x003F BFFF	H0 SARAM (8K X 16) mirror
0x003F F000−0x003F FFFF	Boot ROM (4K X 16)

To summarize, it is possible to load code onto the unprotected on-chip program RAM shown in Table 2−3 via the JTAG connector without any impact from the CSM. The code can be debugged and the peripheral registers initialized, independent of whether the device is in secure or unsecure mode.

2.3 Incorporating Code Security in User Applications

Code security is typically not required in the development phase of a project; however, security is needed once a robust code is developed. Before such a code is programmed in the flash memory (or committed to ROM), a password should be chosen to secure the device. Once a password is in place, the device is secured (i.e., programming a password at the appropriate locations and either performing a device reset or setting the FORCESEC bit (CSMSCR.15) is the action that secures the device). From that time on, access to debug the contents of secure memory by any means (via JTAG, code running off external/on-chip memory etc.) requires the supply of a valid password. A password is not needed to run the code out of secure memory (such as in a typical end-customer usage); however, access to secure memory contents for debug purpose requires a password.

Table 2−4. Code Security Module (CSM) Registers

Memory Address	Register Name	Reset Values	Register Description
KEY Registers − Accessible by the user			
0x0000−0AE0	KEY0†	0xFFFF	Low word of the 128-bit KEY register
0x0000−0AE1	KEY1†	0xFFFF	Second word of the 128-bit KEY register
0x0000−0AE2	KEY2†	0xFFFF	Third word of the 128-bit KEY register
0x0000−0AE3	KEY3†	0xFFFF	Fourth word of the 128-bit key
0x0000−0AE4	KEY4†	0xFFFF	Fifth word of the 128-bit key
0x0000−0AE5	KEY5†	0xFFFF	Sixth word of the 128-bit key
0x0000−0AE6	KEY6†	0xFFFF	Seventh word of the 128-bit key
0x0000−0AE7	KEY7†	0xFFFF	High word of the 128-bit KEY register
0x0000−0AEF	CSMSCR†		CSM status and control register
PWL in Memory − Reserved for passwords only (On R280x devices, all passwords are set to all Fs)			
0x003F−7FF8	PWL0	User defined	Low word of the 128-bit password
0x003F−7FF9	PWL1	User defined	Second word of the 128-bit password
0x003F−7FFA	PWL2	User defined	Third word of the 128-bit password
0x003F−7FFB	PWL3	User defined	Fourth word of the 128-bit password
0x003F−7FFC	PWL4	User defined	Fifth word of the 128-bit password
0x003F−7FFD	PWL5	User defined	Sixth word of the 128-bit password
0x003F−7FFE	PWL6	User defined	Seventh word of the 128-bit password
0x003F−7FFF	PWL7	User defined	High word of the 128-bit password

† EALLOW protected

Figure 2−1. CSM Status and Control Register (CSMSCR)

15	14 7	6 1	0
FORCESEC	Reserved	Reserved	SECURE
W-1	R-0	R-10111	R-1

Legend: R = Read access, W = write access, -0 = value after reset

Note: EALLOW-protected register

Table 2−5. CSM Status and Control Register (CSMSCR) Field Descriptions

Bit(s)	Field	Value	Description
15	FORCESEC		Writing a 1 clears the KEY registers and secures the device. A read always returns a zero.
14−1	Reserved		
0	SECURE		Read-only bit that reflects the security state of the device.
		1	Device is secure (CSM locked)
		0	Device is unsecure (CSM unlocked)

2.3.1 Environments That Require Security Unlocking

Following are the typical situations under which unsecuring can be required:

- Code development using debuggers (such as Code Composer Studio™)

  This is the most common environment during the design phase of a product.

- Flash programming using TI's flash utilities

  Flash programming is common during code development and testing. Once the user supplies the necessary password, the flash utilities disable the security logic before attempting to program the flash. The flash utilities can disable the code security logic in new devices without any authorization, since new devices come with an erased flash. However, reprogramming devices (that already contain custom passwords) require passwords to be supplied to the flash utilities in order to enable programming.

- Custom environment defined by the application

In addition to the above, access to secure memory contents can be required in situations such as:

- Using the on-chip bootloader to program the flash
- Executing code from external memory or on-chip unsecure memory and requiring access to secure memory for lookup table. This is not a suggested operating condition as supplying the password from external code could compromise code security.

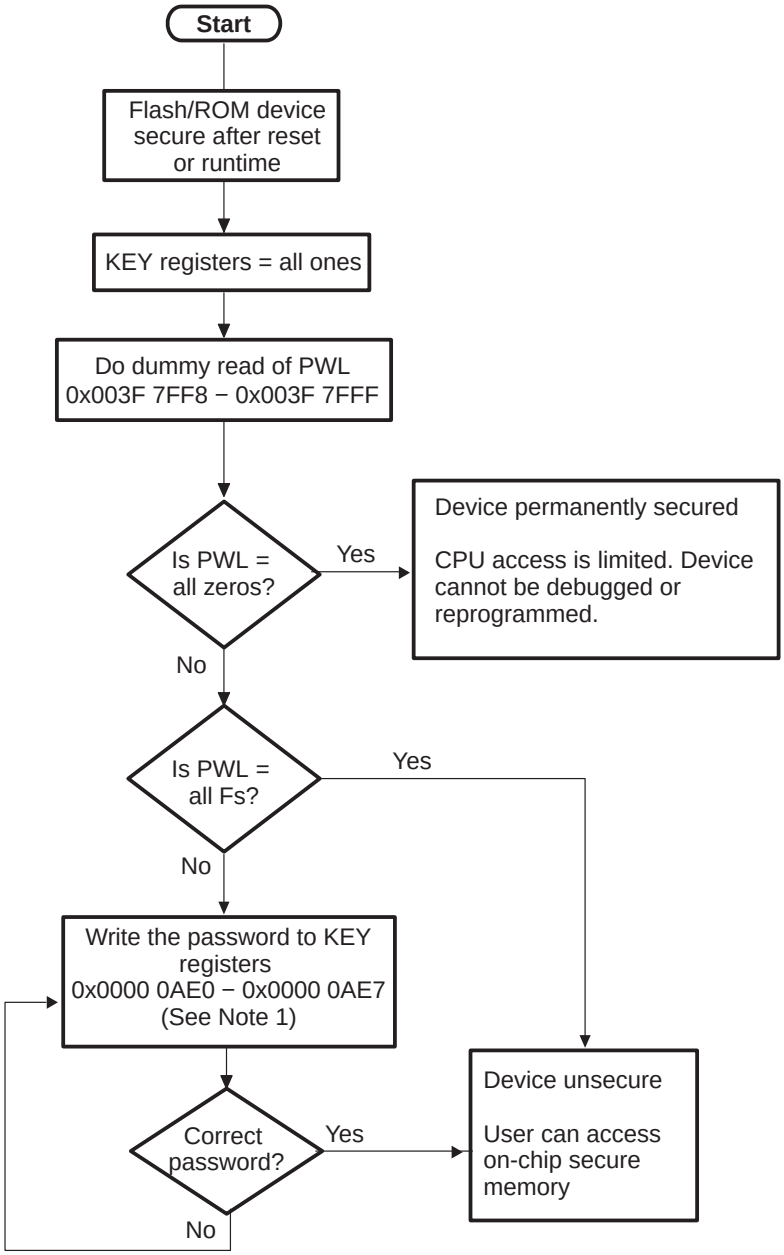
The unsecuring sequence is identical in all the above situations. This sequence is referred to as the *password match flow (PMF)* for simplicity. Figure 2−2 explains the sequence of operation that is required every time the user attempts to unsecure a device. A code example is listed for clarity.

2.3.2 Password Match Flow

Password match flow (PMF) is essentially a sequence of eight dummy reads from password locations (PWL) followed by eight writes to KEY registers.

Figure 2−2 shows how the PMF helps to initialize the security logic registers and disable security logic.

Figure 2−2. Password Match Flow (PMF)



1) The KEY registers are EALLOW protected.

2.3.3 Unsecuring Considerations for Devices With/Without Code Security

Case 1 and Case 2 provide unsecuring considerations for devices with and without code security.

Case 1: Device With Code Security

A device with code security should have a predetermined password stored in the PWL (locations 0x003F 7FF8−0x003F 7FFF in memory). In addition, locations 0x3F7F80 − 0x3F7FF5 should be programmed with all 0x0000 and not used for program and/or data storage. The following are steps to unsecure this device:

1) Perform a dummy read of the PWL.
2) Write the password into the KEY registers (locations 0x0000 0AE0−0x0000 0AE7 in memory).
3) If the password is correct, the device becomes unsecure; otherwise, it stays secure.

Case 2: Device Without Code Security

A device without code security should have 0x FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF (128 bits of all ones) stored in the PWL. The following are steps to use this device:

1) Perform a dummy read of the PWL.
2) Secure memory is fully accessible immediately after this operation is completed.

Note:

A dummy read operation must be performed prior to reading, writing, or programming secure memory, even though the device is not protected with a password.

2.3.4 C Code Example to Unsecure

```
volatile int *CSM = (volatile int *)0x000AE0;    //CSM register file
volatile int *PWL = (volatile int *)0x3F7FF8;    //Password location
volatile int tmp;
int i ;
// Read the 128-bits of the password location (PWL)
// in Flash/ROM at address 0x3F7FF8-0x3F7FFF.
// If the device is secure, then the values read will
// not actually be loaded into the temp variable, so
// this is called a dummy read.
for (i = 0; i<8; i++) tmp = *PWL++;

// If the password location (PWL) is all = ones (0xFFFF),
// then the device will now be unsecure.  If the password
// is not all ones (0xFFFF), then the code below is required
// to unsecure the CSM.
// Write the 128-bit password to the KEY registers
// If this password matches that stored in the
// PWL then the CSM will become unsecure.  If it does not
// match, then the device will remain secure.
// An example password of:
// 0x0123456789ABCDEFCDEF89AB45670123 is used.
asm("  EALLOW");    // Key registers are EALLOW protected
*CSM++ = 0x0123;    // Register KEY0 at 0xAE0
*CSM++ = 0x4567;    // Register KEY1 at 0xAE1
*CSM++ = 0x89AB;    // Register KEY2 at 0xAE2
*CSM++ = 0xCDEF;    // Register KEY3 at 0xAE3
*CSM++ = 0xCDEF;    // Register KEY4 at 0xAE4
*CSM++ = 0x89AB;    // Register KEY5 at 0xAE5
*CSM++ = 0x4567;    // Register KEY6 at 0xAE6
*CSM++ = 0x0123;    // Register KEY7 at 0xAE7
asm("  EDIS");
```

2.3.5 C Code Example to Resecure

```
volatile int *CSM = 0x000AE0;       //CSM register file
//Set FORCESEC bit
asm("  EALLOW");                     //CSMSCR register is EALLOW protected.
*CSM = 0x8000;
asm ("EDIS");
```

2.4 Do’s and Don’ts to Protect Security Logic

2.4.1 Do’s

- To keep the debug and code development phase simple, use the device in the unsecure mode; i.e., use 128 bits of all ones as PWL words (or use a password that is easy to remember). Use passwords after the development phase when the code is frozen.
- Recheck the passwords in PWL before programming the COFF file using flash utilities.
- The flow of code execution can freely toggle back and forth between secure memory and unsecure memory without compromising security. To access data variables located in secure memory when the device is secured, code execution must currently be running from secure memory.
- Program locations 0x3F7F80 − 0x3F7FF5 with 0x0000 when using the CSM.

2.4.2 Don’ts

- If code security is desired, do not embed the password in your application anywhere other than in the PWL or security can be compromised.
- Do not use 128 bits of all zeros as the password. This automatically secures the device, regardless of the contents of the KEY register. The device is not debuggable nor reprogrammable.
- Do not pull a reset after clearing the flash array but before erasing the array. This leaves zeros in the PWL that automatically secures the device, regardless of the contents of the KEY register. The device is not debuggable nor reprogrammable.
- Do not use locations 0x3F7F80 − 0x3F7FF5 to store program and/or data. These locations should be programmed to 0x0000 when using the CSM.

2.5 CSM Features − Summary

1) The flash is secured after a reset until the password match flow (PMF) is executed.

2) The standard way of running code out of the flash or ROM is to program the flash with the code (for ROM devices the program is hardcoded at device fabrication) and powering up the DSP in microcomputer mode. Since instruction fetches are always allowed from secure memory, regardless of the state of the CSM, the code functions correctly even without executing the PMF.

3) Secure memory cannot be modified while the device is secured.

4) Secure memory cannot be read from any code running from unsecure memory while the device is secured.

5) Secure memory cannot be read or written to by the debugger (i.e., Code Composer Studio™) at any time that the device is secured.

6) Complete access to secure memory from both the CPU code and the debugger is granted while the device is unsecured.

Chapter 3

Clocking

This section describes the oscillator, PLL and clocking mechanisms, the watchdog function, and the low-power modes.

Topic **Page**

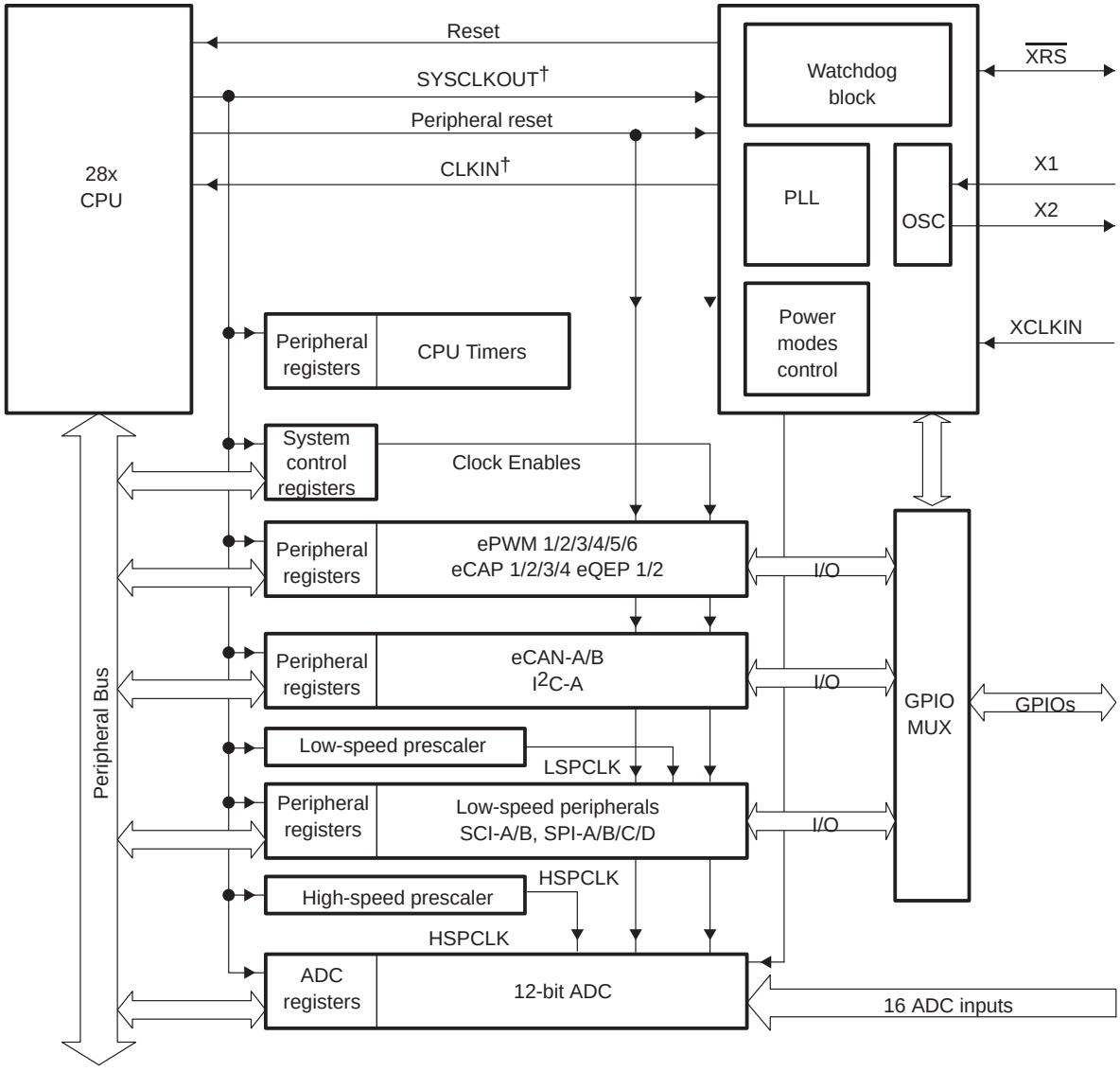
3.1	Clocking and System Control	3-2
3.2	OSC and PLL Block	3-13
3.3	Low-Power Modes Block	3-23
3.4	Watchdog Block	3-26
3.5	32-Bit CPU Timers 0/1/2	3-30

3.1 Clocking and System Control

Figure 3−1 shows the various clock and reset domains in the 280x devices.

The PLL, clocking, watchdog and low-power modes, are controlled by the registers listed in Table 3−1.

Figure 3−1. Clock and Reset Domains



† CLKIN is the clock into the CPU. It is passed out of the CPU as SYSCLKOUT (that is, CLKIN is the same frequency as SYSCLKOUT).

Table 3−1. PLL, Clocking, Watchdog, and Low-Power Mode Registers†

Name	Address	Size (x16)	Description
XCLK	0x0000 7010	1	XCLKOUT pin control and X1/XCLKIN Status Register
PLLSTS	0x0000 7011	1	PLL Status Register
Reserved	0x0000 7012 0x0000 7019	8	
HISPCP	0x0000 701A	1	High-Speed Peripheral Clock Prescaler Register for HSPCLK Clock
LOSPCP	0x0000 701B	1	Low-Speed Peripheral Clock Prescaler Register for HSPCLK clock
PCLKCR0	0x0000 701C	1	Peripheral Clock Control Register 0
PCLKCR1	0x0000 701D	1	Peripheral Clock Control Register 1
LPMCR0	0x0000 701E	1	Low Power Mode Control Register 0
Reserved	0x0000 701F	1	
Reserved	0x0000 7020	1	
PLLCR	0x0000 7021	1	PLL Control Register‡
SCSR	0x0000 7022	1	System Control & Status Register
WDCNTR	0x0000 7023	1	Watchdog Counter Register
Reserved	0x0000 7024	1	
WDKEY	0x0000 7025	1	Watchdog Reset Key Register
Reserved	0x0000 7026 0x0000 7028	3	
WDCR	0x0000 7029	1	Watchdog Control Register
Reserved	0x0000 702A 0x0000 702F	6	

† All of the registers in this table can be accessed only by executing the EALLOW instruction.
‡ The PLL control register (PLLCR) and PLL Status Register (PLLSTS) are reset to a known state by the $\overline{\text{XRS}}$ signal only.

The PCLKCR0 and PCLKCR1 registers enable/disable clocks to the various peripheral modules. Figure 3−2 lists the bit descriptions of the PCLKCR0 register.

Figure 3−2. Peripheral Clock Control 0 Register (PCLKCR0) (See Notes 1 and 2)

15	14	13	12	11	10	9	8
ECANBENCLK	ECANAENCLK	Reserved		SCIBENCLK	SCIAENCLK	SPIBENCLK	SPIAENCLK
R/W-0	R/W-0	R-0		R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
SPIDENCLK	SPICENCLK	Rsvd	I2CAENCLK	ADCENCLK	TBCLKSYNC	Reserved	
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R-0	

Legend: R = Read access, -0 = value after reset

Notes: 1) EALLOW-protected register

2) If a peripheral block is not used, then the clock to that peripheral can be turned off to minimize power consumption.

Table 3−2. Peripheral Clock Control 0 Register (PCLKCR0) Field Descriptions

Bit(s)	Field	Description
15	ECANBENCLK	ECAN-B Clock enable
		0 The eCAN-B module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset.
		1 The eCAN-B module is clocked by the system clock (SYSCLKOUT). This bit is reserved on the 2806 and 2801 devices and writes will be ignored.
14	ECANAENCLK	ECAN-A Clock Enable
		0 The eCAN-A module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset.
		1 The eCAN-A module is clocked by the system clock (SYSCLKOUT).
13−12	Reserved	Reserved
11	SCIBENCLK	SCI-B clock enable
		0 SCI-B module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset.
		1 The SCI-B module is clocked by the low-speed clock (LSPCLK). This bit is reserved on the 2806 and 2801 devices and writes will be ignored.

Table 3−2. Peripheral Clock Control 0 Register (PCLKCR0) Field Descriptions (Continued)

Bit(s)	Field	Description
10	SCIAENCLK	SCI-A clock enable
		0 The SCI-A module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset.
		1 The SCI-A module is clocked by the low-speed clock (LSPCLK).
9	SPIBENCLK	SPI-B clock enable.
		0 The SPI-B module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset.
		1 The SPI-B module is clocked by the low-speed clock (LSPCLK).
8	SPIAENCLK	SPI-A clock enable.
		0 The SPI-A module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset.
		1 The SPI-A module is clocked by the low-speed clock (LSPCLK).
7	SPIDENCLK	SPI-D clock enable. This bit is reserved on the 2801 device and writes will be ignored.
		0 The SPI-D module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset.
		1 The SPI-D module is clocked by the low-speed clock (LSPCLK).
6	SPICENCLK	SPI-C clock enable This bit is reserved on the 2801 device and writes will be ignored.
		0 The SPI-C module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset.
		1 The SPI-C module is clocked by the low-speed clock (LSPCLK).
5	Reserved	0 Reserved
4	I2CAENCLK	I2C clock enable
		0 The I2C module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset.
		1 The I2C module is clocked by the system clock (SYSCLKOUT).
3	ADCENCLK	ADC clock enable.
		0 The ADC is not clocked. For low power operation, this bit is cleared to zero by the user or by reset.
		1 The ADC module is clocked by the high-speed clock (HSPCLK)

Table 3−2. Peripheral Clock Control 0 Register (PCLKCR0) Field Descriptions (Continued)

Bit(s)	Field	Description
2	TBCLKSYNC	ePWM Module Time Base Clock (TBCLK) Sync: Allows the user to globally synchronize all enabled ePWM modules to the time base clock (TBCLK): 0 All enabled ePWM modules clocks are stopped. 1 All enabled ePWM module clocks are started with the first rising edge of TBCLK aligned. For perfectly synchronized TBCLKs, the prescaler bits in the TBCTL register of each ePWM module must be set identically. The proper procedure for enabling ePWM clocks is as follows: 1) Enable ePWM module clocks in PCLKCR1 register. 2) 2. Set TBCLKSYNC to 0. 3) 3. Configure prescaler values and ePWM modes. 4) 4. Set TBCLKSYNC to 1.
1−0	Reserved	Reserved

Figure 3−3. Peripheral Clock Control 1 Register† (PCLKCR1)

15	14	13 12	11	10	9	8
EQEP2ENCLK	EQEP1ENCLK	Reserved	ECAP4ENCLK	ECAP3ENCLK	ECAP2ENCLK	ECAP1ENCLK
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

7 6	5	4	3	2	1	0
Reserved	EPWM6ENCLK	EPWM5ENCLK	EPWM4ENCLK	EPWM3ENCLK	EPWM2ENCLK	EPWM1ENCLK
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read access, -0 = value after reset
† EALLOW-protected register

Table 3−3. Peripheral Clock Control 1 Register (PCLKCR1) Field Descriptions

Bit(s)	Field	Description
15	EQEP2ENCLK	eQEP2 clock enable. This bit is reserved on the 2801 device and writes will be ignored. 0 The eQEP2 module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset. 1 The eQEP2 module is clocked by the system clock (SYSCLKOUT).
14	EQEP1ENCLK	eQEP1 clock enable 0 The eQEP1 module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset. 1 The eQEP1 module is clocked by the system clock (SYSCLKOUT).
13−12	Reserved	Reserved
11	ECAP4ENCLK	eCAP4 clock enable. This bit is reserved on the 2801 device and writes will be ignored. 0 The eCAP4 module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset. 1 The eCAP4 module is clocked by the system clock (SYSCLKOUT).
10	ECAP3ENCLK	eCAP3 clock enable This bit is reserved on the 2801 device and writes will be ignored. 0 The eCAP3 module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset. 1 The eCAP3 module is clocked by the system clock (SYSCLKOUT).
9	ECAP2ENCLK	eCAP2 clock enable 0 The eCAP2 module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset. 1 The eCAP2 module is clocked by the system clock (SYSCLKOUT).

Table 3−3. Peripheral Clock Control 1 Register (PCLKCR1) Field Descriptions (Continued)

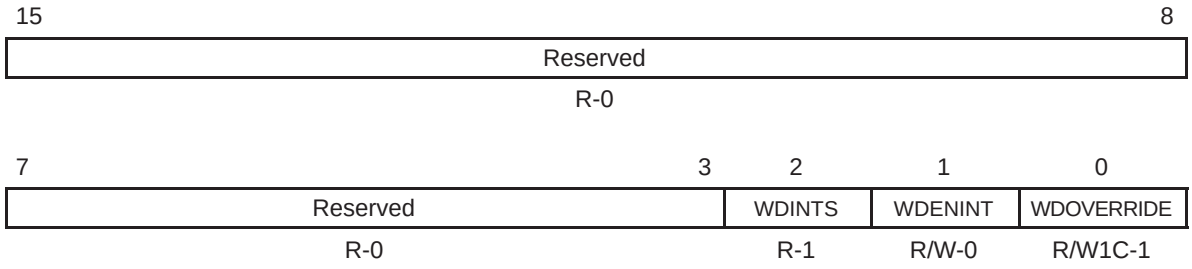
Bit(s)	Field	Description
8	ECAP1ENCLK	eCAP1 clock enable 0 The eCAP1 module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset. 1 The eCAP1 module is clocked by the system clock (SYSCLKOUT).
7−6	Reserved	Reserved
5	EPWM6ENCLK	ePWM6 clock enable To start the TBCLK within the ePWM modules, the TBCLKSYNC bit in PCLKCR0 must also be set. This bit is reserved on the 2801 device and writes will be ignored. 0 The ePWM6 module is not clocked. 1 The ePWM6 module is clocked by the system clock (SYSCLKOUT).
4	EPWM5ENCLK	ePWM5 clock enable. To start the TBCLK within the ePWM modules, the TBCLKSYNC bit in PCLKCR0 must also be set. This bit is reserved on the 2801 device and writes will be ignored. 0 The ePWM5 module is not clocked. 1 The ePWM5 module is clocked by the system clock (SYSCLKOUT).
3	EPWM4ENCLK	ePWM4 clock enable To start the TBCLK within the ePWM modules, the TBCLKSYNC bit in PCLKCR0 must also be set. This bit is reserved on the 2801 device and writes will be ignored. 0 The ePWM4 module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset. 1 The ePWM4 module is clocked by the system clock (SYSCLKOUT).
2	EPWM3ENCLK	ePWM3 clock enable. To start the TBCLK within the ePWM modules, the TBCLKSYNC bit in PCLKCR0 must also be set. 0 The ePWM3 module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset. 1 The ePWM3 module is clocked by the system clock (SYSCLKOUT).

Table 3−3. Peripheral Clock Control 1 Register (PCLKCR1) Field Descriptions (Continued)

Bit(s)	Field	Description
1	EPWM2ENCLK	ePWM2 clock enable. To start the TBCLK within the ePWM modules, the TBCLKSYNC bit in PCLKCR0 must also be set. 0 The ePWM2 module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset. 1 The ePWM2 module is clocked by the system clock (SYSCLKOUT).
0	EPWM1ENCLK	ePWM1 clock enable. To start the TBCLK within the ePWM modules, the TBCLKSYNC bit in PCLKCR0 must also be set. 0 The ePWM1 module is not clocked. For low power operation, this bit is cleared to zero by the user or by reset. 1 The ePWM1 module is clocked by the system clock (SYSCLKOUT).

The system control and status register (SCSR) contains the watchdog override bit and the watchdog interrupt enable/disable bit. Figure 3−4 describes the bit functions of the SCSR register.

Figure 3−4. System Control and Status Register (SCSR)



Legend: R = Read access, -0 = value after reset, W1C = Write 1 to clear

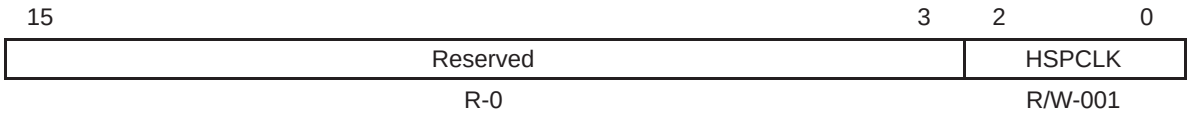
Note: EALLOW-protected register

Table 3−4. System Control and Status Register (SCSR) Field Descriptions

Bits	Field	Description
15−3	Reserved	Reserved
2	WDINTS	Watchdog interrupt status bit. WDINTS reflects the current state of the $\overline{\text{WDINT}}$ signal from the watchdog block. If the watchdog interrupt is used to wake the device from IDLE or STANDBY low power mode, use this bit to make sure the interrupt is not active before attempting to go back into IDLE or STANDBY mode. 0 Watchdog interrupt is active. 1 Watchdog interrupt is not active.
1	WDENINT	Watchdog interrupt enable. 0 The watchdog reset ($\overline{\text{WDRST}}$) output signal is enabled and the watchdog interrupt ($\overline{\text{WDINT}}$) output signal is disabled. This is the default state on reset (XRS). 1 The $\overline{\text{WDRST}}$ output signal is disabled and the $\overline{\text{WDINT}}$ output signal is enabled.
0	WDOVERRIDE	Watchdog override 0 Writing a 0 has no effect. If this bit is cleared, then it remains in this state until a reset occurs. The current state of this bit is readable by the user. 1 You can change the state of the watchdog disable (WDDIS) bit in the watchdog control (WDCR) register. If the WDOVERRIDE bit is cleared by writing a 1, you cannot modify the WDDIS bit.

The high speed peripheral and low speed peripheral clock prescale (HISPCP and LOSPCP) registers are used to configure the high- and low-speed peripheral clocks, respectively. See Figure 3−5 for the HISPCP bit layout and Figure 3−6 for the LOSPCP layout.

Figure 3−5. High-Speed Peripheral Clock Prescaler (HISPCP) Register



Legend: R = Read access, -0 = value after reset

Note: EALLOW-protected register

Table 3−5. High-Speed Peripheral Clock Prescaler (HISPCP) Field Descriptions

Bits	Field	Description
15−3	Reserved	Reserved
2−0	HSPCLK	These bits configure the high-speed peripheral clock (HSPCLK) rate relative to SYSCLKOUT: If HISPCP ≠ 0, HSPCLK = SYSCLKOUT/(HISPCP† X 2) If HISPCP = 0, HSPCLK = SYSCLKOUT 000 High speed clock = SYSCLKOUT/1 001 High speed clock = SYSCLKOUT/2 (reset default) 010 High speed clock = SYSCLKOUT/4 011 High speed clock = SYSCLKOUT/6 100 High speed clock = SYSCLKOUT/8 101 High speed clock = SYSCLKOUT/10 110 High speed clock = SYSCLKOUT/12 111 High speed clock = SYSCLKOUT/14

† HISPCP in this equation denotes the value of bits 2:0 in the HISPCP register.

Figure 3−6. Low-Speed Peripheral Clock Prescaler Register (LOSPCP)

15	3	2	0
Reserved		LSPCLK	
R-0		R/W-010	

Legend: R = Read access, W = write access, -0 = value after reset

Note: EALLOW-protected register

Table 3−6. Low-Speed Peripheral Clock Prescaler Register (LOSPCP) Field Descriptions

Bit(s)	Field	Value	Description
15−3	Reserved		Reserved
2−0	LSPCLK		These bits configure the low-speed peripheral clock (LSPCLK) rate relative to SYSCLKOUT: If LOSPCP $\neq$ 0, LSPCLK = SYSCLKOUT/(LOSPCP† X 2) If LOSPCP = 0, LSPCLK = SYSCLKOUT
		000	Low speed clock = SYSCLKOUT/1
		001	Low speed clock= SYSCLKOUT/2
		010	Low speed clock= SYSCLKOUT/4 (reset default)
		011	Low speed clock= SYSCLKOUT/6
		100	Low speed clock= SYSCLKOUT/8
		101	Low speed clock= SYSCLKOUT/10
		110	Low speed clock= SYSCLKOUT/12
		111	Low speed clock= SYSCLKOUT/14

† LOSPCP in this equation denotes the value of bits 2:0 in the LOSPCP register.

3.2 OSC and PLL Block

The on-chip oscillator and phase-locked loop (PLL) block provides the clocking signals for the device, as well as control for low-power mode entry.

3.2.1 PLL-Based Clock Module

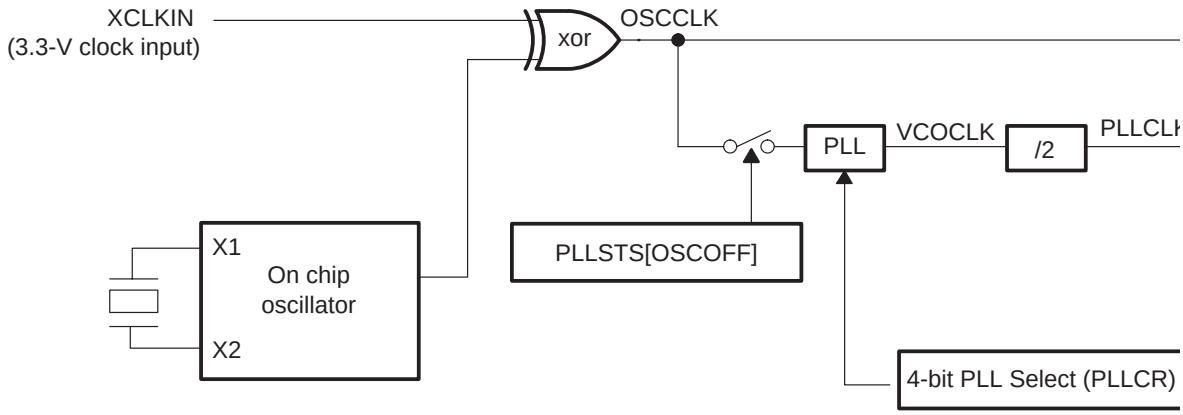
The 280x devices have an on-chip, PLL-based clock module. The PLL has a 4-bit ratio control to select different CPU clock rates.

The PLL-based clock module provides two modes of operation:

- Crystal-operation
  This mode allows the use of an external crystal/resonator to provide the time base to the device. The crystal is connected to the X1/X2 1.8-V pins and XCLKIN is tied low.
- External clock source operation
  This mode allows the internal oscillator to be bypassed. The device clocks are generated from an external clock source input on the XCLKIN pin. You must tie X1 low and leave X2 disconnected. In this case, an external oscillator clock is connected to the XCLKIN pin, which allows for a 3.3-V clock source to be used.

Figure 3−7 shows the OSC and PLL block on the 280x.

Figure 3−7. OSC and PLL Block



The OSC circuit enables a crystal to be attached to the 280x devices using the X1 and X2 pins. If a crystal is not used, then an external oscillator can be directly connected to the XCLKIN pin, the X2 pin is left unconnected, and the X1 pin is tied low. See the *TMS320F2808, TMS320F2806, and TMS320F2801 Digital Signal Processors Data Manual* (literature number SPRS230).

Table 3−7. Possible PLL Configuration Modes

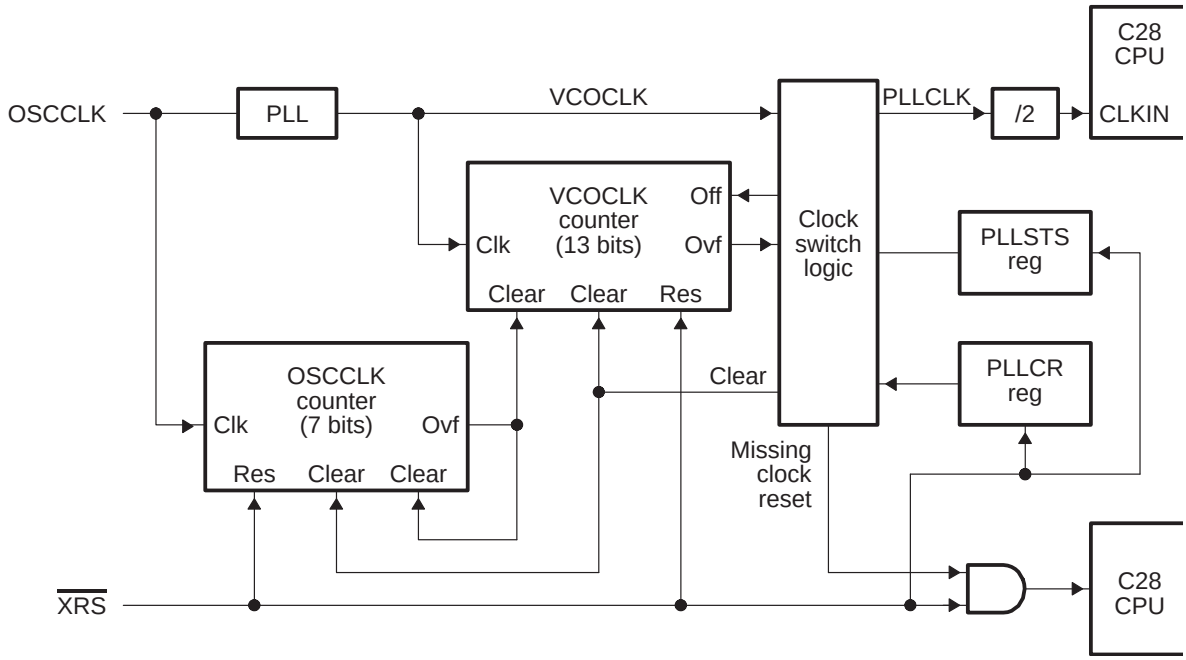
PLL Mode	Remarks	SYSCLKOUT
PLL Off	Invoked by the user setting the PLLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. This can be useful to reduce system noise and for low power operation. The PLLCR register must be set to 0x0000 before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2 or XCLKIN.	OSCCLK
PLL Bypass	The default PLL configuration upon power-up. The PLL itself is bypassed, however the /2 in the module is still used.	OSCCLK/2
PLL Enabled	Achieved by writing a non-zero value n into the PLLCR register. The /2 module in the PLL block divides the output of the PLL by two.	OSCCLK*n/2

3.2.2 Main Oscillator Fail Detection

Due to vibrations, it is possible for the external oscillator to the DSP to become detached and fail to clock the device. When the PLL is being used, the main oscillator fail logic allows the device to detect this condition and default to a known state as described in this section.

Two counters are used to monitor the presence of the OSCCLK signal as shown in Figure 3−8. The first counter is incremented by the OSCCLK signal itself either from the X1/X2 or XCLKIN input. When the PLL is not turned off, the second counter is incremented by the VCOCLK coming out of the PLL block. These counters are configured such that when the 7-bit OSCCLK counter overflows, it clears the 13-bit VCOCLK counter. In normal operating mode, as long as OSCCLK is present, the VCOCLK counter will never overflow.

Figure 3−8. Oscillator Fail-Detection Logic Diagram



If the OSCCLK input signal is missing, then the PLL will output a default “limp mode” frequency and the VCOCLK counter continues to increment. Since the OSCCLK signal is missing, the OSCCLK counter will not increment and, therefore, the VCOCLK counter is not periodically cleared. Eventually, the VCOCLK counter overflows and, the device switches the CLKIN input to the CPU to the limp mode output frequency of the PLL (VCOCLK/2). Then, the oscillator fail detection logic resets the CPU, peripherals and other device logic.

In addition to resetting the device, the missing oscillator logic latches the state into the PLLSTS[MCLKSTS] register bit. When MCLKCSTS is 1, this indicates that the missing oscillator detect logic reset the part and that the CPU is now running at one-half of the limp mode frequency. You should check the MCLKCSTS status bit in the PLLSTS register after a reset to determine if the device was reset by a missing clock condition and, if so, and take the appropriate action. You can reset the missing clock status by writing a 1 to the PLLSTS[MCLKCLR] bit. This will reset the missing clock detection circuits and counters. If OSCCLK is still missing after writing to the MCLKCLR bit, then the VCOCLK counter again overflows and the process will repeat.

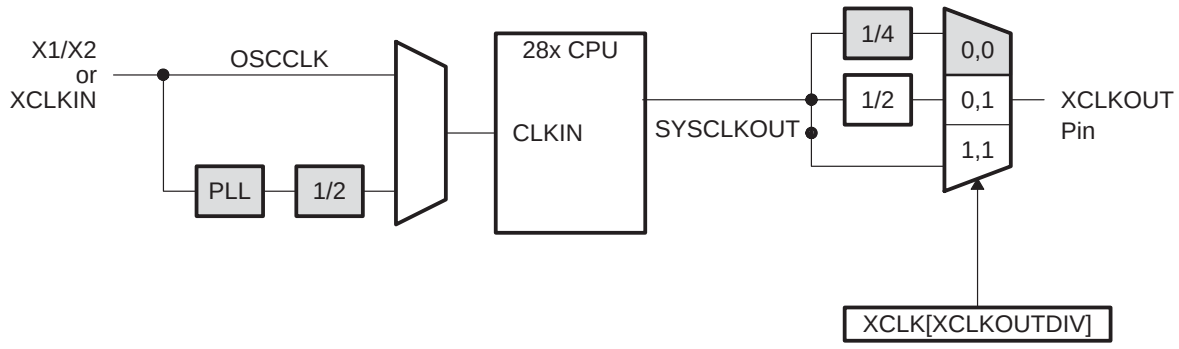
The following should be observed with regards to missing oscillator fail detection:

- Do not write to the PLLCR register when the device is operating in limp mode. When writing to the PLLCR register, the device switches to the CLKIN input to OSCCLK. Since there is no OSCCLK present, the clocks to the system will stop.
- The watchdog is only clocked by OSCCLK and thus cannot generate a reset when OSCCLK is not present. A clock must be present for the watchdog to function.
- In HALT low power mode, all of the clocks to the device are turned off. When the device comes out of HALT mode the oscillator and PLL will power up. The VCOCLK and OSCCLK counters are only enabled after this power-up has completed.

3.2.3 XCLKOUT Generation

The XCLKOUT signal is directly derived from the system clock SYSCLKOUT as shown in Figure 3−9. XCLKOUT can be either equal to, one-half or one-fourth of SYSCLKOUT as determined by the XCLKOUTDIV bits in the XCLK register. By default, at reset XCLKOUT = SYSCLKOUT/4 or XCLKOUT = OSCCLK/8.

Figure 3−9. XCLKOUT Generation



Default at reset

The XCLKOUT signal is active when reset is active. Since XCLKOUT should reflect SYSCLKOUT/4 when reset is low, you can monitor this signal to detect if the device is being properly clocked during debug. There is no internal pullup or pulldown on the XCLKOUT pin.

If XCLKOUT is not being used, it can be turned off by setting the XCLKOUTDIV bits to 1,1 in the XCLK register. In this case, the pin will be 3-stated and can be used as an input.

3.2.4 PLL Clock-in (PLLCR) Register

The PLLCR register is used to change the PLL multiplier of the device. When the CPU writes to the DIV bits, the PLL logic switches the CPU clock (CLKIN) to OSCCLK/2. Once the PLL is stable and has locked at the new specified frequency, the PLL switches CLKIN to the new value as shown in Table 3−8. When this happens, the PLLLOCKS bit in the PLLSTS register is set, indicating that the PLL has finished locking and the device is now running at the new frequency. User software can monitor the PLLLOCKS bit to determine when the PLL has completed locking.

Follow the procedure in Figure 3−10 any time you are writing to the PLLCK register.

3.2.5 External Reference Oscillator Clock Option

TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the DSP chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that ensures start-up and stability over the entire operating range.

Figure 3−10. PLLCR Change Procedure Flow Chart

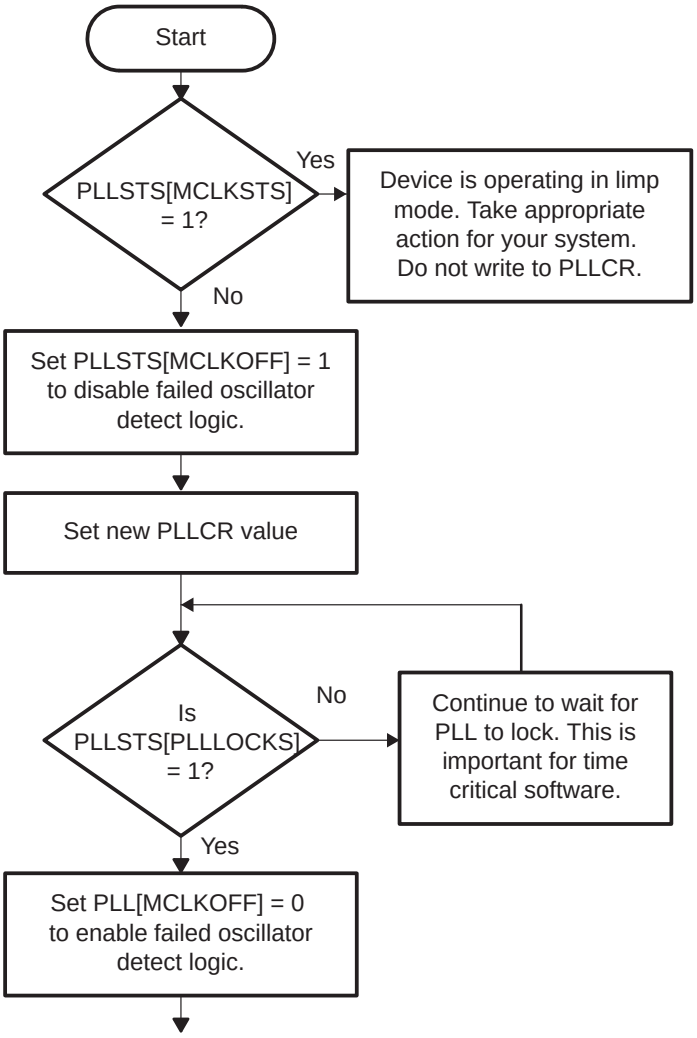
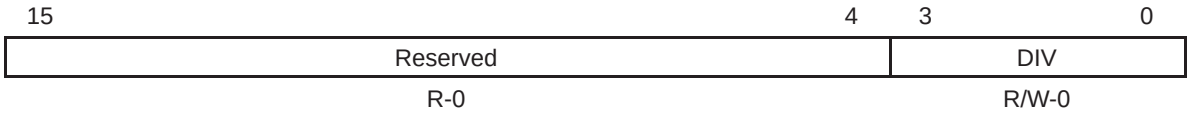


Figure 3−11. PLLCR Register Layout



Legend: R = Read access, W = write access, -0 = value after reset

Note: EALLOW-protected register

The DIV field controls whether the PLL is bypassed or not and sets the PLL clocking ratio when it is not bypassed. PLL bypass is the default mode after reset.

Do not write to the DIV field if the PLL is operating in limp mode as indicated by the PLLSTS [MCLKSTS] bit being set.

Table 3−8. PLLCR Bit Descriptions

DIV Value	Description
0000 (PLL bypass)	CLKIN = OSCCLK/2
0001	CLKIN = (OSCCLK*1)/2
0010	CLKIN = (OSCCLK*2)/2
0011	CLKIN = (OSCCLK*3)/2
0100	CLKIN = (OSCCLK*4)/2
0101	CLKIN = (OSCCLK*5)/2
0110	CLKIN = (OSCCLK*6)/2
0111	CLKIN = (OSCCLK*7)/2
1000	CLKIN = (OSCCLK*8)/2
1001	CLKIN = (OSCCLK*9)/2
1010	CLKIN = (OSCCLK*10)/2
1011 – 1111	reserved

Figure 3−12. PLL Status Register (PLLSTS)

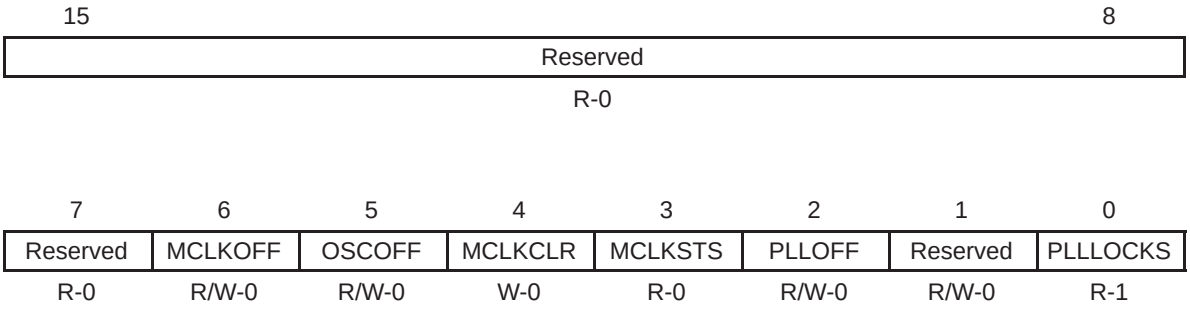


Table 3−9. PLL Status Register (PLLSTS) Field Descriptions

Bit(s)	Field	Description
15−7	Reserved	Reserved
6	MCLKOFF	Missing clock-detect off bit 0 Main oscillator fail-detect logic is enabled. 1 Main oscillator fail-detect logic is disabled. This mode may be used by users not wishing to be affected by the detection circuit. For example, if external clocks are turned off.
5	OSCOFF	Oscillator Clock Off Bit 0 The OSCCLK signal from X1/X2 or XCLKIN is fed to the PLL block. 1 The OSCCLK signal from X1/X2 or XCLKIN is not fed to the PLL block. This mode is useful for testing the main oscillator fail detect logic. This mode does not shut down the internal oscillator.
4	MCLKCLR	Missing Clock Clear Bit 0 Writing a 0 has no effect. This bit always reads 0. 1 Forces the missing clock detection circuits to be cleared and reset. If OSCCLK is still missing, the detection circuit will again generate a reset to the system, set the missing clock status bit (MCLKSTS), and the CPU will be powered by the PLL in Limp Mode frequency.
3	MCLKSTS	Missing Clock Status Bit. Check the status of this bit after a reset to determine whether a missing oscillator condition was detected. Under normal conditions, this bit should be 0. Writes to this bit are ignored. This bit will be cleared by writing to the MCLKCLR bit or by forcing an external reset. 0 Indicates normal operation. A missing clock condition has not been detected. 1 Indicates that OSCCLK was detected as missing. The main oscillator fail detect logic has reset the device and the CPU is now clocked by the PLL in Limp Mode frequency.

Table 3−9. PLL Status Register (PLLSTS) Field Descriptions (Continued)

Bit(s)	Field	Description
2	PLLOFF	PLL Off Bit. This bit turns off the PLL. This is useful for system noise testing. This mode should only be used when PLLCR register is set to 0x0000. 0 PLL On (default) 1 PLL Off If the device is in PLL bypass mode (PLLCR = 0x0000) then STANDBY and HALT low power modes will still work if PLLOFF is set. If the device is not in PLL bypass mode, then STANDBY and HALT low power modes will not work properly.
1	Reserved	This bit is reserved and must always be written as a 0. Do not write a 1 to this bit.
0	PLLLOCKS	PLL Lock Status Bit 0 Indicates that the PLLCR register has been written to and the PLL is currently locking. The CPU is clocked by OSCCLK/2. 1 Indicates that the PLL has finished locking and is now stable.

Figure 3−13. XCLKOUT Register (XCLK)

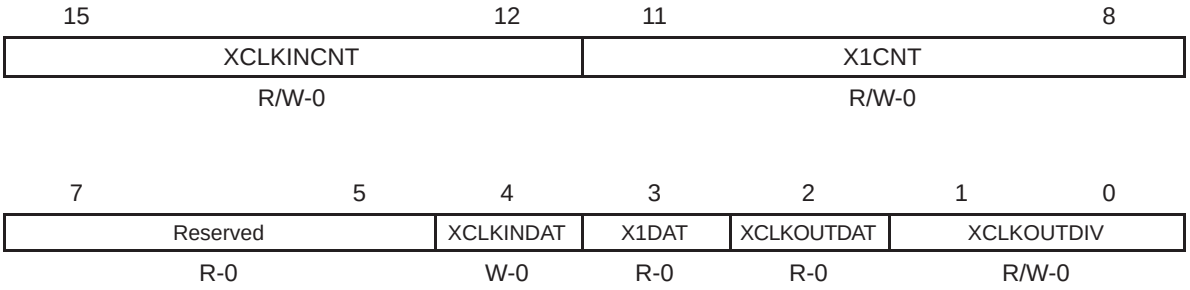


Table 3−10. XCLKOUT Register (XCLK) Field Descriptions

Bit(s)	Field	Description
15−12	XCLKINCNT	XCLKIN Counter. This 4-bit counter starts incrementing after reset if a clock is present on the XCLKIN pin. When the counter reaches 0xF it stops counting. If XCLKIN is not used as clock input, the counter value is 0 or 1. Any write operation to the XCLK register clears the counter asynchronously.
11−8	X1CNT	X1/X2 Counter. This 4-bit counter starts incrementing after reset if a clock is present on the X1/X2 pin. When the counter reaches 0xF it stops counting. If X1/X2 is not used as clock input, the counter value is 0 or 1. Any write operation to the XCLK register clears the counter asynchronously.
7−5	Reserved	Reserved
4	XCLKINDAT	XCLKIN Data Bit. Reading this bit gives the current state of the XCLKIN signal before the XOR gate, which reflects the input state of the XCLKIN pin. When the XCLKIN pin is not used as a clock source, it should be tied low externally.
3	X1DAT	X1 Data Bit. Reading this bit gives the current state of the oscillator cell output just before the XOR gate which will reflect the input state of the X1 pin. When the oscillator is not used, the X1 pin should be pulled low externally and the oscillator internal signal will reflect this.
2	XCLKOUTDAT	XCLKIN Data Bit. Reading this bit gives the current state of the XCLKOUT pin. This feature is only available when XCLKOUT is turned off (XCLKOUTDIV = 1,1).
1−0	XCLKOUTDIV	XCLKOUT Divide Ratio. These two bits select the XCLKOUT frequency ratio relative to SYSCLKOUT. The ratios are: 00 XCLKOUT = SYSCLKOUT/4 (default) 01 XCLKOUT = SYSCLKOUT/2 10 XCLKOUT = SYSCLKOUT 11 XCLKOUT = Off (pin in high-impedance mode and can be read as an input in the XCLKOUTDAT bit)

3.3 Low-Power Modes Block

The low-power modes on the 280x devices are similar to the 240x devices. Table 3−11 summarizes the various modes.

The various low-power modes operate as shown in Table 3−12.

See the *TMS320F2808, TMS320F2806, and TMS320F2801 Digital Signal Processor Data Manual* (literature number SPRS230) for exact timing for entering and exiting the low power modes.

Table 3−11. 280x Low-Power Modes

Mode	LPMCR0[1:0]	OSCCLK	CLKIN	SYSCLKOUT	Exit†
IDLE	00	On	On	On‡	$\overline{\text{XRS}}$, Watchdog interrupt, Any enabled interrupt, XNMI
STANDBY	01	On (watchdog still running)	Off	Off	$\overline{\text{XRS}}$, Watchdog interrupt, GPIO Port A signal, Debugger§
HALT	1X	Off (oscillator and PLL turned off, watchdog not functional)	Off	Off	$\overline{\text{XRS}}$, GPIO Port A Signal, Debugger§

† The Exit column lists which signals or under what conditions the low power mode is exited. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise the IDLE mode is not exited and the device goes back into the indicated low power mode.

‡ The IDLE mode on the 28x behaves differently than on the 24x/240x. On the 28x, the clock output from the CPU (SYSCLKOUT) is still functional while on the 24x/240x the clock is turned off.

§ On the 28x, the JTAG port can still function even if the clock to the CPU (CLKIN) is turned off.

Table 3−12. Low Power Modes

Mode	Description
IDLE Mode:	This mode is exited by any enabled interrupt or an NMI. The LPM block itself performs no tasks during this mode.
STANDBY Mode:	If the LPM bits in the LPMCR register are set to 01, the device enters STANDBY mode when the IDLE instruction is executed. In standby mode the clock input to the CPU (CLKIN) is disabled, which disables all clocks derived from SYSCLKOUT. The oscillator and PLL and watchdog will still function. Before entering the STANDBY mode, you should perform the following tasks: ❑ Enable the WAKEINT interrupt in the PIE module. This interrupt is connected to both the watchdog and the low power mode module interrupt. ❑ If desired, specify one of the GPIO port A signals to wake the device in the GPIOLPMSEL register. The GPIOLPMSEL register is part of the GPIO module. In addition to the selected GPIO signal, the $\overline{\text{XRS}}$ input and the watchdog interrupt, if enabled in the LPMCRO register, can wake the device from the STANDBY mode. ❑ Select the input qualification in the LPMCR0 register for the signal that will wake the device. When the selected external signal goes low, it must remain low a number of OSCCLK cycles as specified by the qualification period in the LPMCR0 register. If the signal should be sampled high during this time, the qualification will restart. At the end of the qualification period, the PLL enables the CLKIN to the CPU and the WAKEINT interrupt is latched in the PIE block. The CPU then responds to the WAKEINT interrupt if it is enabled.
HALT Mode:	If the LPM bits in the LPMCR register are set to 1x, the device enters the HALT mode when the IDLE instruction is executed. In HALT mode all of the device clocks, including the PLL and oscillator, are shut down. Before entering the HALT mode, you should perform the following tasks: ❑ Enable the WAKEINT interrupt in the PIE module. This interrupt is connected to both the watchdog and the low power mode module interrupt. ❑ If desired, specify one of the GPIO port A signals to wake the device in the GPIOLPMSEL register. The GPIOLPMSEL register is part of the GPIO module. In addition to the selected GPIO signal, the XRS input will wake the device from the STANDBY mode. When the selected external signal goes low, it is fed asynchronously to the LPM block. The oscillator is turned on and begins to power up. You must hold the signal low long enough for the oscillator to complete power up. When the signal is driven back high again, this will asynchronously release the PLL and it will begin to lock. Once the PLL has locked, it feeds the CLKIN to the CPU at which time the CPU responds to the WAKEINT interrupt if enabled.

The low-power modes are controlled by the LPMCR0 register (Figure 3−14).

Figure 3−14. Low Power Mode Control 0 Register (LPMCR0)

15	8	7	2	1	0
WDINTE	Reserved	QUALSTDBY		LPM	
R/W-0	R-0	R/W-1		R/W-0	

Legend: R = Read access, W = write access, -0 = value after reset

Note: EALLOW-protected register

Table 3−13. Low Power Mode Control 0 Register (LPMCR0) Field Descriptions

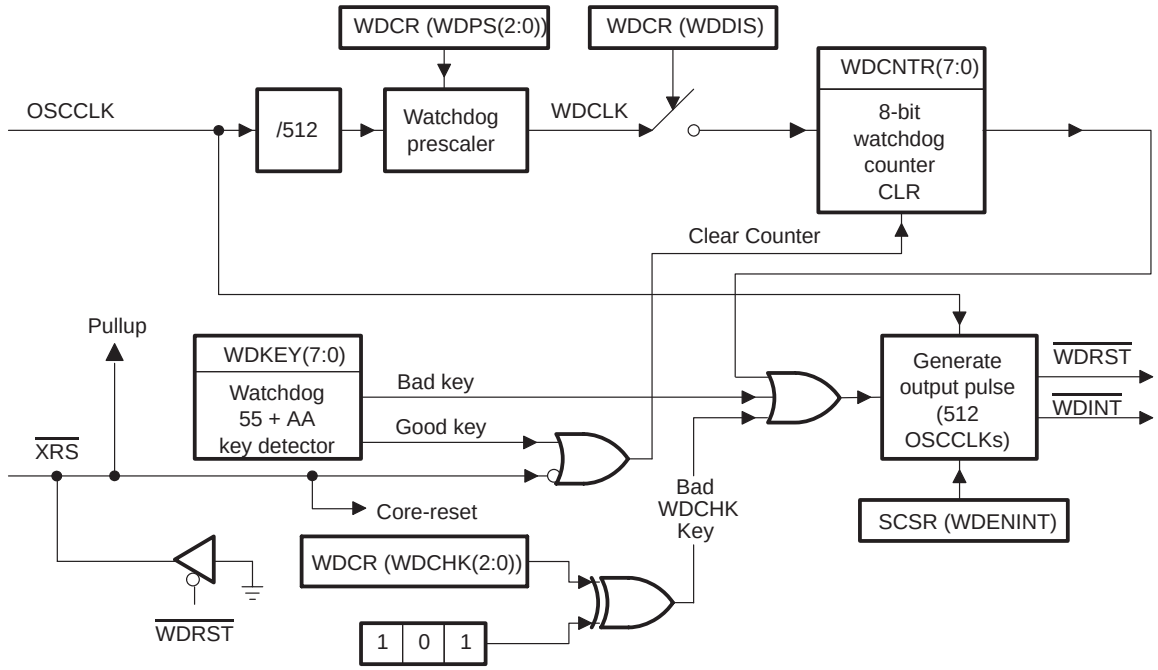
Bits(s)	Field	Description
15	WDINTE	Watchdog interrupt enable 0 The watchdog interrupt is not allowed to wake the device from STANDBY. 1 The watchdog is allowed to wake the device from STANDBY. The watchdog interrupt must also be enabled in the SCSR Register.
14−8	Reserved	Reserved
7−2	QUALSTDBY	Select number of OSCCLK clock cycles to qualify the selected GPIO inputs that wake the device from STANDBY mode. This qualification is only used when in STANDBY mode. The GPIO signals that can wake the device from STANDBY are specified in the GPIOLPMSEL register. 000000 = 2 OSCCLKs 000001 = 3 OSCCLKs . 111111 = 65 OSCCLKs
1−0	LPM†	These bits set the low power mode for the device. 00 Set the low power mode to IDLE 01 Set the low power mode to STANDBY 1x Set the low power mode to HALT

† The low power mode bits (LPM) only take effect when the IDLE instruction is executed. Therefore, you must set the LPM bits to the appropriate mode before executing the IDLE instruction.

3.4 Watchdog Block

The watchdog block on the 280x is similar to the one used on the 240x devices. The watchdog module generates an output pulse, 512 oscillator-clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this, the user disables the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register which resets the watchdog counter. Figure 3−15 shows the various functional blocks within the watchdog module.

Figure 3−15. Watchdog Module



NOTE A: The $\overline{\text{WDRST}}$ signal is driven low for 512 OSCCLK cycles.

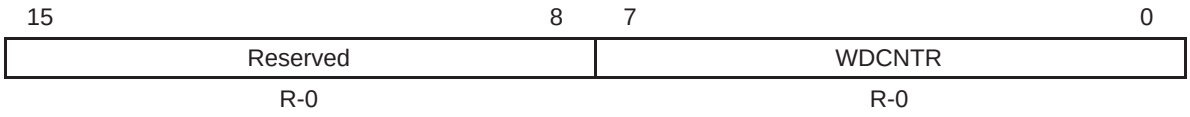
The watchdog interrupt ($\overline{\text{WDINT}}$) signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode timer. If the watchdog interrupt is used to wake up from an IDLE or STANDBY low power mode condition, then make sure that the $\overline{\text{WDINT}}$ signal goes back high again before attempting to go back into the IDLE or STANDBY mode. You can determine the state of this signal by reading the watchdog interrupt enable (WDENINT) bit in the SCSR register.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the watchdog. The watchdog module runs off the oscillator clock. The $\overline{\text{WDINT}}$ signal is fed to the LPM block so that it can wake the device from STANDBY (if enabled). See Low-Power Modes Block section of this data sheet for more details.

In IDLE mode, the $\overline{\text{WDINT}}$ signal can generate an interrupt to the CPU, (the WAKEINT interrupt in the PIE), to take the CPU out of IDLE mode.

In HALT mode, this feature cannot be used because the oscillator (and PLL) are turned off and, therefore, so is the watchdog.

Figure 3−16. Watchdog Counter Register (WDCNTR)



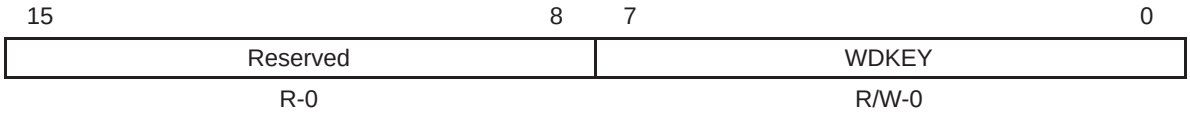
Legend: R = Read access, W = write access, -0 = value after reset

Note: EALLOW-protected register

Table 3−14. Watchdog Counter Register (WDCNTR) Field Descriptions

Bit(s)	Field	Description
15−8	Reserved	Reserved
7−0	WDCNTR	These bits contain the current value of the WD counter. The 8-bit counter continually increments at the watchdog clock (WDCLK), rate. If the counter overflows, then the watchdog initiates a reset. If the WDKEY register is written with a valid combination, then the counter is reset to zero. The watchdog clock rate is configured in the WDCR register.

Figure 3−17. Watchdog Reset Key Register (WDKEY)



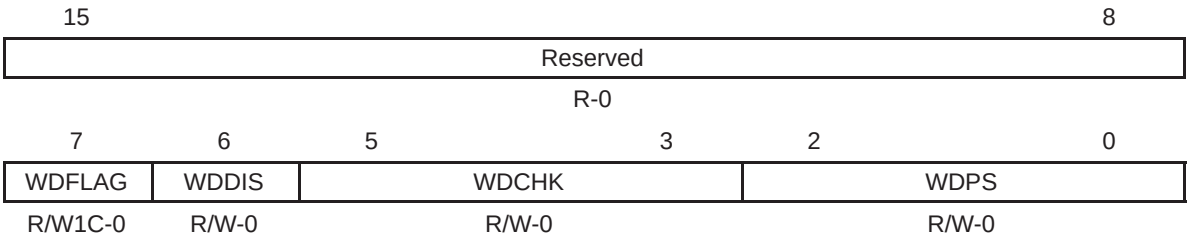
Legend: R = Read access, W = write access, -0 = value after reset

Note: EALLOW-protected register

Table 3−15. Watchdog Reset Key Register (WDKEY) Field Descriptions

Bit(s)	Field	Description
15−8	Reserved	Reserved
7−0	WDKEY	Writing 0x55 followed by 0xAA causes the WDCNTR bits to be cleared. Writing any other value causes an immediate watchdog reset to be generated. Reads return the value of the WDCR register.

Figure 3−18. Watchdog Control Register (WDCR)



Legend: R = Read access, W = write access, W1C = write 1 to clear, -0 = value after reset

Note: EALLOW-protected register

Table 3−16. Watchdog Control Register (WDCR) Field Descriptions

Bit(s)	Field	Description
15−8	Reserved	Reserved
7	WDFLAG	Watchdog reset status flag bit 0 An external device or power-up reset condition. The bit remains latched until you write a 1 to clear the condition. Writes of 0 are ignored. 1 indicates a watchdog reset ($\overline{\text{WDRST}}$) generated the reset condition. .
6	WDDIS	Watchdog disable. On reset, the watchdog module is enabled. 0 Enables the watchdog module. WDDIS can be modified only if the WDOVERRIDE bit in the SCSR2 register is set to 1. 1 Disables the watchdog module
5−3	WDCHK	Watchdog check. You must ALWAYS write 1,0,1 to these bits whenever a write to this register is performed. Writing any other value causes an immediate reset to the core (if WD is enabled).
2−0	WDPS	These bits configure the watchdog counter clock (WDCLK) rate relative to OSCCLK/512: 000 WDCLK = OSCCLK/512/1 001 WDCLK = OSCCLK/512/1 010 WDCLK = OSCCLK/512/2 011 WDCLK = OSCCLK/512/4 100 WDCLK = OSCCLK/512/8 101 WDCLK = OSCCLK/512/16 110 WDCLK = OSCCLK/512/32 111 WDCLK = OSCCLK/512/64

When the $\overline{\text{XRS}}$ line is low, the WDFLAG bit is forced low. The WDFLAG bit is only set if a rising edge on $\overline{\text{WDRST}}$ signal is detected (after synch and an 8192 SYSCLKOUT cycle delay) and the $\overline{\text{XRS}}$ signal is high. If the $\overline{\text{XRS}}$ signal is low when $\overline{\text{WDRST}}$ goes high, then the WDFLAG bit remains at 0. In a typical application, the $\overline{\text{WDRST}}$ signal connects to the $\overline{\text{XRS}}$ input. Hence to distinguish between a watchdog reset and an external device reset, an external reset must be longer in duration then the watchdog pulse.

3.4.1 Emulation Considerations

The watchdog module behaves as follows under various debug conditions:

CPU Suspended: When the CPU is suspended, the watchdog clock (WDCLK) is suspended.

Run-Free Mode: When the CPU is placed in run-free mode, then the watchdog module resumes operation as normal.

Real-Time Single-Step Mode: When the CPU is in real-time single-step mode, the watchdog clock (WDCLK) is suspended. The watchdog remains suspended even within real-time interrupts.

Real-Time Run-Free Mode: When the CPU is in real-time run-free mode, the watchdog operates as normal.

3.5 32-Bit CPU Timers 0/1/2

This section describes the three 32-bit CPU-timers (Figure 3−19) on the 280x devices (TIMER0/1/2).

CPU-Timers 1 and 2 are reserved by TI software-use such as DSP-BIOS. CPU-Timer 0 can be used in user applications.

In the 280x devices, the CPU-timer interrupt signals ($\overline{\text{TINT0}}$, $\overline{\text{TINT1}}$, $\overline{\text{TINT2}}$) are connected as shown in Figure 3−20.

Figure 3−19. CPU-Timers

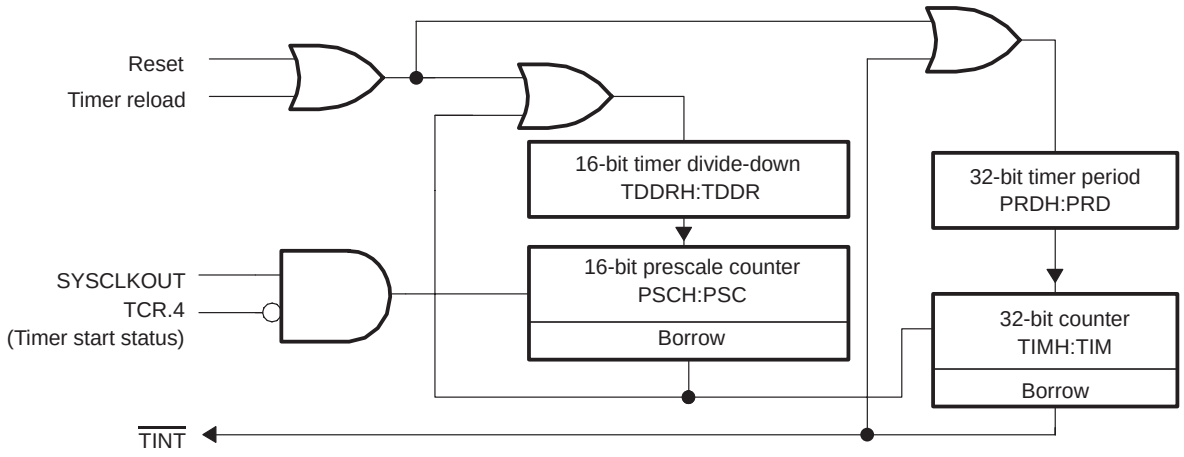
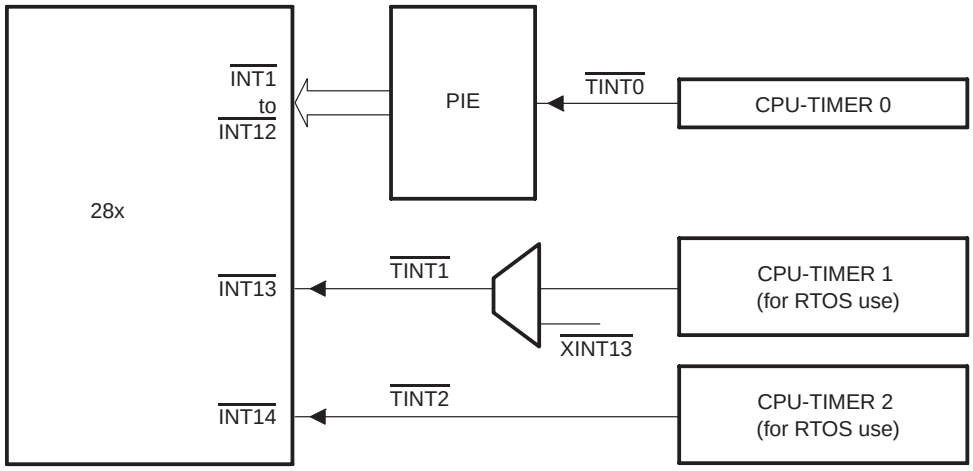


Figure 3−20. CPU-Timer Interrupts Signals and Output Signal



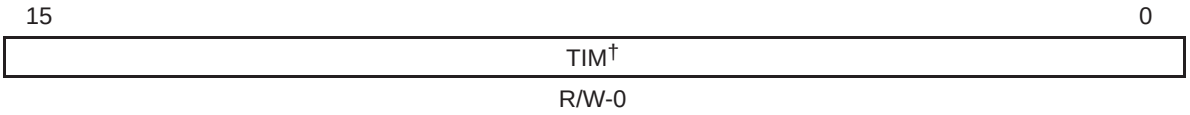
NOTES: A. The timer registers are connected to the Memory Bus of the 28x processor.
B. The timing of the timers is synchronized to SYSCLKOUT of the processor clock.

The general operation of the CPU-timer is as follows: The 32-bit counter register TIMH:TIM is loaded with the value in the period register PRDH:PRD. The counter register decrements at the SYSCLKOUT rate of the 28x. When the counter reaches 0, a timer interrupt output signal generates an interrupt pulse. The registers listed in Table 3−17 are used to configure the timers.

Table 3−17. CPU-Timers 0, 1, 2 Configuration and Control Registers

Name	Address	Size (x16)	Description
TIMER0TIM	0x0C00	1	CPU-Timer 0, Counter Register
TIMER0TIMH	0x0C01	1	CPU-Timer 0, Counter Register High
TIMER0PRD	0x0C02	1	CPU-Timer 0, Period Register
TIMER0PRDH	0x0C03	1	CPU-Timer 0, Period Register High
TIMER0TCR	0x0C04	1	CPU-Timer 0, Control Register
Reserved	0x0C05	1	
TIMER0TPR	0x0C06	1	CPU-Timer 0, Prescale Register
TIMER0TPRH	0x0C07	1	CPU-Timer 0, Prescale Register High
TIMER1TIM	0x0C08	1	CPU-Timer 1, Counter Register
TIMER1TIMH	0x0C09	1	CPU-Timer 1, Counter Register High
TIMER1PRD	0x0C0A	1	CPU-Timer 1, Period Register
TIMER1PRDH	0x0C0B	1	CPU-Timer 1, Period Register High
TIMER1TCR	0x0C0C	1	CPU-Timer 1, Control Register
Reserved	0x0C0D	1	
TIMER1TPR	0x0C0E	1	CPU-Timer 1, Prescale Register
TIMER1TPRH	0x0C0F	1	CPU-Timer 1, Prescale Register High
TIMER2TIM	0x0C10	1	CPU-Timer 2, Counter Register
TIMER2TIMH	0x0C11	1	CPU-Timer 2, Counter Register High
TIMER2PRD	0x0C12	1	CPU-Timer 2, Period Register
TIMER2PRDH	0x0C13	1	CPU-Timer 2, Period Register High
TIMER2TCR	0x0C14	1	CPU-Timer 2, Control Register
Reserved	0x0C15	1	
TIMER2TPR	0x0C16	1	CPU-Timer 2, Prescale Register
TIMER2TPRH	0x0C17	1	CPU-Timer 2, Prescale Register High
Reserved	0x0C18 0x0C3F	40	

Figure 3−21. TIMERxTIM Register†



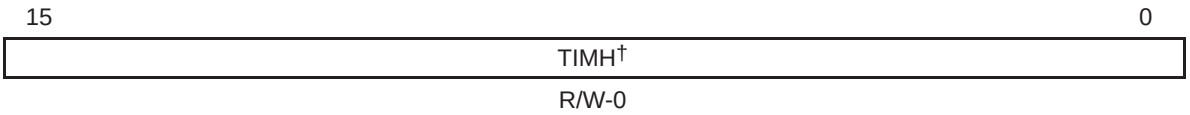
Legend: R = Read access, W = write access, -0 = value after reset

Table 3−18. TIMERxTIM Register Field Descriptions

Bit(s)	Field	Description
15−0	TIM	CPU-Timer Counter Registers (TIMH:TIM): The TIM register holds the low 16 bits of the current 32-bit count of the timer. The TIMH register holds the high 16 bits of the current 32-bit count of the timer. The TIMH:TIM decrements by one every (TDDRH:TDDR+1) clock cycles, where TDDRH:TDDR is the timer prescale divide-down value. When the TIMH:TIM decrements to zero, the TIMH:TIM register is reloaded with the period value contained in the PRDH:PRD registers. The timer interrupt ($\overline{\text{TINT}}$) signal is generated.

† x = 0, 1, or 2

Figure 3−22. TIMERxTIMH Register†



Legend: R = Read access, W = write access, -0 = value after reset

Table 3−19. TIMERxTIMH Register Field Description

Bit(s)	Field	Description
15−0	TIMH	See description for TIMERxTIM.

† x = 0, 1, or 2

Figure 3−23. TIMERxPRD Register†

15	0
PRD	
R/W-0	

Legend: R = Read access, W = write access, -0 = value after reset

Table 3−20. TIMERxPRD Register Field Description

Bit(s)	Field	Description
15−0	PRD	CPU-Timer Period Registers (PRDH:PRD): The PRD register holds the low 16 bits of the 32-bit period. The PRDH register holds the high 16 bits of the 32-bit period. When the TIMH:TIM decrements to zero, the TIMH:TIM register is reloaded with the period value contained in the PRDH:PRD registers, at the start of the next timer input clock cycle (the output of the prescaler). The PRDH:PRD contents are also loaded into the TIMH:TIM when you set the timer reload bit (TRB) in the Timer Control Register (TCR).

† x = 0, 1, or 2

Figure 3−24. TIMERxPRDH Register†

15	0
PRDH	
R/W-0	

Legend: R = Read access, W = write access, -0 = value after reset

Table 3−21. TIMERxPRDH Register Field Description

Bit(s)	Field	Description
15−0	PRDH	See description for TIMERxPRD

† x = 0, 1, or 2

Figure 3−25. TIMERxTCR Register†

15	14	13 12	11	10	9 8
TIF	TIE	Reserved	FREE	SOFT	Reserved
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R-0

7 6	5	4	3 0
Reserved	TRB	TSS	Reserved
R-0	R/W-0	R/W-0	R-0

Legend: R = Read access, W = write access, -0 = value after reset

Table 3−22. TIMERxTCR Register Field Descriptions

Bit(s)	Field	Description
15	TIF	CPU-Timer Interrupt Flag. This flag gets set when the timer decrements to zero. TIF can be cleared by software writing a 1, but it can only be set by the timer reaching zero. Writing a 1 to this bit clears it, writing a zero has no effect.
14	TIE	CPU-Timer Interrupt Enable. If the timer decrements to zero, and TIE is set, the timer asserts its interrupt request.
13−12	Reserved	Reserved
11 10	FREE SOFT	CPU-Timer Emulation Modes: These bits are special emulation bits that determine the state of the timer when a breakpoint is encountered in the high-level language debugger. If the FREE bit is set to 1, then, upon a software breakpoint, the timer continues to run (that is, free runs). In this case, SOFT is a *don't care*. But if FREE is 0, then SOFT takes effect. In this case, if SOFT = 0, the timer halts the next time the TIMH:TIM decrements. If the SOFT bit is 1, then the timer halts when the TIMH:TIM has decremented to zero.

FREE	SOFT	CPU-Timer Emulation Mode
0	0	Stop after the next decrement of the TIMH:TIM (hard stop)
0	1	Stop after the TIMH:TIM decrements to 0 (soft stop)
1	0	Free run
1	1	Free run

Note: That in the SOFT STOP mode, the timer generates an interrupt before shutting down (since reaching 0 is the interrupt causing condition).

9−6	Reserved	Reserved
5	TRB	CPU-Timer Reload bit. When you write a 1 to TRB, the TIMH:TIM is loaded with the value in the PRDH:PRD, and the prescaler counter (PSCH:PSC) is loaded with the value in the timer divide-down register (TDDRH:TDDR). The TRB bit is always read as zero.
4	TSS	CPU-Timer stop status bit. TSS is a 1-bit flag that stops or starts the timer. To stop the timer, set TSS to 1. To start or restart the timer, set TSS to 0. At reset, TSS is cleared to 0 and the timer immediately starts.
3−0	Reserved	Reserved

† x = 0, 1, or 2

Figure 3−26. TIMERxTPR Register†

15	8	7	0
PSC		TDDR	
R-0		R/W-0	

Legend: R = Read access, W = write access, -0 = value after reset

Table 3−23. TIMERxTPR Register Field Descriptions

Bit(s)	Field	Description
15−8	PSC	CPU-Timer Prescale Counter. These bits hold the current prescale count for the timer. For every timer clock source cycle that the PSCH:PSC value is greater than 0, the PSCH:PSC decrements by one. One timer clock (output of the timer prescaler) cycle after the PSCH:PSC reaches 0, the PSCH:PSC is loaded with the contents of the TDDRH:TDDR, and the timer counter register (TIMH:TIM) decrements by one. The PSCH:PSC is also reloaded whenever the timer reload bit (TRB) is set by software. The PSCH:PSC can be checked by reading the register, but it cannot be set directly. It must get its value from the timer divide-down register (TDDRH:TDDR). At reset, the PSCH:PSC is set to 0.
7−0	TDDR	CPU-Timer Divide-Down. Every (TDDRH:TDDR + 1) timer clock source cycles, the timer counter register (TIMH:TIM) decrements by one. At reset, the TDDRH:TDDR bits are cleared to 0. To increase the overall timer count by an integer factor, write this factor minus one to the TDDRH:TDDR bits. When the prescaler counter (PSCH:PSC) value is 0, one timer clock source cycle later, the contents of the TDDRH:TDDR reload the PSCH:PSC, and the TIMH:TIM decrements by one. TDDRH:TDDR also reloads the PSCH:PSC whenever the timer reload bit (TRB) is set by software.

† x = 0, 1, or 2

Figure 3−27. TIMERxTPRH Register†

15	8	7	0
PSCH		TDDRH	
R-0		R/W-0	

Legend: R = Read access, W = write access, -0 = value after reset

Table 3−24. TIMERxTPRH Register Field Descriptions

Bit(s)	Field	Description
15−8	PSCH	See description of TIMERxTPR.
7−0	TDDRH	See description of TIMERxTPR.

† x = 0, 1, or 2

This page is intentionally left blank.

Chapter 4

General-Purpose Input/Output (GPIO)

The GPIO MUX registers are used to select the operation of shared pins on the 280x devices. The pins can be individually selected to operate as Digital I/O or connected to Peripheral I/O signals (via the GPxMUX registers). If selected for Digital I/O mode, registers are provided to configure the pin direction (via the GPxDIR registers) and to qualify the input signal to remove unwanted noise (via the GPxQSEL1/2 and GPxCTRL registers).

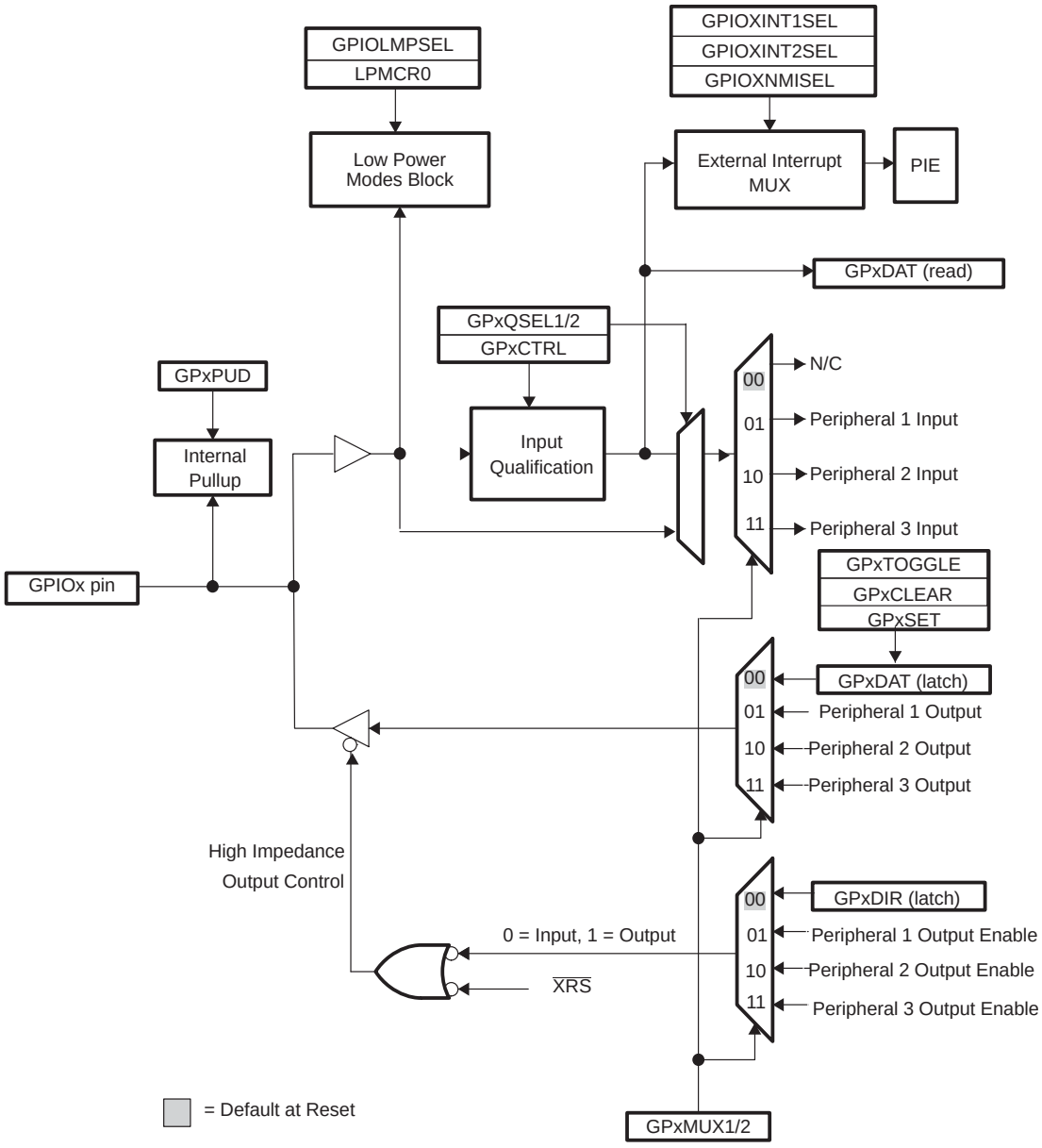
Topic **Page**

4.1	GPIO Module Overview	4-2
4.2	Input Qualification	4-4
4.3	Configuration Overview	4-6
4.4	GPIO and Peripheral MUXing	4-10
4.5	Register Bit Definitions	4-23

4.1 GPIO Module Overview

On the 2808, the GPIO MUX can multiplex up to three independent peripheral signals on a single GPIO pin in addition to providing individual pin bit IO capability. There are two 32-bit IO ports on the 280x devices. Port A consists of GPIO0−GPIO31 and Port B consists of GPIO32−GPIO34. The remaining IOs on Port B are currently reserved for future expansion. Figure 4−1 shows the basic modes of operation for the GPIO module.

Figure 4−1. Modes of Operation



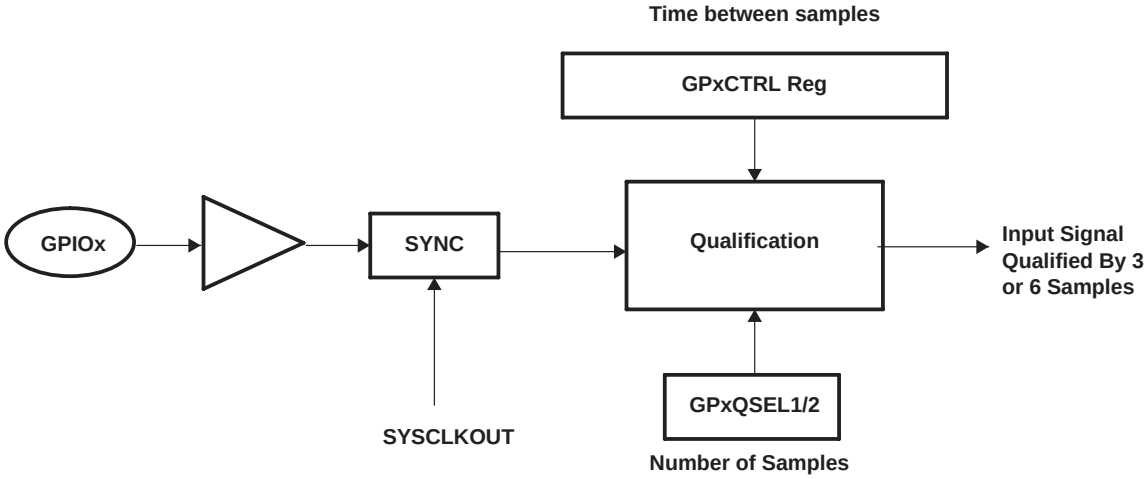
Notes: 1) x stands for the port, either A or B. For example, GPxDIR refers to either the GPADIR and GPBDIR register depending on the particular GPIO pin selected
2) GPxDAT latch/read are accessed at the same memory location.

4.2 Input Qualification

Input qualification is very flexible on the 280x devices. You can select the type of input qualification for each GPIO pin by configuring the GPxQSEL1 and GPxQSEL2 registers in one of the three following options:

- Synchronization to SYSCLKOUT only − This is the default mode of all the GPIO pins at reset. In this mode, the input signal is simply synchronized to the input system clock (SYSCLKOUT). No further qualification is performed on the signal.
- Qualification using a sampling window − In this mode, the input signal is first synchronized to the system clock (SYSCLKOUT) and then qualified by a specified number of cycles before the input is allowed to change. Figure 4−2 shows how the input qualification is performed to eliminate unwanted noise.

Figure 4−2. Input Qualification

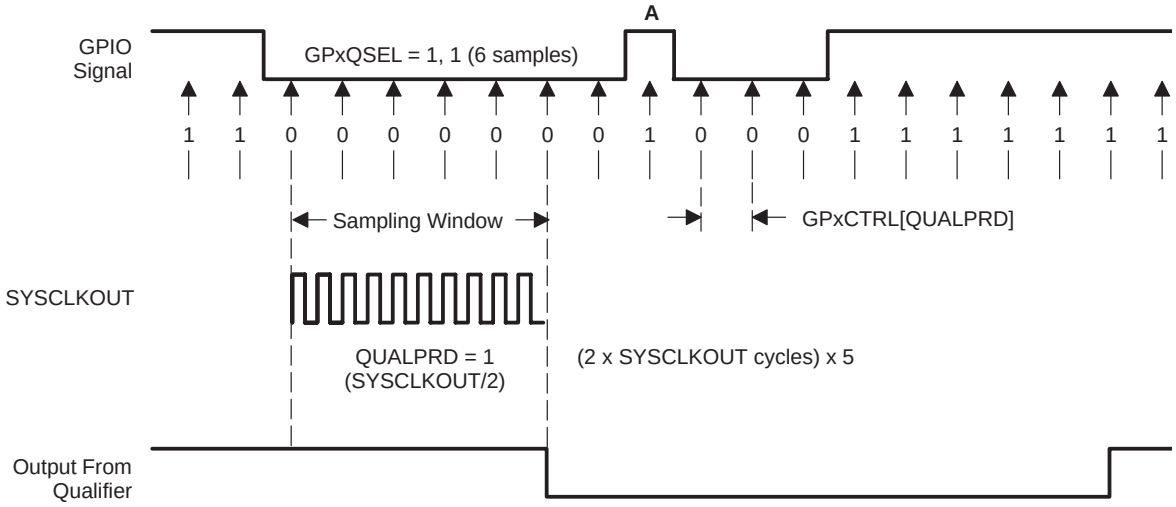


To qualify the signal, the input is synchronized to SYSCLKOUT and then sampled at a regular period. The sampling period is specified by the QUALPRD bits in the GPxCTRL register and is configurable in groups of 8 signals. This specifies the amount of time between samples relative to SYSCKLOUT.

The sampling window, or the number of times the signal is sampled, is either 3-samples or 6-samples wide as specified by the GPxQSEL1/2 registers. When 3 or 6 consecutive cycles are the same, then the input is changed. Because the incoming signal is asynchronous, there can be up to one SYSCLKOUT cycle delay for synchronization to SYSCLKOUT before the sampling window begins.

In Figure 4−3, the glitch (A) will be ignored by the input qualifier. The QUALPRD bit field in the GPxCTRL register specifies the sampling period from 0x00 to 0xFF. The input qualification period is equal to SYSCLKOUT when QUALPRD = 0,0. For any other value of n, the qualification is sampled at a rate 2*n SYSCLKOUT cycles. That is, at every 2n SYSCLKOUT cycle, the GPIO pin will be sampled. For the input qualifier to detect a change, the input should be stable for 3 or 6 samples as specified in the GPxQSEL1/2 register. In Figure 4−3, the sampling window in the GPxQSEL1/2 register has been configured to 6-sample qualification.

Figure 4−3. Input Qualifier Clock Cycles



- No synchronization − This mode is used for peripherals where input synchronization is not required or the peripheral itself performs the synchronization. Examples include communication ports SCI, SPI, eCAN, and I^2C or ePWM trip zone signals, which should not depend on the presence of SYSCLKOUT. This option is not valid if the pin is used as a GPIO input pin. If the pin is configured as a GPIO input and asynch is selected in the GPxQSEL1/2, then the qualification defaults to synchronization to SYSCLKOUT.

4.3 Configuration Overview

To configure the GPIO module, use the following steps:

Step 1: Determine the function of the pin – will the pin be an I/O or a peripheral function? This will help determine how to further configure the pin.

Step 2: If required, enable the internal pullup resistor for the pin. To enable the pullup write to the required bit in the GPxPUD register. The internal pullup resisters are disabled by default. The boot loaders enable pullups on the pins used to load data. The pullups are not, however, enabled for the pins used to determine boot mode selection.

Step 3: If the pin will be used as is an input, specify the required input qualification, if any. The input qualification is specified in the GPxCTRL and GPxQSEL1/2 registers. By default, all of the input signals are synchronized to SYSCLKOUT only.

Step 4: Configure the GPxMUX1/2 registers such that the pin is an I/O or one of three peripheral functions. By default, all GPIO pins are configured at reset as general purpose inputs.

Step 5: If the pin is configured as an I/O, specify the direction of the pin as either input or output in the GPxDIR register. By default, all GPIO pins are inputs. To change the pin from input to output, first load the output latch with the value to be driven by writing the appropriate value to the GPxCLEAR, GPxSET, or GPxTOGGLE register. Once the output latch is loaded, change the pin direction from input to output via the GPxDIR register. The output latch for all pins is cleared at reset.

Step 6: Specify which pins, if any, will be able to wake the device from HALT and STANDBY low power modes. The pins are specified in the GPIOLPMSEL register.

Step 7: Specify the source for the $\overline{\text{XINT1}}$, $\overline{\text{XINT2}}$, and $\overline{\text{XNMI}}$ interrupts. For each interrupt you can specify one of the port A signals as the source. This is done by specifying the source in the GPIOXINT1SEL, GPIOXINT2SEL, and GPIOXNMISEL registers.

For pins that are specified as I/O, you can change the values on the pins by using the following registers:

- GPxDAT Registers: Each I/O port has one data register. The data register is a R/W register that, when read, reflects the current state of the input I/O signal after qualification. Writing to the register sets the corresponding output latch.

  If GPxDAT.bit = 0, AND the pin is an output, then set the output latch low and pull the pin low.

  If GPxDAT.bit = 1, AND the pin is an output, then set the output latch high and pull the pin high.

  If the pin is not configured as a GPIO output, the data is latched only.

  When using the GPxDAT register to change the level of an output pin, you should be cautious not to accidentally change the level of another pin. For example, if you mean to change the output latch level of GPIOA0 by writing to the GPADAT register bit 0, using a read-modify-write instruction. The problem can occur if another I/O port A signal changes level between the read and the write stage of the instruction. You can also change the state of that output latch. You can avoid this scenario by using the GPxSET, GPxCLEAR, and GPxTOGGLE registers to load the output latch instead.

- GPxSET Registers: Each I/O port has one set register. The set registers are write-only registers that read back 0. If the corresponding pin is configured as an output, then writing a 1 to that bit in the set register will set the output latch and pull the corresponding pin high. Writing a 0 to a bit has no effect.

  If GPxSET.bit = 0, ignored

  If GPxSET.bit = 1, AND the pin is an output, then pull the pin high

  If the pin is not configured as a GPIO output, then the latch is set high but not used to drive the pin.

- GPxCLEAR Registers: Each I/O port has one clear register. The clear registers are write-only registers that read back 0. If the corresponding pin is configured as an output, then writing a 1 to that bit in the clear register clears the output latch and pulls the corresponding pin low. Writing a 0 to a bit has no effect.

  If GPxCLEAR.bit = 0, ignored

  If GPxCLEAR.bit = 1, AND the pin is an output, then pull the pin low

  If the pin is not configured as a GPIO output, then the latch is cleared but not used to drive the pin.

- GPxTOGGLE: Each I/O port has one toggle register. The toggle registers are write-only registers that read back 0. If the corresponding pin is configured as an output, then writing a 1 to that bit in the toggle register flips the output latch and pulls the corresponding pin in the opposite direction. That is, if the output pin is low, writing a 1 to the corresponding bit in the toggle register will pull the pin high. Likewise, if the output pin is high, writing a 1 to the corresponding bit in the toggle register will pull the pin low. Writing a 0 to a bit has no effect.

  If GPxTOGGLE.bit = 0, ignored

  If GPxTOGGLE.bit = 1, AND the pin is an output, then pull the pin in the opposite direction

  If the pin is not configured as a GPIO output, then the latch state is flipped but not used to drive the pin.

Table 4−1 lists the GPIO MUX Registers.

Table 4−1. GPIO Control Registers

Name	Address	Size (x16)	Register Description
GPACTRL	0x6F80	2	GPIO A Control Register (0 −31)
GPAQSEL1	0x6F82	2	GPIO A Qualifier Select 1 Register (0 −15)
GPAQSEL2	0x6F84	2	GPIO A Qualifier Select 1 Register (16−31)
GPAMUX1	0x6F86	2	GPIO A MUX 1 Register (0−15)
GPAMUX2	0x6F88	2	GPIO A MUX 2 Register (16−31)
GPADIR	0x6F8A	2	GPIO A Direction Register (0−31)
GPAPUD	0x6F8C	2	GPIO A Pull Up Disable Register (0−31)
Reserved	0x6F8E –0x6F8F	2	
GPBCTRL	0x6F90	2	GPIO B Control Register (32−35)
GPBQSEL1	0x6F92	2	GPIO B Qualifier Select 1 Register (32−35)
GPBQSEL2	0x6F94	2	Reserved
GPBMUX1	0x6F96	2	GPIO B MUX 1 Register (32−35)
GPBMUX2	0x6F98	2	Reserved
GPBDIR	0x6F9A	2	GPIO B Direction Register (32−35)
GPBPUD	0x6F9C	2	GPIO B Pull Up Disable Register (32−35)
Reserved	0x6F9E −0x6FB0	34	

Table 4−2. GPIO Data Registers

Name	Address	Size (x16)	Register Description
GPADAT	0x6FC0	2	GPIO A Data Register (0−31)
GPASET	0x6FC2	2	GPIO A Set Register (0−31)
GPACLEAR	0x6FC4	2	GPIO A Clear Register (0−31)
GPATOGGLE	0x6FC6	2	GPIO A Toggle Register (0−31)
GPBDAT	0x6FC8	2	GPIO B Data Register (32−34)
GPBSET	0x6FCA	2	GPIO B Set Register (32−34)
GPBCLEAR	0x6FCC	2	GPIO B Clear Register (32−34)
GPBTOGGLE	0x6FCE	2	GPIO B Toggle Register (32−34)
Reserved	0x70FC − 0x70FF	4	

Note: These registers are NOT EALLOW protected.

Table 4−3. GPIO Interrupt and Low Power Mode Select Registers

Name	Address	Size (x16)	Register Description
GPIOXINT1SEL	0x6FE0	1	XINT1 GPIO Input Select REgister (0−31)
GPIOXINT2SEL	0x6FE1	1	XINT2 GPIO Input Select Register (0−31)
GPIOXNMISEL	0x6FE2	1	XNMI GPIO Input Select Register (0−31)
Reserved	0x6FE3 – 0x6FE7	5	
GPIOLPMSEL	0x6FE8	1	LPM GPIO Select Register (0−31)

4.4 GPIO and Peripheral MUXing

The 280x devices MUX up to three different peripheral functions along with a GPIO port per pin. This allows you to pick and choose a peripheral mix that will work best for the particular application.

Table 4−5, Table 4−6, and Table 4−6 show an overview of the possible MUX combinations for the 2808, 2806, and 2801 devices sorted by GPIO pin. The second column indicates the I/O name of the pin on the device. Since the I/O name is unique, it is the best way to identify a particular pin. Therefore, the register descriptions in this section only refer to the GPIO name of a particular pin. The MUX register and particular bits that control the selection for each pin are indicated in the first column.

For example, the MUX for the GPIO7 pin is controlled by writing to GPAMUX[15:14]. By writing to these bits, the pin is configured as either GPIO7, or one of up to three peripheral functions. The GPIO7 pin on a 2808 can be configured as follows:

If GPAMUX1[15:14] = 0,0	Pin configured as GPIO7
If GPAMUX1[15:14] = 0,1	Pin configured as EPWM4B (O)
If GPAMUX1[15:14] = 1,0	Pin configured as SPISTED (I/O)
If GPAMUX1[15:14] = 1,1	Pin configured as ECAP2 (I/O)

All the devices in the 280x family have the same MUXing scheme. The only difference is that if a peripheral is not available on a particular device, that MUX selection is reserved on that device.

Some peripherals can be assigned to more than one pin via the MUX registers. For example, the CAP1 function can be assigned to either the GPIO5 or GPIO24 pin, depending on individual system requirements. For example, ECAP1 to GPIO5, set the GPAMUX1[11:10] bits to 1,1. Instead, to assign ECAP1 to GPIO24, set the GPAMUX2[17:16] bit to 0,1.

If no pin is configured as an input to a peripheral, or if more then one pin is configured as an input for the same peripheral, then the input to the peripheral will either default to a 0 or a 1 as shown in Table 4−4. For example, if ECAP1 were assigned to both GPIO5 and GPIO24, the input to the eCAP1 peripheral would default to a high state as shown in Table 4−4.

Table 4−5, Table 4−6, and Table 4−7 show the MUX options for 2808, 2806, and 2801 devices, respectively. Table 4−9 provides a sorting of the MUX table by peripheral. This table can be used to quickly identify the GPIO pins that can be assigned to a particular peripheral function.

Table 4−4. Default State of Peripheral Input

Peripheral Pin	Description	Default
$\overline{\text{TZ1}}$−TZ6	Trip zone 1−6	1
EPWMSYNCI	ePWM Synch Input	0
ECAP1−ECAP4	eCAP1−4 input	1
EQEP1A, EQEP2A	eQEP input	1
EQEP1I, EQEP2I	eQEP index	1
EQEP1S, EQEP2S	eQEP strobe	1
SPICLKA – SPICLKD	SPI-A – SPI-D clock	1
SPISTEA – SPISTED	SPI-A – SPI-D transmit enable	0
SPISIMOA − SPISIMOD	SPI-A – SPI-D Slave-in, master-out	1
SPISOMIA – SPISOMID	SPI-A – SPI-D Slave-out, master-in	1
SCIRXDA – SCIRXDB	SCI-A – SCI-B receive	1
CANRXA− CANRXB	eCAN-A – eCAN-B receive	1
SDAA	I2C data	1
SCLA1	I2C clock	1

Table 4−5. 2808 GPIO MUX Table

Register Bits	Bits = 0,0 (Default)	Bits = 0,1	Bits = 1,0	Bits = 1,1
		GPAMUX1		
1:0	GPIO0	EPWM1A (O)	Reserved	Reserved
3:2	GPIO1	EPWM1B (O)	SPISIMOD (I/O)	Reserved
5:4	GPIO2	EPWM2A (O)	Reserved	Reserved
7:6	GPIO3	EPWM2B (O)	SPISOMID (I/O)	Reserved
9:8	GPIO4	EPWM3A (O)	Reserved	Reserved
11:10	GPIO5	EPWM3B (O)	SPICLKD (I/O)	ECAP1 (I/O)
13:12	GPIO6	EPWM4A (O)	EPWMSYNCI (I)	EPWMSYNCO (O)
15:14	GPIO7	EPWM4B (O)	SPISTED (I/O)	ECAP2 (I/O)
17:16	GPIO8	EPWM5A (O)	CANTXB (O)	$\overline{\text{ADCSOCAO}}$ (O)
19:18	GPIO9	EPWM5B (O)	SCITXB (O)	ECAP3 (I/O)
21:20	GPIO10	EPWM6A (O)	CANRXB (I)	$\overline{\text{ADCSOCBO}}$ (O)
23:22	GPIO11	EPWM6B (O)	SCIRXB (I)	ECAP4 (I/O)
25:24	GPIO12	$\overline{\text{TZ1}}$ (I)	CANTXB (O)	SPISIMOB (I/O)
27:26	GPIO13	$\overline{\text{TZ2}}$ (I)	CANRXB (I)	SPISOMIB (I/O)
29:28	GPIO14	$\overline{\text{TZ3}}$ (I)	SCITXB (O)	SPICLKB (I/O)
31:30	GPIO15	$\overline{\text{TZ4}}$ (I)	SCIRXB (I)	SPISTEB (I/O)
		GPAMUX2		
1:0	GPIO16	SPISIMOA (I/O)	CANTXB (O)	$\overline{\text{TZ5}}$ (I)
3:2	GPIO17	SPISOMIA (I/O)	CANRXB (I)	$\overline{\text{TZ6}}$ (I)
5:4	GPIO18	SPICLKA (I/O)	SCITXB (O)	Reserved
7:6	GPIO19	SPISTEA (I/O)	SCIRXB (I)	Reserved
9:8	GPIO20	EQEP1A (I)	SPISIMOC (I/O)	CANTXB (O)
11:10	GPIO21	EQEP1B (I)	SPISOMIC (I/O)	CANRXB (I)
13:12	GPIO22	EQEP1S (I/O)	SPICLKC (I/O)	SCITXB (O)
15:14	GPIO23	EQEP1I (I/O)	SPISTEC (I/O)	SCIRXB (I)

Table 4−5. 2808 GPIO MUX Table (continued)

Register Bits	Bits = 0,0 (Default)	Bits = 0,1	Bits = 1,0	Bits = 1,1
		GPAMUX2 (Continued)		
17:16	GPIO24	ECAP1 (I/O)	EQEP2A (I)	SPISIMOB (I/O)
19:18	GPIO25	ECAP2 (I/O)	EQEP2B (I)	SPISOMIB (I/O)
21:20	GPIO26	ECAP3 (I/O)	EQEP2I (I/O)	SPICLKB (I/O)
23:22	GPIO27	ECAP4 (I/O)	EQEP2S (I/O)	SPISTEB (I/O)
25:24	GPIO28	SCIRXDA (I)	Reserved	$\overline{\text{TZ5}}$ (I)
27:26	GPIO29	SCITXDA (O)	Reserved	$\overline{\text{TZ6}}$ (I)
29:28	GPIO30	CANRXA (I)	Reserved	Reserved
31:30	GPIO31	CANTXA (O)	Reserved	Reserved
		GPBMUX1		
1:0	GPIO32	SDAA (I/OC)	EPWMSYNCI (I)	$\overline{\text{ADCSOCAO}}$ (O)
3:2	GPIO33	SCLA (I/OC**)**	EPWMSYNCO (O)	$\overline{\text{ADCSOCBO}}$ (O)
5:4	GPIO34	Reserved	Reserved	Reserved

Table 4−6. 2806 GPIO MUX Table

Register Bits	Bits = 0,0 (Default)	Bits = 0,1	Bits = 1,0	Bits = 1,1
		GPAMUX1		
1:0	GPIO0	EPWM1A (O)	Reserved	Reserved
3:2	GPIO1	EPWM1B (O)	SPISIMOD (I/O)	Reserved
5:4	GPIO2	EPWM2A (O)	Reserved	Reserved
7:6	GPIO3	EPWM2B (O)	SPISOMID (I/O)	Reserved
9:8	GPIO4	EPWM3A (O)	Reserved	Reserved
11:10	GPIO5	EPWM3B (O)	SPICLKD (I/O)	ECAP1 (I/O)
13:12	GPIO6	EPWM4A (O)	EPWMSYNCI (I)	EPWMSYNCO (O)
15:14	GPIO7	EPWM4B (O)	SPISTED (I/O)	ECAP2 (I/O)
17:16	GPIO8	EPWM5A (O)	Reserved	$\overline{\text{ADCSOCAO}}$ (O)
19:18	GPIO9	EPWM5B (O)	SCITXB (O)	ECAP3 (I/O)
21:20	GPIO10	EPWM6A (O)	Reserved	$\overline{\text{ADCSOCBO}}$ (O)
23:22	GPIO11	EPWM6B (O)	SCIRXB (I)	ECAP4 (I/O)
25:24	GPIO12	$\overline{\text{TZ1}}$ (I)	Reserved	SPISIMOB (I/O)
27:26	GPIO13	$\overline{\text{TZ2}}$ (I)	Reserved	SPISOMIB (I/O)
29:28	GPIO14	$\overline{\text{TZ3}}$ (I)	SCITXB (O)	SPICLKB (I/O)
31:30	GPIO15	$\overline{\text{TZ4}}$ (I)	SCIRXB (I)	SPISTEB (I/O)
		GPAMUX2		
1:0	GPIO16	SPISIMOA (I/O)	Reserved	$\overline{\text{TZ5}}$ (I)
3:2	GPIO17	SPISOMIA (I/O)	Reserved	$\overline{\text{TZ6}}$ (I)
5:4	GPIO18	SPICLKA (I/O)	SCITXB (O)	Reserved
7:6	GPIO19	SPISTEA (I/O)	SCIRXB (I)	Reserved
9:8	GPIO20	EQEP1A (I)	SPISIMOC (I/O)	Reserved
11:10	GPIO21	EQEP1B (I)	SPISOMIC (I/O)	Reserved
13:12	GPIO22	EQEP1S (I/O)	SPICLKC (I/O)	SCITXB (O)
15:14	GPIO23	EQEP1I (I/O)	SPISTEC (I/O)	SCIRXB (I)

Table 4−6. 2806 GPIO MUX Table (continued)

Register Bits	Bits = 0,0 (Default)	Bits = 0,1	Bits = 1,0	Bits = 1,1
		GPAMUX2 (Continued)		
17:16	GPIO24	ECAP1 (I/O)	EQEP2A (I)	SPISIMOB (I/O)
19:18	GPIO25	ECAP2 (I/O)	EQEP2B (I)	SPISOMIB (I/O)
21:20	GPIO26	ECAP3 (I/O)	EQEP2I (I/O)	SPICLKB (I/O)
23:22	GPIO27	ECAP4 (I/O)	EQEP2S (I/O)	SPISTEB (I/O)
25:24	GPIO28	SCIRXDA (I)	Reserved	$\overline{\text{TZ5}}$ (I)
27:26	GPIO29	SCITXDA (O)	Reserved	$\overline{\text{TZ6}}$ (I)
29:28	GPIO30	CANRXA (I)	Reserved	Reserved
31:30	GPIO31	CANTXA (O)	Reserved	Reserved
		GPBMUX1		
1:0	GPIO32	SDAA (I/OC)	EPWMSYNCI (I)	$\overline{\text{ADCSOCAO}}$ (O)
3:2	GPIO33	SCLA (I/OC**)**	EPWMSYNCO (O)	$\overline{\text{ADCSOCBO}}$ (O)
5:4	GPIO34	Reserved	Reserved	Reserved

Table 4−7. 2801 GPIO MUX Table

Register Bits	Bits = 0,0 (Default)	Bits = 0,1	Bits = 1,0	Bits = 1,1
		GPAMUX1		
1:0	GPIO0	EPWM1A (O)	Reserved	Reserved
3:2	GPIO1	EPWM1B (O)	Reserved	Reserved
5:4	GPIO2	EPWM2A (O)	Reserved	Reserved
7:6	GPIO3	EPWM2B (O)	Reserved	Reserved
9:8	GPIO4	EPWM3A (O)	Reserved	Reserved
11:10	GPIO5	EPWM3B (O)	Reserved	ECAP1 (I/O)
13:12	GPIO6	Reserved	EPWMSYNCI (I)	EPWMSYNCO (O)
15:14	GPIO7	Reserved	Reserved	ECAP2 (I/O)
17:16	GPIO8	Reserved	Reserved	$\overline{\text{ADCSOCAO}}$ (O)
19:18	GPIO9	Reserved	Reserved	Reserved
21:20	GPIO10	Reserved	Reserved	$\overline{\text{ADCSOCBO}}$ (O)
23:22	GPIO11	Reserved	Reserved	Reserved
25:24	GPIO12	$\overline{\text{TZ1}}$ (I)	Reserved	SPISIMOB (I/O)
27:26	GPIO13	$\overline{\text{TZ2}}$ (I)	Reserved	SPISOMIB (I/O)
29:28	GPIO14	$\overline{\text{TZ3}}$ (I)	Reserved	SPICLKB (I/O)
31:30	GPIO15	$\overline{\text{TZ4}}$ (I)	Reserved	SPISTEB (I/O)
		GPAMUX2		
1:0	GPIO16	SPISIMOA (I/O)	Reserved	$\overline{\text{TZ5}}$ (I)
3:2	GPIO17	SPISOMIA (I/O)	Reserved	$\overline{\text{TZ6}}$ (I)
5:4	GPIO18	SPICLKA (I/O)	Reserved	Reserved
7:6	GPIO19	SPISTEA (I/O)	Reserved	Reserved
9:8	GPIO20	EQEP1A (I)	Reserved	Reserved
11:10	GPIO21	EQEP1B (I)	Reserved	Reserved
13:12	GPIO22	EQEP1S (I/O)	Reserved	Reserved

Table 4−7. 2801 GPIO MUX Table (continued)

Register Bits	Bits = 0,0 (Default)	Bits = 0,1	Bits = 1,0	Bits = 1,1
		GPAMUX2 (Continued)		
15:14	GPIO23	EQEP1I (I/O)	Reserved	Reserved
17:16	GPIO24	ECAP1 (I/O)	Reserved	SPISIMOB (I/O)
19:18	GPIO25	ECAP2 (I/O)	Reserved	SPISOMIB (I/O)
21:20	GPIO26	Reserved	Reserved	SPICLKB (I/O)
23:22	GPIO27	Reserved	Reserved	SPISTEB (I/O)
25:24	GPIO28	SCIRXDA (I)	Reserved	$\overline{\text{TZ5}}$ (I)
27:26	GPIO29	SCITXDA (O)	Reserved	$\overline{\text{TZ6}}$ (I)
29:28	GPIO30	CANRXA (I)	Reserved	Reserved
31:30	GPIO31	CANTXA (O)	Reserved	Reserved
		GPBMUX1		
1:0	GPIO32	SDAA (I/OC)	EPWMSYNCI (I)	$\overline{\text{ADCSOCAO}}$ (O)
3:2	GPIO33	SCLA (I/OC)	EPWMSYNCO (O)	$\overline{\text{ADCSOCBO}}$ (O)
5:4	GPIO34	Reserved	Reserved	Reserved

Table 4−8 is a MUX table sorted by peripheral function. This can be used to identify the GPIO pins that can be assigned to a particular peripheral function.

Table 4−8. Peripheral to GPIO Cross Reference

Primary I/O Function (GPxMUX1/2 bits = 0,0)	Peripheral Selection 1 (GPxMUX1/2 bits = 0,1)	Peripheral Selection 2 (GPxMUX1/2 bits = 1,0)	Peripheral Selection 2 (GPxMUX1/2 bits = 1,1)
ADC External Start of Conversion A			
GPIO8	EPWM5A	CANTXB	$\overline{\text{ADCSOCAO}}$
GPIO32	SDAA	EPWMSYNCI	$\overline{\text{ADCSOCAO}}$
ADC External Start of Conversion B			
GPIO10	EPWM6A	CANRXB	$\overline{\text{ADCSOCBO}}$
GPIO10	EPWM6A	CANRXB	$\overline{\text{ADCSOCBO}}$
GPIO33	SCLA	EPWMSYNCO	$\overline{\text{ADCSOCBO}}$
eCAN-A			
GPIO30	CANRXA	Reserved	Reserved
GPIO31	CANTXA	Reserved	Reserved
eCAN-B			
GPIO8	EPWM5A	CANTXB	$\overline{\text{ADCSOCAO}}$
GPIO10	EPWM6A	CANRXB	$\overline{\text{ADCSOCBO}}$
GPIO12	$\overline{\text{TZ1}}$	CANTXB	SPISIMOB
GPIO13	$\overline{\text{TZ2}}$	CANRXB	SPISOMIB
GPIO16	SPISIMOA	CANTXB	$\overline{\text{TZ5}}$
GPIO17	SPISOMIA	CANRXB	$\overline{\text{TZ6}}$
GPIO20	EQEP1A	SPISIMOC	CANTXB
GPIO21	EQEP1B	SPISOMIC	CANRXB
eCAP1			
GPIO5	EPWM3B	SPICLKD	ECAP1
GPIO24	ECAP1	EQEP2A	SPISIMOB

Table 4−8. Peripheral to GPIO Cross Reference (Continued)

Primary I/O Function (GPxMUX1/2 bits = 0,0)	Peripheral Selection 1 (GPxMUX1/2 bits = 0,1)	Peripheral Selection 2 (GPxMUX1/2 bits = 1,0)	Peripheral Selection 2 (GPxMUX1/2 bits = 1,1)
eCAP2			
GPIO7	EPWM4B	SPISTED	ECAP2
GPIO25	ECAP2	EQEP2B	SPISOMIB
eCAP3			
GPIO9	EPWM5B	SCITXB	ECAP3
GPIO26	ECAP3	EQEP2I	SPICLKB
eCAP4			
GPIO11	EPWM6B	SCIRXB	ECAP4
GPIO27	ECAP4	EQEP2S	SPISTEB
ePWM1−6			
GPIO0	EPWM1A	Reserved	Reserved
GPIO1	EPWM1B	SPISIMOD	Reserved
GPIO2	EPWM2A	Reserved	Reserved
GPIO3	EPWM2B	SPISOMID	Reserved
GPIO4	EPWM3A	Reserved	Reserved
GPIO5	EPWM3B	SPICLKD	ECAP1
GPIO6	EPWM4A	EPWMSYNCI	EPWMSYNCO
GPIO7	EPWM4B	SPISTED	ECAP2
GPIO8	EPWM5A	CANTXB	$\overline{\text{ADCSOCAO}}$
GPIO9	EPWM5B	SCITXB	ECAP3
GPIO10	EPWM6A	CANRXB	$\overline{\text{ADCSOCBO}}$
GPIO11	EPWM6B	SCIRXB	ECAP4
ePWM Synchronization Input			
GPIO6	EPWM4A	EPWMSYNCI	EPWMSYNCO
GPIO32	SDAA	EPWMSYNCI	$\overline{\text{ADCSOCAO}}$

Table 4−8. Peripheral to GPIO Cross Reference (Continued)

Primary I/O Function (GPxMUX1/2 bits = 0,0)	Peripheral Selection 1 (GPxMUX1/2 bits = 0,1)	Peripheral Selection 2 (GPxMUX1/2 bits = 1,0)	Peripheral Selection 2 (GPxMUX1/2 bits = 1,1)
ePWM Synchronization Output			
GPIO6	EPWM4A	EPWMSYNCI	EPWMSYNCO
GPIO33	SCLA	EPWMSYNCO	$\overline{\text{ADCSOCBO}}$
eQEP1			
GPIO20	EQEP1A	SPISIMOC	CANTXB
GPIO21	EQEP1B	SPISOMIC	CANRXB
GPIO22	EQEP1S	SPICLKC	SCITXB
GPIO23	EQEP1I	SPISTEC	SCIRXB
eQEP2			
GPIO24	ECAP1	EQEP2A	SPISIMOB
GPIO25	ECAP2	EQEP2B	SPISOMIB
GPIO26	ECAP3	EQEP2I	SPICLKB
GPIO27	ECAP4	EQEP2S	SPISTEB
I^2C-A			
GPIO32	SDAA	EPWMSYNCI	$\overline{\text{ADCSOCAO}}$
GPIO33	SCLA	EPWMSYNCO	$\overline{\text{ADCSOCBO}}$
SCI-A			
GPIO28	SCIRXDA	Reserved	$\overline{\text{TZ5}}$
GPIO29	SCITXDA	Reserved	$\overline{\text{TZ6}}$
SCI-B			
GPIO9	EPWM5B	SCITXB	ECAP3
GPIO11	EPWM6B	SCIRXB	ECAP4
GPIO14	$\overline{\text{TZ3}}$	SCITXB	SPICLKB
GPIO15	$\overline{\text{TZ4}}$	SCIRXB	SPISTEB
GPIO18	SPICLKA	SCITXB	Reserved

Table 4−8. Peripheral to GPIO Cross Reference (Continued)

Primary I/O Function (GPxMUX1/2 bits = 0,0)	Peripheral Selection 1 (GPxMUX1/2 bits = 0,1)	Peripheral Selection 2 (GPxMUX1/2 bits = 1,0)	Peripheral Selection 2 (GPxMUX1/2 bits = 1,1)
SCI-B (Continued)			
GPIO19	SPISTEA	SCIRXB	Reserved
GPIO22	EQEP1S	SPICLKC	SCITXB
GPIO23	EQEP1I	SPISTEC	SCIRXB
SPI-A			
GPIO16	SPISIMOA	CANTXB	$\overline{\text{TZ5}}$
GPIO17	SPISOMIA	CANRXB	$\overline{\text{TZ6}}$
GPIO18	SPICLKA	SCITXB	Reserved
GPIO19	SPISTEA	SCIRXB	Reserved
SPI-B			
GPIO12	$\overline{\text{TZ1}}$	CANTXB	SPISIMOB
GPIO13	$\overline{\text{TZ2}}$	CANRXB	SPISOMIB
GPIO14	$\overline{\text{TZ3}}$	SCITXB	SPICLKB
GPIO15	$\overline{\text{TZ4}}$	SCIRXB	SPISTEB
GPIO24	ECAP1	EQEP2A	SPISIMOB
GPIO25	ECAP2	EQEP2B	SPISOMIB
GPIO26	ECAP3	EQEP2I	SPICLKB
GPIO27	ECAP4	EQEP2S	SPISTEB
SPI-C			
GPIO20	EQEP1A	SPISIMOC	CANTXB
GPIO21	EQEP1B	SPISOMIC	CANRXB
GPIO22	EQEP1S	SPICLKC	SCITXB
GPIO23	EQEP1I	SPISTEC	SCIRXB

Table 4−8. Peripheral to GPIO Cross Reference (Continued)

Primary I/O Function (GPxMUX1/2 bits = 0,0)	Peripheral Selection 1 (GPxMUX1/2 bits = 0,1)	Peripheral Selection 2 (GPxMUX1/2 bits = 1,0)	Peripheral Selection 2 (GPxMUX1/2 bits = 1,1)
SPI−D			
GPIO1	EPWM1B	SPISIMOD	Reserved
GPIO3	EPWM2B	SPISOMID	Reserved
GPIO5	EPWM3B	SPICLKD	ECAP1
GPIO7	EPWM4B	SPISTED	ECAP2
Trip Zones 1−6			
GPIO12	$\overline{\text{TZ1}}$	CANTXB	SPISIMOB
GPIO13	$\overline{\text{TZ2}}$	CANRXB	SPISOMIB
GPIO14	$\overline{\text{TZ3}}$	SCITXB	SPICLKB
GPIO15	$\overline{\text{TZ4}}$	SCIRXB	SPISTEB
GPIO16	SPISIMOA	CANTXB	$\overline{\text{TZ5}}$
GPIO17	SPISOMIA	CANRXB	$\overline{\text{TZ6}}$
GPIO28	SCIRXDA	Reserved	$\overline{\text{TZ5}}$
GPIO29	SCITXDA	Reserved	$\overline{\text{TZ6}}$

4.5 Register Bit Definitions

Table 4−9. GPIO Port A MUX 1 (GPAMUX1) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31−30	GPIO15	R/W	0,0	Configure the GPIO15 pin as: 00 GPIO15 (I/O), General purpose I/O 15 01 $\overline{\text{TZ4}}$ (I), Trip zone 4 10 SCIRXB (I), SCI-B receive. This option is reserved on 2801 devices. 11 SPISTEB (I/O), SPI-B transmit enable
29−28	GPIO14	R/W	0,0	Configure the GPIO14 pin as: 00 GPIO14 (I/O), General purpose I/O 14 01 $\overline{\text{TZ3}}$ (I), Trip zone 3 10 SCITXB (O), SCI-B transmit. This option is reserved on 2801 devices. 11 SPICLKB (I/O), SPI-B clock in
27−26	GPIO13	R/W	0,0	Configure the GPIO13 pin as: 00 GPIO13 (I/O), General purpose I/O 13 01 $\overline{\text{TZ2}}$ (I), Trip zone 2 10 CANRXB (I), eCAN-B receive. This option is reserved on 2806 and 2801 devices. 11 SPISOMIB (I/O)
25−24	GPIO12	R/W	0,0	Configure the GPIO12 pin as: 00 GPIO12 (I/O), General purpose I/O 12 01 $\overline{\text{TZ1}}$ (I), Trip zone 1 10 CANTXB (O), eCAN-B transmit. This option is reserved on 2806 and 2801 devices. 11 SPISIMOB (I/O), SPI-B slave-in, master-out
23−22	GPIO11	R/W	0,0	Configure the GPIO11 pin as: 00 GPIO11 (I/O), General purpose I/O 11 01 EPWM6B (O), ePWM 6 output B. This option is reserved on 2801 devices. 10 SCIRXB (I), SCI-B receive. This option is reserved on 2801 devices. 11 ECAP4 (I/O), eCAP4. This option is reserved on 2801 devices.

Table 4−9. GPIO Port A MUX 1 (GPAMUX1) Register Bit Descriptions (Continued)

Bit(s)	Field	Type	Reset	Description
21−20	GPIO10	R/W	0,0	Configure the GPIO10 pin as: 00 GPIO10 (I/O), General purpose I/O 10 01 EPWM6A (O), ePWM6 output A. This option is reserved on 2801 devices. 10 CANRXB (I), eCAN-B receive. This option is reserved on 2806 and 2801 devices. 11 $\overline{\text{ADCSOCBO}}$ (O), ADC Start of conversion B
19−18	GPIO9	R/W	0,0	Configure the GPIO9 pin as: 00 GPIO9 (I/O) , General purpose I/O 9 01 EPWM5B (O), ePWM5 output B. This option is reserved on 2801 devices. 10 SCITXB (O), SCI-B transmit. This option is reserved on 2801 devices. 11 ECAP3 (I/O), eCAP3
17−16	GPIO8	R/W	0,0	Configure the GPIO8 pin as: 00 GPIO8 (I/O), General purpose I/O 8 01 EPWM5A (O), ePWM5 output A. This option is reserved on 2801 devices. 10 CANTXB (O), eCAN-B transmit. This option is reserved on 2806 and 2801 devices. 11 $\overline{\text{ADCSOCAO}}$ (O), ADC Start of conversion A
15−14	GPIO7	R/W	0,0	Configure the GPIO7 pin as: 00 GPIO7 (I/O), General purpose I/O 7 01 EPWM4B (O), ePWM4 output B. This option is reserved on 2801 devices. 10 SPISTED (I/O), SPI-D transmit enable. This option is reserved on 2801 devices. 11 ECAP2 (I/O), eCAP2
13−12	GPIO6	R/W	0,0	Configure the GPIO6 pin as: 00 GPIO6 (I/O), General purpose I/O 6 01 EPWM4A (O), ePWM4 output A. This option is reserved on 2801 devices. 10 EPWMSYNCI (I), ePWM Synch-in 11 EPWMSYNCO (O), ePWM Synch-out

Table 4−9. GPIO Port A MUX 1 (GPAMUX1) Register Bit Descriptions (Continued)

Bit(s)	Field	Type	Reset	Description
11−10	GPIO5	R/W	0,0	Configure the GPIO5 pin as: 00 GPIO5 (I/O), General purpose I/O 5 01 EPWM3B (O), ePWM3 output B 10 SPICLKD (I/O), SPI-D clock. This option is reserved on 2801 devices. 11 ECAP1 (I/O), eCAP1
9−8	GPIO4	R/W	0,0	Configure the GPIO4 pin as: 00 GPIO4 (I/O), General purpose I/O 4 01 EPWM3A (O), ePWM3 output A 10 Reserved 11 Reserved
7−6	GPIO3	R/W	0,0	Configure the GPIO3 pin as: 00 GPIO3 (I/O), General purpose I/O 3 01 EPWM2B (O), ePWM2 output B 10 SPISOMID (I/O), SPI-D slave-out, master-in. This option is reserved on 2801 devices. 11 Reserved
5−4	GPIO2	R/W	0,0	Configure the GPIO2 pin as: 00 GPIO2 (I/O) General purpose I/O 2 01 EPWM2A (O), ePWM2 output A 10 Reserved 11 Reserved
3−2	GPIO1	R/W	0,0	Configure the GPIO1 pin as: 00 GPIO1 (I/O) General purpose I/O 1 01 EPWM1B (O), ePWM1 output B 10 SPISIMOD (I/O) SPI-D slave-in, master-out. This option is reserved on 2801 devices. 11 Reserved
1−0	GPIO0	R/W	0,0	Configure the GPIO0 pin as: 00 GPIO0 (I/O), General purpose I/O 0 01 EPWM1A (O), ePWM1 output A 10 Reserved 11 Reserved

Table 4−10. GPIO Port A MUX 2 (GPAMUX2) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31−30	GPIO31	R/W	0,0	Configure the GPIO31 pin as:
				00 GPIO31 (I/O) General purpose I/O 31
				01 CANTXA (O), eCAN-A transmit
				10 Reserved
				11 Reserved
29−28	GPIO30	R/W	0,0	Configure the GPIO30 pin as:
				00 GPIO30 (I/O) General purpose I/O 30
				01 CANRXA (I), eCAN-A receive
				10 Reserved
				11 Reserved
27−26	GPIO29	R/W	0,0	Configure the GPIO29 pin as:
				00 GPIO29 (I/O) General purpose I/O 29
				01 SCITXDA (O), SCI-D transmit. This option is reserved on 2806 and 2801 devices.
				10 Reserved
				11 $\overline{\text{TZ6}}$ (I), trip zone 6
25−24	GPIO28	R/W	0,0	Configure the GPIO28 pin as:
				00 GPIO28 (I/O) General purpose I/O 28
				01 SCIRXDA (I), SCI-A receive
				10 Reserved
				11 $\overline{\text{TZ5}}$ (I), trip zone 5
23−22	GPIO27	R/W	0,0	Configure the GPIO27 pin as:
				00 GPIO27 (I/O), General purpose I/O 27
				01 ECAP4 (I/O), eCAP4. This option is reserved on 2801 devices.
				10 EQEP2S (I/O), eQEP2 strobe. This option is reserved on 2801 devices.
				11 SPISTEB (I/O), SPI-B transmit enable

Table 4−10. GPIO Port A MUX 2 (GPAMUX2) Register Bit Descriptions (Continued)

Bit(s)	Field	Type	Reset	Description
21−20	GPIO26	R/W	0,0	Configure the GPIO26 pin as: 00 GPIO26 (I/O), General purpose I/O 26 01 ECAP3 (I/O), eCAP3. This option is reserved on 2801 devices. 10 EQEP2I (I/O), eQEP2 index. This option is reserved on 2801 devices. 11 SPICLKB (I/O), SPI-B clock
19−18	GPIO25	R/W	0,0	Configure the GPIO25 pin as: 00 GPIO25 (I/O), General purpose I/O 25 01 ECAP2 (I/O), eCAP2 10 EQEP2B (I), eQEP2 input B. This option is reserved on 2801 devices. 11 SPISOMIB (I/O), SPI-B slave-out, master-in
17−16	GPIO24	R/W	0,0	Configure the GPIO24 pin as: 00 GPIO24 (I/O), General purpose I/O 24 01 ECAP1 (I/O), eCAP1 10 EQEP2A (I), eQEP2 input A. This option is reserved on 2801 devices. 11 SPISIMOB (I/O), SPI-B slave-in, master-out
15−14	GPIO23	R/W	0,0	Configure the GPIO23 pin as: 00 GPIO23 (I/O), General purpose I/O 23 01 EQEP1I (I/O), eQEP1 index 10 SPISTEC (I/O), SPI-C transmit enable. This option is reserved on 2801 devices. 11 SCIRXB (I/O), SCI-B receive. This option is reserved on 2801 devices.
13−12	GPIO22	R/W	0,0	Configure the GPIO22 pin as: 00 GPIO22 (I/O), General purpose I/O 22 01 EQEP1S (I/O), eQEP1 strobe 10 SPICLKC (I/O), SPI-C clock. This option is reserved on 2801 devices. 11 SCITXB (O), SCI-B transmit. This option is reserved on 2801 devices.

Table 4−10. GPIO Port A MUX 2 (GPAMUX2) Register Bit Descriptions (Continued)

Bit(s)	Field	Type	Reset	Description
11−10	GPIO21	R/W	0,0	Configure the GPIO21 pin as: 00 GPIO21 (I/O), General purpose I/O 21 01 EQEP1B (I), eQEP1 input B 10 SPISOMIC (I/O), SPI-C slave-out, master-in. This option is reserved on 2801 devices. 11 CANRXB (I), eCAN-B receive. This option is reserved on 2806 and 2801 devices.
9−8	GPIO20	R/W	0,0	Configure the GPIO20 pin as: 00 GPIO20 (I/O) General purpose I/O 22 01 EQEP1A (I), eQEP1 input A 10 SPISIMOC (I/O), SPI-C slave-in, master-out. This option is reserved on 2801 devices. 11 CANTXB (O), eCAN-B transmit. This option is reserved on 2806 and 2801 devices.
7−6	GPIO19	R/W	0,0	Configure the GPIO19 pin as: 00 GPIO19 (I/O), General purpose I/O 19 01 SPISTEA (I/O), SPI-A transmit enable 10 SCIRXB (I), SCI-B receive. This option is reserved on 2801 devices. 11 Reserved
5−4	GPIO18	R/W	0,0	Configure the GPIO18 pin as: 00 GPIO18 (I/O), General purpose I/O 18 01 SPICLKA (I/O), SPI-A clock 10 SCITXB (O), SCI-B transmit. This option is reserved on 2801 devices. 11 Reserved
3−2	GPIO17	R/W	0,0	Configure the GPIO17 pin as: 00 GPIO17 (I/O), General purpose I/O 17 01 SPISOMIA (I/O), SPI-A slave-out, master-in 10 CANRXB (I), eCAN-B receive. This option is reserved on 2806 and 2801 devices. 11 $\overline{\text{TZ6}}$ (I), Trip zone 6

Table 4−10. GPIO Port A MUX 2 (GPAMUX2) Register Bit Descriptions (Continued)

Bit(s)	Field	Type	Reset	Description
1−0	GPIO16	R/W	0,0	Configure the GPIO16 pin as:
				00 GPIO16 (I/O), General purpose I/O 16
				01 SPISIMOA (I/O), SPI-A slave-in, master-out
				10 CANTXB (O), eCAN-B transmit. This option is reserved on 2806 and 2801 devices.
				11 $\overline{\text{TZ5}}$ (I), Trip zone 5

Table 4−11. GPIO Port B MUX 1 (GPBMUX1) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31,8	Reserved	R/W	0,0	Reserved
7−6	GPIO35	R/W	0,0	Configure the GPIO35 pin as:
				00 GPIO35 (I/O), General purpose I/O 35
				01 Reserved
				10 Reserved
				11 Reserved
5−4	GPIO34	R/W	0,0	Configure the GPIO34 pin as:
				00 GPIO34 (I/O), General purpose I/O 34
				01 Reserved
				10 Reserved
				11 Reserved
3−2	GPIO33	R/W	0,0	Configure the GPIO33 pin as:
				00 GPIO33 (I/O), General purpose I/O 33
				01 SCLA (I/O), I2C clock
				10 EPWMSYNCO (O), ePWM synch out
				11 $\overline{\text{ADCSOCBO}}$ (O)
1−0	GPIO32	R/W	0,0	Configure the GPIO32 pin as:
				00 GPIO32 (I/O), General purpose I/O 32
				01 SDAA(I/O), I2C data
				10 EWPMSYNCI (I), ePWM synch in
				11 $\overline{\text{ADCSOCAO}}$ (O), ADC start of conversion A

Table 4−12. GPIO Port B MUX 2 (GPBMUX2) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31−0	Reserved	R/W	0,0	Reserved

Table 4−13. GPIO Port A Qualification Control (GPACTRL) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31−24	QUALPRD3	R/W	0:0	Specifies the qualification sampling period for GPIO24 to GPIO31: 0x00 QUALPRD = SYSCLKOUT 0x01 QUALPRD = SYSCLKOUT/2 0x02 QUALPRD = SYSCLKOUT/4 … 0xFF QUALPRD = SYSCLKOUT/510
23−16	QUALPRD2	R/W	0:0	Specifies the qualification sampling period for GPIO16 to GPIO23: 0x00 QUALPRD = SYSCLKOUT 0x01 QUALPRD = SYSCLKOUT/2 0x02 QUALPRD = SYSCLKOUT/4 … 0xFF QUALPRD = SYSCLKOUT/510
15−8	QUALPRD1	R/W	0:0	Specifies the qualification sampling period for GPIO8 to GPIO15: 0x00 QUALPRD = SYSCLKOUT 0x01 QUALPRD = SYSCLKOUT/2 0x02 QUALPRD = SYSCLKOUT/4 … 0xFF QUALPRD = SYSCLKOUT/510
7−0	QUALPRD0	R/W	0:0	Specifies the qualification sampling period for GPIO0 to GPIO7: 0x00 QUALPRD = SYSCLKOUT 0x01 QUALPRD = SYSCLKOUT/2 0x02 QUALPRD = SYSCLKOUT/4 … 0xFF QUALPRD = SYSCLKOUT/510

Note: The register in this table is EALLOW protected.

Table 4−14. GPIO Port B Input Qualification Control (GPBCTRL) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31−8	Reserved	R/W	0:0	Reserved
7−0	QUALPRD0	R/W	0:0	Specifies the qualification sampling period for GPIO32 to GPIO35: 0x00 QUALPRD = SYSCLKOUT 0x01 QUALPRD = SYSCLKOUT/2 0x02 QUALPRD = SYSCLKOUT/4 … 0xFF QUALPRD = SYSCLKOUT/510

Note: This register is EALLOW protected.

Table 4−15. GPIO Port A Qualification Select 1 (GPAQSEL1) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31−30	GPIO15	R/W	0,0	Select input qualification type for GPIO0 to GPIO15. 00 Sync to SYSCLKOUT only. Valid for both peripheral and GPIO pins. 01 Qualification using 3 samples. Valid for both peripheral and GPIO pins. The time between samples is specified in the GPACTRL register. 10 Qualification using 6 samples. Valid for both peripheral and GPIO pins. The time between samples is specified in the GPACTRL register. 11 Async (no Sync or Qualification). This option applies to pins configured as peripherals only. If the pin is configured as a GPIO input, then this option is the same as 0,0 or sync to SYSCLKOUT.
29−28	GPIO14	R/W	0,0	
27−26	GPIO13	R/W	0,0	
25−24	GPIO12	R/W	0,0	
23−22	GPIO11	R/W	0,0	
21−20	GPIO10	R/W	0,0	
19−18	GPIO9	R/W	0,0	
17−16	GPIO8	R/W	0,0	
15−14	GPIO7	R/W	0,0	
13−12	GPIO6	R/W	0,0	
11−10	GPIO5	R/W	0,0	
9−8	GPIO4	R/W	0,0	
7−6	GPIO3	R/W	0,0	
5−4	GPIO2	R/W	0,0	
3−2	GPIO1	R/W	0,0	
1−0	GPIO0	R/W	0,0	

Note: This register is EALLOW protected.

Table 4−16. GPIO Port A Qualification Select 2 (GPAQSEL2) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31−30	GPIO31	R/W	0,0	Select input qualification type for GPIO16 to GPIO31. 00 Sync to SYSCLKOUT only. Valid for both peripheral and GPIO pins. 01 Qualification using 3 samples. Valid for both peripheral and GPIO pins. The time between samples is specified in the GPACTRL register. 10 Qualification using 6 samples. Valid for both peripheral and GPIO pins. The time between samples is specified in the GPACTRL register. 11 Async (no Sync or Qualification). This option applies to pins configured as peripherals only. If the pin is configured as a GPIO input, then this option is the same as 0,0 or sync to SYSCLKOUT.
29−28	GPIO30	R/W	0,0	
27−26	GPIO29	R/W	0,0	
25−24	GPIO28	R/W	0,0	
23−22	GPIO27	R/W	0,0	
21−20	GPIO26	R/W	0,0	
19−18	GPIO25	R/W	0,0	
17−16	GPIO24	R/W	0,0	
15−14	GPIO23	R/W	0,0	
13−12	GPIO22	R/W	0,0	
11−10	GPIO21	R/W	0,0	
9−8	GPIO20	R/W	0,0	
7−6	GPIO19	R/W	0,0	
5−4	GPIO18	R/W	0,0	
3−2	GPIO17	R/W	0,0	
1−0	GPIO16	R/W	0,0	

Note: This register is EALLOW protected.

Table 4−17. GPIO Port B Qualification Select 1 (GPBSEL1) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31−8	Reserved	R/W	0,0	
7−6	GPIO35	R/W	0,0	Select input qualification type for GPIO32 to GPIO34. 00 Sync to SYSCLKOUT only. Valid for both peripheral and GPIO pins 01 Qualification using 3 samples. Valid for both peripheral and GPIO pins. The time between samples is specified in the GPBCTRL register. 10 Qualification using 6 samples. Valid for both peripheral and GPIO pins. The time between samples is specified in the GPBCTRL register. 11 Async (no Sync or Qualification). This option applies to pins configured as peripherals only. If the pin is configured as a GPIO input, then this option is the same as 0,0 or sync to SYSCLKOUT.
5−4	GPIO34	R/W	0,0	
3−2	GPIO33	R/W	0,0	
1−0	GPIO32	R/W	0,0	

Note: The above registers are EALLOW protected.

Table 4−18. GPIO Port B Qualification Select 2 (GPBSEL2) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31−0	GPIO32	R/W	0,0	Select input qualification type for GPIO32 to GPIO35. 00 Sync to SYSCLKOUT only. Valid for both peripheral and GPIO pins 01 Qualification using 3 samples. Valid for both peripheral and GPIO pins. 10 Qualification using 6 samples. Valid for both peripheral and GPIO pins. 11 Async (no Sync or Qualification). This option applies to pins configured as peripherals only. If the pin is configured as a GPIO input, then this option is the same as 0,0 or sync to SYSCLKOUT.

Note: This register is EALLOW protected.

The GPIOADIR and GPIOBDIR registers control the direction of the pins when they are configured as a GPIO in the appropriate MUX register. The direction register has no effect on pins configured as peripheral functions.

Table 4−19. GPIO Port A Direction (GPADIR) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31	GPIO31	R/W	0	Controls direction of GPIO Port A pins when the specified pin is configured as a GPIO in the GPAMUX1 or GPAMUX2 register. 0 Configures the GPIO pin as an input. 1 Configures the GPIO pin as an output The value currently in the GPxDAT output latch is driven on the pin. To initialize the GPxDAT latch prior to changing the pin from an input to an output, use the SET, CLEAR, and TOGGLE registers.
30	GPIO30	R/W	0	
29	GPIO29	R/W	0	
28	GPIO28	R/W	0	
27	GPIO27	R/W	0	
26	GPIO26	R/W	0	
25	GPIO25	R/W	0	
24	GPIO24	R/W	0	
23	GPIO23	R/W	0	
22	GPIO22	R/W	0	
21	GPIO21	R/W	0	
20	GPIO20	R/W	0	
19	GPIO19	R/W	0	
18	GPIO18	R/W	0	
17	GPIO17	R/W	0	
16	GPIO16	R/W	0	
15	GPIO15	R/W	0	
14	GPIO14	R/W	0	
13	GPIO13	R/W	0	

Table 4−19. GPIO Port A Direction (GPADIR) Register Bit Descriptions (Continued)

Bit(s)	Field	Type	Reset	Description
12	GPIO12	R/W	0	
11	GPIO11	R/W	0	
10	GPIO10	R/W	0	
9	GPIO9	R/W	0	
8	GPIO8	R/W	0	
7	GPIO7	R/W	0	
6	GPIO6	R/W	0	
5	GPIO5	R/W	0	
4	GPIO4	R/W	0	
3	GPIO3	R/W	0	
2	GPIO2	R/W	0	
1	GPIO1	R/W	0	
0	GPIO0	R/W	0	

Note: Register is EALLOW protected.

Table 4−20. GPIO Port B Direction (GPBDIR) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31−4	Reserved	R/W	0	
3	GPIO35	R/W	0	Controls direction of GPIO Port B pins when the specified pin is configured in GPIO in the GPBMUX1 or GPBMUX2 register. 0 Configures the GPIO pin as an input. 1 Configures the GPIO pin as an output The value currently in the GPxDAT output latch is driven on the pin. To initialize the GPxDAT latch prior to changing the pin from an input to an output, use the SET, CLEAR, and TOGGLE registers.
2	GPIO34	R/W	0	
1	GPIO33	R/W	0	
0	GPIO32	R/W	0	

Note: Register is EALLOW protected.

The pullup disable (PUD) registers allow you to specify which pins should have an internal pullup resister enabled. The pullups on the pins are all disabled asynchronously when the reset signal is low. When coming out of reset, the pullups remain disabled until you enable them selectively in software by writing to this register. The pullup configuration applies both to pins configured as I/O and those configured as peripheral functions.

Table 4−21. GPIO Port A Internal Pullup Disable (GPAPUD) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31	GPIO31	R/W	1	Configure the internal pullup resister on the selected pin. 0 Enable the internal pullup on the specified pin. 1 Disable the internal pullup on the specified pin.
30	GPIO30	R/W	1	
29	GPIO29	R/W	1	
28	GPIO28	R/W	1	
27	GPIO27	R/W	1	
26	GPIO26	R/W	1	
25	GPIO25	R/W	1	
24	GPIO24	R/W	1	
23	GPIO23	R/W	1	
22	GPIO22	R/W	1	
21	GPIO21	R/W	1	
20	GPIO20	R/W	1	
19	GPIO19	R/W	1	
18	GPIO18	R/W	1	
17	GPIO17	R/W	1	
16	GPIO16	R/W	1	
15	GPIO15	R/W	1	
14	GPIO14	R/W	1	
13	GPIO13	R/W	1	

Table 4−21. GPIO Port A Internal Pullup Disable (GPAPUD) Register Bit Descriptions (Continued)

Bit(s)	Field	Type	Reset	Description
12	GPIO12	R/W	1	
11	GPIO11	R/W	1	
10	GPIO10	R/W	1	
9	GPIO9	R/W	1	
8	GPIO8	R/W	1	
7	GPIO7	R/W	1	
6	GPIO6	R/W	1	
5	GPIO5	R/W	1	
4	GPIO4	R/W	1	
3	GPIO3	R/W	1	
2	GPIO2	R/W	1	
1	GPIO1	R/W	1	
0	GPIO0	R/W	1	

Note: Register is EALLOW protected.

Table 4−22. GPIO Port B Internal Pullup Disable (GPBPUD) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31:4	Reserved	R/W	1	
3	GPIO35	R/W	1	Configure the internal pullup resister on the selected pin. 0 Enable the internal pullup on the specified pin. 1 Disable the internal pullup on the specified pin.
2	GPIO34	R/W	1	
1	GPIO33	R/W	1	
0	GPIO32	R/W	1	

Note: Register is EALLOW protected.

The GPIO data registers indicate the current status of the GPIO pin, irrespective of which mode the pin is in. Writing to this register will set the respective GPIO pin high or low if the pin is enabled as a GPIO input, otherwise the value written is latched but ignored. The state of the output register latch will remain in its current state until the next write operation. A reset will clear all bits and latched values to zero. Reading the GPIODAT register reflects the state of the pin (after qualification), not the state of the output latch of the GPIODAT register.

Typically the DAT registers are used for reading the current state of the pins. To easily modify the output level of the pin refer to the SET/CLEAR and TOGGLE registers.

Table 4−23. GPIO Port A Data (GPADAT) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description	
31	GPIO31	R/W	x		
				0	Reading a 0 indicates that the state of the pin is currently low, irrespective of which mode the pin is in. Writing a 0 will force an output of 0 if the pin is configured as a GPIO in the appropriate MUX and DIR registers; otherwise, the value is latched but not used to drive the pin.
				1	Reading a 1 indicates that the state of the pin is currently high irrespective of which mode the pin is in. Writing a 1 will force an output of 1 if the pin is configured as a GPIO output in the appropriate MUX and DIR registers; otherwise, the value is latched but not used to drive the pin.
30	GPIO30	R/W	x		
29	GPIO29	R/W	x		
28	GPIO28	R/W	x		
27	GPIO27	R/W	x		
26	GPIO26	R/W	x		
25	GPIO25	R/W	x		
24	GPIO24	R/W	x		
23	GPIO23	R/W	x		
22	GPIO22	R/W	x		
21	GPIO21	R/W	x		

Table 4−23. GPIO Port A Data (GPADAT) Register Bit Descriptions (Continued)

Bit(s)	Field	Type	Reset	Description
20	GPIO20	R/W	x	
19	GPIO19	R/W	x	
18	GPIO18	R/W	x	
17	GPIO17	R/W	x	
16	GPIO16	R/W	x	
15	GPIO15	R/W	x	
14	GPIO14	R/W	x	
13	GPIO13	R/W	x	
12	GPIO12	R/W	x	
11	GPIO11	R/W	x	
10	GPIO10	R/W	x	
9	GPIO9	R/W	x	
8	GPIO8	R/W	x	
7	GPIO7	R/W	x	
6	GPIO6	R/W	x	
5	GPIO5	R/W	x	
4	GPIO4	R/W	x	
3	GPIO3	R/W	x	
2	GPIO2	R/W	x	
1	GPIO1	R/W	x	
0	GPIO0	R/W	x	

Note: x = The state of the GPADAT register is unknown after reset. It depends on the state of the input pin after reset.

Table 4−24. GPIO Port B Data (GPBDAT) Register Bit Descriptions

Bit	Field	Type	Reset	Description	
31−4	Reserved	R/W	x		
3	GPIO35	R/W	x		
				0	Reading a 0 indicates that the state of the pin is currently low, irrespective of which mode the pin is in. Writing a 0 will force an output of 0 if the pin is configured as a GPIO in the appropriate MUX and DIR registers; otherwise, the value is latched but not used to drive the pin.
				1	Reading a 1 indicates that the state of the pin is currently high irrespective of which mode the pin is in. Writing a 1 will force an output of 1 if the pin is configured as a GPIO output in the appropriate MUX and DIR registers; otherwise, the value is latched but not used to drive the pin.
2	GPIO34	R/W	x		
1	GPIO33	R/W	x		
0	GPIO32	R/W	x		

Note: x = The state of the GPADAT register is unknown after reset. It depends on the state of the input pin after reset.

Table 4−25. GPIO Port A Set (GPASET) Register Bit Descriptions

Bit	Field	Type	Reset	Description	
31	GPIO31	R=0/W	0	0	Writes of 0 are ignored.
				1	Writing a 1 forces the respective output data latch to 1.
					This register always reads back a 0.
30	GPIO30	R=0/W	0		
29	GPIO29	R=0/W	0		
28	GPIO28	R=0/W	0		
27	GPIO27	R=0/W	0		
26	GPIO26	R=0/W	0		
25	GPIO25	R=0/W	0		
24	GPIO24	R=0/W	0		

Table 4−25. GPIO Port A Set (GPASET) Register Bit Descriptions (Continued)

Bit	Field	Type	Reset	Description
23	GPIO23	R=0/W	0	
22	GPIO22	R=0/W	0	
21	GPIO21	R=0/W	0	
20	GPIO20	R=0/W	0	
19	GPIO19	R=0/W	0	
18	GPIO18	R=0/W	0	
17	GPIO17	R=0/W	0	
16	GPIO16	R=0/W	0	
15	GPIO15	R=0/W	0	
14	GPIO14	R=0/W	0	
13	GPIO13	R=0/W	0	
12	GPIO12	R=0/W	0	
11	GPIO11	R=0/W	0	
10	GPIO10	R=0/W	0	
9	GPIO9	R=0/W	0	
8	GPIO8	R=0/W	0	
7	GPIO7	R=0/W	0	
6	GPIO6	R=0/W	0	
5	GPIO5	R=0/W	0	
4	GPIO4	R=0/W	0	
3	GPIO3	R=0/W	0	
2	GPIO2	R=0/W	0	
1	GPIO1	R=0/W	0	
0	GPIO0	R=0/W	0	

Table 4−26. GPIO Port B Set (GPBSET) Register Bit Descriptions

Bit	Field	Type	Reset	Description
31−4	Reserved	R=0/W	0	
3	GPIO35	R=0/W	0	This register always reads back a 0. 0 Writes of 0 are ignored. 1 Writing a 1 forces the respective output data latch to 1.
2	GPIO34	R=0/W	0	
1	GPIO33	R=0/W	0	
0	GPIO32	R=0/W	0	

Table 4−27. GPIO Port A Clear (GPACLEAR) Register Bit Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R=0/W	0	This register always reads back a 0. 0 Writes of 0 are ignored. 1 Writing a 1 forces the respective output data latch to 0.
30	GPIO30	R=0/W	0	
29	GPIO29	R=0/W	0	
28	GPIO28	R=0/W	0	
27	GPIO27	R=0/W	0	
26	GPIO26	R=0/W	0	
25	GPIO25	R=0/W	0	
24	GPIO24	R=0/W	0	
23	GPIO23	R=0/W	0	
22	GPIO22	R=0/W	0	
21	GPIO21	R=0/W	0	
20	GPIO20	R=0/W	0	
19	GPIO19	R=0/W	0	
18	GPIO18	R=0/W	0	

Table 4−27. GPIO Port A Clear (GPACLEAR) Register Bit Descriptions (Continued)

Bit	Field	Type	Reset	Description
17	GPIO17	R=0/W	0	
16	GPIO16	R=0/W	0	
15	GPIO15	R=0/W	0	
14	GPIO14	R=0/W	0	
13	GPIO13	R=0/W	0	
12	GPIO12	R=0/W	0	
11	GPIO11	R=0/W	0	
10	GPIO10	R=0/W	0	
9	GPIO9	R=0/W	0	
8	GPIO8	R=0/W	0	
7	GPIO7	R=0/W	0	
6	GPIO6	R=0/W	0	
5	GPIO5	R=0/W	0	
4	GPIO4	R=0/W	0	
3	GPIO3	R=0/W	0	
2	GPIO2	R=0/W	0	
1	GPIO1	R=0/W	0	
0	GPIO0	R=0/W	0	

Table 4−28. GPIO Port B Clear (GPCLEAR) Register Bit Descriptions

Bit	Field	Type	Reset	Description
31−4	Reserved	R=0/W	0	
3	GPIO35	R=0/W	0	This register always reads back a 0. 0 Writes of 0 are ignored. 1 Writing a 1 will force the respective output data latch to 0.
2	GPIO34	R=0/W	0	
1	GPIO33	R=0/W	0	
0	GPIO32	R=0/W	0	

Table 4−29. GPIO Port A Toggle (GPATOGGLE) Register Bit Descriptions

Bit	Field	Type	Reset	Description
31	GPIO31	R=0/W	0	This register always reads back a 0. 0 Writes of 0 are ignored. 1 Writing a 1 will force the respective output data latch to toggle from its current state.
30	GPIO30	R=0/W	0	
29	GPIO29	R=0/W	0	
28	GPIO28	R=0/W	0	
27	GPIO27	R=0/W	0	
26	GPIO26	R=0/W	0	
25	GPIO25	R=0/W	0	
24	GPIO24	R=0/W	0	
23	GPIO23	R=0/W	0	
22	GPIO22	R=0/W	0	
21	GPIO21	R=0/W	0	
20	GPIO20	R=0/W	0	
19	GPIO19	R=0/W	0	

Table 4−29. GPIO Port A Toggle (GPATOGGLE) Register Bit Descriptions (Continued)

Bit	Field	Type	Reset	Description
18	GPIO18	R=0/W	0	
17	GPIO17	R=0/W	0	
16	GPIO16	R=0/W	0	
15	GPIO15	R=0/W	0	
14	GPIO14	R=0/W	0	
13	GPIO13	R=0/W	0	
12	GPIO12	R=0/W	0	
11	GPIO11	R=0/W	0	
10	GPIO10	R=0/W	0	
9	GPIO9	R=0/W	0	
8	GPIO8	R=0/W	0	
6	GPIO6	R=0/W	0	
7	GPIO7	R=0/W	0	
5	GPIO5	R=0/W	0	
4	GPIO4	R=0/W	0	
3	GPIO3	R=0/W	0	
2	GPIO2	R=0/W	0	
1	GPIO1	R=0/W	0	
0	GPIO0	R=0/W	0	

Table 4−30. GPIO Port B Clear (GPCLEAR) Register Bit Descriptions

Bit	Field	Type	Reset	Description
31−4	Reserved	R=0/W	0	
3	GPIO35	R=0/W	0	This register always reads back a 0. 0 Writes of 0 are ignored. 1 Writing a 1 will force the respective output data latch to toggle from its current state.
2	GPIO34	R=0/W	0	
1	GPIO33	R=0/W	0	
0	GPIO32	R=0/W	0	

Table 4−31. GPIO XINT1 Interrupt Select (GPIOXINT1SEL) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
15−5	Reserved	R=0	0:0	
4−0	GPIOSEL	R/W	0:0	Select which port A GPIO signal (GPIO0 – GPIO31) will be used as the $\overline{\text{XINT1}}$ interrupt source: 00000 Select GPIO0 pin (default) 00001 Select GPIO1 pin …. 11110 Select GPIO30 pin 11111 Select GPIO31 pin

Note: This register is EALLOW protected.

Table 4−32. GPOIO XINT2 Interrupt Select (GPIOXINT2SEL) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
15−5	Reserved	R=0	0:0	
4−0	GPIOSEL	R/W	0:0	Select which port A GPIO signal (GPIO0 – GPIO31) will be used as the XINT2 interrupt source: 00000 Select GPIO0 pin (default) 00001 Select GPIO1 pin …. 11110 Select GPIO30 pin 11111 Select GPIO31 pin

Note: The above register is EALLOW protected.

Table 4−33. GPIO XNMI Interrupt Select (GPIOXNMISEL) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
15−5	Reserved	R=0	0:0	
4−0	GPIOSEL	R/W	0:0	Select which port A GPIO signal (GPIO0 – GPIO31) will be used as the XNMI interrupt source: 00000 Select GPIO0 pin (default) 00001 Select GPIO1 pin …. 11110 Select GPIO30 pin 11111 Select GPIO31 pin

Note: This register is EALLOW protected.

Table 4−34. GPIO Low Power Mode Wakeup Select (GPIOLPMSEL) Register Bit Descriptions

Bit(s)	Field	Type	Reset	Description
31	GPIO31	R/W	0	
				0 If the bit is cleared, the signal will have no effect in HALT and STANDBY low power modes.
				1 If the respective bit is set to 1, it will enable the selected signal to wake the device from HALT and STANDBY low power modes.
30	GPIO30	R/W	0	
29	GPIO29	R/W	0	
28	GPIO28	R/W	0	
27	GPIO27	R/W	0	
26	GPIO26	R/W	0	
25	GPIO25	R/W	0	
24	GPIO24	R/W	0	
23	GPIO23	R/W	0	
22	GPIO22	R/W	0	
21	GPIO21	R/W	0	
20	GPIO20	R/W	0	
19	GPIO19	R/W	0	
18	GPIO18	R/W	0	
17	GPIO17	R/W	0	
16	GPIO16	R/W	0	
15	GPIO15	R/W	0	
14	GPIO14	R/W	0	
13	GPIO13	R/W	0	
12	GPIO12	R/W	0	
11	GPIO11	R/W	0	

Note: This register is EALLOW protected.

Table 4−34. GPIO Low Power Mode Wakeup Select (GPIOLPMSEL) Register Bit Descriptions (Continued)

Bit(s)	Field	Type	Reset	Description
10	GPIO10	R/W	0	
9	GPIO9	R/W	0	
8	GPIO8	R/W	0	
7	GPIO7	R/W	0	
6	GPIO6	R/W	0	
5	GPIO5	R/W	0	
4	GPIO4	R/W	0	
3	GPIO3	R/W	0	
2	GPIO2	R/W	0	
1	GPIO1	R/W	0	
0	GPIO0	R/W	0	

Note: This register is EALLOW protected.

This page is intentionally left blank.

Chapter 5

Peripheral Frames

This chapter describes the peripheral frames. It also describes the device emulation registers.

Topic **Page**

5.1	Peripheral Frame Registers	5-2
5.2	EALLOW-protected Registers	5-6
5.3	Device Emulation Registers	5-14
5.4	Write-Followed-by-Read Protection	5-16

5.1 Peripheral Frame Registers

The 280x devices contain three peripheral register spaces. The spaces are categorized as follows:

- Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See Table 5−1.
- Peripheral Frame 1: These are peripherals that are mapped to the 32-bit peripheral bus. See Table 5−2.
- Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See Table 5−3.

Table 5−1. Peripheral Frame 0 Registers

Name	Address Range	Size (x16)	Access Type†
Device Emulation Registers	0x0880 0x09FF	384	EALLOW-protected
Reserved	0x0A00 0x0A7F	128	
FLASH Registers‡	0x0A80 0x0ADF	96	EALLOW-protected CSM Protected
Code Security Module Registers	0x0AE0 0x0AEF	16	EALLOW-protected
Reserved	0x0AF0 0x0BFF	272	
CPU-TIMER0/1/2 Registers	0x0C00 0x0C3F	64	Not EALLOW-protected
Reserved	0x0C40 0x0CDF	160	
PIE Registers	0x0CE0 0x0CFF	32	Not EALLOW-protected
PIE Vector Table	0x0D00 0x0DFF	256	EALLOW-protected
Reserved	0x0E00 0x0FFF	512	

† If registers are EALLOW-protected, you cannot perform writes until you execute the EALLOW instruction. The EDIS instruction disables writes to prevent stray code or pointers from corrupting register contents.
‡ The flash registers are also protected by the Code Security Module (CSM).

Table 5−2. Peripheral Frame 1 Registers

Name	Address Range	Size (x16)	Access Type†
eCANA Registers	0x6000 0x60FF	256 (128 x 32)	Some eCAN control registers (and selected bits in other eCAN control registers) are EALLOW-protected.
eCANA Mailbox RAM	0x6100 0x61FF	256 (128 x 32)	Not EALLOW-protected
eCANB Registers	0x6200 0x62FF	256 (128 x 32)	Some eCAN control registers (and selected bits in other eCAN control registers) are EALLOW-protected.
eCANB Mailbox RAM	0x6300 0x63FF	256 (128 x 32)	Not EALLOW-protected
Reserved	0x6400 0x65FF	1024	
ePWM1 Registers	0x6800 0x683F	64 (32 x 32)	Some ePWM registers are EALLOW-protected. See section 5.2.
ePWM2 Registers	0x6840 0x687F	64 (32 x 32)	Some ePWM registers are EALLOW-protected. See section 5.2.
ePWM3 Registers	0x6880 0x68BF	64 (32 x 32)	Some ePWM registers are EALLOW-protected. See section 5.2.
ePWM4 Registers	0x68C0 0x68FF	64 (32 x 32)	Some ePWM registers are EALLOW-protected. See section 5.2.
ePWM5 Registers	0x6900 0x693F	64 (32 x 32)	Some ePWM registers are EALLOW-protected. See section 5.2.
ePWM6 Registers	0x6940 0x697F	64 (32 x 32)	Some ePWM registers are EALLOW-protected. See section 5.2.
Reserved	0x6980 0x69FF	128	
eCAP1 Registers	0x6A00 0x6A1F	32 (16 x 32)	Not EALLOW-protected
eCAP2 Registers	0x6A20 0x6A3F	32 (16 x 32)	Not EALLOW-protected
eCAP3 Registers	0x6A40 0x6A5F	32 (16 x 32)	Not EALLOW-protected

† Peripheral Frame 1 allows 16-bit and 32-bit accesses. All 32-bit accesses are aligned to even address boundaries.

Table 5−2. Peripheral Frame 1 Registers (Continued)

Name	Address Range	Size (x16)	Access Type†
eCAP4 Registers	0x6A60 0x6A7F	32 (16 x 32)	Not EALLOW-protected
Reserved	0x6A80 0x6AFF	32 (16 x 32)	Not EALLOW-protected
eQEP1 Registers	0x6B00 0x6B3F	64 (32 x 32)	Not EALLOW-protected
eQEP2 Registers	0x6B40 0x6B7F	64 (32 x 32)	Not EALLOW-protected
GPIO Control Registers	0x6F80 0x6FBF	128 (64 x 32)	EALLOW-protected
GPIO Data Registers	0x6FC0 0x6FDF	32 (16 x 32)	Not EALLOW-protected
GPIO Interrupt and LPM Select Registers	0x6FE0 0x6FFF	32 (16 x 32)	EALLOW-protected

† Peripheral Frame 1 allows 16-bit and 32-bit accesses. All 32-bit accesses are aligned to even address boundaries.

Table 5−3. Peripheral Frame 2 Registers†

Name	Address Range	Size (x16)	Access Type†
Reserved	0x7000 0x700F	16	
System Control Registers	0x7010 0x702F	32	EALLOW-protected
Reserved	0x7030 0x703F	16	
SPI−A Registers	0x7040 0x704F	16	Not EALLOW-protected
SCI-A Registers	0x7050 0x705F	16	Not EALLOW-protected
Reserved	0x7060 0x706F	128	
ADC Registers	0x7100 0x711F	32	Not EALLOW-protected
Reserved	0x7120 0x773F	224	
SPI-B Registers	0x00 7740 0x00 774F	16	Not EALLOW-protected
SCI-B Registers	0x00 7750 0x00 775F	16	Not EALLOW-protected
SPI-C Registers	0x00 7760 0x00 776F	16	Not EALLOW-protected
Reserved	0x00 7770 0x00 777F	16	
SPI-D Registers	0x00 7780 0x00 778F	16	Not EALLOW-protected
Reserved	0x00 7780 0x00 778F	16	Not EALLOW-protected
I2C Registers	0x00 7900 0x00 793F	64	Not EALLOW-protected
Reserved	0x00 7940 0x00 7FFF	1728	

† Peripheral Frame 2 only allows 16-bit accesses. All 32-bit accesses are ignored (invalid data can be returned or written).

5.2 EALLOW-protected Registers

Several control registers on the 280x devices are protected from spurious CPU writes by the EALLOW protection mechanism. The EALLOW bit in status register 1 (ST1) indicates if the state of protection as shown in Table 5−4.

Table 5−4. Access to EALLOW-protected Registers

EALLOW Bit	CPU Writes	CPU Reads	JTAG Writes	JTAG Reads
0	Ignored	Allowed	Allowed†	Allowed
1	Allowed	Allowed	Allowed	Allowed

† The EALLOW bit is overridden via the JTAG port, allowing full access of protected registers during debug from the Code Composer Studio interface.

At reset the EALLOW bit is cleared enabling EALLOW protection. While protected, all writes to protected registers by the CPU are ignored and only CPU reads, JTAG reads, and JTAG writes are allowed. If this bit is set, by executing the EALLOW instruction, then the CPU is allowed to write freely to protected registers. After modifying registers, they can once again be protected by executing the EDI instruction to clear the EALLOW bit.

The following registers are EALLOW-protected:

- Device Emulation Registers
- Flash Registers
- CSM Registers
- PIE Vector Table
- System Control Registers
- GPIO MUX Registers
- Certain eCAN Registers

Table 5−5. EALLOW-protected Device Emulation Registers

Name	Address Range	Size (x16)	Description
DEVICECNF	0x0880 0x0881	2	Device Configuration Register
PROTSTART	0x0884	1	Block Protection Start Address Register
PROTRANGE	0x0885	1	Block Protection Range Address Register

Table 5−6. EALLOW-protected Flash/OTP Configuration Registers

Name	Address	Size (x16)	Description
		Configuration Registers	
FOPT	0x0000−0A80	1	Flash Option Register
FPWR	0x0000−0A82	1	Flash Power Modes Register
FSTATUS	0x0000−0A83	1	Status Register
FSTDBYWAIT	0x0000−0A84	1	Flash Sleep To Standby Wait State Register
FACTIVEWAIT	0x0000−0A85	1	Flash Standby To Active Wait State Register
FBANKWAIT	0x0000−0A86	1	Flash Read Access Wait State Register
FOTPWAIT	0x0000−0A87	1	OTP Read Access Wait State Register

Table 5−7. EALLOW-protected Code Security Module (CSM) Registers

Register Name	Memory Address	Reset Values	Register Description
KEY Registers − Accessible by the User			
KEY0	0x0AE0	0xFFFF	Low word of the 128-bit KEY register
KEY1	0x0AE1	0xFFFF	Second word of the 128-bit KEY register
KEY2	0x0AE2	0xFFFF	Third word of the 128-bit KEY register
KEY3	0x0AE3	0xFFFF	Fourth word of the 128-bit KEY register
KEY4	0x0AE4	0xFFFF	Fifth word of the 128-bit KEY register
KEY5	0x0AE5	0xFFFF	Sixth word of the 128-bit KEY register
KEY6	0x0AE6	0xFFFF	Seventh word of the 128-bit KEY register
KEY7	0x0AE7	0xFFFF	High word of the 128-bit KEY register
CSMSCR	0x0AEF		CSM status and control register

Table 5−8. EALLOW-protected PIE Vector Table

Name	Address	Size (x16)	Description	CPU Priority	PIE Group Priority
Not used	0x0D00	2	Reserved	−	−
	0x0D02				
	0x0D04				
	0x0D06				
	0x0D08				
	0x0D0A				
	0x0D0C				
	0x0D0E				
	0x0D10				
	0x0D12				
	0x0D14				
	0x0D16				
	0x0D18				
INT13	0x0D1A	2	External Interrupt 13 (XINT13) or CPU-Timer 1 (for RTOS use)	17	−
INT14	0x0D1C	2	CPU-Timer 2 (for RTOS use)	18	−
DATALOG	0x0D1E	2	CPU Data Logging Interrupt	19 (lowest)	−
RTOSINT	0x0D20	2	CPU Real-Time OS Interrupt	4	−
EMUINT	0x0D22	2	CPU Emulation Interrupt	2	−
NMI	0x0D24	2	External Non-Maskable Interrupt	3	−
ILLEGAL	0x0D26	2	Illegal Operation	−	−
USER0	0x0D28	2	User-Defined Trap	−	−
.	.	.	.	.	.
USER11	0x0D3E	2	User-Defined Trap	−	−
INT1.1	0x0D40	2	Group 1 Interrupt Vectors	5	1 (highest)
.	.	.			.
INT1.8	0x0D4E	2			8 (lowest)
.	.	.	Group 2 Interrupt Vectors	6	
.	.	.	to Group 11 Interrupt Vectors	to	
.	.	.		15	
INT12.1	0x0DF0	2	Group 12 Interrupt Vectors	16	1 (highest)
.	.	.			.
INT12.8	0x0DFE	2			8 (lowest)

Table 5−9. EALLOW-protected PLL, Clocking, Watchdog, and Low-Power Mode Registers

Name	Address	Size (x16)	Description
XCLK	0x7010	1	XCLKOUT Pin Control and X1/XCLKIN Status Register
PLLSTS	0x7011	1	PLL Status Register
HISPCP	0x701A	1	High-Speed Peripheral Clock Prescaler Register for HSPCLK Clock
LOSPCP	0x701B	1	Low-Speed Peripheral Clock Prescaler Register for HSPCLK Clock
PCLKCR0	0x701C	1	Peripheral Clock Control Register 0
PCLKCR1	0x701D	1	Peripheral Clock Control Register 1
LPMCR0	0x701E	1	Low Power Mode Control Register 0
PLLCR	0x7021	1	PLL Control Register
SCSR	0x7022	1	System Control and Status Register
WDCNTR	0x7023	1	Watchdog Counter Register
WDKEY	0x7025	1	Watchdog Reset Key Register
WDCR	0x7029	1	Watchdog Control Register

Table 5−10. EALLOW-protected GPIO MUX Registers

Name	Address	Size x16	Register description
GPACTRL	0x0000−6F80	2	GPIO A Control Register (GPIO0 to 31)
GPAQSEL1	0x0000−6F82	2	GPIO A Qualifier Select 1 Register (GPIO0 to 15)
GPAQSEL2	0x0000−6F84	2	GPIO A Qualifier Select 2 Register (GPIO16 to 31)
GPAMUX1	0x0000−6F86	2	GPIO A Mux 1 Register (GPIO0 to 15)
GPAMUX2	0x0000−6F88	2	GPIO A Mux 2 Register (GPIO16 to 31)
GPADIR	0x0000−6F8A	2	GPIO A Direction Register (GPIO0 to 31)
GPAPUD	0x0000−6F8C	2	GPIO A Pull Up Disable Register (GPIO0 to 31)
GPBCTRL	0x0000−6F90	2	GPIO B Control Register (GPIO32 to 35)
GPBQSEL1	0x0000−6F92	2	GPIO B Qualifier Select 1 Register (GPIO32 to 35)
GPBQSEL2	0x0000−6F94	2	reserved

Table 5−10. EALLOW-protected GPIO MUX Registers (Continued)

Name	Address	Size x16	Register description
GPBMUX1	0x0000−6F96	2	GPIO B Mux 1 Register (GPIO32 to 35)
GPBMUX2	0x0000−6F98	2	reserved
GPBDIR	0x0000−6F9A	2	GPIO B Direction Register (GPIO32 to 35)
GPBPUD	0x0000−6F9C	2	GPIO B Pull Up Disable Register (GPIO32 to 35)
GPIOXINT1SEL	0x0000−6FE0	1	XINT1 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT2SEL	0x0000−6FE1	1	XINT2 GPIO Input Select Register (GPIO0 to 31)
GPIOXNMISEL	0x0000−6FE2	1	XNMI GPIO Input Select Register (GPIO0 to 31)
GPIOLPMSEL	0x0000−6FE8	2	LPM GPIO Select Register (GPIO0 to 31)

Table 5−11. EALLOW-protected eCAN−A Registers

Name	Address	Size (x16)	Description
CANMC	0x0000−6014	2	Master Control Register†
CANBTC	0x0000−6016	2	Bit Timing Configuration Register‡
CANGIM	0x0000−6020	2	Global Interrupt Mask Register§
CANMIM	0x0000−6024	2	Mailbox Interrupt Mask Register
CANTSC	0x0000−602E	2	Time Stamp Counter
CANTIOC	0x0000−602A	1	I/O Control Register for CANTXA Pin¶
CANRIOC	0x0000−602C	1	I/O Control Register for CANRXA Pin#

† Only bits CANMC[15:9] and [7:6] are protected
‡ Only bits BCR[23:16] and [10:0] are protected
§ Only bits CANGIM[17:16] , [14:8], and [2:0] are protected
¶ Only IOCONT1[3] is protected
# Only IOCONT2[3] is protected

Table 5−12. EALLOW-protected eCAN−B Registers

Name	Address	Size x16	Register description
CANMC	0x0000−6214	2	Master Control Register†
CANBTC	0x0000−6216	2	Bit Timing Configuration Register‡
CANGIM	0x0000−6220	2	Global Interrupt Mask Register§
CANMIM	0x0000−6224	2	Mailbox Interrupt Mask Register
CANTSC	0x0000−622E	2	Time Stamp Counter
CANTIOC	0x0000−622A	2	I/O Control Register for CANTXA Pin¶
CANRIOC	0x0000−622C	2	I/O Control Register for CANRXA Pin#

† Only bits CANMC[15:9] and [7:6] are protected
‡ Only bits BCR[23:16] and [10:0] are protected
§ Only bits CANGIM[17:16] , [14:8], and [2:0] are protected
¶ Only IOCONT1[3] is protected
# Only IOCONT2[3] is protected

Table 5−13. EALLOW-protected ePWM−1 Registers

Name	Address	Size x16	Register description
TZSEL	0x0000−6812	1	Trip Zone Select Register
TZDCSEL	0x0000−6813	1	Trip Zone Digital Comparator Select Register
TZCTL	0x0000−6814	1	Trip Zone Control Register
TZEINT	0x0000−6815	1	Trip Zone Enable Interrupt Register
TZCLR	0x0000−6817	1	Trip Zone Clear Register
TZFRC	0x0000−6818	1	Trip Zone Force Register

Table 5−14. EALLOW-protected ePWM−2 Registers

Name	Address	Size x16	Register description
TZSEL	0x0000−6852	1	Trip Zone Select Register
TZDCSEL	0x0000−6853	1	Trip Zone Digital Comparator Select Register
TZCTL	0x0000−6854	1	Trip Zone Control Register
TZEINT	0x0000−6855	1	Trip Zone Enable Interrupt Register
TZCLR	0x0000−6857	1	Trip Zone Clear Register
TZFRC	0x0000−6858	1	Trip Zone Force Register

Table 5−15. EALLOW-Protected ePWM−3 Registers

Name	Address	Size x16	Register description
TZSEL	0x0000−6892	1	Trip Zone Select Register
TZDCSEL	0x0000−6893	1	Trip Zone Digital Comparator Select Register
TZCTL	0x0000−6894	1	Trip Zone Control Register
TZEINT	0x0000−6895	1	Trip Zone Enable Interrupt Register
TZCLR	0x0000−6897	1	Trip Zone Clear Register
TZFRC	0x0000−6898	1	Trip Zone Force Register

Table 5−16. EALLOW-Protected ePWM−4 Registers

Name	Address	Size x16	Register description
TZSEL	0x0000−68D2	1	Trip Zone Select Register
TZDCSEL	0x0000−68D3	1	Trip Zone Digital Comparator Select Register
TZCTL	0x0000−68D4	1	Trip Zone Control Register
TZEINT	0x0000−68D5	1	Trip Zone Enable Interrupt Register
TZCLR	0x0000−68D7	1	Trip Zone Clear Register
TZFRC	0x0000−68D8	1	Trip Zone Force Register

Table 5−17. EALLOW-Protected ePWM−5 Registers

Name	Address	Size x16	Register description
TZSEL	0x0000−6912	1	Trip Zone Select Register
TZDCSEL	0x0000−6913	1	Trip Zone Digital Comparator Select Register
TZCTL	0x0000−6914	1	Trip Zone Control Register
TZEINT	0x0000−6915	1	Trip Zone Enable Interrupt Register
TZCLR	0x0000−6917	1	Trip Zone Clear Register
TZFRC	0x0000−6918	1	Trip Zone Force Register

Table 5−18. EALLOW-Protected ePWM−6 Registers

Name	Address	Size x16	Register description
TZSEL	0x0000−6952	1	Trip Zone Select Register
TZDCSEL	0x0000−6953	1	Trip Zone Digital Comparator Select Register
TZCTL	0x0000−6954	1	Trip Zone Control Register
TZEINT	0x0000−6955	1	Trip Zone Enable Interrupt Register
TZCLR	0x0000−6957	1	Trip Zone Clear Register
TZFRC	0x0000−6958	1	Trip Zone Force Register

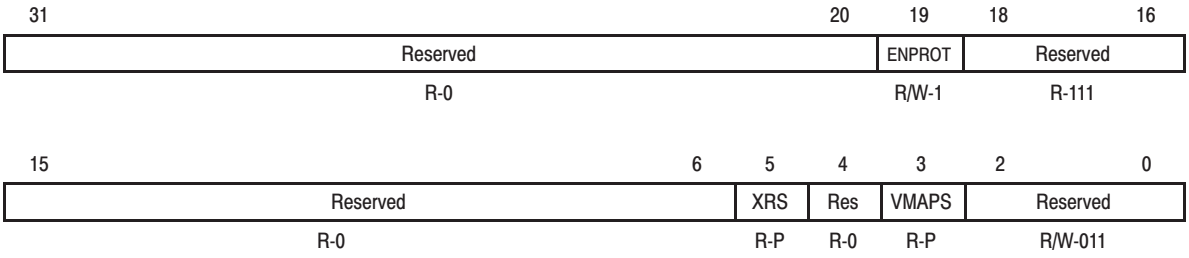
5.3 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 5−19.

Table 5−19. Device Emulation Registers

Name	Address Range	Size (x16)	Description
DEVICECNF	0x0880 0x0881	2	Device Configuration Register
Reserved	0x0882	1	
DEVICEID	0x0883	2	Device ID Register
PROTSTART	0x0884	1	Block Protection Start Address Register
PROTRANGE	0x0885	1	Block Protection Range Address Register
Reserved	0x0886 0x09FF	378	

Figure 5−1. Device Configuration (DEVICECNF) Register



Legend: R = Read, W = Write, P = pin value after reset, -n = reset value

Note: EALLOW-protected register

Table 5−20. DEVICECNF Register Bit Descriptions

Bits	Field	Value	Description
31−20	Reserved		
19	ENPROT		Enable Write-Read Protection Mode Bit.
		0	Disables write-read protection mode
		1	Enables write-read protection as specified by the PROTSTART and PROTRANGE registers
18−6	Reserved		
5	XRS		Reset Input Signal Status. This is connected directly to the $\overline{\text{XRS}}$ input pin.
4	Reserved		
3	VMAPS		VMAP Configure Status. This indicates the status of VMAP.
2−0	Reserved		

Figure 5−2. DEVICEID Register

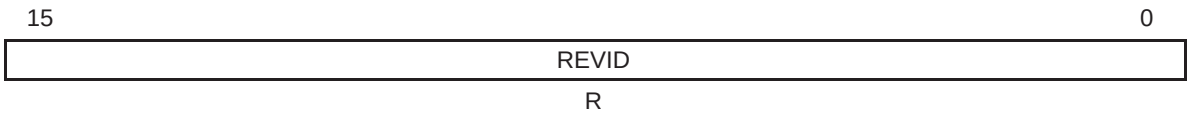


Table 5−21. DEVICEID Register Bit Description

Bits	Field	Reset	Description
15−0	REVID	These 16 bits specify the silicon revision number for the particular part. This number always starts with 0x0000 on the first revision of the silicon and is incremented on any subsequent revisions.	
		0x0000	Revision 0 (for first silicon)
		0x0001	Revision A
		0x0002	Revision B and so forth

5.4 Write-Followed-by-Read Protection

The PROTSTART and PROTRANGE registers set the memory address range for which CPU “write” followed by “read” operations are protected (operations occur in sequence rather then in their natural pipeline order). This is necessary protection for certain peripheral operations.

Example: The following lines of code perform a write to register 1 (REG1) location and then the next instruction performs a read from Register 2 (REG2) location. On the processor memory bus, with block protection disabled, the read operation is issued before the write as shown:

```
MOV    @REG1,AL      -----  +
TBIT   @REG2,#BIT_X  -----  |----> Read
                     +----> Write
```

If block protection is enabled, then the read is stalled until the write occurs as shown:

```
MOV    @REG1,AL      -----  +
TBIT   @REG2,#BIT_X  ---    +      |
                     |      +----> Write
                     +------> Read
```

NOTE: The C28x CPU automatically protects writes followed by reads to the same memory address. The protection mechanism described above is for cases where the address is not the same, but within a given region in memory (as defined by the PROTSTART and PROTRANGE registers).

Table 5−22. PROTSTART and PROTRANGE Registers

Name	Address	Size	Type	Reset	Description
PROTSTART	0x0884	16	R/W	0x0100†	The PROTSTART register sets the starting address relative to the 16 most significant bits of the processors lower 22-bit address reach. Hence, the smallest resolution is 64 words.
PROTRANGE	0x0885	16	R/W	0x00FF†	The PROTRANGE register sets the block size (from the starting address), starting with 64 words and incrementing by binary multiples (64, 128, 256, 512, 1K, 2K, 4K, 8K, 16K, ..., 2M).

† The default values of these registers on reset are selected to cover the Peripheral Frame 1, Peripheral Frame 2, and XINTF Zone 1 areas of the memory map (address range 0x4000 to 0x8000).

Table 5−23. PROTSTART Valid Values†

Start Address	Register Value	Register Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0040	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x0000 0080	0x0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0x0000 00C0	0x0003	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
0x003F FF00	0xFFFC	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
0x003F FF40	0xFFFD	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0x003F FF80	0xFFFE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0x003F FFC0	0xFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

† The quickest way to calculate register value is to divide the desired block starting address by 64.

Table 5−24. PROTRANGE Valid Values‡

Block Size	Register Value	Register Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
64	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
128	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
256	0x0003	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
512	0x0007	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
1K	0x000F	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
2K	0x001F	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
4K	0x003F	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
8K	0x007F	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
16K	0x00FF	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
32K	0x01FF	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
64K	0x03FF	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
128K	0x07FF	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
256K	0x0FFF	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
512K	0x1FFF	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1M	0x3FFF	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2M	0x7FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4M	0xFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

‡ Not all register values are valid. The PROTSTART address value must be a multiple of the range value. For example: if the block size is set to 4K, then the start address can only be at any 4K boundary.

Chapter 6

Peripheral Interrupt Expansion (PIE)

The peripheral interrupt expansion (PIE) block multiplexes numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support 96 individual interrupts that are grouped into blocks of eight. Each group is fed into one of 12 core interrupt lines ($\overline{INT1}$ to $\overline{INT12}$). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that you can modify. The CPU, upon servicing the interrupt, automatically fetches the appropriate interrupt vector. It takes nine CPU clock cycles to fetch the vector and save critical CPU registers. Therefore, the CPU can respond quickly to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the PIE block.

Topic **Page**

6.1 Overview of the PIE Controller 6-2
6.2 Vector Table Mapping 6-6
6.3 Interrupt Sources 6-9
6.4 PIE Configuration Registers 6-24
6.5 PIE Interrupt Registers 6-26
6.6 External Interrupt Control Registers 6-39

6.1 Overview of the PIE Controller

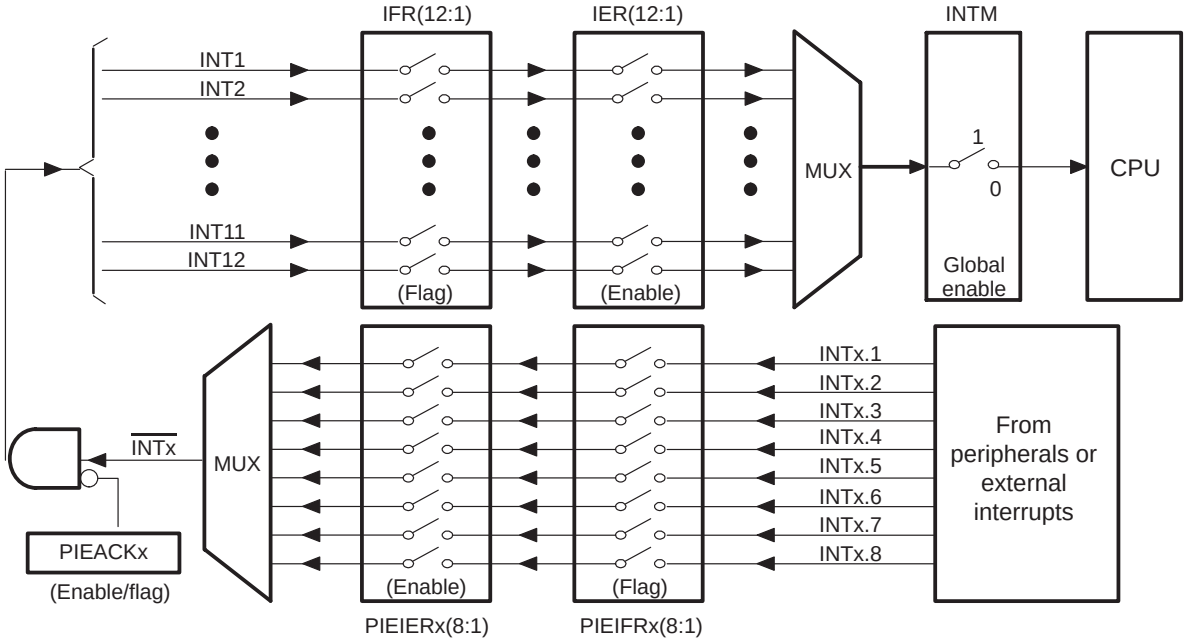
The 28x CPU supports one nonmaskable interrupt (NMI) and 16 maskable prioritized interrupt requests (INT1−INT14, RTOSINT, and DLOGINT) at the CPU level. The 28x devices have many peripherals and each peripheral is capable of generating one or more interrupts in response to many events at the peripheral level. Because the CPU does not have sufficient capacity to handle all peripheral interrupt requests at the CPU level, a centralized peripheral interrupt expansion (PIE) controller is required to arbitrate the interrupt requests from various sources such as peripherals and other external pins.

The PIE vector table is used to store the address (vector) of each interrupt service routine (ISR) within the system. There is one vector per interrupt source including all MUXed and nonMUXed interrupts. You populate the vector table during device initialization and you can update it during operation.

Interrupt Operation Sequence

Figure 6−1 shows an overview of the interrupt operation sequence for all multiplexed PIE interrupts. Interrupt sources that are not multiplexed are fed directly to the CPU.

Figure 6−1. Overview: Multiplexing of Interrupts Using the PIE Block



- **Peripheral Level**

  An interrupt-generating event occurs in a peripheral. The interrupt flag (IF) bit corresponding to that event is set in a register for that particular peripheral.

  If the corresponding interrupt enable (IE) bit is set, the peripheral generates an interrupt request to the PIE controller. If the interrupt is not enabled at the peripheral level, then the IF remains set until cleared by software. If the interrupt is enabled at a later time, and the interrupt flag is still set, the interrupt request is asserted to the PIE.

  Interrupt flags within the peripheral registers must be manually cleared. See the peripheral reference guide for a specific peripheral for more information.

- **PIE Level**

  The PIE block multiplexes eight peripheral and external pin interrupts into one CPU interrupt. These interrupts are divided into 12 groups: PIE group 1 − PIE group 12. The interrupts within a group are multiplexed into one CPU interrupt. For example, PIE group 1 is multiplexed into CPU interrupt 1 (INT1) while PIE group 12 is multiplexed into CPU interrupt 12 (INT12). Interrupt sources connected to the remaining CPU interrupts are not multiplexed. For the nonmultiplexed interrupts, the PIE passes the request directly to the CPU.

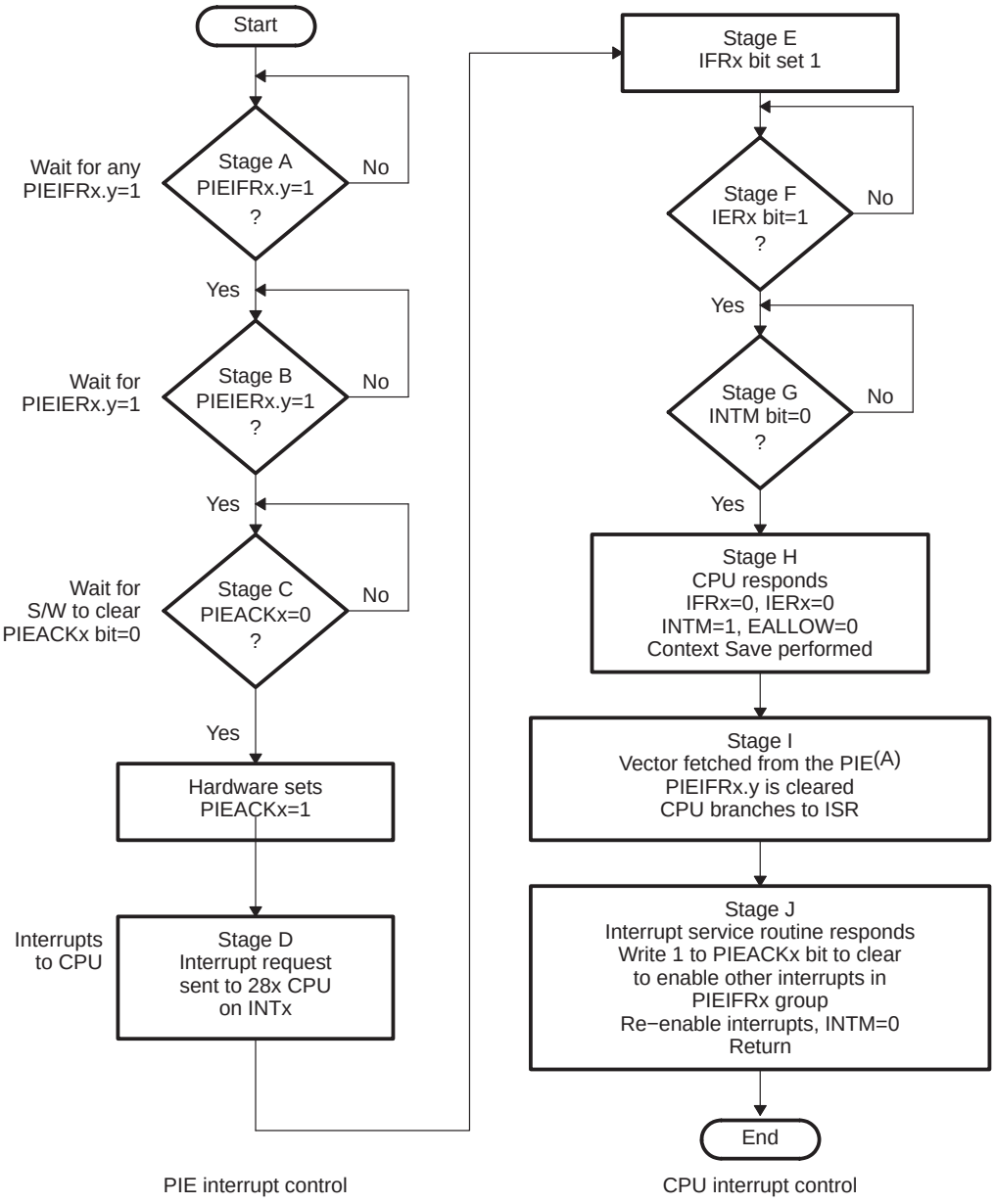
  For multiplexed interrupt sources, each interrupt group in the PIE block has an associated flag bit (PIEIFRx.y) and enable bit (PIEIERx.y). In addition, there is one acknowledge bit (PIEACK) for every PIE interrupt group (INT1 to INT12) referred to as PIEACKx. Figure 6−2 illustrates the behavior of the PIE hardware under various PIEIFR and PIEIER register conditions.

  Once the request is made to the PIE controller, the corresponding PIE interrupt flag (PIEIFRx.y) bit is set. If the PIE interrupt enable (PIEIERx.y) bit is also set for the given interrupt then the PIE checks the corresponding PIEACKx bit to determine if the CPU is ready for an interrupt from that group. If the PIEACKx bit is clear for that group, then the PIE sends the interrupt request to the CPU. If PIEACKx is set, then the PIE waits until it is cleared to send the request for INTx. See Section 6.3 for details.

- **CPU Level**

  Once the request is sent to the CPU, the CPU level interrupt flag (IFR) bit corresponding to INTx is set. After a flag has been latched in the IFR, the corresponding interrupt is not serviced until it is appropriately enabled in the CPU interrupt enable (IER) register or the debug interrupt enable register (DBGIER) and the global interrupt mask (INTM) bit.

Figure 6−2. Typical PIE/CPU Interrupt Response − INTx.y



Note: For multiplexed interrupts, the PIE responds with the highest priority interrupt that is both flagged and enabled. If there is no interrupt that is both flagged and enabled. If there is no interrupt both flagged and enabled, then the highest priority interrupt within the group (INTx.1) is used. See Section 6.3.3 for more details.

As shown in Table 6−1, the requirements for enabling the maskable interrupt at the CPU level depends on the interrupt handling process being used. In the standard process, which happens most of the time, the DBGIER register is not used. When the 28x is in real-time emulation mode and the CPU is halted, a different process is used. In this special case, the DBGIER is used and the INTM bit is ignored. If the DSP is in real-time mode and the CPU is running, the standard interrupt-handling process applies.

Table 6−1. Enabling Interrupt

Interrupt Handling Process	**Interrupt Enabled If**…
Standard	INTM = 0 and bit in IER is 1
DSP in real-time mode and halted	Bit in IER is 1 and DBGIER is 1

The CPU then prepares to service the interrupt. This preparation process is described in detail in *TMS320C28x DSP CPU and Instruction Set Reference Guide* (literature number SPRU430). In preparation, the corresponding CPU IFR and IER bits are cleared, EALLOW and LOOP are cleared, INTM and DBGM are set, the pipeline is flushed and the return address is stored, and the automatic context save is performed. The vector of the ISR is then fetched from the PIE module. If the interrupt request comes from a multiplexed interrupt, the PIE module uses the group PIEIERx and PIEIFRx registers to decode which interrupt needs to be serviced. This decode process is described in detail in Section 6.3.3.

The address for the interrupt service routine that is executed is fetched directly from the PIE interrupt vector table. There is one 32-bit vector for each of the possible 96 interrupts within the PIE. Interrupt flags within the PIE module (PIEIFRx.y) are automatically cleared when the interrupt vector is fetched. The PIE acknowledge bit for a given interrupt group, however, must be cleared manually when ready to receive more interrupts from the PIE group.

6.2 Vector Table Mapping

On 28xx devices, the interrupt vector table can be mapped to five distinct locations in memory. In practice only the PIE vector table mapping is used for 280x devices.

This vector mapping is controlled by the following mode bits/signals:

VMAP:	VMAP is found in Status Register 1 ST1 (bit 3). A device reset sets this bit to 1. The state of this bit can be modified by writing to ST1 or by SETC/CLRC VMAP instructions. For normal F2810/12 operation leave this bit set.
M0M1MAP:	M0M1MAP is found in Status Register 1 ST1 (bit 11). A device reset sets this bit to 1. The state of this bit can be modified by writing to ST1 or by SETC/CLRC M0M1MAP instructions. For normal 28xx device operation, this bit should remain set. M0M1MAP = 0 is reserved for TI testing only.
ENPIE:	ENPIE is found in PIECTRL Register (bit 0). The default value of this bit, on reset, is set to 0 (PIE disabled). The state of this bit can be modified after reset by writing to the PIECTRL register (address 0x0000 0CE0).

Using these bits and signals the possible vector table mappings are shown in Table 6−2.

Table 6−2. Interrupt Vector Table Mapping†

Vector MAPS	Vectors Fetched From	Address Range	VMAP	M0M1MAP	MP/$\overline{MC}$	ENPIE
M1 Vector‡	M1 SARAM Block	0x000000−0x00003F	0	0	X	X
M0 Vector‡	M0 SARAM Block	0x000000−0x00003F	0	1	X	X
BROM Vector	ROM Block	0x3FFFC0−0x3FFFFF	1	X	0	0
PIE Vector	PIE Block	0x000D00−0x000DFF	1	X	X	1

† On the 280x devices, the VMAP and M0M1MAP modes are set to 1 on reset. The ENPIE mode is forced to 0 on reset.
‡ Vector map MO and M1 Vector is a reserved mode only. On the 28x devices these are used as RAM.

The M1 and M0 vector table mapping is reserved for TI testing only. When using other vector mappings, the M0 and M1 memory blocks are treated as RAM blocks and can be used freely without any restrictions.

After a device reset operation, the vector table is mapped as shown in Table 6−3.

Table 6−3. Vector Table Mapping After Reset Operation†

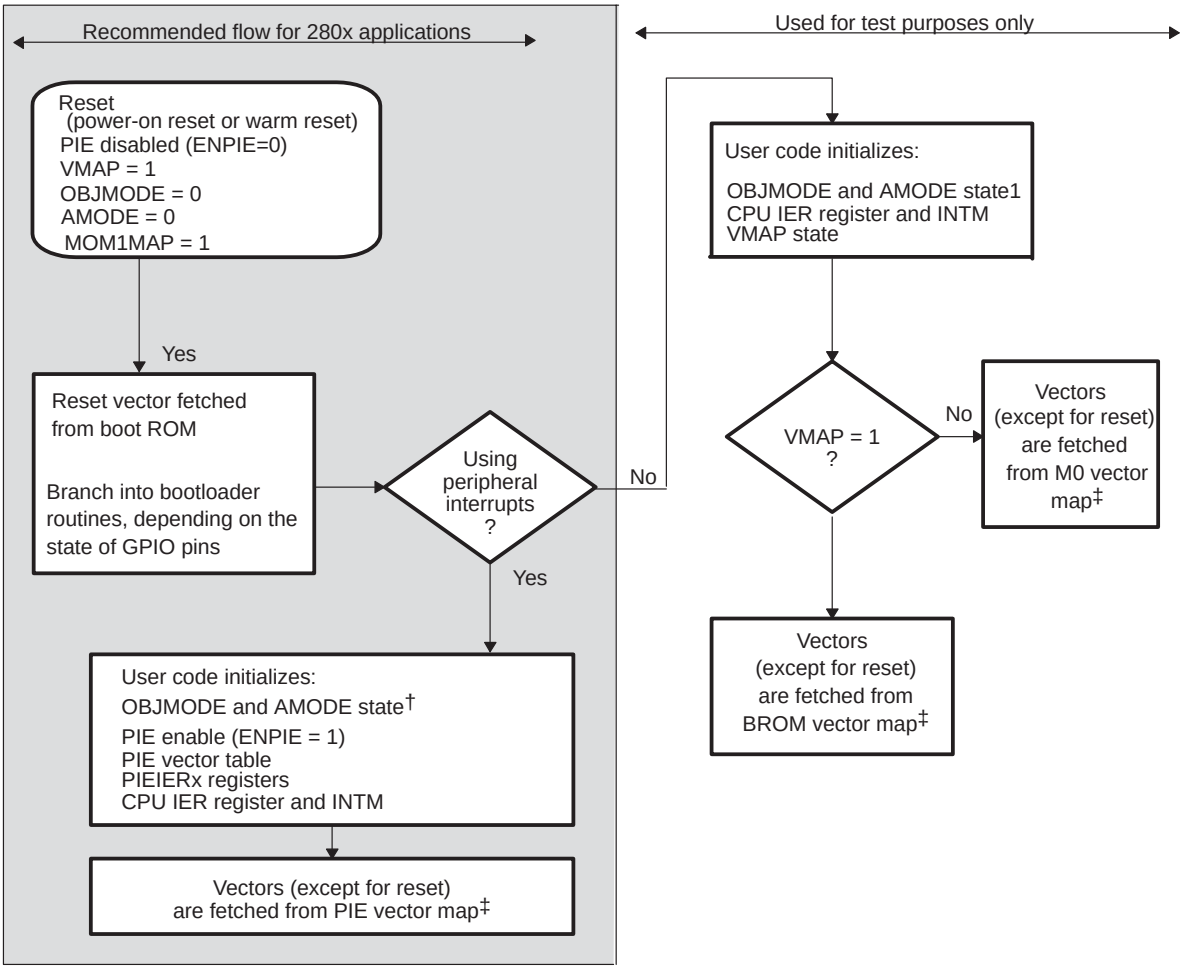
VECTOR MAPS	RESET FETCHED FROM	ADDRESS RANGE	VMAP	M0M1MAP	MP/$\overline{MC}$	ENPIE
BROM Vector	ROM Block	0x3FFFC0−0x3FFFFF	1	1	0	0

† On the 28x devices, the VMAP and M0M1MAP modes are set to 1 on reset. The ENPIE mode is forced to 0 on reset.

After the reset and boot is complete, the PIE vector table should be initialized by the user's code. Then the application enables the PIE vector table. From that point on the interrupt vectors are fetched from the PIE vector table. Note: when a reset occurs, the reset vector is always fetched from the vector table as shown in Table 6−3. After a reset the PIE vector table is always disabled.

Figure 6−3 illustrates the process by which the vector table mapping is selected.

Figure 6−3. Reset Flow Diagram



† The compatibility operating mode of the 28xCPU is determined by a combination of the OBJMODE and AMODE bits in Status Register 1 (ST1):

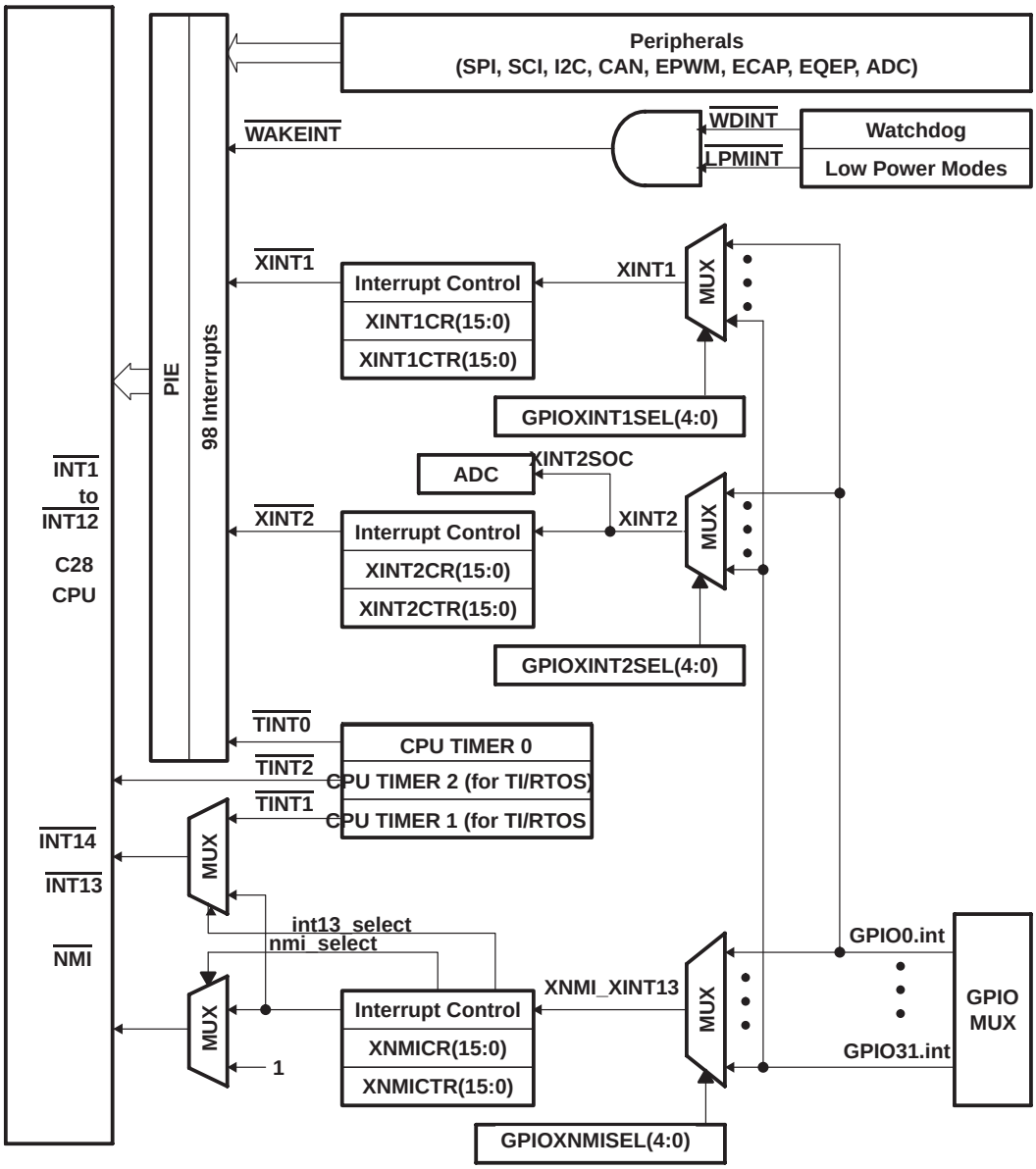
C28x Mode	1	0	
C2xLP Source-Compatible	1	1	
C27x Object-Compatible	0	0	(Default at reset)

‡ The reset vector is always fetched from the BROM.

6.3 Interrupt Sources

Figure 6−4 shows how the various interrupt sources are multiplexed within the 280x devices. This MUXing scheme may not be exactly the same on all 28x devices. See the data sheet of your particular device for details.

Figure 6−4. External and PIE Interrupt Sources



Note: In the GPIO MUX, the XINT1, XINT2 and XNMI signals are synchronized and optionally qualified by a user programmable number of clock cycles. This filters out glitches from the input source. See the GPIO MUX section for more details.

6.3.1 Procedure for Handling Multiplexed Interrupts

The PIE module multiplexes eight peripheral and external pin interrupts into one CPU interrupt. These interrupts are divided into 12 groups: PIE group 1 − PIE group 12. Each group has an associated enable PIEIER and flag PIEIFR register. These registers are used to control the flow of interrupts to the CPU. The PIE module also uses the PIEIER and PIEIFR registers to decode to which interrupt service routine the CPU should branch.

There are three main rules that should be followed when clearing bits within the PIEIFR and the PIEIER registers:

1) **Never clear a PIEIFR bit**. An incoming interrupt may be lost while the read−modify−write operation takes place. To clear a PIEIFR bit, the pending interrupt must be serviced. If you want to clear the PIEIFR bit without executing the normal service routine, then use the following procedure:

Step 1: Set the EALLOW bit to allow modification to the PIE vector table.

Step 2: Modify the PIE vector table so that the vector for the peripheral's service routine points to a temporary ISR. This temporary ISR will only perform a return from interrupt (IRET) operation.

Step 3: Enable the interrupt so that the interrupt will be serviced by the temporary ISR.

Step 4: After the temporary interrupt routine is serviced, the PIEIFR bit will be clear

Step 5: Modify the PIE vector table to re−map the peripheral's service routine to the proper service routine.

Step 6: Clear the EALLOW bit.

The CPU IFR register is integrated within the CPU. Because of this clearing a bit within the CPU IFR register can be done without concern for losing an incoming interrupt.

2) **Software-prioritizing interrupts.** Use the method found in *C28x Peripheral Examples in C* (literature number SPRC097).

   Use the CPU IER register as a global priority and the individual PIEIER registers for group priorities. In this case the PIEIER register is only modified within an interrupt. In addition, only the PIEIER for the same group as the interrupt being serviced is modified. This modification is done while the PIEACK bit holds additional interrupts back from the CPU.

Never disable a PIEIER bit for a group when servicing an interrupt from an unrelated group.

3) **Disabling interrupts using PIEIER**. If the PIEIER registers are used to enable and then later disable an interrupt then the procedure described in Section 6.3.2 must be followed.

6.3.2 Procedures for Enabling And Disabling Multiplexed Peripheral Interrupts

The proper procedure for enabling or disabling an interrupt is by using the peripheral interrupt enable/disable flags. The primary purpose of the PIEIER and CPU IER registers is for software prioritization of interrupts within the same interrupt group. The software *package C28x Peripheral Examples in C* (literature number SPRC097) includes an example showing this method of software prioritizing interrupts. Should bits within the PIEIER registers need to be cleared outside of this context, one of the following two procedures should be followed:

1) **Use the PIEIERx register to disable the interrupt and preserve the associated PIEIFRx flags.**

To clear bits within a PIEIERx register while preserving the associated flags in the PIEIFRx register the following procedure should be followed:

Step 1: Disable global interrupts (INTM = 1)

Step 2: Clear the PIEIERx.y bit to disable the interrupt for a given peripheral. This can be done for one or more peripherals within the same group.

Step 3: Wait 5 cycles. This delay is required to insure that any interrupt that was incoming to the CPU has been flagged within the CPU IFR register.

Step 4: Clear the CPU IFRx bit for the peripheral group. This is a safe operation on the CPU IFR register.

Step 5: Clear the PIEACKx bit for the peripheral group

Step 6: Enable global interrupts (INTM = 0)

2) **Use the PIEIERx register to disable the interrupt and clear the associated PIEIFRx flags.**

   To perform a software reset of a peripheral interrupt and clear the associated flag in the PIEIFRx register and CPU IFR register, then the following procedure should be followed:

Step 1: Disable global interrupts (INTM = 1)

Step 2: Set the EALLOW bit.

Step 3: Modify the PIE vector table to temporarily map the vector of the specific peripheral interrupt to a empty interrupt service routine (ISR). This empty ISR will only perform a return from interrupt (IRET) instruction. This is the safe way to clear a single PIEIFRx.y bit without losing any interrupts from other peripherals within the group.

Step 4: Disable the peripheral interrupt at the peripheral register.

Step 5: Enable global interrupts (INTM = 0).

Step 6: Wait for any pending interrupt from the peripheral to be serviced by the empty ISR routine.

Step 7: Disable global interrupts (INTM = 1).

Step 8: Modify the PIE vector table to map the peripheral vector back to its original ISR.

Step 9: Clear the EALLOW bit.

Step 10: Disable the PIEIER bit for given peripheral.

Step 11: Clear the IFR bit for given peripheral group (this is safe operation on CPU IFR register).

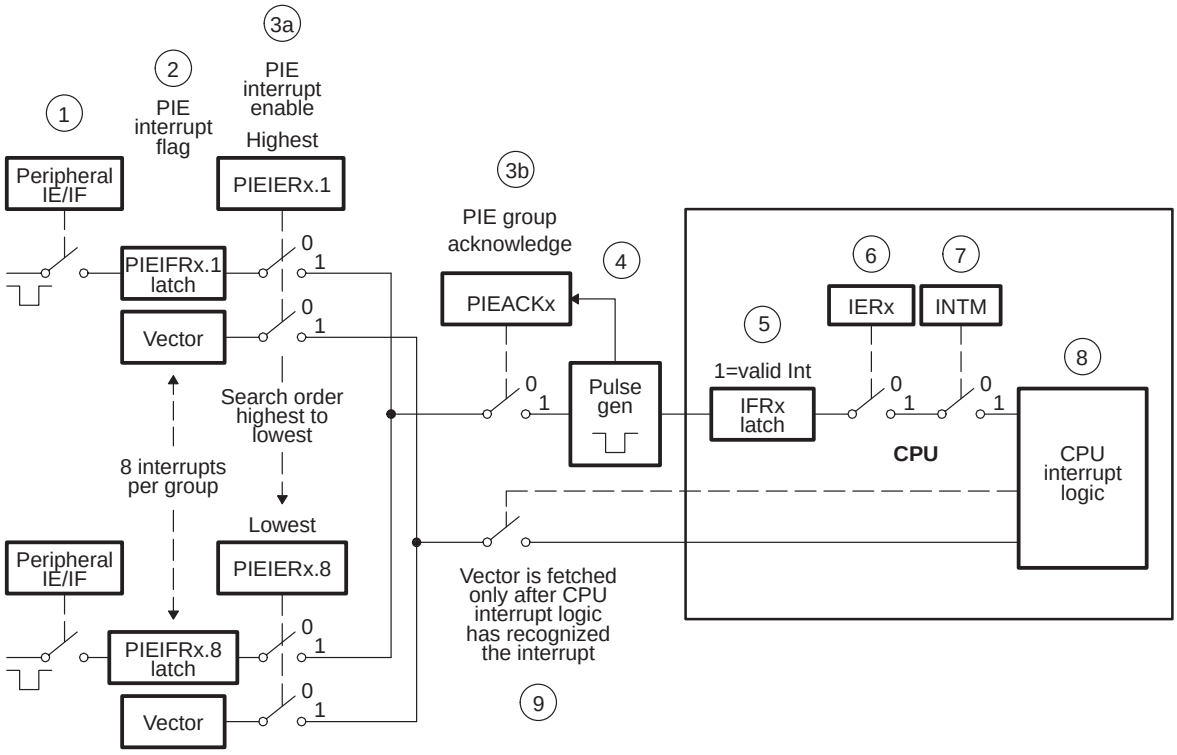
Step 12: Clear the PIEACK bit for the PIE group.

Step 13: Enable global interrupts.

6.3.3 Flow of a Multiplexed Interrupt Request From a Peripheral to the CPU

Figure 6−5 shows the flow with the steps shown in circled numbers. Following the diagram, the steps are described.

Figure 6−5. Multiplexed Interrupt Request Flow Diagram



Step 1: Any peripheral or external interrupt within the PIE group generates an interrupt. If interrupts are enabled within the peripheral module then the interrupt request is sent to the PIE module.

Step 2: The PIE module recognizes that interrupt y within PIE group x (INTx.y) has asserted an interrupt and the appropriate PIE interrupt flag bit is latched: PIEIFRx.y = 1.

Step 3: For the interrupt request to be sent from the PIE to the CPU, both of the following conditions must be true:

a) The proper enable bit must be set (PIEIERx.y = 1) and

b) The PIEACKx bit for the group must be clear.

Step 4: If both conditions in Step 3 are true, then an interrupt request is sent to the CPU and the acknowledge bit is again set (PIEACKx = 1). The PIEACKx bit will remain set until you clear it to indicate that additional interrupts from the group can be sent from the PIE to the CPU.

Step 5: The CPU interrupt flag bit is set (CPU IFRx = 1) to indicate a pending interrupt x at the CPU level.

Step 6: If the CPU interrupt is enabled (CPU IER bit x = 1, or DBGIER bit x = 1) AND (7) the global interrupt mask is clear (INTM = 0) then the CPU will service the INTx.

Step 7: The CPU recognizes the interrupt and performs the automatic context save, clears the IER bit, sets INTM, and clears EALLOW. All of the steps that the CPU takes in order to prepare to service the interrupt are documented in the *TMS320C28x DSP CPU and Instruction Set Reference Guide* (literature number SPRU430).

Step 8: The CPU will then request the appropriate vector from the PIE.

Step 9: For multiplexed interrupts, the PIE module uses the current value in the PIEIERx and PIEIFRx registers to decode which vector address should be used.

There are two possible cases:

- The vector for the highest priority interrupt within the group that is both a) enabled in the PIEIERx register, and b) flagged as pending in the PIEIFRx is fetched and used as the branch address. In this manner if an even higher priority enabled interrupt was flagged after Step 4**,** it will be serviced first.
- If no flagged interrupts within the group are enabled, then the PIE will respond with the vector for the highest priority interrupt within that group. That is the branch address used for INTx.1. This behavior corresponds to the 28x TRAP or INT instructions.

Note:

Because the PIEIERx register is used to determine which vector will be used for the branch, you must take care when clearing bits within the PIEIERx register. The proper procedure for clearing bits within a PIEIERx register is described in Section 6.3.2. Failure to follow these steps can result in changes occurring to the PIEIERx register after an interrupt has been passed to the CPU at point (5) in Figure 6−5. In this case the PIE will respond as if a TRAP or INT instruction was executed unless there are other interrupts both pending and enabled.

At this point, the PIEIFRx.y bit is cleared and the CPU branches to the vector of the interrupt fetched from the PIE.

6.3.4 The PIE Vector Table

The PIE vector table (see Table 6−4) consists of a 256 x 16 SARAM block that can also be used as RAM (in data space only) if the PIE block is not in use. The PIE vector table contents are undefined on reset. The CPU fixes interrupt priority for INT1 to INT12. The PIE controls priority for each group of eight interrupts. For example, if INT1.1 should occur simultaneously with INT8.1, both interrupts are presented to the CPU simultaneously by the PIE block, and the CPU services INT1.1 first. If INT1.1 should occur simultaneously with INT1.8, then INT1.1 is sent to the CPU first and then INT1.8 follows. Interrupt prioritization is performed during the vector fetch portion of the interrupt processing.

A TRAP 1 to TRAP 12 instruction or an INTR INT1 to INTR INT12 instruction fetches the vector from the first location of each group (INTR1.1 to INT12.1). Similarly an OR IFR,#16-bit operation causes the vector to be fetched from INTR1.1 to INTR12.1 locations if the respective interrupt flag is set. All other TRAP, INTR, OR IFR,#16-bit operations fetch the vector from the respective table location. You should avoid using such operations for INTR1 to INTR12. The TRAP #0 operation returns a vector value of 0x000000 The vector table is EALLOW protected.

Table 6−4. 280x PIE Vector Table

Name	VECTOR ID	Address	Size (x16)	Description	CPU Priority	Pie Group Priority
Reset	0	0x0000 0D00	2	Reset is always fetched from location 0x003F FFC0 in Boot ROM.	1 (highest)	−
INT1	1	0x0000 0D02	2	Not used. See PIE Group 1	5	−
INT2	2	0x0000 0D04	2	Not used. See PIE Group 2	6	−
INT3	3	0x0000 0D06	2	Not used. See PIE Group 3	7	−
INT4	4	0x0000 0D08	2	Not used. See PIE Group 4	8	−
INT5	5	0x0000 0D0A	2	Not used. See PIE Group 5	9	−
INT6	6	0x0000 0D0C	2	Not used. See PIE Group 6	10	−
INT7	7	0x0000 0D0E	2	Not used. See PIE Group 7	11	−
INT8	8	0x0000 0D10	2	Not used. See PIE Group 8	12	−
INT9	9	0x0000 0D12	2	Not used. See PIE Group 9	13	−
INT10	10	0x0000 0D14	2	Not used. See PIE Group 10	14	−
INT11	11	0x0000 0D16	2	Not used. See PIE Group 11	15	−
INT12	12	0x0000 0D18	2	Not used. See PIE Group 12	16	−
INT13	13	0x0000 0D1A	2	External Interrupt 13 (XINT13) or CPU−Timer1 (for TI/RTOS use)	17	−
INT14	14	0x0000 0D1C	2	CPU−Timer2 (for TI/RTOS use)	18	−
DATALOG	15	0x0000 0D1E	2	CPU Data Logging Interrupt	19 (lowest)	−
RTOSINT	16	0x0000 0D20	2	CPU Real−Time OS Interrupt	4	−
EMUINT	17	0x0000 0D22	2	CPU Emulation Interrupt	2	−
NMI	18	0x0000 0D24	2	External Non−Maskable Interrupt	3	−
ILLEGAL	19	0x0000 0D26	2	Illegal Operation	−	−

Notes: 1) All the locations within the PIE vector table are EALLOW protected.
2) The VECTOR ID is used by DSP/BIOS.
3) Reset is always fetched from location 0x003F FFC0 in Boot ROM.

Table 6−4. 280x PIE Vector Table (Continued)

Name	VECTOR ID	Address	Size (x16)	Description		CPU Priority	Pie Group Priority
USER0	20	0x0000 0D28	2	User−Defined Trap		−	−
USER1	21	0x0000 0D2A	2	User Defined Trap		−	−
USER2	22	0x0000 0D2C	2	User Defined Trap		−	−
USER3	23	0x0000 0D2E	2	User Defined Trap		−	−
USER4	24	0x0000 0D30	2	User Defined Trap		−	−
USER5	25	0x0000 0D32	2	User Defined Trap		−	−
USER6	26	0x0000 0D34	2	User Defined Trap		−	−
USER7	27	0x0000 0D36	2	User Defined Trap		−	−
USER8	28	0x0000 0D38	2	User Defined Trap		−	−
USER9	29	0x0000 0D3A	2	User Defined Trap		−	−
USER10	30	0x0000 0D3C	2	User Defined Trap		−	−
USER11	31	0x0000 0D3E	2	User Defined Trap		−	−
PIE Group 1 Vectors – MUXed into CPU INT1							
INT1.1	32	0x0000 0D40	2	SEQ1INT	(ADC)	5	1 (highest)
INT1.2	33	0x0000 0D42	2	SEQ2INT	(ADC)	5	2
INT1.3	34	0x0000 0D44	2	reserved		5	3
INT1.4	35	0x0000 0D46	2	XINT1		5	4
INT1.5	36	0x0000 0D48	2	XINT2		5	5
INT1.6	37	0x0000 0D4A	2	ADCINT	(ADC)	5	6
INT1.7	38	0x0000 0D4C	2	TINT0	(CPU−Timer0)	5	7
INT1.8	39	0x0000 0D4E	2	WAKEINT	(LPM/WD)	5	8 (lowest)
PIE Group 2 Vectors − MUXed into CPU INT2							
INT2.1	40	0x0000 0D50	2	EPWM1_TZINT	(EPWM1)	6	1 (highest)

Notes: 1) All the locations within the PIE vector table are EALLOW protected.
2) The VECTOR ID is used by DSP/BIOS.
3) Reset is always fetched from location 0x003F FFC0 in Boot ROM.

Table 6−4. 280x PIE Vector Table (Continued)

Name	VECTOR ID	Address	Size (x16)	Description		CPU Priority	Pie Group Priority
INT2.2	41	0x0000 0D52	2	EPWM2_TZINT	(EPWM2)	6	2
INT2.3	42	0x0000 0D54	2	EPWM3_TZINT	(EPWM3)	6	3
INT2.4	43	0x0000 0D56	2	EPWM4_TZINT	(EPWM4)	6	4
INT2.5	44	0x0000 0D58	2	EPWM5_TZINT	(EPWM5)	6	5
INT2.6	45	0x0000 0D5A	2	EPWM6_TZINT	(EPWM6)	6	6
INT2.7	46	0x0000 0D5C	2	Reserved		6	7
INT2.8	47	0x0000 0D5E	2	Reserved		6	8 (lowest)
PIE Group 3 Vectors − MUXed into CPU INT3							
INT3.1	48	0x0000 0D60	2	EPWM1_INT	(EPWM1)	7	1 (highest)
INT3.2	49	0x0000 0D62	2	EPWM2_INT	(EPWM2)	7	2
INT3.3	50	0x0000 0D64	2	EPWM3_INT	(EPWM3)	7	3
INT3.4	51	0x0000 0D66	2	EPWM4_INT	(EPWM4)	7	4
INT3.5	52	0x0000 0D68	2	EPWM5_INT	(EPWM5)	7	5
INT3.6	53	0x0000 0D6A	2	EPWM6_INT	(EPWM6)	7	6
INT3.7	54	0x0000 0D6C	2	reserved		7	7
INT3.8	55	0x0000 0D6E	2	reserved		7	8 (lowest)
PIE Group 4 Vectors − MUXed into CPU INT4							
INT4.1	56	0x0000 0D70	2	ECAP1_INT	(ECAP1)	8	1 (highest)
INT4.2	57	0x0000 0D72	2	ECAP2_INT	(ECAP2)	8	2
INT4.3	58	0x0000 0D74	2	ECAP3_INT	(ECAP3)	8	3
INT4.4	59	0x0000 0D76	2	ECAP4_INT	(ECAP4)	8	4
INT4.5	60	0x0000 0D78	2	Reserved		8	5
INT4.6	61	0x0000 0D7A	2	Reserved		8	6

Notes: 1) All the locations within the PIE vector table are EALLOW protected.
2) The VECTOR ID is used by DSP/BIOS.
3) Reset is always fetched from location 0x003F FFC0 in Boot ROM.

Table 6−4. 280x PIE Vector Table (Continued)

Name	VECTOR ID	Address	Size (x16)	Description		CPU Priority	Pie Group Priority
INT4.7	62	0x0000 0D7C	2	Reserved		8	7
INT4.8	63	0x0000 0D7E	2	Reserved		8	8 (lowest)
PIE Group 5 Vectors − MUXed into CPU INT5							
INT5.1	64	0x0000 0D80	2	EQEP1_INT	(EQEP1)	9	1 (highest)
INT5.2	65	0x0000 0D82	2	EQEP1_INT	(EQEP2)	9	2
INT5.3	66	0x0000 0D84	2	Reserved		9	3
INT5.4	67	0x0000 0D86	2	Reserved		9	4
INT5.5	68	0x0000 0D88	2	Reserved		9	5
INT5.6	69	0x0000 0D8A	2	Reserved		9	6
INT5.7	70	0x0000 0D8C	2	Reserved		9	7
INT5.8	71	0x0000 0D8E	2	Reserved		9	8 (lowest)
PIE Group 6 Vectors − MUXed into CPU INT6							
INT6.1	72	0x0000 0D90	2	SPIRXINTA	(SPI−A)	10	1 (highest)
INT6.2	73	0x0000 0D92	2	SPITXINTA	(SPI−A)	10	2
INT6.3	74	0x0000 0D94	2	SPIRXINTB	(SPI−B)	10	3
INT6.4	75	0x0000 0D96	2	SPITXINTB	(SPI−B)	10	4
INT6.5	76	0x0000 0D98	2	SPIRXINTC	(SPI−C)	10	5
INT6.6	77	0x0000 0D9A	2	SPITXINTC	(SPI−C)	10	6
INT6.7	78	0x0000 0D9C	2	SPIRXINTD	(SPI−D)	10	7
INT6.8	79	0x0000 0D9E	2	SPITXINTD	(SPI−D)	10	8 (lowest)
PIE Group 7 Vectors − MUXed into CPU INT7							
INT7.1	80	0x0000 0DA0	2	Reserved		11	1 (highest)
INT7.2	81	0x0000 0DA2	2	Reserved		11	2

Notes: 1) All the locations within the PIE vector table are EALLOW protected.
2) The VECTOR ID is used by DSP/BIOS.
3) Reset is always fetched from location 0x003F FFC0 in Boot ROM.

Table 6−4. 280x PIE Vector Table (Continued)

Name	VECTOR ID	Address	Size (x16)	Description		CPU Priority	Pie Group Priority
INT7.3	82	0x0000 0DA4	2	Reserved		11	3
INT7.4	83	0x0000 0DA6	2	Reserved		11	4
INT7.5	84	0x0000 0DA8	2	Reserved		11	5
INT7.6	85	0x0000 0DAA	2	Reserved		11	6
INT7.7	86	0x0000 0DAC	2	Reserved		11	7
INT7.8	87	0x0000 0DAE	2	Reserved		11	8 (lowest)
PIE Group 8 Vectors − MUXed into CPU INT8							
INT8.1	88	0x0000 0DB0	2	I2CINT1A	I2C−A	12	1 (highest)
INT8.2	89	0x0000 0DB2	2	I2CINT2A	I2C−A	12	2
INT8.3	90	0x0000 0DB4	2	Reserved		12	3
INT8.4	91	0x0000 0DB6	2	Reserved		12	4
INT8.5	92	0x0000 0DB8	2	Reserved		12	5
INT8.6	93	0x0000 0DBA	2	Reserved		12	6
INT8.7	94	0x0000 0DBC	2	Reserved		12	7
INT8.8	95	0x0000 0DBE	2	Reserved		12	8 (lowest)
PIE Group 9 Vectors − MUXed into CPU INT9							
INT9.1	96	0x0000 0DC0	2	SCIRXINTA	(SCI−A)	13	1 (highest)
INT9.2	97	0x0000 0DC2	2	SCITXINTA	(SCI−A)	13	2
INT9.3	98	0x0000 0DC4	2	SCIRXINTB	(SCI−B)	13	3
INT9.4	99	0x0000 0DC6	2	SCITXINTB	(SCI−B)	13	4
INT9.5	100	0x0000 0DC8	2	ECAN0INTA	(eCAN−A)	13	5
INT9.6	101	0x0000 0DCA	2	ECAN1INTA	(eCAN−A)	13	6
INT9.7	102	0x0000 0DCC	2	ECAN0INTA	(eCAN−B)	13	7

Notes: 1) All the locations within the PIE vector table are EALLOW protected.
2) The VECTOR ID is used by DSP/BIOS.
3) Reset is always fetched from location 0x003F FFC0 in Boot ROM.

Table 6−4. 280x PIE Vector Table (Continued)

Name	VECTOR ID	Address	Size (x16)	Description		CPU Priority	Pie Group Priority
INT9.8	103	0x0000 0DCE	2	ECAN1INTA	(eCAN−B)	13	8 (lowest)
PIE Group 10 Vectors − MUXed into CPU INT10							
INT10.1	104	0x0000 0DD0	2	Reserved		14	1 (highest)
INT10.2	105	0x0000 0DD2	2	Reserved		14	2
INT10.3	106	0x0000 0DD4	2	Reserved		14	3
INT10.4	107	0x0000 0DD6	2	Reserved		14	4
INT10.5	108	0x0000 0DD8	2	Reserved		14	5
INT10.6	109	0x0000 0DDA	2	Reserved		14	6
INT10.7	110	0x0000 0DDC	2	Reserved		14	7
INT10.8	111	0x0000 0DDE	2	Reserved		14	8 (lowest)
PIE Group 11 Vectors − MUXed into CPU INT11							
INT11.1	112	0x0000 0DE0	2	Reserved		15	1 (highest)
INT11.2	113	0x0000 0DE2	2	Reserved		15	2
INT11.3	114	0x0000 0DE4	2	Reserved		15	3
INT11.4	115	0x0000 0DE6	2	Reserved		15	4
INT11.5	116	0x0000 0DE8	2	Reserved		15	5
INT11.6	117	0x0000 0DEA	2	Reserved		15	6
INT11.7	118	0x0000 0DEC	2	Reserved		15	7
INT11.8	119	0x0000 0DEE	2	Reserved		15	8 (lowest)
PIE Group 12 Vectors − Muxed into CPU INT12							
INT12.1	120	0x0000 0DF0	2	Reserved		16	1 (highest)
INT12.2	121	0x0000 0DF2	2	Reserved		16	2
INT12.3	122	0x0000 0DF4	2	Reserved		16	3

Notes: 1) All the locations within the PIE vector table are EALLOW protected.
2) The VECTOR ID is used by DSP/BIOS.
3) Reset is always fetched from location 0x003F FFC0 in Boot ROM.

Table 6−4. 280x PIE Vector Table (Continued)

Name	VECTOR ID	Address	Size (x16)	Description	CPU Priority	Pie Group Priority
INT12.4	123	0x0000 0DF6	2	Reserved	16	4
INT12.5	124	0x0000 0DF8	2	Reserved	16	5
INT12.6	125	0x0000 0DFA	2	Reserved	16	6
INT12.7	126	0x0000 0DFC	2	Reserved	16	7
INT12.8	127	0x0000 0DFE	2	Reserved	16	8 (lowest)

Notes: 1) All the locations within the PIE vector table are EALLOW protected.
2) The VECTOR ID is used by DSP/BIOS.
3) Reset is always fetched from location 0x003F FFC0 in Boot ROM.

The interrupt grouping for peripherals and external interrupts connected to the PIE module is shown in Table 6−5. Each row in the table shows the 8 interrupts multiplexed into a particular CPU interrupt.

Table 6−5. 280x PIE Peripheral Interrupts(A)

	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1.y	WAKEINT (LPM/WD)	TINT0 (TIMER 0)	ADCINT (ADC)	XINT2	XINT1	Spare	SEQ2INT (ADC)	SEQ1INT (ADC)
INT2.y	Reserved	Reserved	EPWM6_ TZINT (EPWM6)	EPWM5_ TZINT (EPWM5)	EPWM4_ TZINT (EPWM4)	EPWM3_ TZINT (EPWM3)	EPWM2_ TZINT (EPWM2)	EPWM1_ TZINT (EPWM1)
INT3.y	Reserved	Reserved	EPWM6_INT (EPWM6)	EPWM5_INT (EPWM5)	EPWM4_INT (EPWM4)	EPWM3_INT (EPWM3)	EPWM2_INT (EPWM2)	EPWM1_INT (EPWM1)
INT4.y	Reserved	Reserved	Reserved	Reserved	ECAP4_INT (ECAP4)	ECAP3_INT (ECAP3)	ECAP2_INT (ECAP2)	ECAP1_INT (ECAP1)
INT5.y	Spare	Reserved	Reserved	Reserved	Reserved	Reserved	EQEP2_INT (EQEP2)	EQEP1_INT (EQEP1)
INT6.y	SPITXINTD (SPI-D)	SPIRXINTD (SPI-D)	SPITXINTC (SPI-C)	SPIRXINTC (SPI-C)	SPITXINTB (SPI-B)	SPIRXINTB (SPI-B)	SPITXINTA (SPI-A)	SPIRXINTA (SPI-A)
INT7.y	Spare 0x0DAE	Spare	Spare	Spare	Spare	Spare	Spare	Spare 0x0DA0
INT8.y	Spare 0x0DBE	Spare	Spare	Spare	Spare	Spare	I2CINT1A (I2C−A)	I2CINT2A (I2C−A)
INT9.y	ECAN1INTB (CAN−B)	ECAN0INTB (CAN−B)	ECAN1INTA (CAN−A)	ECAN0INTA (CAN−A)	SCITXINTB (SCI−B)	SCIRXINTB (SCI−B)	SCITXINTA (SCI−A)	SCIRXINTA (SCI−A)
INT10.y	Spare	Spare	Spare	Spare	Spare	Spare	Spare	Spare
INT11.y	Spare 0x0DEE	Spare	Spare	Spare	Spare	Spare	Spare	Spare 0x0DE0
INT12.y	spare 0x0DFE	Spare	Spare	Spare	Spare	Spare	Spare	Spare 0x0DF0

Note: Reserved locations are for future devices; however, these interrupts can be used as software interrupts if they are enabled at the PIEIFRx level.

6.4 PIE Configuration Registers

The registers controlling the functionality of the PIE block are shown in Table 6−6.

Table 6−6. PIE Configuration and Control Registers

Name	Address	Size (x16)	Description
PIECTRL	0x0000−0CE0	1	PIE, Control Register
PIEACK	0x0000−0CE1	1	PIE, Acknowledge Register
PIEIER1	0x0000−0CE2	1	PIE, INT1 Group Enable Register
PIEIFR1	0x0000−0CE3	1	PIE, INT1 Group Flag Register
PIEIER2	0x0000−0CE4	1	PIE, INT2 Group Enable Register
PIEIFR2	0x0000−0CE5	1	PIE, INT2 Group Flag Register
PIEIER3	0x0000−0CE6	1	PIE, INT3 Group Enable Register
PIEIFR3	0x0000−0CE7	1	PIE, INT3 Group Flag Register
PIEIER4	0x0000−0CE8	1	PIE, INT4 Group Enable Register
PIEIFR4	0x0000−0CE9	1	PIE, INT4 Group Flag Register
PIEIER5	0x0000−0CEA	1	PIE, INT5 Group Enable Register
PIEIFR5	0x0000−0CEB	1	PIE, INT5 Group Flag Register
PIEIER6	0x0000−0CEC	1	PIE, INT6 Group Enable Register
PIEIFR6	0x0000−0CED	1	PIE, INT6 Group Flag Register
PIEIER7	0x0000−0CEE	1	PIE, INT7 Group Enable Register
PIEIFR7	0x0000−0CEF	1	PIE, INT7 Group Flag Register
PIEIER8	0x0000−0CF0	1	PIE, INT8 Group Enable Register
PIEIFR8	0x0000−0CF1	1	PIE, INT8 Group Flag Register
PIEIER9	0x0000−0CF2	1	PIE, INT9 Group Enable Register
PIEIFR9	0x0000−0CF3	1	PIE, INT9 Group Flag Register
PIEIER10	0x0000−0CF4	1	PIE, INT10 Group Enable Register
PIEIFR10	0x0000−0CF5	1	PIE, INT10 Group Flag Register
PIEIER11	0x0000−0CF6	1	PIE, INT11 Group Enable Register

Note: The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

Table 6−6. PIE Configuration and Control Registers (Continued)

Name	Address	Size (x16)	Description
PIEIFR11	0x0000−0CF7	1	PIE, INT11 Group Flag Register
PIEIER12	0x0000−0CF8	1	PIE, INT12 Group Enable Register
PIEIFR12	0x0000−0CF9	1	PIE, INT12 Group Flag Register
Reserved	0x0000−0CFA 0x0000−0CFF	6	Reserved

Note: The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

6.5 PIE Interrupt Registers

Table 6−7. PIECTRL Register-Address CE0

15	1	0
PIEVECT		ENPIE
R-0		R/W-0

Legend: R = Read access, W = write access, -0 = value after reset

Table 6−8. PIECTRL Bit Descriptions

Bits	Field	Description
15−1	PIEVECT	These bits indicate the address within the PIE vector table from which the vector was fetched. The least significant bit of the address is ignored and only bits 1 to 15 of the address is shown. You can read the vector value to determine which interrupt generated the vector fetch. **Example** `If PIECTRL = 0x0d27` then the vector from address 0x0D26 (illegal operation) was fetched.
0	ENPIE	Enable vector fetching from PIE block. When ENPIE is set to 1, all vectors are fetched from the PIE vector table. If this bit is set to 0, the PIE block is disabled and vectors are fetched from the CPU vector table in boot ROM or external interface Zone 7. All PIE block registers (PIEACK, PIEIFR, PIEIER) can be accessed even when the PIE block is disabled. **Note:** The reset vector is never fetched from the PIE, even when it is enabled. This vector is always fetched from boot ROM or XINTF Zone 7 depending on the state of the XMPNMC input signal.

Figure 6−6. PIE Interrupt Acknowledge Register (PIEACKx) Register-Address CE1

15	12	11	0
Reserved		PIEACK	
R-0		R/W1C-1	

Legend: R = Read access, W1C = write1 to clear, -0 = value after reset

Table 6−9. PIEACKx Bit Descriptions

Bits	Field	Description
15−12	Reserved	
11−0	PIEACK	Writing a 1 to the respective interrupt bit enables the PIE block to drive a pulse into the core interrupts input, if an interrupt is pending on any of the group interrupts. Reading this register indicates if an interrupt is pending in the respective group. Bit 0 refers to INT1 up to Bit 11, which refers to INT12. Note: Writes of 0 are ignored.

6.5.1 PIE Interrupt Flag Registers

There are twelve PIEIFR registers, one for each CPU interrupt used by the PIE module (INT1−INT12).

Figure 6−7. PIEIFRx Register (x = 1 to 12)

15							8
Reserved							
R-0							

7	6	5	4	3	2	1	0
INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 6−10. PIEIFRx Bit Descriptions

Bits	Field	Description
15−8	Reserved	
7	INTx.8	These register bits indicate if an interrupt is currently active. They behave very much like the CPU interrupt flag register. When an interrupt is active, the respective register bit is set. The bit is cleared when the interrupt is serviced or by writing a 0 to the register bit. This register can also be read to determine which interrupts are active or pending. x = 1 to 12. INTx means CPU INT1 to INT12
6	INTx.7	
5	INTx.6	
4	INTx.5	
3	INTx.4	
2	INTx.3	
1	INTx.2	
0	INTx.1	

Notes: 1) All of the above registers reset values are set by reset.
2) Hardware has priority over CPU accesses to the PIEIFR registers.
3) The PIEIFR register bit is cleared during the interrupt vector fetch portion of the interrupt processing.

Note:

Never clear a PIEIFR bit. An interrupt may be lost during the read-modify-write operation. See Section 6.3.1 for a method to clear flagged interrupts.

6.5.2 PIE Interrupt Enable Registers

There are twelve PIEIER registers, one for each CPU interrupt used by the PIE module (INT1−INT12).

Figure 6−8. PIEIERx Register (x = 1 to 12)

15							8
Reserved							
R-0							

7	6	5	4	3	2	1	0
INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 6−11. PIEIERx Bit Descriptions

Bits	Field	Description
15−8	Reserved	
7	INTx.8	These register bits individually enable an interrupt within a group and behave very much like the core interrupt enable register. Setting a bit to 1 enables the servicing of the respective interrupt. Setting a bit to 0 disables the servicing of the interrupt.
6	INTx.7	
5	INTx.6	x = 1 to 12. INTx means CPU INT1 to INT12
4	INTx.5	
3	INTx.4	
2	INTx.3	
1	INTx.2	
0	INTx.1	

Note: All of the above registers reset values are set by reset.

Note:

Care must be taken when clearing PIEIER bits during normal operation. See Section 6.3.2 for the proper procedure for handling these bits.

6.5.3 CPU Interrupt Flag Register (IFR)

The CPU interrupt flag register (IFR), is a 16-bit, CPU register and is used to identify and clear pending interrupts. The IFR contains flag bits for all the maskable interrupts at the CPU level (INT1−INT14, DLOGINT and RTOSINT). When the PIE is enabled, the PIE module multiplexes interrupt sources for INT1−INT12.

When a maskable interrupt is requested, the flag bit in the corresponding peripheral control register is set to 1. If the corresponding mask bit is also 1, the interrupt request is sent to the CPU, setting the corresponding flag in the IFR. This indicates that the interrupt is pending or waiting for acknowledgement.

To identify pending interrupts, use the PUSH IFR instruction and then test the value on the stack. Use the OR IFR instruction to set IFR bits and use the AND IFR instruction to manually clear pending interrupts. All pending interrupts are cleared with the AND IFR #0 instruction or by a hardware reset.

The following events also clear an IFR flag:

- The CPU acknowledges the interrupt.
- The 28x device is reset.

Notes:

1) To clear an IFR bit, you must write a zero to it, not a one.

2) When a maskable interrupt is acknowledged, *only* the IFR bit is cleared automatically. The flag bit in the corresponding peripheral control register is *not* cleared. If an application requires that the control register flag be cleared, the bit must be cleared by software.

3) When an interrupt is requested by an INTR instruction and the corresponding IFR bit is set, the CPU does not clear the bit automatically. If an application requires that the IFR bit be cleared, the bit must be cleared by software.

4) IMR and IFR registers pertain to core-level interrupts. All peripherals have their own interrupt mask and flag bits in their respective control/configuration registers. Note that several peripheral interrupts are grouped under one core-level interrupt.

Figure 6−9. Interrupt Flag Register (IFR) — CPU Register

15	14	13	12	11	10	9	8
RTOSINT	DLOGINT	INT14	INT13	INT12	INT11	INT10	INT9
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Note: R = Read access, W = Write access, –0 = value after reset

Table 6−12. IFR Bit Descriptions

Bits	Field	Description
15	RTOSINT	Real-time operating system flag. RTOSINT is the flag for RTOS interrupts. 0 No RTOS interrupt is pending 1 At least one RTOS interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
14	DLOGINT	Data logging interrupt fag. DLOGINT is the flag for data logging interrupts. 0 No DLOGINT is pending 1 At least one DLOGINT interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
13	INT14	Interrupt 14 flag. INT14 is the flag for interrupts connected to CPU interrupt level INT14. 0 No INT14 interrupt is pending 1 At least one INT14 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
12	INT13	Interrupt 13 flag. INT13 is the flag for interrupts connected to CPU interrupt level INT13. 0 No INT13 interrupt is pending 1 At least one INT13 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request

Table 6−12. IFR Bit Descriptions (continued)

Bits	Field	Description
11	INT12	Interrupt 12 flag. INT12 is the flag for interrupts connected to CPU interrupt level INT12. 0 No INT12 interrupt is pending 1 At least one INT12 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
10	INT11	Interrupt 11 flag. INT11 is the flag for interrupts connected to CPU interrupt level INT11. 0 No INT11 interrupt is pending 1 At least one INT11 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
9	INT10	Interrupt 10 flag. INT10 is the flag for interrupts connected to CPU interrupt level INT10. 0 No INT10 interrupt is pending 1 At least one INT6 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
8	INT9	Interrupt 9 flag. INT9 is the flag for interrupts connected to CPU interrupt level INT6. 0 No INT9 interrupt is pending 1 At least one INT9 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
7	INT8	Interrupt 8 flag. INT8 is the flag for interrupts connected to CPU interrupt level INT6. 0 No INT8 interrupt is pending 1 At least one INT8 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
6	INT7	Interrupt 7 flag. INT7 is the flag for interrupts connected to CPU interrupt level INT7. 0 No INT7 interrupt is pending 1 At least one INT7 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request

Table 6−12. IFR Bit Descriptions (continued)

Bits	Field	Description
5	INT6	Interrupt 6 flag. INT6 is the flag for interrupts connected to CPU interrupt level INT6. 0 No INT6 interrupt is pending 1 At least one INT6 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
4	INT5	Interrupt 5 flag. INT5 is the flag for interrupts connected to CPU interrupt level INT5. 0 No INT5 interrupt is pending 1 At least one INT5 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
3	INT4	Interrupt 4 flag. INT4 is the flag for interrupts connected to CPU interrupt level INT4. 0 No INT4 interrupt is pending 1 At least one INT4 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
2	INT3	Interrupt 3 flag. INT3 is the flag for interrupts connected to CPU interrupt level INT3. 0 No INT3 interrupt is pending 1 At least one INT3 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
1	INT2	Interrupt 2 flag. INT2 is the flag for interrupts connected to CPU interrupt level INT2. 0 No INT2 interrupt is pending 1 At least one INT2 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request
0	INT1	Interrupt 1 flag. INT1 is the flag for interrupts connected to CPU interrupt level INT1. 0 No INT1 interrupt is pending 1 At least one INT1 interrupt is pending. Write a 0 to this bit to clear it to 0 and clear the interrupt request

6.5.4 Interrupt Enable Register (IER) and Debug Interrupt Enable Register (DBGIER)

The IER is a 16-bit CPU register. The IER contains enable bits for all the maskable CPU interrupt levels (INT1−INT14, RTOSINT and DLOGINT). Neither NMI nor XRS is included in the IER; thus, IER has no effect on these interrupts.

You can read the IER to identify enabled or disabled interrupt levels, and you can write to the IER to enable or disable interrupt levels. To enable an interrupt level, set its corresponding IER bit to one using the OR IER instruction. To disable an interrupt level, set its corresponding IER bit to zero using the AND IER instruction. When an interrupt is disabled, it is not acknowledged, regardless of the value of the INTM bit. When an interrupt is enabled, it is acknowledged if the corresponding IFR bit is one and the INTM bit is zero.

When using the OR IER and AND IER instructions to modify IER bits make sure they do not modify the state of bit 15 (RTOSINT) unless a real-time operating system is present.

When a hardware interrupt is serviced or an INTR instruction is executed, the corresponding IER bit is cleared automatically. When an interrupt is requested by the TRAP instruction the IER bit is not cleared automatically. In the case of the TRAP instruction if the bit needs to be cleared it must be done by the interrupt service routine.

At reset, all the IER bits are cleared to 0, disabling all maskable CPU level interrupts.

The IER register is shown in Figure 6−10, and descriptions of the bits follow the figure.

Figure 6−10. Interrupt Enable Register (IER) — CPU Register

15	14	13	12	11	10	9	8
RTOSINT	DLOGINT	INT14	INT13	INT12	INT11	INT10	INT9
R/W-0	R/W–0	R/W–0	R/W–0	R/W–0	R/W–0	R/W–0	R/W–0

7	6	5	4	3	2	1	0
INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1
R/W-0	R/W–0	R/W–0	R/W–0	R/W–0	R/W–0	R/W–0	R/W–0

Note: R = Read access, W = Write access, –0 = value after reset

Table 6−13. IER Bit Descriptions

Bits	Field	Description
15	RTOSINT	Real-time operating system interrupt enable. RTOSINT enables or disables the CPU RTOS interrupt. 0 Level INT6 is disabled 1 Level INT6 is enabled
14	DLOGINT	Data logging interrupt enable. DLOGINT enables or disables the CPU data logging interrupt. 0 Level INT6 is disabled 1 Level INT6 is enabled
13	INT14	Interrupt 14 enable. INT14 enables or disables CPU interrupt level INT14. 0 Level INT14 is disabled 1 Level INT14 is enabled
12	INT13	Interrupt 13 enable. INT13 enables or disables CPU interrupt level INT13. 0 Level INT13 is disabled 1 Level INT13 is enabled
11	INT12	Interrupt 12 enable. INT12 enables or disables CPU interrupt level INT12. 0 Level INT12 is disabled 1 Level INT12 is enabled
10	INT11	Interrupt 11 enable. INT11 enables or disables CPU interrupt level INT11. 0 Level INT11 is disabled 1 Level INT11 is enabled
9	INT10	Interrupt 10 enable. INT10 enables or disables CPU interrupt level INT10. 0 Level INT10 is disabled 1 Level INT10 is enabled
8	INT9	Interrupt 9 enable. INT9 enables or disables CPU interrupt level INT9. 0 Level INT9 is disabled 1 Level INT9 is enabled

Table 6−13. IER Bit Descriptions (continued)

Bits	Field	Description
7	INT8	Interrupt 8 enable. INT8 enables or disables CPU interrupt level INT8. 0 Level INT8 is disabled 1 Level INT8 is enabled
6	INT7	Interrupt 7 enable. INT7 enables or disables CPU interrupt level INT7. 0 Level INT7 is disabled 1 Level INT7 is enabled
5	INT6	Interrupt 6 enable. INT6 enables or disables CPU interrupt level INT6. 0 Level INT6 is disabled 1 Level INT6 is enabled
4	INT5	Interrupt 5 enable. INT5 enables or disables CPU interrupt level INT5. 0 Level INT5 is disabled 1 Level INT5 is enabled
3	INT4	Interrupt 4 enable. INT4 enables or disables CPU interrupt level INT4. 0 Level INT4 is disabled 1 Level INT4 is enabled
2	INT3	Interrupt 3 enable. INT3 enables or disables CPU interrupt level INT3. 0 Level INT3 is disabled 1 Level INT3 is enabled
1	INT2	Interrupt 2 enable. INT2 enables or disables CPU interrupt level INT2. 0 Level INT2 is disabled 1 Level INT2 is enabled
0	INT1	Interrupt 1 enable. INT1 enables or disables CPU interrupt level INT1. 0 Level INT1 is disabled 1 Level INT1 is enabled

The Debug Interrupt Enable Register (DBGIER) is used only when the CPU is halted in real-time emulation mode. An interrupt enabled in the DBGIER is defined as a time-critical interrupt. When the CPU is halted in real-time mode, the only interrupts that are serviced are time-critical interrupts that are also enabled in the IER. If the CPU is running in real-time emulation mode, the standard interrupt-handling process is used and the DEBIER is ignored.

As with the IER, you can read the DBGIER to identify enabled or disabled interrupts and write to the DBGIER to enable or disable interrupts. To enable an interrupt, set its corresponding bit to 1. To disable an interrupt, set its corresponding bit to 0. Use the PUSH DBGIER instruction to read from the DBGIER and POP DBGIER to write to the DEBIER register. At reset, all the DBGIER bits are set to 0.

Figure 6−11. Debug Interrupt Enable Register (DBGIER) — CPU Register

15	14	13	12	11	10	9	8
RTOSINT	DLOGINT	INT14	INT13	INT12	INT11	INT10	INT9
R/W-0							

7	6	5	4	3	2	1	0
INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1
R/W-0							

Note: R = Read access, W = Write access, –0 = value after reset

Table 6−14. DBGIER Bit Descriptions

Bits	Field	Description
15	RTOSINT	Real-time operating system interrupt enable. RTOSINT enables or disables the CPU RTOS interrupt. 0 Level INT6 is disabled 1 Level INT6 is enabled
14	DLOGINT	Data logging interrupt enable. DLOGINT enables or disables the CPU data logging interrupt. 0 Level INT6 is disabled 1 Level INT6 is enabled
13	INT14	Interrupt 14 enable. INT14 enables or disables CPU interrupt level INT14. 0 Level INT14 is disabled 1 Level INT14 is enabled

Table 6−14. DBGIER Bit Descriptions (continued)

Bits	Field	Description
12	INT13	Interrupt 13 enable. INT13 enables or disables CPU interrupt level INT13. 0 Level INT13 is disabled 1 Level INT13 is enabled
11	INT12	Interrupt 12 enable. INT12 enables or disables CPU interrupt level INT12. 0 Level INT12 is disabled 1 Level INT12 is enabled
10	INT11	Interrupt 11 enable. INT11 enables or disables CPU interrupt level INT11. 0 Level INT11 is disabled 1 Level INT11 is enabled
9	INT10	Interrupt 10 enable. INT10 enables or disables CPU interrupt level INT10. 0 Level INT10 is disabled 1 Level INT10 is enabled
8	INT9	Interrupt 9 enable. INT9 enables or disables CPU interrupt level INT9. 0 Level INT9 is disabled 1 Level INT9 is enabled
7	INT8	Interrupt 8 enable. INT8 enables or disables CPU interrupt level INT8. 0 Level INT8 is disabled 1 Level INT8 is enabled
6	INT7	Interrupt 7 enable. INT7 enables or disables CPU interrupt level INT77. 0 Level INT7 is disabled 1 Level INT7 is enabled
5	INT6	Interrupt 6 enable. INT6 enables or disables CPU interrupt level INT6. 0 Level INT6 is disabled 1 Level INT6 is enabled

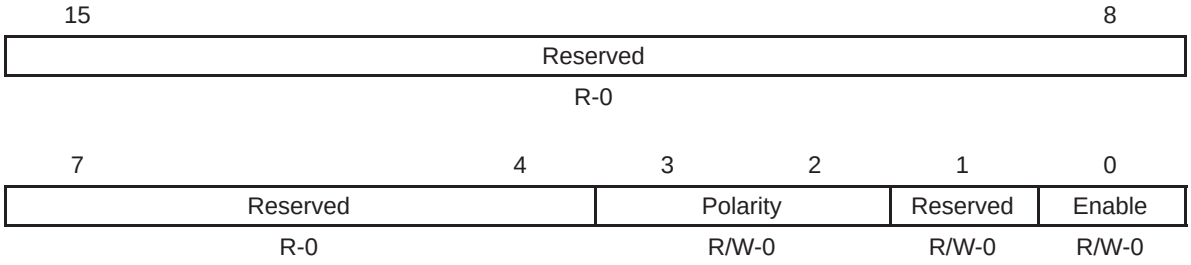
Table 6−14. DBGIER Bit Descriptions (continued)

Bits	Field	Description
4	INT5	Interrupt 5 enable. INT5 enables or disables CPU interrupt level INT5. 0 Level INT5 is disabled 1 Level INT5 is enabled
3	INT4	Interrupt 4 enable. INT4 enables or disables CPU interrupt level INT4. 0 Level INT4 is disabled 1 Level INT4 is enabled
2	INT3	Interrupt 3 enable. INT3 enables or disables CPU interrupt level INT3. 0 Level INT3 is disabled 1 Level INT3 is enabled
1	INT2	Interrupt 2 enable. INT2 enables or disables CPU interrupt level INT2. 0 Level INT2 is disabled 1 Level INT2 is enabled
0	INT1	Interrupt 1 enable. INT1 enables or disables CPU interrupt level INT1. 0 Level INT1 is disabled 1 Level INT1 is enabled

6.6 External Interrupt Control Registers

Some devices support three masked external interrupts XINT1, XINT2, XINT13. XINT13 is multiplexed with one non-maskable interrupt XNMI. Each of these external interrupts can be selected for negative or positive edge triggered and can also be enabled or disabled (including XNMI). The masked interrupts also contain a 16-bit free running up counter that is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time stamp the interrupt.

Figure 6−12. External Interrupt 1 Control Register (XINT1CR) — Address 7070h

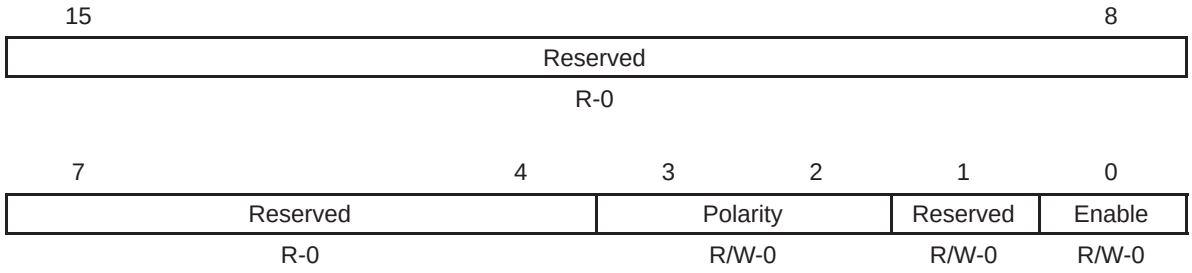


Note: R = Read access, W = Write access, –0 = value after reset

Table 6−15. XINT1CR Bit Descriptions

Bits	Field	Description
15−4	Reserved	Reads return zero; writes have no effect.
3−2	Polarity	This read/write bit determines whether interrupts are generated on the rising edge or the falling edge of a signal on the pin. 00 Interrupt generated on a falling edge (high-to-low transition) 01 Interrupt generated on a rising edge (low-to-high transition) 00 Interrupt generated on a falling edge (high-to-low transition) 01 Interrupt generated on both a falling edge and a rising edge (high-to-low transition and low-to-high transition)
1	Reserved	Reads return zero; writes have no effect
0	Enable	This read/write bit enables or disables external interrupt XINT1. 0 Disable interrupt 1 Enable interrupt

Figure 6−13. External Interrupt 2 Control Register (XINT2CR) — Address 7071h

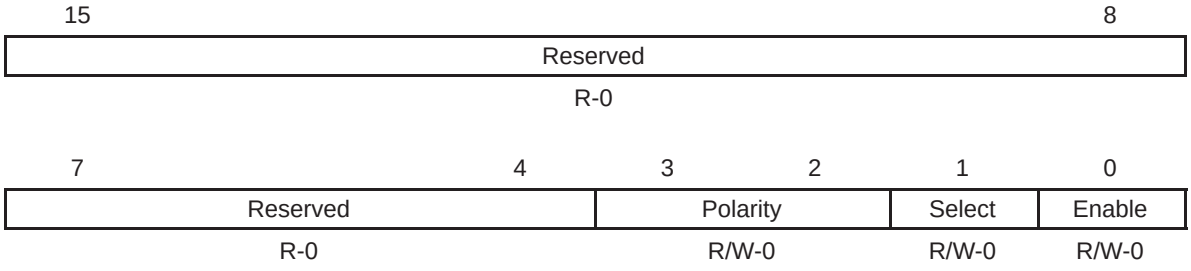


Note: R = Read access, W = Write access, –0 = value after reset

Table 6−16. XINT2CR Bit Descriptions

Bits	Field	Description
15−4	Reserved	Reads return zero; writes have no effect.
3−2	Polarity	This read/write bit determines whether interrupts are generated on the rising edge or the falling edge of a signal on the pin. 00 Interrupt generated on a falling edge (high-to-low transition) 01 Interrupt generated on a rising edge (low-to-high transition) 10 Interrupt is generated on a falling edge (high-to-low transition) 11 Interrupt generated on both a falling edge and a rising edge (high-to-low and low-to-high transition)
1	Reserved	Reads return zero; writes have no effect
0	Enable	This read/write bit enables or disables external interrupt XINT2. Disable interrupt Enable interrupt

Figure 6−14. External NMI Interrupt Control Register (XNMICR) — Address 7077h



Note: R = Read access, W = Write access, –0 = value after reset

Table 6−17. XNMICR Bit Descriptions

Bits	Field	Description
15−4	Reserved	Reads return zero; writes have no effect.
3−2	Polarity	This read/write bit determines whether interrupts are generated on the rising edge or the falling edge of the signal on the pin.
		00 Interrupt generated on a falling edge (high-to-low transition)
		01 Interrupt generated on a rising edge low-to-high transition)
		10 Interrupt is generated on a falling edge (high to low transition)
		11 Interrupt generated on both a falling edge and a rising edge (high to low and low to high transition)
1	Select	Select the source for INT13
		0 Timer 1 connected To INT13
		1 XNMI_XINT13 connected To INT13
0	Enable	This read/write bit enables or disables external interrupt NMI
		0 Disable XNMI interrupt
		1 Enable XNMI interrupt

The XNMI Control Register (XNMICR) can be used to enable or disable the NMI interrupt to the CPU. In addition, you can select the source for the INT13 CPU interrupt. As shown in Figure 6−4, the source of the INT13 interrupt can be either the internal CPU Timer1 or the external GPIO signal assigned to XNMI.

On the F280x devices, CPU Timer1 is reserved for use by TI software. The INT13 interrupt can, however, still be connected to XNMI_XINT13 for customer use.

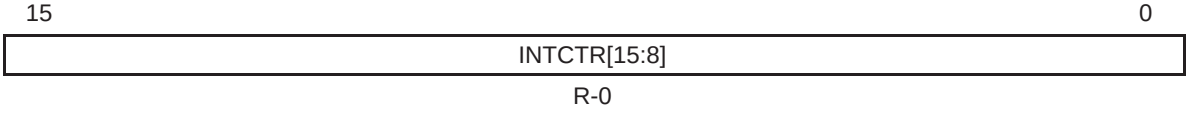
Table 6−18 shows the relationship between the XNMICR Register settings and the interrupt sources to the 28x CPU.

Table 6−18. XNMICR Register Settings and Interrupt Sources

XNMICR	Register Bits	28x CPU Interrupt		Timestamp
ENABLE	SELECT	NMI	INT13	(XNMICTR)
0	0	Disabled	CPU Timer 1	None
0	1	Disabled	XNMI	None
1	0	XNMI	CPU Timer 1	XNMI
1	1	Disabled	XNMI	XNMI

For each external interrupt, there is also a 16-bit counter that is reset to 0x000 whenever an interrupt edge is detected. These counters can be used to accurately time stamp an occurrence of the interrupt.

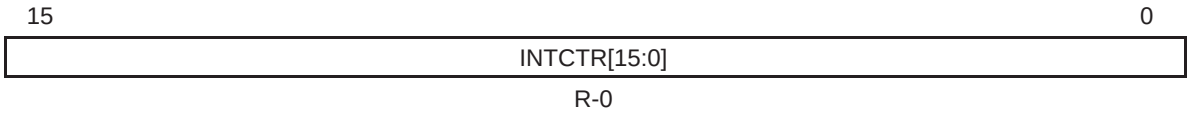
Figure 6−15. External Interrupt 1 Counter (XINT1CTR) — Address 7078h



Note: R = Read access, –0 = value after reset

Bits	Field	Description
15−0	INTCTR	This is a free running 16-bit up-counter that is clocked at the SYSCLKOUT rate. The counter value is reset to 0x0000 when a valid interrupt edge is detected and then continues counting until the next valid interrupt edge is detected. When the interrupt is disabled, the counter stops. The counter is a free-running counter and wraps around to zero when the max value is reached. The counter is a read only register and can only be reset to zero by a valid interrupt edge or by reset.

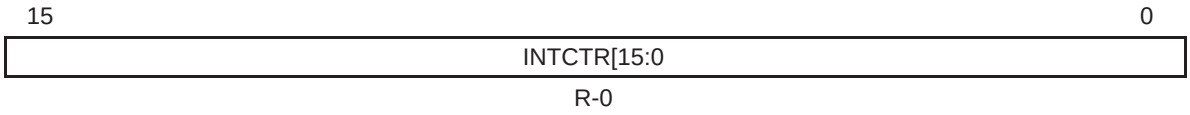
Figure 6−16. External Interrupt 2 Counter (XINT2CTR) — Address 7079h



Note: R = Read access, –0 = value after reset

Bits	Field	Description
15−0	INTCTR	This is a free running 16-bit up-counter that is clocked at the SYSCLKOUT rate. The counter value is reset to 0x0000 when a valid interrupt edge is detected and then continues counting until the next valid interrupt edge is detected. When the interrupt is disabled, the counter stops. The counter is a free-running counter and wraps around to zero when the max value is reached. The counter is a read only register and can only be reset to zero by a valid interrupt edge or by reset.

Figure 6−17. External NMI Interrupt Counter (XNMICTR) — Address 707Fh



Note: R = Read access, –0 = value after reset

Bits	Field	Description
15−0	INTCTR	This is a free running 16-bit up-counter that is clocked at the SYSCLKOUT rate. The counter value is reset to 0x0000 when a valid interrupt edge is detected and then continues counting until the next valid interrupt edge is detected. When the interrupt is disabled, the counter stops. The counter is a free-running counter and wraps around to zero when the max value is reached. The counter is a read only register and can only be reset to zero by a valid interrupt edge or by reset.

This page is intentionally left blank.