TMS320x281x, 280x DSP Peripheral Reference Guide

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TMS320x281x, 280x DSP Peripherals

This overview guide describes all the peripherals available for TMS320x28x devices. Table 1 shows the peripherals used by each device. You can download the peripheral guide by clicking on the literature number, which is linked to the portable document format (pdf) file.

Note:

The 281x EV, SCI, and SPI peripherals are almost identical to those available on the 240x™ devices; however, these modules have enhanced features. See the respective documents for details.

Brief descriptions of the peripherals are included in the following sections.

Table 1. Peripheral Selection Guide

Peripheral	Lit. No.	2812 Device	2811 Device	2810 Device	2808 Device	2806 Device	2801 Device
TMS320x281x System Control and Interrupts	SPRU078	✓	✓	✓			
TMS320x280x System Control and Interrupts	SPRU712				✓	✓	✓
TMS320x281x External Interface (XINTF)	SPRU067	✓					
TMS320x281x, 280x Enhanced Controller Area Network (eCAN)	SPRU074	✓	✓	✓	✓	✓	✓
TMS320x281x Event Manager (EV)	SPRU065	✓	✓	✓			
TMS320x281x Analog-to-Digital Converter (ADC)	SPRU060	✓	✓	✓			
TMS320x280x Analog-to-Digital Converter (ADC)	SPRU716				✓	✓	✓
TMS320x281x Multichannel Buffered Serial Port (McBSP)	SPRU061	✓	✓	✓			
TMS320x281x, 280x Serial Communications Interface (SCI)	SPRU051	✓	✓	✓	✓	✓	✓
TMS320x281x, 280x Serial Peripheral Interface (SPI)	SPRU059	✓	✓	✓	✓	✓	✓
TMS320x281x Boot ROM	SPRU095	✓	✓	✓			
TMS320x280x Boot ROM	SPRU722				✓	✓	✓
TMS320x280x Enhanced Quadrature Encoder Pulse (eQEP)	SPRU790				✓	✓	✓
TMS320x280x Enhanced PWM Module	SPRU791				✓	✓	✓
TMS320x280x Enhanced Capture (eCAP) Module	SPRU807				✓	✓	✓
TMS320x280x Inter-Integrated Circuit (I^2C)	SPRU721				✓	✓	✓

1.1 System Control and Interrupts (different 281x and 280x versions)

The *TMS320x281x System Control and Interrupts Peripheral Guide* (SPRU078) and the *TMS320x280x System Control and Interrupts Peripheral Guide* (SPRU712) include information on the following modules:

- ❑ Memory, including Flash and OTP configuration
- ❑ Code security module (CSM)
- ❑ Clocking, low power modes, watchdog, and CPU-timers
- ❑ General-purpose inputs/outputs (GPIO)
- ❑ Peripheral frames
- ❑ Peripheral interrupt expansion (PIE)

1.1.1 Code Security Module (CSM)

Security is defined with respect to the access of the on-chip program memory and prevents unauthorized copying of proprietary code. The code security module (CSM) blocks access to several on-chip program memory blocks.

1.1.2 Peripheral Clocking

The clocks to each individual peripheral can be enabled/disabled so as to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports and the event managers, CAP and QEP blocks can be scaled relative to the CPU clock. This enables the timing of peripherals to be decoupled from increasing CPU clock speeds.

1.1.2.1 CPU-Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value. CPU-Timers 1 and 2 are reserved for Real-Time OS (RTOS) applications. CPU-Timer 2 is connected to INT14 of the CPU. CPU-Timer 1 can be connected to INT13 of the CPU. CPU-Timer 0 is for general use and is connected to the PIE block.

1.1.2.2 Watchdog Timer

The 28x devices support a watchdog timer. The user software must regularly reset the watchdog counter within a certain time frame; otherwise, the

watchdog generates a reset to the processor. The watchdog can be disabled if necessary.

1.1.3 General-Purpose Input/Output (GPIO) Multiplexer

Most of the peripheral signals are multiplexed with general-purpose I/O (GPIO) signals. This enables you to use a pin as GPIO if the peripheral signal or function is not used. On reset, all GPIO pins are configured as inputs. You can then individually program each pin for GPIO mode or Peripheral Signal mode. For specific inputs, you can also select the number of input qualification cycles to filter unwanted noise glitches.

1.1.4 Peripheral Frames

The 281x and 280x devices contain three peripheral register spaces. Some registers within these frames can be protected from CPU writes by the EALLOW protection mechanism.

1.1.5 Peripheral Interrupt Expansion (PIE) Block

The PIE block multiplexes numerous interrupt sources into a smaller set of interrupt inputs. The interrupts are grouped into blocks of eight and each group is fed into one of 12 CPU interrupt lines ($\overline{\text{INT1}}$ to $\overline{\text{INT12}}$). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. It takes nine CPU clock cycles to fetch the vector and save critical CPU registers. Therefore, the CPU can respond quickly to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the PIE block.

1.2 TMS320x281x External Interface (XINTF) (SPRU067)

The external interface (XINTF) on the 2812 device is a nonmultiplexed asynchronous bus that is used to interface to external devices and memory.

1.3 TMS320x281x, 280x Enhanced Controller Area Network (eCAN) (SPRU074)

This is the enhanced version of the CAN peripheral. It supports 32 mailboxes, time stamping of messages, and is CAN 2.0B-compliant.

1.4 TMS320x281x Event Manager (EV) (SPRU065)

The event manager module includes general-purpose timers, full-compare/pulse-width modulation (PWM) units, capture inputs (CAP) and

quadrature-encoder pulse (QEP) circuits. Two such event managers are provided, which enable two three-phase motors to be driven or four two-phase motors. The event managers on the F2810 and F2812 are compatible to the event managers on the 240x devices (with some minor enhancements).

1.5 TMS320x281x, 280x Analog-to-Digital Converter (ADC) (different 281x and 280x versions)

The ADC block is a 12-bit converter, single ended, 16-channels. It contains two sample-and-hold units for simultaneous sampling. See the *TMS320x281x Analog-to-Digital Converter (ADC) Reference Guide* (literature number SPRU060) or the *TMS320x280x Analog-to-Digital Converter (ADC) Reference Guide* (literature number SPRU712) for details on how to use the ADC for your device.

1.6 TMS320x281x Multichannel Buffered Serial Port (McBSP) (SPRU061)

The McBSP is used to connect to E1/T1 lines, phone-quality codecs for modem applications or high-quality stereo-quality Audio DAC devices. The McBSP receive and transmit registers are supported by a 16-level FIFO. This significantly reduces the overhead for servicing this peripheral.

1.7 TMS320x281x, 280x Serial Communications Interface (SCI) (SPRU051)

The SCI is a two-wire asynchronous serial port, commonly known as UART. On the F2810 and the F2812, the port supports a 16-level, receive and transmit FIFO for reducing servicing overhead.

1.8 TMS320x281x, 280x Serial Peripheral Interface (SPI) (SPRU059)

The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. The port supports a 16-level, receive and transmit FIFO for reducing servicing overhead.

1.9 Boot ROM (different 281x and 280x versions)

The boot ROM is factory-programmable with boot-loading software. Boot-mode signals (general-purpose I/Os) are used to tell the bootloader software

which mode to use. The Boot ROM also contains standard math tables such as SIN/COS for use in IQ math related algorithms. See the *TMS320x281x Boot ROM Reference Guide* (literature number SPRU095) or the *TMS320x280x Boot ROM Reference Guide* (SPRU722) for details.

1.10 TMS320x280x Inter-Integrated Circuit (I2C) (SPRU721)

This guide describes the features and operation of the inter-integrated circuit (I^2C) module that is available on the TMS320x280x digital signal processor (DSP). The I^2C module provides an interface between one of these DSPs and devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus) specification version 2.1 and connected by way of an I^2C-bus. External components attached to this 2-wire serial bus can transmit/receive 1- to 8-bit data to/from the 280x DSP through the I^2C module. This chapter assumes the reader is familiar with the I^2C-bus specification.

1.11 TMS320x280x Enhanced Quadrature Encoder Pulse (eQEP) Module (SPRU790)

The enhanced quadrature encoder pulse (eQEP) module is used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine for use in a high-performance motion and position-control system

1.12 TMS320x280x Enhanced Capture (eCAP) Module (SPRU807)

The enhanced Capture (eCAP) Module is essential in systems where accurate timing of external events is important.

Uses for eCAP include:

- ❏ Speed measurements of rotating machinery (e.g., toothed sprockets sensed via Hall sensors)
- ❏ Elapsed time measurements between position sensor triggers
- ❏ Period and duty cycle measurements of pulse train signals
- ❏ Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

1.13 TMS320x280x Enhanced PWM (ePWM) Module (SPRU791)

The enhanced pulse width modulator (ePWM) peripheral controls many of the power-related systems found in both commercial and industrial equipments.

The main systems include digital motor control, switch mode power supply control, uninterruptible power supplies (UPS), and other forms of power conversion. The PWM peripheral performs a DAC function, where the duty cycle is equivalent to a DAC analog value; it is sometimes referred to as a Power DAC.