## TMS320C27x Instruction Set Simulator

# **Technical Reference**

Literature Number: SPRU603B JULY 2002-Revised OCTOBER 2003



## **Contents**

Pref	ace		5
1	Feat	ures	7
2	Desc	cription	7
3	Sup	ported Hardware Resources	8
	3.1	CPU	8
	3.2	Memory	8
	3.3	Peripherals	8
4	Sup	ported Simulation Features	8
	4.1	Port Connect	8
	4.2	Pin Connect	8
	4.3	Pipeline Display	9
5	Perf	ormance Numbers	9
		List of Figures	
1	C27x	Pipeline Display Plug-In Window	9
		List of Tables	
1	Proce Simu	essors Supported by the C27x lator	7
2	Pins	Supported by the Pin Connect Feature of the C27x Simulator	8
3	Perfo	ormance Numbers of the C27x Simulator	9



## Read This First

## **About This Manual**

This manual provides the following information:

- Names the TMS320C27x<sup>™</sup> digital signal processors (DSPs) that are supported by the TMS320C27x Instruction Set Simulator
- Describes capabilities of the simulator
- · Lists which modules and pins of each device are modeled
- · Provides some benchmarking data

#### **Related Documentation From Texas Instruments**

**TMS320C27x DSP CPU and Instruction Set Reference Guide** (literature number SPRU220) describes the CPU and the assembly language instructions of the TMS320C27x 16-bit fixed- point DSPs. It also describes emulation features available on these DSPs.

#### **Trademarks**

TMS320C27x, Code Composer Studio, TMS320C2000, C27x are trademarks of Texas Instruments.

Intel, Pentium are trademarks of Intel Corporation or its subsidiaries in the United States and other countries.





## Introduction to the TMS320C27x Instruction Set Simulator

The TMS320C27 $x^{TM}$  Instruction Set Simulator, available within the Code Composer Studio<sup>TM</sup> Integrated Development Environment (IDE) for TMS320C2000<sup>TM</sup>, simulates the instruction set of the C27 $x^{TM}$  core.

#### 1 Features

The TMS320C27x simulator supports the following features:

- Included in the Code Composer Studio Integrated Development Environment (IDE) for TMS320C2000
- TMS320C27x CPU full instruction set architecture execution
  - Parallel instruction execution
- Configurable memory simulation
- · Accurate cycle simulation
  - On-chip memory blocks
  - External memory blocks
- Port Connect
  - Supports external data simulation
- Pin Connect
  - Supports external event simulation
- Supports pipeline display

## 2 Description

Table 1 lists the simulator cores and peripherals supported, with the corresponding configuration to be selected under the Import Configuration menu of Code Composer Studio Setup.

Table 1. Processors Supported by the C27x Simulator

Processor	Code Composer Studio IDE Import Configuration
TMS320C27x	C27xx Cycle Accurate Simulator



## 3 Supported Hardware Resources

### 3.1 CPU

Simulation includes the full instruction set architecture (except emulation instructions).

## 3.2 Memory

The simulator provides configurable memory simulation. By default, the simulator does not provide any memory mapping specific to the device or processor. All the memory blocks in Program, Data, and I/O space can be simulated by adding memory blocks using the simulator configuration file. The memory blocks can also be added using the Memory Map Add feature in GEL for debugger visibility.

The simulator provides cycle-accurate simulation for both core and memory blocks. For example, for on-chip memories, the simulator takes care of the number of cycles required to access memory depending on wait states specified by the simulator configuration file.

## 3.3 Peripherals

The simulator does not support any peripherals.

## 4 Supported Simulation Features

## 4.1 Port Connect

The C27x simulator provides the Port Connect feature for Program and Data space for all processor configurations. Before using this feature, make sure that the address being connected to is already mapped by the simulator configuration file. For serial ports, data can be transmitted by connecting some files at the memory mapped locations for the serial port transmit register in write mode. Similarly, data can be received by connecting some files at the memory mapped locations for the serial port receive register in read mode.

## 4.2 Pin Connect

The C27x simulator provides the Pin Connect feature for all processor configurations. The list of pins supported is shown in Table 2.

Table 2. Pins Supported by the Pin Connect Feature of the C27x Simulator

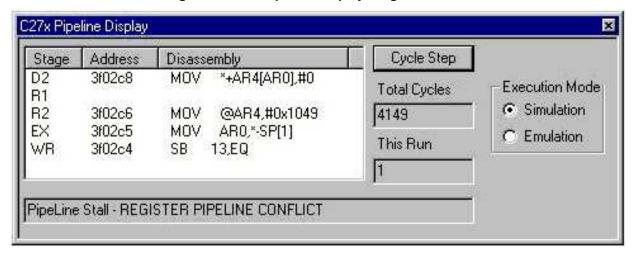
INT1	INT10
INT2	INT11
INT3	INT12
INT4	INT13
INT5	INT14
INT6	DLOGINT
INT7	RTOSINT
INT8	NMI
INT9	EMUINT



## 4.3 Pipeline Display

Figure 1 shows the five stages of the C27x pipeline display plug-in. It also indicates if the pipeline has been stalled due to a register or memory conflict.

Figure 1. C27x Pipeline Display Plug-In Window



## 5 Performance Numbers

Table 3 shows the performance numbers of the simulator. These numbers were gathered on a 900 MHz Intel<sup>™</sup>Pentium<sup>™</sup> III PC with 128MB of RAM. The application used for measurement is rsmbc.

Table 3. Performance Numbers of the C27x Simulator

Simulator Configuration	Simulator Speed (in kilo- cycles/second)
C27xx	175