

***TMS320C6000 DSP
Software-Programmable
Phase-Locked Loop (PLL) Controller
Reference Guide***

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Read This First

About This Manual

This document describes the operation of the software-programmable phase-locked loop (PLL) controller in the digital signal processors (DSPs) of some of the TMS320C6000™ DSP family. Refer to the device-specific datasheet to determine if the PLL controller is used on a particular device.

Notational Conventions

This document uses the following conventions.

- ☐ Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

The following documents describe the C6000™ devices and related support tools. Copies of these documents are available on the Internet at www.ti.com.
Tip: Enter the literature number in the search box provided at www.ti.com.

TMS320C6000 CPU and Instruction Set Reference Guide (literature number SPRU189) describes the TMS320C6000™ CPU architecture, instruction set, pipeline, and interrupts for these digital signal processors.

TMS320C6000 Peripherals Reference Guide (literature number SPRU190) describes the peripherals available on the TMS320C6000™ DSPs.

TMS320C6000 Technical Brief (literature number SPRU197) gives an introduction to the TMS320C62x™ and TMS320C67x™ DSPs, development tools, and third-party support.

TMS320C64x Technical Overview (SPRU395) gives an introduction to the TMS320C64x™ DSP and discusses the application areas that are enhanced by the TMS320C64x VelociTI™.

TMS320C6000 Programmer's Guide (literature number SPRU198) describes ways to optimize C and assembly code for the TMS320C6000™ DSPs and includes application program examples.

TMS320C6000 Code Composer Studio Tutorial (literature number SPRU301) introduces the Code Composer Studio™ integrated development environment and software tools.

Code Composer Studio Application Programming Interface Reference Guide (literature number SPRU321) describes the Code Composer Studio™ application programming interface (API), which allows you to program custom plug-ins for Code Composer.

TMS320C6x Peripheral Support Library Programmer's Reference (literature number SPRU273) describes the contents of the TMS320C6000™ peripheral support library of functions and macros. It lists functions and macros both by header file and alphabetically, provides a complete description of each, and gives code examples to show how they are used.

TMS320C6000 Chip Support Library API Reference Guide (literature number SPRU401) describes a set of application programming interfaces (APIs) used to configure and control the on-chip peripherals.

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Phase-Locked Loop (PLL) Controller

This document describes the operation of the software-programmable phase-locked loop (PLL) controller in the digital signal processors (DSPs) of some of the TMS320C6000™ DSP family. Refer to the device-specific datasheet to determine if the PLL controller is used on a particular device.

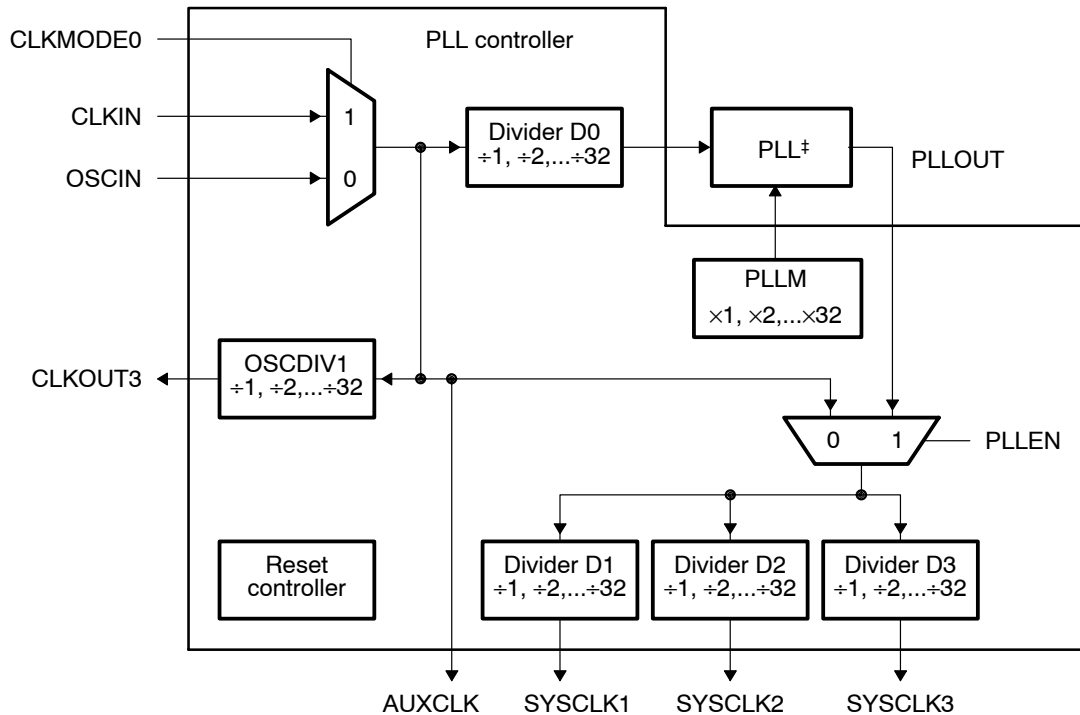
1 Overview

The PLL controller (Figure 1) features software-configurable PLL multiplier controller, dividers (OSCDIV1, D0, D1, D2, and D3), and reset controller. The PLL controller accepts an input clock, as determined by the logic state on the CLKMODE0 pin, from the CLKIN pin or from the on-chip oscillator output signal OSCIN. The PLL controller offers flexibility and convenience by way of software-configurable multiplier and dividers to modify the input signal internally. The resulting clock outputs are passed to the DSP core, peripherals, and other modules inside the C6000™ DSP.

- ☐ The input reference clocks to the PLL controller:
 - CLKIN: input signal from external oscillator (3.3V), CLKMODE0 = 1
 - OSCIN: output signal from on-chip oscillator (1.2V), CLKMODE0 = 0
- ☐ The resulting output clocks from the PLL controller:
 - AUXCLK: internal clock output signal directly from CLKIN or OSCIN.
 - CLKOUT3: output of divider OSCDIV1.
 - SYSCLK1: internal clock output of divider D1.
 - SYSCLK2: internal clock output of divider D2.
 - SYSCLK3: internal clock output of divider D3.

Refer to your device-specific datasheet on how these inputs and outputs of the PLL controller are used. Some devices may not support all of the above clocks.

Figure 1. PLL Controller Block Diagram†



† See the device-specific datasheet for the clocks supported. Some devices may not support all clock inputs/outputs.

‡ See the device-specific datasheet for more details about the PLL.

2 Functional Description

The following sections describe the multiplier, dividers, and reset controller in the PLL controller.

2.1 Multiplier and Dividers

The PLL controller is capable of programming the PLL through the PLL multiplier control register (PLLM) from a $\times 1$ to $\times 32$ multiplier rate (see the device-specific datasheet for the PLL multiplier rates supported on your device). The clock dividers (OSCDIV1, D0, D1, D2, and D3) are programmable from $\div 1$ to $\div 32$ divider ratio and may be disabled. When a clock divider is disabled, no clock is output from that clock divider. A divider only outputs a clock when it is enabled in the corresponding OSCDIV1 or PLLDIV n registers.

The input reference clock (either CLKIN or OSCIN) is directly output as the auxiliary clock (AUXCLK) for use by some peripherals. For example, the multi-channel audio serial port (McASP) uses AUXCLK to generate audio clocks. In addition to AUXCLK, the input reference clock is directly input to the oscillator divider (OSCDIV1). If OSCDIV1 is enabled, OD1EN = 1, the input reference clock is divided down by the value in the oscillator divider ratio bits (RATIO) in OSCDIV1. The output from OSCDIV1 is the output clock CLKOUT3.

The divider D0 and the PLL may also be bypassed. The PLL enable bit (PLEN) in the PLL control/status register (PLLCR) determines the PLL controller mode. When PLEN = 1, PLL mode, D0 and PLL are used; when PLEN = 0, bypass mode, D0 and PLL are bypassed and the input reference clock is directly input to dividers D1, D2, and D3.

When in PLL mode (PLEN = 1), the input reference clock is supplied to divider D0. If D0 is enabled, D0EN = 1, the input reference clock is divided down by the value in the PLL divider ratio bits (RATIO) in PLLDIV0. The output from divider D0 is input to the PLL. The PLL multiplies the clock by the value in the PLL multiplier bits (PLLM) in the PLL multiplier control register (PLLM). The output from the PLL (PLLOUT) is input to dividers D1, D2, and D3.

When enabled (D n EN = 1), the dividers D1, D2, and D3 divide down by the value in RATIO in PLLDIV n the output clock of the PLL. The output clocks of dividers D1, D2, and D3 have 50% duty cycle and are SYSCLK1, SYSCLK2, and SYSCLK3, respectively.

2.2 Reset Controller

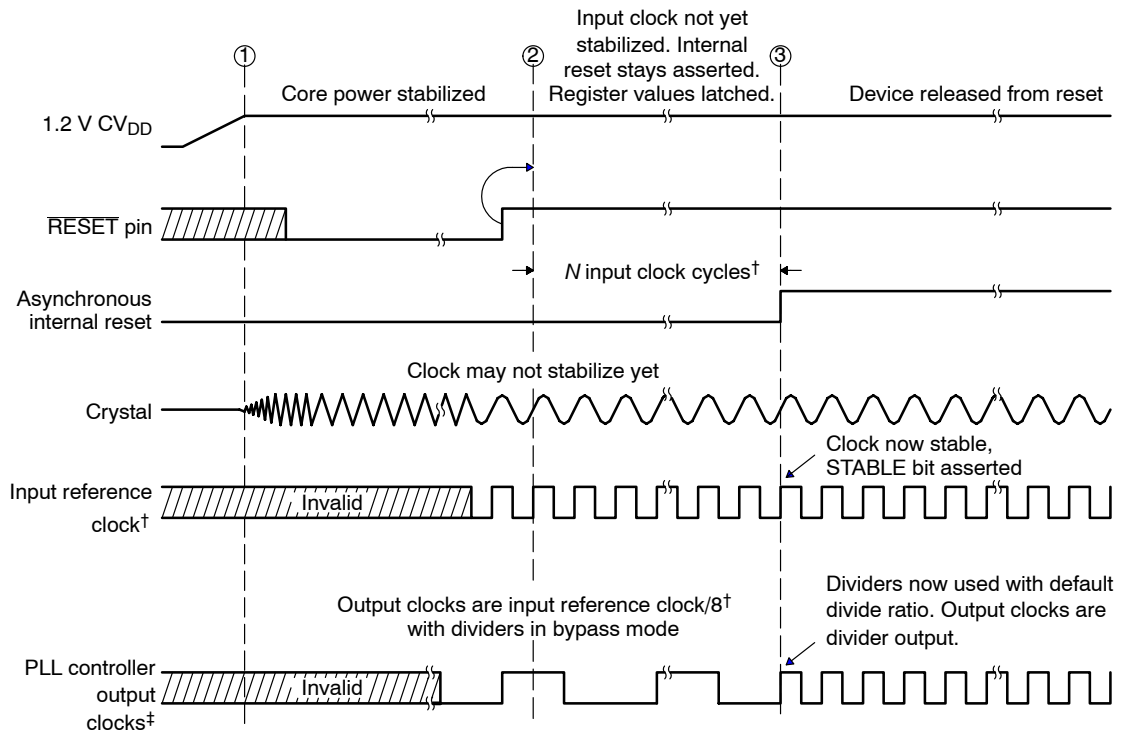
At power up, the device $\overline{\text{RESET}}$ signal may not be asserted long enough to wait for the on-chip or off-chip oscillator to stabilize. This means the input reference clock (either CLKIN or OSCIN) may be a bad clock when a device $\overline{\text{RESET}}$ signal is deasserted high. After $\overline{\text{RESET}}$ is deasserted, the reset controller lengthens the asynchronous internal reset signal to ensure that the input clock source is stable.

The reset controller resides within the PLL controller and the main function is to internally lengthen the reset signal from the $\overline{\text{RESET}}$ input pin until the input clock source is stable (after 512 CLKIN cycles or 4096 OSCIN cycles). This is to ensure that the rest of the device will see the internal reset deasserted only after the input clock is stabilized. Figure 2 shows the lengthening of the internal reset signal.

The PLL controller multiplier and dividers are bypassed when the internal reset signal is low. The frequency of all clock outputs of the PLL controller (AUXCLK, SYSCLK1, SYSCLK2, SYSCLK3, and CLKOUT3) are fixed to the input reference clock (CLKIN or OSCIN) divided by 8. After 512 CLKIN cycles or 4096 OSCIN cycles, the reset controller brings the device out of reset and sets the oscillator input stable bit (STABLE) in the PLL control/status register (PLLCSR). The dividers are used after this point and are set to their default divide ratio.

Values are latched into the registers at the rising edge of $\overline{\text{RESET}}$.

Figure 2. Reset Controller Lengthening the Internal Reset Signal



[†] $N = 512 \times \text{CLKIN}$ cycles when $\text{CLKMODE} = 1$ (input reference clock is CLKIN);

$N = 4096 \times \text{OSCIN}$ cycles when $\text{CLKMODE} = 0$ (input reference clock is OSCIN)

[‡] Output clocks include AUXCLK, SYSCLK1, SYSCLK2, SYSCLK3, and CLKOUT3 at the PLL controller boundary. Refer to the device-specific datasheet for clock behavior at the device pins.

3 Configuration

The following sections provide procedures for initialization, power down, and wake up of the PLL controller.

3.1 Initialization

The PLL and PLL controller are to be initialized by software after reset. The PLL controller registers should be modified only by the CPU or via emulation. The HPI should not be used to directly access the PLL controller registers. The initialization of the PLL controller should be performed as soon as possible at the beginning of the program, before initializing any peripherals. Upon device reset, one of the following two software initialization procedures must be done to properly set up the PLL and PLL controller.

3.1.1 PLL Mode (PLEN = 1)

If the system intends to use divider D0 and PLL, perform the following:

- 1) In PLLCSR, write PLEN = 0 (bypass mode).
- 2) Wait 4 cycles of the slowest of PLLOUT, CLKIN (if CLKMODE = 1), and OSCIN (if CLKMODE = 0).
- 3) In PLLCSR, write PLLRST = 1 (PLL is reset).
- 4) Program PLLDIV0, PLLM, and OSCDIV1.
- 5) Program PLLDIV1-3. Note that there must be wait states between accesses to PLLDIV1-3. Each wait state is 8 cycles of the slowest of the old and new SYSCLK1-3 clock rates. Some devices may also require users to program the PLLDIV1-3 registers in a particular order, to ensure no violation of system clock ratios. See PLL Controller section of the device-specific datasheet for other restrictions.
- 6) Wait for PLL to properly reset. See device-specific datasheet for PLL reset time.
- 7) In PLLCSR, write PLLRST = 0 to bring PLL out of reset.
- 8) Wait for PLL to lock. See device-specific datasheet for PLL lock time.
- 9) In PLLCSR, write PLEN = 1 to enable PLL mode.

Steps 1, 2, and 3 are required when PLEN and PLLRST bits are not already 0 and 1, respectively. These steps are not required when the device is coming out of reset (they are performed by hardware).

3.1.2 Bypass Mode (PLEN = 0)

If the system intends to bypass divider D0 and PLL, perform the following:

- 1) In PLLCSR, write PLEN = 0 (bypass mode).
- 2) Wait 4 cycles of the slowest of PLLOUT, CLKIN (if CLKMODE = 1), and OSCIN (if CLKMODE = 0).
- 3) In PLLCSR, write PLLRST = 1 (PLL is reset).
- 4) Program OSCDIV1.
- 5) Program PLLDIV1-3. Note that there must be wait states between accesses to PLLDIV1-3. Each wait state is 8 cycles of the slowest of the old and new SYSCLK1-3 clock rates. See PLL Controller section of the device-specific datasheet for other restrictions.

Steps 1, 2, and 3 are required when PLEN and PLLRST bits are not already 0 and 1, respectively. These steps are not required when the device is coming out of reset (they are performed by hardware).

3.2 Power Down

The PLL may be powered down, in which case the PLL controller is in bypass mode and the DSP runs from a divided down version of the input reference clock. The DSP is still able to respond to events because it is still being clocked by the bypass clock (directly from CLKIN or OSCIN), although at a lower frequency.

Perform the following procedure to power down the PLL:

- 1) In PLLCSR, write PLEN = 0 (bypass mode).
- 2) Wait 4 cycles of the slowest of PLLOUT, CLKIN (if CLKMODE = 1), and OSCIN (if CLKMODE = 0).
- 3) In PLLCSR, write PLLPWRDN = 1 to power down the PLL.

3.3 Power Wake Up

Perform the following procedure to wake up the PLL from its power-down mode:

- 1) In PLLCSR, write PLEN = 0 (bypass mode).
- 2) Wait 4 cycles of the slowest of PLLOUT, CLKIN (if CLKMODE = 1), and OSCIN (if CLKMODE = 0).
- 3) In PLLCSR, write PLLPWRDN = 0 to wake up the PLL.
- 4) Follow the reset sequence described in section 3.1.

4 Registers

The PLL controller registers configure the operation of the PLL controller. The PLL controller registers are listed in Table 1. See the device-specific datasheet for the memory address of these registers.

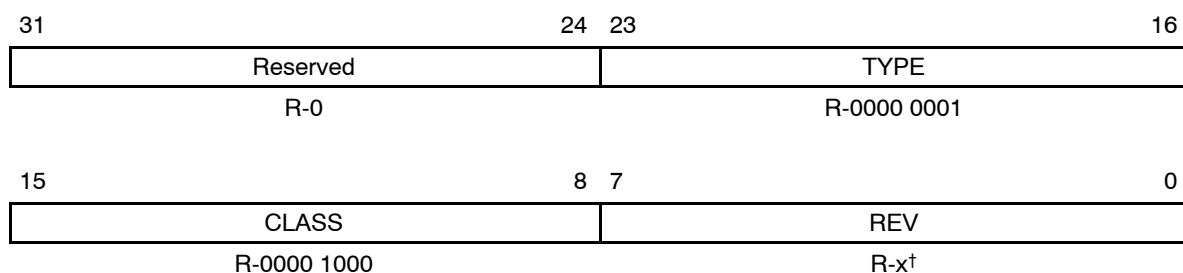
Table 1. PLL Controller Registers

Acronym	Register Name	Section
PLLPID	PLL controller peripheral identification register	4.1
PLLCSR	PLL control/status register	4.2
PLLM	PLL multiplier control register	4.3
PLLDIV0-3	PLL controller divider registers	4.4
OSCDIV1	Oscillator divider 1 register	4.5

4.1 PLL Controller Peripheral Identification Register (PLLPID)

The PLL controller peripheral identification register (PLLPID) contains identification code for the PLL controller. PLLPID is shown in Figure 3 and described in Table 2.

Figure 3. PLL Controller Peripheral Identification Register (PLLPID)



Legend: R = Read only; -x = value after reset

[†] See the device-specific datasheet for the default value of this field.

Table 2. PLL Controller Peripheral Identification Register (PLLPID) Field Descriptions

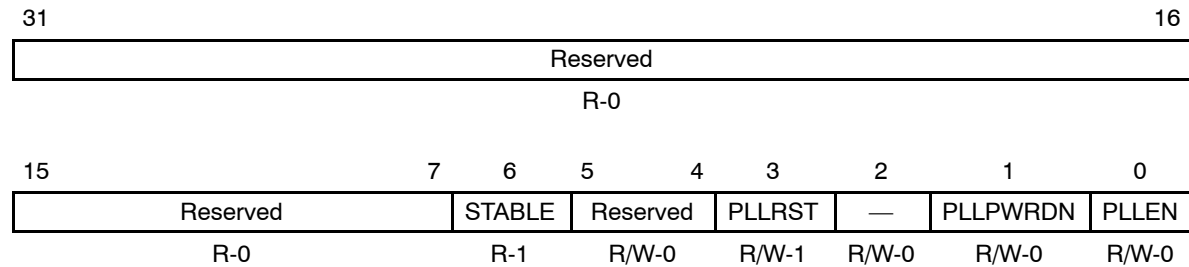
Bit	field [†]	symval [†]	Value	Description
31-24	Reserved	–	0	These reserved bit locations are always read as 0. A value written to this field has no effect.
23-16	TYPE	OF(value)	01h	Identifies type of peripheral. PLL controller
15-8	CLASS	OF(value)	08h	Identifies class of peripheral. Serial port
7-0	REV	OF(value)	x	Identifies revision of peripheral. See the device-specific datasheet for the value.

[†] For CSL implementation, use the notation PLL_PID_field_symval

4.2 PLL Control/Status Register (PLLCSR)

The PLL control/status register (PLLCSR) is shown in Figure 4 and described in Table 3.

Figure 4. PLL Control/Status Register (PLLCSR)



Legend: R = Read only; R/W = Read/write; -n = value after reset

Table 3. PLL Control/Status Register (PLLCSR) Field Descriptions

Bit	field [†]	symval [†]	Value	Description
31-7	Reserved	–	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
6	STABLE	OF(value)	0	Oscillator input stable bit indicates if the OSCIN/CLKIN input has stabilized. The STABLE bit is set to 1 after the reset controller counts 4096 OSCIN or 512 CLKIN input clock cycles after the RESET signal is asserted high. It is assumed that the OSCIN/CLKIN input is stabilized after this number of cycles.
			0	OSCIN/CLKIN input is not yet stable. Oscillator counter is not finished counting.
			1	Oscillator counter is done counting and OSCIN/CLKIN input is assumed to be stable.
5-4	Reserved	–	0	Reserved. The reserved bit location is always read as 0. Always write a 0 to this location.
3	PLLRST			PLL reset bit.
		0	0	PLL reset is released.
		1	1	PLL reset is asserted.
2	Reserved	–	0	Reserved. The reserved bit location is always read as 0. Always write a 0 to this location.

[†] For CSL implementation, use the notation PLL_PLLCSR_field_symval

Table 3. PLL Control/Status Register (PLLCSR) Field Descriptions (Continued)

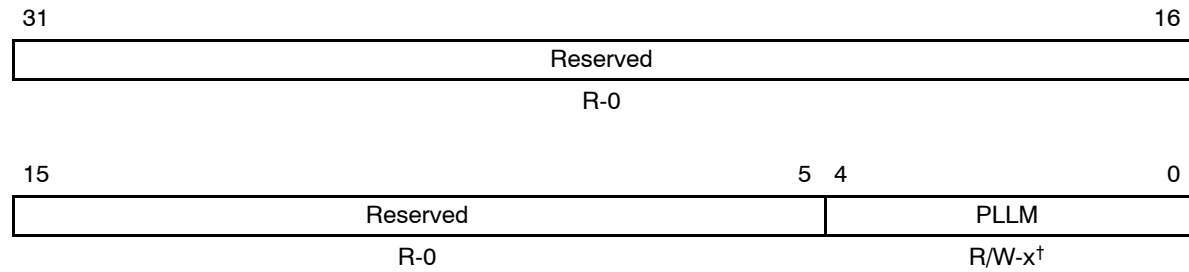
Bit	field [†]	symval [†]	Value	Description
1	PLLWRDN			PLL power-down mode select bit.
		NO	0	PLL is operational.
		YES	1	PLL is placed in power-down state.
0	PLLEN			PLL enable bit.
		BYPASS	0	Bypass mode. Divider D0 and PLL are bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down directly from input reference clock.
		ENABLE	1	PLL mode. PLL output path is enabled. Divider D0 and PLL are not bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down from PLL output.

[†] For CSL implementation, use the notation PLL_PLLCSR_field_symval

4.3 PLL Multiplier Control Register (PLLM)

The PLL multiplier control register (PLLM) is shown in Figure 5 and described in Table 4. The PLLM defines the input reference clock frequency multiplier in conjunction with the PLL divider ratio bits (RATIO) in the PLL controller divider 0 register (PLLDIV0).

Figure 5. PLL Multiplier Control Register (PLLM)



Legend: R = Read only; R/W = Read/write; -n = value after reset

† Refer to the device-specific datasheet for the reset value of this field.

Table 4. PLL Multiplier Control Register (PLLM) Field Descriptions

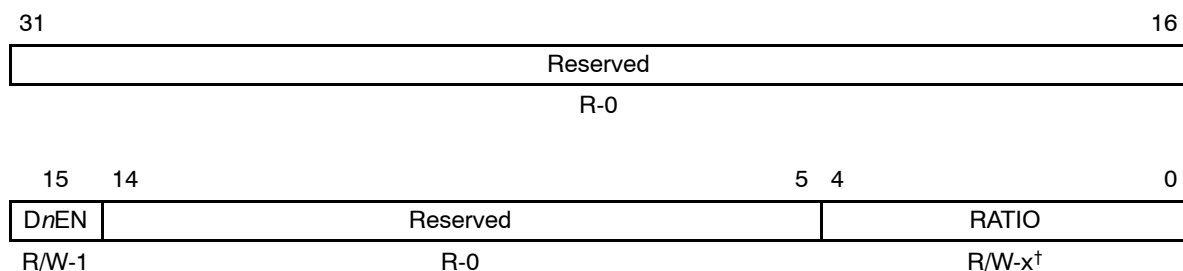
Bit	Field	symval [†]	Value	Description
31-5	Reserved	–	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
4-0	PLLM	OF(value)	0-1Fh	PLL multiplier bits. Defines the frequency multiplier of the input reference clock in conjunction with the PLL divider ratio bits (RATIO) in PLLDIV0. See the device-specific datasheet for the PLL multiplier rates supported on your device.

[†] For CSL implementation, use the notation PLL_PLLM_PLLM_symval

4.4 PLL Controller Divider Registers (PLLDIV0-3)

The PLL controller divider register (PLLDIV) is shown in Figure 6 and described in Table 5.

Figure 6. PLL Controller Divider Register (PLLDIV)



Legend: R = Read only; R/W = Read/write; -n = value after reset

† Refer to the device-specific datasheet for the reset value of this field.

Table 5. PLL Controller Divider Register (PLLDIV) Field Descriptions

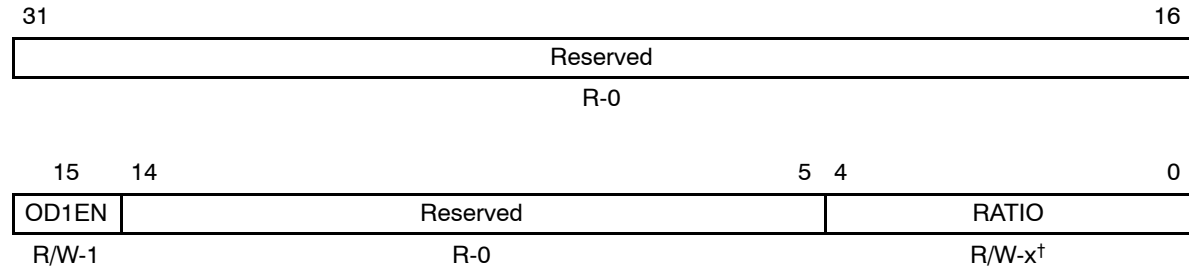
Bit	field†	symval†	Value	Description
31-16	Reserved	–	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15	DnEN			Divider Dn enable bit.
		DISABLE	0	Divider n is disabled. No clock output.
		ENABLE	1	Divider n is enabled.
14-5	Reserved	–	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
4-0	RATIO	OF(value)		Divider ratio bits.
			0	÷1. Divide frequency by 1.
			1h	÷2. Divide frequency by 2.
			2h-1Fh	÷3 to ÷32. Divide frequency by 3 to divide frequency by 32.

† For CSL implementation, use the notation PLL_PLLDIVn_field_symval

4.5 Oscillator Divider 1 Register (OSCDIV1)

The oscillator divider 1 register (OSCDIV1) is shown in Figure 7 and described in Table 6.

Figure 7. Oscillator Divider 1 Register (OSCDIV1)



Legend: R = Read only; R/W = Read/write; -n = value after reset

† Refer to the device-specific datasheet for the reset value of this field.

Table 6. Oscillator Divider 1 Register (OSCDIV1) Field Descriptions

Bit	field†	symval†	Value	Description
31-16	Reserved	–	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15	OD1EN			Oscillator divider 1 enable bit.
		DISABLE	0	Oscillator divider 1 is disabled. No clock output.
		ENABLE	1	Oscillator divider 1 is enabled.
14-5	Reserved	–	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
4-0	RATIO	OF(value)		Oscillator divider 1 ratio bits. Defines the frequency divider ratio for output clock CLKOUT3.
			0	÷1. Divide frequency by 1.
			1h	÷2. Divide frequency by 2.
			2h-1Fh	÷3 to ÷32. Divide frequency by 3 to divide frequency by 32.

† For CSL implementation, use the notation PLL_OSCDIV1_field_symval

Revision History

Table 7 lists the changes made since the previous version of this document.

Table 7. *Document Revision History*

Page	Additions/Modifications/Deletions
Global	Removed device-specific references, instructed users to refer to the device-specific datasheet to determine if the PLL controller is used on a particular device.
7	In section 1, Overview, added sentence to last paragraph: Some devices may not support all of the above clocks.
8	In Figure 1, added footnote: See the device-specific datasheet for the clocks supported. Some devices may not support all clock inputs/outputs.
9	In first paragraph of section 2.1: removed information regarding OD1EN and dividers, and added information regarding clock dividers and clock output.
11	In Figure 2, changed signal from Output clocks to PLL controller output clocks, and added more information to second footnote: Output clocks include AUXCLK, SYSCLK1, SYSCLK2, SYSCLK3, and CLKOUT3 at the PLL controller boundary. Refer to the device-specific datasheet for clock behavior at the device pins.
15	In Table 2, changed bit values for TYPE bit to 01h and CLASS bit to 08h.
16	In Table 3, updated description of STABLE bit.
18	In Figure 5, changed reset value of PLLM bit and added footnote: Refer to the device-specific datasheet for the reset value of this field.
19	In Figure 6, changed reset value of RATIO bit and added footnote: Refer to the device-specific datasheet for the reset value of this field.
19	In Table 5, updated description of RATIO bit.
20	In Figure 7, changed reset value of RATIO bit and added footnote : Refer to the device-specific datasheet for the reset value of this field.
20	In Table 6, updated description of RATIO bit.

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